Study on Heterostructure Semiconductor Devices Using Grafting Technique

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To my family

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Abstract

In this thesis, the approaches of forming heterostructure schematics for III-V silicon tandem solar cell, Si/GaN diode, and III-V/diamond HBTs have been explored. The current challenges in forming heterostructure using arbitrary types of semiconductors have been investigated using the semiconductor grafting technique, which is available to combine two semiconductors without considering lattice mismatch. Devices in which heterostructures are employed are widely used in our modern life; however, forming heterostructure between two arbitrary types of semiconductors without considering lattice match has not yet been achieved despite many attempts six decades. Heterostructure involving arbitrary semiconductor combination will potentially open many opportunities for material engineering and enable much broader applications–photonic devices, optical devices, and power devices.

In the first part of this thesis, a novel way to fabricate heterogeneous electronics that imitate plant grafting in nature, named by "semiconductor grafting technique, " is introduced with a brief explanation of heterostructure in terms of high efficiency, high speed, and high power applications. Moreover, one of the current research trends is the wideband gap material—GaN, Diamond, Etc.—will be presented to meet the future demand such as an autonomous vehicle system, various wireless applications, satellite system, clouding storage system, artificial intelligence (AI) computing, various sensors and so on.

The second part of the thesis will cover overcoming the efficiency limit of silicon solar cells using III-V/Silicon tandem structure. By employing semiconductor grafting techniques, two solar cells based on silicon and III-V material are directly bonded. By considering total cost, expensive III-V wafers are recycled using the ELO (epitaxial lift-off) process. The bonding interface with an ultrathin Al_2O_3 layer is optically transparent, and thermally and electrically

conductive. Besides, the whole fabrication process is compatible with the conventional CMOS fabrication process, making the technology exploited easily by commercial production lines to achieve mass production. Furthermore, the performance of the tandem solar cells have been improved to the extent of these performance parameters: conversion efficiency (η) of 30.2% with fill factor (*FF*) of 68%, open-circuit voltage (V_{OC}) of 1.63V, and short circuit current density (J_{SC}) of 28.48mA/cm^2.

The third part of the thesis will present Si/GaN heterogeneous structure diodes with their performance. Silicon, one of the chosen materials in this chapter, is cheap, abundant, widely known material and the most extensively used semiconductor material in semiconductor electronics. Another material, GaN, has been a desirable wide bandgap semiconductor material due to its superior electrical and mechanical properties. This chapter has conducted several analyses, such as XRD, TEM, AFM, Raman spectroscopy, to verify the interface quality and junction formation by the semiconductor grafting technique. Also, the pSi/nGaN diode was fabricated to check their performance, which presents the lowest ideality factor of 1.14 and highest I_{ON}/I_{OFF} ratio of 1.18x10^7 at ±1 V. Overall, the diamond-wurtzite heterostructure diode formed with p+Si NM grafted on n-type GaN fabricated by the semiconductor grafting technique with the ultrathin Al_2O_3 tunneling layer has been successfully demonstrated.

The fourth part of the thesis will cover electronics beyond two-port passive devices such as HBTs (heterojunction bipolar transistors) with GaAs/AlGaAs/Diamond. Diamond is one of the most prospective materials in nature. Diamond has superior properties—high bandgap (5.47 eV), high critical electric field (7.7 - 20 MV/ cm), which allows operation at high voltages, the high thermal conductivity (~ 22 W/cm·K at RT). It means that the power devices have their intrinsic heat spreader leading to high heat dissipation efficiency during operation, and high hole mobility

(> 2000 cm^2/ V·s), which allows high-speed, high-frequency operation and low dielectric constant (5.7) which able to improve the high-frequency characteristics. The III-V materials, AlGaAs/GaAs, are used as an emitter and base, respectively, due to its high speed and linearity characteristic. By combining diamond and III-V material as a collect, emitter, and base, we can meet the demand of smaller and faster microelectronic devices with high power operation. In this part, the current trend of diamond device applications—Schottky diode and FETs will be introduced, and later basic theme and performance of HBTs with AlGaAs/GaAs/diamond will be presented.

Finally, the last part of the thesis will sum up all the results briefly, and the future direction will be presented. Shortly, obtaining a large arbitrary heterogeneous structure with reliability will satisfy the needs for future applications that require high speed and high power in cutting-edge technologies, including autonomous vehicle systems.

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CHAPTER 1

Introduction

1.1. Heterostructure for high efficiency, high speed, and high power applications

The structures involving more than one kind of material are called a heterostructure. The semiconductor heterostructure is one of the most important inventions in the last century that have deeply impacted human society [1]. For semiconductor device applications, the difference in energy gaps provides another degree of freedom. For the case of a homostructure, the current gain is only related to doping concentrations of emitter and base. However, for a heterostructure, the energy bandgap difference leads to a potential advantage in the gain, which would increase exponentially in proportion to the band offset value. This advantage results in tandem solar-cell with high efficiency, high-speed switching devices, and high-power transistors [2]. In order to form heterostructures using semiconductors, a lattice mismatch is an essential requirement. Figure 1.1 shows the crystal orientation illustration of Si and GaN heterostructure. Between the Si and GaN, there is a noticeable difference in the lattice constants. Traditionally, heterostructures are formed by the epitaxial growth technology between lattice-matched semiconductors, slightly lattice-mismatched semiconductors, and lattice-mismatched semiconductors with graded layer to reduce the defects at the interface [3-8].

We should take lattice constant, strain, and critical layer thickness of those semiconductors involved into account during the growth process. [9-11]. Figure 1.2 represents the essential kinds of binary-cubic semiconductors' energy bandgaps versus their lattice constant at 300°K. The right-hand scale gives the light wavelength λ, corresponding to the bandgap energy [12]. Despite the massive success of lattice-matched heterostructures, forming heterostructures between two arbitrary types of semiconductors not restricted by the lattice match condition has been sought after and attempted for over six decades without success. Because it would potentially open a much larger space for materials engineering, and enable much broader kinds of applications than lattice-matched applications, By using the conventional growth method, forming heterostructure between two large lattice-mismatched semiconductors is extremely difficult to obtain a single crystal semiconductor without degrading interface quality [13]. Moreover, the combination of heteroepitaxial growth is limited to binary, ternary, and quaternary alloys of lattice-matched III-V compound materials. Thus, combining semiconductors from different groups such as III-V and II-IV was considered almost impossible.

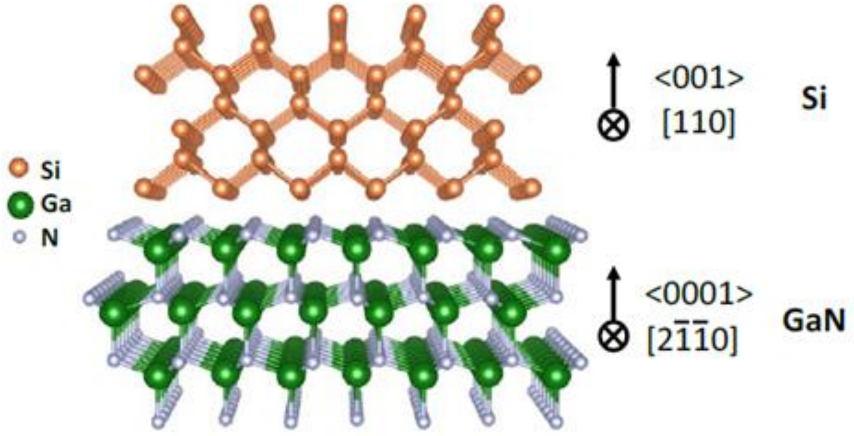

Figure 1.1 *Crystal orientation illustration of Si and GaN heterostructure.*

Many research groups have been studied in several ways—wafer bonding and wafer fusion to combine arbitrary semiconductors without concern of lattice match [14-17]. Wafer bonding provides another degree of freedom to bond different lattice-mismatched materials. From the wafer bonding technique, III-V materials can be combined with silicon or III-Nitride materials, which can be used for HBTs (Heterojunction Bipolar Transistor), photodiode, tandem solar cells, and so one [18-20]. However, high temperature and high pressure are necessary to put the different semiconductors together [16]. These processes lead to an increase in the interfacial layer thickness with an amorphous layer formed, and defect densities increased between the junctions. Not only the quality of junctions but also tunneling current path matter, those problems are critical for junction applications such as a tandem solar cell. The thicker amorphous layers produce defect cites between the bonding interface, increasing the density of the generation-recombination center, which is mainly an issue preventing a reduction of the tunneling probability and, finally, degrades the performance of devices [21]. Moreover, due to the different thermal expansion coefficients of arbitrary semiconductor materials, the wafer bonding process with different wafer sizes is limited. This process causes mechanical stress between the interface and may create void or cracks [22].

At this point, we have introduced and intensely studied another method involving the dramatic change in forming heterostructures of semiconductors, which we name by "Semiconductor Grafting."

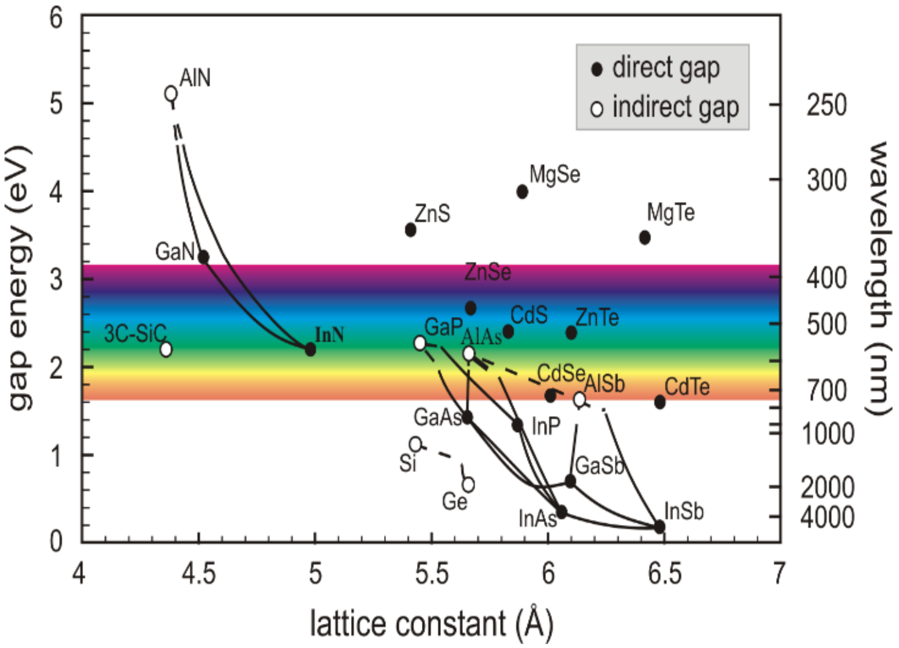

Figure 1.2 *Bandgaps of the most essential elemental and binary cubic semiconductors versus their lattice constant at 300°K. The right-hand scale gives the light wavelength λ, corresponding to the bandgap energy [12].*

1.2. Semiconductor Grafting technique

What is grafting in nature? Grafting is a horticultural technique by which small pieces of plants are joined to continue growing up together. There are two parts called scion and rootstock. The scion is the upper part that is selected for its stems, leaves, flowers, or fruit, while the rootstock is the lower part for roots. This joining method's success is possible by the presumption that the vascular tissues can grow together with an inter-material to attach one part to one another, such as glue, bandage, and tubes. Figure 1.3 shows the schematic diagram of the cabbage tube grafting method. For grafting, the cabbage and kale seedlings were used as (A) a scion and (B) a rootstock, respectively [23]. Grafting technique is commonly used in the asexual propagation of commercially grown plants—the reason why a horticulturist graft is used because the advantages of both kinds of plants are guaranteed. Combining high yield fruit and well-immunized root make super yields. As shown in Figure 1.4, there is a fascinating example: the combination of tomatoes and potatoes, Ketchup’n Fries.

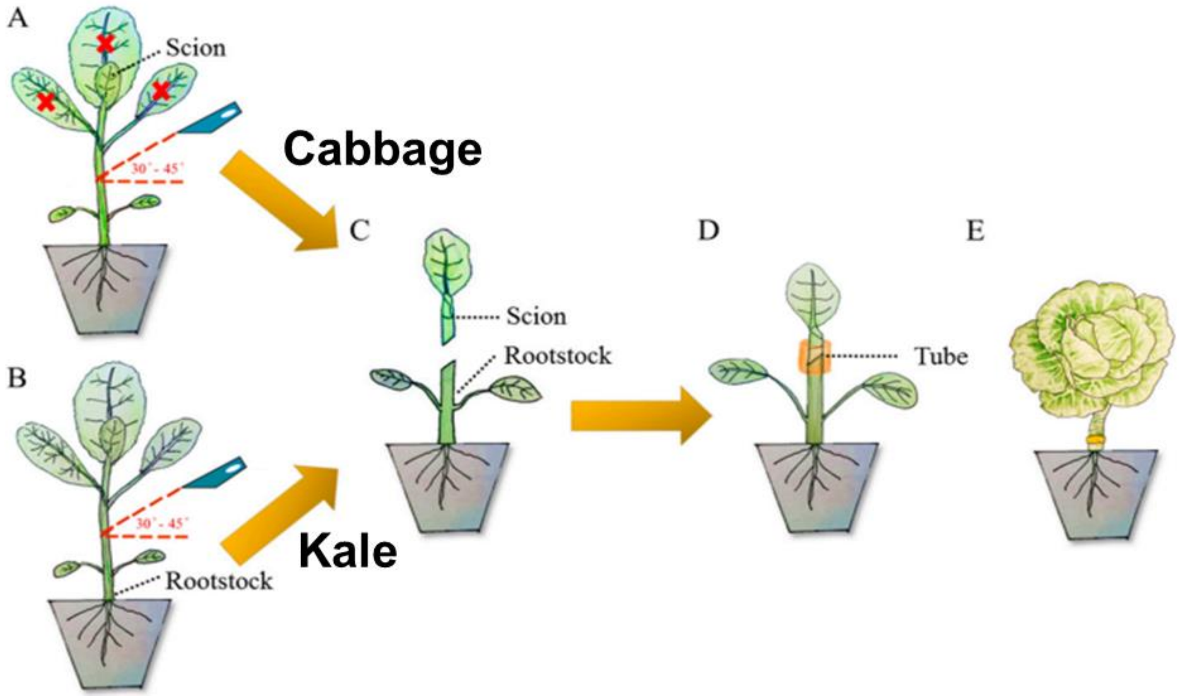

***Figure 1.3** Schematic diagram of the cabbage tube grafting method. For grafting, the cabbage and kale seedlings were used as (A) a scion and (B) a rootstock, respectively* [23].

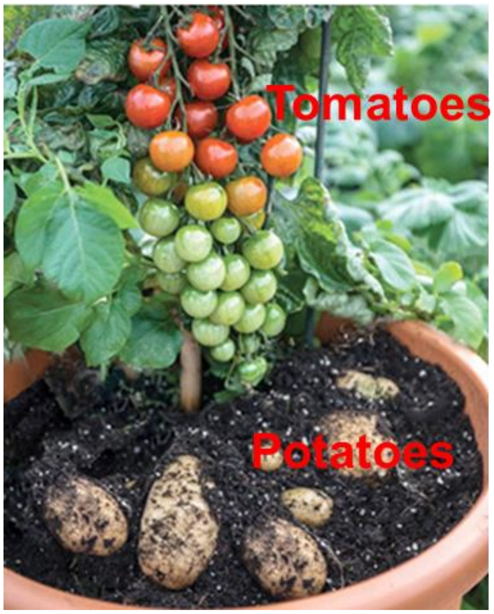

Figure 1.4 *The example of a grafting plant was joined tomatoes and potatoes called "Ketchup' n Fries."*

Now, we can apply this extraordinary technique to applications of semiconductor electronics. Today, high-speed applications based on III-V compound semiconductors are used in high-frequency radio equipment such as mobile communication terminals. Also, it can be used in fast switching devices in digital circuits. GaAs-based-transistors have merits of the best cost/performance ratios, which brings them to have a strong position in the market for device mass-production to meet the modern telecommunication society's enormous demands. In the meantime, the increasing need for microelectronic devices operating at high power, high frequency, and high temperature present a continuous challenge for semiconductor materials to approach large bandgap materials such as GaN, SiC, and Diamond. Traditional semiconductors (e.g., Si, Ge, and GaAs) already meet their theoretical limits and can no longer meet the industry's increasing power, frequency, and temperature handling requirements [24-27].

For trying to solve this problem and exploit the advantages of III-V materials and large bandgap material, the semiconductor grafting technique can be used to form heterostructure. Here is an example: We can suppose some fruit for high-speed III-V material, and root for large bandgap material to get high voltage application, and finally, we can use an ultrathin dielectric interlayer a bandage. Figure 1.5 shows the example of the semiconductor grafting AlGaAs/GaAs/Diamond structure for heterojunction bipolar transistors. The III-V material, AlGaAs/GaAs, is used as an emitter and base, respectively, due to its high speed and linearity characteristics [28-30]. One of the largest bandgap materials–diamond substrate–is used as a collector because it has a large bandgap and high breakdown characteristic [31]. These combined efforts for fabricating such high-performance heterojunction bipolar transistors are reviewed and discussed in Chapter 4. In addition, in Chapter 3, the semiconductor grafting technique was focused on forming heterostructure with the most common semiconductor materials: silicon and GaN (diamond-wurtzite structure).

Forming heterostructure between two arbitrary types of semiconductors without considering lattice matches can open a number of opportunities for material engineering and enable much broader applications–electronics, optoelectronics, and energy [32-34]. To be specific, to form tandem structures using silicon and III-V materials, we can overcome the limit of silicon solar cells [19]. An effort to achieve Si and III-V tandem solar cells with high conversion efficiency is introduced in Chapter 2. Moreover, the needs for large bandgap material are briefly explained in the following section.

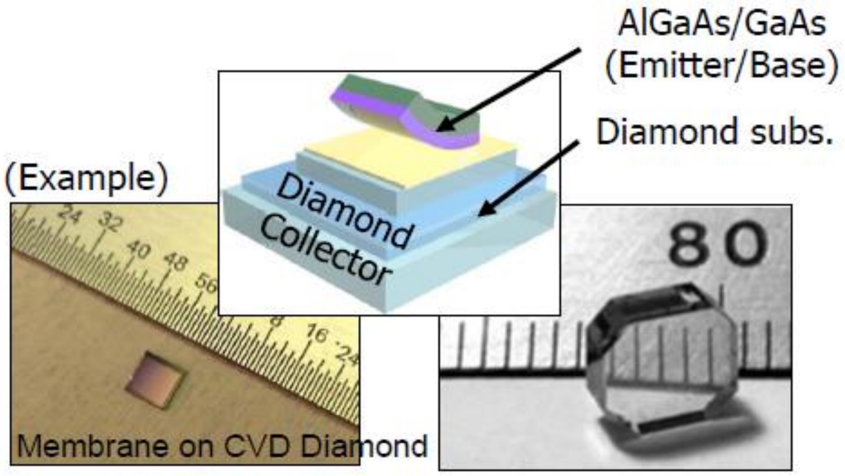

Figure 1.5 *The example of the semiconductor grafting AlGaAs/GaAs/Diamond (Emitter/Base/Collector) structure for heterojunction bipolar transistors (Detail information of this HBT is in chapter 4).*

1.3.Wideband gap material applications for future demand

Like the invention of the semiconductor integrated circuits in the 1950s and their prevalence in the era of modern computing and electronics for industrial applications, the power semiconductor business has been growing rapidly with an increasing impact on our lifestyles [35]. Due to matured CMOS (complementary metal-oxide-semiconductor) technology, silicon-based material has been dominant over all kinds of electronic applications [36, 37]. Nevertheless, all good things must come to an end. The silicon-based semiconductor industry is not an exception. Thus, many researchers anticipate that the silicon industry will be declining in the near future. According to Moore’s Law, the number of transistors incorporated on a single chip doubles approximately every two years [38, 39]. In conventional silicon-based technology, Moore's Law cannot be satisfied anymore. Because of the thermal issue, and the current leakage issue is occurring from the technology of excessively scaled-down structures.

Similarly, in the applications of medium- to high-power electronics (automotive sector, satellite communications, high-speed trains, mobile terminals), silicon-based devices have had an increasing challenge to relieve poor thermal dissipation and current leakage loss. Fundamentally, silicon technology is reaching its physical limits [40, 41]. In the near future, power electronics applications will require a more compact design with improved heat handling and dissipating capabilities. To meet these demands, a new generation of semiconductor materials is necessary. In recent years, silicon carbide (SiC) and gallium nitride (GaN)–namely wide bandgap (WBG)–have been emerged as the first solution for replacing silicon due to their advantages in terms of efficiency, device area, heatsink, passive filter volume reduction, radiation hardness and switching frequency [24-26]. Moreover, many research groups have researched ultra-wide bandgap (UWBG) semiconductors such as AlN, Ga_2O_3, and diamond, which have a desirable characteristic for power electronics–scaling down with less difficulty, high efficiency, and withstanding higher voltages and higher temperatures [26, 42-45].

Figure 1.6 shows the power versus frequency domain matching with the map of the power device application. As shown in Figure 1.6, the left side fields are currently dominated by silicon-based devices. As mentioned already, silicon power devices are based on mature CMOS technology and provide the best trade-off between performance and cost. According to their purposes, the range of relatively low frequencies with low to medium power, there are several optimized designs of silicon-based transistors alongside the technological progress -Insulated Gate Bipolar Transistors (IGBTs), Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), and thyristors. However, as shown in the right side Figure 1.6, modern society requests a variety of applications in the medium- to high-power electronics [31, 46, 47]. To be specific, RF related applications such as automotive, satellite communications, mobile terminals, computing, and data storage sever centers also benefit from the characteristics of wide bandgap semiconductors.

Regarding not only the explosion of mobile device usage such as smartphones and tablets but also the widespread, global trend towards online streaming service, leads to the creation of users and up/download data. The increasing traffic results in high performance demands on data center, wireless, satellite communications, and mobile terminals. Obviously, silicon-based RF power transistors have almost reached the limits of operating frequency, power density, and breakdown voltage.

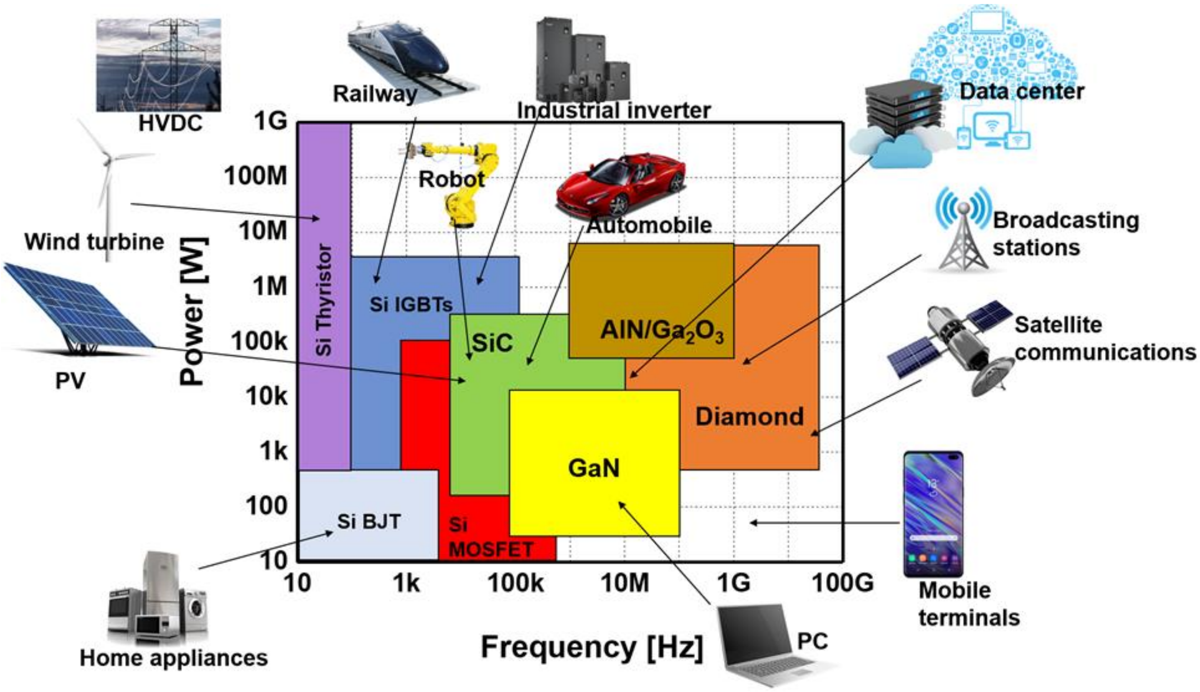

Figure 1.6 *The power versus frequency domain matching with various power device applications.*

Moreover, the increasing demand for energy-efficient society with low carbon emission leads to a need for new technology in the field of power electronics applications. Today, leading technology companies such as Tesla, Alphabet Inc. (Google, Waymo LLC), Uber Technology Inc., Etc., have been developing autonomous driving technology. Not only these companies but also traditional automotive companies such as Volkswagen, Toyota, General Motors, and Hyundai Etc., also began to invest in research on self-driving cars [48-50]. Because many people anticipate the breakthrough for the next generation should be related to autonomous driving technology. Figure 1.7 shows a brief schematic diagram of autonomous technology [51]. A number of scaled-down power device applications have been required for the future autonomous vehicle system. It includes many kinds of technology–mobile, wireless, satellite, clouding storage system, artificial intelligence (AI) computing, various sensors, Etc.

Following this trend, the large bandgap materials promise high-performance electronics in terms of power, frequency, and temperature. With its superior properties—high bandgap (5.47 eV), high critical electric field (7.7 - 20 MV/ cm), the high thermal conductivity (~ 22 W/cm·K at RT), and high hole mobility (> 2000 cm^2/ V·s), diamond has tremendous advantages beyond the silicon and other wide bandgap materials (WBGs) for ultra-high voltage and high-temperature (HT) applications (> 3 kV and > 450 K, respectively) [52].

Figure 1.7 *Demand for lots of power and smaller device applications for Future autonomous vehicle systems. It includes many technologies – mobile, wireless, satellite, clouding storage system, Artificial intelligence (AI) computing, various sensors, Etc. [51].*

This thesis is organized as follows: Three different topics are using the grafting technique.

First, Si and III-V tandem solar cells will be addressed in Chapter 2. For solar cell applications, we should consider the cost-effective method. In this chapter, we overcome the theoretical efficiency limit of silicon solar cells using semiconductor grafting techniques. The performance of the tandem solar cell with considering total cost will be presented in this chapter.

Second, in Chapter 3, the semiconductor grafting technique is focused on forming heterostructures with Si-GaN (diamond-wurtzite structure) semiconductor. Silicon is the most common semiconductor material, and GaN is one of the most popular materials these days because of its properties—direct wide bandgap, high saturation velocity, and high breakdown electric field [53-55]. Without considering lattice mismatch, Si/GaN combination diode will be discussed, and radically different material combinations will be demonstrated.

Third, an introduction to III-V/Diamond heterostructure formation for the fabrication of HBTs will be presented in Chapter 4, demonstrating the material properties of AlGaAs/GaAs nanomembrane as an emitter and base. Also, an overview of the diamond as a collector is explained in this chapter, where different figures of merit will be discussed to compare the electrical properties of diamond and other wide bandgap semiconductors. By using the semiconductor grafting technique, the fabrication of AlGaAs/GaAs NM on the diamond sub-collector and electrical characteristics of the heterojunction bipolar transistors will be described.

Finally, the summary of this thesis and the outlook can be found in Chapter 5.

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CHAPTER 2

Tandem solar cell – III-V solar cell on silicon solar cell by Epitaxial Lift-off (ELO) and Grafting technique

2.1 Introduction

As of early 2000, it is assumed that the world energy demand will remarkably increase by about 70% by 2030. The energy sources from fossil fuels, supplying 80% of all energy consumed worldwide, face rapid resource depletion. Increasing demand for energy with the depletion of fossil resources and its associated climate change, including global warming, environmentally sustainable energy technology is required. All the sustainable energy technologies, including solar power (electrical and thermal), wind turbine, hydropower, wave, and tidal power, biomass, Etc., the sun related technology is the most promising one owing to its unlimited, tremendous supply—3×10^{24} J per Year which is 10,000 times more than the annual energy consumes in the Earth. If we can convert the only 0.1% of solar energy on Earth's surface with 10% efficiency, our energy demand would be satisfied [1-7].

As shown in Figure 2.1, the PV industry has been growing steadily [8, 9]. Fig. 2.1 (a) represent the annual amount of PV solar systems installed by manufacturers in the unit of giga-watts (1GW = 1 billion watts) as a function of a year from 2013 to 2019. Global solar PV installations were exceeded 100 GW in 2019, according to new research, Wood Mackenzie. The only shortfall in 2018 was due to fewer installations than forecast in China. Beyond 2018, global demand returned to growth and rose above 100 GW for the first time in 2019.

Moreover, installations of the early 2020s are estimated to be around 115-120 GW and emerging markets. Nevertheless, the good news is that China still takes up a significant amount of global demand; the diversity of the global market is rising in Latin America, the Middle East, and Africa. In the entire world, there was cumulative PV solar installed of 628.9 GW at the end of 2019 compared to that of 417 GW at the end of 2017, as shown in Fig. 2.1 (b). 20% of the PV installation is distributed to private house rooftops, commercial buildings take another 20% of that, and the left 60% of that is in the utility plants connected to the grid.

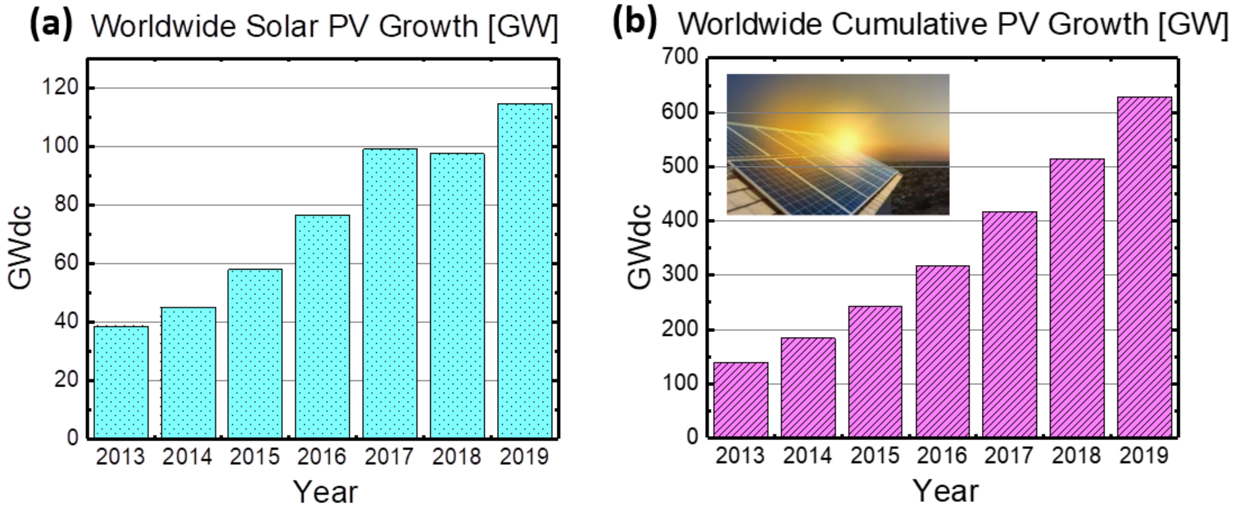

Figure 2.1 *Worldwide Solar PV Growth, (a) Annual PV demand GW as a function of the year (b) Cumulative PV growth GW as a function of the year.*

Figure 2.2 shows the market shares by PV technology [10]. The crystalline silicon solar cell (such as single-crystalline, multi-crystalline, and ribbon growth, Etc.) dominates the solar market by a large portion of 93%. A share of thin films for all thin-film technologies such as cadmium telluride (CdTe), copper indium gallium diselenide (CIGS), amorphous thin-film silicon (a-Si, TF-Si), Etc, was only 7% of the total shares in 2018, which is decreased by18% in 2009 [11-13]. The market share of crystalline silicon solar cells has been rapidly increasing in the last few years as Chinese manufacturers grew. Also, the quality of multi-crystalline has been tremendously improved, and finally, the efficiencies of thin-film (CdTe) and multi-crystalline silicon became comparable. Moreover, the crystalline silicon "cell" prices dropped by 60% in 2011 because raw material demand, polysilicon, which takes up the most significant part of the total cost, dropped rapidly [14]. To sum up, decreasing costs and increasing the crystalline silicon solar cell efficiency make it stronger continuously [15].

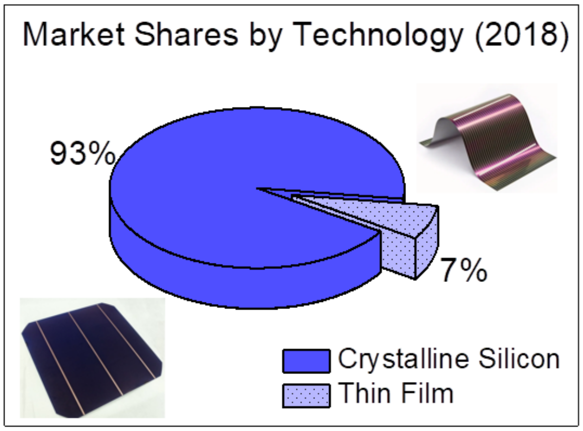

Figure 2.2 *PV market shares by technology, crystalline silicon solar cells (Single crystalline, Multi crystalline, Ribbon growth, Etc.) are dominant (93%) compare to Thin film technology (cadmium telluride (CdTe), copper indium gallium diselenide (CIGS), and amorphous thin-film silicon (a-Si, TF-Si), Etc.).*

However, everybody knows the efficiency limit of silicon solar cells [16-19]. In 1961, William Shockley and Hans Queisser first calculated the efficiency limit called Shockley Queisser limit (SQ Limit) [20]. The modern SQ Limit calculation is the maximum efficiency of 33% for any single-junction solar cell. The theoretical maximum of Si solar cell efficiency is 30% [21]. If we take surface recombination, light loss from each layer into account, this number decreases more. Even though several assumptions are involved in the calculation of SQ Limit, it is still applicable to 99.9% of the solar cells on the market today.

This limit is the beginning point of this chapter. How can we exceed the SQ limit? There are three basic concepts. First, make a tandem structure. It means using more than one material and junction in a cell. Then, the SQ limit increases more than 42% depending on how many cells are stacked in pn junctions tuned to a different solar spectrum frequency. This method has been considered as a first and popular way to overcome the SQ limit. The top layer of the junction can be made thinner than wavelengths of sunlight that goes through the bottom layer since sunlight only reacts strongly with band gaps that have roughly the same width with the wavelength of each junction [22]. It allows the semiconductors to be stacked for applications of multijunction solar cells [4, 23-28]. Second, increase the input of light source using a concentrator. In Concentrated Photo Voltaic (CPV), sunlight is focused onto a small solar cell by Fresnel lenses to collect more sunlight (1 sun to 500 suns) per unit of surface area. The primary purpose of the CPV system is to increase the efficiency of a solar cell.

Moreover, if the tracking system is added, input power is increased significantly [29, 30]. A tiny multi-junction solar cell of 39% efficiency is mounted at the focal point, converting the sun's energy into electrical energy. Shortly, efficiencies of CPVs are expected to approach 50% [31-33]. Lastly, try to absorb heat energy from photons, which is greater than bandgap. The quantum dots solar cells can absorb excess photon energy [34-40]. Quantum dots are extremely small "nanocrystals," whose diameter is between 1 and 20 nanometers. By interspersing QDs in a larger semiconducting material, QDs can harvest some of the excess photon energy for electrical energy [40]. In this Thesis, the first method was chosen along with considering total cost and commercialization.

Combined silicon and III-V material multi-junction tandem solar cells have been significant in photovoltaic applications. With the remarkable optical and electrical properties of III-V materials, epitaxial III-V solar cells have been researched steadily with silicon solar cells [19, 41]. Even though the epitaxial III-V solar cells have high efficiency, the critical problem of low cost-efficiency exists in applications of low concentration. Thus, for this reason, III-V solar cells have been targeted for space applications [42, 43]. Regarding the concern of the cost and high efficiency, the combination of silicon with III-V material has several advantages. First of all, considering solar spectrum absorption, silicon of 1.12 eV energy bandgap is the right candidate for tandem solar cells using III-V materials.

Moreover, epitaxial III-V materials of only a few micrometers thicknesses are needed for light absorption. Meanwhile, high thermal conductivity and mechanical strength of silicon support heat dissipation for III-V solar cells and tandem structure reliability. Thus, many research groups have been studying to pursue high-performance III-V/Si tandem solar cells with different approaches [44-48].

There are several ways to form III-V/Si tandem structure solar cells, but they all have their own disadvantages. The most general and simple method is direct growth. The challenging point of epitaxial growth of high-quality III-V materials on Si substrate has been a large lattice mismatch (~4%), causing degradation in conversion efficiency [49-51]. As an alternative, wafer bonding allows homogeneous epitaxial growth of high-performance solar cells on different substrates. Using this method, four-junction solar cells of GaInP/GaAs on GaAs and GaInAsP/GaInAs on InP marked the world record efficiency for concentration application [52]. Not only this combination, but also silicon with III-V, has been studied on applications of low-temperature, interface optical transparency, and thermal and electrical conductivity [53-55]. However, due to the consumption of two wafer substrates, the total fabrication cost is high. For trying to solve this problem, epitaxial lift-off (ELO) III-V films and solar cells have been introduced, so that the expensive III-V wafers can be reused [56-66]

In this chapter, using semiconductor grafting techniques, two solar cells based on silicon and III-V material were directly bonded. By considering total cost, the epitaxial lift off process (ELO) was conducted to recycle and reuse expensive III-V wafers. The bonding interface with an ultrathin Al_2O_3 layer is optically transparent, and thermally and electrically conductive. In addition, the whole fabrication process was relying on conventional CMOS fabrication technology for applying to the commercial production line quickly.

2.2 Methods

a. Silicon solar cell fabrication (bottom cell)

Silicon wafers produced by Shinsung Solar Energy (currently Shinsung E&G), which is the company where the author worked, was used for the bottom cell with a partially modified process. Figure 2.3 shows the flow chart of a conventional silicon solar cell process. Regarding this tandem solar cell, five kinds of processes are taken for cleaning the silicon wafer, doping process, phosphorus diffusion ($POCl_3$) process and phosphosilicate glass (PSG) (formed after diffusion process) etching, anti-reflection (AR) coating, and rear side aluminum metallization and fast-firing process.

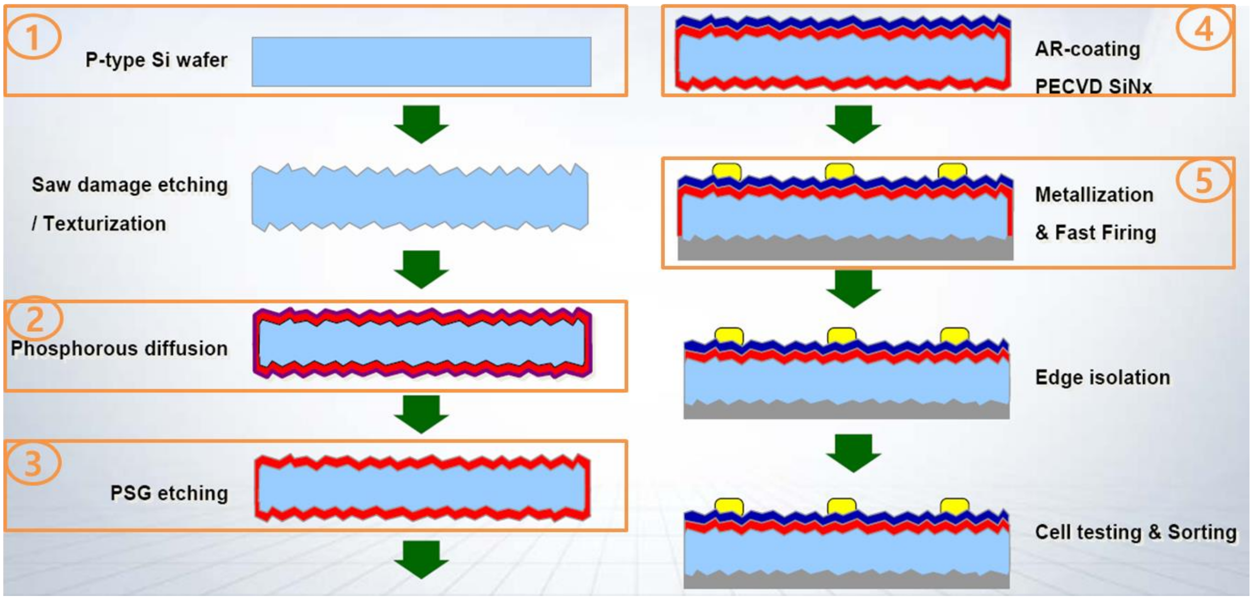

Figure 2.3 *Conventional silicon solar cell process flow chart. For this tandem solar cell, five kinds of processes are taken – cleaning the wafer (1), doping (2, 3), anti-reflection (AR) coating (4), and rear side metallization process (5).*

Figure 2.4 shows the preparation of the silicon bottom cell. Fig. 2.4 (a) shows the process flow charts for Si bottom cell. Except for the front surface chemical mechanical polishing (CMP) process, all processes were conducted in Shinsung Solar Energy Ltd. First, the monocrystal boron-doped p-type six-inch (156×156 mm^2) commercial-grade CZ silicon wafers with the thickness of 200 µm ± 20 and the resistivity of 0.5 to 3.0 Ω-cm were used for the silicon bottom cells. Once the wafer is diced from Si ingot, the wafer is then immersed in the mixed solution to remove the saw damage, which is called saw damage etching (SDE), and then immersed into an alkaline mixture solution to form the texturing both surfaces. However, one of the criteria for the semiconductor graft technique, the surface roughness of the host substrate, should be below 2 nm. Therefore, chemical mechanical polishing was processed on the front side of the Si wafer by outsourcing. The surface root-mean-square roughness was verified by atomic force measurement (AFM).

In contrast, due to increased light reflection inside the solar cells from the rear side, the rear side texturization remains. After the texturization and front-side CMP process, the doping process has proceeded in an 80MW capacity R&D line in Shinsung Solar Energy Ltd. The wafer is placed in the $POCl_3$ diffusion tube furnace to perform front side gas diffusion. The heavily p-type doped region was formed on the front side, and the peak doping concentration of the front surface is 1×10^{20} cm^3. After two steps of the diffusion process, pre-deposition, and drive-in process, phosphosilicate glass was formed. By using a diluted hydrofluoric solution, the formed glass can be removed. Right after the doping process, generally, silicon nitride (SiNx) anti-reflection coating was performed by using tube-type plasma-enhanced chemical vapor deposition (PECVD).

On the other hand, anti-reflection coating was performed after the front side metallization process for this tandem structure due to stacked III-V solar cell on the silicon solar cell. However, the front side of the silicon solar cell was covered by Silicon oxi-nitride (SiON) of 200nm grown by PECVD to protect the front side layer during other processes, which are screen printed metallization and fast-firing process. Finally, the rear side of the textured surface of the Si substrate is then coated with the aluminum paste by using a screen printer and conveyor belt type fast firing process to create an ohmic contact and back surface field (BSF) to increase the probability of carrier collection. During the fast-firing process, particles and contaminants on the front side can be removed by wet etching the SiON with HF rinsing right before Al_2O_3 ultrathin layer deposition via ALD. Fig. 2.4 (b) shows the schematic diagram of modified silicon bottom cells from Shinsung Solar Energy Ltd., while their real images are shown in Fig. 2.4 (c).

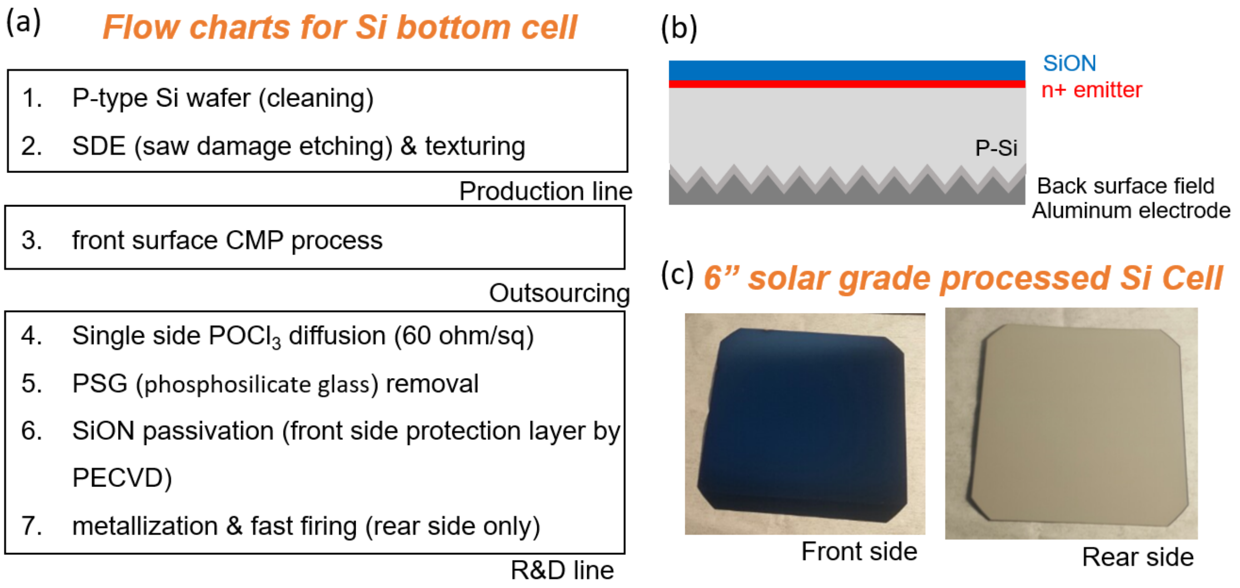

Figure 2.4 *Silicon bottom cell preparation (a) process flow charts for Si bottom cell except for outsourcing, all the processes were conducted in Shinsung Solar Energy. Ltd, (b) schematic diagram of modified Si bottom cell structure from Shinsung Solar Energy, (c) optical images of 6” solar grade processed Si cell (the front side is coated with SiON, while the rear side printed aluminum paste.*

b. III-V substrate preparation (top cell)

Figure 2.5 (a) shows the Shockley-Queisser limit of dual junction solar cells as a function of the bandgap combinations. By considering the current matching and relaxation of hot carriers, the preferred bandgap combination is highly limited, with a tiny range [30, 53, 67]. Silicon with an energy bandgap of 1.12 eV combines most successfully with a material with a bandgap energy of 1.8 eV. In this work, Al0.3Ga0.7As with a bandgap of 1.8 eV is selected as a top cell. This bandgap combination is close to the optimum conversion efficiency value shown in Fig. 2.5 (a). A schematic diagram of this tandem solar cell structure is shown in Fig. 2.5 (b).

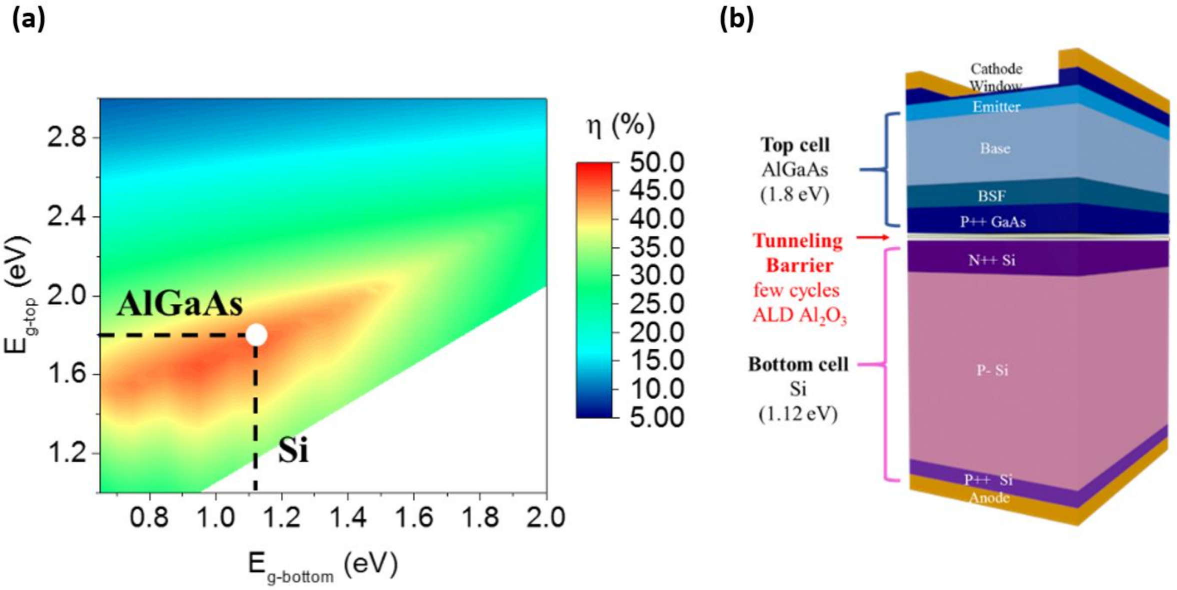

Figure 2.5 *(a) Shockley-Queisser limit of the dual junction solar cells. (b) Schematic diagram of the AlGaAs/Si tandem cell structure with an intermediate p++ GaAs/Al_2O_3/n++ Si direct tunneling junctions.*

The structure of the GaAs/AlGaAs/GaAs/Si heterogeneous tandem cell with the highest conversion efficiency was precisely simulated with Silvaco^{TM} by implementing the Monte Carlo method on the simulation design of GaAs/AlGaAs/GaAs top cell structures grown on a GaAs handling substrate with an AlAs sacrificial interlayer of 1μm. The epi-layer on top of GaAs substrates was subsequently patterned with strips with sequential 30s of boron trichloride (BCl_3) of 10 sccm and argon of 5 sccm etching with a Plasma Therm SLR series inductively coupled plasma (ICP) etcher until the sacrificial AlAs layer is exposed. The post-etching GaAs substrate was to dip into N-Methyl-2-pyrrolidone (NMP) to remove any photoresist residue. The samples were rinsed with water and immersed in isopropyl alcohol (IPA) before further processing.

c. ALD Al_2O_3 deposition

Before the semiconductor grafting process, the native oxide formed on the top surface of the silicon cell without SiON was removed by pure HF solution treatment, thoroughly post-water rinsing, and drying with nitrogen gas. The ultrathin layer Al_2O_3, which acts as a quantum tunneling layer and a passivation layer, was deposited on the as-cleaned silicon solar cell substrate using *ex-situ* Ultratech/Cambridge Nanotech Savannah S200 ALD system. Right after removing native oxide using the HF solution, the silicon cell was loaded into the chamber without exposing the air. This ALD system was integrated with a nitrogen-filled glove box to avoid exposure to oxygen and moisture. The ALD process began with two cycles of 0.015 sec H_2O pretreatment. Then difference cycles (none, 3, 4, 5, 6, 7, 10) of trimethylaluminum (TMA)/water vapor cycles for the ALD Al_2O_3 deposition have chronologically proceeded vacuum condition. After deposition cycles, a stabilization step of 300 sec was followed by a five sccm H_2O flow. During the process, the chamber was heated to 200˚C. TMA of 97.05% purity (Sigma-Aldrich Co.) and high purity deionized water (The Science Company) was used as the ALD precursors.

d. Grafting III-V nanomembrane on silicon solar cell with ELO process

Figure 2.6 shows the semiconductor grafting process to integrate an III-V solar cell on a silicon solar cell. The first loop in Fig. 2.6(a), an expensive III-V wafer recycling process, is the same as the conventional ELO process. First, III-V solar cell with AlAs sacrificial layer was grown on the GaAs handling substrate (#1) along with the number in Fig. 2.6(a). Then, III-V NM was patterned and etched (#2) like the previous section b. Step #3 in Fig. 2.6(a) shows the AlAs sacrificial layer's etching to release the III-V NMs. For releasing the GaAs/AlGaAs/GaAs epi-layer strips, the GaAs substrate was placed in diluted HF solutions (1:200) under the N_2 ambient condition for two hours. The sacrificial layer's etching process into HF solution was complex processing that involved chemical reactions, dissolution of byproducts, and mass transport [56, 57, 65]. The undercut process could be affected by many factors such as the geometry of the sample, the concentration of etchant, and the sacrificial layer's chemical composition. Thus, the condition of the undercut process varied depending on materials. Once the top cell III-V membrane was suspended from the substrate with a fully etched AlAs sacrificial layer, the samples were rinsed with water and immersed in isopropyl alcohol (IPA) before further processing. The stripe GaAs NM was picked up by PDMS stamps (#4), and the III-V wafer could be recycled after re-growing the GaAs/AlAs layer (#5). Typically, once the undercut etching was finished, the freestanding III-V films could be grafted for various applications, including flexible electronics [58, 68]. The second loop in Fig. 2.6(a), which is III-V top cell, was integrated into the silicon bottom cell with an Al_2O_3 ultrathin layer. We called this method the semiconductor grafting technique. The undercut GaAs substrate was taken out from the IPA solutions, and the released GaAs/AlGaAs/GaAs nanomembrane is picked up by the PDMS stamps (#6). The upside-down GaAs/AlGaAs/GaAs nanomembrane has the bottom surface face-up. The native oxide of the GaAs surface was removed by rinsing with diluted HF solution for a short time on the surface. After the sample was cleaned with water to remove any residue of the HF process, the PDMS was immediately applied onto the top smooth surface of the silicon bottom cell with an ultrathin Al_2O_3 layer deposited by ALD (#7). No bonding or adhesive agents were needed in the semiconductor grafting process. The bonding strength exclusively depends on the van der Waals forces between the III-V and silicon surfaces with the Al_2O_3 ultrathin layer [60]. It is a significant advantage to eliminate shadowing loss from bonding or adhesive agent. Moreover, there is no obstacle to the heat dissipation of solar cells. The GaAs/AlGaAs/GaAs nanomembrane was firmly applied on top of the silicon bottom cell, and the clean interface from the two solar cells and deposited ultrathin Al_2O_3 layer were the keys of the integrating (#8). After the releasing process, the bonding annealing process increased bonding strength between two cells (#9). Fig. 2.6 (d) shows the microscope image after removing the AlAs sacrificial layer, which was removed at step #3 in the process flow. Fig. 2.6 (c) shows the microscope image of strip-type III-V NMs (top cell) on the PDMS stamp after picking up the process (#6). Fig. 2.6 (d) shows the microscope image of strip-type III-V NMs (top cell) on the silicon bottom cell with bonding annealing (#9).

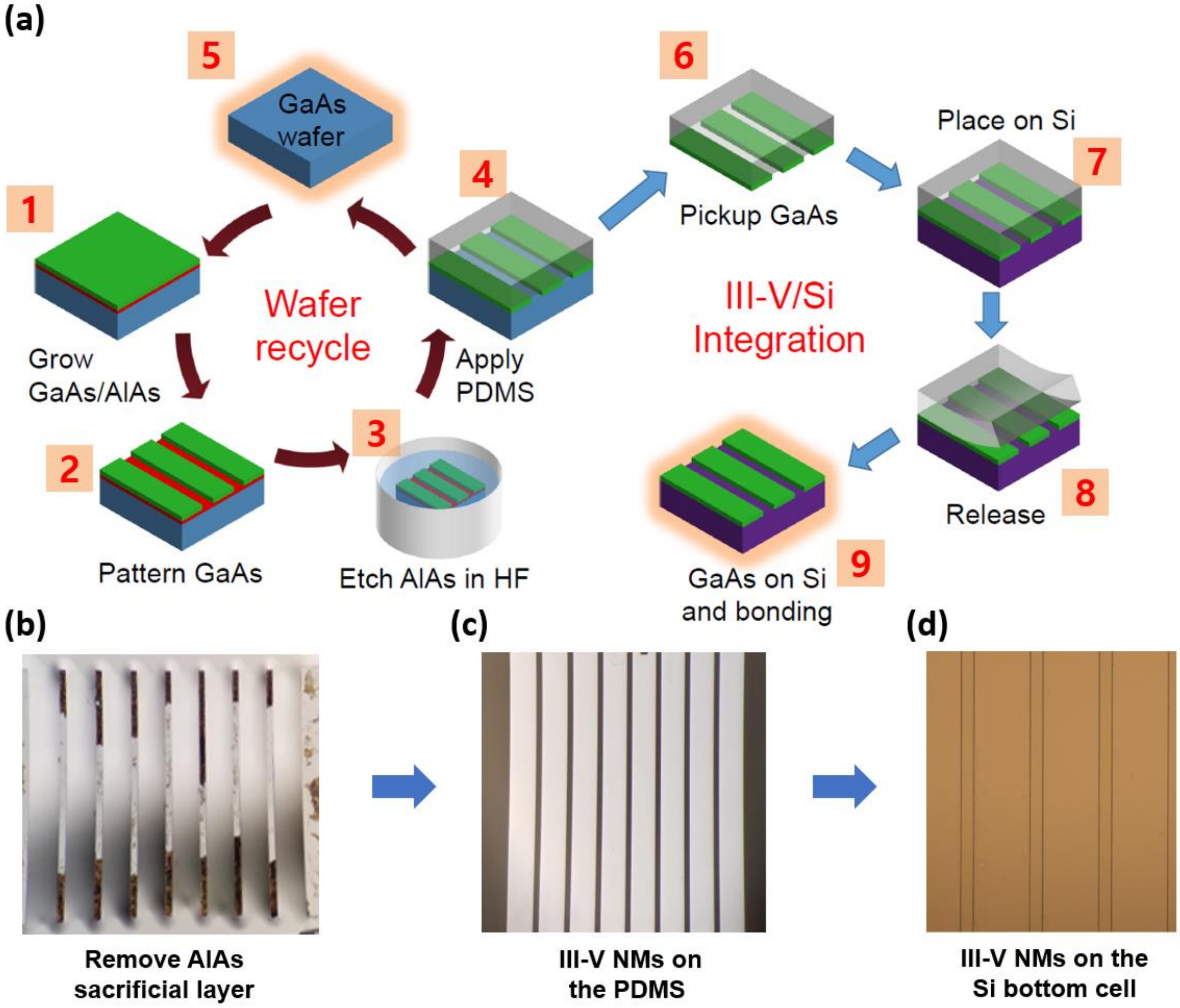

Figure 2.6 *The semiconductor grafting process to combine III-V solar cells on silicon solar cells. The process of recycling expensive GaAs wafer is the same as the ELO process. (a) Process flow of expensive GaAs wafer recycle and III-V/Si solar cell integration, (b) the microscope image of after removing AlAs sacrificial layer (step #3 in the process flow), (c) the microscope image of strip-type III-V NMs (top cell) on the PDMS stamp (after picking up process which is step #6), (d) the microscope image of strip-type III-V NMs (top cell) on the silicon bottom cell with bonding annealing (#9).*

e. Tandem cell fabrication process

As mentioned in the last part of the previous section, after the semiconductor grafting of the III-V top solar cell NM on the silicon bottom cell, a thermal anneal process for 5min at 250°C at N_2 ambient was processed to improve the Val der Waals bonding strength between the two cells. To form an ohmic contact to the top III-V solar cell, Pd/Ge/Au 30/45/180 nm was deposited as electrodes on the top windows layer of the GaAs n+ layer on the AlGaAs solar cell by using an electron-beam evaporator (Angstrom Engineering, Nexdep Physical Vapor Deposition Platform). Following rapid thermal annealing for 60 seconds at 500°C at N_2 ambient was proceeded to form the ohmic contact of the top cell. Later, the same metal structures of Ti/Cu/Au of 10nm/1500nm/200nm thickness were deposited on the top of the ohmic contact layer to reduce the device resistance. Next, the top contact layer was etched with a Plasma Therm SLR series inductively coupled plasma (ICP) using the deposited metal as the self-aligned etching mask to open the absorption layers. After dry etching, the final GaAs n+ layer of 20nm was removed by wet-etching to achieve surface smoothness and remove non-uniformed defects produced by the dry etching. Then, deep dry etching was carried out to define the solar cell active region, and the structure was not etched once the etching process exposed the top surface of the silicon solar cell. In order to check the cell performance of the separate solar cell, another metal pad was deposited on the top of the silicon solar cell: Ti/Au of 10/100 nm by using an electron-beam evaporator. High enough etching depth was needed for individual tandem solar cells on the same substrate when it comes to silicon solar cell isolation.

The final step was the deposition of anti-reflection coating using a dielectric evaporator (Angstrom Engineering, Nexdep Physical Vapor Deposition Platform). Before deposition, the sample was cleaned to remove photoresist thoroughly by using Plasma Asher with 250W power

O_2 plasma. A short time of dip in 1:10 HCL was then proceeded to remove native oxide before the anti-reflection layer. The double anti-reflection layers, TiO2/SiO2 of 45/80nm, were implemented for the designed structure.

f. Characterizations

A silicon bottom cell morphology was characterized by a Bruker Multimode 8 atomic force microscopy (AFM). The textured surface topography was measured by the Olympus LEXT OLS series 3D laser microscope. Transmission Electron Microscopy (TEM) was measured to verify interlayer conformation. To confirm the isolation of the cells, the Zygo 3D surface profiler was used. A Keithley 4200-SCS semiconductor parameter analyzer measured the Current-voltage (*I*–*V*) characteristics. Quantum efficiency was measured to be 350nm to 1200 nm in the home-made optical measurement system. The tandem solar cells were internally measured under the one sun intensity (AM 1.5G) calibrated by reference solar cell in the home-made optical measurement system. With conversion efficiency measurement, open-circuit voltage, and short circuit current and fill factor were calculated together. For each measurement of different light input, calibrated sun numbers were applied.

2.3 Results and discussion

a. surface morphology of silicon bottom cells and III-V top cells

For the semiconductor grafting technique, surface roughness is critical to forming heterostructures and their device performances. Olympus LEXT OLS series 3D laser microscope was used to measure textured surface morphology. Bruker Multimode 8 atomic force microscopy (AFM) was used to check the surface roughness after the CMP process. According to data obtained through several experiments, root-mean-square roughness (R_{rms}) of less than 2 nm should be guaranteed for the success of the semiconductor grafting technique. Firstly, a textured silicon substrate was polished by the CMP process to obtain a smooth surface. Figure 3.5 shows topographic images of silicon bottom cells. Fig. 2.7 (a) shows the textured surface of the silicon bottom cell whose height is 5 to 8 μm. Fig. 2.7(b) shows AFM topographic image after the CMP process with deposition of ultrathin Al_2O_3 layer by ALD. The R_{rms} is 2.01 nm in the measured area (100×100 μm^2). For III-V top cell NMs, after fully undercut of an AlAs sacrificial layer, the III-V top cell strips were picked up by a PDMS stamp. The AFM instrument measured the backside of the III-V top cell strips on the PDMS. As shown in Figure 2.8, the undercut side's surface is immaculate and flat, with R_{rms} of 0.321 nm in 1×1 μm^2. AFM measurement confirmed that the backside surface of the III-V top cell and the top surface of the silicon bottom cell with ultrathin Al_2O_3 layer are both smooth enough for the semiconductor grafting technique.

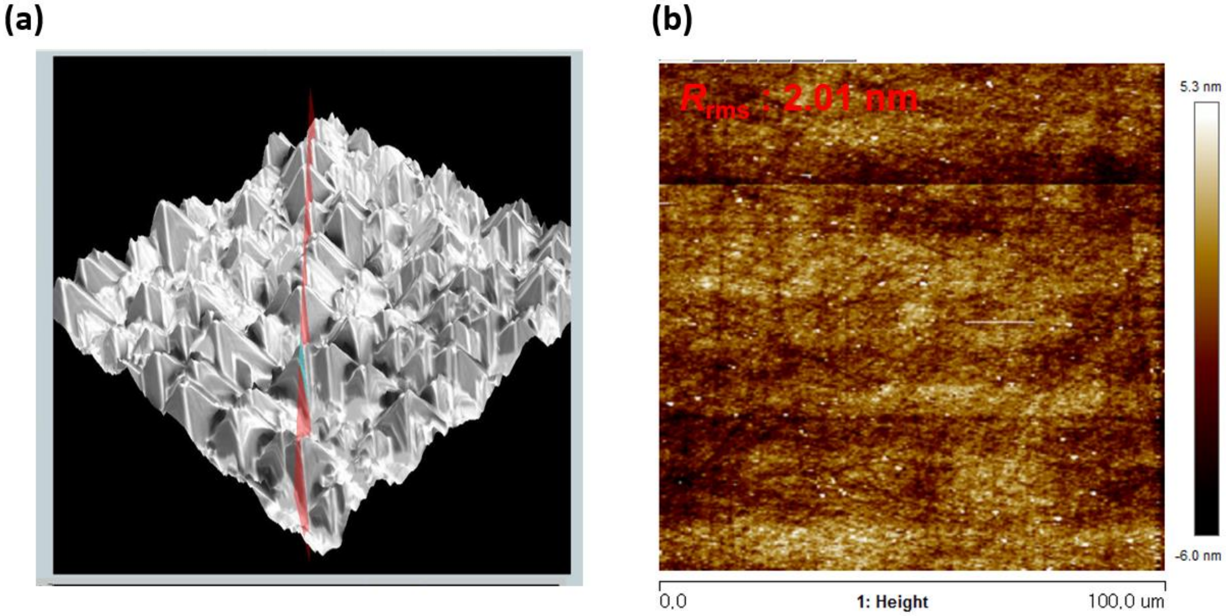

Figure 2.7 *Surface topographic images of silicon bottom cell (a) textured surface before CMP process measured by 3D laser microscopy (b) smooth surface after CMP process measured by AFM*

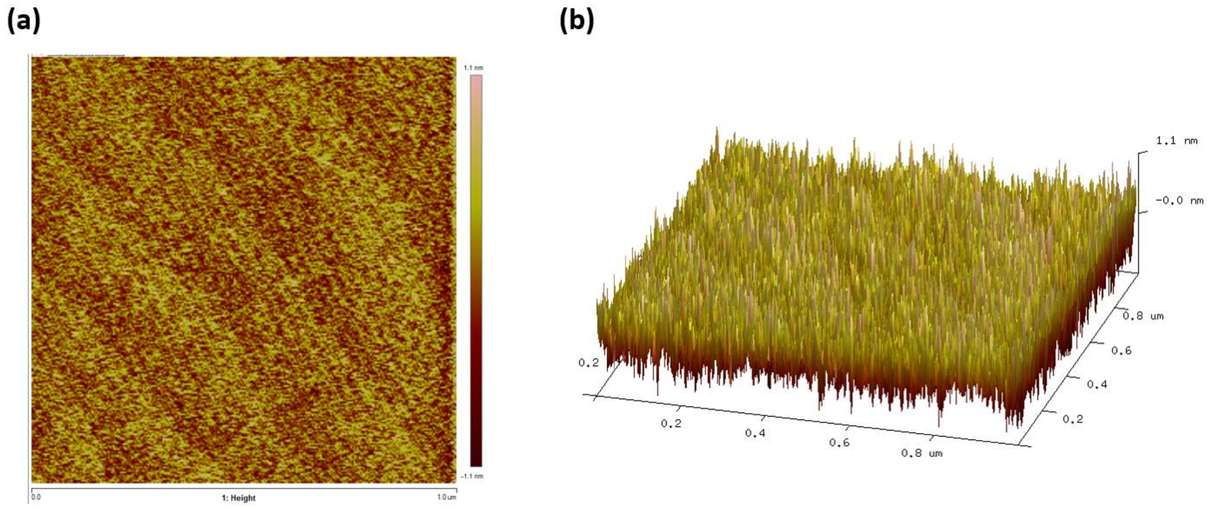

Figure 2.8 *AFM topographic images* $(1\times1\ \mu m^2)$ *of the bottom side of III-V top cell on PDMS,* $R_{\mathrm{rms}} = 0.321$ *nm (a) 2D morphology and (b) 3D morphology*

b. CTLM test of electrodes

Before starting the fabrication, to obtain the best performance of diodes, we should check and determine the resistance of ohmic contacts processed using a low-temperature ohmic annealing step. The Circular Transmission Line Method (CTLM) structures were formed on the front surface of GaAs top cells and the front surface of silicon bottom cells. The rear side of the silicon bottom cells was printed by Aluminum paste and passed through a firing belt guaranteed by Shinsung Solar Energy Ltd. The CTLM structure consists of circular contacts separated from an electric field by a ring-shaped gap, as shown in Fig. 2.9. It had to be confirmed that the same metal combination and annealing conditions for each cell were used in this test. The detailed specification is in table 2.1. The *I-V* characteristics of the CLTM pattern were measured using a Keithley 4200 Semiconductor Parameter Analyzer.

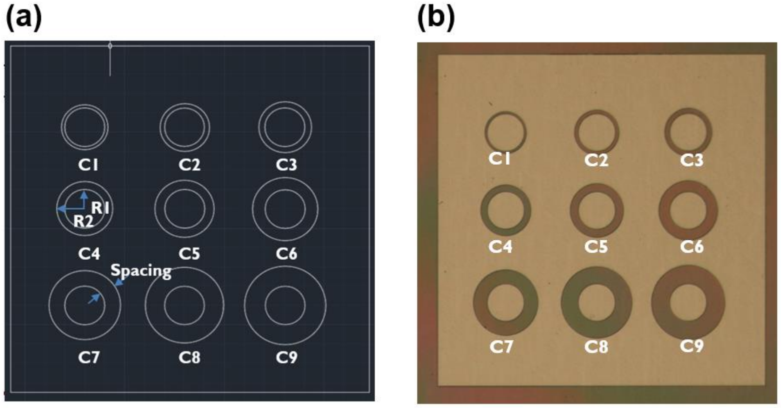

Figure 2.9 *Top view of the Circular Transmission Line Measurements (CTLM) structure. (a) CAD designed image with R_1 and R_2, which are radii of the inner and outer circle contact, respectively, and Spacing is the gap between R_1 and R_2 [μm], which is a variable (b) The microscopic images of CTLM pattern on the substrate.*

Table 2.1 *The R_1 [μm], R_2 [μm], and Spacing [μm] values of each samples (circle).*

#	R1 [μm]	R2 [μm]	Spacing [μm]
C1	50	58	8
C2	50	62	12
C3	50	66	16
C4	50	70	20
C5	50	74	24
C6	50	82	32
C7	50	90	40
C8	50	98	48
C9	50	102	52

For n-type GaAs top cell contact, Pd/Ge/Au metal layers were used with annealing in for one minute at N_2 ambient of 450°C. When it comes to Si bottom cell front contacts, Ti/Au metal was used for the front side, and Al paste with firing was used for the rear side contact. Figure 2.10 shows the measured *I-V* characteristics for different length of spacings between CTLM patterns and the n+GaAs top cell contact (Pd/Ge/Au) in Fig. 2.10 (a) and between the CTLM patterns and the n+Si bottom cell front contact (Ti/Au) in Fig. 2.10 (b). Both solar cells contact parameters are shown in table 2.2. The front contacts of both cells have a relatively low contact resistance of 1.56×10^{-5} Ωcm^2 and 3.75×10^{-6} Ωcm^2 from n+GaAs and n+Si contact, respectively. The sheet resistance can also be found in Table 2.2, with 49.86 Ω/□ and 9.09 Ω/□, respectively.

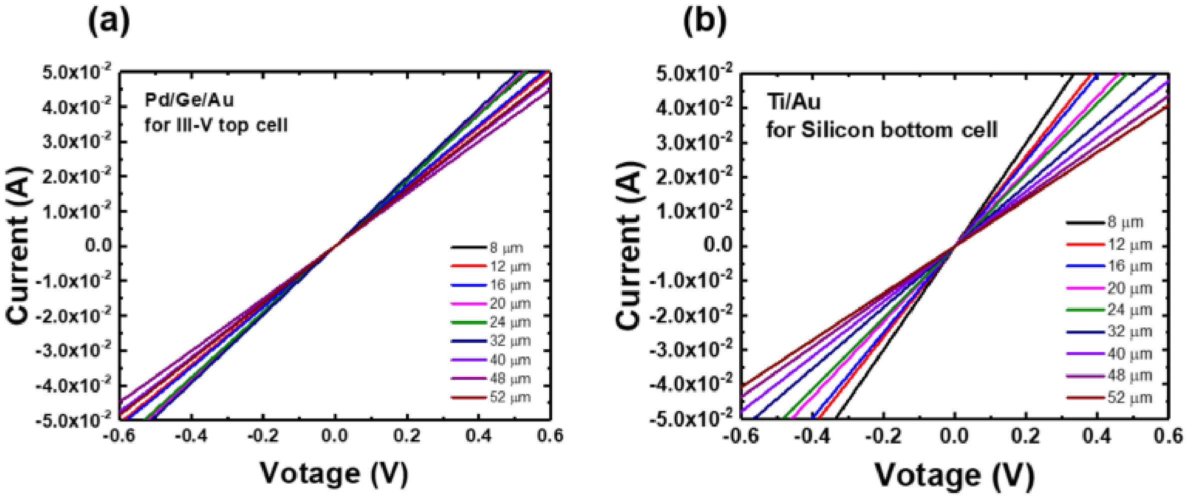

Figure 2.10 *Circular Transmission Line Measurements (CTLM) study of each cell contact, n+GaAs for top cell, and n+Si for bottom cell front contact.*

Table 2.2 *The sheet resistance (R_s (Ω/□)) and specific contact resistance (ρ_c (Ω-cm^2)) of metal contact of each cell.*

Material	**R_S(Ω/□)**	**$\rho_C(\Omega \cdot \mathrm{cm}^2)$**
n+GaAs	49.86	1.56×10^{-5}
n+Si	9.09	3.75×10^{-6}

c. Electrical connection property between two cells with TEM study

Transmission Electron Microscopy (TEM) was measured to verify the bonded p+GaAs/Al_2O_3/n+Si heterojunction interface cross-section. Fig. 2.11 (a) shows a crystal orientation illustration of the GaAs/Si heterostructure. Compared to this illustration, Fig. 2.11 (b) shows a TEM image of the GaAs/Si heterostructure interface region with an Al_2O_3 ultrathin layer. The scale bar of the TEM image is nm. The TEM study implies that GaAs and Si forms a single crystallized structure. On the other hand, the Al_2O_3 ultrathin layer in the heterostructure is shown in the non-crystallized region [67]. It means that the single crystal quality of GaAs and Si is not affected during the semiconductor grafting process. Moreover, there is no lattice distortion or dislocation around the bonded interface. It indicates that the Al_2O_3 works as a thermal buffer layer during the thermal anneal and cooling process.

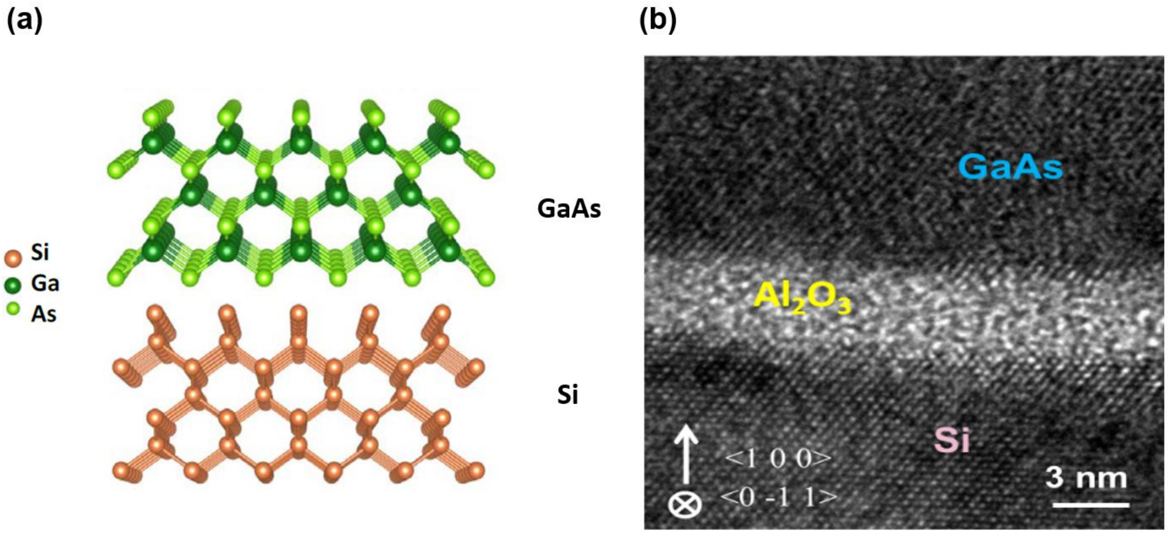

Figure 2.11 *Cross-sectional transmission electron microscopy (TEM) micrograph GaAs/Si two cells interface with* Al_2O_3 *ultrathin layer. (a) crystal orientation illustration of GaAs and Si heterostructure (b) TEM image of two cells interfacial compared with a 3 nm scale bar.*

Figure 2.12 shows the electrical characteristics of tunneling juncti*on* of simplified structures that contain only the thin film of p+ GaAs whose doping concentration is the same as the real III-V top cell and the top of n+ Si bottom cell substrates. The 100nm p+ GaAs membrane was bonded on the silicon bottom cell substrates with different cycles of ultrathin Al_2O_3 interlayer by using the semiconductor grafting method to study the interface of the lattice-mismatched tunneling diode between two cells. Figure 2.12 (a) shows the microscope image of 100nm p+GaAs/n+Si tunneling diode. As predicted from the simulation, surface conditions of the exposed n+ Si have an excessive amount of surface states and cause the *I-V* curve of the combined tunneling diode to become Schottky type of curves Fig. 2.12 (b). To design a good tunneling junction between the monolithic tandem solar cells, minimizing the tunneling interface loss is crucial. Unlike the native oxide with poor barrier quality, the resistance of the interfacial tunneling diode decreases exponentially as increasing the passivation cycles of the Al_2O_3 layer deposited by ALD. The electrical characteristics gradually switch from rectifying current to ohmic current, as shown in 2.12 (b). It is proof that the density of the surface trapping states, which is the dangling bond of silicon, is decreased by the surface passivation of the -O-Al- process. However, the more cycles of passivation, the thicker the Al_2O_3 became while reducing carriers tunneling.

Furthermore, as plotted in Fig. 2.12 (c), the resistance variance also decreased exponentially. This fact agrees with the report regarding the passivation effect in a few cycles of the ALD process. According to the tunneling diode experiment, the ALD passivation cycle between the 4 to 5 performed the lowest resistance across the junction and overall uniform passivation of the surface states on the silicon bottom cells. Hereby, the four cycles of the Al_2O_3 ultrathin layer were chosen as the interfacial condition for the fabrication of the monolithic III-V/Si tandem solar cells. The photocurrent can flow vertically across the interface ultrathin Al_2O_3 layer instead of laterally within each cell layer with a very conductive interface layer. Thus, there are no current spreading issues in the junction of III-V top cell and Si bottom cell junction.

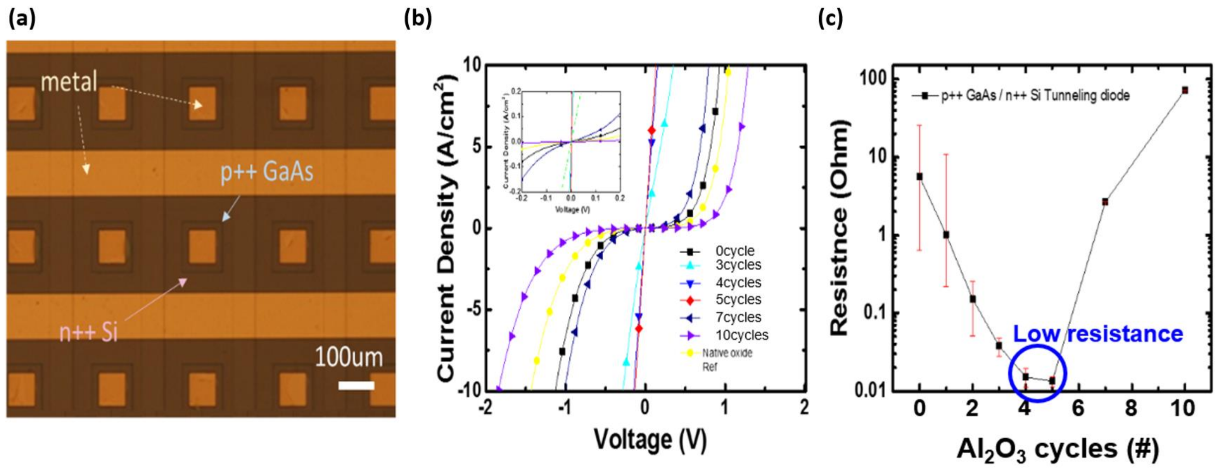

Figure 2.12 *Electrical measurement of p+GaAs/Al_2O_3/n+Si tunneling diode with the different cycle of Al_2O_3 deposition by ALD, (a) the microscope image of 100 nm p+GaAs/n+Si tunneling diode, (b) Current density of the tunneling diode as a function of voltage with different cycles of the ALD deposition, (c) Resistance and error distribution of the tunneling diode with different cycles of the ALD deposition.*

d. Tandem solar cell performance

Figure 2.13 shows the final structure of tandem solar cells. The top view of the microscope image is shown in Fig. 2.13 (a). Due to the TiO_2/SiO_2 double layer anti-reflection coating, the surface of the tandem cell looks darkish. Fig. 2.13(b) is 3D and 2D morphologies measured by the Zygo 3D surface profiler. As shown in the 3D profile, the III-V top cell of 1.8 μm is on the top of the Silicon bottom cell, isolated by ~ 2 μm depth deep ICP etching. This tandem cell structure included silicon front metal pads for checking the electrical performance of each cell. On the contrary, Figure 2.14 (a) shows the tandem structure with the metal pad on the front III-V top cell only. The aluminum paste was screen printed on the rear side of the silicon bottom cell.

The improvement in the quality of the high-quality interface between the two lattice-mismatched solar cells was further validated through the solar cell's overall performance. The III-V/silicon tandem solar cells with improved interface involving the Al_2O_3 ultrathin layer was characterized under AM1.5 standard spectrum with light intensity 100mW/cm^2 in a home-made optical measurement system. The incident light spectrum is mixed with a Xenon light source filtered out above 600nm and a thermal radiation source to cover the infrared red wavelength. The measurement system was calibrated by a reference solar cell.

This ultrathin and high-quality Al_2O_3 deposited by ALD provide perfect optical transparency in the medium region between each solar cell. The microscope image of the fabricated tandem cell arrays is displayed in Fig. 2.14 (a). The tandem solar cell with improved tunneling junction characteristic has a conversion efficiency of 30.2% (η) with fill factor (FF) of 68%, open-circuit voltage (V_{OC}) of 1.63V, and short circuit current density (J_{SC}) of 28.48mA/cm^2. As shown in Fig. 2.14 (b), the significant difference between this work and the previous research (plotted in green) is the improvement of the fill factor, which means that the performance of this work has reduced the unnecessary loss in the solar cell. In this research, the lattice defects and traps have been alleviated by passivation with the high quality ultrathin Al_2O_3 layer deposited by the ALD process, which was verified in the previous section. The uniformity of the tandem cell can be supported by electroluminescence (EL) image with forward biasing to examine the carrier injection between the two cells. In the inset image Fig. 2.13 (b), the whole area of a cell with Al_2O_3 of 4 cycles at the interface was illuminated uniformly, indicating that the carriers are flowing along the whole surface evenly. The result also has proved the reduction effect in the traps and non-radiated recombination at the interface [69-71]. It can be supported that the high-quality interface in the designed tandem cells has been achieved by implementing the ultrathin Al_2O_3 layer deposited by ALD. It provides the perfect optical transparency in the medium region of the tandem cells, the ultrathin layer mitigates the lattice mismatch problems, and the atomic-layer thick nature enhances the thermal conduction between the stacked solar cells.

Figure 2.14 (c) shows the external quantum efficiency (EQE) of tandem solar cells [72]. High bandgap (1.8 eV) III-V top cells absorb light of short wavelength, and low bandgap (1.12 eV) silicon bottom cells absorb long wavelength. The maximum of the external quantum efficiency has been marked above 80%. It means that recombination or other defects were minimized. By introducing solar cells involving an III-V thin film, the energy conversion efficiency in the low wavelength area has been increased, and the stacking structure of the higher bandgap materials has contributed to increasing the overall voltage output of the tandem cells [73-75].

Besides, a further investigation of performances of the tandem solar cells was conducted. With different light intensity up to 4.5 Sun, the cell parameters such as fill factor (FF), short circuit current (I_{SC}), and open-circuit voltage (V_{OC}) were analyzed and compared to those of other kinds of devices. The optical filters controlled the incident light intensity with different attenuation ratios. The measurement was conducted under room temperature (RT) without cooling management, and the result is presented in Fig. 2.14 (d) to (f). Among the factors, the average short circuit current (I_{SC}) as a function of the number of suns remained the same value while the intensity of the light increased. This fact indicates the generated photocarriers are proportional to the intensity of incident light and, has not reached a saturation point.

On the other hand, the open-circuit voltage (V_{OC}) is steadily increased as the more carriers are accumulated on each side of the junctions. However, the fill factor decreases from 68% to 60%, while light intensity increases from 1 Sun to 4.5 Sun. The effect of increasing temperature can explain the primary reason for the decrease in FF. Without effective thermal management, the temperature on the substrate was increased due to the absorption of light in the infrared wavelength range. It could generate the more trap states at the surface of III-V materials, and it is the reason causing the recombination process at the surface. Although the FF decreases by 11%, the conversion efficiency of the tandem cell only was changed from 30.3% to 29%. It is the merit of silicon-based tandem solar cell that has good thermal conductivity. To sum up, Table 2.3 shows the parameters of the tandem solar cell, conversion efficiency (η) of 30.2% with fill factor (FF) of 68%, open-circuit voltage (V_{OC}) of 1.63V, and short circuit current density (J_{SC}) of 28.48mA/cm^2.

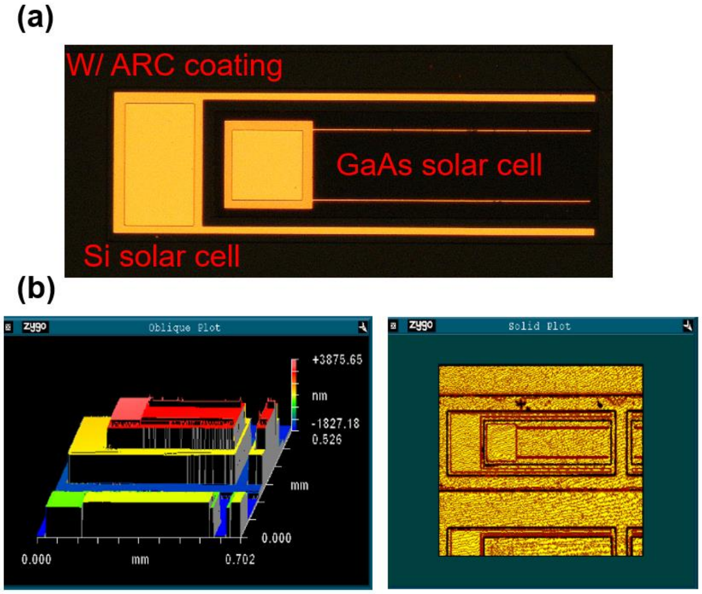

Figure 2.13 *(a) The microscope image of the top view of the tandem cell with a silicon bottom cell testing metal pad. Due to* TiO_2/SiO_2 *ARC coating, the surface looks darkish in (b) the 3D and 2d morphologies from* the Zygo 3D surface profiler.

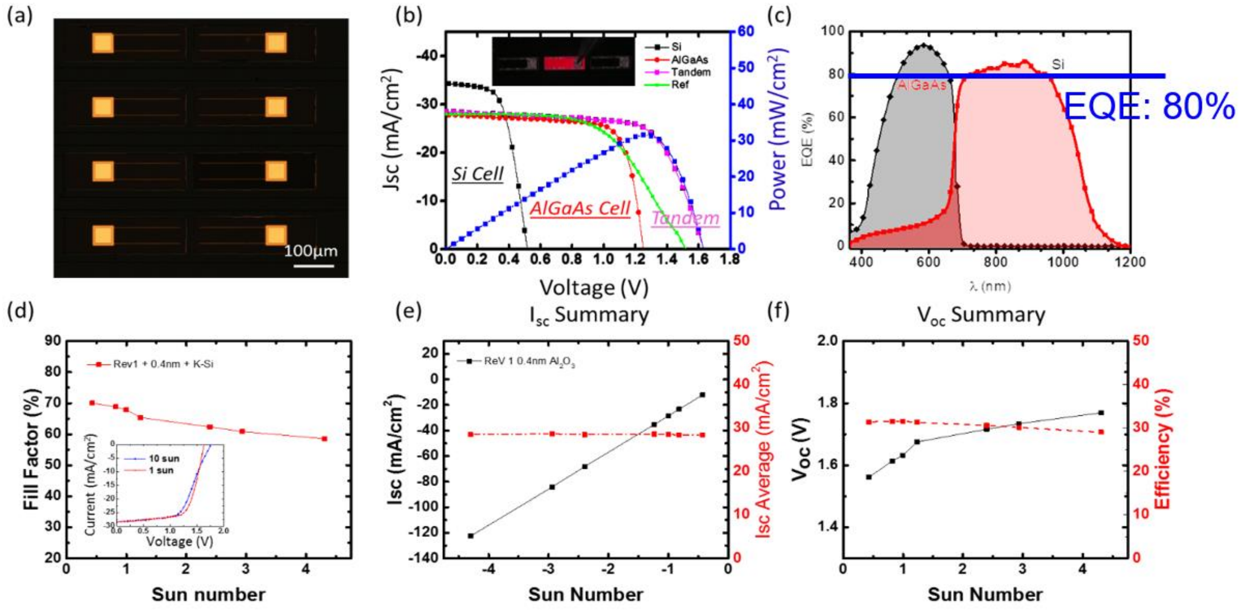

Figure 2.14 *III-V/Si tandem solar cell of 30.2% with Al2O3 improved tunneling barriers. (a) The optical Image of III-V/Si tandem solar cell with four cycles of* Al_2O_3 *interfacial layer (b) AM1.5 photovoltaic measurement of Si, III-V, and tandem cell to verify the performance of the solar cells, inset: electroluminescence (EL) image of the tandem cell to check uniformity, (c) EQE measurement as a function of light wavelength, (d) Fill Factor (e)* J_{SC} *(f)* V_{OC} *& efficiency as a function of different sun number.*

Table 2.3 *The cell parameters- The conversion efficiency (η), The fill factor (FF), Open circuit voltage (*V_{OC}*), and Short circuit current density (*J_{SC}*).*

Parameters	
η	**30.2%**
FF	**68%**
V_{OC}	**1.63 V**
J_{SC}	**25.48 mA/cm²**

2.4 Conclusions

To be concluded, the III-V tandem solar cell was fabricated by the grafting method with the III-V wafer recycle process. It has a high voltage output and high conversion efficiency that overcomes the silicon solar cell efficiency limit. The improved tunneling junction structures via the Al_2O_3 ultrathin layer deposited by ALD have been investigated while focusing on both cells' interface. The ultrathin and high quality Al_2O_3 tunneling barrier shows that optical transparency and thermal conduction characteristics were compared to the tandem solar cells with epoxy or adhesive. Substantial improvement in the overall performance of tandem solar cell in terms of open-circuit voltage (V_{OC}), and short circuit current density (J_{SC}), fill factor (FF), and the conversion efficiency (η) has been reported.

Moreover, using grafting techniques, it is easy to transfer nanomembrane to other cells or substrates from the perspective of fabrication. Besides, this III-V/Si tandem solar cell can be used in the space. According to NASA, mass and volume of objects are all parameters to be taken into account while launched. The key idea of the solar cell for space application is whether it is possible to make smaller, lighter than conventional solar cells while still maintaining high performance[76, 77]. Our III-V solar cells, beyond the silicon, can be grafted on other thin, flexible, stretchable, and rollable substrates in order to utilize in the space [68, 78].

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CHAPTER 3

Si/GaN Heterostructure and Diode Fabrication

3.1 Introduction

Heterostructure semiconductors devices have been widely used in modern life. In a heterostructure, more than two different semiconductors are brought into physical contact. The concept of heterostructure have been started to utilize for the optoelectronic applications to increase the carrier injection [1, 2]. The heterostructure devices such as lasers [3-6], HBTs [7-9], and high electron mobility transistors (HEMTs) [10-12] have been used in various applications – mobile phone, optical applications, wireless and satellite communications, and solar cells. Thanks to increasing demand and impact of heterojunctions, Zhores I. Alferov and Herbert Kroemer won the 2000 Novel Prize for "developing semiconductor heterostructures used in high-speed- and opto-electronics" [13].

Heterostructures are normally grown by Molecular Beam Epitaxy or (MBE) Metal Organic Chemical Vapor Deposition (MOCVD) epitaxial growth techniques [14, 15]. During the growth, we should consider lattice constant, strain, and critical layer thickness. Despite the huge success of lattice-matched heterostructures, forming heterostructures between two arbitrary types of semiconductors without considering lattice match has been sought after and attempted for over six decades without success. With typical growth method, forming heterostructure between two large lattice mismatched semiconductors is extremely difficult to get a single crystal semiconductor without degrading interface quality. There are some ways to form lattice mismatched hetero structure. Using conventional growth method, it has been shown the lattice match issue could be alleviated by adopting specific orientation and nano-scale seeds. However, the growth area is restricted due to difficulty of the relaxation of mismatched material in whole area [16, 17]. Another widely spread method is wafer bonding or fusion process. It provides an alternative way for the two arbitrary semiconductors heterostructure formations [18-23]. But several limitations exist in this application [24, 25]. All the materials do not have their host substrate and costly and time-consuming issues because of thinning down process as well [26, 27]. The most critical limitation is requirement of high temperature high pressure process. These processes lead to increase the interfacial layer thickness with forming of an amorphous layer and defect densities between the junctions. Today, many researchers have been studied combinations of distinct 2D materials to create heterostructures with different functionalities for electronic and optoelectronic applications, but they struggle for performance limitations cause of difficulty in controlling the interfaces and synthesis of 2D material in the wafer-scale [28, 29].

The several limitations associated with methods above, the semiconductor grafting method is one of the best options to circumvent these difficulties. Grafting one semiconductor to the host substrate has several advantages. Transferred (guest) semiconductor is entirely compliant with host substrate and nearly free of dislocation from thermal mismatch. During the grafting method, the Al_2O_3 interfacial layer is used to solve the wafer bonding issues – thick amorphous layer between interface, surface dangling bonds, which create defects energy level within semiconductor bandgap and act as trapping centers. The ultrathin Al_2O_3 interfacial layer deposited by atomic layer deposition (ALD), acts as passivation to reduce the dangling band amount, and but also as a tunneling layer for carrier transport. Moreover, the oxide layer represents strong bonds with other material chemically, ultrathin Al_2O_3 layer has a potentially advantage of robust passivation capabilities. Finally, this ultra-thin layer can be exploited for strain buffer layers and diffusion barrier during the other thermal process for the device fabrication [30].

In this Chapter 3, the most common material and the hottest material which are p-Si and n-GaN respectively are selected to represent of p-n heterojunctions formed between dissimilar crystal lattice structure of Diamond-Wurtzite.

One of the chosen materials in this chapter, Silicon is cheap, abundant, best known material in semiconductor field. Most of all, silicon dioxide (SiO_2) has the good quality and extremely controlled on the silicon substrate. In most transistor designs, a highly insulating material is needed to reduce electron current leakage. Thus, with CMOS technology, silicon is the most widely used semiconductor material. GaN is one of the most desirable wide band gap (WBG) semiconductor material due to its superior electrical and mechanical properties. As shown in Table 3.1, the major physical properties of silicon, GaAs, WBG materials and ultra-wide band gap (UWBG) materials are given. One of the main advantages of using WBG materials is that it can operate in much higher temperatures and can also be scaled down to a smaller size than the equivalent silicon-based power devices as a function of capacitance, enabling previously impossible applications. Some of the more popular WBG materials in the industry are silicon carbide (SiC) and gallium nitride (GaN). In research environments, Ga_2O_3, AlN and diamond are also used (detailed information is in chapter 4). While silicon possesses a bandgap of 1.12 electron volts [eV], SiC and GaN have a bandgap of 3.3 eV and 3.4 eV, respectively. The high-power density of GaN leads to make possible smaller devices and systems due to reduced input and output capacitance requirements and expand the operation bandwidth beyond the silicon [31]. The high critical electric field allows higher voltage operation and eases to match impedance. Thus, using a WBG material such as GaN makes superior performance RF applications possible with high-electron-mobility transistors (HEMTs) and monolithic microwave integrated circuits (MMICs), and lower gate capacitance which enables higher speeds and greater bandwidth [32-34].

To investigate the interface quality of heterostructure formed by the semiconductor grafting method, we have investigated the interface using several analysis equipment such as Raman spectroscopy, X-Ray Diffraction (XRD), and Transmission Electron Microscopy (TEM). In addition, diodes using p-Si/n-GaN heterostructures were fabricated with an Al_2O_3 ultrathin interlayer. Their much-improved performance compared to others reported result can verify that the semiconductor grafting technique is a good option to form heterostructure using arbitrary semiconductors. This combination form practically rectifying behavior with a low ideality factor of 1.14, low level reverse current density, high level forward current density and extremely high on-and-off current ratio at ±1V which is 1.18×10^7.

Table 3.1 *The comparison of material properties of silicon, GaAs, WBG and UWBG semiconductors for power applications. This chapter deals with devices fabricated using silicon and GaN, which are highlighted in yellow.*

Material				**WBG**		**UWBG**		
		Silicon	**GaAs**	**4H-SiC**	**GaN**	**Ga2O3**	**Diamond**	**AlN**
Bandgap [eV]		1.12	1.44	3.3	3.4	4.9	5.5	6.1
Critical Electric Field [MV/cm]		0.3	0.4	2.8	3.5	8	7.7-20	10
Mobility [cm^2/Vs] @RT	**Electron**	1500	8500	1000	2000 (2DEG) >1000 (bulk)	300	1060	300
	Hole	480	< 400	120	<100 (2DHG) <200 (bulk)	14	2100 (bulk) <300 (2DHG)	14
Thermal Conductivity [W/mK]		150	56	370	100(on Si) 165(on Sapphire) 253 (on GaN)	11-27	2200-2400	253-319
Relative Permittivity [a.u.]		11.8	12.9	9.8	9	9.9	5.5	8.5
Substrate diameter [inch]		8-17.7	3-8	8	8	4	<1	2
Substrate Dislocation [cm^{-2}]		<10	10^2-10^3	10^2	10^4	10^4	10^4-10^6	10^4
Saturation Velocity [x10^{7}cm/s]	**Electron**	1	0.72	1.9	2.5	2	2.5	1.4
	Hole	0.8	0.9	1.2	-	-	1.4	
Built in Voltage [V]		0.6	1.1	2.8	2.9	-	4.9	-
N-type dopant		available	available	available	available	available	moderate	moderate
P-type dopant		available	available	available	available	x	available	poor
Commercial devices		MOSFETs IGBTs Diodes Thyristors BJTs	MOSFETs BJTs Diodes HEMTs	Diodes BJTs MOSFETs	HEMTs			

Calculation assumed constant doping for both sides of the junction (1x10^{15} cm^{-3}) @ room temperature conditions.

3.2 Methods

a. Silicon and GaN Wafer Preparation to Semiconductor Grafting Process

Silicon nanomembrane preparation: The most common way to obtain a freestanding nanomembrane (NM) of semiconductor involves selective wet etching of the sacrificial layer underneath the NMs [35]. To obtain silicon NMs from silicon-on-insulator (SOI) wafers, diluted hydrofluoric acid (HF) is used to remove the SiO_2 buried-oxide (box) layer. Thus, any materials that are vulnerable to HF called sacrificial layer underneath the NM can be removed while the selective wet etching process [36-39]. Figure 3.1 shows the schematic diagram of the designed SOI wafer for the semiconductor grafting process, and Silvaco simulation results to get the specified thickness and doping level for the silicon layer on SiO_2 box layer. Ion implanted boron doping was carefully simulated with Silvaco using the Monte Carlo method to form designed thickness of p-type SiNM and uniformly heavily doped. The ion implantation process was proceeded by outsourcing with structures from the simulation result. After the ion-implantation, drive-in process was conducted in an in-house thermal furnace tube at 1050 °C for 12 minutes. The simulated doping concentration value is 1×10^{20} cm^{-3} and the actual value obtained from circular transmission line measurement (CTLM) is 9.7×10^{19} cm^{-3}, which is almost identical. The measured thickness of boron-doped SiNM is 180 nm. To graft silicon NM to a host substrate, etching holes are necessary in order to undercut the box layer by dipping into the HF solution. After a brief cleaning step with sonicating in acetone and isopropyl alcohol (IPA) and deionized (DI) water (18.2 MΩ) individually for 10 min respectively, etching holes were patterned by photolithography and were dry-etched by a reactive ion etching (RIE) process to remove the Si layer to form the etching holes. After forming etching holes in the silicon NM, a cleaning process was proceeded as below. Sonication in acetone and isopropyl alcohol (IPA) and deionized (DI) water (18.2 MΩ) for 10 min, respectively, at room temperature (RT) were proceeded. The Piranha cleaning (H_2SO_4 : H_2O_2 = 3 : 1 for 10 min at 100°C) was performed to remove trace amounts of organic residues, such as photoresist. After the Piranha process, an RCA1 (29% NH_4OH : 30% H_2O_2 : DI H_2O = 1 : 1 : 5) cleaning step was performed for 15 minutes at 75°C to remove organic debris, followed by an RCA2 (37% HCl : 30% H_2O_2 : DI H_2O = 1 : 1 : 5) cleaning step for 15 minutes at 75°C to remove ionic debris.

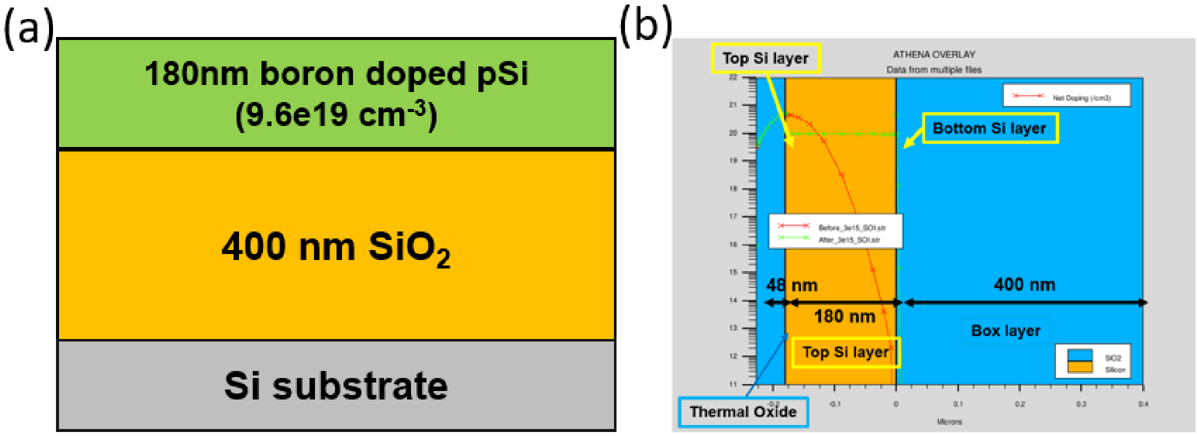


Figure 3.1 *(a) The schematic diagram of designed SOI wafer to semiconductor grafting process (b) Silvaco simulation to get specific thickness heavy doped silicon layer on* SiO_2 *box layer.*

GaN substrate preparation: The n-type Wurtzite Ga-polar GaN was grown on a SiC substrate by metal organic chemical vapor deposition (MOCVD). A 1.2 µm-thick, Si-doped n-type GaN layer (N_D = 7×10^{19} cm^{-3}) was grown including followed by a 200 nm-thick lightly-doped n-type GaN layer (N_D = 1×10^{17} cm^{-3}) was grown (Figure 3.2). The n-/n+GaN-on-SiC went through the same wet chemical cleaning process as the SiNMs. Then, it was dipped in a diluted hydrofluoric acid solution (49% HF : DI H_2O_2 = 1 : 50) for 1 min at RT to remove surface oxides, making the substrate ready for the deposition of Al_2O_3 ultrathin layer.

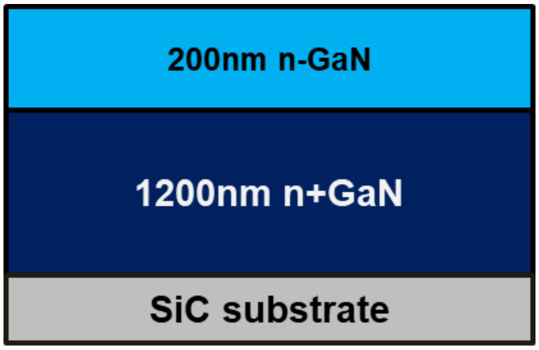


Figure 3.2 *The schematic diagram of epitaxially grown n-/n+ GaN on SiC substrate.*

b. ALD Al_2O_3 Deposition

The ultrathin layer Al_2O_3, which acts as a quantum tunneling layer and a passivation layer, was deposited on the as-cleaned nGaN substrate using *ex-situ* Ultratech/Cambridge Nanotech Savannah S200 ALD system. Right after removing the native oxide using HF, the nGaN substrate was loaded into the chamber without exposing to air. This ALD system was integrated with a nitrogen filled glove box to avoid oxygen and moisture. The ALD process starts with 2 cycles of 0.015 sec H_2O pretreatment, followed by 5 cycles of 0.015 sec trimethylaluminium ($Al(CH_3)_3$, TMA) precursor pulse, 5 sec N_2 purging, 0.015 sec H_2O precursor pulse, and a 5 sec interval under vacuum, at 200˚C. After five deposition cycles, a 300 sec stabilization step was followed by a 5 sccm H_2O flow. TMA, 97% (Sigma-Aldrich Co.) and high purity deionized water (The Science Company) were used as the ALD precursors.

c. Fabrication of Si/GaN Diodes

The Si/GaN lattice mismatched diode fabrication process begins with the semiconductor grafting process after depositing the ultrathin Al_2O_3 film on top of the thoroughly cleaned GaN substrate. The fabrication process of Si/GaN diodes is summarized in Figure 3.3. The substrate is cleaned by methods described earlier (Fig. 3.3 (a)) and is deposited an ultrathin Al_2O_3 (5 cycles) interlayer by the ALD system (Fig. 3.3 (b)). And then, the p+ Si nanomembrane was grafted to the Al_2O_3-deposited nGaN substrate, followed by a thermal anneal process for 5 min at 350 °C at N_2 ambient to increase the Van der Waals bonding strength (Fig. 3.3 (c)).

Figure 3.4 below shows the semiconductor grafting process in greater detail. First, the SOI wafer was cleaned and patterned (Fig. 3.4 (a)). The sacrificial layer (SiO_2 box layer in SOI) was removed by the HF solution (Fig. 3.4 (b)), and the membrane was picked up using a PDMS stamp (Fig. 3.4 (c)) and grafted to an n-type GaN substrate (Fig. 3.4 (d)). Fig. 3.4 (e) and (f) show the normal microscope image and DIC (Differential interference contrast) filtered microscope image of p+Si/nGaN grafted heterostructure. The voids or trapped defects can be inspected by using a DIC filtered image. As shown in Figure 3.4 (f), there are no defects at the interface. Figure 3.4 (b-1), (c-1), and (d-1) show a picture of p+Si NM in the HF solution, the top view optical image of p+Si NM (2.6×2.6 mm^2), and a picture of the grafted p+Si NM on n+GaN substrate, respectively.

After finishing the semiconductor grafting technique, it followed a standard top-down fabrication process [40]. Ni/Au (10/100 nm) was deposited on the p+ Si for the anode electrodes by using an electron-beam evaporator (Angstrom Engineering, Nexdep Physical Vapor Deposition Platform) (Fig. 3.3 (d)). To expose the n+ GaN layer, the p+ Si and n- GaN layers were selectively etched away with a Plasma-Therm SLR series ICP plasma Etcher (Fig. 3.3 (e)). A cathode metal stack of Ti/Al/Ti/Au (25/100/20/100 nm) was deposited on the n+ layer, followed by annealing at

350 °C for 60 seconds in N_2 ambient (Fig. 3.3 (f)). Finally, the anode mesa was formed by etching away the p+ Si membrane using the anode metal as a mask with Plasma-Therm 790 Series ICP plasma Etcher to isolate the diodes (Fig. 3.3 (g)). Figure 3.3 (i) shows the optical microscope image of the resulting p+Si/nGaN heterojunction diode.

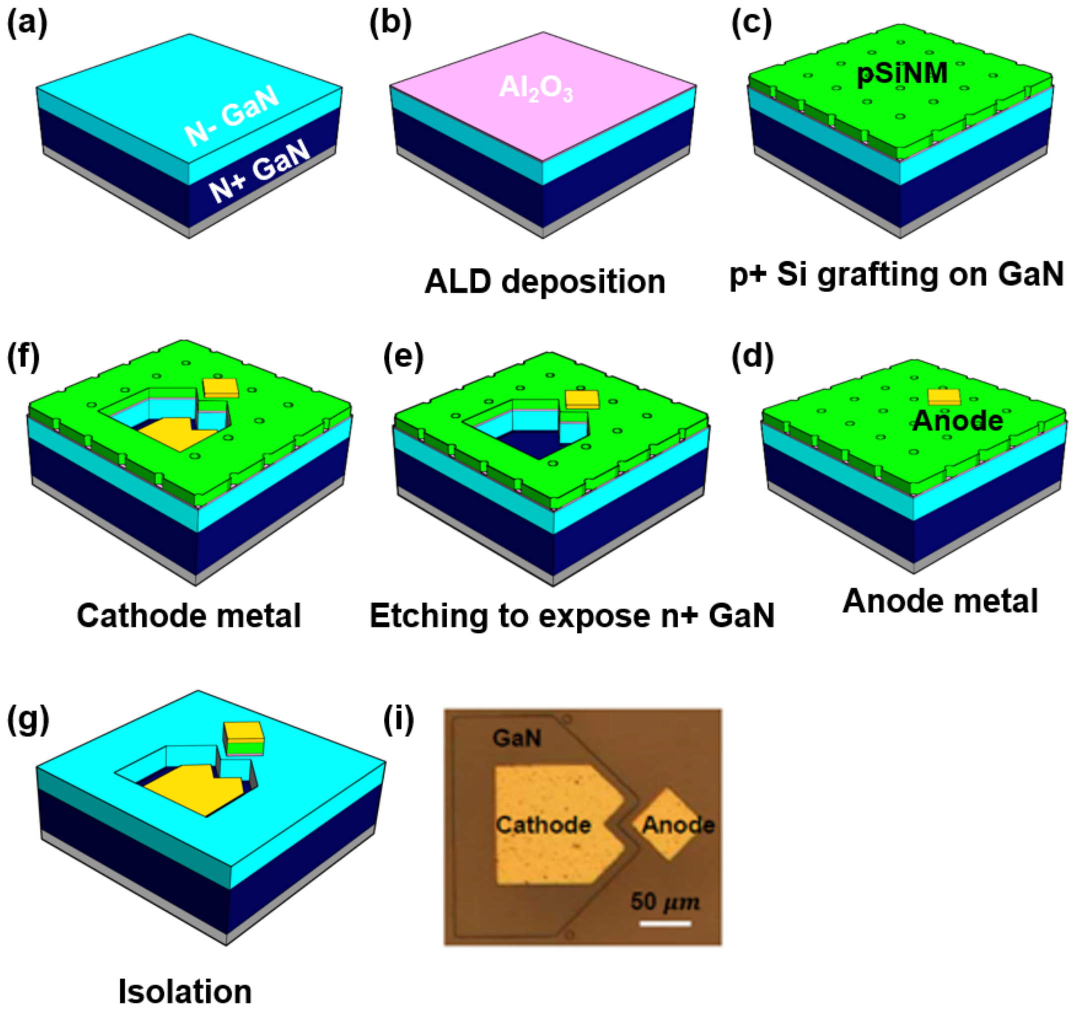


Figure 3.3 *The schematic diagrams of the whole fabrication process of Si/GaN grafted diode. (a) Each substrates cleaning, (b)* Al_2O_3 *ultrathin layer deposition by ALD on GaN substrate, (c) p+Si grating process on* Al_2O_3 *deposited GaN substrate, (d) Anode metallization process on p+Si, (e) MESA etching process to expose n+GaN layer, (f) Cathode metallization process on n+GaN, (g) isolation process, (i) microscope image of Si/GaN diode which scale bar is 50 μm.*

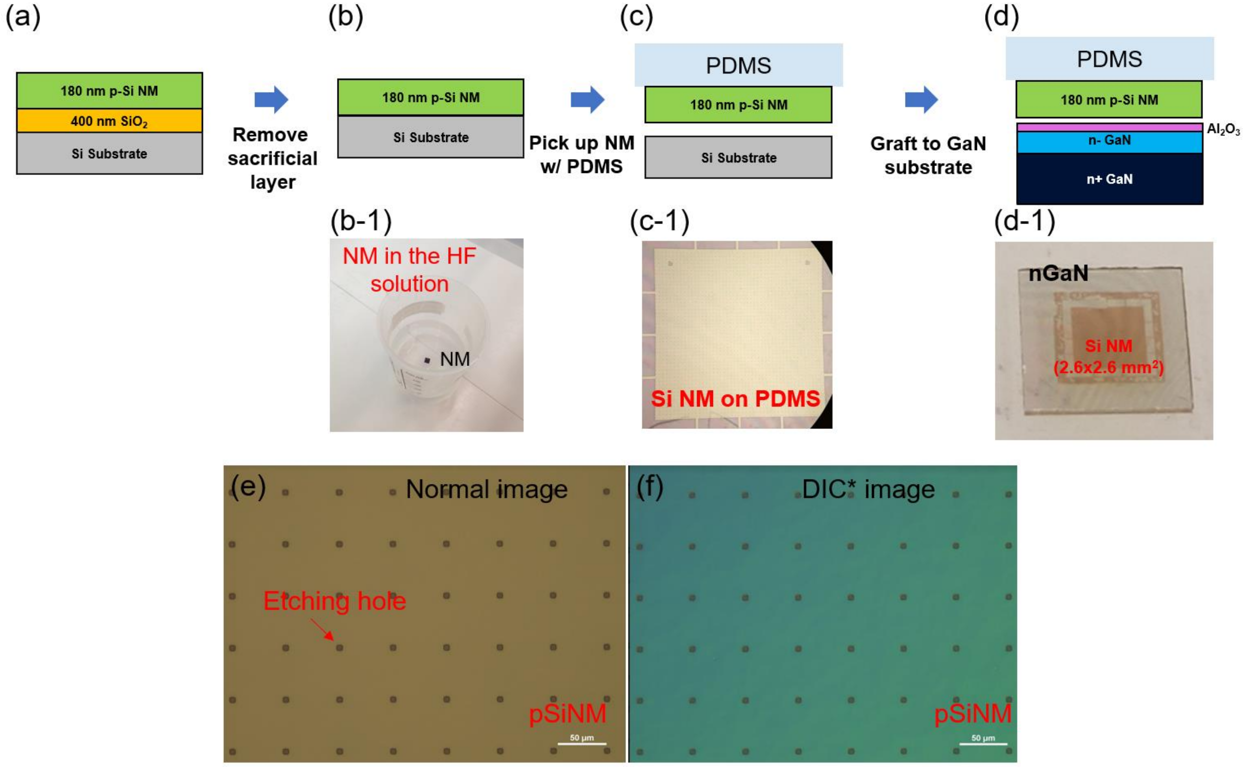


Figure 3.4 *The semiconductor grafting process for Si/GaN heterostructure diode. (a-d) the schematic diagrams of grafting process with assisting PDMS stamp, (a) Silicon nanomembrane, (b) Sacrificial layer removal dipping into the HF solution, (b-1) The real image of NM in the HF solution, (c) Picked up the p+Si NM using PDMS, (c-1) The top view image of p+Si NM on PDMS using microscope, (d) Grafted p+Si NM on n+GaN substrate, (d-1) The real image of grafted p+Si NM on n+GaN substrate (e) The microscope image of grafted p+Si NM image, (f) DIC* (Differential interference contrast) filtered microscope image of grafted p+Si NM image which scale bar is 50 µm.*

d. Characterizations

The morphology of interfacial surfaces – bottom of the p+Si NM and ALD Al_2O_3 on GaN – was characterized by a Bruker Multimode 8 atomic force microscopy (AFM). Current–voltage (*I*–*V*) characteristics were measured by a Keithley 4200-SCS semiconductor parameter analyzer. The capacitance–voltage (C–V) characteristics of p+Si/nGaN diode was examined by an Agilent precision E4980 LCR meter. The Raman spectra on the GaN samples were obtained by a Horiba LabRAM ARAMIS Raman confocal microscope with an 18.5 mW He-Ne (532 nm) green laser. The crystallinity of the film was checked by X-ray diffraction (XRD) Malvern PANalytical Empyrean. Scanning Transmission Electron Microscopy (STEM) was measured to verify interlayer conformation. AFM, Raman spectroscopy, XRD, *C*–*V* and all the *I*–*V* measurements were conducted in ambient air at room temperature.

3.3 Results and discussion

a. Interface roughness measurement

For the semiconductor grafting technique, the surface roughness is critical in forming a heterostructure. If surface defects such as hillocks, or damage from the dry-etching exist on the surface of the host substrate, it is hard to perform the semiconductor grafting for the adhesion and uniformity matter. Also, if pits are on the surface of the host substrate, the performance of device is degraded due to the void between the heterostructure. Bruker Multimode 8 atomic force microscopy (AFM) was used to check the surface roughness. According to data obtained through numerous experiments, a root-mean-square roughness (R_{rms}) value less than ~ 2 nm guarantees the success of the semiconductor grafting technique. Figure 3.5 shows AFM topographic images (1×1 μm^2) of interfaces of both semiconductors. The bottom side – the surface that was in contact with the buried-oxide layer on the SOI wafer before removing the sacrificial layer – of p+ Si NM is shown in Fig. 3.5 (a). This surface topographic image was obtained by performing the measurement on the bottom side of the p+ Si NM on a PDMS after picking up the membrane. The R_{rms} of a representative p+ Si NM, which is the roughness of the undercut surface between silicon and SiO_2, is 0.343 nm. The representative ultrathin-Al_2O_3-deposited-GaN on SiC substrate also has a low R_{rms} value which is 0.459 nm. The R_{rms} value of both interfacial areas are within acceptable values to perform the semiconductor grafting process to form a good quality heterostructure.

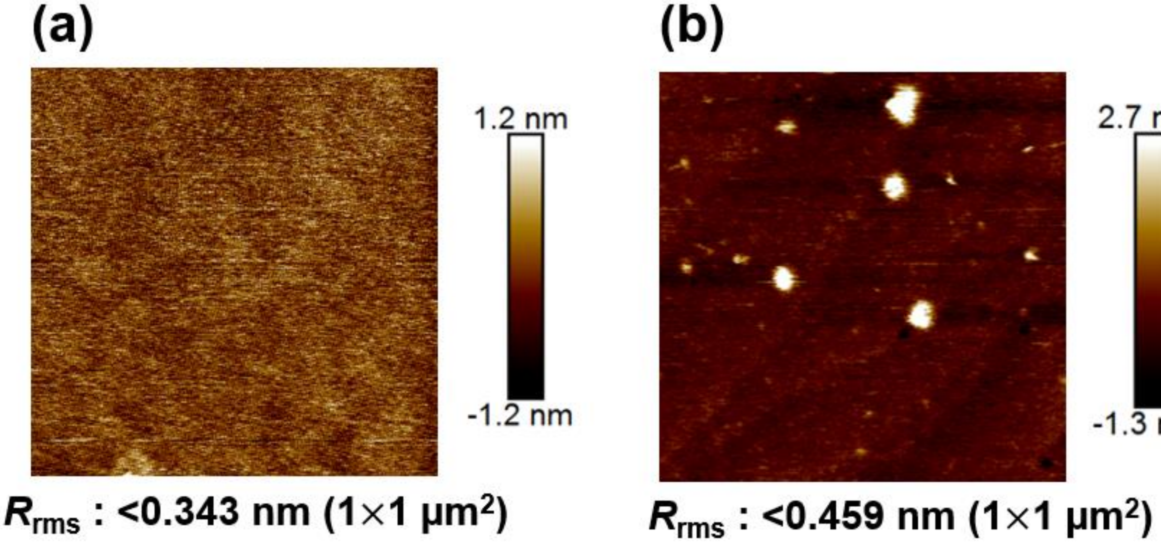
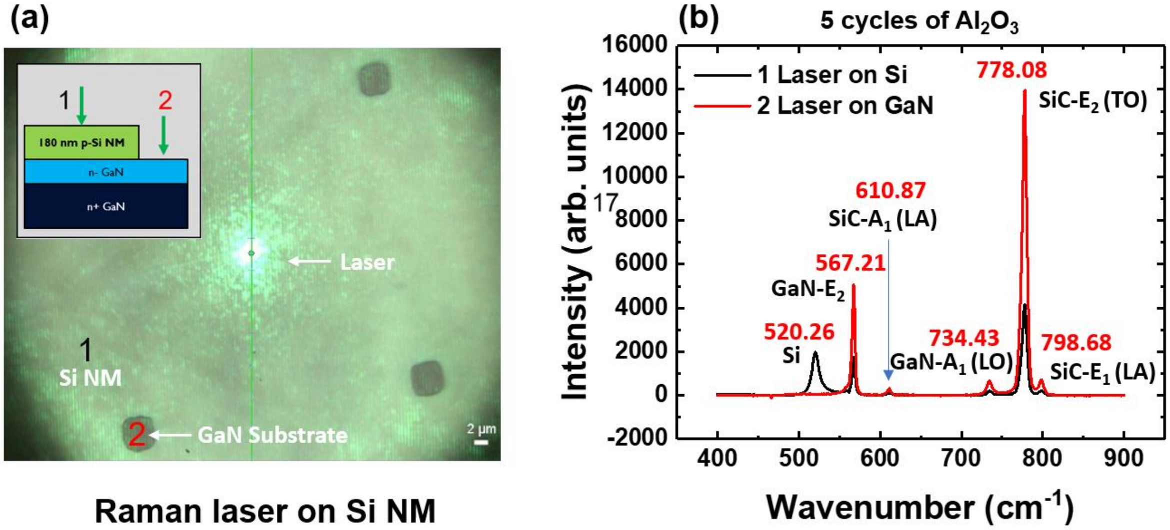


Figure 3.5 *AFM topographic images (1×1 μm*^{2}*) of interfaces of both semiconductors. (a) bottom side of p+Si NM, and (b) ultrathin* Al_2O_3 *on nGaN substrate. Root-mean-square roughness (*R_{rms}*) of the interfaces of both semiconductors are presented below the AFM images.*

b. Raman spectroscopy measurement

Raman spectroscopy measurement, shown in Figure 3.6, is performed to check the strain after semiconductor grafting process. The Raman spectra on GaN substrates were obtained by a Horiba LabRAM ARAMIS Raman confocal microscope with an 18.5 mW He-Ne (532 nm) green laser. For silicon, the penetration depth of this 532 nm wavelength laser is 1260 nm, which is much longer than the NM thickness (~100 nm). Thus, it is the possible way to directly compare the spectral data with laser on silicon with GaN (1) and GaN only (2) which is shown in Fig. 3.6 (a). Inset image of Fig. 3.6 (a) is schematic diagram of laser position 1 and 2 which are on p+Si NM and GaN substrate, respectively. As shown in Fig. 3.6 (b), the Raman spectrum indicates that the Si peak and the GaN peaks appeared at 520.26 cm^{-1} and 567.21 cm^{-1} /734.43 cm^{-1}, respectively. Also, the original substrate SiC peaks appeared at 610.87 cm^{-1} /778.08 cm^{-1}/798.68 cm-1. The peak shift between two different laser position (1) and (2) could not be observed which confirms that the transferred Si NM, as well as GaN substrates, were free of strain induced by the bonding process, even after thermal anneal. Finally, it can be one of the crucial claims to form stable heterostructures using semiconductor grafting technique [36, 41].



Raman laser on Si NM

Figure 3.6 *Raman spectroscopy study to check the strain after semiconductor grafting technique. (a) Raman laser (532nm) on p+Si NM (1) and GaN substrate (2), inset image is schematic diagram of laser position 1 and 2 which are on p+Si NM and GaN substrate, respectively. (b) Raman spectrum of the laser 1 and 2.*

c. XRD measurement

The crystallinity of the film was evaluated by X-ray diffraction (XRD, Malvern PANalytical Empyrean) with a Cu-Kα1 radiation source (λ = 1.5406 Å). The XRD scan as a function of 2θ in Fig. 3.7 (a) exhibits main peaks at 34.56° and 72.92°, which originated from the GaN (004) epi-layer and grafted p+Si NM (400), respectively. Full width at half maximum (FWHM) values of 72.92° from silicon (400) is 0.292. The 2θ value and FWHM for p+ Si NM indicated single crystalline quality after the semiconductor grafting and junction bonding annealing steps. Fig. 3.7 (b) shows the reciprocal space mapping (RSM), where each point – Si (400), GaN (004), and SiC (008) – represents a set of Bragg planes, and the amount of broadening of the reciprocal lattice point can be attributed to mosaic spread [42]. Thus, as shown in the Fig. 3.7 (b), each RSM point from the top layer film is narrow, which indicates high quality crystalline film. Both measurements, Raman spectroscopy and XRD, can evaluate the strain and crystallinity of p+Si/nGaN heterostructures and verify successfully formed heterostructures by the semiconductor grafting technique.

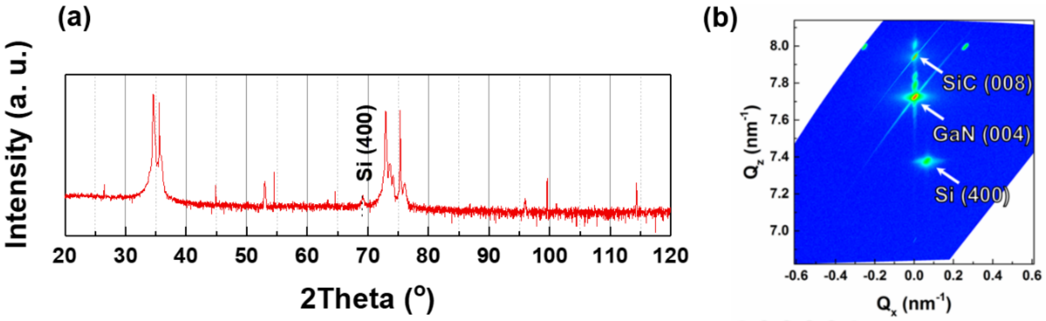
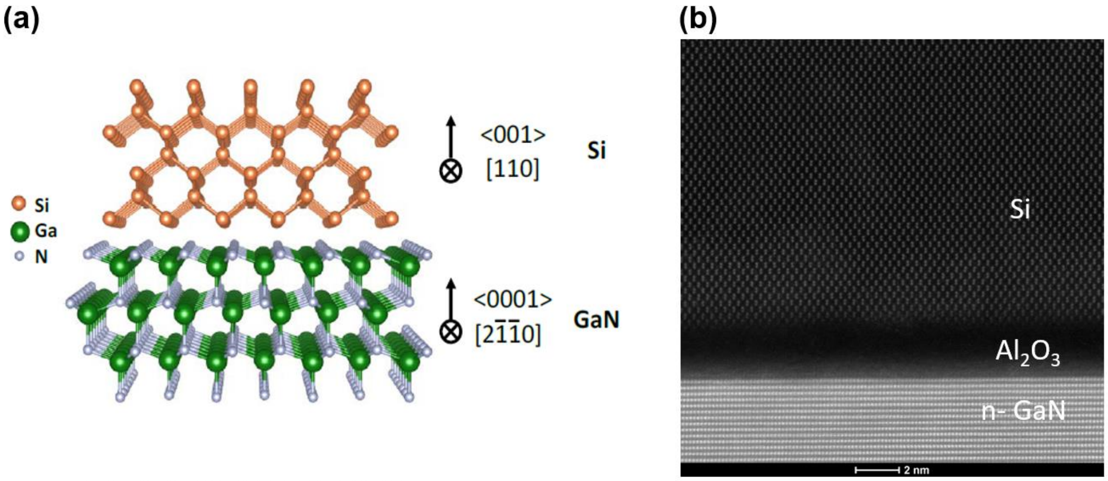


Figure 3.7 *X-ray diffraction study to check the crystallites of the film. (a)* the XRD scan of p+Si NM/GaN heterointerface *(b) Reciprocal space mapping (RSM) for p+Si NM on GaN on SiC substrate.*

d. TEM study of interface monolayer

Scanning Transmission Electron Microscopy (STEM) was carried out to verify interlayer conformation. Fig. 3.8 (a) shows an illustration of the crystal orientation of the Si/GaN heterostructure, and Fig. 3.8 (b) shows a STEM image of interface region of the Si/GaN heterostructure with the Al_2O_3 ultrathin layer. The crystallized regions which are Wurtzite structure GaN [43], diamond structure silicon, and amorphous Al_2O_3 properties were characterized. The Al_2O_3 ultrathin layer in the heterostructure is shown by the non-crystallized region. As shown in the Fig, 3.8 (b), no crystal defects or cracks were observed in the images. This shows that the Al_2O_3 acts as a thermal buffer layer for the thermal anneal and cooling process. Moreover, there is no interdiffusion between the layers, which indicates that the Al_2O_3 layer also acts as a diffusion barrier layer during the thermal process of heterostructure formation.



Crystal orientation illustration

TEM image of interlayer

Figure 3.8 *Cross-sectional Scanning transmission electron microscopy (STEM) micrograph p+Si NM/nGaN heterostructure with* Al_2O_3 *ultrathin layer. (a) Crystal orientation illustration of Si and GaN heterostructure (b) TEM image of interlayer compare with 2 nm scale bar.*

e. CTLM study of electrodes

To ensure low contact resistance for good device performance, contact resistance values of the Si NM and GaN substrate, which was processed using a low-temperature ohmic annealing step, were measured. The Transmission Line Method (TLM) structure formed on p+ Si NM (anode), and Circular Transmission Line Method (CTLM) structure n-GaN (cathode) layer have been investigated. For p+ Si NM involved not only have a significant lattice mismatch but also differ in their thermal expansion coefficients. The devices formed by the semiconductor grafting method should have performance comparable to devices fabricated using materials grown by conventional methods. In order to achieve this, having low thermal budget is required. Ohmic metallization is one of the fabrication steps that needs thermal annealing to form ohmic contact and so defines the thermal budget. Thus, we present a method to form low temperature Ni/Au ohmic contacts for the anode electrode to a p+ Si NM grafted to a Si dummy substrate with the same thickness of the Al_2O_3 ultrathin layer. Figure 3.9 shows the Transmission Line Method (TLM) study results of p+Si NM on Si substrate with Al_2O_3 ultrathin layer. The current-voltage (I-V) characteristics which were obtained using a Keithley 4200 semiconductor characterization system. The relationship between the total resistance R_T, sheet resistance R_S, width of the TLM metal pad W, TLM pad spacing L, contact resistance R_C is defined as: $R_T = (R_S/W)L+2R_C$. Therefore, $2R_C$ is deduced from the y-intercept of the fit line to R_T vs. L. The transfer length L_T is extracted from the negative x-intercept of R_T vs. L plot. Contact resistivity is then evaluated using $\rho_c = R_C \times L_T \times W$. The units of ρ_c are Ohms-cm^2. Fig. 3.9 (a) shows the schematic diagram of this structure before and after isolation process – it should be noted that the Ni/Au metal pads are between the etching holes. The final step of mesa isolation by RIE etches the p+ Si membrane/Al_2O_3 by using the anode electrode as a mask. For both the grafted-NM and SOI wafer rigid TLMs, the following TLM spacings (L) are studied: 5, 10, 20 and 40 μm, where the width (W) of the TLM pad is 28 μm. Fig. 3.9 (b) shows the *I-V* characteristics of the same TLM pattern on samples with different annealing conditions. In the low-voltage regime, linear *I-V* characteristic is observed for a temperature range of 300-400°C, while non-linear *I-V* curves are shown in both cases when no RTA annealing is done and when the anneal temperature is greater than 500°C. Fig. 3.9 (c) shows the study of R_C vs. anneal temperature done on six wafers per grafted and SOI rigid TLMs. Six samples are annealed at five different annealing temperatures (total of thirty samples) of 300°C, 350°C, 400°C, 500°C, and 600°C, each annealed for 60 seconds. One of the samples is not annealed and treated as a reference sample. The lowest ρ_c of 1.46×10^{-6} Ω-cm^2 is achieved at an annealing temperature of 350°C. This condition also has the lowest deviation, whereas other conditions without RTA and high temperature RTA (500°C and 600°C) have relatively higher distribution. We thought that this phenomenon came from the formation of NiSi after annealing process. XRD results for the reference sample shows Ni and Au diffraction peaks (Fig. 3.10 (a)) [44, 45]. The wafer that is annealed at 350°C exhibits nickel mono-silicide (NiSi) diffraction peaks (Fig. 3.10 (b)) [46-48]. Formation of NiSi, also called as the silicidation is proposed to be the cause of the observed low ρ_c. Silicidation causes boron-doping concentration to increase at the NiSi/Si interface which makes a more conductive p-layer [49, 50]. NiSi formation is also known to be stable over a low temperature window, and when the temperature goes beyond this window, either a phase transition occurs to a more resistive nickel disilicide ($NiSi_2$) and/or agglomeration happens [49]. Both phase transition and agglomeration are likely leading to the rise in ρ_c for temperature > 350°C in Fig. 3.10. This is confirmed in Fig 3.10 (c), where the XRD of an 800°C annealed wafer shows an absence of NiSi peak. The uniformity in ρ_c is also observed to increase as ρ_c itself increases. From these results, it looks like Ni silicidation also affects the uniformity of ohmic contacts. To sum up, we have confirmed an optimal annealing condition (350°C 60 s) for the p+Si NM Ni/Au metal annealing process.

Figure 3.11 shows the measured *I-V* characteristics with different spacings from the n-GaN (Ti/Al/Ti/Au) CTLM patterns – the CTLM measurements have already been explained in the previous chapter. The sheet resistance and contact resistivity results for both materials (Si and GaN) are summarized in Table 3.2. The p+Si NM and nGaN substrate have relatively low contact resistance values of 1.46×10^{-6} Ω-cm^2 and 1.72×10^{-5} Ω-cm^2 which were achieved from anode and cathode contact, respectively. The sheet resistances values for the Si NM and GaN are 75 Ω/□ and 51.49 Ω/□, respectively.

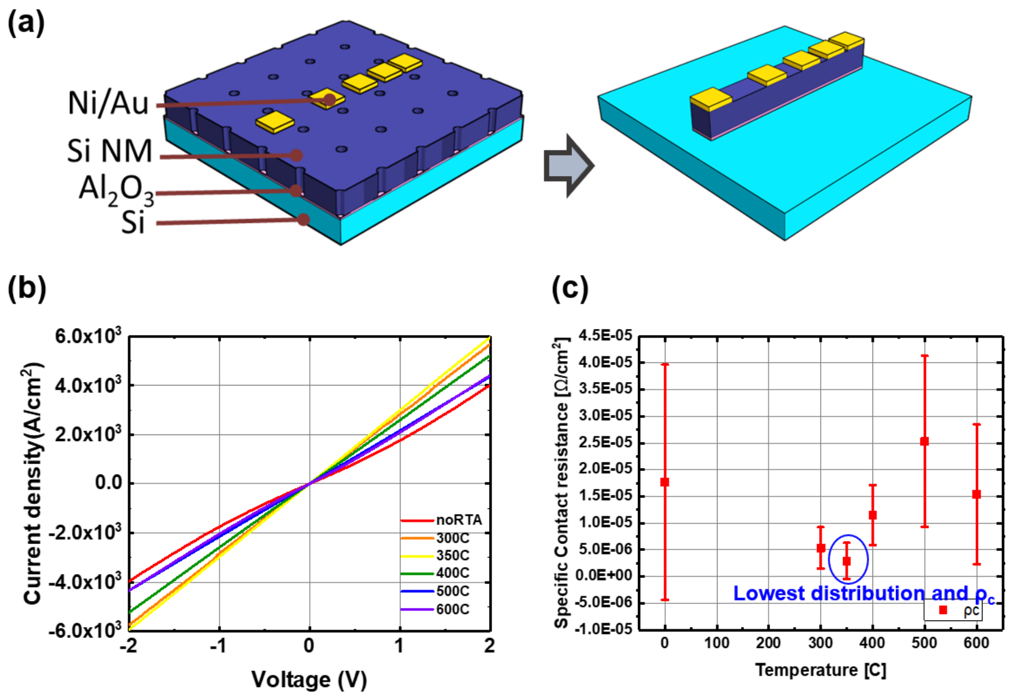


Figure 3.9 *Transmission Line Measurements (TLM) study. (a) Schematic diagram of TLM pattern on grafted p+Si NM on Si dummy substrate with* Al_2O_3 *ultrathin layer, (b) J-V characteristics of same TLM pattern under different annealing conditions, (c) Specific contact resistance (*ρ_C*) of p+Si NM metal contact (Ni/Au) with different annealing temperature.*

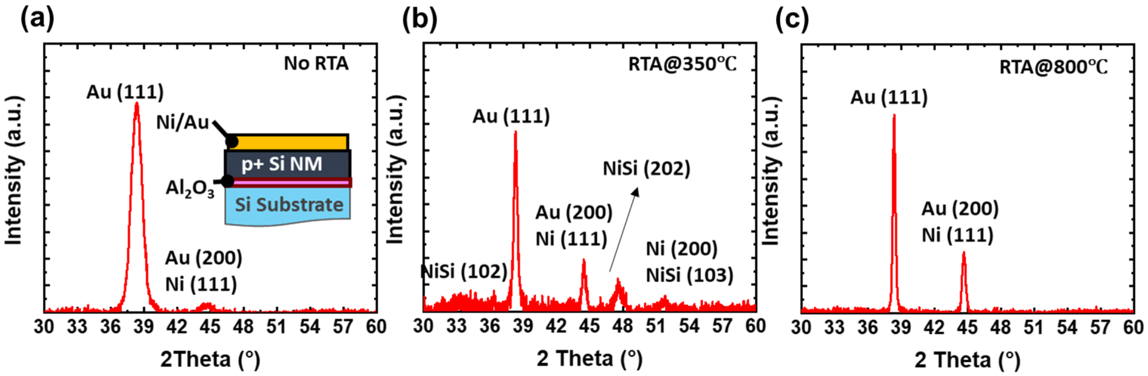


Figure 3.10 *X-ray diffraction (XRD) spectrum of Ni/Au on p+Si NM to check the formation of NiSi with different annealing conditions. (a) no RTA condition, inset: the cross section* schematic diagram of the *sample, (b) RTA at 350°C, (c) high temperature RTA at 800°C.*

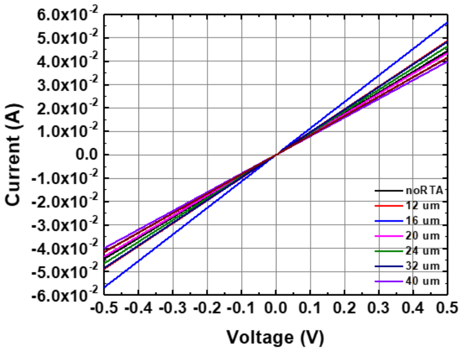


Figure 3.11 *Circular Transmission Line Measurements (TLM) study of n+GaN substrate.*

Table 3.2 *The sheet resistance (R_S ($\Omega/\square$)) and specific contact resistivity (ρ_c (Ωcm^2)).*

Material	$R_S(\Omega/\square)$	$\rho_C(\Omega\cdot \mathrm{cm}^2)$
p+Si NM	75	1.46x10^{-6}
n+GaN	51.49	1.72x10^{-5}

f. Electrical characteristic of diodes

Si/GaN heterostructure diode was fabricated using the new process condition explained in the previous section Figure 3.12 exhibits the electrical characteristic measurement results of a p+Si/nGaN heterostructure (Diamond-Wurtzite) grafted diode. Current–voltage (*I–V*) characteristics were measured and capacitance–voltage (*C–V*) characteristics were examined. The *J-V* curve is shown in Fig. 3.12 (a). p+Si/nGaN heterostructure grafted diode has a nearly ideal diode behavior. There are two insets for Fig. 3.12 (a) – the schematic diagram of the diode structure is shown on the top left, and top view optical microscope image of the anode and cathode is shown on the bottom right. This heterojunction diode has low level reverse-bias current density and high level forward current density. It also has long ideal region and reasonable series resistance region. *The J-V* curve shows an ideality factor of 1.14 for the p+Si/nGaN heterostructure in Fig. 3.12 (a). A reverse bias is driven up to 35 V to investigate the breakdown mechanism for this device, as plotted in the Fig. 3.12 (b), which shows a breakdown voltage of 28.4 V. The breakdown is attributed to a combined effect of avalanche multiplication and thermal instability [51]. As shown in Fig. 3.12 (c), to find out the band alignments for the heterojunction diodes under the influence of the interface with ultrathin Al_2O_3 layer to compare with simulation results, the flat-band voltage was extracted from the $1/C^2$ as a function of voltage plot at 1 MHz frequency. The value of flat-band voltage is 1.29 V, which was obtained from the intercept of the linear fitting. The band diagram of the p+Si/nGaN heterostructure was constructed based on the measured flat-band voltage, as shown in Fig. 3.12 (d). The difference between the theoretical and experimental values are traced back to the interface dipole and reflected as band upwards or downwards bending of the interfacial layer in Fig. 3.8 (c). On the other hand, the conduction band and valence band discontinuity shift accordingly, from the values determined by the electron affinities. The *C-V* characteristics, reverse bias current, and breakdown characteristic of the diode have proven the legitimacy of the ultrathin oxide interface approach for creating lattice-mismatch heterostructures.

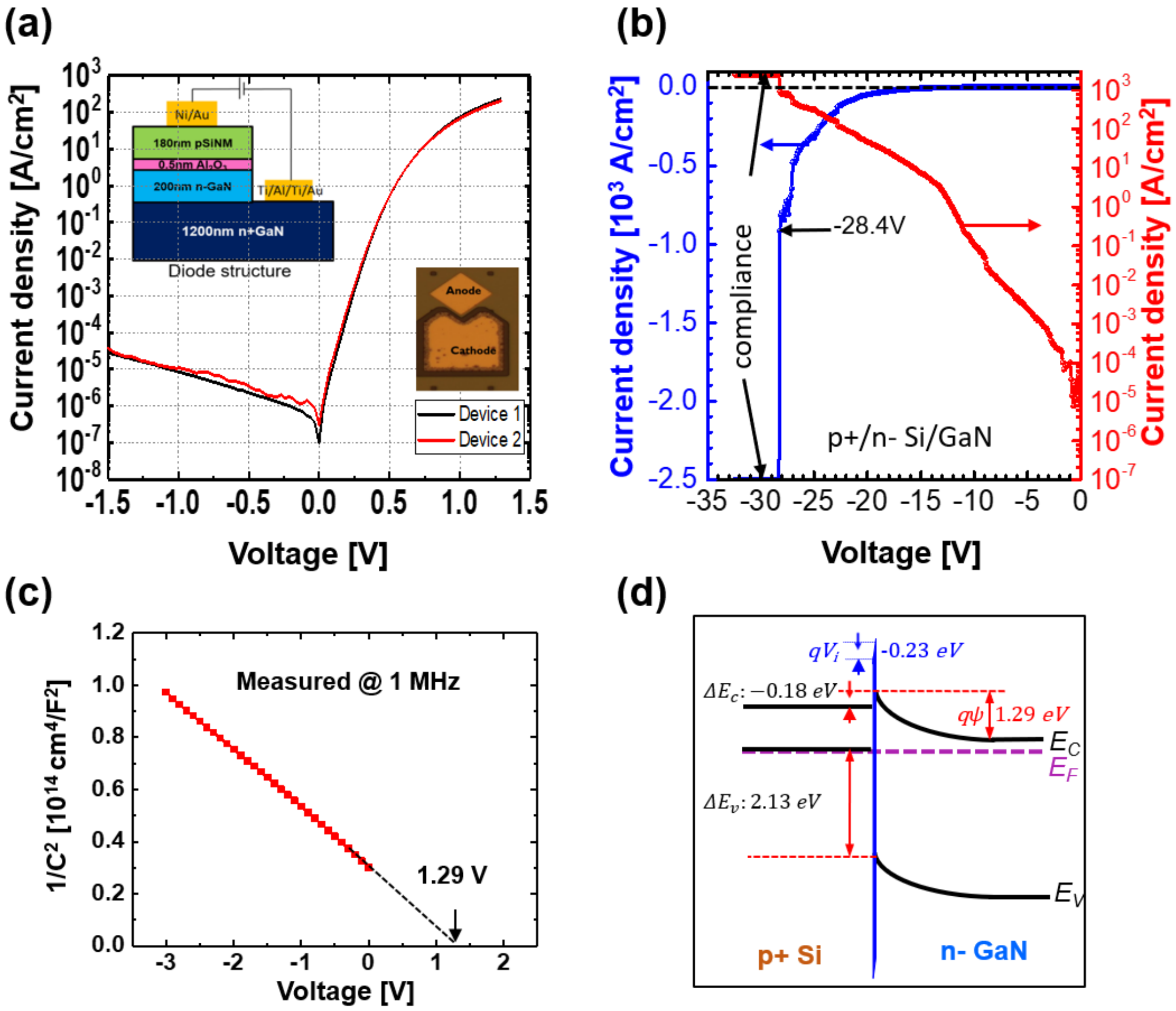


Figure 3.12 *Electrical characteristic of p+Si/nGaN heterostructure grafted diode, (a) Current density-voltage measurement, inset: schematic diagram of diode structure (left top), and top view of microscope image of anode and cathode (right bottom), (b) measured current density-voltage under reverse bias driven up to 35 V with the breakdown voltage of -28.4 V, (c) extracted flat band voltage from C-V measurement under 1 MHz which value is 1.29 V, (d) band diagram under equilibrium status with extracted flat band voltage.*

g. Comparison with other references

Table 3.3 compares the ideality factor, and I_{ON}/I_{OFF} ratio from our results to other results in the literature that uses the same material combination but did not use the semiconductor grafting method. In contrast with other combination of heterostructure diodes such as Ge/Si, or GaAs/GaN, only a few research groups have studied the Si/GaN combination. This is most likely because it is difficult to form this combination of heterostructure using conventional growth methods. As shown in Table 3.3, there is only one other Si/GaN diode reported, which was grown by molecular beam epitaxy [52]. It is clearly shown that the diodes prepared by the semiconductor grafting method with the ultrathin Al_2O_3 layer presents the lowest ideality factor (~ 1.14) and highest I_{ON}/I_{OFF} ratio (1.18×10^7 at ±1 V). The approximation of an ideality factor of 1.14 which is nearly around 1 points out the negligible proportion of current arises from the recombination centers, and no Fermi-level pinning effect occurs in the interfacial area. This is the fact that the diode current does not decrease by defect density [53]. The reduced defects states, due to the well-passivated interface using the ultrathin Al_2O_3 layer by ALD, is further verified by the suppressed leakage current under reverse bias.

Table 3.3 *Comparison with reference result with pSi/nGaN heterostructure.*

Heterojunction	**Method**	**Ideality Factor**	**I_{ON}/I_{OFF} ratio (@ ±1V)**	**Ref.**
pSi/nGaN	Molecular beam epitaxy	~1.5	$\sim 1 \times 10^3$	[52]
pSi/nGaN	Semiconductor grafting	1.14	1.18×10^7	This work

h. Uniformity of samples

To verify the uniformity of the samples, the current voltage characteristics for all the device in the sample were measured. There are 332 devices in the sample (Fig. 3.13 (a). To verify the uniformity in whole sample, the pixel mapping method was used (Fig. 3.13 (b). As shown in Fig. 3.13, one pixel represents the one device.

Figure 3.14 shows the results of pixel mapping. The values of ideality factor and current on/off ratio were plotted and shown in Fig. 3.14 (a) and Fig. 3.14 (b) respectively. As shown in Fig. 3.14(a), the range of ideality factor for all devices are between 1.08 to 2.6. The dominance range of ideality factor is 1.15 to 1.16, and 1/3 devices which is 107 diodes are in this range.

Figure 3.14 (b) shows the current on/off ratio characteristic. The represent current on/off ratio range is 1×10^2 to 1×10^7 and dominance range of current on/off ratio is 1×10^6 to 5×10^6. Also, as shown in Fig. 3.15, ideality factor and current on/off ratio follow the Gaussian distribution. It means that the uniformity of Si/GaN heterostructure diode is successfully verified and move to further works which is applying large scale grafting.

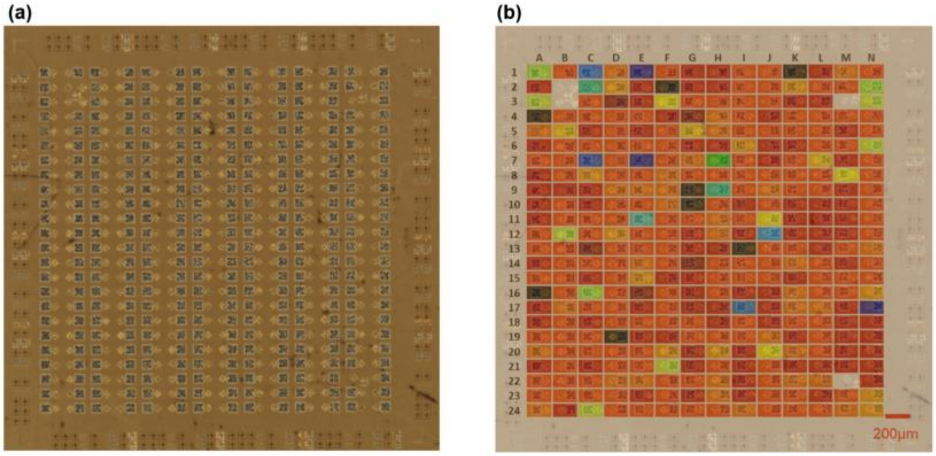


Figure 3.13 *Microscopic image of the samples. One pixel represents the one device. (a) Total 332 devices. (b) pixel mapping method.*

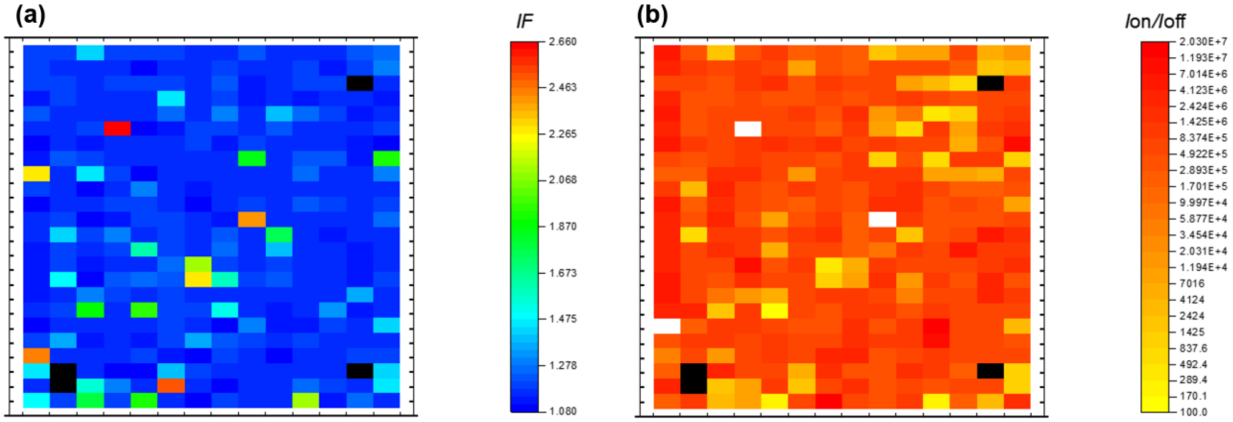


Figure 3.14 *Pixel mapping result of whole device. (a) Ideality factor. (b) Current on/off ratio.*

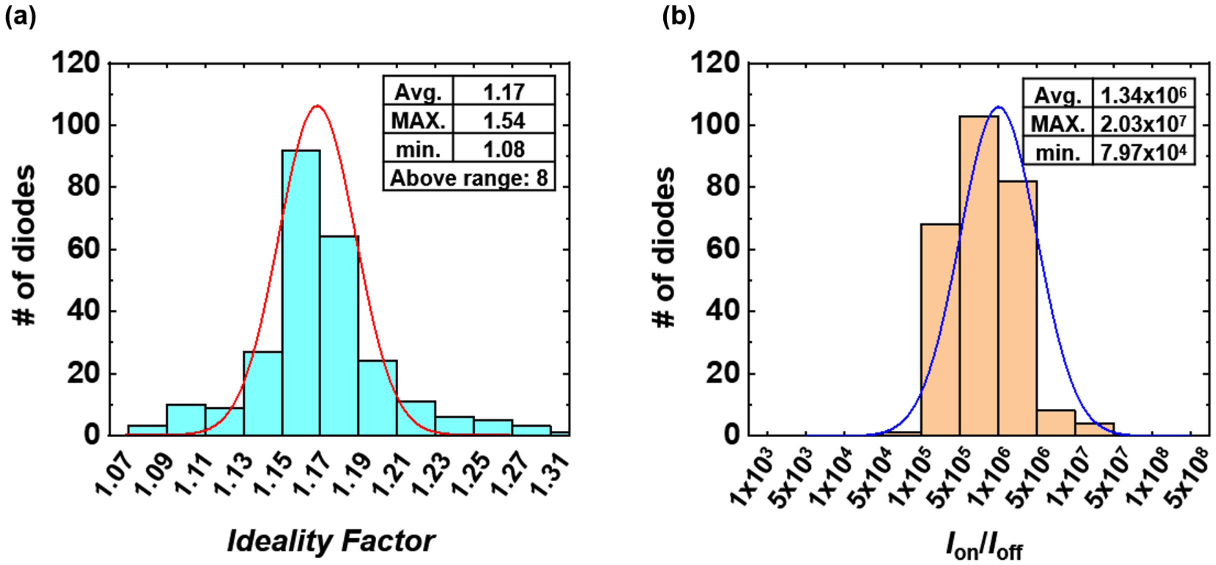


Figure 3.15 *Gaussian distribution of whole device. (a) Ideality factor. (b) Current on/off ratio.*

i. Future works

This is future work for Si/GaN diode structure using semiconductor grafting technique. As you see in Fig. 3.16, even though the diode in Fig. 3.12 has an impressive performance, there is still room for improvement. Thanks to modify design of structure and process like annealing condition, the performance of device was increased that almost meet the ideal characteristic of diode. The ideality factor has achieved 1.02 and current on/off ratio at +-1V is 4.39×10^{8}. It is lower ideality factor and more than one order higher current on/off ratio than the result in table 3.3. Also, applying to the industry field for semiconductor grafting technique, verifying the possibility of this technique to apply to the wafer-scale should be needed. It is one of the major obstacles that we must solve. Many colleagues and collaborators have made an effort to make a successful result for more than two years. To conduct semiconductor grafting on 2inch wafer, there are tons of 1x1mm unit cells with connecting anchors (Fig. 3.17). Figure 3.17 (a) shows the All layers of CAD file of 1×1 unit cell design with anchors. These anchors playing a critical role in grafting process. Thanks to anchor, even though we failed to graft one-unit cell, this result did not affect to neighbor unit cell. Figure 3.17 (b) shows the CAD file design for 2-inch wafer which has total 1569 unit cells. Figure 3.17(c) shows the microscope image of grafted unit cell. Figure 3.18 shows the result of SiNM grafting in 2-inch host substrate. Large scale silicon nanomembrane was grafted to a 2-inch host substrate. The number of the total unit cell is 1569, and only 19 unit cells were failed to graft. More than 98% of the yield was shown in this result. Area #1 shows 64 grafted unit cells without any defects, area #2 shows the result from a successfully grafted unit cell, and area #3 shows failed grafted one. The four anchors on the edge side of the unit cell are blocked to spread failed results to neighbor unit cells. Figure 3.18 (b) shows the images 2inch silicon grafted result. Using 2-inch semiconductor grafting technique, uniformity, reliability and performance should be confirmed like small scale samples.

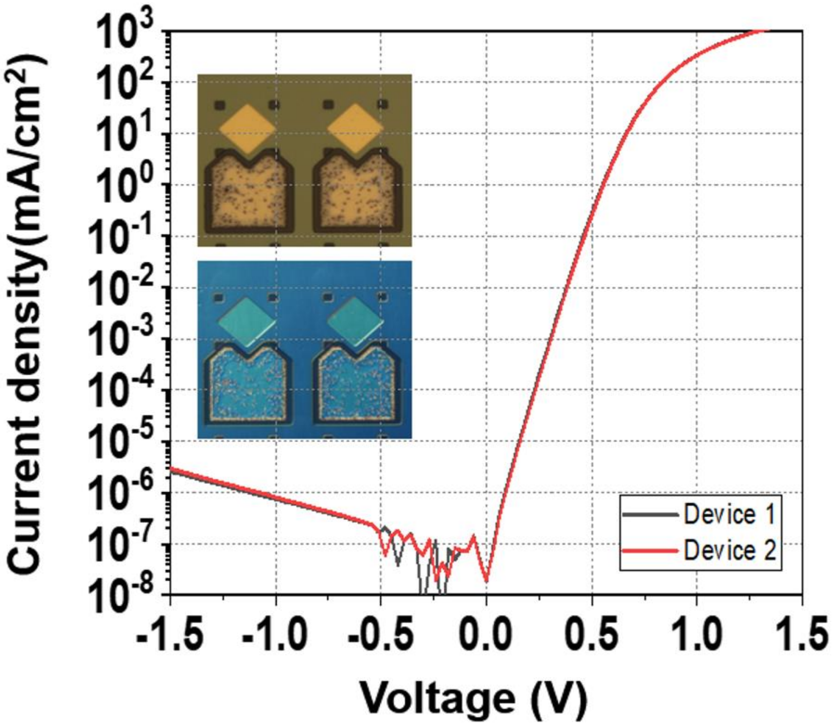
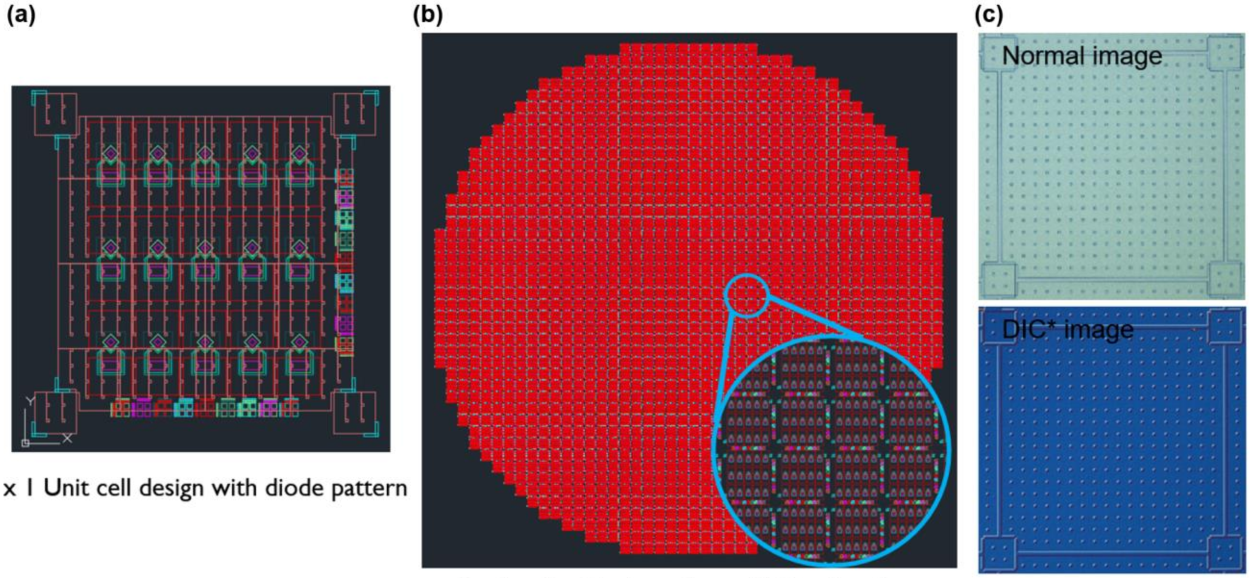


Figure 3.16 *IV characteristic of modified Si/GaN diode.*



x 1 Unit cell design with diode pattern

Design for 2inch wafer - 1569unit cells

Figure 3.17 *Design for 2-inch large scale grafting. (a) 1x1 Unit cell design with all diode layers. (b) CAD file design for 2-inch wafer which has total 1569 unit cells. (c) microscopic images of an unit cell.*

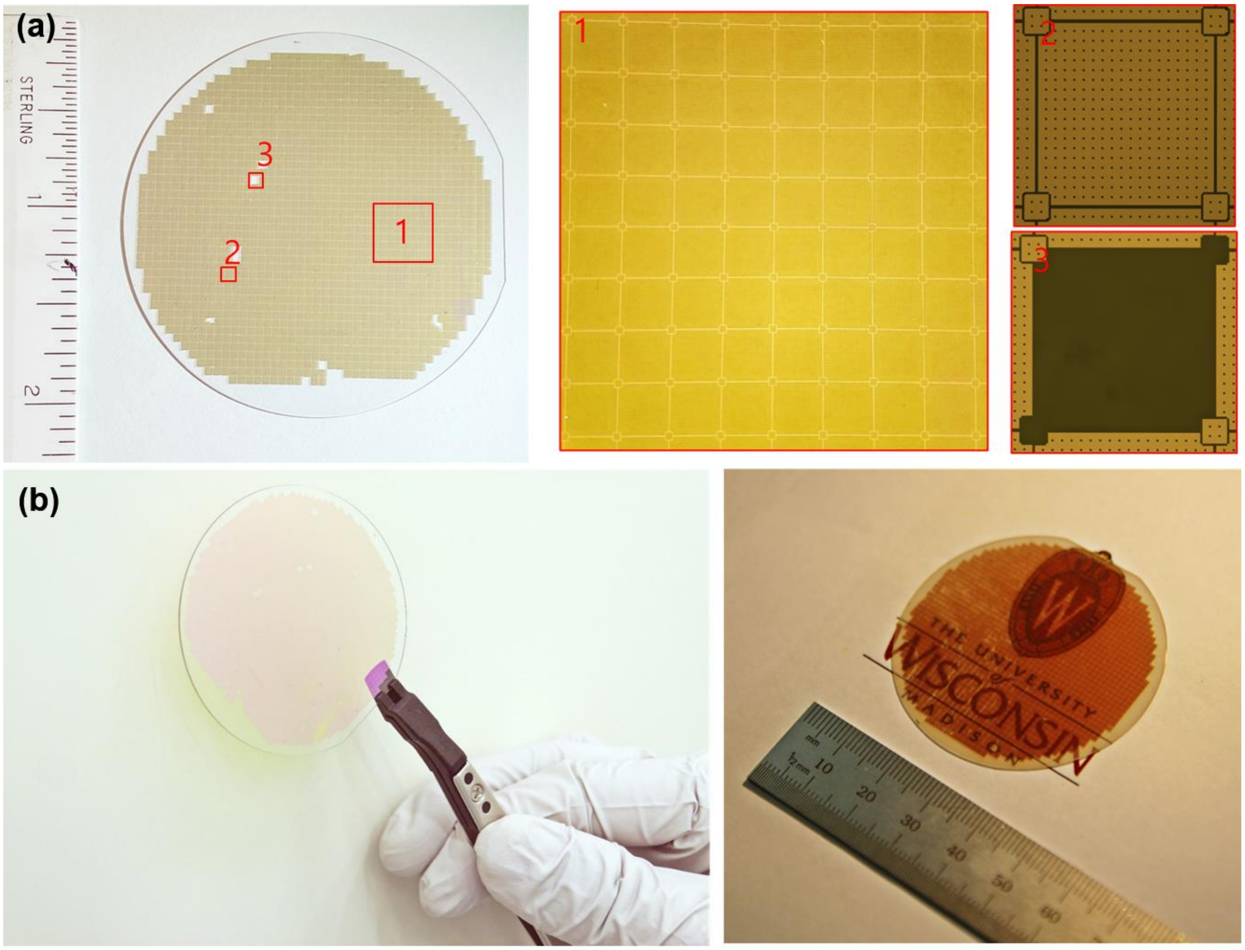


Figure 3.18 *the result of SiNM semiconductor grafting in 2-inch. (a) images of large-scale grafted result. Area #1: images of 64 grafted unit cells. Area #2: successfully grafted unit cell. Area #3: failed grafted unit cell.*

3.4 Conclusions

To sum up, a Diamond-Wurtzite heterostructure diode of p+Si NM on nGaN formed by the semiconductor grafting technique with the ultrathin Al_2O_3 tunneling layer has been successfully demonstrated. The semiconductor grafting technique gives lots of freedom to form superior performance heterostructures without considering lattice mismatch and thus allows us to create lots of combination of semiconductors with broader band offset.

In this chapter, to verify the semiconductor grafting technique, several measurement studies have been conducted. First, AFM measurements were carried out to observe the surface roughness of the interface. This is because below 2 nm R_{rms} of interface is one of the criteria of successful semiconductor grafting. Second, Raman spectroscopy and X-ray diffraction measurements were performed to evaluate the strain of the film and the crystallinity of the film, respectively, after semiconductor grafting and bonding annealing process. Both measurement results prove the successful formation of a heterostructure without strain while keeping their own crystallinity. Third, a STEM study was followed to investigate the interface of two semiconductors with ultrathin Al_2O_3 layer by ALD. The results show the effective function of the Al_2O_3 layer at the interface – it acts as a thermal buffer, a diffusion barrier, and a passivation layer. Finally, the electrical properties have been studied. Using the optimized metal contact annealing, the heterostructure diodes in this work remarkably outperforms other diodes from the literature that uses the same Si/GaN structure when comparing typical diode figures-of-merit such as the ideality factor and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio – 1.14 and 1.18×10^7 at ±1 V, respectively. The rapid ramping up of the current under forward bias and low dark current under reverse bias with the large on-and-off ratio at ±1V of 1.18×10^7 indicate that there is no existence of noticeable electric resistance between the interface and ultrathin Al_2O_3 tunneling layer.

In conclusion, these results show that the semiconductor grafting technique can provide another pathway in demonstrating various types of heterostructure devices, such as fast speed and large bandgap three-port devices (HBTs, HEMTs), which will be described in the next chapter. Again, to form heterostructure between two arbitrary types of semiconductors without considering lattice match can open tons of opportunities for material engineering and enable much broader applications in photonic devices, optical devices, and power devices. Moreover, it also satisfies the demand of future applications – high speed, high power to autonomous vehicle system and other technologies.

3.5 Reference

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CHAPTER 4

Diamond-Collector Heterojunction Bipolar Transistors (HBTs)

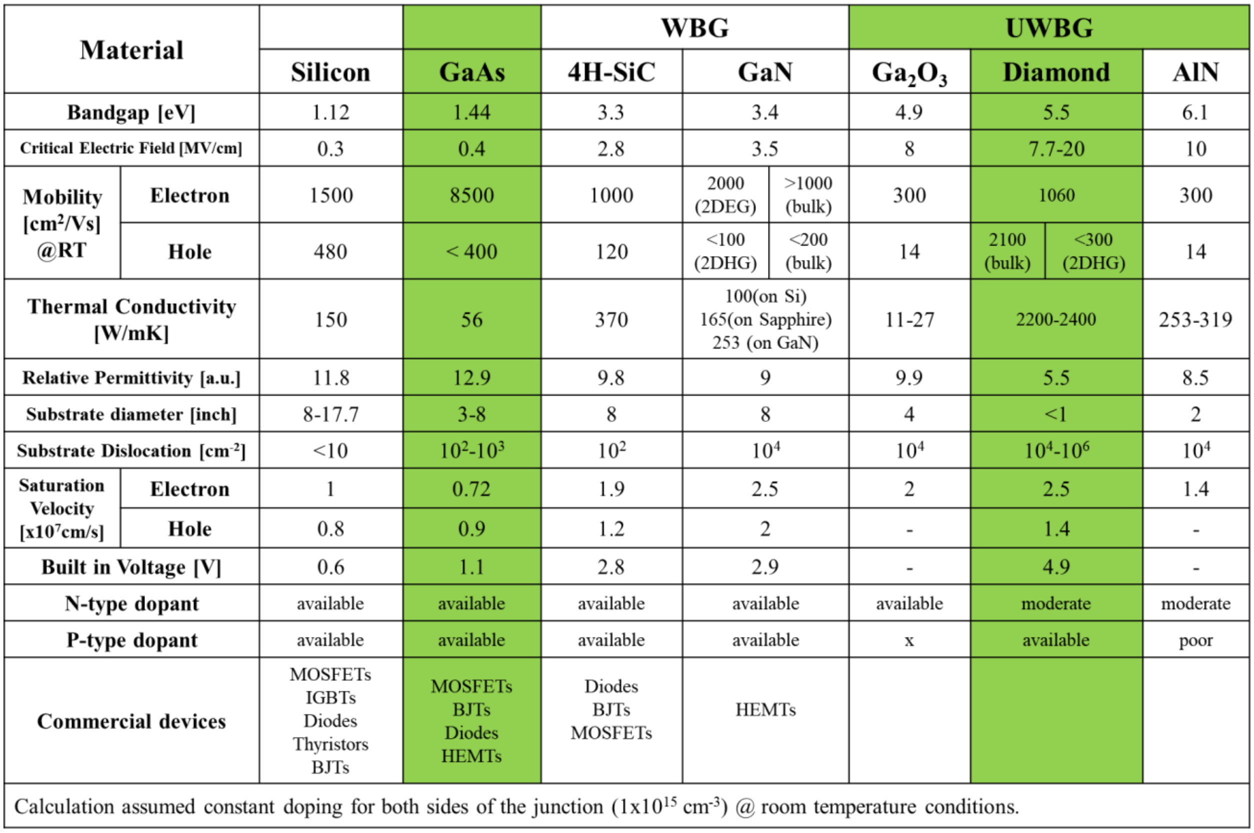
4.1 Introduction

Today, it is impossible to imagine the world without semiconductor technology. Our modern lifestyle relies heavily on a variety kinds of semiconductor devices including domestic and industrial applications. The demand of smaller and faster microelectronic devices with high power operation requires continuous investigations of semiconductor materials. Furthermore, in the near future, all the electronic devices will have more compact and integrated design. It leads to the issue of heat dissipation. However, as shown in previous chapter in Figure 1.6, currently most used semiconductor material, silicon, cannot fulfill the power level requirements because of its physical limitation. To satisfy these demands, a new generation of semiconductor materials should be taken in account. In this context, since early of 2010s, semiconductor devices comprising of wide bandgap (WBG) and ultra-wide bandgap (UWBG) materials have been researched in many groups to apply their advantages such as efficiency, compact device area, heatsink and passive filter volume reduction, radiation hardness and switching frequency , which are superior over conventional silicon devices [1-3]. Several wideband gap materials such as SiC and GaN have been successfully commercialized. Thus, they already set their position in the left side of the silicon devices in Figure 1.6. Thanks to their superior electrical properties—large bandgap, high carrier mobilities, high breakdown voltages, thermal and mechanical stability, SiC and GaN are the best candidates for high power, high frequency applications [4-6]. When it comes to non-commercialized material, the ultra-wide bandgap (UWBG) materials such as Ga_2O_3, AlN and Diamond also have been researched, too. As shown in the Table 4.1, diamond material has by far the best material properties [7]. Diamond is one of the most prospect materials in nature. Diamond is an allotrope of carbon, which belongs to the fourth column of the periodic table along with silicon and germanium. Also, diamond represents the ultimate material for single element semiconductors [8]. Compared to other WBG or UWBG semiconductors, diamond has superior advantages such as its high hole-electron mobility, critical electric field, the highest known thermal conductivity, and the widest bandgap. It has also distinctive characteristics: electron emission at surfaces and band gap control with hydrogen and oxygen termination of surfaces [9-13]. These extraordinary properties let diamond become an ideal candidate for many applications. However, because of its cost and rarity, diamond has not been commonly used and researched in several decades. With recent progress in diamond synthesis of the improvement of the quality of diamond growth using high pressure high temperature (HPHT) and Chemical vapor deposition (CVD) methods, the new era of power electronics has been emerged [14-19]. The n-type doping and wafer size limitation of diamond substrates are still waiting for improvement to commercialize like GaN or SiC [8]. The n-type doping by nitrogen or phosphorous has still obstacle to forming high electron densities, thus this kind of doping is insufficient for high performance devices. For this reason, there are two device applications: p-type channel filed effect transistors (FETs) and Schottky diodes, which have been researched heavily recently. [20-77]. Besides, compared to

FETs, bipolar junction transistors (BJTs) are surely needed in certain situations such as device controlling by current, operating faster beyond the limit of conventional silicon, obtaining larger gain bandwidth and so on. Specifically, a key limiting physical trade-off for dynamic range is to achieve high power amplification at the maximum possible voltage swing (signal). The most common example of this trade-off the amount of maximum power in which the devices can normally operate is in GaN FET technology when scaling the drain voltage results in huge current swings. For this reason, our approach in this chapter shows the alternative way through a new kind of HBTs that maximizes common base amplifier performance. The new way is possible because the new HBT configuration ties power gain directly to voltage gain in devices with inherently high power densities and that operate at higher voltages. Instead of n-doping of diamond that poses a huge challenge, the semiconductor grafting process can be applied to integrate designed III-V emitter-base layer to diamond collector. As shown in Figure 4.1, the schematic diagram of HBTs comprising of AlGaAs/GaAs NMs as an emitter and base, respectively, on the diamond sub collector. Diamond substrate grown by HPHT method is shown in Fig. 4.1 (b), and HBTs fabricated on diamond is shown in Fig 4.1 (c). The dimension of both diamond substrates is 4×4 mm^2. Due to high speed and linearity characteristics of III-V materials (AlGaAs/GaAs), and the ultra large bandgap with high breakdown characteristic of diamond, high-performance heterojunction bipolar transistor will be realized.

In this chapter, firstly, I am going to explain material characteristics of both III-V and diamond. Also, advantage of using III-V semiconductor and diamond will be discussed in terms of a new class of HBT that maximizes common base amplifier performances. Several measurements were performed to investigate this structure. Moreover, preliminary test results are also shown in this chapter. Details of fabrication process and device performance will be explained in this chapter. Finally, to improve the current gain, I am going to suggest several ways to modify the structure for future directions.

Table 4.1 *The comparison of material properties of silicon, GaAs, WBG and UWBG semiconductors in terms of power applications. In this chapter 4, GaAs and diamond are handled and marked green [7].*



Material				**WBG**			**UWBG**			
		Silicon	**GaAs**	**4H-SiC**	**GaN**		**Ga_2O_3**	**Diamond**		**AlN**
Bandgap [eV]		1.12	1.44	3.3	3.4		4.9	5.5		6.1
Critical Electric Field [MV/cm]		0.3	0.4	2.8	3.5		8	7.7-20		10
Mobility [cm^2/Vs] @RT	**Electron**	1500	8500	1000	2000 (2DEG)	>1000 (bulk)	300	1060		300
	Hole	480	< 400	120	<100 (2DHG)	<200 (bulk)	14	2100 (bulk)	<300 (2DHG)	14
Thermal Conductivity [W/mK]		150	56	370	100(on Si) 165(on Sapphire) 253 (on GaN)		11-27	2200-2400		253-319
Relative Permittivity [a.u.]		11.8	12.9	9.8	9		9.9	5.5		8.5
Substrate diameter [inch]		8-17.7	3-8	8	8		4	<1		2
Substrate Dislocation [cm^{-2}]		<10	10^2-10^3	10^2	10^4		10^4	10^4-10^6		10^4
Saturation Velocity [x10^7cm/s]	**Electron**	1	0.72	1.9	2.5		2	2.5		1.4
	Hole	0.8	0.9	1.2	2		-	1.4		-
Built in Voltage [V]		0.6	1.1	2.8	2.9		-	4.9		-
N-type dopant		available	available	available	available		available	moderate		moderate
P-type dopant		available	available	available	available		x	available		poor
Commercial devices		MOSFETs IGBTs Diodes Thyristors BJTs	MOSFETs BJTs Diodes HEMTs	Diodes BJTs MOSFETs	HEMTs					
Calculation assumed constant doping for both sides of the junction (1x10^{15} cm^{-3}) @ room temperature conditions.										

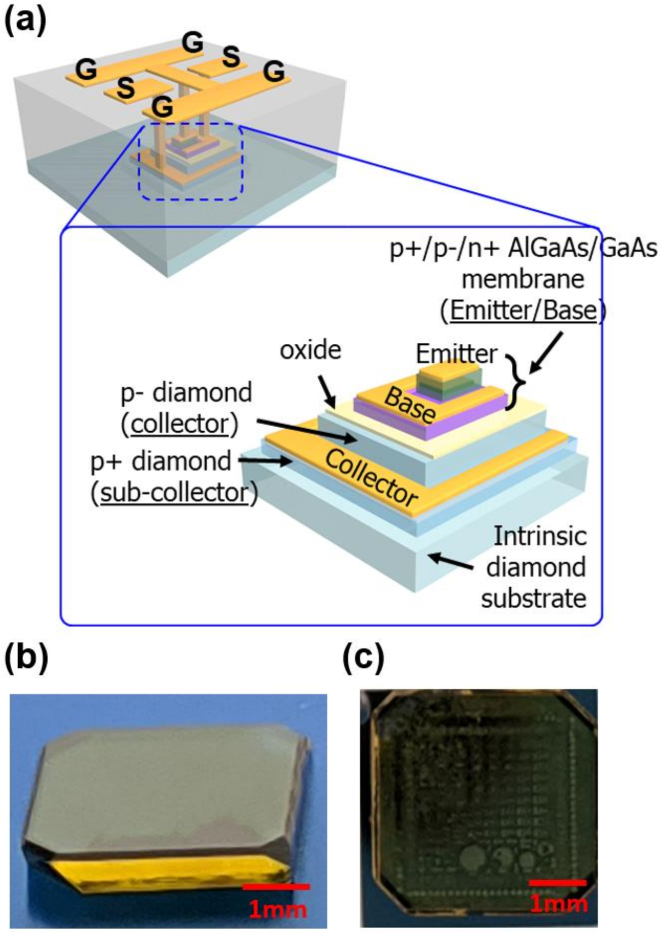


Figure 4.1 *The structure of AlGaAs/GaAs/Diamond (Emitter/Base/Collector) for heterojunction bipolar transistors via semiconductor grafting process. (a) Schematic diagram of HBTs device, (b) HPHT growth diamond substrate, (c) fabricated HBTs on the diamond substrate. The scale bar is 1mm in both images.*

4.2 Trends in diamond power semiconductor devices

As the relatively great activation energy of the n-type dopants, nitrogen and phosphorous, leads to low free-electron density in diamond semiconductor, it is challenging to achieve high-performance devices with those dopants [8]. Thus, two major applications such as p-type channel filed effect transistors (FETs) and Schottky diodes, have been researched in the past [20-77]. In this section, the state-of-the-art diamond power devices will be reviewed in terms of critical performance factors.

Diode application takes an essential part in power-device functions such as power converters, filters, and free-wheeling application. The superior characteristics of boron-doped diamond devices–operating performance in high temperature and a great saturation velocity–allow them to have a high breakdown voltage and the lower ON state resistance ($R_{\mathrm{on\_spec}}$). The lesser $R_{\mathrm{on\_spec}}$ at the same breakdown voltage brings the wafer size reduction which leads to have lower input capacitance and higher switching frequency [78]. As shown in Table 4.2, diamond Schottky diodes, as one kind of unipolar mode devices, have been mainly researched regarding boron-doped layers. The early diamond Schottky diodes were reported in 1990s [79-81], with the first successful CVD growths of boron doped diamond layers. A high blocking voltages (up to 10 kV [24]) and critical electric field (7.7 MV/cm [34]) have been reported the literatures. Several Ampere have been measured for the diodes [36] and high temperature operations (over 525 K) have been investigated without any degradation of the Schottky properties [20-23, 26, 28, 31, 32, 35, 36, 42, 47, 50, 52]. Because it is very challenging to grow self-standing diamond crystal with both of low resistivity and self-standing property, pseudo vertical diamond structure has been usually developed to bypass those difficulties [27, 29, 34, 39, 51]. Despite of those obstacles in growing n-type diamond layer, a few groups have successfully fabricated PIN diamond diodes [33, 37, 41, 49]. Compared to unipolar-mode diodes, bipolar-mode diodes possess a few advantages which originate from the high built-in voltage of the p-n junctions. One of the examples is a significant ON-state voltage drop. This mode can be used for high voltage applications in a situation where more than 10 kV of external bias is necessary [49].

In terms of diamond FETs, over the last two decades, FETs fabricated on H-terminated surface have mainly been investigated as a leading area of diamond-transistor research. The basic structure was introduced by Kawarada [82]. Owing to superior electrical properties of diamond semiconductor, the material seems to be an ideal candidate for niche electronics in extreme conditions. No other semiconductor can compete against diamond with regard to the material properties and expected performance in Table 4.1. Nevertheless, many technical limitations–size of substrates, lack of shallow n-type dopant–need to be solved in order to achieve the high performance introduced above. As shown in the Table 4.3, there are many published FETs works with various approaches. First, the most researchers have focused on the Heterojunction Field Effect Transistor (HFET) taking advantage of the unique property of H-terminated diamond surface. The H-terminated surface induces Two-Dimensional Hole Gas (2DHG), which is used for a conductive channel for the devices. 2DHG was proved to be an innovative way to obtain an almost-zero activation energy for a hole channel. This channel with a sheet charge density in the 10^{13} cm^{-2} range is fully activated at room temperature. Many research groups have been reported their performance value with different combination of oxide and metal layer and gate structures [58, 60, 62, 64-67, 74, 76]. Second, Shikata group have fabricated several diamond MESFETs, exploring different Schottky gate metals (Mo, Pt, Al). A high breakdown voltage (>2kV) with a normally-ON characteristic and a high threshold voltage (V_{th}) have been observed in the diamond MESFETs whose typical gate-to-drain distance is 50μm. Promising scalability on a gate-to-drain distance has been proved for diamond MESFETs [57, 83-85]. The other approaches to fabricate FETs are based on a different active-layer design focusing on thin and heavily-boron doped layers. These p–n + junctions in diamond JFET have been fabricated by Yamasaki group [71-73]. Diamond semiconductor is highly reliable for power electronics applications due to absence of gate oxide layers which tend to generate high density of interface states [72]. In terms of Metal Oxide Semiconductor (MOS), an ideal structure needs MOS interface in high quality. Thus, various kinds of diamond-oxide interface have been suggested such as Al_2O_3, ReO_3, No_2/Al_2O_3, HfO_2, MO_3, Nb_2O_5, V_2O_5, WO_3, Ta_2O_5, and ZrO_2 [86]. Depending on surface treatment on gate metal, the best combination of oxide and gate metal varies, and is generally related to a behavior of a gate leakage current. Deep-depletion diamond MOSFETs experimentally relies on Al_2O_3/Ti/Pt/Au stack layers. A high breakdown field 4MV cm^{-1} has been reported for a normally-ON device [61, 75, 77]. Diamond Fin-FET with CVD boron doping in HPHT undoped substrate has been investigated by using E-beam lithographic process. Those works exploit the lesser metal work function of Al and SiO_2 layers whose thickness is 45nm, and the depletion width is about 55nm which is a half of the fin channel width [75]. All the research indicate that diamond seems to be an ideal material for niche electronics in extreme conditions. However, compared to silicon-based devices, diamond-related works are still at its beginning phase of development. Recent progress in the diamond growth and doping technique will potentially lead to pioneer new possibilities for innovative diamond electronic concepts.

Table 4.2. *State-of-the-art diamond diodes research results with parameters and key factors*

#	Device type [diode]	Doping [cm^{-3}]	$J_{\text{on state}}$ [A/cm^2]	V_{br} [V]	I_{on}/I_{off}	Notes	Ref.
1	Schottky diodes	P : 8.2×10^{16}	10@4V	N/A	N/A	Thermionic field-modelling theory	Shikata group [31]
2	Schottky diodes	P- : 10^{17} P+ : 10^{20}	0.2A@7V	N/A	N/A	0.5inch diamond wafer	Shikata group [28]
3	Schottky Diodes	P-: 10^{15} P+: 10^{20}	500@5V	N/A	10^{10}@5V @RT	Ru/diamond Schottky diodes	Shikata group [20]
4	Schottky Diodes	P-: 10^{13} P+: 10^{19}	1@10V	2500V	10^{7}	*A circular gold Schottky contact*	Johansson group [21]
5	Schottky Diodes	P-: 10^{16} P+: 10^{20}	30@10V	N/A	10^{9}@10V @RT 10^{2} @10V @1100K	Very high temperature	Kohn group [22]
6	Schottky diodes	P : 1.2×10^{15}	10^{-1}~10^{-4} @ 2V	N/A	N/A	Wet-chemical oxidation	Ito group [35]
7	Schottky diodes	P- : 7.5×10^{14} P+ : 5×10^{20}	4×10^{-4} @ 15V	N/A	10^{5}@15V	-	Deneuvile group [23]
8	Schottky diodes	P- : 10^{15} P+ : 10^{16}	-5mA @ 5V	N/A	10^{11}@5V	Operating at 250C	Shikata group [26]
9	Schottky diodes	P : 10^{17}	70@6V	N/A	10^{4}@15V	High temperature/voltage	Asano group [32]
10	Schottky diodes	P : 10^{18}	2.5@5V	N/A	N/A	Fast response	Volkov group [52]
11	Schottky diodes	P : 1.2×10^{15}	0.1@3V	N/A	10^{9}@3V	Low leakage by using UV treatment	Ito group [92]
12	Schottky diodes	P : 4×10^{14} ~ 5×10^{16}	N/A	6500V	N/A	High voltage	Wright group [50]
13	Schottky diodes	P : 10^{16}	1@4V	N/A	10^{10}@ 4V	Fast switching/high forward current	Teraji group [42]
14	Schottky diodes	P : 10^{18}	62.5@4V	>400V	N/A	10A forward current	Blank group [36]

#	Device type [diode]	Doping [cm^{-3}]	$J_{\text{on state}}$ [A/cm^2]	V$_{br}$ [V]	I_{on}/I_{off}	Notes	Ref.
15	Schottky PN diodes (SPND)	N : 2×10^{17} P: 2×10^{20}	3×10^4 @ 8V	N/A	10^7@ 8V	*Nitrogen doping*	Tokuda group [38]
16	SPND	N : 10^{18} P-: 7×10^{16} P+: 6×10^{18}	5×10^3 @ 6V	N/A	10^{10}@ 6V	Fast switching operation	Yamasaki group [40]
17	SPND	N : 10^{18} P+: 5×10^{20}	10^5 @ 8V	-58V	10^{13}@ 8V	No trade-off relation b/w on-resistant and blocking voltage	Yamasaki group [60]
18	SPND	N : 5×10^{19} P : 9×10^{19}	10^{-7} @ 10V	N/A	≈1@10V	Reverse I-V Characteristic	Goodnick group [38]
19	SPND	P+: 5×10^{20} N-: 10^{16}-10^{17}	10000@7V	N/A	5×10^3	Temperature dependence	Yamasaki group [40]
20	Pseudo-vertical Schottky diodes (PVSD)	P : 1.5×10^{15}	1000@8V	N/A	10^{13}@8V	Zr/oxidized diamond interface	Perno group [34]
21	PVSD	P- : 5×10^{15} P+: N/A	125 @ 1.5V	N/A	1250 @ 1V	Integrated temperature sensor	Rouger Group[39]
22	PVSD	P- : 10^{16} P+: 5×10^{20}	0.05A @ 7V	N/A	10^{12} @7V	Device scaling	Shikata Group [29]
23	PVSD	P: 1.38×10^{17}	3000@8V	N/A	Very large	High temperature application	Shikata group[27]
24	PVSD	P- : 1.2×10^{16} P+: 2×10^{17}	50@1.9V	N/A	Very large	Ion-beam assisted lift-off technique	Blank Group [51]
25	PIN diodes	N : 7×10^{17} P: 4×10^{14}	N/A	900V	N/A	High-voltage application	Yamasaki group [38]
26	PIN diodes	N : 10^{20} P: 5×10^{20}	300@50V 10^{-7}@-200V	>600V	Very large	Reverse recovery of PIN dioes	Yamasaki group [33]
27	PIN diodes	N : 10^{20} P : 10^{20}	10^{-3} @ 8V	N/A	10^9@ 8V	Heavy doping	Yamasaki group [41]
28	PIN diodes	N : 5×10^{19} P : 10^{20}	N/A	-1000V	N/A	High voltage (100)-/(111)-substrate	Chowdhury group [49]

***Table 4.3**. State-of-the-art diamond FET research results with parameters and key factors.*

#	Device type	Doping [cm^{-3}]	I_{DS} [mA/mm]	μ [cm^2/Vs]	V_{br} [V]	Figures	Notes	Ref.
1	MOSFET	P++: ~1×10^{20} (50 nm) N-: ~1×10^{17} (10 µm)	1.6 @ 300K V_{GS}=-5V V_{DS}=-1V L_G: 5 µm	8.0	<50 V @300K	5 µm G length, Al_2O_3 passivation	Low BV, First proof of concept	Yamasaki group [77]
2	MOSFET	N: ~×10^{17}	-80@673K V_{DS}=-10V V_{GS}=-4V	N/A	1000V@ 673K	>5 µm G length	Wide temperature/high voltage	Hiraiwa group [68]
4	Vertical FinFET	P+ : 10^{19} P- : 5×10^{16}	<1 @ 300K <10 @ 450K V_{DS}=-15V V_{GS}=-16V	N/A	>16V @300K	FinFET	Fin channel allows for normally-OFF operation	Tsang group [75]
5	MESFET	P : 10^{15}	-0.06@ V_{DS}=-10V V_{GS}=30V	N/A	>1500V	5µm~30µm G length	High BR voltage	Shikata group [57]
6	JFET	P: ~10^{17} N-: ~8×10^{19} (7 µm)	2µA @573K V_{DS}<-10V	N/A	>600V @300K	7 µm G length	Positive temperature coeeficient of the BV	Yamasaki group [71-73]
7	JFET	P:~1.5×10^{16} N+:8×10^{19}	N/A	N/A	N/A	0.26 µm channel width	V_{th}: -3V "Normally-off" operation	Hatano group [59]
8	HFET	P : 10^{16} N : 5×10^{14}	-400@ V_{DS}=-10V V_{GS}=-3.5V	33-35	N/A	0.1 µm G length	Nitrogen Dioxide atmosphere	Kasu group [66]
9	HFET	N/A	37.6@ V_{DS}=-12V V_{GS}=-9V	38.7	N/A	4 µm G length/ HfO2 passivation	HfO2 gate	Koide group [65]
10	HFET	P: 10^{14} N-: 10^{16}	1300@300K V_{DS}=-12V V_{GS}=-5V	N/A	>2kV@300K	15 µm G length	Lateral current limits the resistance	Kawarada group [67]
11	Lateral HFET	N : 10^{14}	175@ V_{DS}=-10V V_{GS}=-10V	N/A	N/A	Triple gate 5µm G length	Triple-gate	Koide group [64]
12	Lateral HFET	N/A	1300@ 300K V_{DS}=-12V V_{GS}=-5V	N/A	>2000@ 300K	Al2O3-passivation 150nm G length	Lateral current limits resistance	Moran group [60]
13	Lateral HFET	N/A	-550@ V_{DS}=-10V V_{GS}=-3V	N/A	N/A	100nm G length	Beneficial for RF application	Coe group [58]
14	Lateral HFET	P : ~1×10^{14}	-900@ V_{DS}=-6V V_{GS}=-5V	N/A	N/A	N/A	Al_2O_3-passivation layer (RF)	Kasu group [76]
15	Vertical HFET	P : 10^{14} N : 10^{19}	200@ 300K V_{DS}=-50V V_{GS}=-20V	74~98	350V@ 300K	Al2O3-passivation 10µm G length	Beneficial vertical current from P+layer	Kawarada group [62]
16	Vertical HFET	P: ~3×10^{19} N-: ~1×10^{18} (3 µm)	>0.2 @300K/600K V_{DS}=-50V V_{GS}=-20V	N/A	350V @300K	20 µm G length Al_2O_3 passivation	Beneficial vertical current spreading only starts from the p+layer	Kawarada group [74]

4.3 Reviews of each material and methods

a. Diamond (Collector) substrate

First, brief touch of diamond crystal structure with basic band structure, diamond is a metastable allotrope of carbon atoms. Each carbon atom is covalently bonded with other neighbor four carbon atoms with its atoms arranged in a variation of the face centered cubic crystal structure called a diamond lattice. These carbons bonds with neighbors are 1.54 Å, and the lattice constant of diamond is 3.566 Å. The simple tetrahedral structure with symmetry and strong covalent bonds is the main reason of the distinctive properties of diamond. Thanks to its atomic structure, diamond has superior properties - High bandgap (5.47 eV), high critical electric field (7.7 - 20 MV/ cm) which allows operation at high voltages, the high thermal conductivity (~ 22 W/cm·K at RT) which means the power devices have their own intrinsic heat spreader leading to high heat dissipation efficiency during operation, and high hole mobility (> 2000 cm^2/ V·s) which allows high-speed, high-frequency operation and low dielectric constant (5.7) which able to improve the high-frequency characteristics.

Figure 4.2 shows that diamond has the uncommon ability to isolate massive voltages with a small fraction of the material. Direct compare with Silicon, for isolating 10,000V, the amount of diamond needed is 50 times less than that of silicon. Moreover, it also has the unique ability of heat dissipations. Table 4.4 shows the basic material properties comparison relative to silicon. Diamond, compared to other wide bandgap semiconductor such as GaN or SiC, has lots of merits for high performance devices [4-6, 87, 88]. In order to evaluate semiconductor materials on the capability of high-speed-power operation, researchers have estimated the figure of merits (FoMs) by using the Johnson Figure of Merit (JFM) shown in Equation 4.1 where E_{CRI} is critical electric field, v_{sat} is drift saturation velocity [88]. The JFM focused on power electronics operating at high frequency. Moreover, there is another factor which shows the switching speed and heat dissipating capabilities of transistor which is called Keyes Figure of merit (KFM) shown in Equation 4.2 where λ is thermal conductivity, c is the speed of light (3×10^{8}m/s) [87] The JFM and KFM of diamond material are, respectively, more than one-thousand times and twenty times as much as those of silicon. Thus, these FoMs values indicate that the performance of diamond devices potentially exceeds those of devices fabricated with conventional materials, especially in the following characteristics: a high breakdown electric field, a highest thermal conductivity, a greater mobility and a saturation velocity of carriers, and a low dielectric constant. Even though diamond power devices are very promising, the research on them is still at its initial phase, meaning that many follow-up research should be conducted to catch up with other wide-bandgap semiconductors which were successfully commercialized for power electronics like GaN and SiC.

$$JFM = \left(\frac{E_{\mathrm{CRI}}\times v_{\mathrm{sat}}}{2\times\pi}\right)^{2} \tag{4.1}$$

$$KFM = \lambda\sqrt{\frac{c\times v_{\mathrm{sat}}}{4\times\pi\times\epsilon_{r}}} \tag{4.2}$$

Related with this chapter, for high dynamic range applications, the revolutionary performance metrics in high power, power added efficiency (PAE), and linearity is required at the device level. A key limiting physical trade-off for dynamic range is to achieve high power amplification at the maximum possible voltage swing (signal). For this reason, our approach is to focus on meeting the program goals through a new class of HBTs that maximizes common base amplifier performance because this configuration ties power gain directly to voltage gain in devices with inherently high power densities and that operate at higher voltages. In state-of-the-art SiGe circuits, common-base amplifiers are often used to extract the maximum device-level performance. Unfortunately, the dynamic range is limited severely by supply voltage (collector breakdown) and in mixed-signal processes with digital devices by the lower voltages associated with digital scaling. In other technology related with InP HBTs can cover above 500 GHz. While, for the THz level, this technology also has been severely limited collector breakdown fields and scaled emitter dimensions exclude them from consideration for total power and dynamic range (signal levels on loads during power amplification). Also, the reliability of scaling device is worried because of increased electric field and operation current density, which lead to enhanced avalanche multiplication and raised junction temperature [89]. To solve this problem, diamond is one of the best materials in terms of extreme high critical electric fields value which is 7.7-20 MV/cm. The lightly doped diamond collector provides a trade space for achieving a high collector breakdown voltage HBT. Moreover, diamond is a good heat handling and dissipating capabilities.

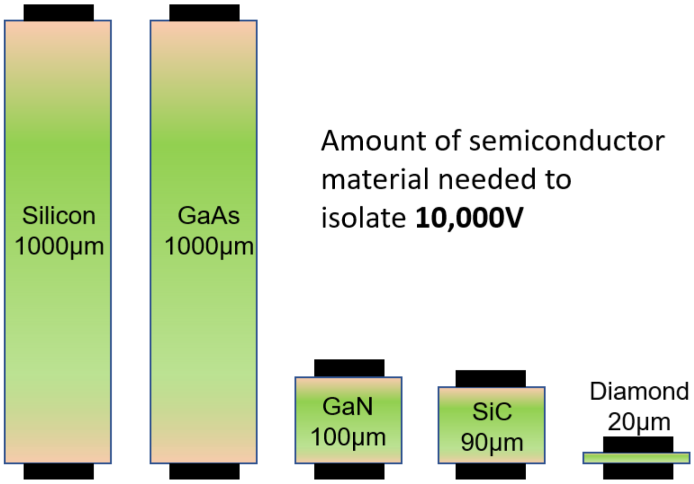


Figure 4.2 *The intuitive comparison of amount of semiconductor material needed to isolate 10,000V.*

Table 4.4 *Basic material properties comparison relative to silicon.*

Property (relative to silicon)	**Si**	**GaAs**	**GaN**	**SiC**	**Diamond**
Critical electric field	1	1.3	9.3	12	**26-67**
Thermal conductivity	1	0.4	1.1	2.5	**~15**
Thermal expansion coefficient	1	1.6	2.2	1.6	**0.03**
Dielectric constant	1	1.1	0.8	0.8	**0.5**
Saturated carrier velocity	1	0.9	2.5	1.9	**~1.4**
JFM ratio	1	1.4	850	315	**1300-8700**
KFM ratio	1	0.3	2.0	3.7	**>25**
Depending on parameters, the values of FoMs vary.					

For diamond substrate preparation was conducted by expert diamond group which is Fraunhofer USA in Michigan State University. They have unique capability in diamond materials development across substrates, epitaxy, and doping. In addition, this process requires high quality diamond polishing (R_{rms} < 2nm) which is a critical element for our approach and a notoriously difficult process due to inheritance characteristic of diamond, but one in which we have expertise.

HPHT (100) surface single crystal diamond (SCD) was grown with 3° angle from (100) plane substrate. The HPHT synthesis allows to achieve high purity with a low defect density. However, there is size restriction due to inherent limitations of this technique. Commercially available HPHT substrates can be found in 2×2 mm^2 to 10×10 mm^2. In this work, 4×4mm^2 HPHT substrates were used. Laser cutting was used to make specific size diamond substrate. After cutting the sample, the samples were mechanically polished and which roughness is enough to deposit p- and p+ doping with boron by microwave plasma CVD system that uses feed gases of hydrogen, methane and diborane. After mechanical polishing process, cleaning process was proceeded to remove residue using RIE system. To precise control of light and heavy boron doping process, each process was separated in different reactors. The deposition temperature was 800°C to 1000°C. The heavy doping was conducted first with ~$1x10^{20}$/cm^3 and light doping was followed below $1x10^{16}$/cm^3. The doping level was check by four-point probe measurement (Fig. 4.3 (a)). The deposition thickness was measured by gram difference. The doping concentration was confirmed by SIMS measurement. For semiconductor grafting technique, below 2nm RMS roughness should be needed (Fig. 4.3 (b)). Thus, after microwave CVD growth for p+ and p- layer doping, CMP process was conducted to form a flat surface. The CMP slurry included phosphoric acid, potassium permanganate and boron carbide powder with DI water. Due to diamond intrinsic characteristic, CMP rate is slower than other material which is 10 - 20 nm per an hour. Figure 4.4 (a) and (b) shows the diamond surface morphologies before and after 4hrs CMP process, respectively. After finish diamond substrate preparation, diamond was cleaned in boiled acid (H_2SO_4:HNO_3 3:1 at 100 °C, 20 min, HCl at 70 °C, 20 min) and piranha cleaning for 10min. Then surface treatment was conducted. It will explain in section (c).

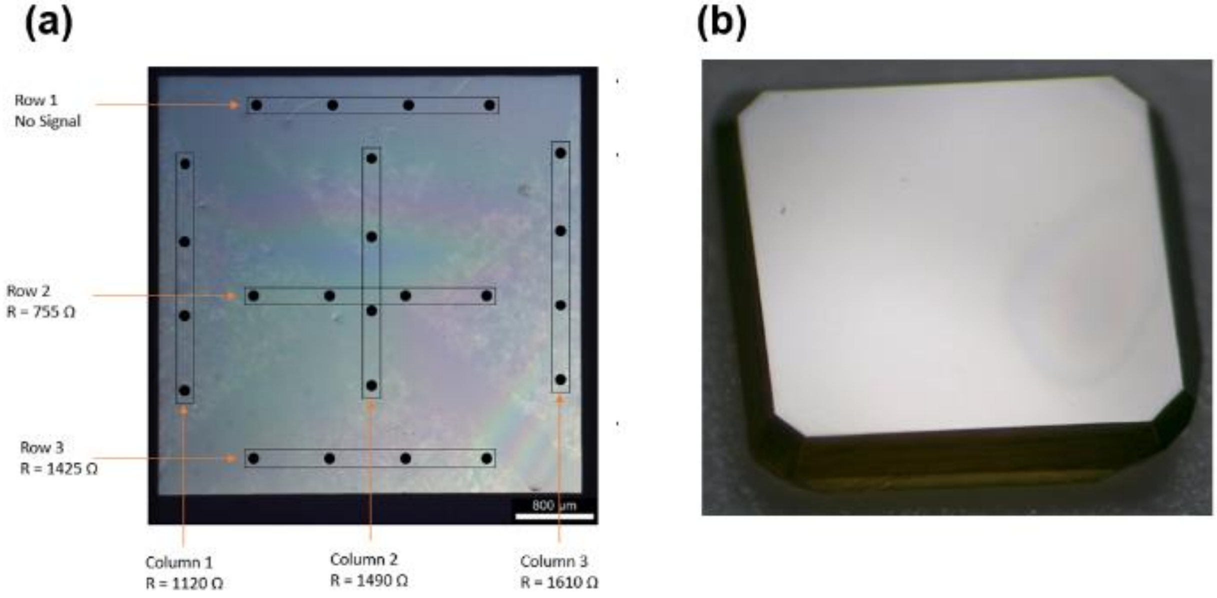


Figure 4.3 *(a) four-point probe measurement to check doping level, (b) very smooth diamond substrate*

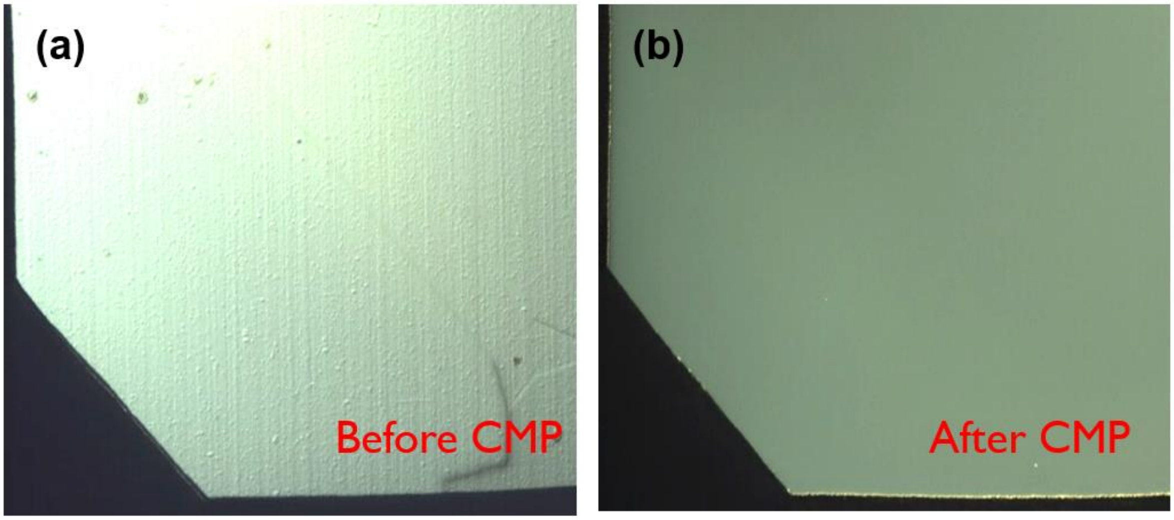


Figure 4.4 *The diamond surface morphologies with ×100 magnification microscope, (a) surface image before CMP, (b) surface image after 4hrs CMP.*

b. AlGaAs/GaAs (Emitter-Base) NMs

The most stumbling block for diamond doping is the absence of shallow donors and acceptors due to the small lattice of diamond. Currently, boron for p-type doping, and nitrogen and phosphorous for n-type doping are considered for suitable the impurity doping [90]. Unlike boron for p-type doping, nitrogen or phosphorous n-type doping are not that effective enough to produce high electron densities so far [8]. To fabricate bipolar devices, LEDs both types doping are necessary. Instead of n-doping difficulty of diamond, the semiconductor grafting process can be applied to form bipolar structures.

The choice of the emitter/base (E/B) junction is complicated because it has to be simultaneously fabrication compatible, have the appropriate band alignment, and perform at the highest level. There are several candidates to consider for the emitter and base. One candidate is p-n Si/Ge. For this combination, two semiconductor grafting layer processes would be needed, so the fabrication challenge (yield risk) is severe. Also, the major issue with Si/Ge is the large band offset in the valence band (0.51 eV) at the emitter-base heterojunction. To mitigate this problem, another compromised candidate is using a Si_xGe_{1-x} alloy, where x is small (0.1-0.2). However, a tight-tolerance balance is needed between current gain (β) and the energy spike at the E-B junction, and material supplier problems which we considered to be impractical. Otherwise, the E-B structure that we found to be suitable is (p/n) $Al_{0.3}Ga_{0.7}As$ and GaAs. For this combination, the valence band offset is only 0.04 eV and a total E-B band offset of 0.37 eV, which is ideal for the proposed pnp HBT. After finishing the determination of emitter/base structure at the material level, the doping condition and the emitter thickness (We) should be designed. The emitter AlxGa1-xAs thickness is 120 nm to optimize frequency response and the composition is x=0.3 to provide the best emitter injection efficiency without degrading the resistance such so that frequency performance would be degraded. The band offset between $Al_{0.3}Ga_{0.7}As$ and GaAs is sufficient for providing a high DC current gain (β). For the emitter doping profiles, a p+ GaAs will be used as emitter cap. The emitter $Al_{0.3}Ga_{0.7}As$ doping level is set for ~10^{17} /cm^3. The base doping and base thickness are set to heavier than emitter which is ~10^{19}/cm^3 order and few tens of nm, respectively. Since GaAs and AlGaAs growth are mature, we will not optimize these device parameters initially, but rather focus on improving the ideality factors for the emitter-base diodes. The 400 nm $Al_{0.95}Ga_{0.05}As$ layer was used as a sacrificial layer for the semiconductor grafting process. The structures of the E-B junction were carefully simulated with Silvaco^{TM} using the Monte Carlo method. The epi-layer on top of GaAs substrates is patterned with etching hole and sequential 30s of boron trichloride (BCl_3) 10 sccm, and Argon 5 sccm etching with a Plasma Therm SLR series inductively coupled plasma (ICP) etcher until the sacrificial $Al_{0.95}Ga_{0.05}As$ layer is exposed. After cleaning the photoresist on the top of the surface, then the sample is ready to further semiconductor grafting process.

c. Diamond surface treatment with ALD Al_2O_3 deposition

Before Al_2O_3 deposition on the diamond, the cleaned diamond surface was treated by oxygen or hydrogen to modify the electron affinity. The surface termination of diamond has a critical impact. Each termination states creates different electro-chemical properties of the devices. The most crucial part of the surface termination is related with bandgap. The surface electronic states inside of the bandgap may lead to Fermi-level-Pinning (FLP) effects and surface dipoles which form various the electron affinity of the diamond semiconductor [91].

To be specific, Oxygen termination has a positive electron affinity (PEA) of 1.7 eV. It is normally applied to improve the adhesion of oxide and diamond layers. To induce O-terminated surface, ozone treatment and immersion in hot mixed acid are commonly used [92]. Several species of bonding (C=O, C-OH, C-O-C, C-O-O-C) can be formed at the surface during the oxygen treatment. Oxygen terminated diamonds are mainly used for the passivation layer and the removal of the hole-type conductive layer which is generated at the hydrogen terminated diamond surface [67]. However, the main drawback of oxygen termination surface is the high FLP problem which generated by high density interface states. It can affect the electrical properties of metal oxide semiconductor (MOS) structures [93].

Otherwise, hydrogen terminated (H-terminated) diamond surfaces has a negative electron affinity (NEA) of > -1 eV [94, 95]. To obtain H-terminated surface, plasma treatment or hot filament method are commonly used, and these methods have been researched due to their unique property of surface conductivity with C-H bond diamond surface. Although the mechanism of surface conductivity is not well understood yet, the adsorbates on C-H bond on H-terminated diamond substrate and the local exchange of charge with the diamond valence band are plausible way for explanation of the formation of the 2DHG in diamond FETs. Recently, 2DHG has been demonstrated on C-H surfaces passivated with Al_2O_3 oxide [96, 97].

According to Silvaco simulation, we obtained specific electron affinity value (~ 0.1 eV) to form desired band alignment to balance hole transport and electron emission. One of our project teams in SUNY Buffalo's effort, electron affinity of diamond can be precisely tuned using a H_2O treatment in ALD system at 300°C. It means that H-terminated surface treated to less H-terminated surface. Also, we have been developed the method to verify the electron affinity value instantly using contact angle measurement. The original method to find electron affinity immediately is ultraviolet photoelectron spectroscopy (UPS) [98]. Unlike X-ray photoelectron spectroscopy, UPS (He 1 discharge lamp which is corresponding to an energy of 21.2 eV) can obtain accurate work function from the secondary cut off, while XPS only shows the binding energy [99]. Firstly, the sample was measured by UPS to get the reference value of electron affinity. Then, we directly matched electron affinity to the value of contact angle. The number of H_2O pulse can change the degree of contact angle. It means that each contact angle is corresponding with specific electron affinity value. We have repeated this experiment several times with different the number of H_2O pulses. Finally, we found that depending on the number of H_2O pulses, the contact angle was changed linearly and can control the electron affinity by using H_2O pulses treatment in ALD system. The detail data of surface treatment is explained in results and discussion section.

d. Fabrication of HBT

After semiconductor grafting process with AlGaAs/GaAs EB NMs and the ultrathin Al_2O_3 film on top of the surface treated diamond collector, the fabrication process has been followed the conventional top-down process with lithography, etching, and deposition.

Figure 4.5 shows AlGaAs/GaAs/Diamond HBTs mask design. As you shown in the CAD design (Fig, 4.5 (a)), different sizes and types of HBTs patterns are in the small 4×4mm^2 diamond substrates. We have tried to put lots of devices with variations. For small RF pattern, interconnection pattern is designed to measure RF performance. The critical dimension is 2.5 μm between the emitter and base metal fingers. Fig. 4.5 (b) shows fabricated HBTs with interconnection metal pads.

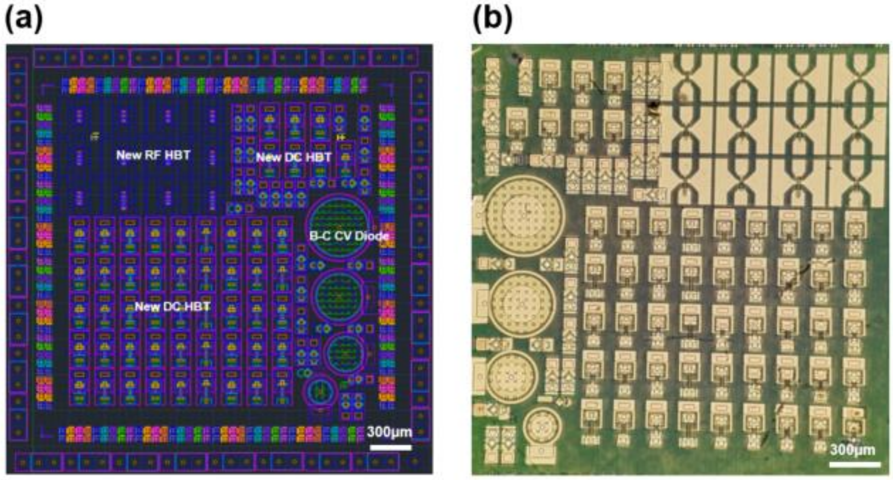


Figure 4.5 *III-V/Diamond HBTs mask design, (a) Mask CAD file, (b) real sample images after isolation, the scale bar is 300 μm.*

The whole fabrication of AlGaAs/GaAs/diamond pnp HBTs process after semiconductor grafting process was shown in Figure 4.6. The detailed semiconductor grafting process is explained in 3.2.c parts in previous chapter. 3. After bonding AlGaAs/GaAs emitter-base structure to diamond collector, Ti/Pt/Au (15/50/100 nm) was deposited on the p+GaAs layer on the p-AlGaAs emitter side shown in Fig. 4.6 (a). above two images show microscope images of the emitter metals on the EB NMs. The black dots in the NMs are etching holes. Next, one of the critical etching steps which is emitter layer etching to achieve the base GaAs NM. The base thickness is extremely thin (25~45nm), so etching test with dummy was proceeded in advance every time. As shown in above microscope image, the color of NM was different because of the NM thickness difference. After successfully finish the etching, current level can be confirmed by *I-V* measurement of n+ base layer. The emitter metal was worked as a masking layer and etching was proceeded by a Plasma Therm SLR series ICP plasma Etcher. A base metal stack of Pd/Ge/Au (30/40/100 nm) was deposited on the n+ GaAs layer (Fig. 4.6 (c)). The microscope images represent RF and DC HBTs with different finger lengths and gaps between emitter and base layers. Afterwards, emitter-base mesa was formed by etching away the remain base membrane followed by p-diamond layer etching to achieve p+ layer. For diamond etching, typically, metal mask was used []. However, for the special structure with semiconductor grafting process was not able to use metal mask as usual. So, we used photoresist mask and modified the etching recipe of RIE with carbon tetrafluoride (CF_4) gas. The schematic diagram and microscope images of mesa etching process is shown in Fig. 4.6 (d). Like before, the current level of p+ diamond layer can be confirmed by *I-V* measurement. Last metal deposition step was proceeded on the p+diamond layer to form collector metal which is Ti/Pt/Au (50/50/100 nm) followed by simultaneously ohmic annealing was carried out at 350 °C for 15 s in N_2 ambient (Fig. 4.6 (e)). Finally, interconnection process was conducted which involved 700nm SiO_2 deposition for passivation by Plasma Therm Plasma-enhanced chemical vapor deposition (PECVD), via open etching with RIE, and final interconnection metal was deposited (Ti/Al/Ti/Au, 25/1650/25/100 nm). The oxide passivation layer was determined by height difference between top emitter metal to bottom diamond substrate and interconnection metal was followed by passivation layer thickness. The final interconnection metal shapes are represented in Fig. 4.6(f) with schematic diagram to help to understand final structure. The schematic diagrams are not a real scale.

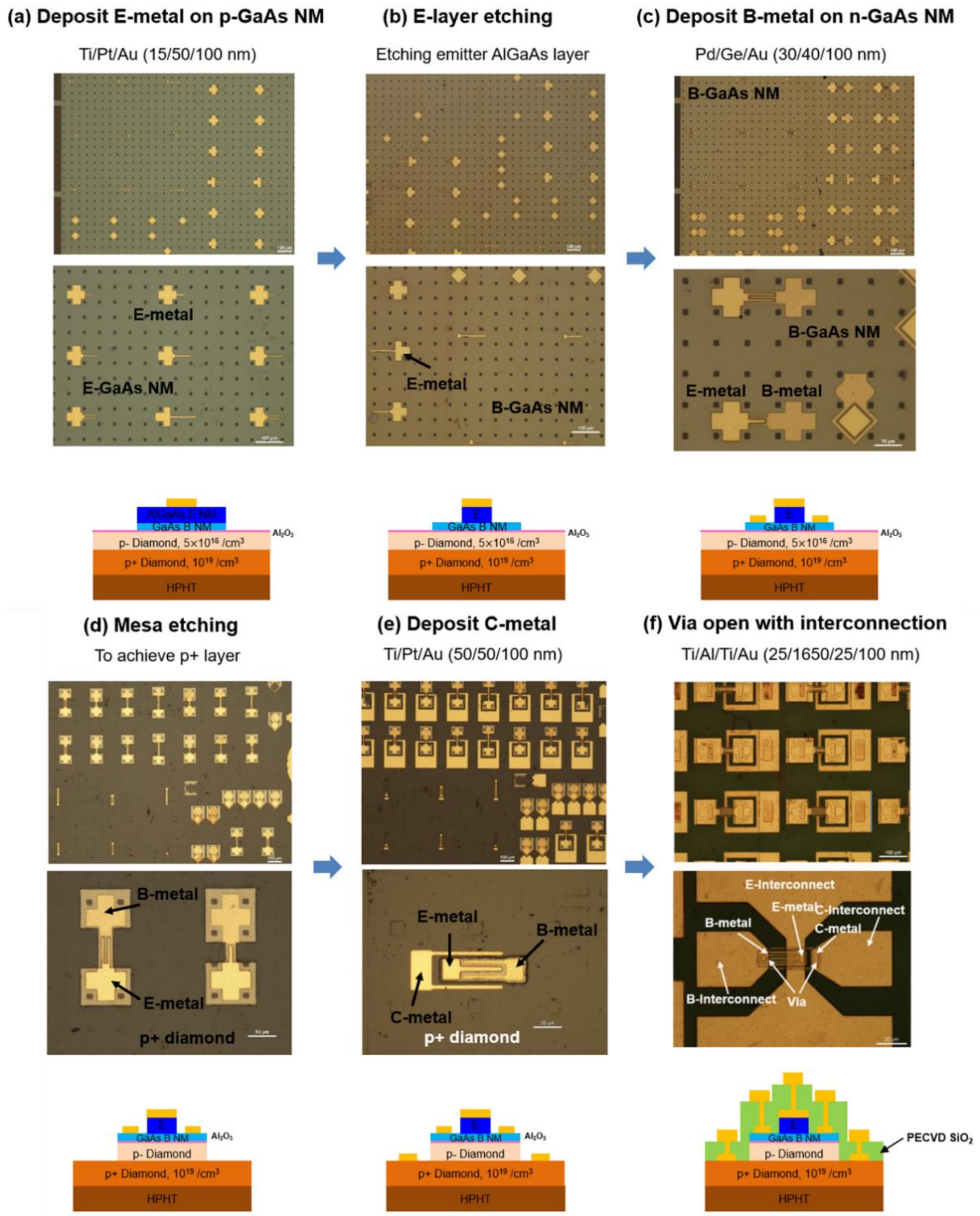


Figure 4.6 *The microscope images and schematic diagram of III-V/Diamond HBTs fabrication process, (a) deposit emitter metal on pGaAs NM, (b) emitter layer etching to achieve base region, (c) deposit base metal on nGaAs NM, (d) mesa etching to achieve p+diamond layer, (e) deposit collector metal on diamond, (f) PECVD oxide deposition, via open, and interconnection metal deposition. The schematic diagrams are not a real scale.*

e. Characterizations

The morphology of interfacial surfaces which are bottom of GaAs EB NMs and ALD Al_2O_3 on diamond were characterized by a Bruker Multimode 8 atomic force microscopy (AFM). Due to critical step of diamond CMP process, roughness of diamond surface was checked every time. To verify the surface treatment, electron affinity was calculated by ultraviolet photoelectron spectroscopy (UPS) and matching with the droplet angle from Contact angle measurement (Dataphysics OCA 15 optical contact angle). Current–voltage (*I*–*V*) and gain characteristics were measured by a Keithley 4200-SCS semiconductor parameter analyzer. Scanning Transmission Electron Microscopy (STEM) was measured to verify interlayer conformation.

4.4 Results and discussion

a. AFM measurement of both interfacial surfaces

In order to be compatible with the semiconductor grafting technique, we would prefer to have surface roughness levels that are < 2nm, preferably 1 nm or less. This presents a notoriously difficult problem in diamond. Many decades have been spent attempting to polish, smooth, and remove the resulting damage from diamond. State of the art processes still routinely finish with ~ 2nm of roughness, and worse, extreme features outside the root-mean-square roughness (R_{rms}) statistics and striations. Also, some pits and peaks exist on the substrate depending on previous process – RIE cleaning, CVD growth, and CMP. To obtain very smooth diamond, it has recently been shown that it is important to have the proper orientation <100> and to polish in the proper direction [110] [100]. This result in slow removal rates and very smooth diamond. Try to avoid device performance degradation due to surface roughness, we always check the diamond surface root-mean-square roughness (R_{rms}) after surface treatment by Bruker Multimode 8 atomic force microscopy (AFM). Figure 4.7 shows AFM topographic images ($10\times10\ \mu m^2$) of interfaces of both semiconductors. The surface treated diamond surface has a low R_{rms} value which is 0.6 nm which is shown in Fig. 4.7 (a). The bottom side of III-V epi (base side) is shown in Fig. 4.7 (b). This surface topographic image was obtained after picking up the membrane using PDMS and measured the surface roughness of cleaned III-V NM epi on the PDMS. The root-mean-square roughness (R_{rms}) of the III-V NM which is the undercut surface is 1.5 nm. The R_{rms} value of both interfacial areas are acceptable to perform semiconductor grafting process with successful approach to form heterostructure.

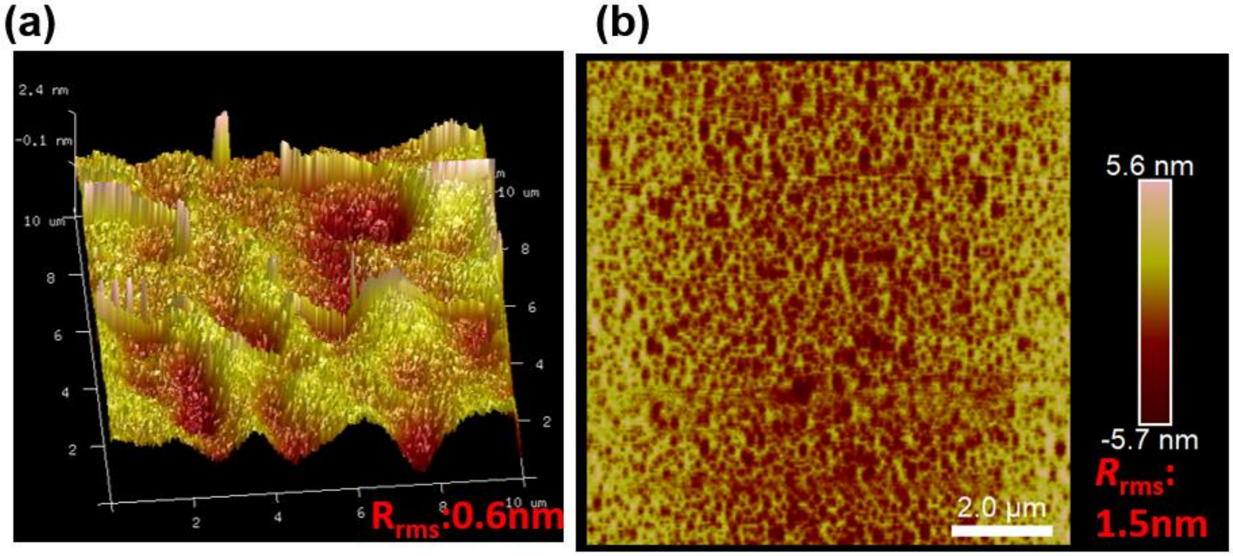


Figure 4.7 *AFM topographic images (10×10 μm*^{2}*) of interfaces of both semiconductors, (a) bottom side of III-V epi, and (b) surface treated diamond. Root-mean-square roughness (*R_{rms}*) of the interfaces of both semiconductors are presented below the AFM images.*

b. TEM study of interface monolayer

Scanning Transmission Electron Microscopy (STEM) was measured to verify interlayer conformation. Fig. 4.8 (a) shows STEM image of interface region of the GaAs/Diamond heterostructure with Al_2O_3 ultrathin layer. The scale bar of the TEM image is 2nm. Due to difference atom size of GaAs and Diamond, focused images of GaAs and Diamond are separately represented in Fig. 4.8 (b) and Fig. 4.8 (c), respectively. The Al_2O_3 ultrathin layer in the heterostructure is shown by the non-crystallized region. As shown in the Fig, 4.8 (b), there is no crystal defects cracks between the interface area. This is another proof of the interface Al_2O_3 as a thermal buffer layer during thermal anneal and cooling process. Like Si/GaN interface in chapter. 3, the Al_2O_3 ultrathin layer also served as a diffusion barrier layer during the thermal process of heterostructure formation.

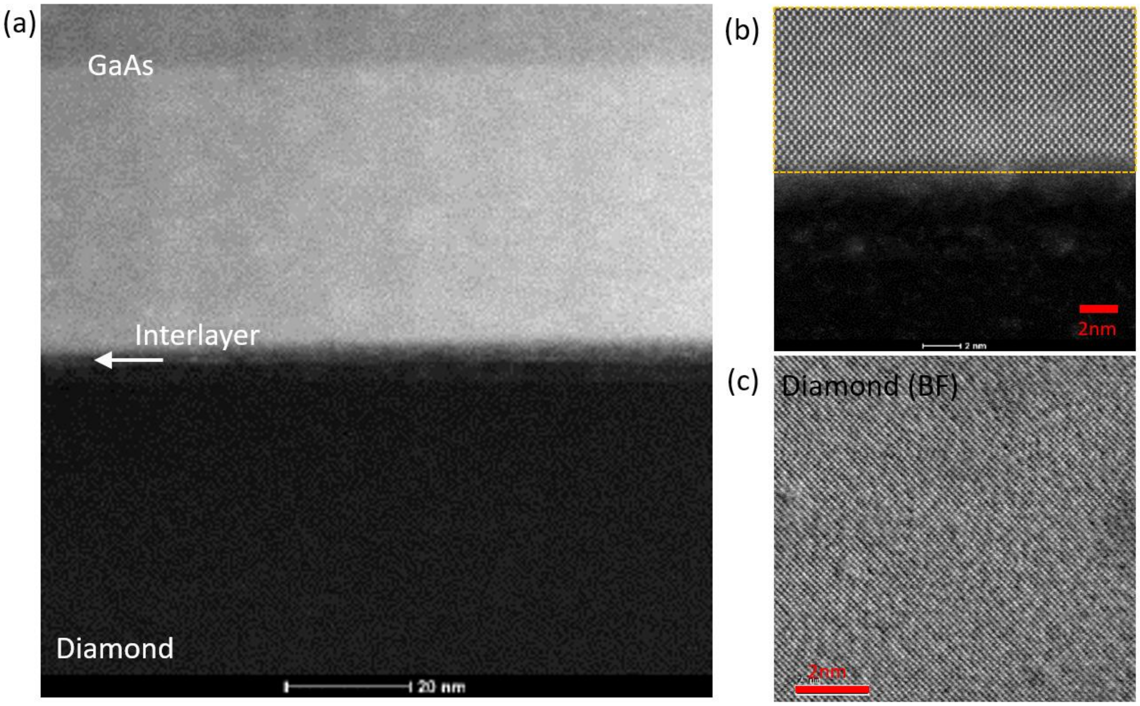


Figure 4.8 *Cross-sectional Scanning transmission electron microscopy (STEM) micrograph GaAs/diamond heterostructure with* Al_2O_3 *ultrathin layer. (a) GaAs/diamond interface, (b) focus on GaAs with 2 nm scale bar, (c) focus on diamond with 2 nm scale bar.*

c. CTLM study of electrodes

Before starting the fabrication, in order to get the best performance of HBTs, we should check and determine contact resistance which was processed using a low temperature ohmic annealing step within a thermal budget. Every layer (emitter, base, and collector) was required different combination and thickness metal. The most challenge is to develop p+ diamond contact process within the thermal budget of the GaAs E/B structure. The Circular Transmission Line Method (CTLM) structures for the emitter and base side of GaAs E/B and collector side of diamond were formed. It should be confirmed that the exact same metal combination and annealing conditions for each cell were used in this test. The CLTM test was measured using a Keithley 4200 Semiconductor Parameter Analyzer. For emitter p+GaAs contact, Ti/Pt/Au metal combination was used and for base n+GaAs contact Pd/Ge/Au were used. For p+ diamond collector contact, Ti/Pt/Au metal were used. Figure 4.9 shows the measured *I-V* characteristics with different spacings CTLM patterns from the p+GaAs emitter metal contact (Ti/Pt/Au) in Fig. 4.9 (a), n+GaAs base metal contact (Pd/Ge/Au) in Fig. 4.9 (b), and p+diamond collector metal contact (Ti/Pt/Au) in Fig. 4.9 (c). Metal annealing process was conducted simultaneously at 350°C for 15sec in N_2 ambient. All the contact parameters are shown in table 4.5. All the contacts have relatively low contact resistance values of 1.94×10^{-5} Ωcm², 1.25×10^{-5} Ωcm², and 3.12×10^{-6} Ωcm² which were achieved from p+GaAs, n+GaAs and p+diamond contact, respectively. Also, the sheet resistances can be found in Table 4.5 which values are 268 Ω/□ and 64.07 Ω/□, and 55 Ω/□, respectively.

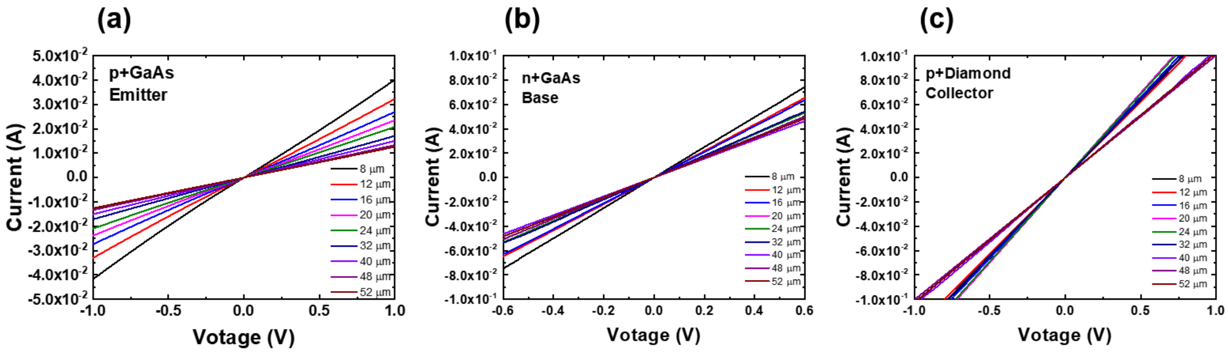


Figure 4.9 *Circular Transmission Line Measurements (TLM) study of each metal contact (a) p+GaAs emitter, (b) n+GaAs base, and (c) p+diamond collector I-V measurement, respectively.*

Table 4.5 *The sheet resistance (R_s (Ω/□)) and specific contact resistance (ρ_c (Ω-cm^2)) of each metal contact.*

Material	$R_S(\Omega/\square)$	$\rho_C(\Omega \cdot \mathrm{cm}^2)$
p+AlGaAs	268	1.94×10^{-5}
n+GaAs	64.07	1.25×10^{-5}
P+diamond	55	3.12×10^{-6}

d. Preliminary experiment – GaAs-Diamond diode *I-V* characterizations

Before the start the fabrication of the HBT using GaAs-diamond heterostructure, we've fabricated GaAs-Diamond diode at the initial stage. The results were encouraging for high breakdown collector operation. For this test, nGaAs NM was grafted on the p-diamond. Figure 4.10 shows the electrical characteristic of GaAs-Diamond heterostructure grafted diode. The current density versus voltage was shown in Fig. 4.10 (a). The breakdown voltage was measured current density-voltage under reverse bias driven up to 1100 V which was shown in Fig. 4.10 (b). The blue line is experimental result and green line is simulation result by Silvaco. In this simulation, the Fowler-Nordheim (FN) tunneling model was used []. Below breakdown voltage, both results were well matched. Unconsidered parameters during the simulation lead to breakdown voltage difference between the two curves. As shown in Figure 4.10, the ideality factor of this combination diode is 1.27 and breakdown voltage is around 1000V. This result confirmed that collector-base junction can be formed by Diamond-GaAs combination. More than words, this result was based on not heavily doped GaAs material. After getting optimized simulation result, this structure has more room to improve the performance.

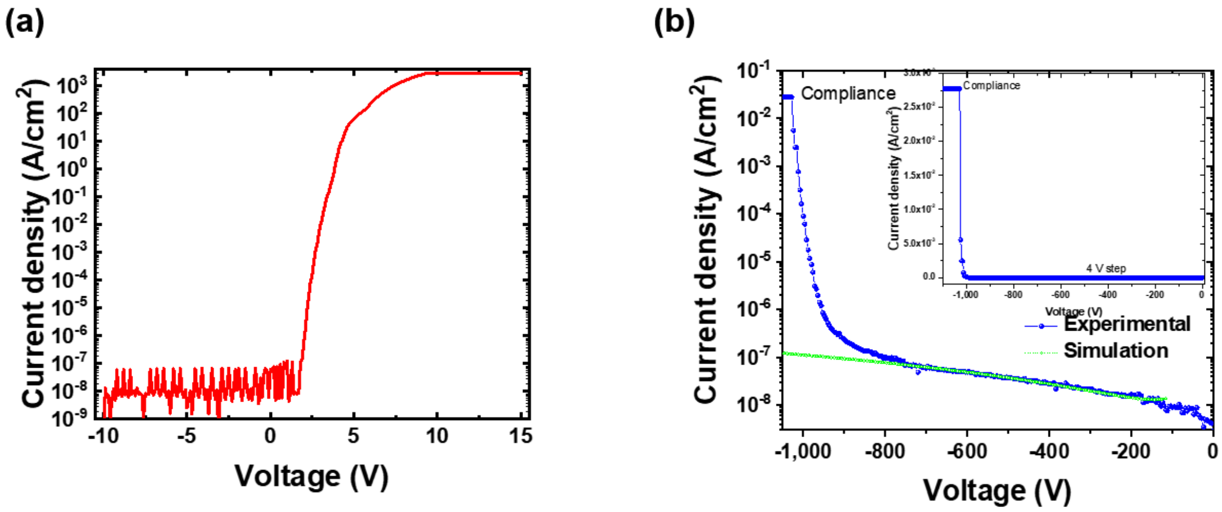


Figure 4.10 *Electrical characteristic of GaAs-Diamond heterostructure grafted diode, (a) Current density-voltage measurement, (b) measured current density-voltage under reverse bias driven up to 1100 V with the breakdown voltage of -1kV, inset: linear curve, blue line is experimental result and green line is simulation result by Silvaco.*

e. Electron affinity tuning with band diagram modification

Without diamond surface treatment, diamond originally has a negative electron affinity. Due to negative electron affinity, holes are accumulated in the collector at the base interface and cause depletion and breakdown in the GaAs. Figure 4.12 (a) shows hole accumulation at the interface of collector. This problem defeats the purpose of the diamond collector. Therefore, the degree of hydrogen and oxygen termination will need to be controlled to retain proper band alignment. As mentioned in the previous chapter, according to Silvaco simulation, we obtained specific electron affinity value (~ 0.1 eV) to form desired band alignment to balance hole transport and electron emission. Figure 4.12 (b) shows the modified band diagram which was applied desired electron affinity. As shown in this figure, there is smooth shape of band diagram at the base and collector interface. Then, SUNY which is one of our project teams has conducted electron affinity tuning using a H_2O treatment in ALD system at 300°C. Figure 4.12 explains how to verify the desired electron affinity. As shown in Fig. 4.12 (a), contact angle value was corresponding with the number of H_2O pulses in ALD system. To be conclude, contact angle is increased +0.7° with each 10 H_2O pulses. Inlet figure shows the contact angle degree change with 50 H_2O pulses in ALD system. Figure 4.12 (b) shows that the reference sample which has 0.08 eV electron affinity obtained from UPS measurement. It was directly matched 71° of contact angle measurement. This value came from 280 H_2O pulses treatment using ALD at 300°C. To sum up, electron affinity of diamond can be precisely tuned using a H_2O treatment in ALD system. Control of the diamond surface condition is a critical issue to success to get the high-performance devices using diamond.

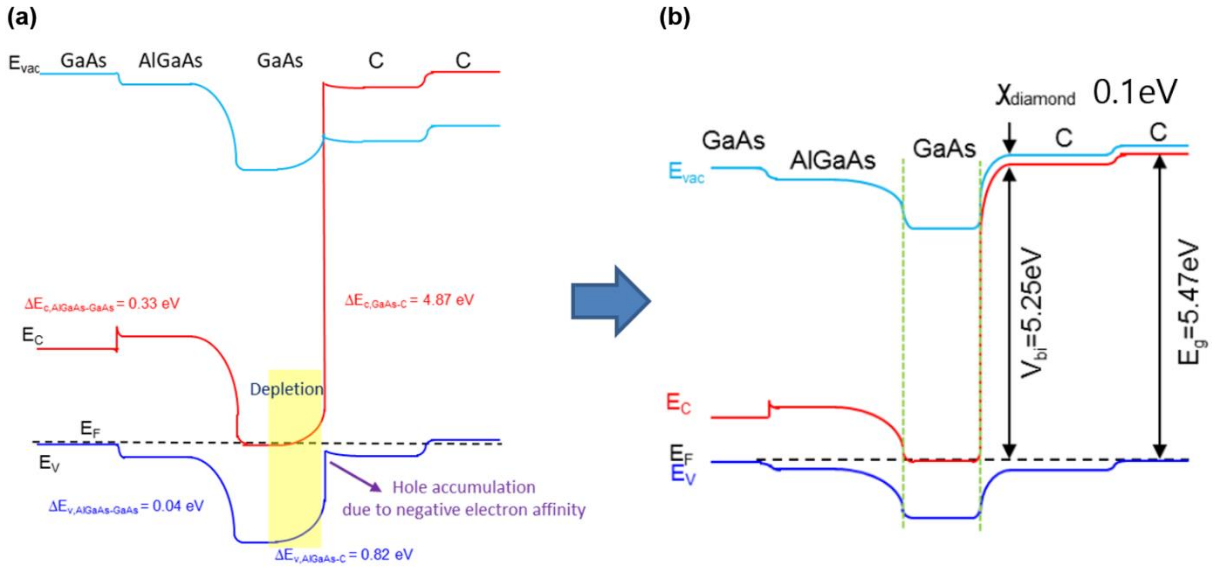


Figure 4.11 *The bandgap diagram of III-V/Diamond heterostructure. (a) the bandgap diagram from non-surface treatment diamond, due to negative electron affinity of diamond, holes are*

accumulated at the interface, (b) band alignment modification using diamond surface treatment, desired band alignment to balance hole transport and electron emission.

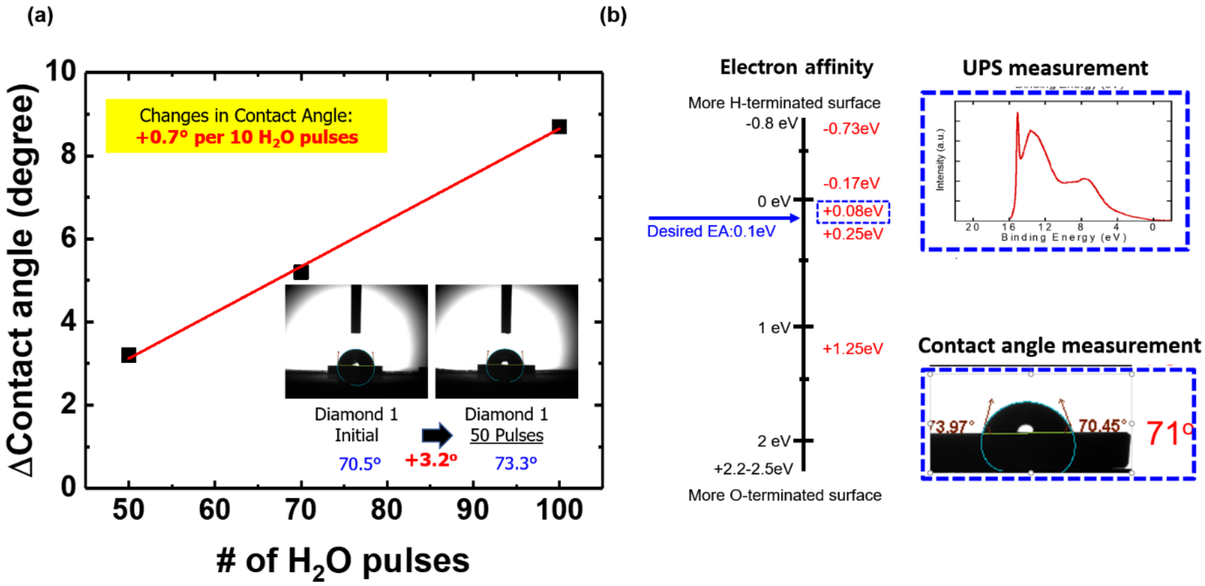


Figure 4.12 *(a) Contact angle measurement trend depending on the number of H_2O pulses, inset image is contact angle change after 50 of H_2O pulses, (b) desired electron affinity value which is 0.1eV and the correlation data of UPS measurement and contact angle measurement which can be matched directly.*

f. Tunnel junction characteristic with Al_2O_3 dielectric interlayer

Before moving to HBT fabrications, tunneling characteristic of Al_2O_3 ultra-thin interlayer was investigated. Direct comparison of the tunnel junction characteristic with and without Al_2O_3 layer, benefit of semiconductor grafting method was confirmed. Two diamonds have grown at the same chamber and their average sheet resistance are identical which is about 1000 Ω/□. Figure 4.13 (a) shows the schematic diagram of the GaAs/Diamond heterostructure with Al_2O_3 ultrathin interlayer to measure *I-V* characteristic. The structure of two samples is the identical which is n+GaAs grafted on p+ diamond, unless Al_2O_3 ultrathin interlayer is present or not. Figure 4.13 (b) shows the current level comparison of both diamond substrates which are with and without Al_2O_3 ultrathin inter layer to prove identity of both samples. As shown in Fig. 4.13 (b) the current level of both diamond samples is the same within measurement error range. Figure 4.14 shows *I-V* measurement of the GaAs/Diamond contact with and without Al_2O_3 ultrathin interlayer. The blue and red line represent the sample with and without Al_2O_3 ultrathin inter layer, respectively. As shown in Fig 4.14 (a), the sample with Al_2O_3 has better ohmic characteristic. Moreover, Fig 4.14 (b) indicate statistical current density data of each voltage point with two different samples. The variation among the devices in with Al_2O_3 sample is lower than that in without Al_2O_3 sample. Al_2O_3 layer works as chemical and field effect passivation layer. So, they can reduce recombination at the surface, and it leads to increase current. Also due to fixed negative charge density of Al2O3 layer, hole tunneling is increased. Last, decreasing tunneling barrier thickness leads to increase tunneling possibility.

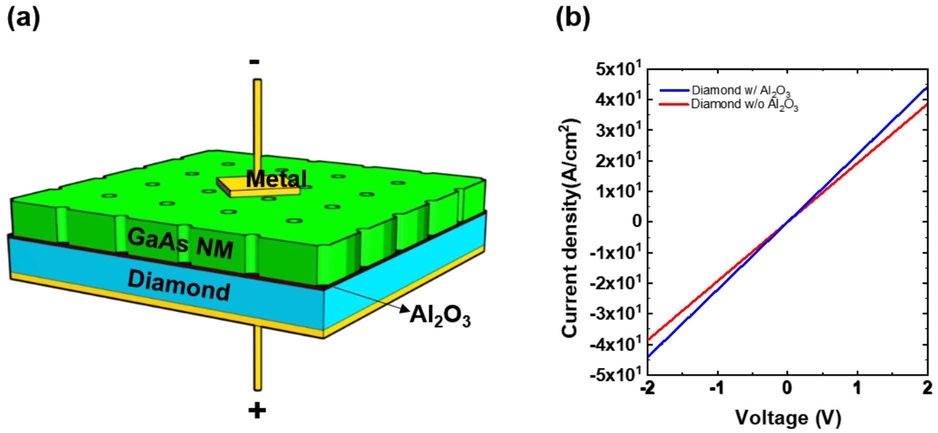


Figure 4.13 *(a) Schematic diagram of the GaAs/Diamond heterostructure with Al_2O_3 ultrathin interlayer, (b) the current level comparison of both diamond substrates (w/ and w/o Al_2O_3 layer) to prove identity of both samples.*

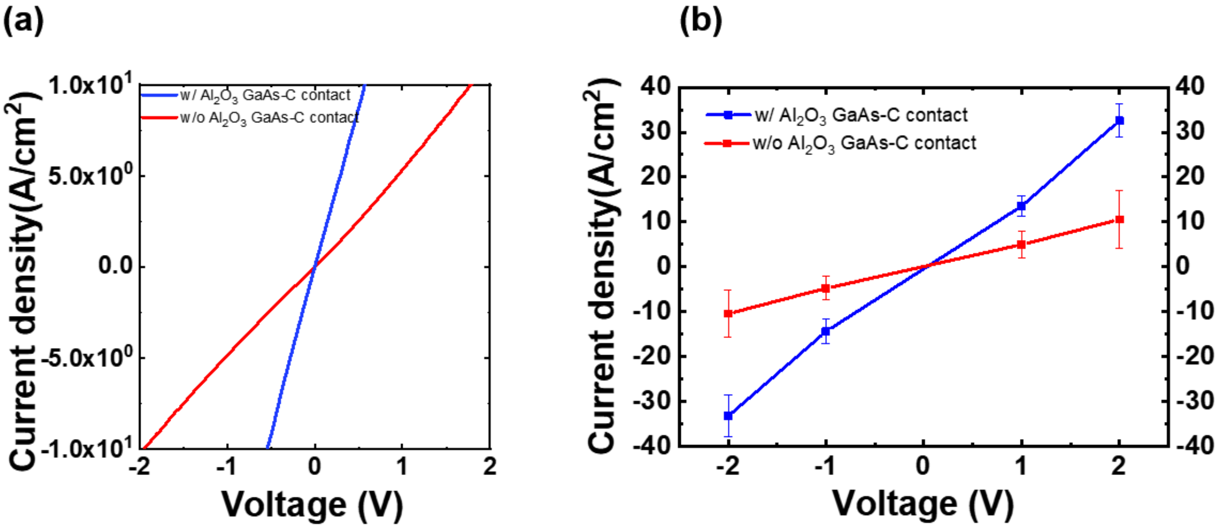


Figure 4.14 *I-V measurement of the GaAs/Diamond contact with and without Al_2O_3 ultrathin interlayer, (a) current density versus voltage plot (b) Statistical data of each voltage points.*

g. Electrical characteristics of emitter-base, and collector-base junction

The direct current (DC) characteristics of the devices were characterized using a Keithley 4200 Parameter Analyzer. Before measuring the three-port device characterization, diode characteristics of emitter-base and collector-base junction were measured. Figure 4.15 shows the measured *I–V* characteristics of the p–n AlGaAs/GaAs E-B and the p–n Csp3-GaAs C-B junctions of the HBT. The integrity of the emitter-base (E-B) and collector-base (C-B) junctions in terms of electrical performances is verified by the excellent rectifying current-voltage (*I–V*) curves measured from an HBT with an emitter area of 40 × 40 μm^2. The *I-V* curve of each junction shows an ideality factor of 1.26 for the emitter-base and 1.85 for base-collection heterostructure in Fig. 4.15 (a) and (b), respectively. The current on-off ratio (I_{on}/I_{off}) under ±1.5 V for the E-B junction is 2.61×10^5, and that for C-B junction under ±3 V is 1.27×10^9. The low ideality factor (n) and the high I_{on}/I_{off} value of the E-B junction is the result of the epitaxially grown interface of the heterojunction with rather mature growth conditions for this class of materials. The high I_{on}/I_{off} value of the C-B junction is the quantitative evidence of the epitaxy-like grafted heterojunction with very low interface states [101]. Each junctions' diode has low-level reverse-bias current and high level forward current. It also has a long ideal region and reasonable series resistance region. For this experiment, the critical part for both junction diode is that finding the best condition for diamond collector metal annealing process within a thermal budget of III-V material, which is emitter and base layer. As shown in Fig. 4.15, a rapid thermal annealing process was conducted at 350°C for 15 sec in N_2 ambient. The etching process to achieve the n-type GaAs base layer and p-type diamond collector layer were also optimized to compare the SIMs result and experimental result. Thanks to the pure interface at the C-B junction and their high ratio of doping concentrations, the depletion region is expected to widen substantially into the p− diamond collector layer. For the C-B diode, hole current is the dominant current under forward bias due to the high electron energy barrier; following the simulation result from our work, a conduction band discontinuity (ΔEC) is 3.75 eV [102]. Because of the low hole current density, the effects of series resistance always appear at very low forward bias values, inducing generally higher n values for the GaAs-diamond n–p diodes than emitter-base p–n diodes. Thus, the quality of the GaAs-diamond interface is not clearly reflected by the ideality factor values but proof of the very low reverse-bias current density and the very high I_{on}/I_{off}. Regarding the low density of states of the C-B heterojunction interface, the generation current from the interface is negligible. Alternately, most of the measured current under the reverse bias of the B-C diode comes from the generation current in the depleted p− diamond region. Due to the ultrawide bandgap characteristic of the diamond, under the condition of having a positive electron affinity, the generation current of depletion diamond should be very low, which is shown in Figure 4.15(a). However, regarding the three-port device measurement, the current gain ($\beta = I_C/I_B$) of the HBT is only about unity. The low current gain results from several factors, among which the most critical one is the energy barrier existing at the B-C junction [102]. Another investigated issue is the exact nature of the GaAs-diamond interface. During the membrane separation process, the sacrificial layer is $Al_{0.95}Ga_{0.05}As$, and the entire Al containing layer near the GaAs was not fully removed by the etch process. It is investigated by thickness measurement and SIMS profile. One possible reason is due to the GaAs and $Al_{0.95}Ga_{0.05}As$ not being atomically abrupt from heteroepitaxy. Any thin residual Al containing layer on the GaAs nanomembrane is affected the band alignment and device operation like current flow.

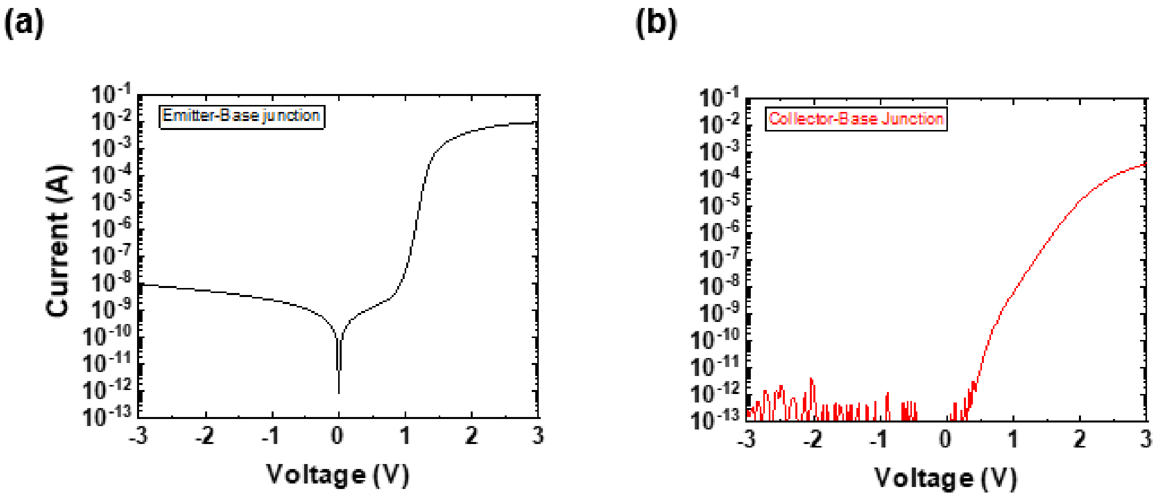


Figure 4.15 *I-V measurement of the diode characteristics of each junction, (a) emitter-base junction (b) collector-base junction.*

4.5 Conclusions

In summary, power electronics applications will require a more compact design with improved heat handling and dissipating capabilities in the near future. To meet these demands, a new generation of semiconductor materials is necessary. Following this trend, the large bandgap materials promise high-performance electronics in terms of power, frequency, and temperature. With its superior properties—high bandgap (5.47 eV), high critical electric field (7.7 - 20 MV/cm), high thermal conductivity (~ 22 W/cm·K at RT), and high hole mobility (> 2000 cm^2/ V·s), diamond has tremendous advantages beyond the silicon.

In this chapter, I have demonstrated the viability of semiconductor grafting in forming AlGaAs/GaAs/diamond heterojunctions to overcome the limitations of n-type doping to implement diamond for bipolar device applications. The preliminary HBT experimental study-numerical simulation work, material properties, GaAs-diamond *IV* result, emitter-base, and collector-base junction formation and its diode characterization indicate a clear direction for further investigation toward the realization of high-performance diamond-collector HBTs and other types of bipolar junction devices in the future. Specifically, maintaining low interface density of states of the GaAs-diamond interface is critical while tuning the electron affinity of a diamond. Although a high-performance GaAs/diamond n–p junction has been already achieved through this study, diamond surface treatment via ALD to find a specific electron affinity plays a significant role for interface charge at the interface, and it needs to be studied further. Moreover, realizing a desired n+ GaAs base layer thickness in the E-B membrane layer by completely removing the Al-containing sacrificial layer is also important for yielding a working HBT. Further gain improvement is expected as the electron affinity tuning of the diamond and structure study.

Again, the formation of a p–n–p HBT using a double heterostructure AlGaAs/GaAs/diamond layered structure showed promise of functional high current gain HBT for future demand.

4.6 Reference

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CHAPTER 5

Conclusions and Future Directions

In this thesis, the semiconductor heterostructure without considering lattice mismatch has been investigated via III-V/silicon tandem solar cell, Si/GaN diode, and AlGaAs/GaAs/diamond HBTs. Using the semiconductor grafting technique with an ultrathin oxide layer at the interface, it becomes possible to form a heterostructure between two arbitrary types of semiconductors without considering a lattice match, creating many opportunities in the area of material engineering. Furthermore, the technique enables much broader applications– photonic devices, optical devices, and power devices. Al_2O_3 ultrathin oxide layer deposited by atomic layer deposition (ALD) functions as both a passivation layer that reduces the surface defect states and a tunneling layer that allows carriers to transport between abrupt semiconductors.

In chapter 2, the III-V tandem solar cell was fabricated by grafting technique with an III-V wafer recycle process. It has a high voltage output and high conversion efficiency that makes it overcome the silicon solar cell efficiency limit. The improved tunneling junction structures by the Al_2O_3 ultrathin layer deposited by ALD have been investigated at both cells' interface. Moreover, using the grafting technique, it becomes easier to transfer nanomembranes on any cells and substrates. In addition, this III-V/Si tandem solar cell can be used in the space. According to NASA, the objects' mass and volume are all parameters to be considered while launching to space. The key idea of the solar cell for space application is whether it is possible to make smaller, lighter than conventional solar cells while still maintaining high performance. Our III-V solar cells, beyond the silicon, can be grafted on other thin, flexible, stretchable, and rollable substrates.

In chapter 3, the diamond-wurtzite heterostructure diodes consisted of p-type Si NM on n-type GaN were fabricated by the semiconductor grafting technique with the ultrathin Al_2O_3 tunneling layer. The semiconductor grafting technique gives plenty of freedom to form heterostructures with superior performance while avoiding the issue of lattice mismatch. Thus, the technique allows us to create many combinations of semiconductors with the broader band offset. To verify if the two arbitrary semiconductors were bonded well, the electrical properties have been studied. The heterostructure diodes in this work remarkably outperform diodes in referred literature regarding essential diode factors such as ideality factor and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio–1.14 and 1.18×10^{7} at ±1 V, respectively. In order to commercialize, a large-scale fabrication method should be developed. Several ways were reported and introduced by many research groups and companies—transfer printing machine, roll to roll printing, inkjet printing, remote epitaxy using 2D material, Etc.

In chapter 4, beyond the two-port passive devices, AlGaAs/GaAs/Diamond HBTs were investigated. To meet the demand of next-generation high power switching devices and RF devices, the diamond is considered the most desirable candidate material due to its own unique property of ultrawide bandgap (UWGB) material and electrical properties. Due to poor n-type characteristics of the diamond, the majority of applications are unipolar devices such as Schottky diode and FETs. This thesis, III-V emitter, and base layers were used by the semiconductor grafting technique to overcome the poor n-type doping characteristics. The excellent rectifying I-V curves verify the integration of emitter-base and collector-base junctions in electrical performances.

Despite the high energy barrier, the excellent collector-base junction indicates the prospect of an operational HBTs with an optimized barrier height of collector-base junction energy, which is made possible by tuning the electron affinity of the diamond. Several ways to get a current gain (β) are proposed for future work.

First, using a thinner base is one of the options. Smaller GaAs diffusivity makes the base hard to collect the carrier. Decreasing the base thickness increases chance to collect the carriers, avoiding the Kirk effect. Also, modifying the releasing GaAs layer structure—reversed structure with the base on top and bottom emitter and doing a double flip grafting process can remove uncertain layers below the cutting point during the undercut process. Following this method, a thin base layer is guaranteed at the stage of growth epi. Second, find a way to decrease the series resistance in collector reason. At this moment, emitter, base, and collector metal are annealed at the same time. According to review literature, the annealing temperature of the diamond metal is higher than the GaAs metal temperature. Changing the process sequence can solve this problem.

At last, it is using a heavy doped base and collector to form the thinner depletion region. Also, it leads to avoiding of band-to-band tunneling between collector-base junction. Changing the base into a material with a larger bandgap is one of the possible ways to get a high gain.

In the near future, after obtaining large arbitrary heterogeneous structures with reliability, it does satisfy the needs for future applications – high speed, high power to the autonomous vehicle system, and other cutting edge technologies.

Appendix

A1-1. Materials

- Isopropyl alcohol (IPA) (KMG, cat. no. 200440) ! CAUTION IPA is flammable.
- Acetone (KMG, cat. no. 200406) ! CAUTION Acetone is flammable.
- Wiper (Fisher Scientific, ITW Texwipe, cat. no.18330A)
- Hydrofluoric acid (HF) 49 % (J.T.Baker, CAS. no. 7664-39-3) ! CAUTION HF is extremely corrosive.
- 1:6, 1:20 Buffered oxide etchant (BOE) (J.T.Baker) ! CAUTION BOE is extremely corrosive.
- Hydrochloric acid (HCl) 36.5-38.0% (J.T.Baker, CAS. no. 7647-01-0)
- Sulfuric acid (H_2SO_4) 98% (J.T.Baker, CAS. no. 7664-93-9)
- Phosphoric acid (H_3PO_4) 98% (J.T.Baker, CAS. no. 7664-38-2)
- Ammonium Hydroxide (NH_4OH) 28.0-30.0% (J.T.Baker, CAS. no. 1336-21-6)
- Hydrogen peroxide (H_2O_2) 30% (J.T.Baker, CAS. no. 7722-84-1)
- AZ 4620 photoresist (AZ Electronic materials)
- AZ 5214 photoresist (AZ Electronic materials)
- S 1813 photoresist (Shipley)
- Lor3A lift-off resists (Micro Chem)
- MIF-321 developer (Shipley)
- AZ 917MIF developer (AZ Electronic materials)
- MICROPOSIT™ REMOVER 1165 a.k.a N-Methyl-2-pyrrolidone (NMP) (Shipley) !CAUTION Carbon tip tweezer get damaged.
- Gold, Palladium, Titanium, germanium, Platinum, Nickel (Kurt J. Lesker Company)
- TiO_2, SiO_2 (Kurt J. Lesker Company)
- Trimethylaluminium ($Al(CH_3)_3$, TMA) precursor (Sigma-Aldrich Co. CAS Number 75-24-1)

A1-2. EQUIPMENT

- Mask aligner (KARL SUSS MJB3)
- Reactive ion etcher (RIE, Unaxis 790, SEMCO RIE 10NR, ICP general etcher 790 series)
- Plasma enhanced chemical vapor deposition (PECVD, Plasma Therm PT70)
- ICP etcher (Plasma Therm SLR series inductively coupled plasma (ICP))
- Atomic Layer Deposition (Ultratech/Cambridge Nanotech Savannah S200 ALD system)
- Electron-beam metal evaporator (Angstrom Engineering, Nexdep Physical Vapor Deposition Platform, CHA Industries, CHA-600)
- Electron-beam dielectric evaporator (Angstrom Engineering, Nexdep Physical Vapor Deposition Platform, Telemark)
- Ultrasonic cleaning bath (Bransonic, cat. no. CPX5800H)
- Dicing Saw (Microautomation 1006 Wafer Saws)
- Rapid Thermal Annealer (RTA, Heatpulse 610)

A1-3. MEASUREMENT EQUIPMENT

- Profilometer (TENCOR ALPHASTEP 200)
- 3D surface profiler (Zygo profiler)
- Microscope (Nikon)
- Optical Reflectometer (FILMETRICS F-20)
- Atomic force microscope (Bruker Catalyst BioAFM)
- Raman spectroscopy (Horiba Jobin Yvon Labram Aramis Raman)
- X-ray diffraction (XRD, PANalytical Empyrean, Bruker D8 Discovery)
- Secondary Electron Microscope (SEM, Zeiss LEO 1530)
- Contact angle measurement (Dataphysics OCA 15 optical contact angle)
- I-V measurement (Keithley 4200-SCS semiconductor parameter analyzer, HP4155)
- C-V measurement (Agilent precision E4980 LCR meter)
- Scanning Transmission microscope (STEM, outsourcing, Purdue Univ. Prof. Wang’s group)

B1. Fabrication protocols

B1-1 Fabrication of III-V/Si tandem solar cells

1. Cleaning process
    a. III-V substrate using ultrasonic 3V in acetone (100 ml), IPA (100 ml), and DI water (100 ml) for 5 minutes and dry with nitrogen (N_2) gun thoroughly.
    b. Silicon bottom cell – SiON removal: HF dropping using pipet 10s and cleaning using ultrasonic 7V in acetone (100 ml), IPA (100 ml), and DI water (100 ml) for 5 minutes and dry with nitrogen (N_2) gun thoroughly.

    ▲ CRITICAL STEP Check the correct substrates for the purpose, HF is extremely corrosive, rear side aluminum paste get damaged by HF, try to avoid it
2. Nanomembrane preparation
    a. Patterning
        i. Spin coating – AZ1827, 4000rpm 30sec

        ▲ CRITICAL STEP Using 3" chuck, the sample is attached on the edge
        ii. Baking – 105°C 3min
        iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 60sec
        iv. Develop – MIF-321 90sec

        ▲ CRITICAL STEP Check all the sample using microscope
    b. O2 cleaning: Unaxis 790**:** 100w power, 20mT, O_2 20SCCM, 10sec
    c. GaAs etching: ICP etcher: RF1 (RIE): 60W, RF2 (ICP): 500W, BCl_3 10SCCM, Ar 5SCCM, 15mT (30step)

    ▲ CRITICAL STEP Always check the etch rate
    d. PR removal: 1165: dipping, change 1165 solutions, ultrasonic below 3V for 30sec, Rinse in the DI water thoroughly

    ▲ CRITICAL STEP Carbon tip tweezer get damaged.
3. Undercut process
    a. Soak into diluted HF solution 1:160~180: 2hr~2hr 30min

    ▲ CRITICAL STEP 200ml final, cover the lead, N2 circumstance using plastic bag with N2 gun, applied vibration, heat the DI water to remove oxide bubble in the water (135°C hotplate 20~30min)
    b. After fully undercut, put it in water (gently), and store in IPA solution

    ▲ CRITICAL STEP III-V NMs are really brittle, do not rinse directly
4. ALD deposition: Right before Al2O3 deposition using ALD, remove native oxide of the Si bottom cell using BOE 1:6 pipet 10s, DI water rinsing thoroughly, 4 cycles of 0.015 sec trimethylaluminium ($Al(CH_3)_3$, TMA) precursor pulse, 5 sec N2 purging, 0.015 sec H2O precursor pulse with 200°C substrate temperature

▲ CRITICAL STEP While transferring to ALD, using zipper bag with N_2 gun
5. Pick up & grafting
    a. Super clean silicon surface with Al_2O_3 ultrathin layer
    b. PDMS stamp (2.5×2.5×1.5 cm, 1:4 curing agent: PDMS)

c. MF321 cleaning for III-V NMs using pipets
d. 250°C bonding annealing for 5min in N_2 ambient by RTA

▲ CRITICAL STEP Thick NMs needs force to attach the host substrate, pushing by the second finger, always check the microscope

6. Metal patterning
    a. O2 plasma treatment: 30w power, 50mT, O_2 50SCCM, 15sec
    b. Patterning
        i. Spin coating – AZ5214, 2500rpm 30sec

        ▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge

        ii. Baking – 95°C 3min
        iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 2.5sec
        iv. Baking – 115°C 90sec
        v. Post exposure – 25sec with the same light source
        vi. Develop – AZ 917 MIF 28sec
    c. O2 cleaning: Unaxis 790**:** 100w power, 20mT, O_2 20SCCM, 10sec
    d. HCl dipping to remove native oxide 1:10 15s -> rinse thoroughly

    ▲ CRITICAL STEP rinse thoroughly, HCl needs more time to rinse

7. Metal deposition (1st): Pd/Ge/Au 30/40/100 nm
8. RTA process: 450°C for 1min at N_2 ambient
9. (selective) Metal deposition (2nd): Ti/Cu/Au 10/1500/200 nm
10. Lift off: dip into 1165 30min

    ▲ CRITICAL STEP Carbon tip tweezer get damaged, using pipet to blow in DI water

11. III-V layer etching (metal contact layer removal): ICP etcher: RF1 (RIE): 60W, RF2 (ICP): 500W, BCl_3 10SCCM, Ar 5SCCM, 15mT

    ▲ CRITICAL STEP Check the etching rate, etching is critical, finding an exact time to etch every time depending on the target thickness, after ICP etching using PR Asher or RIE do Plasma Descum process (previous recipe was eliminated in WCAM)

12. Final wet etching: H_3PO_4:H_2O_2:H_2O = 3:1:25 (18:6:150ml) ~15 sec; 2.667/sec etch)

    ▲ CRITICAL STEP Check the correct solution depending on the materials (https://cleanroom.byu.edu/wet_etch)

13. Active region defines
    a. Patterning
        i. Spin coating – AZ1827, 4000rpm 30sec

        ▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge

        ii. Baking – 105°C 3min
        iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 60sec
        iv. Develop – MIF-321 90sec

        ▲ CRITICAL STEP Check all the sample using microscope

14. Active region define etching: ICP etcher: RF1 (RIE): 60W, RF2 (ICP): 500W, BCl_3 10SCCM, Ar 5SCCM, 15mT

  a. If Silicon bottom cell front metal pad is needed, stop etching when you meet the silicon substrate, then patterning and metal deposition (Ti/Au 10/100 nm)
    i. Spin coating – AZ5214, 2500rpm 30sec

    ▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge

    ii. Baking – 95°C 3min
    iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 2.5sec
    iv. Baking – 115°C 90sec
    v. Post exposure – 25sec with the same light source
    vi. Develop – AZ917 MIF 28sec
  b. Unless, etch all the n+ silicon layer using 790 RIE: 100w power, 15mT, SF$_6$ 67SCCM, O$_2$ 5SCCM.

▲ CRITICAL STEP Check the etching rate, etching is critical, finding an exact time to etch every time depending on the target thickness, after ICP etching using PR Asher or RIE do Plasma Descum process (previous recipe was eliminated in WCAM), check PR thickness every time before starting etching process, if need, re-pattern the active region define patterning (step #13).

15. Anti-reflection coating
  a. Patterning
    i. Spin coating – Lor3A 4k rpm 30s

    ▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge, need ramping up

    ii. Baking – 200°C 5min
    iii. Spin coating – S1813 A 4k rpm 30s

    ▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge

    iv. Baking – 105°C 3min
    v. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 90sec
    vi. Develop – MIF-321 60S+a
  b. O2 cleaning: Unaxis 790**:** 100w power, 20mT, O$_2$ 20SCCM, 10sec
  c. HCl dipping to remove native oxide 1:10 15s -> rinse thoroughly
  d. Evaporate the AR layer (TiO2 (45nm, A3D0.7), SiO2 (80nm A2D1.5))

16. Lift off: dip into 1165 30min

▲ CRITICAL STEP Carbon tip tweezer get damaged, using pipet to blow in DI water

B1-2 Fabrication of Si/GaN Heterojunction diodes

1. Cleaning process (pSOI, nGaN substrate)
    - a. Using ultrasonic 3V in acetone (100 ml), IPA (100 ml), and DI water (100 ml) for 5 minutes and dry with nitrogen (N_2) gun thoroughly.
    - b. piranha solution(H_2SO_4:H_2O_2 3:1 120°) for 10 min
    - c. RCA1 (NH_4OH:H_2O_2:DI = 1:1:5) 10min
    - d. RCA2 (HCl:DI = 1:1) 10min
    - e. HF:DI (1:1) 10min

      ▲ CRITICAL STEP Check the correct substrates for the purpose, HF is extremely corrosive, SiC on GaN substrate is transparent, mark on the back side, piranha solution is self-heat up.
2. Nanomembrane preparation
    - a. Patterning
        - i. Spin coating – AZ1813, 4000rpm 30sec

          ▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge
        - ii. Baking – 105°C 3min
        - iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 30sec
        - iv. Develop – MIF-321 40sec

          ▲ CRITICAL STEP Check all the sample using microscope, check whether the screen oxide is on top or not. If you suspect it is on the top, please dip into HF solution several seconds.
    - b. O2 cleaning: Unaxis 790: 100w power, 20mT, O_2 20SCCM, 10sec
    - a. Si etching hole etching: 790 RIE: 100w power, 15mT, SF_6 67SCCM, O_2 5SCCM.

      ▲ CRITICAL STEP If screen oxide is on top, nothing can be etched
    - c. PR removal: acetone (100ml) dipping, IPA (100ml) cleaning.

      ▲ CRITICAL STEP Q-tip can be used. Undercut process
    - d. Soak into HF solution: pure (100ml) 50min

      ▲ CRITICAL STEP IPA can be mixed with the same ratio, check the chemical disposal, if not fully etched, put IPA (100ml) 10min, Acetone (100ml) 5min, then dip into HF again. Check the microscope every time.
    - e. After fully undercut, put it in water (gently), and store in IPA solution

      ▲ CRITICAL STEP can rinse directly using DI water gun
3. ALD deposition: Right before Al2O3 deposition using ALD, remove native oxide of the nGaN host substrate using BOE 1:6 pipet 10s, DI water rinsing thoroughly, 5 cycles of 0.015 sec trimethylaluminium ($Al(CH_3)_3$, TMA) precursor pulse, 5 sec N2 purging, 0.015 sec H2O precursor pulse with 200°C substrate temperature

   ▲ CRITICAL STEP While transferring to ALD, using zipper bag with N_2 gun
4. Pick up & grafting
    - a. Super clean nGaN substrate with Al_2O_3 ultrathin layer
    - b. PDMS stamp (2.5×2.5×1.5 cm, 1:4 curing agent: PDMS)

   ▲ CRITICAL STEP attach fast, detach moderate speed

   c. Cleaning for III-V NMs using DI water
   d. 350°C bonding annealing for 5min in N_2 ambient by RTA

5. Cathode mesa etching
   a. O2 plasma treatment: Unaxis 790: 30w power, 50mT, O_2 50SCCM, 15sec
   b. Patterning
      i. 1st Spin coating – AZ5214, 2500rpm 30sec

      ▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge

      ii. Baking – 95°C 3min
      iii. 2nd Spin coating – AZ5214, 2500rpm 30sec
      iv. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 4sec
      v. Baking – 115°C 90sec
      vi. Post exposure – 50sec with the same light source
      vii. Develop – AZ 917 MIF 28sec
      viii. Hard baking 115°C 15min
   c. Mesa etching:
      i. Si etching Unaxis 790: 100w power, 40mT, CF_4 45SCCM, O_2 5SCCM, 90+90+30sec for 180nm thick etching
      ii. N-GaN etching ICP etcher: RF1 (RIE): 100W, RF2 (ICP): 500W, BCl_3 10SCCM, Cl_2 16SCCMAr 5SCCM, 4mT, 40s loop recipe (~5min etch rate ~2.3nm/s achieved 415nm ± 15 nm)
   d. PR removal: acetone (100ml) dipping

   ▲ CRITICAL STEP Q-tip can be used, check the etching rate, etching is critical, finding an exact time to etch every time depending on the target thickness, after ICP etching using PR Asher or RIE do Plasma Descum process (previous recipe was eliminated in WCAM), check PR thickness every time before starting etching process, if need, re-pattern the mesa patterning (step #5-b).

6. Metal patterning (Cathode)
   a. Patterning
      i. Spin coating – AZ5214, 2500rpm 30sec

      ▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge

      ii. Baking – 95°C 3min
      iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 2.5sec
      iv. Baking – 115°C 90sec
      v. Post exposure – 25sec with the same light source
      vi. Develop – AZ 917 MIF 28sec
   b. O2 cleaning: Unaxis 790**:** 100w power, 20mT, O_2 20SCCM, 10sec
   c. BOE dipping to remove native oxide 1:6 15s -> rinse thoroughly

   ▲ CRITICAL STEP BOE is extremely corrosive

7. Metal deposition: Ti/Al/Ti/Au, 20/100/45/100nm
8. Lift off: dip into acetone IPA 10min respectively (@ slide glass)

   ▲ CRITICAL STEP pipet can be used to blow in the liquid solutions

9. RTA process: 400°C for 1min at N_2 ambient

   ▲ CRITICAL STEP Check the correct temperature, it varies many time

10. Metal patterning (Anode)
    a. Patterning
        i. Spin coating – AZ5214, 2500rpm 30sec

           ▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge

        ii. Baking – 95°C 3min
        iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 2.5sec
        iv. Baking – 115°C 90sec
        v. Post exposure – 25sec with the same light source
        vi. Develop – AZ 917 MIF 28sec
    b. O2 cleaning: Unaxis 790**:** 100w power, 20mT, O_2 20SCCM, 10sec
    c. BOE dipping to remove native oxide 1:6 15s -> rinse thoroughly

       ▲ CRITICAL STEP BOE is extremely corrosive

11. Metal deposition: Ni/Au, 10/100nm
12. Lift off: dip into acetone IPA 10min respectively (@ slide glass)

    ▲ CRITICAL STEP pipet can be used to blow in the liquid solutions

13. Device isolation: Si etching Unaxis 790: 100w power, 40mT, CF_4 45SCCM, O_2 5SCCM, 90+90+30sec for 180nm thick etching
14. Measurement (IV measurement)
15. (selective) Additional RTA process (temperature varies, (600c 30s))
16. (selective) top surface passivation: ALD deposition: 80 cycles of 0.015 sec trimethylaluminium ($Al(CH_3)_3$, TMA) precursor pulse, 5 sec N2 purging, 0.015 sec H2O precursor pulse with 200°C substrate temperature (8nm deposition by Wang’s group)

    ▲ CRITICAL STEP For III-V samples, it must necessary, but not in Si sample.

    (degradation was shown due to further annealing)

B1-3 Fabrication of GaAs/Diamond Heterojunction Bipolar Transistors (HBTs)

1. Cleaning process (GaAs EB epi)
    a. Using ultrasonic 3V in acetone (100 ml), IPA (100 ml), and DI water (100 ml) for 5 minutes and dry with nitrogen (N_2) gun thoroughly.

    ▲ CRITICAL STEP Diamond is already treated. Do not put it on the chemical solution except acetone and IPA (scrubbing is allowed)
2. Nanomembrane preparation (GaAs EB epi) and grafting process
    a. Patterning
        i. Spin coating – AZ1813, 2500rpm 30sec

        ▲ CRITICAL STEP Using 3" chuck, the sample is attached on the edge
        ii. Baking – 105°C 3min
        iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 30sec
        iv. Develop – MIF-321 30sec

        ▲ CRITICAL STEP Check all the sample using microscope
    b. O2 cleaning: Unaxis 790**:** 100w power, 20mT, O_2 20SCCM, 10sec
    c. GaAs etching: ICP etcher: RF1 (RIE): 60W, RF2 (ICP): 500W, BCl_3 10SCCM, Ar 5SCCM, 15mT

    ▲ CRITICAL STEP Depending on samples, target etching thickness varies
    d. PR removal: dip into acetone, and IPA

    ▲ CRITICAL STEP scrubbing is allowed.
    e. Soak into HF solution: diluted HF (1:20 (100ml) to 1:200 (200ml), 12min to 4-5hrs respectively)

    ▲ CRITICAL STEP Depending on samples etching rate and conditions varies. Need to test undercut time. Cf. 1:20 12min for 18R335,336 and 20R015, 1:200 4-5hrs for 20R016, 36, and 36 (inverted structure)
    f. After fully undercut, rinse using pipet and pick up process directly

    ▲ CRITICAL STEP GaAs NMs are very brittle, cannot use DI gun. Using wipers, soak the water and HF droplets every single time.
    g. Pick up process
        i. **Conventional method:** Mount the samples in the Old MJB, and attach prepared PDMS stamp to the nanomembrane, and quickly detach them from the GaAs substrates. Then, GaAs nanomembranes are on the PDMS stamps.
        ii. Clean the nanomembranes with MF321 and DI water drops by using pipettes. Carefully, soak the liquid with wipers.
        iii. **Double-Flip method:** Then, move the samples directly into DI water container made of Teflon. After shaking samples softly, the nanomembrane may arise, and float on the water surface.
        iv. Take a Teflon plate close to a nanomembrane. Then, it will be attached to the plate after flipping once. (1st filp)

v. While taking the plate and membranes still inside the water, get a prepared PDMS stamp, and attach the nanomembranes on it inside water. (2nd flip)
vi. If the nanomembranes are attached to the PDMS stamp, then carefully take it out of water.

▲ CRITICAL STEP The base surface always should be facing up out of water surface because of being hydrophobic, while the base surface is facing down to water inside because it is hydrophilic. You do not need to worry about which surface (base of emitter) is facing up and down. Sharp tweezer may help to handle the NMs in the water.

h. Grafting process
i. Cleaning the diamond sample thoroughly
ii. Mount the NMs on Diamond using MJB3
iii. After attaching the NM on the diamond, move it to table
iv. Detach the PDMS stamp slowly with from one corner to opposite side corner.

▲ CRITICAL STEP double side tape may help to attach the sample in the MJB3 and table. For cleaning process, rigid Q-tips may be necessary. In this process, nanomembranes can be easily cracked or moved on the PDMS stamp.

i. Bonding annealing: 350C 5min with N_2 ambient

3. (selective) Emitter etching process: depending on GaAs epi, emitter thickness is controllable. Then, ICP etcher: RF1 (RIE): 60W, RF2 (ICP): 500W, BCl_3 10SCCM, Ar 5SCCM, 15mT

▲ CRITICAL STEP Always check the etch rate, PR Asher may help to etch PR residue.

4. Metal patterning (Emitter)
a. O2 plasma treatment: Unaxis 790: 30w power, 50mT, O_2 50SCCM, 15sec
b. Patterning
i. Spin coating – AZ5214, 2500rpm 30sec

▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge

ii. Baking – 95°C 3min
iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 2.3sec
iv. Baking – 112°C 90sec
v. Post exposure – 25sec with the same light source
vi. Develop – AZ 917 MIF 28sec
c. O2 cleaning: Unaxis 790**:** 100w power, 20mT, O_2 20SCCM, 10sec
d. 1:20 HCl dipping to remove native oxide 20s -> rinse thoroughly

▲ CRITICAL STEP HCl solution need more time to rinse

5. Metal deposition: Ti/Pt/Au, 15/50/100nm
6. Lift off: dip into acetone and IPA 10min respectively (@ slide glass)

▲ CRITICAL STEP pipet can be used to blow in the liquid solutions, Q-tip is not recommended

7. Base Etching (CRITICAL ETCHING STEP!!): ICP etcher: RF1 (RIE): 60W, RF2 (ICP): 500W, BCl_3 10SCCM, Ar 5SCCM, 15mT

   ▲ CRITICAL STEP Always check the etch rate, PR Asher may help to etch PR residue, aside from the real sample, a few GaAs dummy samples should be involved to test etch rates. Final etching thickness can be measured with PR masking of edge side of the real sample.

8. Metal patterning (Base)
   a. Patterning
      i. Spin coating – AZ5214, 2500rpm 30sec

         ▲ CRITICAL STEP Using 3" chuck, the sample is attached on the edge

      ii. Baking – 95°C 3min
      iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 2.3sec
      iv. Baking – 112°C 90sec
      v. Post exposure – 25sec with the same light source
      vi. Develop – AZ 917 MIF 28sec
   b. O2 cleaning: Unaxis 790**:** 100w power, 20mT, O_2 20SCCM, 10sec
   c. 1:20 HCl dipping to remove native oxide 20s -> rinse thoroughly

      ▲ CRITICAL STEP HCl solution need more time to rinse

9. Metal deposition: Pd/Ge/Au, 30/40/100nm
10. Lift off: dip into acetone and IPA 10min respectively (@ slide glass)

    ▲ CRITICAL STEP pipet can be used to blow in the liquid solutions, Q-tip is not recommended

11. Collector Etching
    a. Patterning
       i. Spin coating – AZ1827, 4000rpm 30sec

          ▲ CRITICAL STEP Using 3" chuck, the sample is attached on the edge

       ii. Baking – 105°C 3min
       iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 60sec
       iv. Develop – MIF-321 90sec

          ▲ CRITICAL STEP Check all the sample using microscope

    b. O2 cleaning: Unaxis 790**:** 100w power, 20mT, O_2 20SCCM, 10sec
    c. GaAs etching: ICP etcher: RF1 (RIE): 60W, RF2 (ICP): 500W, BCl_3 10SCCM, Ar 5SCCM, 15mT (1-2 step)

       ▲ CRITICAL STEP Always check the etch rate (GaAs NMs is very thin)

    d. P- diamond layer etching: 790 ICP RIE: RF1 (RIE): 250W, RF2 (ICP): 0W, CF_4 90SCCM, O_2 2SCCM, 50mT (~528V DC, ~90nm/3min)

       ▲ CRITICAL STEP check the current level to verify the p+ layer. Using IV measurement equipment. 3mA-5mA would be ok @10V, check PR thickness every time before starting etching process, if need, re-pattern the mesa patterning (step #11-a).

    e. PR removal: dip into acetone and IPA 10min respectively (@ slide glass)

▲ CRITICAL STEP pipet can be used to blow in the liquid solutions, Q-tip is not recommended, PR Asher may help to remove remain PR.

12. Metal patterning (Base)
    a. Patterning
        i. Spin coating – AZ5214, 2500rpm 30sec

        ▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge

        ii. Baking – 95°C 3min
        iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 2.3sec
        iv. Baking – 112°C 90sec
        v. Post exposure – 25sec with the same light source
        vi. Develop – AZ 917 MIF 28sec
    b. O2 cleaning: Unaxis 790**:** 100w power, 20mT, O_2 20SCCM, 10sec
    c. 1:6 BOE dipping to remove native oxide 20s -> rinse thoroughly

    ▲ CRITICAL STEP BOE solution is extremely corrosive.

13. Metal deposition: Ti/PT/Au, 50/50/100nm
14. Lift off: dip into acetone and IPA 10min respectively (@ slide glass)

    ▲ CRITICAL STEP pipet can be used to blow in the liquid solutions, Q-tip is not recommended

15. RTA process: 350°C for 15sec at N_2 ambient

    ▲ CRITICAL STEP This condition is newly optimized condition. Check using dummy sample first.

16. Interconnection
    a. Oxide deposition (PECVD): PT70: deposition pressure 900mT, N_2O: 900SCCM, 2% Silane: 400SCCM, RF power: 25W, Substrate temperature 250°C (0.58nm/s)

    ▲ CRITICAL STEP Typical thickness: 700nm, please check the total height difference of the samples.

    b. Via patterning
        i. 1st Spin coating – AZ5214, 2500rpm 30sec

        ▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge

        ii. Baking – 95°C 3min
        iii. 2nd Spin coating – AZ5214, 2500rpm 30sec
        iv. Baking – 95°C 3min
        v. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 4sec
        vi. Baking – 115°C 90sec
        vii. Post exposure – 50sec with the same light source
        viii. Develop – AZ 917 MIF 28sec
        ix. Hard baking 115°C 15min
    c. Via etching
        i. oxide etching Unaxis 790: 100w power, 40mT, CF_4 45SCCM, O_2 5SCCM

        ▲ CRITICAL STEP check the etch rate, check the current level to verify oxide is fully etched, check PR thickness every time before starting etching process, if need, re-pattern the mesa patterning (step #16-b).

        ii. 1:6 BOE dipping to remove remain thin oxide ~10s -> rinse thoroughly

        ▲ CRITICAL STEP BOE solution is extremely corrosive.

    d. Interconnection metal patterning
        i. Spin coating – AZ5214, 2500rpm 30sec

        ▲ CRITICAL STEP Using 3” chuck, the sample is attached on the edge

        ii. Baking – 95°C 3min
        iii. Lithography – MJB3 365nm (i-line), 5.5mW/cm^2(ch1), 2.3sec
        iv. Baking – 112°C 90sec
        v. Post exposure – 25sec with the same light source
        vi. Develop – AZ 917 MIF 28sec
    e. O2 cleaning: Unaxis 790**:** 100w power, 20mT, O_2 20SCCM, 10sec
    f. 1:6 BOE dipping to remove native oxide 20s -> rinse thoroughly

    ▲ CRITICAL STEP BOE solution is extremely corrosive.

    g. Metal deposition: Ti/Cu/Ti/Au, 25/1100/25/100nm

    ▲ CRITICAL STEP Depending on oxide thickness, Cu thickness varies.

17. Lift off: dip into acetone and IPA 10min respectively (@ slide glass)

    ▲ CRITICAL STEP pipet can be used to blow in the liquid solutions

18. IV measurement
19. Current gain measurement (Gummel plot)