

HETEROSTRUCTURE MODIFICATIONS, FABRICATION  
IMPROVEMENTS, AND MEASUREMENT AUTOMATION OF  
SI/SiGE QUANTUM DOTS FOR QUANTUM COMPUTATION

*by*

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A dissertation submitted in partial fulfillment of  
the requirements of the degree of

DOCTOR OF PHILOSOPHY

(Physics)

*at the*

UNIVERSITY OF WISCONSIN-MADISON

2021

Date of final oral examination: April 27, 2021

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# Abstract

Quantum computing – leveraging quantum phenomena to perform complex and otherwise intractable computational problems – has rapidly progressed from a theoretical aspiration to a potential reality. Currently, there are many competing approaches to the way the physical qubits (quantum bits) are built, from trapped ions, to superconducting circuits, to semiconductor quantum dots, and beyond. Here, we focus on quantum dots, where electrons or holes are confined within a semiconductor and the quantized nature of charge and spin are utilized for computation. Within the field of quantum dots, heterostructures made of silicon and silicon-germanium are especially enticing due to their low density of defects and nuclear spin. Although quantum dots are a promising avenue for quantum computation because of their intrinsically small size and similarity to classical transistors, nearly every aspect of their design, realization, and control has yet to be fully optimized.

This thesis explores modifications to the heterostructure, fabrication, and measurement of Si/SiGe quantum dots in the pursuit of improved quantum dot qubits. The valley splitting in silicon quantum dots, a near degeneracy of the lowest lying energy states, is critical to the formation and performance of silicon qubits. In this work, we present several modifications to the Si/SiGe heterostructure in an effort to enhance this splitting. In particular, we investigate the effects of introducing germanium to the silicon quantum well by the inclusion of a single spike in germanium concentration or an oscillatory concentration throughout the well. We present experimental measurements of the energy spectrum arising from both modifications and, coupled with theoretical support, demonstrate enhancements to the valley splitting.

Next, we present several fabrication techniques with the goal of improved quantum dot functionality and lowered charge noise, a major barrier to higher quality devices. We report a new strategy for etched-palladium fabrication and discuss the current progress. Finally, we present work towards the automation of quantum dot tuning. As quantum dot devices increase in the number of qubits, so do the number of electrostatic gates which control the device. We discuss the development of automated tuning procedures and present a procedure for the formation of well-controlled quantum dots from initial voltage settings.

# Acknowledgments

This thesis, and the path I took to it, was supported and guided by so many people in so many ways. Though this Acknowledgments section cannot fully describe my gratitude, I'd like to recognize and thank many who have helped me in this journey toward a physics PhD.

Firstly, I'd like to thank the members of my defense committee, Prof. Mark Eriksson, Dr. Mark Friesen, Prof. Robert Joynt, Prof. Victor Brar, and Prof. Jason Kawasaki, for accepting this role, reviewing this thesis, and attending my defense.

Before I attended the University of Wisconsin–Madison for graduate school, I was enriched by the mentorship and instruction of excellent teachers and physicists. In high school, Dr. Arjumand Haque was my patient, compassionate, and entertaining physics teacher, and the reason I chose physics over other science fields. For my time in undergrad, at The Ohio State University, I want to thank Dr. Jim Beatty, Dr. Patrick Allison, Dr. Robert Perry, Dr. Tom Lemberger, Dr. John Draskovic, Dr. Stan Steers and the rest of the excellent physics and astronomy professors I had. I also want to thank Dr. Stefan Wehner, Dr. Christian Fischer, and Dr. Liz Rösken from my time at Universität Koblenz.

Over the past six years, I have had the privilege of learning from and researching with my advisor, Mark Eriksson. Before I had even accepted my graduate school offer, he agreed to let me research in his group during the summer before classes, a critical reason I finally decided on UW. Mark has been a fount of knowledge on all things quantum dots, and his unyielding optimism is surely partly the reason why anything I've achieved in this work has been a success. Mark's philosophy that all his students should earning not just their own

PhD, but everyone's around them too, is the reason why I've had the opportunity to work on so many different projects and learn so many different skills.

I'd also like to especially thank the second half of 'Mark & Mark', Mark Friesen. Valley splitting, at least to me, can be a complex beast and Mark has slain it. He has been an invaluable resource to me in so many ways. On the subject of theorists, Sue Coppersmith and Bob Joynt have both helped me immensely. The scientific tag-team of Mark and Sue is unbeatable. Bob, hopefully known to history as the inventor of the Wiggle Well, is ultimately the source of what I consider to be my most interesting and promising research. Of course, much of this work would be impossible without the heterostructures grown by Don Savage. Don's 'outsider' perspective on quantum dots has also made him invaluable collaborator on presentations and publications.

In addition to these advisors and mentors, many other UW staff members have been a great help. In the physics department, Ann Austin is a wizard of purchasing, and has been more efficient, helpful, and patient than I thought possible. Sara Yaeger, who runs the student machine shop, ensured my very first project with Mark (evaporator shielding upgrades) was a success. The cleanroom staff, including Dan Christensen, Kurt Kupcho, Quinn Leonard, Hal Giles, and Ed Gonzales, have trained me and advised me on all things fab. Finally, Gabe Berhardt from the helium facility has miraculously keep the liquid helium flowing, despite international embargoes, pandemics, quenches, and leaks.

For my peers, there are too many memories and too many ways you've helped me to do any of them justice. I'll simply mention, by name and in no particular order, Ryan Foote, Joelle Corrigan, JP Dodson, Ekmel Ercan, Adam Frees, Ben Harpt, Nathan Holman, Gabriel Jaffe, Emily Joseph, Trevor Knapp, Merritt Losert, Evan MacQuarrie, Sam Neyens, Alex Opremcak, Mario Palma, Will Ruchotzke, Luke Smith, Brandur Thorgrímsson, Leah Tom, Jose Carlos Abadillo-Uriel, Michael Wolfe, Yuan-Chi Yang, and Guoji Zhang.

While at UW, I also had the opportunity to collaborate with researchers at NIST. I'd like to thank Justyna Zwolak and the rest of our collaborators for a rewarding effort to automate

and improve quantum dot device tuning. In addition to the collaboration, I'd like to thank Justyna for inviting me on a visit to NIST, which led to my post-doc position with Michael Stewart and Garnett Bryant.

Lastly, I'd like to thank my friends and family for supporting me both in physics and in life. Thank you to my parents, my brother, and my ever-supportive wife, Amy.

### **Funding acknowledgments:**

This research was sponsored in part by the NSF through Grant Number DMR-1206915, by the Army Research Office (ARO) through Grant Number W911NF-17-1-0274, and the Vannevar Bush Faculty Fellowship program sponsored by the Basic Research Office of the Assistant Secretary of Defense for Research and Engineering and funded by the Office of Naval Research through Grant No. N00014-15-1-0029. Development and maintenance of the growth facilities used for fabricating samples was supported by DOE (DE-FG02-03ER46028). We acknowledge the use of facilities supported by NSF through the UW-Madison MRSEC (DMR-1720415) and the MRI program (DMR-1625348). The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Army Research Office (ARO), or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation herein.

Additional acknowledgments can be found in Ch. 3.

# Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
1.1	Motivation for this Work . . . . .	1
1.2	Thesis Outline . . . . .	3
<b>2</b>	<b>Basics of Silicon Quantum Dots for Quantum Computation</b>	<b>5</b>
2.1	Silicon Quantum Dots: An Overview . . . . .	5
2.1.1	Quantum Confinement . . . . .	5
2.1.2	Energy Landscape of Quantum Dots . . . . .	8
2.1.3	Valley States in Si Quantum Dots . . . . .	9
2.1.4	Quantum Computing with Si Quantum Dots . . . . .	12
2.2	Standard Fabrication for Si/SiGe Devices . . . . .	15
2.2.1	Lithography . . . . .	15
2.2.2	Standard Process Flow . . . . .	17
2.3	Standard Heterostructure and Quantum Dot Measurements . . . . .	22
2.3.1	Classical Hall Effect . . . . .	22
2.3.2	Quantum Hall Effect . . . . .	25
2.3.3	Coulomb Blockade . . . . .	31
2.3.4	Charge Sensing . . . . .	34
2.3.5	Lever Arm Measurement . . . . .	36
2.3.6	Low-frequency Noise Characterization . . . . .	38

2.3.7	The Charge Stability Diagram . . . . .	40
2.3.8	Magnetospectroscopy . . . . .	42
2.3.9	Pulsed-Gate Spectroscopy . . . . .	45
<b>3</b>	<b>Valley Splitting Control Through Heterostructure Modifications</b>	<b>49</b>
3.1	Intentional Mis-Cut of the Heterostructure for Valley Splitting Enhancement	49
3.1.1	Introduction to Mis-Cut Heterostructures . . . . .	49
3.1.2	Methods . . . . .	51
3.1.3	Mis-Cut Results . . . . .	53
3.2	Valley Splittings in Si/SiGe Quantum Dots with a Germanium Spike in the Silicon Well . . . . .	55
3.2.1	Introduction . . . . .	55
3.2.2	Experimental Methods . . . . .	57
3.2.3	Experimental Results . . . . .	59
3.2.4	Theory . . . . .	62
3.2.5	Conclusions . . . . .	66
3.2.6	Acknowledgments . . . . .	66
3.2.7	Appendix: Magnetospectroscopy Data Acquisition and Registration .	67
3.2.8	Appendix: Magnetospectroscopy Fitting . . . . .	69
3.2.9	Appendix: $g$ -factor Measurement . . . . .	71
3.2.10	Appendix: Electric Field Tuning of states in the Quantum Dot . . . .	71
3.2.11	Appendix: Envelope functions for the tight-binding simulations . . .	74
3.3	Quantum Hall measurements of the Ge spike heterostructure . . . . .	76
3.3.1	Anomalous Behavior in Quantum Hall Data . . . . .	76
3.3.2	Possible Origins of Anomalous Behavior . . . . .	81
3.4	The Wiggle Well: enhancing valley splitting by oscillating the germanium concentration in silicon quantum wells . . . . .	84
3.4.1	Introduction . . . . .	84

3.4.2	Wiggle Well Theory . . . . .	85
3.4.3	Experimental Methods . . . . .	87
3.4.4	Experimental Results . . . . .	90
3.4.5	Tight-Binding Simulations and Alloy Disorder . . . . .	92
3.4.6	Conclusions . . . . .	94
3.4.7	Acknowledgments . . . . .	95
3.4.8	Appendix: Additional WW theory . . . . .	95
3.4.9	Appendix: Heterostructure Growth . . . . .	95
3.4.10	Appendix: Fabrication Details and Hall Measurement . . . . .	96
3.4.11	Appendix: Gate Lever Arms for Dot Tuning . . . . .	97
<b>4</b>	<b>Improvements and Alternatives to Quantum Dot Fabrication</b>	<b>99</b>
4.1	Fabrication Changes for 2DEG Transport Mobility Improvements . . . . .	100
4.1.1	Introduction to Mobility-Limiting Charge Defects . . . . .	100
4.1.2	Fabrication Modifications . . . . .	101
4.1.3	Results . . . . .	102
4.2	Localized Implantation of Phosphorus Atoms for Donor-Dot Qubits . . . . .	103
4.2.1	Introduction to Donor Atom Quantum Dots . . . . .	103
4.2.2	Fabrication Methods of the Donor-Dot Device . . . . .	105
4.2.3	Quantum Dot Measurements of the Donor-Dot Device . . . . .	107
4.2.4	Outlook . . . . .	109
4.3	SPARTA: Subtractive Palladium Anneal-Ready	
	Two-layer Architecture . . . . .	110
4.3.1	Introduction . . . . .	110
4.3.2	SPARTA Fabrication . . . . .	111
4.3.3	SPARTA Challenges . . . . .	117
4.3.4	Fabrication Recipes for SPARTA . . . . .	119

<b>5</b>	<b>Automation of Quantum Dot Measurements</b>	<b>123</b>
5.1	Auto-Tuning Methods . . . . .	124
5.1.1	Review of Automated Tuning Approaches . . . . .	124
5.1.2	Automated Tuning Using Neural Network Classification of Quantum Dot States . . . . .	125
5.2	Bridging the Gap Between Device Turn-On and Dot Manipulation: Cold-Start Tuning . . . . .	127
5.2.1	Initialization . . . . .	128
5.2.2	Global Turn-On . . . . .	129
5.2.3	Center Screening Gate Pinch-Off . . . . .	130
5.2.4	Ohmic Sweeps and Bias Compensation . . . . .	131
5.2.5	Individual Channel Turn-On . . . . .	133
5.2.6	Individual Reservoir Turn-On / Pinch-Off . . . . .	134
5.2.7	Triangle Plots . . . . .	135
5.2.8	Finger Gate Pinch-Offs . . . . .	138
5.2.9	Wall-Wall Plots . . . . .	139
5.2.10	Transition to a Charge-Sensed Quantum Dot System . . . . .	141

# List of Figures

2.1	Quantum dot confinement in silicon heterostructures . . . . .	6
2.2	Fundamentals of the electronic structure of silicon . . . . .	9
2.3	Valley states in a strained silicon well . . . . .	11
2.4	Basics of quantum dot qubits . . . . .	13
2.5	The lithographic fabrication process . . . . .	16
2.6	Micron-scale fabrication of quantum dots . . . . .	18
2.7	Nanometer-scale fabrication of quantum dots . . . . .	20
2.8	Classical Hall effect . . . . .	24
2.9	Fundamentals of the quantum Hall effect and Shubnikov-de Haas oscillations	28
2.10	Example quantum Hall and Shubnikov-de Haas oscillation data . . . . .	30
2.11	Coulomb blockade of a quantum dot . . . . .	31
2.12	Charge sensing quantum dots . . . . .	35
2.13	Thermal lever arm measurement . . . . .	37
2.14	Low-frequency noise measurement of a quantum dot . . . . .	38
2.15	Double quantum dots . . . . .	40
2.16	Magneto spectroscopy of a quantum dot . . . . .	43
2.17	Pulsed gate spectroscopy of a quantum dot . . . . .	46
3.1	SiGe heterostructures on intentionally mis-cut substrates . . . . .	50
3.2	Hall bar resistances on a 4° mis-cut heterostructure . . . . .	52

3.3	Valley splitting results of mis-cut heterostructures . . . . .	54
3.4	Ge Spike Heterostructure and devices . . . . .	57
3.5	Magneto spectroscopy of a quantum dot . . . . .	60
3.6	Tight-binding results of the Ge spike heterostructure . . . . .	64
3.7	Registration of magneto spectroscopy data. . . . .	67
3.8	Electron $g$ -factor measurement. . . . .	72
3.9	Gate tuning for experimental and simulated electric field tunings. . . . .	73
3.10	Electric field tuned magneto spectroscopy at the 3-4 electron charging transition	74
3.11	Hall bar resistances on the Ge spike heterostructure . . . . .	77
3.12	Fan diagrams of the Ge spike heterostructure . . . . .	78
3.13	Labeled SdHO minima in inverse magnetic field for the Ge spike heterostructure	79
3.14	SdHO minima and quantum Hall plateaus of the Ge spike heterostructure . .	80
3.15	Simulation of a Hall bar with two conduction channels . . . . .	83
3.16	The Wiggle Well . . . . .	86
3.17	Growth and measurement of a Wiggle Well . . . . .	88
3.18	Energy of a Wiggle Well quantum dot. . . . .	91
3.19	Valley splitting of the Wiggle Well near $q=20$ . . . . .	96
3.20	Wiggle Well Hall Bars . . . . .	97
3.21	Lever arms for voltage tunings . . . . .	98
4.1	Mobility dependence of offset thickness and fabrication processing . . . . .	102
4.2	Windowed implantation of phosphorus ions . . . . .	105
4.3	Double-dot device fabricated over donor-implanted heterostructure . . . . .	107
4.4	Transport and charge sensed evidence of donor transitions . . . . .	108
4.5	Comparison of resist structure for positive and negative tone lithography . .	112
4.6	Comparison of fabrication layers for the overlapping Al design and SPARTA	114
4.7	SPARTA layer design . . . . .	115
4.8	Fabrication difficulties with the SPARTA process . . . . .	117

5.1	Labeled gates of a triple dot device . . . . .	128
5.2	Global turn-on of a quantum dot device . . . . .	129
5.3	Pinch-off curve of the central screening gate . . . . .	131
5.4	Ohmic bias sweeps for bias compensation . . . . .	132
5.5	Pinch-off curve for a single reservoir gate with example fits . . . . .	134
5.6	Schematics of a triangle plot without and with narrow channel conduction .	136
5.7	Example data for narrow channel conduction and the triangle plot . . . . .	137
5.8	Example finger gate pinch-off curves . . . . .	139
5.9	Wall-wall plot and tuned plunger gate plot of a quantum dot . . . . .	140

# List of Tables

3.1	Extracted spin-splittings from magnetospectroscopy . . . . .	61
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# Chapter 1

## Introduction

### 1.1 Motivation for this Work

The ubiquity and utility of computers in our world is ever expanding. However, there are certain valuable computational problems that will always remain out of reach of so-called classical computers. Since their conception 40 years ago, quantum computers have emerged as a novel computational method with the promise of solving some of these problems. Quantum computers differ from their classical counterparts by obeying quantum mechanics and leveraging two of its foundational principles: superposition and entanglement [1]. Similar to classical computers, quantum computers are built from bits, but these quantum bits – qubits – are not restricted to the binary values of zero or one. Instead, a single qubit is a coherent superposition of zero and one, described by an amplitude and a relative phase. With two or more qubits, quantum entanglement between them allows for more complex computational logic than classical computers. Put simply, a system with  $n$  qubits holds  $2^n$  possible states, meaning that the computational power of quantum computers grows exponentially with the size of the system.

The large-scale computational tasks that quantum computers are envisioned to solve, such as simulation of large quantum systems [2], prime factorization [3], database search [4], and

large-scale optimization [5], are still ahead of us. Promisingly, there are several quantum computing strategies that are increasingly successful. Of note, quantum computers with dozens of individual qubits have been build out of superconducting circuits or trapped ions [6, 7]. At the time of this writing, the largest chemical simulation on a quantum computer has been a 12 qubit modeling of the isomerization mechanism of diazene in a superconducting quantum computer [8].

Another quantum computing strategy, one which we focus on for this work, uses semiconductor quantum dots as qubits [9]. In brief, semiconductor quantum dots are free charges in a semiconductor tightly confined in three dimensions and cooled to very low mK-K temperatures. This confinement leads to quantization of the charge, in multiples of  $e$ , which occupy discrete energy levels much like electrons around an atom. The confinement arises from a combination of material choice and electrical gate control, depending on design specifics. These quantized levels provide the necessary basis for qubit formation. Within the field of semiconductor quantum dots, there are several host material choices, notably heterostructures of gallium and arsenic, silicon and silicon oxide, or silicon and germanium. Although quantum dots formed in these different heterostructures share many advantages and challenges, we focus here on Si/SiGe heterostructures where quantum dots form in a thin silicon layer sandwiched between layers of SiGe.

Quantum confinement in this heterostructure is achieved through band structure engineering of a silicon quantum well and through electrostatic control of metal gates on the heterostructure surface. Because of this, the design of both the heterostructure and the surfaces gates are key points of focus. In particular, conduction band electrons confined in silicon heterostructures exhibit a near-degeneracy of the lowest two energy levels called the valley states. The energy splitting between these states, the valley splitting, has important implications for qubit design and control. On the surface of the heterostructure, the gates laterally define the dots; their design and fabrication directly affect dot and noise performance. Finally, because most quantum dot qubit designs require multiple gates per qubit,

control of these gates rapidly becomes an intractable problem for heuristic control. For this reason, automation of quantum dot tuning and control is increasingly vital. In this work, we explore experiments concerning these three key concepts: heterostructures and valley splitting, gate fabrication, and measurement automation.

As this motivation is brief, please see Ref. [10] for a review of silicon quantum electronics. For a review of quantum computing, see Ref. [1]. For a review of low-dimensional semiconductor physics, see Ref. [11].

## 1.2 Thesis Outline

This work covers an array of experiments performed at the University of Wisconsin–Madison. Broadly put, this work focuses on Si/SiGe heterostructure modifications for enhancement of the valley splitting, gate fabrication modifications for improvements to device control and charge noise, and efforts towards the automation of quantum dot measurements.

Chapter 2 outlines the basics of silicon quantum dots for quantum computing and provides key explanations of terminology, techniques, and measurements used throughout this work. We begin with a discussion of quantum dot formation in silicon heterostructures, the origin and role of valley splitting, and how quantum dots can be manipulated as qubits. This is followed by a review of standard techniques and procedures for quantum dot fabrication. This chapter ends with a list of standard heterostructure and quantum dot measurements, from simple electron transport measurements to more complex energy spectroscopy.

Chapter 3 focuses on modifications to the heterostructure with the goal of controlling and increasing the valley splitting. Three different techniques for heterostructure modification are presented. First, silicon substrates with intentional mis-cuts to the surface are used to create double atomic steps at the heterostructure interfaces. We report the valley splitting in these mis-cut samples as measured in Hall bars. Next, a thin spike in germanium concentration is added to silicon quantum well, near the upper interface, to modify each valley wave function

and increase the valley splitting. In this heterostructure, the excited state spectrum of a few-electron quantum dot is measured via magnetospectroscopy. The final heterostructure modification presented is called the ‘Wiggle Well’, in which an oscillatory concentration of germanium is added throughout the quantum well. A singly occupied quantum dot in the Wiggle Well is measured using pulsed-gate spectroscopy, showing a large and tunable valley splitting.

Chapter 4 spans various efforts to modify the standard fabrication process of quantum dots for enhanced control and superior charge noise behavior. This chapter begins with simple thermal anneals and lithographic dose changes to improve the transport mobility in Hall bars. We also present attempts to create donor-dot devices in which an implanted phosphorus donor is coupled to a gate-defined quantum dot to create a qubit with the advantages of both systems. We conclude this chapter with an description of the progress towards ‘SPARTA’, a novel fabrication process in which etched palladium gates replace the current standard of overlapping aluminum gates.

Finally, in Chapter 5, we discuss efforts towards automation of the tuning of quantum dot devices, including work done in collaboration with scientists at the National Institute for Standards and Technology (NIST), and we present a routine for the formation of well-controlled quantum dots from initial voltage settings. We name this routine ‘cold-start’ tuning, as we begin tuning *ab initio* with no prior knowledge of the device performance. This is presented in a manner that can be coded into an automated procedure, and we discuss various scripting tools that are required.

## Chapter 2

# Basics of Silicon Quantum Dots for Quantum Computation

This chapter is an overview of the basics of silicon quantum dots for quantum computation. We present an overview of how quantum dots form, a typical quantum dot fabrication process, and key measurements useful for understanding and controlling these systems. Many of the concepts presented here are used throughout the rest of this work. This chapter may also serve as a helpful guide to those new to the field of silicon quantum dot qubits.

### 2.1 Silicon Quantum Dots: An Overview

#### 2.1.1 Quantum Confinement

A quantum dot can be defined as any system in which electrons (or holes) are confined into measurably discrete energy levels [12]. In silicon heterostructures, confinement is achieved through the design of the heterostructure and by applied gate voltages. Silicon is a semiconductor with a small ( $\sim$  eV) band gap between the fully occupied valence band and unoccupied conduction band (at zero temperature). The conductivity of silicon can be easily modified through impurity doping with n-type (electron) or p-type (hole) carriers. Externally applied

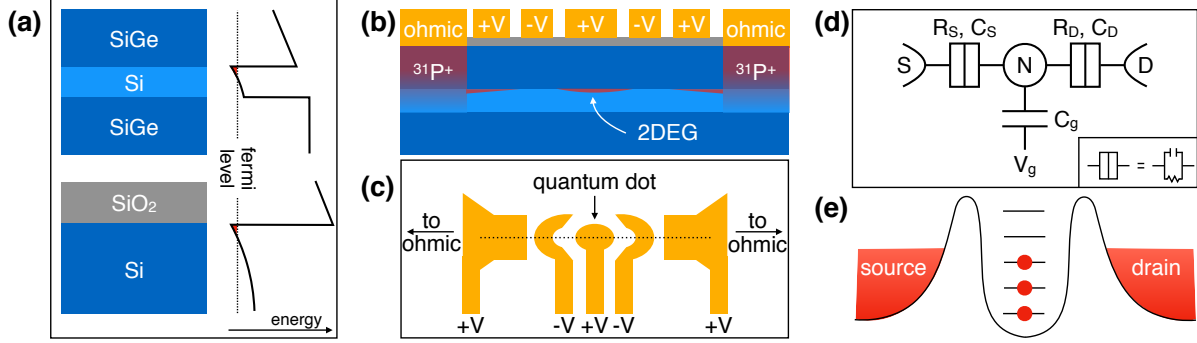


Figure 2.1: (a) Side-view schematic of Si/SiGe (top) and SiMOS (bottom) heterostructures on the left. The schematics to the right show the conduction band minimum for these heterostructures with a large positive voltage applied to the surface such that the upper interface of the silicon layer is lowered below the fermi level. A two-dimensional electron gas (2DEG) can then form at this interface. (b) Side-view schematic of a Si/SiGe quantum dot device. The surface gates (yellow) are isolated from the heterostructure by a dielectric (gray). With multiple surface gates, the 2DEG can be selectively formed and depleted to confine electrons into a quantum dot. (c) Top view schematic of a simplistic gate layout for a gate-defined, accumulation-mode quantum dot device. The central gate accumulates electrons into the quantum dot with a positive voltage. The next nearest gates deplete electrons surrounding the dot to define its extent with negative voltages. Larger gates to the sides create reservoirs of electrons that extend out to the phosphorus implanted regions. Ohmic metal, shown in (b), contacts these doped regions for direct current flow through the 2DEG. (d) Approximate circuit diagram for a quantum dot with  $N$  electrons coupled to a source and drain, controlled by a gate voltage  $V_g$ . (e) Schematic view of the energy in the quantum dot device along the dotted line in (c). Electrons inhabit quantized energy levels within the quantum dot, between reservoirs of a continuous density of states.

electric fields can also bend the conduction and valence bands of silicon across the fermi level to modify the conductivity. These techniques are used to create silicon transistors that make up nearly all modern electronics, but can also be leveraged to form quantum dots.

The two standard silicon heterostructures used to form quantum dots, Si/SiGe and SiMOS, are shown in Fig. 2.1(a). In both, the key to vertical confinement is the changing band gap across materials. In Si/SiGe, a  $\sim 10$  nm layer of silicon is sandwiched between layers of silicon-germanium, often  $\text{Si}_{0.7}\text{Ge}_{0.3}$ . The lattice constant of germanium is larger by 4.2%. With careful heterostructure growth, the thin silicon layer is under tensile strain from this lattice mismatch. The changing band gap and tensile strain leads to a significant ( $\sim 150$  meV) offset of the conduction band minimum of silicon compared to the surrounding

SiGe, creating a ‘quantum well’ [13,14]. The conduction band minimum of this heterostructure is shown schematically on the right side of Fig. 2.1(a). With an applied external electric field, the conduction band minimum can be pulled low enough to cross the fermi level. These newly populated conduction band states near the fermi level form a two-dimensional electron gas (2DEG) [11]. A 2DEG is a two-dimensional sheet of electrons, vertically confined by the triangular potential in the quantum well but free to move in any lateral direction. Typically, for strong confinement or low temperatures, all electrons occupy the same state in the confined direction, but exhibit a continuous density of states in the plane of the 2DEG. The situation is similar for SiMOS (silicon metal-oxide-semiconductor) heterostructures. The conduction band minimum of silicon is much lower than that of silicon oxide and leads to a similar quantum well and 2DEG at the interface between the two. The electric field which creates the 2DEG can be achieved by selectively doping a layer of the heterostructure, but for quantum dot applications, is most commonly created with positive voltages applied above the surface of the heterostructure. The quality of these 2DEGs can be described in a simple manner by their transport mobility, a measure of the ease of electron flow. Electron mobility is dependent on the density of conducting electrons, scattering from the roughness of the quantum well interface, and remote impurity scattering. In Si/SiGe heterostructures, the peak mobility is typically in the range of  $10^5 - 10^6 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  [15,16].

With vertical confinement achieved through careful engineering of the heterostructure, lateral confinement is accomplished through careful design of gates on the surface. By selectively applying positive or negative voltages to individual metallic gates, electrons in the 2DEG can be ‘corralled’ into small regions. Due to fabrication limitations of surface gates and a smaller in-plane effective mass, the lateral confinement is typically an order of magnitude weaker than the vertical confinement, on order 100 nm. Figure 2.1(b) shows a simple side-view schematic of a Si/SiGe quantum dot device. The 2DEG forms near the upper interface of the silicon quantum well and is selectively accumulated by gate voltages on the surface. These gates are separated from the heterostructure by a dielectric to avoid

direct current flow. At the sides of this schematic, phosphorus doped regions metalize the heterostructure. Metal contacts on the surface allow for direct current flow through the 2DEG. Figure 2.1(c) shows a top-down view of the gate design. The side gates accumulate electrons into a 2DEG, often referred to as a ‘reservoir’ of electrons. The central three gates selectively deplete and accumulate electrons into a quantum dot. Figure 2.1(d) shows an approximate circuit diagram for a single quantum dot coupled to a source, drain, and single gate voltage. Real quantum dot devices often have much more complex gate designs and will be discussed in more detail later in Sec. 2.2.2.

### 2.1.2 Energy Landscape of Quantum Dots

As mentioned, electrons in a quantum dot occupy measurably discrete energy levels. The electrons that make up the 2DEG naturally obey quantum mechanics and occupy unique states, but the confinement must be strong enough for these states to be distinguishable. Figure 2.1(e) shows a schematic representation of a quantum dot, showing quantized energies between the continuous density of states in nearby 2DEG reservoirs. If we suppose the lateral confinement of an imaginary quantum dot resembles an infinite square well in two-dimensions with 100 nm width and length, the ground and first excited states would be separated by roughly 0.6 meV, given the in-plane effective mass of silicon in the quantum well. Electrons confined within a quantum dot act much like the electron orbits around atomic nuclei, leading to quantum dots sometimes being referred to as ‘artificial atoms’. The electrons occupy these orbital states, determined by the strength of confinement. This brings us to a critical point: for these states to be distinguishable, the thermal energy of the system must be much less than the energy separation of the quantum dot. As a point of reference, a reservoir at the boiling point of liquid helium (4.2 K) has a Boltzmann factor  $k_B T = 0.36$  meV. For this reason, nearly all quantum dot experiments are performed at sub-Kelvin temperatures.

In addition to the electrons occupying distinct states, adding electrons to a quantum dot requires overcoming the electrostatic repulsion of the electrons. The change in Coulomb

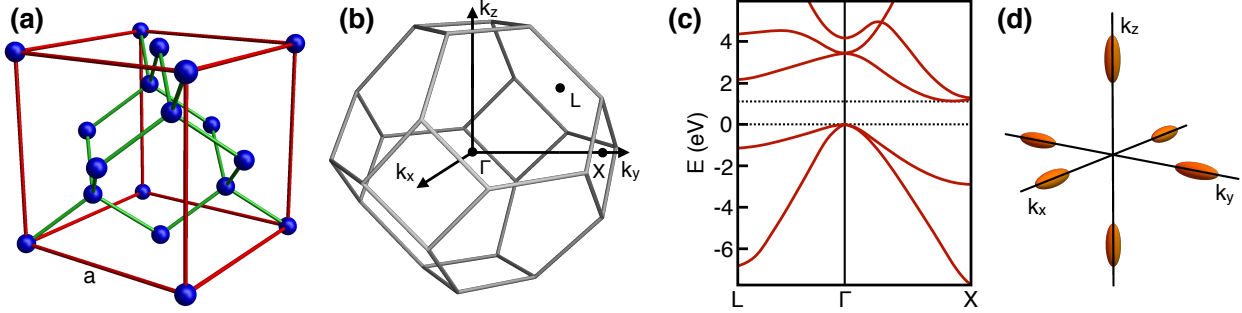


Figure 2.2: (a) The face-centered diamond-cubic structure of the silicon atomic lattice. The lattice constant of silicon is  $a = 0.543$  nm and the nearest neighbor atom separation is  $\frac{a}{4}(\hat{x} + \hat{y} + \hat{z})$ . (b) Edges of the first Brillouin zone boundary for silicon, with some high-symmetry points labeled. (c) Select portion of the band structure of silicon, showing the valence band maximum at the  $\Gamma$  point and the conduction band minimum in the  $X$  direction near the Brillouin zone boundary at  $k_0 = 0.82(2\pi/a)$ . (d) Constant energy surfaces above the conduction band minimum for the six degenerate points in reciprocal space. The asymmetric effective mass and tensile strain in Si/SiGe quantum wells lifts the in plane  $k_x$  and  $k_y$  minima well above the  $z$  valley minima.

energy is best described in terms of the capacitance,  $C$ , of the dot. Adding a single electron to a quantum dot requires overcoming the charging energy,  $E_C = e^2/C$  [17]. We can roughly approximate the capacitance of a quantum dot confined in a 2DEG by calculating the self-capacitance of a disk with radius  $R$ ,  $C_0 = 8\epsilon_r\epsilon_0 R$ . For  $R = 50$  nm, an approximation for the charging energy would be  $E_C = 4$  meV. Thus, we may expect the Coulomb energy to dominate the total energy required to add electrons to a quantum dot.

### 2.1.3 Valley States in Si Quantum Dots

Working in silicon adds an additional consideration to the energy landscape of a quantum dot: valley states. To understand valley states, we need to take a closer look at the chemical and electrical structure of silicon. The crystal lattice of silicon, shown in Fig. 2.2(a), has a face-centered diamond-cubic structure. Silicon has an indirect band gap, meaning the minimum of the conduction band is offset from the maximum of the valence band in reciprocal space. Figure 2.2(c) shows a small portion of the electronic band structure of silicon along two high-symmetry directions as labeled in Fig. 2.2(b). The band gap is  $\sim 1$  eV, with the

conduction band minimum at  $k_0 = 0.82(2\pi/a)$  where  $a = 0.543$  nm is the lattice constant. This leads to an important effect. Because silicon has cubic symmetry and a conduction band minimum away from the center of reciprocal space near the X point, there are six degenerate minima. These degenerate minima are called the valley states. Figure 2.2(d) shows a constant energy surface around the conduction band minima. Here, it is clear that the effective mass (curvature of the band structure in reciprocal space) differs in the transverse and longitudinal directions.

For quantum computing, degenerate energy states are undesirable. Thankfully, confinement within a 2DEG lifts this degeneracy. As mentioned, the effective mass of conduction band electrons in silicon is anisotropic. With confinement in the  $z$  direction as electrons are pulled against the Si/SiGe (or Si-SiOx) interface, the  $z$  valley states are confined in the 2DEG with the longitudinal effective mass ( $m_l = 0.91m_0$ ) while the  $x$  and  $y$  valley states are confined with the transverse effective mass ( $m_t = 0.19m_0$ ) [14]. This results in higher bound state energies for the  $x$  and  $y$  valleys, lifting their energies above that of the  $z$  valley states. In Si/SiGe heterostructures, the in-plane tensile strain caused by the lattice mismatch between silicon and the SiGe alloy additionally lifts the in-plane valley states. In a Si/SiGe heterostructure with 30% germanium in the alloy, the separation in energy of the  $z$  valley states and the  $x$  and  $y$  states is  $\sim 200$  meV.

With the in-plane valleys lifted, this leaves a two-fold degeneracy of the  $z$  valley states [14]. Within a quantum well, and with an applied vertical electric field, the pure plane wave Bloch functions of the valley states are no longer eigenstates. This vertical confinement within the quantum well and against the upper interface couples the two  $z$  valley states and creates eigenstates of the symmetric and antisymmetric combination of these two valleys. The Bloch oscillations, determined by the momentum vector  $k_0$  of the valley states, persist within an confining envelope determined by the well and electric field. These oscillations are rapid due to the large value of  $k_0$ . These two states are out of phase from one another by a quarter of a wavelength but share the same overall envelope. The resulting wave function densities

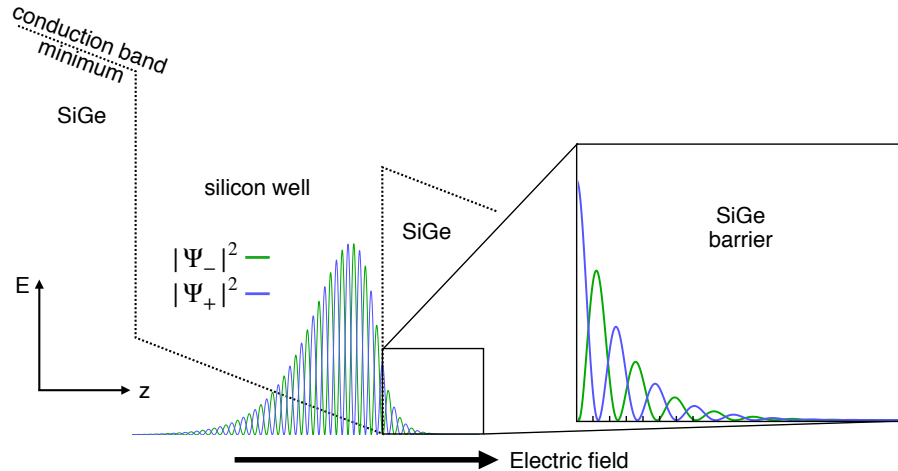


Figure 2.3: Schematic representation of the wave function densities of the symmetric and anti-symmetric valley states in a silicon quantum well. The overall wave function envelopes of the two states are identical, but the phase difference results in different extensions into the SiGe barrier. As shown in the expansion on the right, the total contribution to the wave function that exists in the higher energy barrier differs between the two states. This leads to a small but important lifting of the two-fold valley degeneracy.

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$|\Psi_{\pm}|^2$  are shown schematically in Fig. 2.3.

Focusing now on the evanescent portion of the wave functions that extend into the SiGe barrier (shown on the right of Fig. 2.3), the phase difference between the two states is clearer. The contribution to the wave function that exists inside this SiGe barrier is different for each state. Because the barrier has a higher energy, the differing contribution leads to an energy splitting between the two eigenstates. This energy splitting is referred to as the valley splitting. Theoretical modeling of the valley splitting in an ideal heterostructure predicts a splitting greater than 1 meV. However, in real devices, the valley splitting is significantly reduced by lattice disorder, interfacial defects, and atomic steps [18]. Valley splittings measured experimentally typically lie between 20 and 200  $\mu\text{eV}$  [19–31]. Because the valley splitting is determined by the extent to which the wave function envelope extends into the SiGe barrier, increasing the vertical electric field and pulling the wave function harder against the interface can increase the valley splitting. We discuss heterostructure modifications for valley splitting control in Ch. 3. For a more detailed analysis of valley

splitting in Si/SiGe heterostructures, refer to Ref. [32].

### 2.1.4 Quantum Computing with Si Quantum Dots

With a grasp of quantum dots, we now turn to a discussion of their use in quantum computers. First, however, we discuss what makes a system suitable for quantum computing. A set of 5 criterion, outlined by David P. DiVincenzo in 2000, succinctly describes the necessary requirements for the physical implementation of quantum computing [33]. These are:

1. A scalable physical system with well characterized qubits
2. The ability to initialize the state of the qubits to a simple fiducial state
3. Long relevant decoherence times, much longer than the gate operation time
4. A ‘universal’ set of quantum gates
5. A qubit-specific measurement capability

To understand these criteria, we introduce some quantum computing notation. A single qubit, with two distinct energies, is described by two degrees of freedom. We can write the qubit state as

$$|\psi\rangle = \alpha |0\rangle + \beta |1\rangle \quad (2.1)$$

where  $|\alpha|^2 + |\beta|^2 = 1$ . This system can be projected on the surface of a sphere, called the Bloch sphere [1]. This is shown in Fig. 2.4(a). Equation (2.1) then takes the form

$$|\psi\rangle = \cos\left(\frac{\theta}{2}\right) |0\rangle + e^{i\phi} \sin\left(\frac{\theta}{2}\right) |1\rangle. \quad (2.2)$$

For an arbitrary two qubit state, we write:

$$|\psi'\rangle = \alpha_{00} |00\rangle + \alpha_{01} |01\rangle + \alpha_{10} |10\rangle + \alpha_{11} |11\rangle, \quad (2.3)$$

likewise with a normalization condition for the complex coefficients.

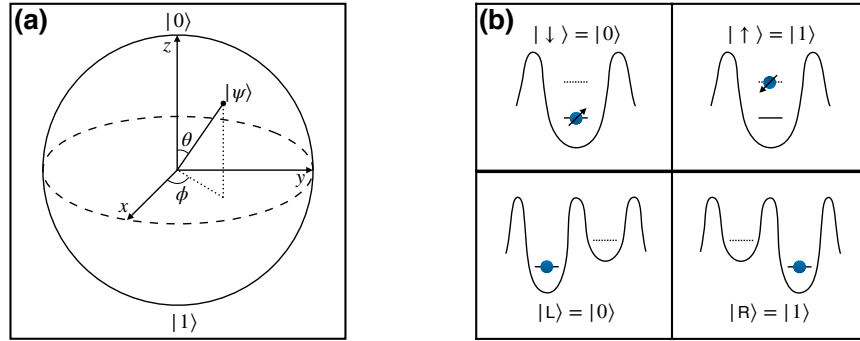


Figure 2.4: (a) Schematic of the logical states of a qubit on a Bloch sphere. The qubit state can be described by two angles,  $\phi$  and  $\theta$ . (b) Schematics of the logical states of a single spin qubit (top) and charge qubit (bottom). The single spin qubit states are split by an applied magnetic field. The charge qubit states differ by the difference in energy between each dot.

We can now discuss the DiVincenzo criteria with more clarity. A good quantum computing system must have qubits with well defined states  $|\psi\rangle$  (Criterion 1). The system must be capable of initialization, for example into the  $|00\rangle$  state (Criterion 2). The qubits states must persist for longer than the operation time (Criterion 3). In the Bloch sphere representation, we can describe ‘decoherence’ as a combined term for relaxation (loss of  $\theta$  information) and dephasing (loss of  $\phi$  information). The sources and timescales of dephasing and relaxation are often different. However, a mathematical limit places the maximum dephasing time as twice the relaxation time [1]. Criterion 4 requires that the full state of the system  $|\psi'\rangle$  must be fully controlled through single and multi-qubit manipulations. Finally, we must be capable of reading the quantum state of each qubit (Criterion 5).

A quantum dot-based qubit system was first proposed in 1998 [9]. In this proposal, the spin projections of a single electron quantum dot are used as the logical states. The energy splitting between the two states is set by an applied magnetic field. Since this proposal of a single spin qubit, many other qubit systems built from quantum dots have been proposed and experimentally realized. All qubit designs, however, leverage some combination of the spin and the orbital (positional) degree of freedom. The basis for these two qubit types, spin qubit and charge qubit, are shown in Fig. 2.4(b). In general, qubits which utilize spin have longer coherence times but slower manipulation times than charge-based qubits. An example qubit

design that utilizes both charge and spin is the quantum-dot-hybrid qubit, which consists of three electrons confined within two quantum dots [34,35]. The qubit states are defined by the singlet-triplet spin splitting between two electrons in a single quantum dot, but qubit control is achieved through charge manipulation between both dots. Qubits built from quantum dots are enticing due to their relatively small size and similarity to transistors which form the basis for classical computing. Building a large quantum computer with thousands or millions of qubits seems attainable, given the billions of transistors in a modern processor.

The first physically realized quantum dot qubits were in GaAs/AlGaAs heterostructures [36–38]. Dots formed in GaAs have several advantages over silicon: a smaller effective mass, higher mobility 2DEGs, and no valley states to consider. However, III-V elements (Ga and As) necessarily have non-zero nuclear spin. This spin environment acts as a significant source of decoherence in spin qubits. In contrast,  $^{28}\text{Si}$ , the main stable isotope of silicon, has zero nuclear spin. This inherent advantage has led to a gradual shift towards silicon and germanium heterostructures for quantum dot qubits over the last decade. The current state-of-the-art in silicon quantum dot qubits are two-qubit gates and multi-dot arrays [39–41]. Through isotopic purification of silicon, the highest single qubit gate fidelity (a measure of the accuracy of a quantum gate) achieved to-date is  $> 99.9\%$  in a single spin qubit [42].

Regardless of qubit design, valley splitting plays an important role in silicon quantum dot qubits. In single spin qubits, the spin relaxation time is often limited by the presence of the excited valley state. In the quantum-dot-hybrid qubit and the valley-orbit qubit, the valley splitting determines the logical states of the qubit [34,43]. Control of the valley splitting is of critical importance to any silicon qubit. We explore modifications to the heterostructure for valley splitting control in Ch. 3.

Similarly, good control of qubit parameters and proper state readout is heavily dependent on gate design. This varies significantly across the silicon dot community and the charge noise (another dominant source of noise for qubits) has been reduced with newer designs and fabrication methods [44]. We discuss modifications to fabrication processes for enhanced

control and lowered charge noise in Ch. 4.

Finally, as the size of the systems scale, heuristic control of all gate voltages becomes increasingly difficult. We present techniques for automation of various quantum dot tuning procedures in Ch. 5.

## 2.2 Standard Fabrication for Si/SiGe Devices

In this section, we describe standard fabrication procedures and designs used for silicon quantum dots. Details of Si/SiGe heterostructure growth, achieved through chemical vapor deposition (CVD) or molecular beam epitaxy (MBE), may be found in Ref. [14, 15, 45]. This information is useful as a reference for Ch. 4, where fabrication modifications are explored.

### 2.2.1 Lithography

Lithography, in the context of semiconductor device fabrication, describes a process in which a pattern is transferred, by means of an etch or a deposition, from a thin film called resist (often a polymer) to a substrate. The patterning of the resist is achieved through select exposure to light (photo-lithography) or high energy electrons (electron-beam-lithography). This process is shown schematically in Fig. 2.5.

The process begins with a substrate, such as a silicon wafer, and photo- or e-beam-resist. Liquid (but viscous) resist is deposited onto the substrate. By spinning the substrate at high speeds, the resist is thinned into a uniform layer across the substrate. This resist-substrate stack is then often thermally annealed to partially cure the resist.

Next, the resist is patterned. In photo-lithography, a photomask is used to transfer the pattern. Photomasks are transparent glass or quartz panes with an opaque chrome pattern printed on one side. By aligning the photomask to the substrate and shining collimated light through the mask, the resist is only exposed in the ‘unmasked’ region. Resist is photo-sensitive and is chemically altered by light exposure during patterning. In e-beam-

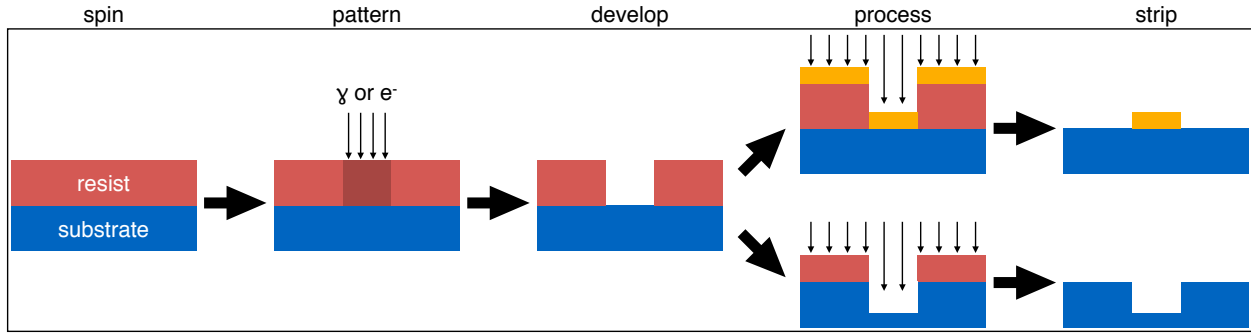


Figure 2.5: A standard lithographic process for semiconductor fabrication, from left to right. First, a photoresist or electron-beam resist is spun onto the substrate, typically followed by a thermal cure. Next, the resist is exposed to either light or high-energy electrons in a specific pattern. The pattern is then developed using a tuned chemical process to selectively remove either the exposed or unexposed resist. This pattern is then transferred to the substrate either through a deposition or an etch. Finally, the resist is chemically removed and only the material deposited or etched pattern remains.

lithography, a focused beam of electrons with energy 10 – 200 keV is rastered across the e-beam-resist to similarly expose the resist in a pattern. The resolution limit of photo-lithography is determined by the wavelength of light used for exposure. For optical or near-UV photo-lithography, this translates to a resolution limit in the hundreds of nm. For electron-beam lithography, the resolution limit is determined by both beam spread and choice of resist. Polymer based resists such as PMMA have resolution limits in the tens of nm. For this reason, larger structures  $> 1 \mu\text{m}$  are fabricated via photo-lithography and smaller structures, such as the voltage gates for quantum dots, are fabricated via e-beam-lithography.

After exposure, the pattern must be developed. As the exposed resist is now chemically altered, a chemical solution is used to selectively dissolve either the exposed or the unexposed regions. The process used is specific to each resist and the desired outcome.

Once developed, the patterned resist on the substrate can now be used as a stencil for various processing. In quantum dot fabrication, there is an array of etches and depositions that need to be performed in a patterned shape. The resist, as its name suggests, can be used to ‘resist’ etching of the substrate below. For depositions, the presence of the resist blocks any material making contact with the substrate surface.

After processing, the remaining resist must be stripped away. This is again a chemical process, similar to development. For depositions, removing the resist is often referred to as ‘lift-off’, because the excess deposition material on top of the resist is lifted off as the resist is dissolved.

At the end of the lithographic process, the substrate is left with either an additional patterned layer of material or an etched pattern. This process is repeated many times in typical quantum dot fabrication to achieve gate, oxide, implanted, and etched structures.

### 2.2.2 Standard Process Flow

Over the years, the Eriksson research group has developed a standard process flow for quantum dot fabrication on Si/SiGe heterostructures. This process can be roughly divided into two sections: micron-scale steps performed using a Nikon i-Line Stepper (photo-lithography) and nanometer-scale steps performed using an Elionix electron-beam-lithography tool. The resulting fabricated device after these two process flows are shown in Fig. 2.6.

#### Micro-fabrication of Quantum Dots

Photo-lithography is used for the majority of the fabrication steps. Starting with a Si/SiGe heterostructure grown on a silicon chip or wafer, alignment marks are patterned and etched into the heterostructure. The Stepper photo-lithography tool is capable of self-alignment of the masks to the substrate and the etched marks provide features for alignment. The physical etch of the SiGe is achieved through a dry plasma process, typically a fluoridated chemical such as  $\text{CHF}_3$  or  $\text{SF}_6$  combined with  $\text{O}_2$ .

Next, another etch of the heterostructure is performed to create what is referred to as the mesa. This step removes both the SiGe spacer above the quantum well and the silicon quantum well itself across the majority of the device. What is left is a small,  $150\ \mu\text{m}$  square mesa of heterostructure shown in the center of Fig. 2.6(a) and the entirety of Fig. 2.6(b). With this etch, a 2DEG may only form within the confines of this mesa. In this way,

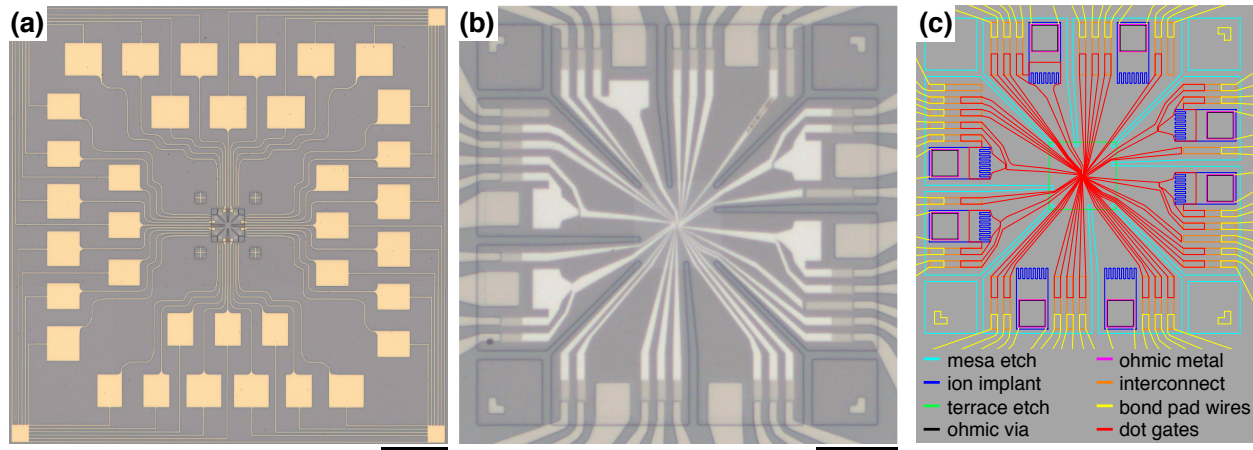


Figure 2.6: (a) Optical image of the photo-lithography fabrication of a quantum dot device, with a 300  $\mu\text{m}$  scale bar. The large gold pads are the bond pads for each gate, leading towards the center where the gates are fabricated. (b) Optical image of a quantum dot device, focused on the central ‘active region’ where electrons can accumulate, with a 30  $\mu\text{m}$  scale bar. The bond pad wires in this image are palladium (dark gray), and approach the center from all sides. The gate metal for this quadruple dot device is aluminum (light gray). The etched oxide terrace is visible as the lighter colored square in the center. (c) CAD schematic of the device shown in (b). Each color represents a different photo-lithography step, except for the red pattern which are the three layers of electron-beam-lithography.

unintended electron accumulation or current paths across other parts of the device is avoided.

After mesa definition, the ohmic contacts are implanted with phosphorus. As described previously in Sec. 2.1.1, regions of the heterostructure can be doped with free electron carriers, in this case phosphorus, to ‘metalize’ the silicon. This allows for direct electrical contact to the 2DEG. After resist patterning, the devices are sent to an external contractor who bombards the surface with high energy ( $\sim 20$  keV) phosphorus ions which implant into the heterostructure. A typical ion density for silicon devices measured at very low temperatures is  $1 - 5 \times 10^{20}$  ions/cm<sup>-3</sup>. After their return and removal of any resist or other mask, the devices are briefly annealed to 700 °C to repair any crystal damage from the implantation.

Next, a dielectric is deposited across the surface. This dielectric is typically aluminum oxide, deposited with an atomic layer deposition (ALD) tool. A small 32  $\mu\text{m} \times 32 \mu\text{m}$  square of oxide is etched away in the center of the device on the mesa. This is a wet etch using a buffered hydrofluoric acid. Following the etch, an additional layer of oxide is deposited.

With this process, we have created a thin oxide layer over where dots will form and a thicker layer elsewhere. This oxide ‘terrace’ is done to ensure good electrical isolation of gates across the entire device while minimizing the thickness near the dots. As will be discussed in Ch. 4, this is done in an attempt to minimize charge noise and minimize the distance between the surface gates and the 2DEG. With an oxide now covering the entire surface of the heterostructure, an etch step is required to remove the oxide over the phosphorus implanted region for good metallic contact. This is again a wet HF etch.

The final three micro-fabrication steps are metal depositions. These metal depositions are additive processes, meaning the resist is patterned first and the metal is deposited in the space where developed resist has been removed. The three metal layers to be deposited are the metal ohmic contacts to the ion implanted region, interconnects, and the bond pad wires. The metal for the ohmic contacts are deposited onto the bare silicon where the oxide was etched away. As the name suggests, the function of the interconnects is to connect the bond pad wires to the dot gate metal. Due to the limitations of attaching wires to bond pads on the surface of the substrate, the bond pad metal thickness should be  $\sim 200$  nm or greater. The dot gates however, with narrow  $< 100$  nm widths, need to be much thinner. Because the bond pads are deposited prior to the gates, achieving good step coverage of the thin gate metal on the thick bond pad metal is not guaranteed. For this reason, thin  $\sim 20$  nm interconnects are deposited first, such that the bond pads metal and gate metal can be deposited onto each end. For additional details on the role of interconnects, refer to Ref. [46]. These metal steps are clearly visible in Fig. 2.6(a-b). The metal used in (a) is a stack of thin titanium (for adhesion) followed by gold. The metal in (b) is titanium and palladium. These noble metals (Au and Pd) are used due to their resistance to oxidation, so that good connection to subsequent metal depositions can be made.

Figure 2.6(a) also shows an additional safety feature of our designs: bond pad straps. Because these quantum dot devices are small with very thin oxide layers separating each gate, they are extremely prone to damage from electrostatic discharge (ESD). To prevent

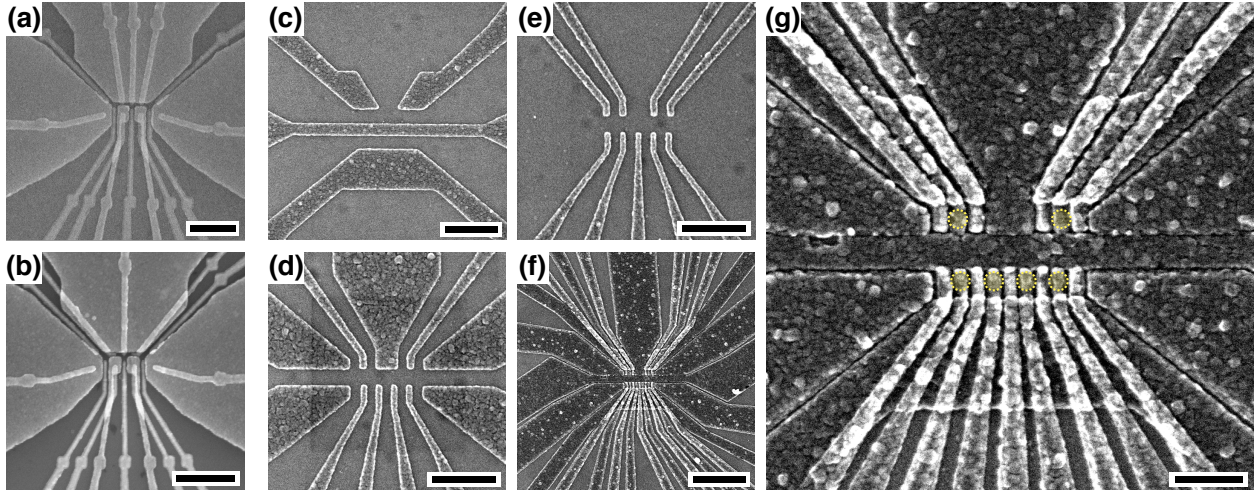


Figure 2.7: (a-b) SEM images of similar ‘open-style’ two-layer quantum dot devices. The gate material is gold, isolated by deposited aluminum oxide. The scale bar for both is 500 nm. (c-e) SEM images of the first, second, and third layer gates of an overlapping aluminum quadruple quantum dot device, with a 500 nm scale bar. (f) SEM image of a completed and layered device of the gate design in (c-e), with a 1  $\mu\text{m}$  scale bar. (g) Magnified image of the same device in (f), with a 250 nm scale bar. The locations of the quantum dots are highlighted with yellow circles, showing a linear array of four dots opposing two charge sensing dots.

this during fabrication, all bond pad wires are connected together with bond pad straps. These are the thin wires seen in Fig. 2.6(a) running along the outside edge of the image. This keeps all gates and ohmics at the same potential, reducing the chance of charge build-up and subsequent discharge. After the device is mounted and wired to a PCB with its own grounding system, these wires are cut with a diamond tipped blade.

### Design and Nano-fabrication of Quantum Dots

All that remains in fabrication is the dot gate lithography. The design of the micron-sized features and the division between photo- and e-beam-lithography is intended to allow for maximum versatility of gate design as far into the fabrication process as possible. All previous steps can be completed at the wafer scale to create hundreds of potential dot devices. Then, the wafer can be diced and the final steps of gate lithography can be completed as needed, with design iterations as desired.

Currently, most gate fabrication in the Eriksson group is done in an additive process, meaning gate metal lift-off is required. Figure 2.7 shows scanning electron microscope (SEM) images of two different gate styles. Figure 2.7(a-b) shows two iterations of an ‘open’ style design with two quantum dots in the center fabricated with two layers of gates. The layers are isolated from one another and the heterostructure surface by deposited aluminum oxide. Electrons can be loaded into the two dots from reservoirs at the top of the image. Charge sensing, discussed in Sec. 2.3.4, can be performed on either side of the device. This design style has been successfully implemented for two-axis control of a singlet-triplet qubit [47], measurement of transport through an impurity coupled to a quantum dot [48], characterization of a double dot in a Si/SiGe nanomembrane [49], and a programmable two-qubit quantum processor in silicon [40].

Despite these successes, a newer design with greater control, less dielectric, and a tighter design has taken hold as the standard for silicon quantum dot fabrication. We’ll refer to this design here and elsewhere in this work as the ‘overlapping aluminum gate design’. Pioneered in 2007, this design is based on tightly packed or overlapping aluminum gates, isolated from one another by a thin layer of oxidation of the aluminum itself [50]. In this way, no deposited dielectric is needed between each gate layer. This oxidation can be enhanced in a number of ways, most notably by an oxygen plasma ash, as described in Ref. [46]. Figure 2.7(c-e) shows an SEM image of a typical three-layer design for a quadruple quantum dot. The first layer of gates, referred to as the ‘screening’ gates, are used to deplete electrons with low or negative voltages, allowing the 2DEG to form only between these gates. The second layer is the accumulation layer, with larger reservoir gates to the sides and individual ‘plunger’ gates for control of the chemical potential of the dots. This design has two charge sensors in the upper channel opposing the linear array of four dots. The third and final layer defines the ‘barrier’ or ‘tunnel’ gates, which control the tunneling between dots and to the reservoirs. Figure 2.7(f) shows all three layers together. Figure 2.7(g) shows a much higher magnification SEM image of the same device. The alignment of the second and third layer

gates between the screening gates is clear. The overlapping aluminum gate design has been used in a two-qubit gate in MOS [39], a two-qubit gate in Si/SiGe [41], and an exchange-only triple dot qubit [51]. Another main advantage of this design is its inherent extensibility to large dot arrays; a nine dot linear array has been shown to be stable and controllable [52].

This section is meant merely as an introduction and overview of typical quantum dot fabrication and is in no way an exhaustive list of quantum dot gate designs. Designs are often tailor-made to the desired goal or qubit design. Certain qubits such as the single spin qubit in silicon require either an electron spin resonance (ESR) gate or a micro-magnet for full control of the qubit state. Additionally, various readout or qubit coupling schemes involve specific gate designs or additional resonance circuits [53–55]. We discuss modifications to these fabrication processes in Ch. 4.

## 2.3 Standard Heterostructure and Quantum Dot Measurements

In this section, we introduce and describe key measurement techniques that are used throughout this work. We begin with a discussion of Hall bar measurements, which can characterize key parameters of a 2DEG. Then, we describe various quantum dot measurements, from dot formation to energy spectroscopy.

### 2.3.1 Classical Hall Effect

The classical Hall effect is a remarkably simple phenomenon arising from electric current in a perpendicular magnetic field. Simply put, when electrons flow perpendicular to an applied magnetic field, a voltage builds transverse to the electron flow. This is just the Lorentz force law, that a force exists on a charge  $q$  with velocity  $\vec{v}$  in a magnetic field  $\vec{B}$ :  $\vec{F} = q(\vec{v} \times \vec{B})$ . The power of the effect comes with understanding how the electrons flow according to the applied voltage bias and magnetic field.

For the classical Hall effect, the 2DEG can be described simplistically by the Drude model [56]. In this model, conducting electrons move in a similar manner to ideal gases. We assume electrons scatter with scattering time  $\tau$ , scattered electrons return to zero momentum, and electrons respond to external electric and magnetic fields in-between scattering events. From this, the change in momentum of an electron in an electric and magnetic field is

$$\frac{d\vec{p}}{dt} = -e(\vec{E} + \vec{v} \times \vec{B}) - \frac{\vec{p}}{\tau}. \quad (2.4)$$

We can replace the momentum with  $m^*\vec{v}$ , and then define the electric current as  $\vec{j} = -en\vec{v}$ , where  $n$  is the density of conducting electrons. With these substitutions and assuming a steady state such that  $d\vec{p}/dt = 0$ , the electric field is

$$\vec{E} = \left( \frac{1}{ne} \vec{j} \times \vec{B} + \frac{m^*}{ne^2\tau} \vec{j} \right). \quad (2.5)$$

We can see here that in addition to the field along the direction of current flow, there is a field transverse to both the current and the field. This creates a voltage called the Hall voltage. We can define a resistivity matrix  $\rho$  as  $\vec{E} = \rho \vec{j}$ . If we imagine a current along the  $x$ -direction and a magnetic field along the  $z$ -direction, the Hall resistivity is

$$\rho_{xy} = \frac{B}{ne} \quad (2.6)$$

and the resistivity along the current flow is

$$\rho_{xx} = \frac{m^*}{ne^2\tau}. \quad (2.7)$$

Herein lies the purpose. By measuring these resistivities, the electron density and the scattering time can be determined. In a 2DEG, the dimensionality reduces to two and the electron density becomes a two-dimensional density  $n_{2D}$ . Typically, the 2DEG is formed into a bar

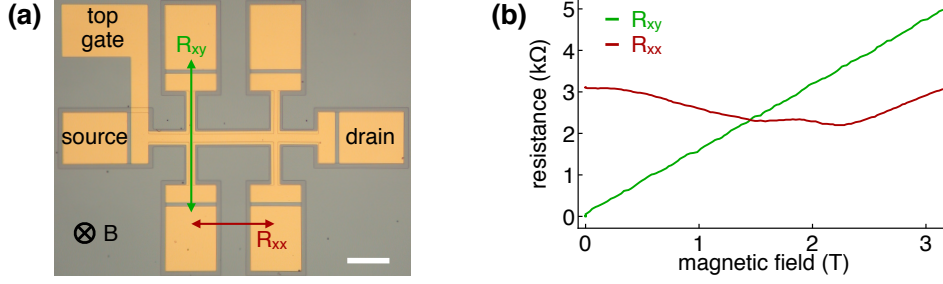


Figure 2.8: (a) Optical image of a Hall bar with a 200  $\mu\text{m}$  scale bar. The labeled top gate is used to accumulate electrons in the quantum well of the Hall bar (center). A voltage bias is applied and a current flows from the source to the drain ohmic. Longitudinal ( $R_{xx}$ ) and transverse ( $R_{xy}$ ) resistances are measured as a perpendicular magnetic field is swept. (b) Classical Hall resistances for  $R_{xx}$  and  $R_{xy}$  showing the expected linear slope of the transverse ( $R_{xx}$ ) resistance. This measurement shows a carrier density  $n_{2D} = 3.99 \times 10^{11} \text{ cm}^{-2}$  and a transport mobility  $\mu = 50,300 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ , measured at 3 K.

shape called a Hall bar to simplify the measurement. For a two-dimensional Hall bar with current flowing down the length  $L$  (with width  $W$ ) and a magnetic field perpendicular to both length and width, we can calculate the carrier density from the Hall resistance  $R_{xy}$  as

$$n_{2D} = \frac{1}{e} \left( \frac{R_{xy}}{B} \right)^{-1}. \quad (2.8)$$

Often, instead of using the scattering time  $\tau$  as a figure of merit for the quality of the 2DEG, the mobility  $\mu = e\tau/m^*$  is used. This mobility is effectively a measure of how easily electrons flow. Higher mobility means less scattering and lower resistance. Generally, higher mobility is desired. With a Hall bar, we can calculate this mobility through a measurement of the Hall resistance and the longitudinal resistance at zero magnetic field  $R_{xx}(B=0)$  as

$$\mu = \frac{L}{W} \frac{(R_{xy}/B)}{R_{xx}(B=0)}. \quad (2.9)$$

This mobility is called the *transport* mobility, as only scattering which negatively affects the current flow contributes to this value.

Figure 2.8 shows an optical image of a Hall bar (a) and a Hall measurement (b). A

standard Hall bar is nothing more than a field effect transistor (FET) with additional ohmic contacts for resistance probing. The Hall bar has six ohmic contacts consisting of a source and drain and four ohmics for measuring the Hall and longitudinal resistances. A single top gate accumulates electrons into a 2DEG which overlaps the ion implanted regions and the bar region. The top gate is isolated from the heterostructure by an oxide and a mesa etch creates a trench around the device to avoid stray current flow. The measured bar region lies in between the central four ohmics. In this device, the bar has a length/width ratio of 10. The magnetic field is applied perpendicular to the plane of the 2DEG, so that the Hall and longitudinal resistances are measured as labeled. In Fig. 2.8(b), these resistances are plotted as a function of applied magnetic field. As expected, the Hall resistance increases linearly with magnetic field. The behavior of the longitudinal resistance is not important presently, but will be discussed in Sec. 2.3.2.

As previously stated, these Hall bar measurements are used to measure the carrier density and mobility. These can be useful for determining the quality of the heterostructure grown, as defects lead to scattering. Generally, the mobility in the limit of high carrier density is dominated by impurities within or near the quantum well while the mobility in the low carrier density limit is dominated by remote impurities in the fabrication stack, *e.g.* within oxides. The minimum carrier density such that the disorder is overcome and finite current flows through the 2DEG is called the percolation density, corresponding to the metal-to-insulator transition [57]. The limits of low and high carrier density can be fit to separate power laws and used to interpret the sources of disorder affecting the 2DEG [58, 59]. In this work, the classical Hall effect is utilized in both Ch. 3 and Ch. 4 for characterization of heterostructure growth and device fabrication.

### 2.3.2 Quantum Hall Effect

In the previous section, we treated electrons in a 2DEG in a classical sense. However, particularly at low temperatures and with minimal scattering, these electrons should be

described quantum mechanically [11]. We start by replacing our electric and magnetic fields with the scalar potential  $\phi$  and the vector potential  $\mathbf{A}$ . We can then write the Schrödinger equation for charge  $q$  at position  $\mathbf{R}$  and time  $t$  in these potentials as

$$\left( \frac{1}{2m} [\hat{\mathbf{p}} - q\mathbf{A}(\mathbf{R}, t)]^2 + q\phi(\mathbf{R}, t) \right) \Psi(\mathbf{R}, t) = i\hbar \frac{d}{dt} \Psi(\mathbf{R}, t), \quad (2.10)$$

where  $\hat{\mathbf{p}}$  is the canonical momentum operator  $-i\hbar\nabla$ . If we introduce a magnetic field in the  $z$ -direction and choose a Landau gauge such that  $\mathbf{A} = (0, Bx, 0)$ , we arrive at

$$\left( -\frac{\hbar^2}{2m} \nabla^2 - \frac{ie\hbar Bx}{m} \frac{\partial}{\partial y} + \frac{(eBx)^2}{2m} + V(z) \right) \psi(\mathbf{R}) = E\psi(\mathbf{R}), \quad (2.11)$$

where  $V(z)$  is the confinement of the quantum well and  $E$  is the kinetic energy. Focusing on motion in the plane of the 2DEG, we can write the energy eigenvalues as

$$\epsilon = \left( n - \frac{1}{2} \right) \hbar\omega_c, \quad (2.12)$$

where  $n$  are positive integers and  $\omega_c = |eB/m|$  is the cyclotron frequency. Eq. (2.12) is familiar, as it has the form of the energy of a quantum harmonic oscillator.

This result turns out to be very consequential. We see that the allowed energies of the electrons are independent of their momentum. Therefore, states with the same  $n$  but different momentum  $k$  are degenerate. A 2DEG in the absence of a magnetic field has a continuous density of states out to its fermi level. In a magnetic field, however, this collapses to a series of delta functions called Landau levels.

The number of states per Landau level is determined by the electron density and the applied magnetic field. The allowed number of electrons per Landau level per area (density of states) is  $eB/h$  and the Landau levels fill up, starting with  $n = 1$ , until all electrons occupy a level. At larger magnetic field, these levels spread in energy and are allowed more electrons per level. The number of occupied Landau levels is called the filling factor  $\nu$ . This

is generally a continuous number but takes on integer values  $n$  at magnetic fields

$$B_n = \frac{\hbar n_{2D}}{n}. \quad (2.13)$$

These Landau levels can be interpreted as the allowed orbital energies of circular electron motion. In real silicon 2DEG systems, we have the added energy splittings associated with the Zeeman energy as well as the valley splitting. We can then approximate the energy eigenstates as

$$\epsilon = \left(n - \frac{1}{2}\right)\hbar\omega_c \pm \frac{1}{2}g\mu_B B \pm E_{valley}(B), \quad (2.14)$$

where  $g$  is the electron  $g$ -factor,  $\mu_B$  is the Bohr magneton, and  $E_{valley}$  is the valley splitting. We write the valley splitting as a function of magnetic field because with increasing magnetic field, the magnetic length (approximate orbit of the electron) decreases, leading to a smaller sampling of the quantum well interface. With this, there are now four Landau levels for each orbital. The condition for integer filling factor still applies to each of these new levels.

Although these Landau levels are theoretically degenerate delta functions with no width in energy, they will be broadened in real devices with finite scattering and temperature. The shape of the broadening is not precisely known, but is considered to be either Gaussian or Lorentzian in shape [60, 61]. For our calculations here, we assume a Gaussian broadening with magnitude  $\Gamma$ . We then rewrite the density of states as

$$g(E) = \frac{eB}{h} \sum_{n=1}^{\infty} \left[ \frac{1}{\sqrt{2\pi}\Gamma} \exp \left( -\frac{1}{2\Gamma^2} \left[ \epsilon - \left( \left(n - \frac{1}{2}\right)\hbar\omega_c \pm \frac{1}{2}g\mu_B B \pm E_{valley}(B) \right) \right]^2 \right) \right] \quad (2.15)$$

The Landau level broadening is approximately related to the quantum lifetime by  $\Gamma \approx \hbar/2\tau_q$  [59, 62]. The quantum lifetime,  $\tau_q$ , describes the time between scattering events. This differs from the transport lifetime in that all scattering events, not just those that adversely affect transport, are accounted for.

Figure 2.9(a) shows the first eight Landau levels for a 2DEG in silicon with a carrier

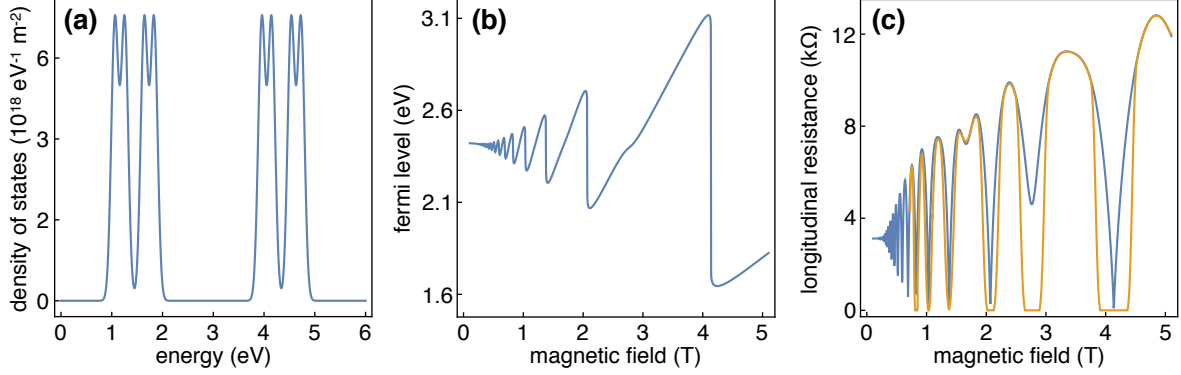


Figure 2.9: (a) Simulation of the density of states in a vertically confined 2DEG in a magnetic field  $B = 5$  T. The two widely separated groupings are separated Landau levels, further separated by the Zeeman splitting and the (much smaller) valley splitting. The broadening of these Landau levels is Gaussian. (b) A fan diagram of the fermi level for the system in (a) with a carrier density  $n_{2D} = 4 \times 10^{11} \text{ cm}^{-2}$ . The large vertical shifts are a results of the ‘pinning’ of the fermi level to a Landau level. (c) Longitudinal resistance of this simulation with a transport mobility  $\mu = 50,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  showing the expected Shubnikov-de Haas oscillations. The blue curve shows the results with no localized states while the orange curve is a rough approximation to include localization which results in wide regions of zero resistance.

density of  $n_{2D} = 4 \times 10^{11} \text{ cm}^{-2}$  at 5 T with an arbitrary Landau level broadening  $\Gamma = 70 \text{ } \mu\text{eV}$ . As the magnetic field increases, these states increase in energy and spread apart. The fermi energy passes through these Landau levels as the magnetic field changes. At integer filling factors, the fermi energy lies evenly between Landau levels. At sufficient separation of the Landau levels, the density of states at the fermi level, which is responsible for longitudinal conduction, approaches zero. In the limit that the transverse conduction is much larger than the longitudinal conduction, the longitudinal resistance is proportional to the longitudinal conduction. Therefore, at integer filling factors, the longitudinal resistance also approaches zero. This effect is dampened by the fact that as the density of states approaches zero, the change in fermi energy is rapid, resulting in a ‘pinning’ of the fermi level to the broadened Landau levels. This effect is shown in Fig. 2.9(b). As the magnetic field increases, higher Landau levels empty and the fermi level rapidly snaps to the next level. The fermi level here is calculated by integrating Eq. (2.15) to an energy  $\epsilon$  such that the electron density equals the total value  $4 \times 10^{11} \text{ cm}^{-2}$ .

To approximate the longitudinal resistance, we evaluate Eq. (2.15) at the fermi level and normalize the value to the classical value at  $B = 0$  for a mobility  $\mu = 50,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ . The result, shown in blue in Fig. 2.9(b), shows oscillations of the resistance with magnetic field. These are Shubnikov-de Haas oscillations and the minima occur at integer filling factors  $\nu$ . At larger magnetic field, these oscillations spread apart and increase in size.

The last effect we consider for this modeling is the distinction between localized and extended states. When the density of states is very small, the defects and impurities which contribute to electron scattering cause localization of the electron states. For finite conduction, the electron states must propagate along the length of the Hall bar, which these localized states cannot. Wide regions between the peaks of the Landau levels where the density of states is low exhibit this localization effect, leading to wide regions where the conduction, and therefore the resistance, is exactly zero. This effect is approximated in the orange curve of Fig. 2.9(c), where any density of states at the fermi level below a threshold is set to exactly zero.

Notably absent from this discussion is the effect of the lateral confinement of the Hall bar. This will introduce an additional confinement term to the Schrodinger equation and can be helpful to explain especially low magnetic field results. This confinement can also be helpful to describe the effect of edge states: conduction along the edges of the Hall bar. At the edges, the energies of the Landau levels rapidly increase and approach infinity (for an infinite well). This bending leads to an integer number of states along the edges, corresponding to the number of filled Landau levels. In the wide regions of zero resistance in the longitudinal resistance, only these edge states contribute to the Hall resistance. This leads to a quantization of the Hall resistance at integer filling factor. This effect is called the integer quantum Hall effect and the resistance at integer filling factor  $n$  is  $R_{xy} = h/(ne^2)$ .

Example longitudinal and Hall resistances in the quantum Hall regime are shown in Fig. 2.10(a). The Shubnikov-de Haas oscillations (SdHO) are clearly present and show wide plateaus of zero resistance at high field. The Hall resistance also shows wide plateaus at the

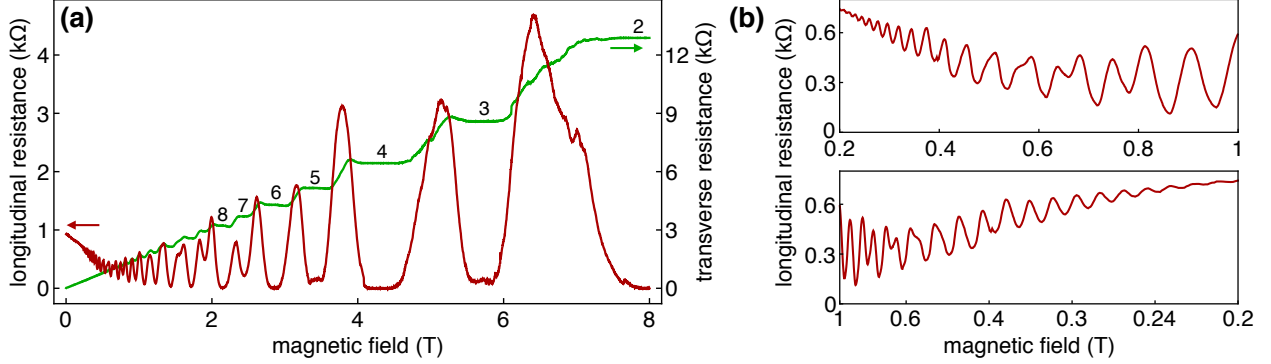


Figure 2.10: (a) Transverse (green) and longitudinal (red) resistances for a Hall bar measured below 100 mK ( $n_{2D} = 4.15 \times 10^{11} \text{ cm}^{-2}$ ,  $\mu = 160,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ). Strong quantum Hall plateaus and Shubnikov-de Haas oscillations are present. The integer filling factor  $\nu$  is labeled for select plateaus/minima. (b) Longitudinal resistance from (a), focusing on the low field region. The upper panel shows these SdHO plotted against linear magnetic field. The bottom panel shows the same, plotted in inverse magnetic field. The oscillations are evenly spaced in inverse magnetic field, with the onset of a doubling of the frequency at higher magnetic field as the Zeeman splitting increases beyond the level broadening.

same field as the SdHO minima. We can label the filling factors of these plateaus either from the resistance of the Hall plateaus or the carrier density calculated from the low field slope. Figure 2.10(b) shows a zoom-in of the low-field longitudinal resistance. We can see that as the field increases, an additional oscillation appears. This is the spin splitting increasing with increasing field, resulting in better separated Landau levels and creating deeper SdHO minima. If we plot this data in inverse magnetic field, shown in the bottom plot, these oscillations are evenly spaced and double in frequency as the spin splitting increases at higher field. This periodicity is just the filling factor equation Eq. (2.13). The periodicity of the oscillations in inverse field is another way to determine the carrier density of the system.

The quantum Hall effect is a very powerful phenomenon with many applications. For our purposes, it can be used to estimate the energy separation of these Landau levels, particularly the valley splitting. Additionally, the low-field behavior of the SdHO at varying temperature can be used to determine the quantum lifetime,  $\tau_q$ . The ratio  $\tau/\tau_q$  can be used to predict whether interface or remote scattering dominates the 2DEG behavior [59, 63]. In this work, the quantum Hall effect is utilized several times throughout Ch. 3.

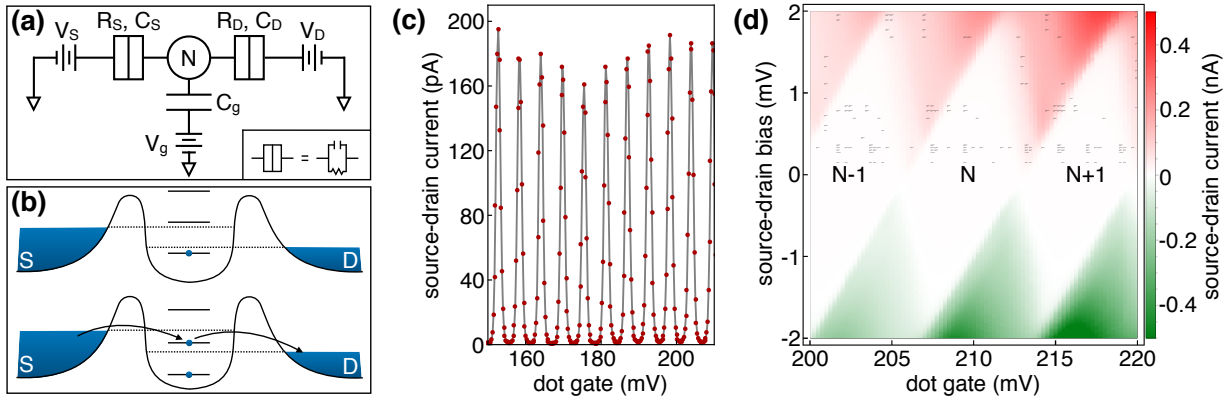


Figure 2.11: (a) Approximate circuit diagram for a single quantum dot coupled to a source reservoir, drain reservoir, and gate. The electrostatic energy of the quantum dot is influenced by these capacitances and the voltages applied. (b) Schematic of a changing chemical potential of a quantum dot between a source and drain. When no QD state lies in the bias window between the source and drain, no current flows (top). If the QD energy is modified to position a state in the bias window, electrons can shuttle between source and drain (bottom). (c) Example Coulomb blockade oscillations of a single quantum dot. The gray line connects the measured red points as a guide. (d) Coulomb diamonds of a single quantum dot. The stable regions of charge, where no current flows, are labeled with the relative number of electrons,  $N$ . Increasing the source-drain bias narrows these Coulomb blockade regions to form the diamond shape.

### 2.3.3 Coulomb Blockade

We now turn our attention to various quantum dot (QD) measurements. The simplest and most foundational of these is Coulomb blockade [17]. As previously discussed in Sec. 2.1.2, the energy of a quantum dot consists of the Coulomb repulsion of the electrons and the single-particle energy spacing between quantum levels (valleys, etc.). In well defined quantum dots, overcoming the Coulomb repulsion is the main energy requirement for adding additional electrons to the QD.

Figure 2.11(a) shows an approximate circuit diagram for a quantum dot coupled to a source reservoir, a drain reservoir, and an electrostatic gate. We can write the electrostatic energy of the quantum dot (ignoring single particle energies, spin energy, etc.) as a function of the charge  $Q$  on the dot

$$U(N) = \frac{Q^2}{2C}, \quad (2.16)$$

where  $C$  is the total capacitance of the dot,  $C = C_S + C_D + C_g$ . The charge  $Q$  of the dot encompasses the charge induced by the source, drain, and gate voltages, as well as the voltage of the dot itself. We can rewrite the charge as

$$Q = C_S V_S + C_D V_D + C_g V_g - C V_{dot}. \quad (2.17)$$

We rewrite the charge induced on the dot as  $C V_{dot} = eN$ , where  $e$  is the magnitude of fundamental charge and  $N$  is the number of electrons induced on the dot. The electrostatic energy of the dot becomes

$$U(N) = \frac{(-eN + C_S V_S + C_D V_D + C_g V_g)^2}{2C} = \frac{E_C}{2} (-N + q/e)^2, \quad (2.18)$$

where  $q = C_S V_S + C_D V_D + C_g V_g$  and  $E_C$  is the charging energy,  $E_C = e^2/C$ . We define the chemical potential of the dot as the energy required to add the  $N^{\text{th}}$  electron:

$$\mu(N) = U(N) - U(N - 1) = E_C(N - 1/2) - \frac{E_C}{e} q. \quad (2.19)$$

From this, we can see that the chemical potential of the dot is determined by the number of electrons on the dot, as well as the voltages and capacitances which make up  $q$ . The  $q$  term is continuous, but the occupation of the quantum dot,  $N$ , is discrete. Therefore, the chemical potential of the dot, while a continuous function, only results in a change in electron occupation at certain values of  $q$ .

The energy landscape of a quantum dot is shown schematically in Fig. 2.11(b). The quantum dot shown in the center has a series of well separated quantized energy levels (separated by  $E_C$ ). Source and drain 2DEG reservoirs on either side have a continuous density of states below their fermi level. The quantum dot is separated from these reservoirs by tunnel barriers on either side controlled by gate voltages. The energy of the quantum dot and these barriers can be tuned as desired. Figure 2.11(b) shows a source-drain bias: the

fermi level of the source and drain differ ( $V_S \neq V_D$ ). With sufficiently opaque barriers, this energy imbalance can be maintained when there is no available quantum dot state within this source-drain bias window. This is shown in the top schematic of Fig. 2.11(b) and is called Coulomb blockade. By changing the gate voltage over the QD and shifting the chemical potential of the dot, a QD state can be brought into this bias window and an electron can be shuttled from the source to the drain, as shown in the bottom schematic. For Coulomb blockade to be apparent, the temperature of the system must be lower than the charging energy of the dot and the tunnel resistances must be higher than the resistance quantum. In the limit of low tunnel rates, low temperature  $T$ , and large quantum dot energy splittings, the conductance  $G$  of a Coulomb blockade peak is given by [64]

$$\frac{G}{G_\infty} = \frac{\Delta E}{4k_B T} \cosh^{-2} \left( \frac{e(C_g/C)|V - V_0|}{2k_B T} \right), \quad (2.20)$$

where  $\Delta E$  is the internal energy splitting of the dot,  $C_g$  is the capacitance of the gate,  $C$  is the total capacitance of the dot, and  $V_0$  is the gate voltage at maximum resonant tunneling.

Figure 2.11(c) shows the source-drain current through a quantum dot as the dot gate voltage is swept. The current is highly nonlinear and oscillates between a high value and zero. These oscillations are called Coulomb blockade oscillations. Each peak corresponds to the addition (or subtraction) of an electron to the quantum dot. Each minimum corresponds to a stable number of electrons in the quantum dot as there are no available states for tunneling on or off. If we also sweep the source-drain bias, as done in Fig. 2.11(d), we see what are called Coulomb diamonds [12]. The large white diamonds of zero current are the stable regions of quantized dot occupation  $N$ . As the source-drain bias is increased from zero, the region of finite current flow widens. At negative bias, electrons are shuttled in the opposite direction and the current flow reverses. The angles and size of these diamonds are determined by the capacitances to the source and drain, the asymmetry of the source-drain bias, the charging energy of the dot, and the capacitance between the gate and the dot. The charging

energy of the dot can be easily determined by the source-drain bias at which the diamonds of finite current intersect. For this measurement, the charging energy is around 2 meV. The structure of the current flow within the finite current diamonds is due to the internal energy spacings of quantum dot. As the source-drain bias increases, additional excited state energy levels such as an excited valley or orbital state can contribute to the conductance and the current increases. With precise measurement, these Coulomb diamonds can be used to measure the excited state energy spectrum in a quantum dot [65].

### 2.3.4 Charge Sensing

In quantum dot qubits, knowing the electron occupation of the quantum dots is vital. For charge qubits, the occupation of the dot determines the qubit state. For qubits which utilize spin, ‘spin-to-charge conversion’ is used to map the spin state to a specific charge state [36,66]. Therefore, having a way to externally sense the charge occupation of a quantum dot is essential. ‘Charge sensing’ is a catch-all term for many different techniques to sense absolute or relative dot occupation. Here, we focus on perhaps the most straightforward approach of a nearby QPC or QD charge sensor [67].

The energy of a quantum dot is very sensitive to nearby electrostatic changes. Near a Coulomb blockade peak, small changes to gate voltages or nearby charges can significantly affect the current through the dot. We can use this high sensitivity to our advantage as a sensor of other quantum dots. Figure 2.12(a) shows the current through a quantum dot as the gate voltage of a separate and independent dot that we want to sense is swept. There are two effects to be noted. Most obviously, there are abrupt changes to the current about every 40 mV. These large shifts in current are due to a changing occupation of the sensed dot. With increasing voltage, each shift corresponds to an electron being added to the dot. The Coulomb blockade peak position shifts due to this change in the nearby electrostatic environment. The second effect to be noted is the overall slope in current between charge transitions. This is due to the voltage change on the sensed dot gate. This effect is much

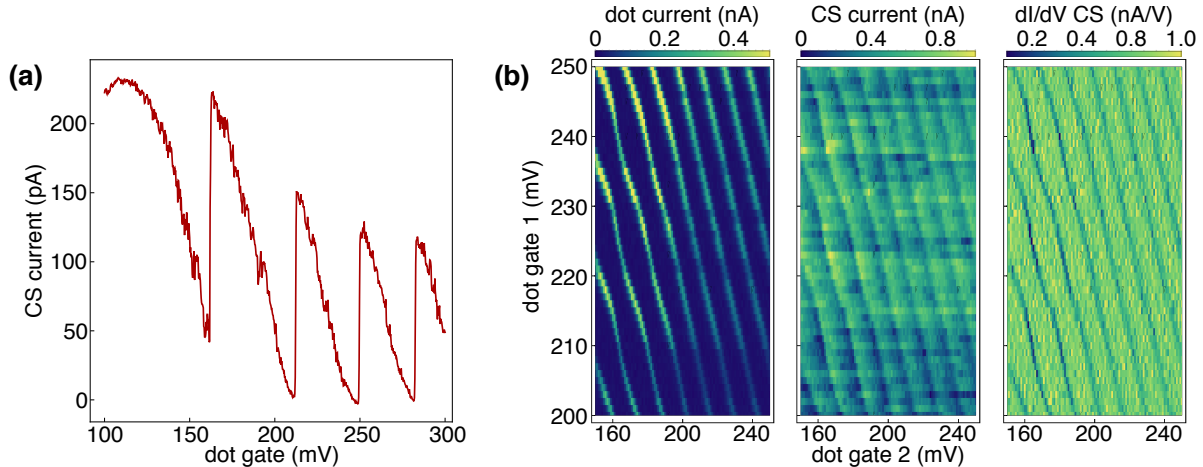


Figure 2.12: (a) Example current through a charge sensor quantum dot as the sensed dot gate voltage is swept. The abrupt changes in current are a result of the changing electron occupation of the nearby dot. (b) Two-dimensional charge sensing of a quantum dot. The left panel shows Coulomb blockade oscillations of the transport current through the sensed quantum dot as two dot gate voltages are swept to create a  $2D$  image. The center panel shows the current through the charge sensor, with abrupt changes at the charge transitions. The right panel shows the numerical differentiation of the charge sensor signal with respect to dot gate 2, showing peaks at the charge transitions.

smaller, leading to the gradual shift in the charge sensor current.

This charge sensing technique can be quite useful. Figure 2.12(b) shows electron transitions of a quantum dot through changes to two gates. The left panel shows the direct transport current through the dot. The voltage at which electrons are added to the dot appear as Coulomb blockade peaks. In the central panel the current through a nearby charge sensor feels the effect of these electron transitions, resulting in shifts at these voltages. In the right panel, a derivative of the charge sensor results in peaks at the charge transitions like those in direct transport. Often at very low dot occupations, maintaining a large enough tunnel rate for a detectable transport current is difficult. Charge sensing in this way removes the need for particularly fast tunnel rates which are often detrimental for qubit use.

This charge sensing technique is not limited to measuring the changing occupation of a single quantum dot. Coupled quantum dot systems can be measured with a single charge sensor, and the differing distance between the charge sensor and the sensed dot results in a

differing response, which can be used to determine the location of each dot. A charge sensed double quantum dot system is shown later in Sec. 2.3.7.

### 2.3.5 Lever Arm Measurement

The energies of quantum dots are experimentally manipulated with voltages on surface gates. Knowing those explicit energies, however, is often very important for spectroscopy and qubit manipulation. For this reason, we need a conversion between the gate voltage and the energy of the dot. The conversion factor between a gate and the energy of a quantum dot is called a lever arm,  $\alpha$ . The lever arm is a measure of the capacitance between the gate and the dot, determined by the gate geometry and the location and shape of the dot. There are many ways to measure this value. In transport, the lever arm can be calculated from a Coulomb diamond as its width (gate voltage) divided by half its height (source-drain bias). However, in the low electron regime for qubits, we must rely on charge sensing methods and we focus on a thermal-based method here.

Figure 2.13(a) shows a charge sensed electron transition. Adapted from Ref. [64] and Ref. [68], we can fit the charge sensor current with

$$I_{CS}(V) = A \tanh\left(\frac{\alpha(V - V_0)}{2k_B T_e}\right) + b * V + I_0, \quad (2.21)$$

where the last two terms adjust for a current offset and the cross capacitance of the gate voltage. As written, the width of the charge sensor transition is dependent on both the lever arm  $\alpha$  and the electron temperature  $T_e$ . This is a measure of the temperature of the electron reservoir, as the quantum dot has no defined temperature. Therefore, if we can control and measure the electron temperature, we can determine the lever arm.

Figure 2.13(b) shows the same charge sensed transition as (a), but at an elevated temperature. The transition is clearly broadened significantly by this change. The temperature in the system is changed by heating the mixing chamber of the dilution refrigerator in which

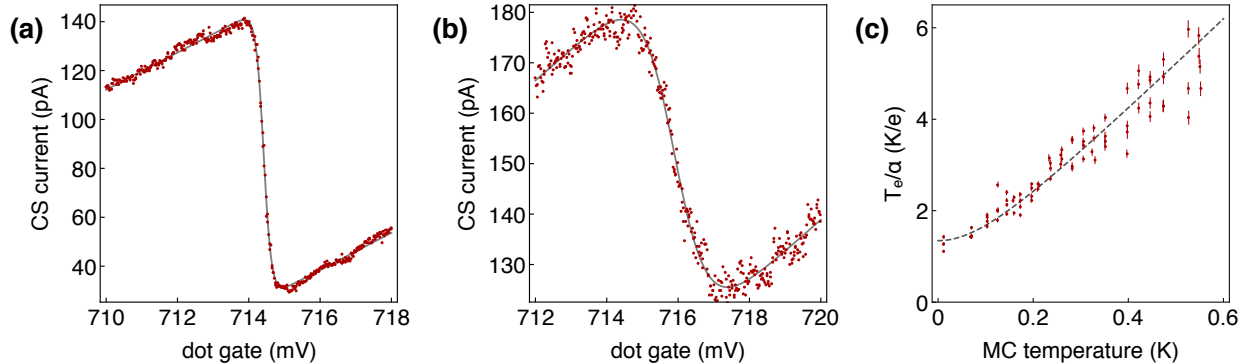


Figure 2.13: Charge sensed transition of a quantum dot at a fridge temperature of 12 mK. (b) Charge sensed transition of the same quantum dot in (a) at a fridge temperature of 550 mK. The gray curves in (a-b) are fits to the data using Eq. (2.21). (c) Lever arm and electron temperature fit of a thermally broadened charge sensed electron transition. The extracted lever arm is  $\alpha = 0.99$  eV/V and the base electron temperature is  $T_{e0} = 133$  mK.

the device is loaded. The transition in both (a) and (b) can be fit with Eq. (2.21) to extract a single  $T_e/\alpha$  parameter for each curve. This parameter is plotted in Fig. 2.13(c) as a function of the mixing chamber temperature. As the lever arm should stay fixed across temperature, the parameter  $T_e/\alpha$  increases with increasing fridge temperature. At very low temperatures, it plateaus. This is due to the electron temperature de-coupling from the fridge temperature. The 2DEG experiences some heating from electrical and thermal noise of the device wiring. Because the electron-phonon coupling in silicon is relatively weak, the electrons cannot fully thermalize to the fridge at very low temperatures. At higher fridge temperatures, this effect is diminished and the electron temperature is in equilibrium with the fridge temperature. We fit the electron temperature  $T_e$  phenomenologically with

$$\frac{T_e}{\alpha} = \frac{1}{\alpha} \sqrt{T_{MC}^2 + T_{e0}^2}, \quad (2.22)$$

where  $T_{MC}$  is the mixing chamber temperature and  $T_{e0}$  is the electron temperature at  $T_{MC} = 0$ . Fitting the data in Fig. 2.13(c) with this function, we can now extract a lever arm and a base electron temperature. This lever arm can then be used to convert gate voltage changes into changes in the chemical potential of the dot.

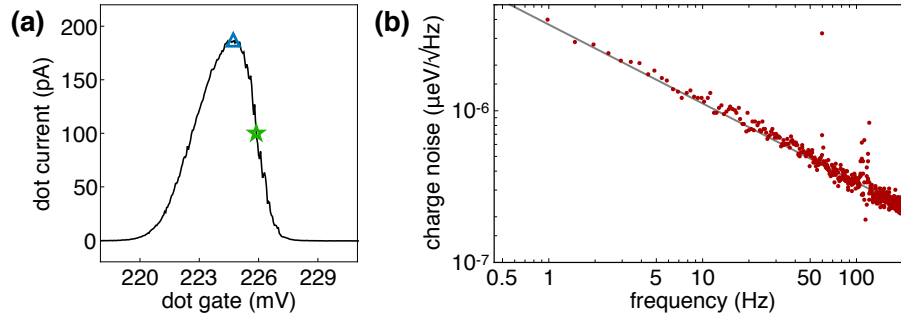


Figure 2.14: (a) Coulomb blockade peak of a single quantum dot with labeled sensitive (green star) and insensitive (blue triangle) points for measurement. (b) Charge noise curve of the dot peak in (a), showing a  $1/f$  like dependency (gray line). The current power spectrum of the insensitive peak is subtracted from the sensitive point before conversion to the charge noise. The stray points near 60 and 120 Hz are environmental noise.

### 2.3.6 Low-frequency Noise Characterization

Noise is a near universal inhibitor to larger and better performing qubit devices of all designs. In quantum dot based qubits, electrical noise called charge noise can be the dominant noise source. Electrostatic fluctuations of the environment surrounding QDs can arise from many sources, but are mainly attributed to two-level-system (TLS) defects at material interfaces or within dielectrics [69–71]. This charge noise can affect the energy, shape, and position of quantum dots. For silicon qubits, charge noise can often be the most significant limit to higher fidelities [42, 72]. For charge noise characterization, there is a relatively simple and quick measurement that can be performed on a single quantum dot coupled to a source and drain [69, 73]. The power spectrum of the current through a Coulomb blockade peak is measured and converted into a charge noise spectrum. This is performed as follows.

First, a Coulomb blockade peak is tuned to have a large (dot current)/(gate voltage) slope. To measure the charge noise that impacts the chemical potential of a quantum dot, we operate at a point where the measured signal, the current, is sensitive to changes in the chemical potential. The dot gate voltage is set to the highly sloped side of a Coulomb blockade peak, as shown in Fig. 2.14(a), indicated by the green star. The power spectral density (PSD) of the current,  $S_I(f)$ , is acquired in a long time-trace at this voltage point.

This measurement captures the chemical potential noise in the device which affects the current, but also captures bias voltage noise as well as noise from any current or voltage pre-amplifiers in the circuit. We therefore need to subtract out these external noise sources. This can be done by subtracting the noise at a point which is insensitive to the chemical potential noise we are interested in. A good choice for this insensitive point is the peak of the Coulomb blockade curve, marked in Fig. 2.14(a) by the blue triangle. In an ideal case, the slope at the insensitive point is exactly zero. Subtracting a current PSD at a point with finite slope is a major source of error in this approach.

This current PSD is then converted to a measure of the charge noise in the device. This is done with a measure of both the lever arm,  $\alpha$ , and the slope at the sensitive point to convert to a PSD of the chemical potential  $\mu$ .

$$S_\mu(f) = \alpha^2 \left| \frac{dI}{dV_{gate}} \right|^{-2} S_I(f) \quad (2.23)$$

This has units of energy<sup>2</sup>/frequency and represents the charge noise at the dot in terms of the change in chemical potential. The total integrated charge noise,  $\sigma_\epsilon$ , which is often reported for qubit measurements, can be attained by taking a square root and integrating over the bandwidth of the measurement [74]. Figure 2.14(b) shows an example charge noise result. Charge noise in silicon quantum dots typically shows a  $1/f$  dependence, as highlighted by the  $1/f$  gray line in Fig. 2.14(b). The value at 1 Hz is often reported as a standard metric. In the field of gate defined silicon quantum dots, the lowest charge noise measured lies in the  $0.1 - 1 \mu\text{eV Hz}^{-1/2}$  range [44].

While this measurement is performed in a lower frequency range than most qubits are operated, the magnitude and power law of the noise has been shown to track up through the megahertz range [42, 75]. This measurement can then be remarkably powerful as a predictor of the noise spectrum of a quantum dot qubit, despite its relative ease. A separate, but related, method of charge noise measurement involves tracking the peak location of a Coulomb

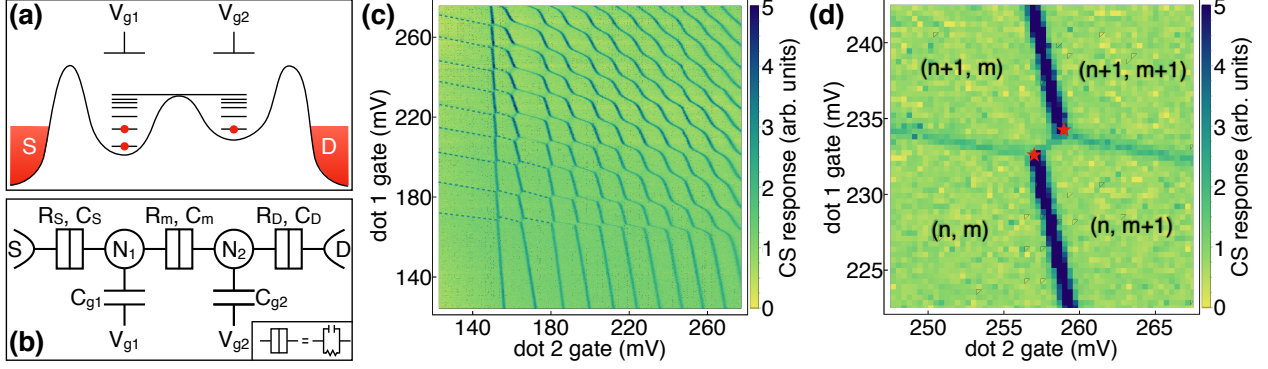


Figure 2.15: (a) Schematic of the energies of a double quantum dot system. The left dot is coupled to the source reservoir and the right dot is coupled to the drain reservoir. The dot occupation is controlled by gate voltages  $V_{g1}$  and  $V_{g2}$ . (b) Approximate circuit diagram for the double quantum dot system shown in (a). Not shown is the cross capacitance between gate 1 and dot 2, and gate 2 and dot 1. (c) Large stability diagram of a charge sensed double quantum dot. The slopes of the transition lines give insight into the relative positions of the electrons. There is a smooth transition from a single central dot in the upper right to a coupled double dot in the lower left. Some transitions associated with dot gate 1 are difficult to see, due to charge sensor insensitivity in that region. Added dashed lines highlight the transitions in these insensitive regions. (d) A stability diagram, focused on a single polarization line in a double dot regime. The dot occupation of the double dot system is labeled as  $(N_1 = n, N_2 = m)$ . The triple points are labeled with red stars. The short transition line between the triple points is called the polarization line. Changes in voltage across this line result in moving an electron from one dot to the other.

blockade peak in time. This is used to measure charge noise at lower frequencies [27].

### 2.3.7 The Charge Stability Diagram

In this work so far, we have focused on a single quantum dot, or a quantum dot and a sensing dot which do not exchange electrons. We now discuss a double quantum dot system, in which a secondary quantum dot is added to the same current channel so that electrons can be exchanged between each dot [76].

This is shown schematically in Fig. 2.15(a), where each dot is coupled to a single reservoir and the energy of each dot can be individually controlled by gate voltages  $V_{g1}$  and  $V_{g2}$ . Figure 2.15(b) shows an approximate circuit diagram for this double quantum dot system. The electron occupation of each dot is affected by the coupling to the source, drain, and

each other, as well as the voltages on the gates. For brevity, we simply refer to Ref. [76] for a detailed derivation of the chemical potential of each dot. We instead focus here on a qualitative description.

Figure 2.15(c) show a ‘stability diagram’ of a double quantum dot system measured with a charge sensor. The current through the charge sensor is measured with a lock-in referenced to a small oscillating voltage applied to dot gate 2. The signal is maximum at charge transitions, an effective differentiation of a DC charge sensor measurement. This stability diagram shows 5 different regions of the charge transition behavior. The relative slopes of the charge transitions with respect to each dot gate gives insight into the relative location of the dots.

Starting with the upper right of the figure, where both dot gate voltages are high, we see roughly  $45^\circ$  lines. Here, the coupling between the two dots is very high (large  $C_m$ ). We effectively have one single large dot, positioned roughly between the two dot gates. As we lower both gate voltages, these transition lines change and begin to form sets of horizontal and vertical lines. In this regime, we now have two coupled but distinct quantum dots. At very low voltages, no more transition lines are present, and both dots are empty. On the left and bottom edges of the figure, we see transitions associated with only a single dot, as the other dot has been fully emptied.

We now focus in on the double-dot region of this stability diagram. Figure 2.15(d) shows a zoomed in look at a single transition of each dot. The relative occupation of each dot is labeled as  $(N_1 = n, N_2 = m)$ . As expected, increasing the voltage on each gate adds an electron to that dot. However, because these dots are nearby and so are the gates which control their occupation, there is a cross capacitance between gate 1 and dot 2, as well as gate 2 and dot 1. This leads to the finite slope of these transitions, *i.e.*, changing gate 1 affects the energy of dot 2 and vice versa. We also see that the addition of an electron in one dot affects the charge transition of the other dot. Because these dots are capacitively coupled together, the energy of one dot changes the energy of the other. This leads to a separation of

the intersection between the charge transitions for each dot (labeled with red stars). These points are called triple points, and the line between them is called the polarization line. The stable regions of charge across the polarization line show an extra electron in either dot. Therefore, changing the gate voltages to cross the polarization line corresponds to moving an electron from one dot to the other. The presence of the polarization line shows that electrons can be exchanged between the dots. As a final note, we comment that as the inter-dot coupling increases, the curvature at the triple points increases, as can be seen in higher voltage ranges in Fig. 2.15(c).

Creating multi-dot systems is crucial for most quantum dot computing schemes. Double quantum dots are necessary for systems such as the charge qubit, singlet-triplet qubit, or quantum-dot-hybrid qubit [34,37,77]. Triple quantum dots, in which there are three coupled dots, are used for the exchange-only qubit and the charge quadrupole qubit [78,79]. For single spin qubits which only need a single dot, two qubit gates based on the exchange coupling between the electrons requires a double dot system [80]. Thus, as shown in Sec. 2.2.2, most quantum dot devices are designed to host multiple dots.

### 2.3.8 Magnetospectroscopy

As discussed previously in Sec. 2.1.2-2.1.3, electrons in a quantum dot occupy discrete energy levels. With a single electron in a quantum dot, the atomic-orbital-like energy levels are further split by the valley splitting. At zero-magnetic-field, each level is doubly-degenerate due to the two possible spin states. As additional electrons are added, the charge repulsion of the electrons modifies the energy separation between these levels. These electron-electron interactions can cause significant deviations from the single-particle energy splittings, as shown in Ref. [81]. When measuring the energy splittings of multi-electron quantum dots, it is important to keep the influence of electron-electron interactions in mind.

One method of measuring the energy spectrum of a multi-electron quantum dot is magnetospectroscopy [21,82–84]. By introducing an in-plane magnetic field, the ground spin state

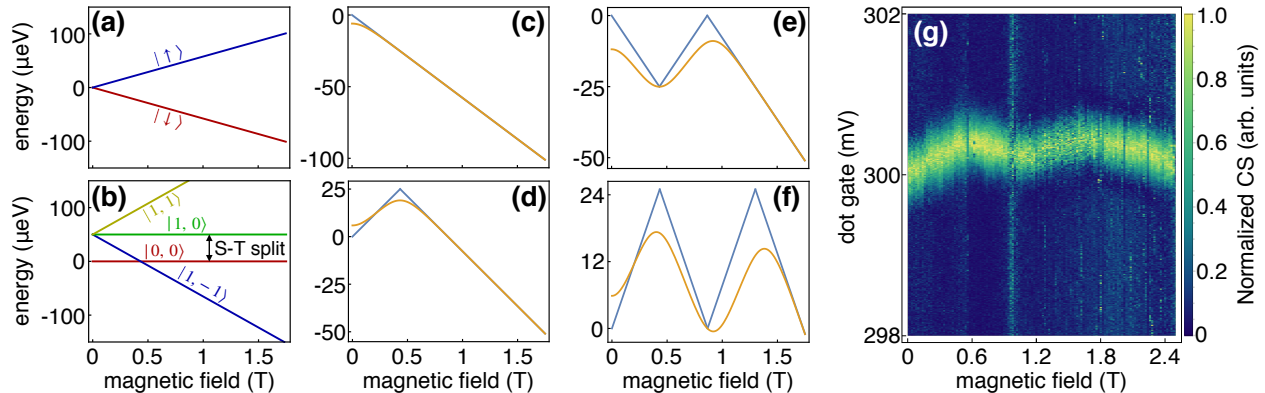


Figure 2.16: (a) Spin states of a single electron quantum dot as a function of magnetic field. At increasing magnetic field, the spin down state lowers in energy while the spin up state increases. (b) Spin states of a two electron quantum dot. At low magnetic field, the singlet state is the lowest energy state. As the field increases, the  $T_-$  state becomes the lowest energy state at a field determined by the singlet-triplet splitting. (c-f) Magnetospectroscopy curves for the 0-1, 1-2, 2-3, and 3-4 electron transitions, respectively. The blue curves show the result for simply subtracting the lowest energy spin state of the lesser electron occupation from the lowest energy spin state of the greater electron occupation. The orange curves show a more accurate model, allowing for excited state occupation due to a finite electron temperature (100 mK) and taking into account the multiplicity of each spin state. (g) Example magnetospectroscopy curve of a 3-4 electron transition, showing the characteristic ‘M’ shape of the curve. The charge sensor (CS) is measured via a lock-in, so that the peak signal corresponds to the electron transition. The data at each magnetic field step is normalized for visibility.

of the quantum dot can be changed. The changes in the ground state are detected through the changing energy, and therefore gate voltage, of an electron transition as the magnetic field is swept.

We first consider the case of a single electron in a quantum dot. At zero-magnetic-field, the electron occupies the lowest possible valley-orbit state and either spin state. As the magnetic field  $B$  increases, the spin states are split by the Zeeman energy,  $E_Z = m_s g \mu_B B$ , where  $m_s$  is the spin projection along the magnetic field,  $g$  is the electron  $g$ -factor ( $\approx 2$  for silicon), and  $\mu_B$  is the Bohr magneton. Thus, at finite magnetic field, the spin down state becomes the lowest energy state available. This is shown schematically in Fig. 2.16(a). At increasing magnetic field, the energy of down state continues to decrease. Therefore, if the electron transition between 0 and 1 electrons is swept, the voltage at which the electron is

added decreases as the magnetic field increases. The rate at which this occurs (the slope of energy/field) is determined by the difference in Zeeman energy between the two occupations. This is shown in Fig. 2.16(c) as the blue line.

We now consider the electron transition from 1 to 2 electrons. The spin states of a two electron system are shown in Fig. 2.16(b), labeled by the total spin and projection,  $|S, m_s\rangle$ . At zero-magnetic-field, the singlet state  $|0, 0\rangle = \frac{1}{\sqrt{2}}(|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle)$  is the lowest energy state. Due to the asymmetry of the spin state, both electrons can occupy the lowest energy valley-orbit state. For the triplet states where  $S = 1$ , one electron must occupy a higher valley-orbit state, increasing the total energy of the dot. As shown in Fig. 2.16(b), the triplet states are offset from the singlet state by the singlet-triplet splitting. In silicon quantum dots, the lowest excited state to occupy is often the first excited valley state, so the singlet-triplet splitting is approximately equal to the valley splitting (electron-electron interactions result in  $E_{S-T} < E_{valley}$ ). At sufficient magnetic field, the  $T_-$  state,  $|1, -1\rangle$ , becomes the lowest lying spin state. As previously stated, the slope of the electron transition with magnetic field is determined by the difference in Zeeman energies between the two electron occupations  $m_s(N+1) - m_s(N)$ . At low field, the ground state of the 2 electron system does not change with magnetic field, but the 1 electron state decreases. This results in an increasing slope of the charge transition. However, once the  $T_-$  state becomes the ground spin state for 2 electrons, the transition slopes downwards in energy. This ‘kink’ in the magnetospectroscopy slope for the 1-2 electron transition is shown in blue in Fig. 2.16(d). Given the known charge occupation and Zeeman energy of each spin state, the singlet-triplet splitting can be extracted from the magnetic field of the magnetospectroscopy kink. This process can be repeated at higher electron transitions, with an increasing number of kinks associated with additional changes to the spin states of each electron occupation across the transition. Figure 2.16(e-f) show these magnetospectroscopy curves for the 2-3 and 3-4 electron transitions.

This discussion holds true at zero temperature. However, finite temperatures allow for thermal excitations into higher spin or valley-orbit states, which modifies these magnetospec-

troscopy curves. A grand canonical ensemble approach, in which both energy and electrons can be exchanged between a quantum dot and a finite-temperature reservoir, can be used to more accurately determine the zero-magnetic-field excited spin states of any electron occupation. This approach is described in detail in Sec. 3.2.8. The consequences of thermal excitations are shown in Fig. 2.16(c-f) by the orange lines. Setting the electron temperature to 100 mK results in curvature at the kinks and displacement of their magnetic field location.

An experimental example of magnetospectroscopy at the 3-4 electron transition is shown in Fig. 2.16(g). The ‘M’ shape, as shown in Fig. 2.16(f), is clearly visible. Magnetospectroscopy can be used as an effective tool for obtaining the zero-magnetic-field excited spin states, such as the singlet triplet splitting. For negligible electron-electron interactions, these excited spin states can be interpreted as the single-particle valley-orbit states. This limit can be achieved in very tightly confined quantum dots, but generally the results extrapolated are only lower bounds due to e-e interactions [29]. The magnetospectroscopy slope far away from spin flips can also be used as a method to extract the gate-to-dot lever arm, if the  $g$ -factor is already known. Magnetospectroscopy is used here in Sec. 3.2.

### 2.3.9 Pulsed-Gate Spectroscopy

Pulsed-gate spectroscopy is another method of measuring the excited states of a quantum dot which does not require a magnetic field [21, 29, 52, 85–89]. In pulsed-gate spectroscopy, a square wave voltage is applied to the quantum dot gate. The frequency of the square wave is chosen to be similar to the tunnel rate of the resonant electron transition. With this applied pulse train, the electron is loaded on and off the dot repeatedly. Figure 2.17(a) shows a single energy level split by the energy of the pulse,  $E_{pulse}$ . The electron loads into the dot with loading rate  $\Gamma_g$  when the loading side of the pulse (solid line) dips below the fermi level of the reservoir. The electron unloads from the dot when the unloading side of the pulse (dotted line) rises above the fermi level (see Fig. 2.17(c)). If the amplitude of the pulse is sufficiently large, the electron can also be loaded into excited states of the quantum dot with

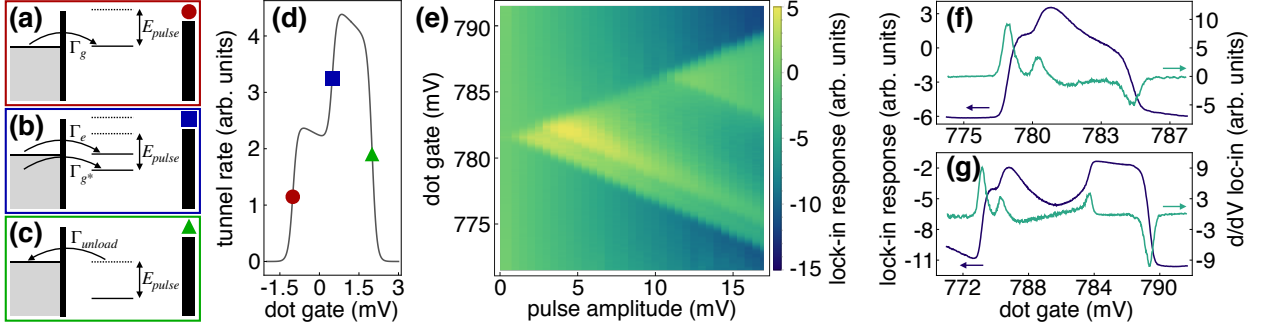


Figure 2.17: (a-c) Schematics of the loading and unloading of an electron into a quantum dot from an electron reservoir with an applied square pulse  $E_{pulse}$ . The solid lines represent the ‘loading’ energy of the pulse while the dotted lines represent the ‘unloading’ energy of the pulse. In (a), when the loading energy matches the fermi level of the reservoir, the dot is loaded at a tunnel rate  $\Gamma_g$ . In (b), at a lower dot energy, an additional excited state can be loaded in with tunnel rate  $\Gamma_e$  while the ground state loading rate is modified due to energy dependent tunneling effects. In (c), the electron unloads when the unloading energy matches the fermi level of the reservoir. (d) Schematic of the tunnel rate for a dot with two accessible energy states. The colored markers are associated with those in (a-c). (e) Example pulsed gate spectroscopy as a function of dot gate voltage and pulse amplitude. As the pulse amplitude is increased, additional excited states are visible as downward sloping lines. (f-g) Highly averaged vertical line-cuts (blue) of (e) at 8 mV and 16 mV, respectively. The green curves show a numerical differentiation of these curves, resulting in peaks at the loading energies for each state.

loading rate  $\Gamma_e$ , shown in Fig. 2.17(b). The off-resonant loading rate into the ground state is generally reduced due to energy depending tunneling effects. The addition of the excited state results in an abrupt change in the total tunnel rate into the dot. Figure 2.17(d) shows a schematic of the changing tunnel rate between a dot and a reservoir for a dot with two energy states separated in voltage space by 1.5 mV and a pulse amplitude of 3 mV. The abrupt changes in tunnel rate are thermally broadened and referenced back to Fig. 2.17(a-c) by the colored shapes. The energy separation between these changes in the loading rate is the energy splitting between those states.

To measure the effect of pulsed-gate spectroscopy, there are several approaches. The DC (long time averaged) current of a nearby charge sensor can be used to detect the fractional change in average electron occupation as additional energy states become accessible. Alternatively, an AC lock-in measurement can be performed. Here, we present a ‘low-frequency’

AC lock-in measurement, in which the charge sensor current is measured by a lock-in that is referenced to the fundamental frequency of the square wave. When measured in this way, a large lock-in response is measured when the charge sensor, which is sensitive to the dot, oscillates with the same frequency as the applied pulse. In the limit that the tunnel rate of the ground state  $\Gamma_g$  is much larger than the pulse frequency, the electron will load into the dot during every pulse cycle. Adding additional loading states at higher pulse amplitude will not change the charge sensor response, as the electron is already loaded 100% of the time. However, if  $\Gamma_g$  is similar to or somewhat lower than the pulse frequency, the electron will load during the loading pulse time for only a fraction of the pulse cycles. Adding additional excited states by increasing the pulse amplitude or changing the DC voltage will increase the total tunnel rate into the dot and change the lock-in response. With this measurement technique, the lock-in response maps out the changing tunnel rate of the electron into the dot. This is the fundamental process for any pulsed-gate spectroscopy method. The tunnel rates into the dot should be similar to the pulse frequency such that adding additional loading states significantly alters the measured response.

Figure 2.17(e) shows a pulsed-gate spectroscopy scan of the 0-1 electron transition as a function of both pulse amplitude and DC voltage on the dot gate. We see a ‘V’ shape opening up from the resonant tunneling voltage at zero pulse amplitude. The bottom of this V is the ground state loading line and the top of the V is the unloading line. Within the V shape, the electron spends a fraction of the time in the quantum dot, on average. Below, the electron is always unloaded. Above, the electron is always loaded. As the pulse amplitude increases, additional loading lines appear and trend downwards with the ground state loading line. For the 0-1 electron transition, the first excited loading line is the valley splitting and the second excited loading line, at much higher amplitude, is the orbital splitting. On this plot, the vertical separation between these excited loading lines and the ground loading line is the energy splitting in gate voltage space. Multiplying by the gate-to-dot lever arm converts this into an energy splitting.

Figures 2.17(f) and (g) show vertical line-cuts of Fig. 2.17(e) at 8 and 16 mV, respectively. The blue curves show the raw lock-in response of this low-frequency pulsed-gate spectroscopy method. Large changes in the lock-in response correspond to large changes in the tunnel rate, or average electron occupation. Taking a numerical derivative, shown in green, these abrupt changes become peaks. This can then be fit to extract the separation between the peaks, and therefore the energy splittings of the dot. The fits are based on a phenomenological estimation for the average occupation of the dot,  $\langle n \rangle$ , described in Ref. [29] as

$$\langle n \rangle = \sum_i \Gamma_i \frac{e^{(E_i - E_F)/E_{0i}}}{e^{(E_i - E_F)/k_B T} + 1}, \quad (2.24)$$

where the sum is over the available energy states,  $E_i$  is the energy of the  $i^{\text{th}}$  state,  $E_F$  is the fermi energy of the reservoir,  $k_B T$  is the temperature of the system, and  $E_{0i}$  and  $\Gamma_i$  are fitting parameters for each state. The differentiated signal of the low-frequency pulsed-gate spectroscopy measurement can be considered a derivative of the average occupation:  $d\langle n \rangle/dV$ . Substituting  $\alpha V_i$  for  $E_i$  and  $\alpha V$  for  $E_F$ , where  $\alpha$  is the lever arm and  $V$  is the gate voltage, we can take the voltage derivative of Eq. (2.24) to arrive at a fitting function for multiple peaks in the pulse-spec data. The extracted voltage splittings are then the separation of the voltages  $V_i$  in the fit.

Pulsed-gate spectroscopy can be a powerful tool because it can be used to measure single electron energy splittings, unlike magnetospectroscopy. This method is used extensively in Sec. 3.4 to measure the valley and orbital splitting of a single-electron quantum dot. However, the need to independently measure the lever arm of the gate can introduce additional error to the fits. Pulsed-gate spectroscopy can also be used to measure the spin splitting in a quantum dot if a magnetic field is applied. This is used in Sec. 3.2 to measure the electron g-factor. Pulsed-gate spectroscopy and magnetospectroscopy can be used in concert to confirm each others results, as done in Ref. [29].

## Chapter 3

# Valley Splitting Control Through Heterostructure Modifications

In this chapter, we explore modifications to the Si/SiGe heterostructure with the intent to control and increase the valley splitting in quantum dots. As discussed in Sec. 2.1.3, the valley splitting in a silicon quantum well is fundamentally a microscopic phenomenon, dependent on the exact details of the heterostructure interfaces and the shape and position of the wave function. Here, we present three separate approaches which modify the heterostructure interface or germanium concentration within the well.

### 3.1 Intentional Mis-Cut of the Heterostructure for Valley Splitting Enhancement

#### 3.1.1 Introduction to Mis-Cut Heterostructures

Growth of a Si/SiGe heterostructure, whether through chemical vapor deposition (CVD) or molecular beam epitaxy (MBE), typically starts with a silicon wafer. Silicon wafers are usually sliced and polished so that the surface is normal to a high symmetry lattice plane. For strained silicon wells, the surface is normal to the (001) plane. Realistically, the

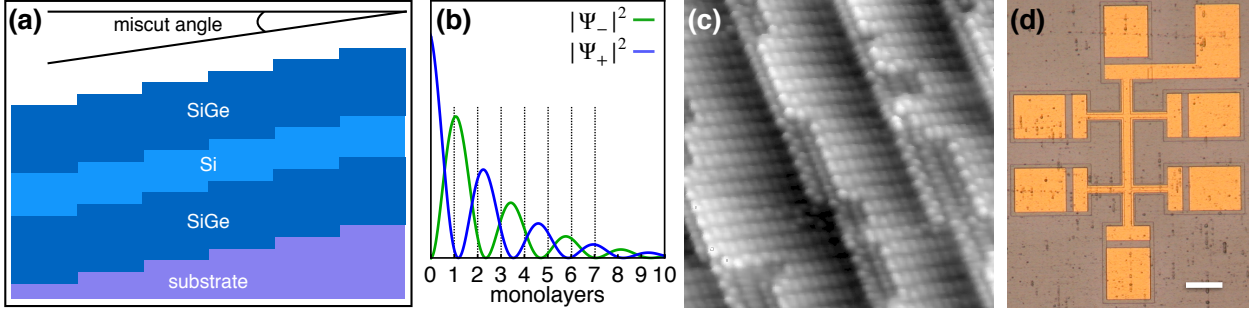


Figure 3.1: (a) Schematic of a mis-cut heterostructure. When the surface of a silicon substrate is mis-aligned to the crystallographic axes, atomic steps will be present on the surface. These atomic steps will transfer to the heterostructure grown on the substrate, resulting in regular atomic steps at the quantum well interface. (b) Wave function densities of the valley states in the SiGe barrier (interface at zero). The separation between mono-atomic-layers is shown with dashed lines. Shifting the wave functions by one monolayer results in a nearly  $\pi$  phase shift. (c) Scanning tunneling microscope (STM) image of a silicon surface miscut by  $4^\circ$  along the  $[110]$  axis, showing double-atomic steps  $[90]$ . (d) Optical image of an example Hall bar fabricated on a mis-cut heterostructure, with a  $100 \mu\text{m}$  scale bar.

surface will never be perfectly aligned to a lattice plane. This results in atomic steps on the surface. These atomic steps will persist throughout the heterostructure growth, such that each interface (like the quantum well interfaces) also exhibits atomic steps. This is shown schematically in Fig. 3.1(a). The density of atomic steps is determined by the angle and direction of the mis-cut, although additional steps and disorder are introduced during heterostructure growth. Typically, a nominally flat silicon wafer will have a mis-cut angle of  $0.1 - 0.2^\circ$ , introducing atomic steps every  $40 - 80 \text{ nm}$  in the direction of mis-cut. Alloy disorder, the random placement of silicon and germanium atoms within a given layer, is also important for Si/SiGe quantum wells, and is discussed later in Sec. 3.4.

Atomic steps at the quantum well interface have a significant impact on the valley splitting. From the valley splitting discussion in Sec. 2.1.3 and Ref. [32], the wave function densities of the symmetric and antisymmetric valley states in a one-dimensional tight-binding approximation are

$$|\Psi_+(z)|^2 = 2 \cos^2(k_0 z + \phi) F^2(z) \quad (3.1)$$

$$|\Psi_-(z)|^2 = 2 \sin^2(k_0 z + \phi) F^2(z) \quad (3.2)$$

where  $k_0$  is the conduction band minimum at  $0.82(2\pi/a)$ ,  $\phi$  is an overall phase, and  $F(z)$  is an envelope function. The frequency of these wave function densities is  $2k_0$ . The system will minimize the ground state valley energy through changes to  $\phi$ . The ground state will have a minimum at the quantum well interface, which causes the excited state to maximize at the interface. These wave function densities within the SiGe barrier are shown in Fig. 3.1(b), with the interface at zero on the  $x$ -axis. For a single atomic step  $a/4$ , the phase shift across the step is then  $2k_0(a/4) = 0.82\pi$ . If the wave function extends laterally over a step, a single valley state cannot be minimized in both regions. This can be viewed as destructive interference of the valley states across the atomic step, resulting in a reduced valley splitting.

For this work, we propose that if the atomic steps could be engineered to stack in pairs, such that each step is double in height, the phase of the valley states would be better preserved across steps. A double atomic step is indeed possible, given the correct angle and direction of mis-cut. The single-to-double-atomic step phase change is angle and temperature dependent, but for a mis-cut along the  $[110]$  crystal direction and given the temperatures required for heterostructure growth, the minimum angle for double-atomic steps is between  $2^\circ$  and  $4^\circ$  [91–93]. Figure 3.1(c) shows a scanning tunneling microscopy (STM) image of a silicon surface, mis-cut by  $4^\circ$  along the  $[110]$  direction. The steps are bunching into double-atomic steps to minimize strain energy at the surface.

Here, we fabricate Hall bar devices on three heterostructures: one with nominally no mis-cut, one with a  $2^\circ$  mis-cut along the  $[010]$  direction, and one with a  $4^\circ$  mis-cut along the  $[110]$  direction. The  $2^\circ$  sample should have single-atomic steps at the quantum well interfaces while the  $4^\circ$  sample should have double-atomic steps. With these different heterostructures and mis-cuts, we can investigate the role of step height on the valley splitting.

### 3.1.2 Methods

The valley splitting is estimated through measurements of the Shubnikov-de Haas minima in the longitudinal resistance of Hall bars in the quantum Hall regime. Figure 3.1(d) shows

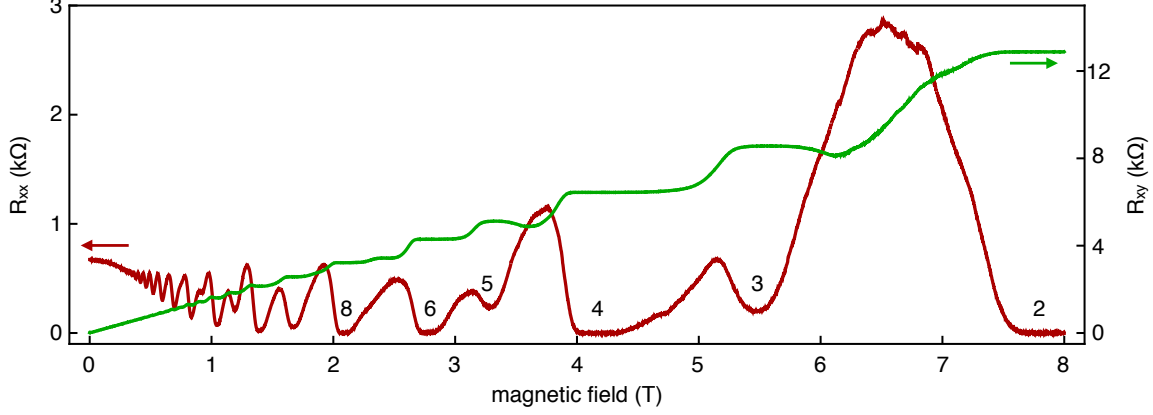


Figure 3.2: Sourcing 1.5 nA, the longitudinal (red) and transverse (green) resistances are measured on a  $4^\circ$  mis-cut Hall bar as a perpendicular magnetic field is swept. For this measurement, the mobility is  $230,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  at a carrier density of  $4.0 \times 10^{11} \text{ cm}^{-2}$ . Both deep Shubnikov-de Haas oscillation minima and quantum Hall plateaus are clearly visible, with select integer filling factors of the SdHO minima labeled.

an optical image of a Hall bar fabricated on the  $4^\circ$  mis-cut heterostructure. The top gates on all devices are separated from the heterostructure by 15 nm of aluminum oxide grown by atomic layer deposition at  $150^\circ\text{C}$ . The gate and ohmic metal is a bi-layer of titanium and gold. A single Hall bar from each of the three heterostructures were loaded together into a dilution refrigerator with a base temperature  $< 100 \text{ mK}$ .

Figure 3.2 shows a typical measurement of the transverse and longitudinal resistances of a Hall bar. For this measurement of the  $4^\circ$  mis-cut sample, the transport mobility is  $230,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  at a carrier density of  $4.0 \times 10^{11} \text{ cm}^{-2}$ . The mobilities of the flat and the  $2^\circ$  samples at a similar carrier density are  $250,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  and  $160,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ , respectively. Quantum Hall effects, as described in Sec. 2.3.2, are clearly visible. The Shubnikov-de Haas oscillations (SdHO) show deep minima which plateau at zero resistance for several integer filling factors. As described in Eq. (2.14), the ‘orbital’ Landau energies are separated by  $\hbar\omega_c = (\hbar e/m^*)B$  where  $m^*$  is the longitudinal effective mass in the silicon quantum well,  $m^* \approx 0.2m_e$ . The Zeeman splitting of the spin-up and -down states is given by  $g\mu_B B = (\hbar e/m_e)B$  for  $g = 2$ . Therefore, at any magnetic field, the spin splitting is  $\approx 5\times$  smaller than the Landau level orbital splitting. At large fields, both of these energy

splittings are much larger than the typical 20 – 200  $\mu\text{eV}$  range for the valley splitting. The hierarchy of Landau level splittings is therefore orbital  $>$  spin  $>$  valley. With this, we can assign each integer filling factor  $\nu$  to a specific splitting. Notably, the valley splitting is responsible for the odd integer filling factor SdHO minima. Inspecting the depth and width of these minima, we see that the odd minima are the shallowest and narrowest, which agrees with the assumption that the valley splitting is smaller than the other splittings.

We can measure these splittings by manipulating the temperature of the system. At the center of a Shubnikov-de Haas minima, the fermi energy of the conducting electrons in the Hall bar is spaced equally between two Landau levels. Following the method described in Ref. [94], the ‘activation’ of electrons into an excited level above the fermi energy through thermal excitations results in the resistance of the SdHO minima following an Arrhenius scaling

$$R_{xx} \propto e^{\frac{\Delta E}{2k_B T}}, \quad (3.3)$$

where  $\Delta E$  is energy gap between the Landau levels,  $k_B$  is the Boltzmann constant, and  $T$  is the temperature of the 2DEG. At minima which correspond to odd filling factors, the level splitting is the valley splitting. Therefore, by measuring the longitudinal resistance at the odd SdHO minima as a function of temperature, we can extract the valley splitting. However, we note that this is a measure of the *gap* between levels. With large Landau level broadening, the gap can be significantly reduced from the center-to-center splitting. For this reason, the measured splittings are sometimes referred to as ‘mobility gaps’ [25].

### 3.1.3 Mis-Cut Results

Figure 3.3(a-c) shows thermal activation of the resistance of the  $\nu = 3$  SdHO minima for the three heterostructures at  $n_{2D} = 4.0 \times 10^{11} \text{ cm}^{-2}$ . The SdHO minima at base temperature are shown in the insets. The mixing chamber of the fridge in which the devices are loaded is heated. Setting the magnetic field to the minimum of the  $\nu = 3$  SdHO, the longitudinal

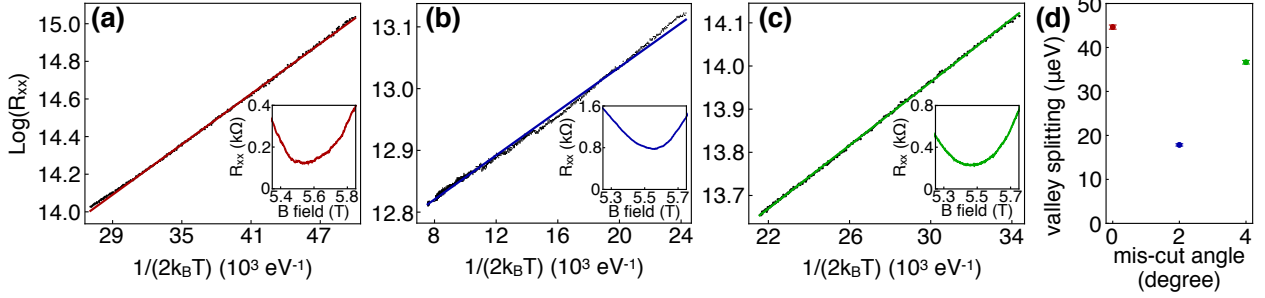


Figure 3.3: (a-c) Measurement of the resistance of the  $\nu = 3$  SdHO minimum as the temperature is swept for the on-axis (a),  $2^\circ$  mis-cut (b), and  $4^\circ$  mis-cut (c) Hall bars. All three measurements are performed at or very near  $n_{2D} = 4.0 \times 10^{11} \text{ cm}^{-2}$ . The insets in (a-c) show the  $\nu = 3$  minimum for each measurement at base temperature  $T_{MC} < 100 \text{ mK}$ . (d) Calculated  $\nu = 3$  valley splittings from the slope of the linear fits in (a-c). As shown, the valley splitting is maximal for the on-axis sample and minimal for the  $2^\circ$  mis-cut. The double atomic steps of the  $4^\circ$  mis-cut does improve the valley splitting over  $2^\circ$ , but falls short of an enhancement over a flat sample.

resistance  $R_{xx}$  is measured as the fridge is slowly cooled. We plot the natural log of the resistance as a function of inverse temperature of the fridge. Plotted in this manner, the slope of a linear fit to the data will extract the approximate valley splitting (mobility gap). It is important to note that the valley splitting is expected to increase with both magnetic field and carrier density. At higher magnetic field, the magnetic length decreases and electrons in the 2DEG interact with a smaller lateral area of disorder at the quantum well interface, leading to an increased valley splitting. At higher carrier density, following Eq. (2.13), the magnetic field for a given filling factor will be higher. Additionally, the carrier density is controlled by the top gate voltage; increasing the top gate to increase the carrier density should also increase the vertical electric field, which increases the valley splitting. For this reason, the measurements were taken at the same carrier density (and therefore the same magnetic field).

Figure 3.3(d) shows the extracted splittings from (a-c). As anticipated, the  $2^\circ$  mis-cut sample shows the smallest valley splitting out of all three samples. The  $4^\circ$  sample shows a doubling of the valley splitting over the  $2^\circ$  sample. However, the flat sample still shows the largest valley splitting. This is likely due to the flat sample having drastically fewer

atomic steps than either mis-cut samples. It is important to note that these results are only single measurements of each heterostructure, and are in no way definitive. However, we can infer that the valley splitting is affected by step density and that the type of atomic step – single or double – further influences its value. For practical purposes of increasing the valley splitting, the disorder caused by the severe mis-cut angle required may outweigh the benefits of the double-atomic steps.

## 3.2 Valley Splittings in Si/SiGe Quantum Dots with a Germanium Spike in the Silicon Well

This section is adapted from Ref. [30].

### 3.2.1 Introduction

Low-lying valleys in the silicon conduction band are a focal point in the pursuit of gate-defined quantum dot qubits. For silicon quantum wells strained between layers of relaxed silicon-germanium, there are only two low-lying valley states, separated in energy by the valley splitting [14,32,95]. While defect-free Si/SiGe heterostructures are predicted to have  $> 1$  meV valley splitting, interfacial disorder, growth on a substrate that is mis-cut with respect to the crystal axes, and other imperfections lead to typical valley splittings in the range of tens to hundreds of  $\mu\text{eV}$  [18]. For single-electron spin qubits, the valley splitting should be as large as possible [39,96]. For other qubit implementations, such as the quantum-dot-hybrid qubit, the valley splitting is integral to the logical state energies, and an intermediate valley splitting of order  $30 \mu\text{eV}$  is desirable [35,43,81,97].

The valley splitting in SiGe heterostructures can be tuned by controlling the vertical electric field or lateral dot position [21,26,27,29,98,99]. In the first case, the applied electric field affects the wave function overlap with the SiGe barrier and therefore affects the valley splitting; however, the electric field is often bounded by material limits or control limits of

the dot for qubit use. In the second case, the lateral position of the dot determines the disorder profiles it experiences at the quantum well interface; however, this tuning method is inherently unpredictable as the disorder itself is poorly controlled or characterized. Previous work modifying the Si/SiGe heterostructure by inclusion of extra germanium at the quantum well interface has highlighted the critical role of disorder in these heterostructures [25].

Here, we explore a new method for modifying the valley splitting by including an ultra-thin layer of silicon-germanium within the silicon quantum well. This spike in germanium concentration is placed near the upper interface of the quantum well where the two-dimensional electron gas (2DEG) is formed [100]. It effectively splits the quantum well into two regions, significantly affecting the shapes of the two valley wave functions and increasing the energy splitting between them. We describe the growth of this heterostructure and characterize it with scanning transmission electron microscopy (STEM). Hall bars and quantum dot devices are fabricated on the heterostructure, and magnetospectroscopy is used to measure the excited state energy spectrum of a few-electron quantum dot. These results reveal a large and tunable valley splitting. Furthermore, they demonstrate that stable and clean quantum device behavior is achievable in the presence of large modulations in Ge concentration, even when it is positioned directly at the peak of the electron wave function in the quantum well. In order to understand how the SiGe layer within the quantum well contributes to the valley splitting, we perform one- and two-dimensional tight-binding simulations of a single-electron quantum dot in the presence of common interfacial disorder. We present numerical calculations showing that the presence of the ultra-thin SiGe layer in this sample increases the valley splitting by a factor of two compared to a heterostructure without this layer. This doubling is robust against large changes in the Ge concentration of the spike, its position in the quantum well, and the vertical electric field.

This paper is organized as follows. In Sec. 3.2.2 we describe the experimental growth and measurement methods. In Sec. 3.2.3 we present magnetospectroscopy results at the 1-2, 2-3, and 3-4 electron charging transitions and tuning of the excited state spectrum at

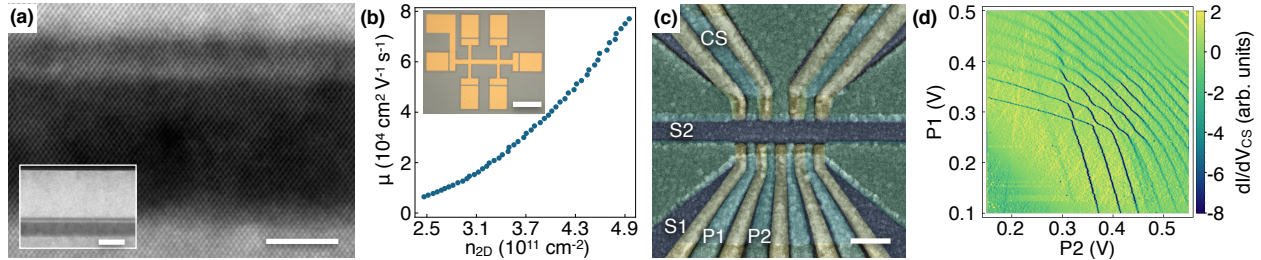


Figure 3.4: (a) High-angle annular dark-field (HAADF) images of the SiGe heterostructure characterized, acquired with a scanning transmission electron microscope (STEM). Higher brightness in the images corresponds to higher germanium concentration. The main image focuses on the silicon quantum well, with a 5 nm scale bar. The inset shows the heterostructure from the surface to the well, with a 20 nm scale bar. (b) Carrier density and transport mobility of a Hall bar fabricated on the heterostructure shown in (a), measured in a dilution refrigerator at  $< 50$  mK. The inset shows an optical image of the Hall bar, with a 200  $\mu\text{m}$  scale bar. Dimensions of the Hall bar are 200  $\mu\text{m}$  long by 20  $\mu\text{m}$  wide. (c) False-colored scanning electron micrograph of the quantum dot device measured, with a 200 nm scale bar. The different colors (blue, green, yellow) indicate different gate layers. (d) Stability diagram of a double quantum dot formed using the left two quantum dot plunger gates (P1 and P2) and charge sensing quantum dot (CS), as labeled in (c).

the 3-4 electron charging transition. In Sec. 3.2.4, we present both effective mass theory and tight-binding theory of the Ge spike's effect on the valley splitting. Section 3.2.5 is a summary, and the Appendices present details of the magnetospectroscopy measurements and tight binding calculations.

### 3.2.2 Experimental Methods

The heterostructure is grown by ultra-high vacuum chemical vapor deposition (UHV-CVD) on a linearly graded SiGe alloy with a final 2  $\mu\text{m}$  layer of  $\text{Si}_{0.705}\text{Ge}_{0.295}$ . Prior to heterostructure growth, the SiGe substrate is cleaned and prepared as described in Ref. [25]. The heterostructure is grown at 600  $^\circ\text{C}$  with a mixture of silane and germane gases. A 550 nm, 29.5% Ge alloy layer is grown before the silicon quantum well. The main silicon well is grown, then germane is re-introduced to grow the ultra-thin layer of SiGe. The germane flow is stopped to grow the silicon layer in the quantum well above the SiGe layer, followed by a 33 nm layer of 29.5% Ge alloy. The growth is capped with a 1 nm layer of silicon. The

resulting heterostructure is shown in Fig. 3.4(a) in a high-angle annular dark-field (HAADF) image acquired with a scanning transmission electron microscope (STEM). The lighter colored SiGe layer within the darker colored Si quantum well is clearly visible. This spike in Ge content is approximately 1 nm thick, creating a  $\sim 1.5$  nm secondary quantum well above the  $\sim 10$  nm main quantum well. In the inset, a broader view of the heterostructure shows that the location and thickness of the germanium spike is relatively constant across a wide area.

Hall bar and quantum dot devices were fabricated simultaneously on this heterostructure. A 20 nm layer of aluminum oxide grown by atomic layer deposition at 200 °C isolates the various metallic gates from the surface of the heterostructure, followed by a 15 minute, 450 °C forming gas anneal. All measurements were performed in a dilution refrigerator with a base temperature below 50 mK. Measurements of the Hall bar device shown in Fig. 3.4(b) reveal transport mobilities in the range of  $1-8 \times 10^4$  cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> across an electron density range of  $2.5-5 \times 10^{11}$  cm<sup>-2</sup>. Fabrication of the quantum dots follows the procedures of Ref. [46], using a three-layer, overlapping aluminum gate design with each layer isolated by the self-oxidation of the aluminum. This oxidation is enhanced by a 15 minute down-stream oxygen plasma ash. A false-colored scanning electron micrograph of a quadruple quantum dot device nominally identical to the one measured is shown in Fig. 3.4(c). The bottom half of the device shows four linearly arranged quantum dots, opposing two charge sensing quantum dots on the top half. For the work reported here, the left side of the device is used. Figure 3.4(d) shows a double quantum dot stability diagram in the zero-to-few electron regime of the left two dot plunger gates, P1 and P2, sensed by the charge sensor dot CS. For additional double quantum dot measurements of this device, see Ref. [101].

In Sec. 3.2.3 below we report the results of magnetospectroscopy performed on a single quantum dot, in order to characterize the valley splitting, by determining the value of the in-plane magnetic field that causes a change in the ground state spin configuration [21, 82–84]. To perform magnetospectroscopy, as a function of the in-plane magnetic field, we measure

the voltage on gate P2 at which electron charging transitions occur. See Sec. 3.2.7 for example raw data and Sec. 3.2.8 for the fitting procedures used in Fig. 3.5. We measure the  $g$ -factor of electrons in this heterostructure to be  $g = 1.98 \pm 0.03$  (see Sec. 3.2.9), matching the expected value for silicon [102].

### 3.2.3 Experimental Results

In this section, we first discuss how the relevant energy splittings are extracted from the magnetospectroscopy measurements. Next, we report the energy splittings for different electron occupations in the dot. We then show how the splittings depend on the vertical electric field and lateral confinement in the dot by tuning the gate voltages to maintain a constant dot occupancy.

Figure 3.5(a) shows the 0-1 charge transition as a function of the in-plane magnetic field  $B$ , which decreases the ground state energy by  $m_s g \mu_B B$ , where  $m_s$  is the spin projection along the magnetic field,  $g$  is the electron  $g$ -factor, and  $\mu_B$  is the Bohr magneton. The slope of the transition line is determined by the combination of the Zeeman effect and the lever arm  $\alpha$  connecting the voltage on gate P2 to the chemical potential of the quantum dot. As shown in the inset, and the corresponding fit to the data points, this data is consistent with single-electron occupation of the quantum dot.

The singlet-triplet (ST) splitting can be extracted by performing the same measurement at the 1-2 charge transition, as shown in Fig. 3.5(b). For small  $B$ , the transition line slopes upward, because a spin of opposite sign is added to form a singlet ground state. A kink occurs in the curve when the  $T_-$  state is Zeeman shifted by an amount equal to the zero-magnetic-field singlet-triplet splitting and becomes the ground state. Tracking the line labeled  $|1, -1\rangle$  in the inset to zero magnetic field enables extraction of this splitting, and a value of 31.4  $\mu\text{eV}$  is reported in Table 3.1. This is a lower bound on the single-electron valley splitting, because electron-electron interactions suppress the two-electron ST splitting from this value [29].

Magnetospectroscopy of the 2-3 electron charging transition (Fig. 3.5(c)) displays two

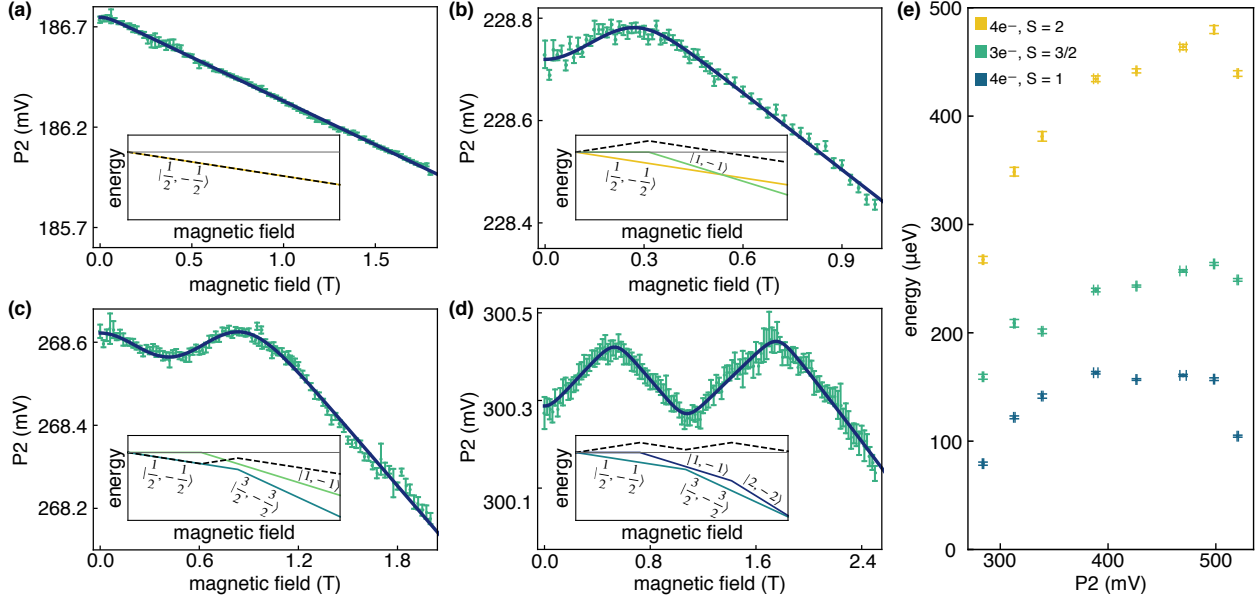


Figure 3.5: (a-d) Dependence on magnetic field of the gate voltage at which an additional electron enters the dot at the 0-1, 1-2, 2-3, and 3-4 electron charging transitions, respectively. Green points show the location of the maximum of the differentiated charge sensor signal of the electron charging transition. Dark blue lines show the computed fits to the data, as described in Sec. 3.2.8. Zero-magnetic-field spin splittings extracted from the fits in (b-d) are presented in Table 3.1. Insets to (a-d) schematically show the changing ground spin states and resulting magnetospectroscopy curve. The colored lines show the energies of the ground spin states  $|S, m_s\rangle$  of both electron occupations in the main figure as a function of magnetic field. As the spin state energies of each electron occupation differs, the energy of the electron charging transition changes with magnetic field. Subtracting the lower occupation spin energy from the higher occupation spin energy, we obtain the magnetospectroscopy curve, shown as the dashed black line. Thus, the magnetospectroscopy slope measured at any electron charging transition  $n \rightarrow n + 1$  is proportional to  $m_s(n + 1) - m_s(n)$ . (e) Magnetospectroscopy results at the 3-4 electron charging transition as a function of  $P2$  and  $S1/S2$  voltage tunings, as described in Sec. 3.2.3. The zero-magnetic-field excited state energies of the polarized spin states for 3 and 4 electrons are shown, labeled by their spin number,  $S$ .

kinks: the first reveals the 2-electron ST splitting, but in this case at gate voltages corresponding to the 2-3 transition instead of the 1-2 transition. That is, the electric field pulling the electrons onto the ultra-thin SiGe layer and against the interface is larger, and as a result the extracted 2-electron ST splitting of  $47.9 \mu\text{eV}$  is larger than at the 1-2 transition. The second kink reveals the energy of the zero-magnetic-field excited state  $|3/2, -3/2\rangle$ , as reported in Table 3.1.

electron	$2e^-$	$3e^-$	$4e^-$	$4e^-$	P2
charging	$S=1$	$S=\frac{3}{2}$	$S=1$	$S=2$	$\alpha$
transition	( $\mu\text{eV}$ )	( $\mu\text{eV}$ )	( $\mu\text{eV}$ )	( $\mu\text{eV}$ )	(eV/V)
1 $\rightarrow$ 2	31.4(5)	-	-	-	0.115(2)
2 $\rightarrow$ 3	47.9(7)	88.8(6)	-	-	0.126(2)
3 $\rightarrow$ 4	-	121(1)	64(1)	263(4)	0.17(1)

Table 3.1: Zero-magnetic-field excited spin state energies extracted from the magnetospectroscopy curves in Fig. 3.5(b-d). Each row corresponds to a different electron charging transition, as indicated in the first column. The second column reports the two-electron singlet-triplet splitting. The final column shows the lever arm,  $\alpha$ , as calculated from the magnetospectroscopy slope.

Figure 3.5(d) reports magnetospectroscopy for the 3-4 electron charging transition, revealing a set of three kinks corresponding to the zero-magnetic-field energies of three excited states, as reported in Table 3.1. These excited state energies again place a lower bound on the valley splitting, in this case at yet larger electric field, corresponding to the 3-4 charge transition. With the larger number of electrons involved, and as shown in Sec. 3.2.8, Eqs. (3.12-3.14), we can extract the valley splitting of both the ground and the first excited orbital state, in the approximation that electron-electron interactions are negligible. We find a ground state valley splitting of  $57 \pm 2 \mu\text{eV}$  and a valley splitting of the first orbital excited state of  $78 \pm 4 \mu\text{eV}$ . The first excited orbital state energy is also extracted in this approximation, which we find is  $132 \pm 2 \mu\text{eV}$ .

With these measurements at various electron charging transitions, we find that the valley splitting increases with electric field, consistent with results on conventional Si/SiGe heterostructures [26, 98, 99]. Furthermore, the 3-4 electron charging transition allows us to characterize excitations primarily associated with valleys and orbitals.

To better understand the range of device tunings that are possible with electric fields, we perform additional magnetospectroscopy measurements at the 3-4 transition as a function of vertical electric field. Here, we simultaneously adjust the voltages on several gates, as described below, to ensure that only the electric field changes (not the dot location), while

keeping the charge occupation fixed. The quantum dot is beneath gate P2, which we make more positive in order to increase the electric field, thus pulling the dot tighter against the interface and the ultra-thin SiGe layer. Simultaneously, we make the voltages on gates S1 and S2 more negative to increase the confinement energy and adjust the barrier gate voltages to maintain reasonable tunnel rates. Section 3.2.10 shows the resulting magnetospectroscopy curves and reports COMSOL simulations which confirm that this approach increases the electric field while keeping the dot centered in the channel.

Figure 3.5(e) shows the three zero-magnetic-field excitation energies of the 3-4 electron charging transition as a function of the voltage on gate P2. We note that larger P2 gate voltage corresponds to stronger vertical electric field and stronger lateral confinement. Remarkably, each of these excitation energies can be tuned by at least 60% through this tuning approach. Using Eq. (3.12), we estimate a tuning range of 60 – 144  $\mu\text{eV}$  for the valley splitting, as we simultaneously adjust the electric field and confinement potential.

Previous results have shown valley splitting tunability of 15% with a maximum value of 213  $\mu\text{eV}$  [27] as well as 140% tunability with a maximum value of 87  $\mu\text{eV}$  [29]. Here, we show 140% tunability with a lower bound on the maximum valley splitting of 144  $\mu\text{eV}$ . Hence, we conclude that the presence of the ultra-thin SiGe layer inside the quantum well facilitates, or is at least compatible with, a large and widely tunable valley splitting in few-electron dots.

### 3.2.4 Theory

In order to better understand the underlying physics of the Ge spike inside the quantum well and its contribution to the valley splitting, we perform effective mass and tight-binding calculations with and without this additional SiGe layer. These calculations are performed in single-electron quantum dots.

## Effective Mass Theory

We first begin with an effective mass theory interpretation of the valley splitting due to a single atom barrier within the quantum well. Valley splitting is determined by the interactions between electronic wave functions and barrier interfaces in the quantum well. For weak valley-orbit interactions, the two low-energy eigenfunctions  $\psi$  can be approximately written as  $\sqrt{2}F(\mathbf{r}) \cos(k_0z + \varphi)$  and  $\sqrt{2}F(\mathbf{r}) \sin(k_0z + \varphi)$ , where  $F(\mathbf{r})$  is the effective mass envelope function,  $k_0$  is the position of the conduction-band valley minimum in reciprocal space,  $z$  is the position coordinate in the [001] growth direction, and  $\varphi$  is a fixed phase that maximizes the valley splitting [32]. For a single-atom barrier potential at  $z = z_s$ , the variable  $\varphi$  is determined such that the ground-state wave function has a node at the barrier,  $\cos(k_0z_s + \varphi) = 0$ , while the excited state wave function takes its maximum value, such that  $\sin(k_0z_s + \varphi) = 1$ . The resulting potential energy difference for these two eigenstates is large, and can be further enhanced by positioning the barrier at the peak of the envelope function, yielding a very large valley splitting. For a more complete description of how the wave function envelopes differ, the valley-orbit coupling induced by the single-atom barrier should be taken into account, as described in Sec. 3.2.11. The envelopes of the two valley states are plotted in Fig. 3.6(a) and differ significantly, indicating an extraordinary level of mixing between the orbital and valley degrees of freedom (valley-orbit coupling). Large valley-orbit coupling occurs because the ground-state wave function has a node with  $\psi = 0$  at the position of the barrier (blue arrow and gray circle), while the excited-state wave function is maximized at the same location (green arrow and gray circle).

## Tight-Binding Theory

We investigate the effect of the germanium spike on the excited state spectrum using a tight-binding model to calculate single-electron valley splittings [98, 103]. We first consider the one-dimensional Ge spike geometry shown in Fig. 3.6(a). The resulting wave function densities for the ground and excited valley states are plotted as discrete points in Fig. 3.6(a),

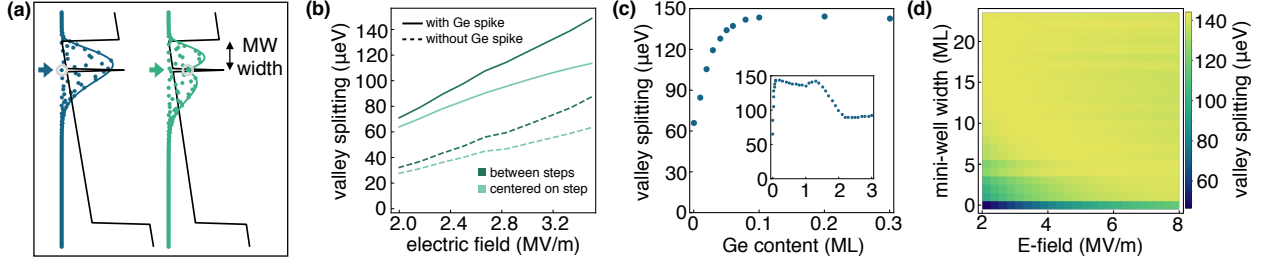


Figure 3.6: Results of tight-binding calculations of the valley splitting in the presence of a Ge spike, assuming realistic interfacial disorder with uniform atomic steps spaced 45 nm apart. (a) One-dimensional tight-binding calculations of wave function densities ( $|\psi|^2$ ) for the ground state (blue circles) and the first excited state (green circles) of an electron in a 12.9 nm quantum well and vertical electric field of 5.5 MV/m, with a single-atom barrier positioned 19 monolayers below the top of the quantum well. Solid lines show the density envelopes, computed as described in Sec. 3.2.11, while the data points are obtained using a tight-binding theory, as described in Section 3.2.4. (b) The valley splitting of the lowest orbital of a quantum dot, where the quantum dot is placed halfway between two steps (darker lines) or centered at a step (lighter lines). The solid lines are calculated for a heterostructure modeled after the experimental growth results shown in Fig. 3.4(a), while the dashed lines are calculated for a standard heterostructure with no added germanium in the silicon well. The addition of a germanium spike roughly doubles the valley splitting. (c) Tight-binding calculations of the valley splitting in a quantum dot with a 3 MV/m vertical electric field, centered halfway between two steps in a heterostructure with a monolayer (ML) spike in germanium located 20 ML below the upper interface of the quantum well. The main figure shows the valley splitting as a function of germanium content. The inset shows the same for higher germanium content, with contents greater than 1 achieved by increasing the spike thickness through additional mono-layers closer to the upper interface of the well. (d) Valley splitting as a function of the location of the Ge spike and the applied electric field for a single ML spike of 30% germanium. The location of the Ge spike is defined in terms of the width of the ‘miniwell’ created between the Ge spike and the upper interface of the quantum well (shown by the black arrow in (a), labeled with MW width). For the case of zero miniwell width, the Ge spike contacts the  $\text{Si}_{0.7}\text{Ge}_{0.3}$  capping layer, consistent with a heterostructure with no added SiGe layer.

showing good agreement with the envelopes calculated in Sec. 3.2.11.

We then perform two-dimensional tight-binding simulations using the method described in Ref. [104] to investigate how realistic disorder in the heterostructure affects the single-electron valley splitting. The electric fields applied in the experiments are estimated using COMSOL, as described in Sec. 3.2.10. We introduce atomistic disorder at the quantum well interfaces by assuming a uniform step density of 45 nm/step, which allows us to ap-

proximately match the valley splitting results in the simulations to the lower bounds of the valley splittings calculated from Fig. 3.5(e). Similarly, the lower bound of the orbital splitting, calculated from Fig. 3.5(e), is adopted as the lateral parabolic confinement  $\hbar\omega$  in the tight-binding model. As noted above, this correspondence is not accurate in the presence of strong electron-electron interactions; however, it allows us to establish an approximate working regime for our simulations.

The simulations are performed for both a standard SiGe heterostructure and a heterostructure with an added realistic spike in germanium, whose shape profile is estimated from the STEM results in Fig. 3.4(a). These results are presented in Fig. 3.6(b). Because the location of the dot with respect to the background of atomic steps influences the valley-orbit coupling, we perform two sets of simulations: the first with the dot centered halfway between two steps, and the second with the dot centered directly on a step. For the lowest orbital, the addition of the germanium spike within the quantum well results in a doubling of the valley splitting compared to a standard heterostructure, as shown in Fig. 3.6(b). This doubling is approximately independent of both the quantum dot position and the applied electric field, indicating a rather robust effect. Additionally, the simulated increasing lateral confinement with increasing electric field results in an increasing valley splitting for all simulated interfaces.

To investigate further how a spike in germanium within the quantum well affects the valley splitting, we also vary the germanium concentration, spike location, and electric field in tight-binding simulations, for the case of a mono-atomic-layer spike. Figure 3.6(c) shows the valley splitting dependence on germanium content within the spike. For a mono-atomic-layer spike, we observe that the doubling of the valley splitting is already achieved with less than 10% germanium. This remains true up to a thickness of 1.5 monolayers of pure germanium, as shown in the inset. Figure 3.6(d) shows the valley splitting dependence on both the vertical location of a 30% Ge spike and the applied electric field. Here, we define the spike position in terms of the ‘mini-well’ width, referring to the number of atomic layers in

the portion of the quantum well above the top of the spike and shown by the black arrow in Fig. 3.6(a). We note that a mini-well of width zero corresponds to a typical heterostructure without the Ge spike. Remarkably, the observed doubling in the valley splitting is fairly resilient to both spike positioning and vertical electric field, over its entire range. For the case of zero mini-well width, the valley splitting shows a strong dependence on vertical electric field as more of the wave function is pulled into the alloy. Once the Ge spike is separated by several monolayers from the interface, however, the valley splitting remains essentially constant as a function of spike position and electric field. These results suggest an enhanced valley splitting can be obtained without needing to carefully position the germanium spike.

### 3.2.5 Conclusions

We have studied a new heterostructure containing a spike in germanium concentration in the quantum well at the approximate location of the 2DEG. Hall bars and quantum dots were successfully fabricated and measured on this structure. Magnetospectroscopy measurements were used to probe the few-electron energy splittings and explore how these splittings change with gate voltage tunings. We showed large and widely tunable few-electron energy splittings, arising from a large and tunable single-electron valley splitting. Tight-binding simulations in a single-electron quantum dot showed that the valley splitting doubles in the presence of the germanium spike, and that this effect should be robust against typical growth imperfections. These results serve as an example that large changes to the standard Si/SiGe heterostructure still allow for stable quantum dot formation while modifying its underlying properties.

### 3.2.6 Acknowledgments

This research was sponsored in part by the Army Research Office (ARO), through Grant Number W911NF-17-1-0274 and the Vannevar Bush Faculty Fellowship program sponsored by the Basic Research Office of the Assistant Secretary of Defense for Research and Engineering and funded by the Office of Naval Research through Grant No. N00014-15-1-0029. Devel-

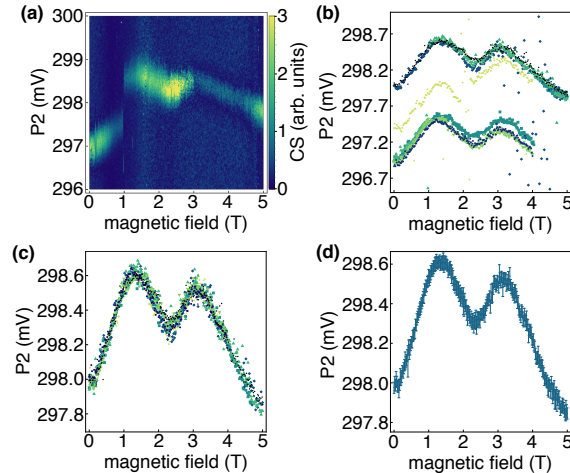


Figure 3.7: (a) Example magnetospectroscopy dataset with characteristic ‘jump’ near 1 Tesla. (b) Extracted peak locations of unmodified datasets. Black points are the reference scan, colored points are all other datasets at this tuning. (c) Same data as in (b), with registration shifts. (d) Final dataset, with plotted voltage error.

opment and maintenance of the growth facilities used for fabricating samples was supported by DOE (DE-FG02-03ER46028). We acknowledge the use of facilities supported by NSF through the UW-Madison MRSEC (DMR-1720415) and the MRI program (DMR-1625348). The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Army Research Office (ARO), or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation herein.

### 3.2.7 Appendix: Magnetospectroscopy Data Acquisition and Registration

The electron charging transition of the dot formed under P2 is sensed by the charge sensor dot CS (labeled in Fig. 3.4(c)). A small ac voltage is applied to P2 and the current through the charge sensor is measured by a lock-in amplifier, such that electron charging transitions appear as peaks in the lock-in response, as shown in Fig. 3.7(a). To extract the peak location

of the electron charging transition, we fit to each fixed-magnetic-field voltage scan. This fit, based on conductance through a quantum dot [64], is

$$\frac{dI_{sensor}}{dV} = a + b * (\cosh[\frac{V - V_{peak}}{c}])^{-2}, \quad (3.4)$$

where  $V_{peak}$  is the extracted peak location and  $a$ ,  $b$ , and  $c$  are additional fit parameters not used in this analysis.

Due to the length of time required for a magnetospectroscopy scan ( $\sim$ hours) and the relative instability of the nearby charge landscape, finite shifts in the electrostatic potential of the quantum dot result in few mV shifts in the dot transition with respect to the P2 voltage during the measurement, as shown near 1 T in Fig. 3.7(a). These shifts occur infrequently ( $\sim$ once per hour), allowing for repeated magnetic field sweeps to fully measure the magnetospectroscopy curve. After measurement, registration of the various scans is performed to achieve a single magnetospectroscopy curve.

To perform this registration, multiple magnetospectroscopy scans are repeatedly collected. The scan with the largest segment of data uninterrupted by a charge jump is determined and used as the registration reference. Each additional scan is registered to this reference in the magnetic field range in which they overlap (Fig. 3.7(b)). To calculate the voltage shift required to register each scan or a portion of a scan, the sum of the squared residuals between them is calculated, excluding the largest 10% of residuals. This sum is then minimized by allowing for an overall voltage shift to the scan, resulting in overlapping data sets like that shown in Fig. 3.7. This process is repeated for all additional scans. A final data set is created (Fig. 3.7(d)) by calculating the weighted mean at each magnetic field value, using the uncertainty in the fit for the peak location from the original scans as the weights.

### 3.2.8 Appendix: Magnetospectroscopy Fitting

In order to fit magnetospectroscopy data, we implement a model utilizing a grand canonical ensemble, in which both the energy and the number of particles can be exchanged between a quantum dot and a reservoir. The energy states  $E_i$  of the quantum dot with  $N_i$  electrons can be written as a function of the charging energy,  $E_c$ , the Zeeman energy of the spins,  $E_Z = m_s g \mu_B B$ , the zero-magnetic-field energy of the excited spin states,  $E_{ex}$ , and the electrostatic energy imparted by the gate voltage,  $V$ , using the lever-arm conversion factor  $\alpha$  [76]:

$$E_i = \frac{1}{2} N_i^2 E_c + E_Z + E_{ex} - N_i \alpha V. \quad (3.5)$$

To calculate the average number of particles, we use

$$\langle N \rangle = \frac{\sum_i N_i g_i \exp\{\beta(N_i \mu - E_i)\}}{\sum_i g_i \exp\{\beta(N_i \mu - E_i)\}}, \quad (3.6)$$

where  $g_i$  is the multiplicity of the  $i^{\text{th}}$  state,  $\beta$  is the Boltzmann factor  $1/k_b T$  and  $\mu$  is the chemical potential of the dot. To analyze the charging transition from  $N$  to  $N + 1$  electrons, we note that the peak in conduction (or peak in differentiated charge sensor signal) corresponds to an average electron occupation of  $N + 1/2$ . Therefore, by equating Eq. (3.6) to  $N + 1/2$  and solving for  $V$ , we obtain an equation for the electron charging transition as a function of magnetic field. Setting  $E_c$  and  $\mu$  to zero (as they only cause an overall shift in  $V$ , which we define as  $V_0$ ), the remaining fitting parameters are now  $\alpha$ , the electron temperature, and the various excited state energies of the polarized spin states. For the 1 electron to 2 electron charging transition, there are 2 and 4 possible spins states, respectively. Defining the singlet-triplet splitting of the 2 electron system as  $E_{ST}$ , we can now express the voltage where the 1-2 electron charging transition occurs as

$$V_{1 \rightarrow 2}(B) = \frac{1}{\alpha \beta} \log \left( \frac{(e^{\beta g \mu_B B} + 1) e^{\beta(\frac{1}{2} g \mu_B B + E_{ST})}}{e^{\beta(g \mu_B B + E_{ST})} + e^{2\beta g \mu_B B} + e^{\beta g \mu_B B} + 1} \right) + V_0. \quad (3.7)$$

To account for the magnetic field dependence of the transverse component of the electron wave function in the dot and the chemical potential of the reservoir [105–107], a quadratic term in magnetic field,  $\gamma B^2$ , is added to the 3-4 electron charging transition fitting function to better fit the magnetospectroscopy curves at large magnetic field.

The gate voltage where the 0-1, 2-3, and 3-4 electron charging transitions occur are

$$V_{0 \rightarrow 1}(B) = -\frac{\beta B g \mu_B + 2 \log(e^{-\beta g \mu_B B} + 1)}{2\alpha\beta} + V_0, \quad (3.8)$$

$$V_{2 \rightarrow 3}(B) = \frac{1}{\alpha\beta} \log \left( \frac{e^{\beta(\frac{1}{2}g\mu_B B - E_{ST} + E_{S=3/2})} (e^{\beta(g\mu_B B + E_{ST})} + e^{\beta g \mu_B B} + e^{2\beta g \mu_B B} + 1)}{(e^{\beta g \mu_B B} + 1)(2e^{\beta(g\mu_B B + E_{S=3/2})} + e^{2\beta g \mu_B B} + 1)} \right) + V_0, \quad (3.9)$$

$$V_{3 \rightarrow 4}(B) = \gamma B^2 + V_0 + \frac{1}{\alpha\beta} \log \left( \frac{(e^{\beta g \mu_B B} + 1) (2e^{\beta(g\mu_B B + E_{S=3/2})} + e^{2\beta g \mu_B B} + 1) e^{\beta(\frac{1}{2}g\mu_B B - E_{S=3/2} + E_{S=1} + E_{S=2})}}{d} \right), \quad (3.10)$$

where the denominator is given by

$$d = 2e^{\beta(2g\mu_B B + E_{S=1} + E_{S=2})} + e^{\beta(g\mu_B B + E_{S=1})} + e^{\beta(2g\mu_B B + E_{S=1})} + e^{\beta(3g\mu_B B + E_{S=1})} + e^{\beta(4g\mu_B B + E_{S=1})} + e^{\beta E_{S=1}} + 3e^{\beta(g\mu_B B + E_{S=2})} + 3e^{\beta(2g\mu_B B + E_{S=2})} + 3e^{\beta(3g\mu_B B + E_{S=2})}, \quad (3.11)$$

$E_{S=3/2}$  is the 3-electron excitation energy, and  $E_{S=1}$  and  $E_{S=2}$  are the 4-electron excitation energies.

As explained in the main text, the lower bounds of the valley and orbital splittings can be estimated from the zero-magnetic-field excited spin energies. Measuring at the 3-4 electron charging transition, the lowest lying valley splitting  $E_{V1}$ , orbital splitting  $E_{Orb}$ , and valley

splitting  $E_{V2}$  of the first excited orbital are given by

$$E_{V1} \geq E_{S=3/2} - E_{S=1}, \quad (3.12)$$

$$E_{Orb} \geq \frac{1}{2}E_{S=2}, \quad (3.13)$$

$$E_{V2} \geq E_{S=2} - E_{S=3/2} - E_{S=1}. \quad (3.14)$$

### 3.2.9 Appendix: $g$ -factor Measurement

Measurements are performed to determine whether the electron  $g$ -factor is modified by the Ge spike or changes with magnetic field, as has been previously reported [87]. Measuring the  $g$ -factor is also important for confirming the accuracy of energy splittings measured with magnetospectroscopy. Here, we employ a method similar to Ref. [87], where pulsed-gate spectroscopy [83, 85, 108] was performed at various applied magnetic fields. Figure 3.8(a) shows how the spin loading lines are split by the applied magnetic field. This spin splitting is tracked as a function of applied magnetic field. Using a lever-arm calculated through measurements of the thermal broadening of the detected charge sensor signal, this spin splitting in voltage space is converted to an energy splitting. Fitting these results linearly, as shown in Fig. 3.8(c), we see that the calculated  $g$ -factor falls within the uncertainty of the expected value of  $g \approx 2$  [102].

### 3.2.10 Appendix: Electric Field Tuning of states in the Quantum Dot

The gates S1 and S2, labeled in Fig. 3.4(c), are used to modify the vertical electric field at the quantum dot. Relative lever arms of the S gates with respect to the plunger gate P2 are calculated from the slope of the electron charging transition in 2D plots of P2 and each S gate. The S gates are then tuned according to these lever arms such that the change in

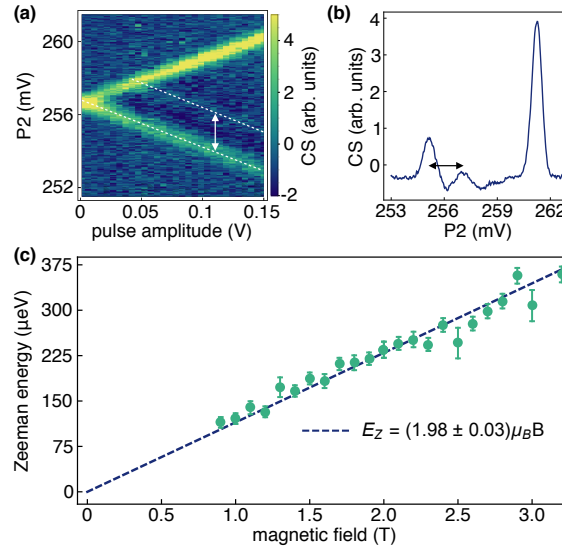


Figure 3.8: (a) Pulsed-gate spectroscopy of the P2 quantum dot at the 0-1 electron charging transition. A 100 – 300 kHz square wave voltage tone is applied to the dot gate. A 2 Tesla in-plane magnetic field is applied to split the spin-dependent loading lines (highlighted with white dashed lines). The white arrow indicates the spin-splitting. (b) A highly averaged voltage scan at a fixed pulse amplitude and a 1.8 Tesla magnetic field. The black arrow indicates the spin-split loading lines. (c) The spin-splitting (Zeeman energy) is calculated from the voltage splitting, multiplied by the dot-to-gate lever arm, and is plotted as a function of applied magnetic field (green points). A linear fit (dashed line) through the data points yields the extracted  $g$ -factor.

voltage of each of these gates affects the dot transition equally. Lowering the voltage on the S gates necessarily results in an increased P2 voltage to maintain the same charge occupation. Additionally, the barrier gates surrounding P2 are modified to maintain an adequate tunnel rate. Figure 3.9(a) shows the lever arm at each tuning for the 4 gates with the largest lever arms. The P2 lever arm is calculated from the magnetospectroscopy fit and the three other lever arms are calculated from the relative lever arms measured during tuning. The shaded area is  $\pm 5\%$  around the weighted mean, showing that the lever arms, and therefore dot positioning with respect to these gates, changes very little across the tuning range. The voltages of the S gates at each tuning are shown in Fig. 3.9(b).

This tuning scheme is replicated with Thomas-Fermi calculations using COMSOL multi-physics to estimate the electric field at the location of the dot and validate our interpretation

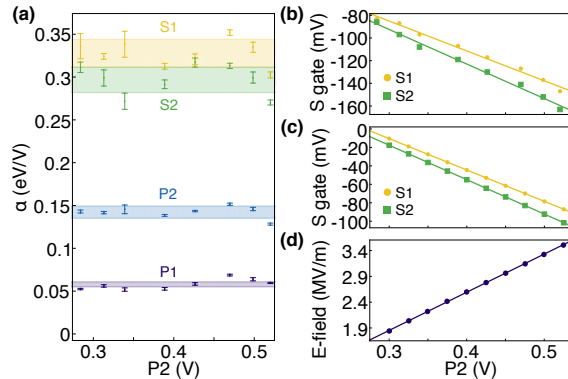


Figure 3.9: (a) Lever arm ( $\alpha$ ) calculations of the four nearby gates with the largest action on the quantum dot as a function of the experimental voltage tuning for Fig. 3.5(e). See Fig. 3.4(c) for gate labeling. The shaded area shows  $\pm 5\%$  variations around the weighted mean. (b) Experimental voltage tuning of the S1 and S2 gates, based on the relative lever arm difference found in (a). Lines are linear fits through the data. (c) Voltage tuning of S1 and S2 gates in a COMSOL simulation meant to extract the applied electric field at the location of the quantum dot. Relative tuning of S gates is based on the relative mutual capacitance between the S gate and the quantum dot. Lines are linear fits through the data. (d) Electric field results from the COMSOL simulated tuning in (c), showing a linearly increasing electric field as a function of P2 voltage. These electric field results are used for the tight-binding calculations shown in Fig. 3.6(b).

of these voltage changes. The three aluminum gate layers are modeled using the intended fabrication dimensions and a 2DEG is located 2 nm beneath the upper interface of a Si/SiGe interface. With P2 set to 300 mV (lower end of experimental tunings), the nearest barrier and screening gate voltages are adjusted to achieve 3.5 electrons confined within the quantum dot. All other gate voltages are set to accumulate a charge density of  $4 \times 10^{11} \text{ cm}^{-2}$ . Similar to the experimental tuning scheme, the mutual capacitances between the dot and gates S1 and S2 are calculated. With the constraints of maintaining 3.5 electrons in the dot and the experimental P2 voltage range, S1 and S2 are ‘symmetrically’ tuned according to their capacitance values. This has the effect of preserving the simulated lateral dot position to within 1 nm. The resulting tuned screening voltages are shown in Fig. 3.9(c). Lack of simulated trapped charge and possible fabrication imperfections causes different voltage ranges to be obtained in the experimental and simulated screening voltage values. Figure 3.9(d) shows the calculated COMSOL electric field results at the center of the quantum dot, which

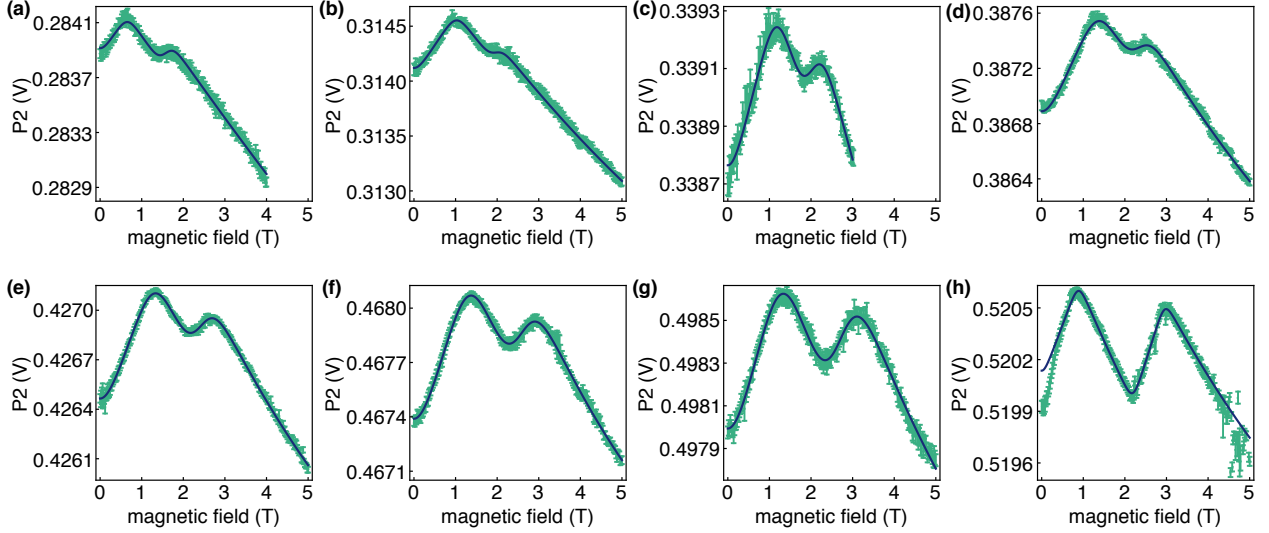


Figure 3.10: (a)-(h) Magnetospectroscopy results (green) across different gate tunings after registration of individual scans. Dark blue lines are fits to these data. Zero-magnetic-field spin splittings calculated from these scans are shown in Fig. 3.5(e).

are found to be linear and increasing with P2 gate voltage, as expected. These electric field results are used to define the electric field range in Fig. 3.6(b).

Figure 3.10 shows the extracted magnetospectroscopy curve from each tuning in Fig. 3.9. The zero-magnetic-field excited spin states calculated from the fits are shown in Fig. 3.5(e).

### 3.2.11 Appendix: Envelope functions for the tight-binding simulations

In this Appendix, we compute the envelope functions for the two lowest valley states shown in Fig. 3.6(a).

As noted in the main text and in Ref. [32], the wavefunction envelopes are modulated by fast oscillations, embodied in the factors  $\cos(k_0z + \varphi)$  or  $\sin(k_0z + \varphi)$ , where  $\pm k_0\hat{z}$  are the positions of the conduction valley minima in reciprocal space and  $\varphi$  is the valley phase. In the simplest case, both valley states have the same envelope. However, a single-atom Ge spike causes strong hybridization of the quantum well subband orbitals, resulting in very different envelopes for the two valley states. There is strong motivation for such hybridization

because the ground state can significantly minimize its energy by choosing a phase  $\varphi$  such that  $\cos(k_0z + \varphi) = 0$  at the location of the Ge spike, thus minimizing its potential energy. Consequently, the ground state does not “feel” the barrier, and its envelope takes the shape of an electron in a quantum well with no spike. The opposite is true for the excited valley state, since both valley states share the same  $\varphi$ ; in this case, the fast oscillations of the excited states are maximized at the location of the spike:  $\sin(k_0z + \varphi) = 1$ .

We can model the effect of valley-orbit coupling in this system as follows. The Hamiltonian for an electron in a quantum well, not including the Ge spike, is given by  $H_0 = -(\hbar^2/2m^*)\partial_z^2 - eEz + V_{\text{QW}}(z)$ , where  $m^*$  is the longitudinal effective mass for Si,  $E$  is the vertical electric field, and  $V_{\text{QW}}(z)$  is the quantum well confinement potential. We also consider a single-atom Ge spike potential, given by  $V_s(z) = v_s\delta(z - z_s)$ , where  $\delta(z - z_s)$  is a Dirac delta function describing the spike, centered at  $z = z_s$ . We must then solve the coupled set of Schrödinger equations [32]

$$\sum_{j=\pm 1} \alpha_j e^{ij(k_0z + \varphi)} (H_0 + V_s - \epsilon) F_j(z) = 0, \quad (3.15)$$

where  $(\alpha_-, \alpha_+)$  is the energy eigenvector and  $\epsilon$  is the energy eigenvalue. Normally, we would expect  $V_{\text{QW}}$  to be the source of the valley splitting; however, here, the effect of  $V_s$  is much stronger than  $V_{\text{QW}}$ , because it is located at a position where  $F_j(z)$  is a maximum. For an approximate solution, we therefore adopt  $V_s$  as the valley-splitting potential.

Normally,  $\alpha_-$ ,  $\alpha_+$ , and  $\varphi$  would be determined by explicitly diagonalizing Eq. (3.15). However, to a very good approximation, we already know that the solution is given by  $\alpha_{\pm} = 1/\sqrt{2}$  for the ground state and  $\alpha_{\pm} = \pm 1/\sqrt{2}$  for the excited state, with  $\varphi$  chosen such that  $\cos(k_0z_s + \varphi) = 0$ . Hence, we can write the (now) decoupled Schrödinger equations as

$$\sqrt{2} \cos(k_0z + \varphi) (H_0 + V_s - \epsilon) F_+(z) = 0, \quad (3.16)$$

$$\sqrt{2} \sin(k_0z + \varphi) (H_0 + V_s - \epsilon) F_-(z) = 0. \quad (3.17)$$

Because of the great difference in characteristic length scales associated with the fast oscillations in  $\cos(k_0z + \varphi)$  and the much slower variations of  $F_+(z)$ , we may treat them independently. (This is one possible statement of the effective mass approximation [109].) We therefore left-multiply the Schrödinger equations by  $\sqrt{2} \cos(k_0z + \varphi)$  or  $\sqrt{2} \sin(k_0z + \varphi)$  and integrate over a unit cell, to remove the fast oscillations, obtaining

$$(H_0 - \epsilon)F_+(z) = 0, \quad (3.18)$$

$$(H_0 + 2V_s - \epsilon)F_-(z) = 0. \quad (3.19)$$

These results are consistent with our previous claim that the ground state ( $F_+$ ) does not feel the spike, while the excited state ( $F_-$ ) feels a doubly tall barrier. Separately solving these two equations yields the envelopes shown in Fig. 3.6(a). The full tight-binding solutions, which are also shown in that figure, are very well described by these envelopes, demonstrating that the approximations used here are very good.

### 3.3 Quantum Hall measurements of the Ge spike heterostructure

In the previous section, we focused on quantum dot measurements and simulations to investigate the role of a germanium spike in the quantum well on the valley splitting. As mentioned, Hall bars were fabricated on this heterostructure and measured at low ( $< 50$  mK) temperatures. This section focuses on anomalous behavior of a Hall bar fabricated on this heterostructure in the quantum Hall regime.

#### 3.3.1 Anomalous Behavior in Quantum Hall Data

Figure 3.11 shows a measurement of the longitudinal and Hall resistance of the Hall bar, showing strong Shubnikov-de Haas oscillations (SdHO) and quantum Hall plateaus. Closer

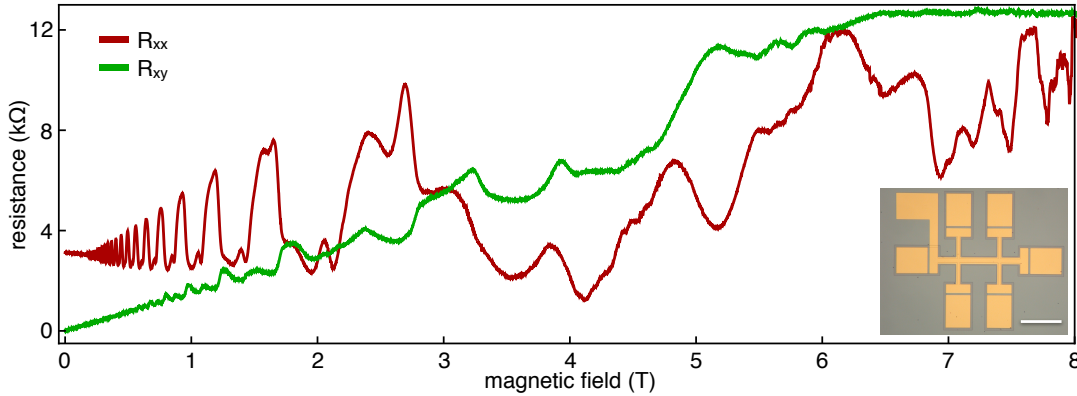


Figure 3.11: Sourcing 1 nA, the longitudinal and transverse resistances are measured on a heterostructure with a spike in germanium concentration within the silicon quantum well. For this measurement, the mobility is  $40,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  at a carrier density of  $4.25 \times 10^{11} \text{ cm}^{-2}$ . Both Shubnikov-de Haas oscillations and quantum Hall plateaus are clearly visible, but the SdHO do not trend towards lower resistance at larger magnetic field. The inset shows an optical image of the measured Hall bar with a  $200 \text{ }\mu\text{m}$  scale bar.

inspection, however, reveals several atypical features. First, despite the early onset of SdHO at low magnetic field, the minima at high magnetic field do not trend towards zero resistance. Between  $6.5\text{--}8 \text{ T}$ , the Hall resistance shows a wide plateau at  $\nu = 2$ , indicating quantization of the conduction channels across the Hall bar, yet the longitudinal resistance shows erratic behavior. Additionally, the Hall resistance shows significant ‘overshoot’ past the plateau resistances at lower magnetic field values. Finally, there appear to be SdHO minima which do not correspond to any integer filling factors.

To investigate this quantum Hall data, ‘fan diagrams’ of the Hall and longitudinal resistances were measured, shown in Fig. 3.12(a-b). These fan diagrams are measurements of the resistances as the carrier density and magnetic field are swept. The carrier density is modified by changing the top gate voltage. The Hall slope at low magnetic field is used to convert the changing top gate voltage into the carrier density axis as plotted in Fig. 3.12(a-b). The mobility calculated from this carrier density and the zero-magnetic-field longitudinal resistance is plotted in Fig. 3.12(c).

Fan diagrams, as their name suggests, show how the quantum Hall plateaus and SdHO minima linearly fan out towards higher field and carrier density. In Fig. 3.12(a), the Hall

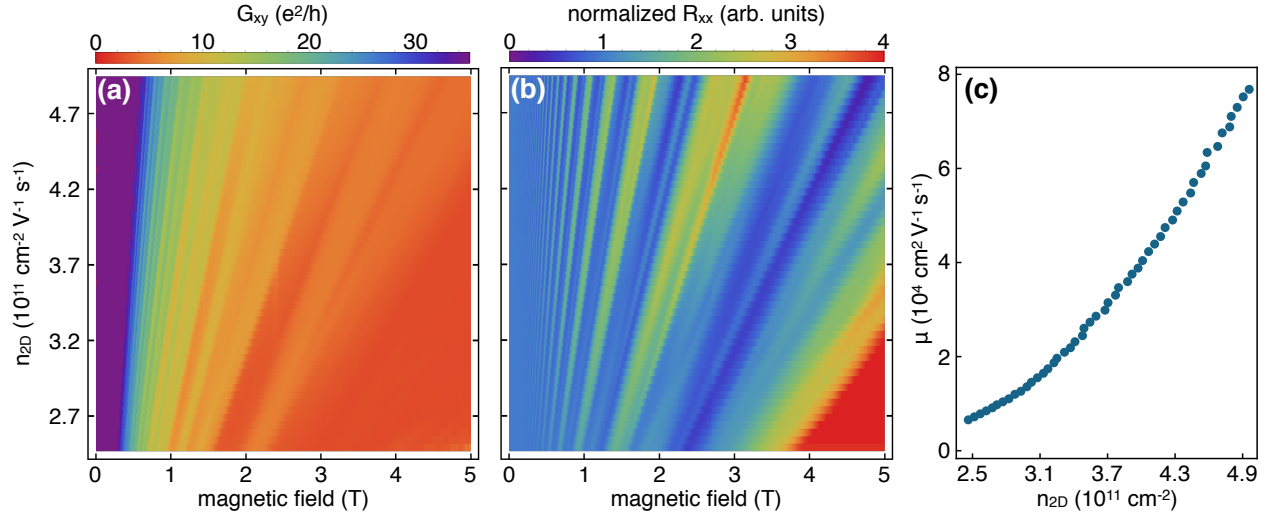


Figure 3.12: Hall conductance  $G_{xy} = 1/R_{xy}$  (a) and normalized longitudinal resistance (b) of the Ge spike heterostructure as a function of carrier density  $n_{2D}$  and magnetic field. Modifying the top gate changes the carrier density, shifting the magnetic field location of quantum Hall plateaus and SdHO minima. The Hall conductance, in units of  $e^2/h$ , should show large plateaus at integer values. In (b), the longitudinal resistance at each carrier density is normalized to the zero-magnetic-field value for better visibility of the oscillations. (c) Transport mobility calculated from the low magnetic field regions of the fan diagrams in (a) and (b). The calculated carrier density is used for the  $y$ -axes in (a) and (b).

conductance  $G_{xy} = 1/R_{xy}$  is plotted in units of  $e^2/h$  so that plateaus occur at integer values. In an ideal sample, the conductance should decrease from left to right in steps corresponding to each integer quantum value. The overshoots are clearly visible in Fig. 3.12(a), as the conductance oscillates up and down in the 1 – 4 T region. The longitudinal resistance fan diagram in Fig. 3.12(b) shows SdHO minima at integer filling factors. However, at high magnetic field, there are more ‘features’ of minima and plateaus than would be anticipated. Clearly, the behavior of these fan diagrams requires more detailed investigation.

Figure 3.13 shows three horizontal line cuts of Fig. 3.12(b) plotted in inverse magnetic field. Figure 3.13(a-c) correspond to  $n_{2D} = 3.0 \times 10^{11} \text{ cm}^{-2}$ ,  $n_{2D} = 4.0 \times 10^{11} \text{ cm}^{-2}$ , and  $n_{2D} = 5.0 \times 10^{11} \text{ cm}^{-2}$ , respectively. As described in Sec. 2.3.2, the SDHO minima are evenly spaced in inverse magnetic field. Following Eq. (2.13), higher carrier density corresponds to faster oscillations.

Select integer filling factors are plotted as vertical lines in Fig. 3.13. The red lines denote

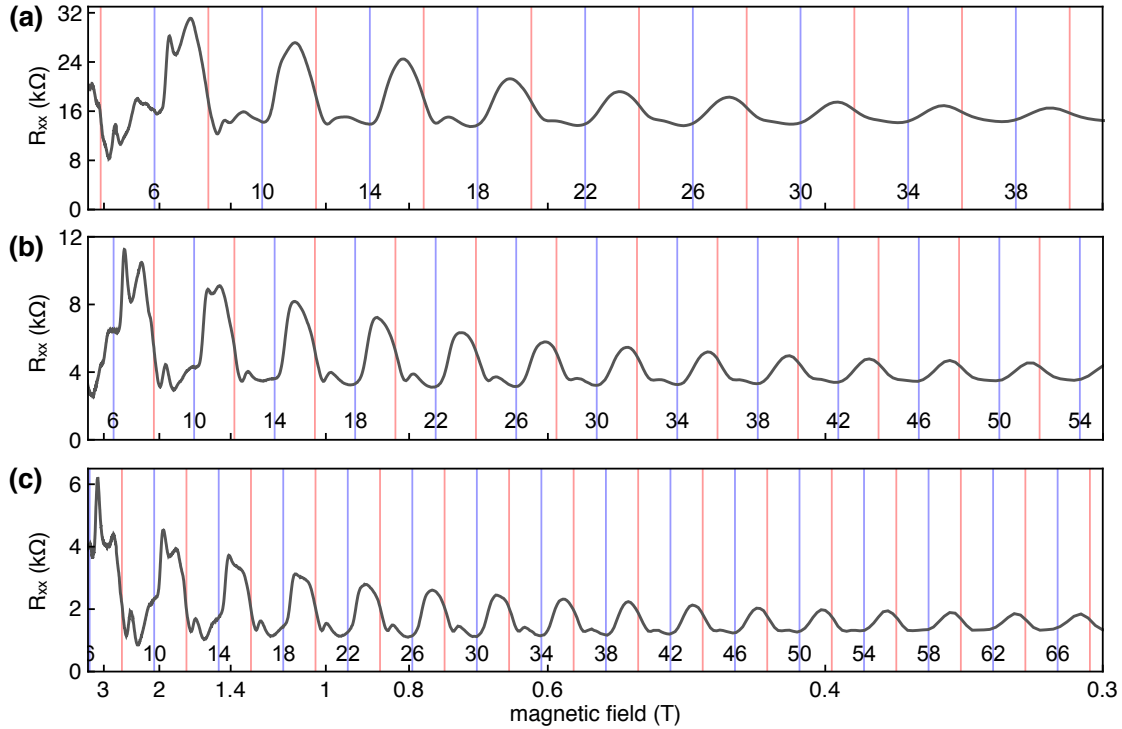


Figure 3.13: Longitudinal resistance plotted in inverse magnetic field for  $n_{2D} = 3.0 \times 10^{11} \text{ cm}^{-2}$  (a),  $n_{2D} = 4.0 \times 10^{11} \text{ cm}^{-2}$  (b), and  $n_{2D} = 5.0 \times 10^{11} \text{ cm}^{-2}$  (c) in Fig. 3.12. The vertical colored lines are placed at the expected SdHO minima given by the calculated carrier densities. The red lines correspond to the orbital filling factors and the blue lines (labeled with the filling factor number  $\nu$ ) correspond to the spin filling factors. The periodicity of the SdHO match the expectation from the calculated carrier densities but the deepest minima, particularly at low magnetic field, correspond to the spin filling factors instead of the orbital filling factors.

$\nu = 4n$  while the blue lines denote  $\nu = 4n + 2$ , where  $n$  is an integer. Given the presence of both spin and valley splitting in silicon quantum wells, the orbital Landau level splittings correspond to every fourth integer filling factor (red lines). In Sec. 3.1.2, we described how the spin splitting of the Landau levels is  $\sim 5 \times$  smaller than the orbital Landau level splitting. As these splittings increase with magnetic field, the oscillations present at small magnetic field should correspond to the orbital Landau level splitting. However, as shown in Fig. 3.13, the lowest magnetic field oscillations (towards the right) occur at  $\nu = 4n + 2$ , which should be the spin splitting. The periodicity of the oscillations (and the colored filling factor lines) are determined by the carrier density according to Eq. (2.13). The placement of the filling factor

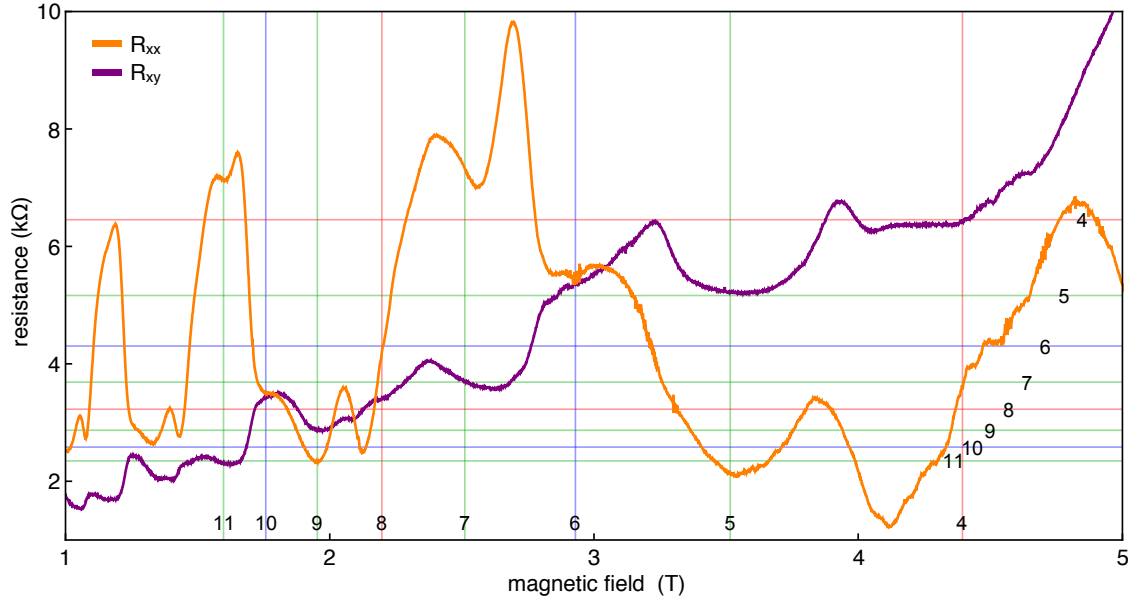


Figure 3.14: Using the data from Fig. 3.11, the filling factors  $\nu$  are labeled for the transverse and longitudinal resistances. The horizontal lines are placed at the expected resistance values of the quantum Hall plateaus while the vertical lines are placed at the expected magnetic field values for the SdHO minima given the calculated carrier density  $n_{2D} = 4.25 \times 10^{11} \text{ cm}^{-2}$ . The red lines correspond to the orbital splitting filling factors, the blue lines correspond to the spin splitting filling factors, and the green lines correspond to the valley splitting filling factors. The quantum Hall plateaus match the expected values relatively well, especially at high magnetic field. The SdHO minima match well for the valley filling factors (green) and the spin filling factors (blue), but not for the orbital filling factors (red).

lines match the carrier density as calculated from the Hall resistance slope at low magnetic field and the periodicity assuming  $\nu = 4n + 2$  minima. The spacing of the filling factor lines cannot be adjusted for the minima to properly correspond to  $\nu = 4n$  orbital Landau level splittings. This effect of the lowest magnetic field splittings corresponding to  $\nu = 4n + 2$  filling factors is independent of carrier density, as the three data sets in Fig. 3.13 show. The  $\nu = 4n$  orbital Landau level filling factors do not appear to align with any minima, even at high magnetic field. At higher magnetic field, the odd filling factor minima appear, which correspond to the valley splitting.

Focusing on higher magnetic field, we can confirm that our placement of the filling factor lines is correct. Figure 3.14 shows both the longitudinal and the Hall resistance in the 1–4 T range for  $n_{2D} = 4.25 \times 10^{11} \text{ cm}^{-2}$ . The vertical lines show where the orbital (red), spin (blue),

and valley (green) filling factor minima should be positioned. Additionally, the quantized Hall resistance values  $h/(ne^2)$  are plotted as horizontal lines, with the colors corresponding to the same fillings as the vertical lines. The  $\nu = 4$  plateau in the Hall resistance is clearly visible, and the resistance at the odd filling factors match well to the expected values. The agreement between the longitudinal resistance minima and the Hall resistance plateaus, especially at odd filling factors, supports the interpretation of the minima-to-filling factor correspondence. At this higher magnetic field range, the ‘misalignment’ of the  $\nu = 4$  orbital filling factors is apparent. For both  $\nu = 4$  and  $\nu = 8$ , a deep SdHO minimum exists at a magnetic field lower than expected for the orbital filling factor. Near  $\nu = 4$ , a quantum Hall plateau aligns with this minimum, and matches the expected resistance. Clearly, there is a ‘disagreement’ between the orbital filling factors and the spin and valley filling factors.

### 3.3.2 Possible Origins of Anomalous Behavior

The origins of these aberrant phenomena is not fully understood. We discuss several possible explanations of these effects. Frequency ‘beating’ of SdHO minima has been shown in systems with strong spin-orbit coupling [110]. Multiple SdHO periodicities have been measured in a sample with two populated electric subbands [111]. Destruction of certain filling factor minima has been observed in a coupled double-well heterostructure [112]. In this heterostructure, however, we do not have a large spin-orbit coupling, as evidenced by the  $g \approx 2$  value of the electron  $g$ -factor measured in Sec. 3.2.9. Additionally, there is no reason for multiple subbands to be populated in a silicon quantum well. Finally, while the Ge spike heterostructure could be considered a double-well, the thickness of the silicon layer above the Ge spike is too narrow for sufficient localization entirely within the mini-well. The effect of filling factor minima destruction found in double-well heterostructures increased with well separation and isolation. In this heterostructure, the spike in germanium concentration is very thin, and the electron wave function is spread over both wells.

Some of the unexplained behavior of the longitudinal and Hall resistances appear as

‘cross-talk’ between the two measurements. The SdHO minima do not trend towards zero at high magnetic field, and the Hall resistance shows strong oscillations between the plateaus. Here, we consider a secondary channel of classical conduction, either due to cap-filling of the silicon at the surface of the heterostructure or the thin silicon layer above the germanium spike. Although we earlier discussed that the electron wave function is shared between the two silicon layers, we propose that conduction through the thinner layer may behave differently. We treat this second channel of conduction classically, meaning that it does not exhibit quantum Hall behavior.

The longitudinal resistivity of the main quantum channel of conduction is calculated using the approach described in Sec. 2.3.2. For the Hall resistivity, we assume a linear Hall slope in magnetic field between integer quantum Hall plateaus aligned to the SdHO minima of the longitudinal resistivity. The conductivity matrix of the ‘main’ channel,  $\sigma_1$ , is calculated as the inverse of the resistivity matrix. A second classical conduction channel is calculated, in which the Hall resistivity is linear in magnetic field and the longitudinal resistivity is flat. The conductivity matrix of this secondary classical channel,  $\sigma_2$ , is similarly calculated as the inverse of its resistivity matrix. We then add these conductivity matrices together, and calculate the inverse to achieve the resistivity matrix of the entire system:  $\rho_{total} = (\sigma_1 + \sigma_2)^{-1}$ . Adding the conductivities of these two channels together and calculating the total resistivity will mix the longitudinal and transverse components. The results are shown as the gray lines in Fig. 3.15. The main quantum channel has a carrier density  $n_{2D} = 4.00 \times 10^{11} \text{ cm}^{-2}$  and a transport mobility  $\mu = 50,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ . The second classical channel has a  $5\times$  smaller carrier density and mobility. The mixing between conduction channels results in the SdHO minima trending towards a non-zero value, similar to the experimental data shown in blue. The change in the Hall resistance is more subtle for the input parameters, but there are some small oscillations present around 1 T. Additionally, the Hall slope at very low magnetic field is mostly unaffected, reflecting the slope (and carrier density) for the quantum channel alone.

From this modeling, we show that some of the behavior we see experimentally, such as

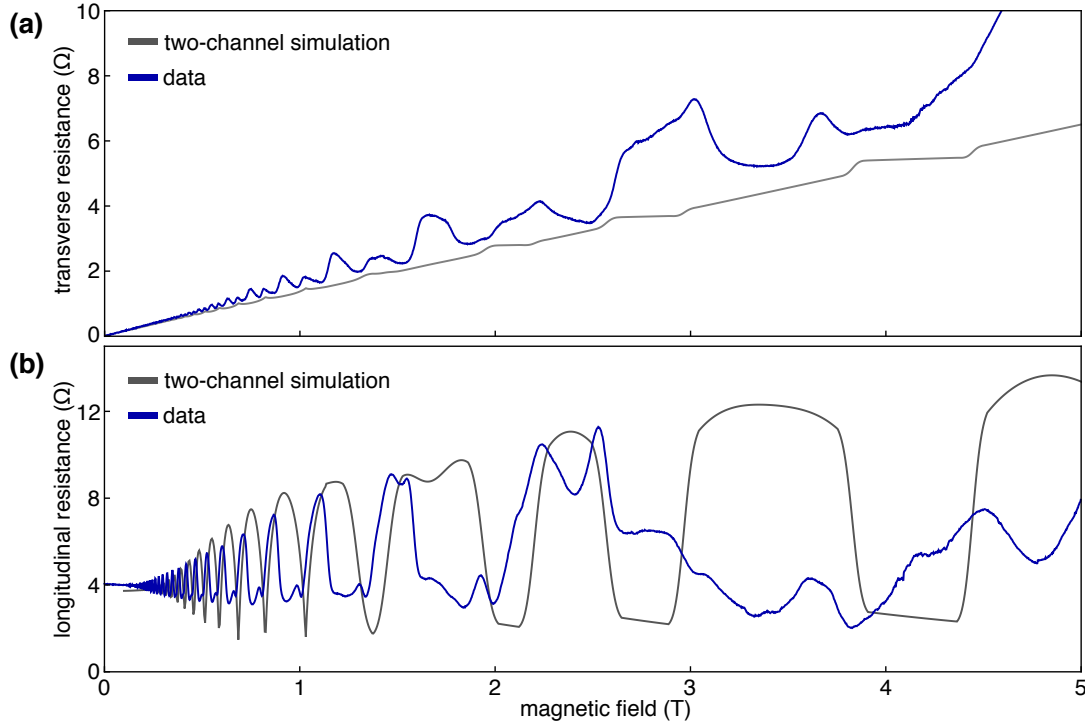


Figure 3.15: Using the Hall bar simulation method described previously in Sec. 2.3.2, a secondary classical conduction channel is added to a main quantum conduction channel. The conductance matrices of the two channels are added together and the total resistivity is calculated. The gray curves show the transverse (a) and longitudinal (b) resistances of this two-channel model. The main channel has a carrier density  $n_{2D} = 4.00 \times 10^{11} \text{ cm}^{-2}$  and a mobility  $\mu = 50,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ . The extra conduction channel has a  $5\times$  smaller carrier density and mobility. Comparing this to a real dataset with the same calculated carrier density (blue), we see that adding a second channel does reproduce the effect that no minima reach zero resistance. We also see some cross-talk effects in each of the two resistances. However, the unexpected depth and location of minima found experimentally cannot be reproduced with a secondary classical channel.

the lack of deep SdHO minima and oscillations in the Hall resistance, could be explained by a secondary channel of classical conduction. However, the location and relative strengths of the SdHO cannot be explained by a second classical channel. An alternative origin of these effects, which is difficult to justify or explore, could be disorder across the length or width of the Hall bar. Pockets of varying carrier density could explain some of the strange minima behavior. Reliable measurements were only acquired in a single Hall bar device. It is possible that these phenomena would not be present in other measured Hall bars with different or less disorder. Finally, we note that strong valley-orbit coupling, which may be present in this

heterostructure due to the presence of the spike in germanium, could potentially produce some of these phenomena. Due to the focus of this work on valley splitting, we did not investigate this Hall bar behavior further.

## **3.4 The Wiggle Well: enhancing valley splitting by oscillating the germanium concentration in silicon quantum wells**

### **3.4.1 Introduction**

Quantum dots in silicon quantum wells of silicon-germanium heterostructures are a promising candidate for quantum computing, but the near-degeneracy of the two low-lying valley states in silicon can pose challenges to qubit formation [14, 32, 40–42, 95]. In Si/SiGe heterostructures, the valley splitting can vary widely due to heterostructure design and unintentional defects, typically tens to a few hundred  $\mu\text{eV}$  [19–30]. The small size and intrinsic variability of the valley splitting has motivated several approaches to modify or tune its value. The valley splitting can be tuned after device fabrication through changes to the applied vertical electric field [26, 98, 99] or by changing the lateral dot position [21, 27, 29]. The Si/SiGe heterostructure has also been modified in attempts to enhance the valley splitting. Introducing additional germanium at the quantum well interface does not significantly modify the valley splitting [25]. However, a single spike in germanium concentration within the quantum well has been studied both theoretically and experimentally, showing that the valley splitting should double due to the inclusion of the Ge spike [30].

Here, we report a novel Si/SiGe heterostructure, the Wiggle Well, with an oscillatory concentration of germanium in the quantum well to increase the valley splitting. The wavevector defined by these oscillations couples the valleys in silicon. Depending on the magnitude of this wavevector, valleys are either coupled within a single Brillouin zone or between different

zones. We grow a Wiggle Well heterostructure by chemical vapor deposition (CVD) with an oscillating Ge concentration in the quantum well between 0% and 9% and a wavelength of 1.8 nm. We find a low temperature transport mobility of this heterostructure in the range of  $1\text{-}3 \times 10^4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ . We fabricate quantum dot devices and present stable dot behavior. We experimentally measure the valley splitting in a singly occupied quantum dot using pulsed-gate spectroscopy and report a valley splitting that is both large and tunable in the range of 54-239  $\mu\text{eV}$ . We analyze both the role of the Ge oscillations and the random placement of the Ge atoms within the quantum well.

### 3.4.2 Wiggle Well Theory

The Wiggle Well heterostructure design is shown schematically in Fig. 3.16(a). The typical pure-silicon quantum well is replaced by an oscillating concentration of silicon and germanium. These oscillations are sinusoidal, as shown in Fig. 3.16(b), between pure silicon and SiGe alloy. The wavelength,  $\lambda$ , of this oscillation is shown and relates to the wavevector,  $q$ , by  $q = 2\pi/\lambda$ .

For a standard Si/SiGe heterostructure, the valley states are split by interactions between the electronic wave functions and barrier interfaces in the quantum well. For the Wiggle Well, an additional contribution to the valley splitting arises from the oscillations of the Ge concentration within the quantum well itself. These oscillations create a potential energy term in the Hamiltonian of the form  $V_{osc} = V_0 \cos(qz)$ , where  $z$  is the distance from the barrier in the direction of growth. This acts as a perturbation on the wavefunctions  $\phi_{\pm}(\vec{r})$  for the valleys centered on the points  $\vec{k} = \pm(0, 0, k_0)$  where  $k_0$  is  $0.84(2\pi/a_0)$  and  $a_0 = 0.543$  nm is the lattice constant. The unperturbed wavefunctions are

$$\phi_{\pm}(\vec{r}) = \psi(z)e^{\pm ik_0 z} \sum_{\vec{K}} c_{\pm}(\vec{K}) e^{i\vec{K} \cdot \vec{r}}, \quad (3.20)$$

separated into an envelope function  $\psi$  and the Bloch functions. The  $\vec{K}$  are reciprocal lat-

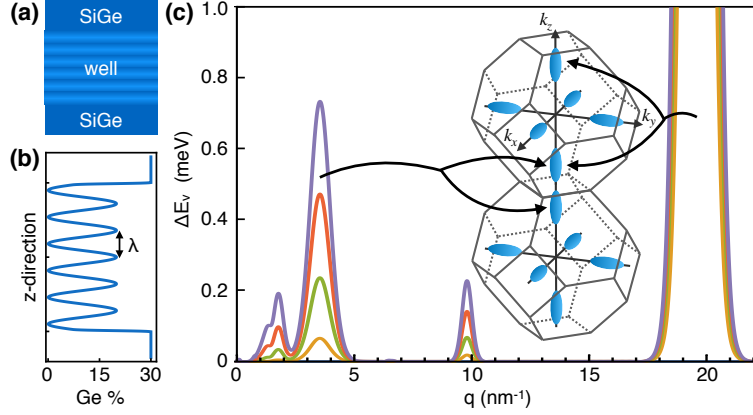


Figure 3.16: (a) Schematic of the Wigggle Well heterostructure, showing Ge oscillations throughout the quantum well. The darker regions have higher Ge concentration. (b) Plot of the sinusoidal Ge concentration for a heterostructure with an average of 10% Ge in the quantum well. The oscillation wavelength,  $\lambda$ , is related to the wavevector by  $q = 2\pi/\lambda$ . (c) The contribution to the valley splitting  $\Delta E_v$  due to a sinusoidal Ge concentration in the quantum well as a function of the wavevector  $q$ . The orange, green, red, and purple curves correspond to average Ge concentrations in the well of 5%, 10%, 15%, and 20%, respectively. The inset schematic shows two neighboring Brillouin zones in the silicon conduction band with constant energy surfaces around the valley minima represented by blue ellipsoids. The peaks at  $q \approx 3.5$  correspond to an Umklapp coupling between the  $z$ -valleys of neighboring Brillouin zones. The peaks at  $q \approx 20$  correspond to the typical coupling between  $z$ -valleys within a single zone. The tops of the peaks at this wavevector lie between 7-23 meV and are shown in Fig. 3.19 in Sec. 3.4.8.

tice vectors and the  $c_{\pm}(\vec{K})$  are expansion coefficients of the cell-periodic part of the Bloch function. The valley splitting  $\Delta E_{VS}$  caused by the added Ge is then [113]

$$\Delta E_{VS} = 2 |\langle \phi_+ | V(z) | \phi_- \rangle| = 2 \left| \sum_{\vec{K}, \vec{K}'} c_+^*(\vec{K}) c_-(\vec{K}') \delta_{K_x, K'_x} \delta_{K_y, K'_y} I(K_z - K'_z) \right|, \quad (3.21)$$

where the last factor stands for the integral

$$I(K_z - K'_z) = \int_{-\infty}^0 |\psi(z)|^2 e^{iQz} V_0 \cos(qz) dz, \quad (3.22)$$

with  $Q = K_z - K'_z - 2k_0$ .  $|\psi(z)|^2$  is a smooth function with a single peak so its Fourier

transform has a single peak at zero wavevector. Hence,  $I(K_z - K'_z)$  will peak strongly when

$$q = \pm Q = \pm(K_z - K'_z - 2k_0). \quad (3.23)$$

The sum over reciprocal lattice vectors in Eq. (3.21) means there are multiple peaks in  $\Delta E_{VS}(q)$ , one every time the condition  $K_z - K'_z = \pm(q \pm 2k_0)$  is satisfied.

Figure 3.16(c) shows the valley splitting due to Ge oscillations in the quantum well as a function of wavevector  $q$ . Each curve corresponds to a different average Ge concentration within the well. This valley splitting is calculated through an estimation of the plane wave expansion coefficients for this heterostructure, with the sum in Eq. (3.21) reduced to six reciprocal lattice vectors [114]. A vertical electric field is applied with a magnitude of  $0.1 \text{ V nm}^{-1}$  to determine the envelope  $\psi$ .

The inset schematic in Fig. 3.16(c) shows two neighboring Brillouin zones for silicon. The valley splitting enhancement at  $q \approx 3.5$  ( $\lambda = 1.8 \text{ nm}$ ) is due to a coupling across two zones, as labeled by the arrows. A much larger enhancement can be achieved by creating an oscillation with a much shorter  $0.32 \text{ nm}$  wavelength, as shown by the  $q \approx 20$  peak. This is caused by the coupling between the  $z$ -valley states within a single Brillouin zone, as is typical for sharp heterostructure interfaces. The smaller peak at  $q \approx 10$  is a harmonic that may arise from finite-size effects in the calculation, while at small  $q$  there is noise due to sensitivity to the details of the barrier interface.

### 3.4.3 Experimental Methods

Figure 3.17(a) shows a scanning transmission electron micrograph of a Wiggle Well heterostructure grown by chemical vapor deposition (CVD). In this growth, alternating layers of silicon and silicon-germanium are grown on a silicon substrate, to fine-tune the oscillation wavelength prior to real heterostructure growth. The wavelength shown in Fig. 3.17(a) is  $\lambda \approx 1.7 \text{ nm}$ . Based on this result, the growth parameters are adjusted slightly to achieve the

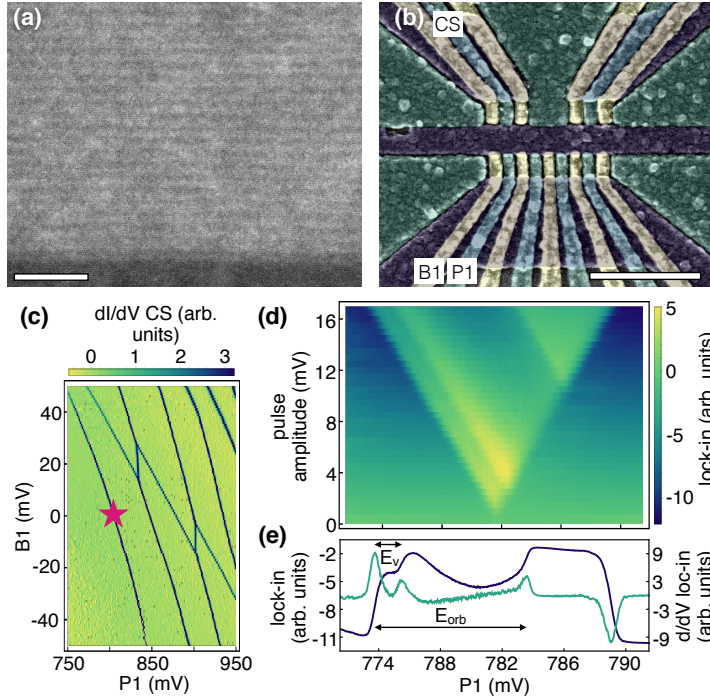


Figure 3.17: (a) High-angle annular dark-field (HAADF) image of a test structure grown on a Si substrate, with a 10 nm scale bar. The brighter regions represent higher Ge concentration. The oscillation wavelength for this test is  $\approx 1.7$  nm. (b) False-colored scanning electron micrograph of a quantum dot device identical to the one measured, with a 500 nm scale bar. The different colors (blue, green, yellow) indicate different gate layers. (c) Stability diagram of a quantum dot formed under the leftmost plunger gate in the lower channel, charge sensed by a quantum dot charge sensor in upper left channel. The gates used for this figure are labeled in (b). Most measurements presented here are performed at the last (leftmost) electron transition in this dot, near the magenta star. (d) Pulsed-gate spectroscopy of a singly-occupied quantum dot. The 0-1 electron charging transition in P1 is swept as the amplitude of a 2 kHz square wave is increased, revealing the characteristic V-shape in a charge sensor lock-in measurement. (e) An averaged line-cut of (d) at a 16 mV pulse amplitude. The blue curve is the lock-in response and the green curve is a differentiation, showing peaks at the loading lines of the energy states. The valley and orbital splittings  $E_v$  and  $E_{orb}$  are labeled with arrows. These voltage splittings are converted to energy splittings with a thermally-measured lever arm.

desired 1.8 nm oscillation period. A new heterostructure is then grown on a linearly graded SiGe alloy with a final concentration of  $\text{Si}_{0.705}\text{Ge}_{0.295}$ . After a 550 nm layer of  $\approx 30\%$  Ge alloy, a quantum well with 5 periods of 0-9% Ge oscillations is grown, followed by another 60 nm of 30% Ge alloy and a 1 nm Si cap. Further growth details can be found in Sec 3.4.9. This growth best matches the orange curve in Fig. 3.16(c) at the  $q \approx 3.5$  peak, where the

valley splitting contribution due to the oscillations is  $\approx 82 \mu\text{eV}$ .

Hall bar and quantum dot devices were fabricated simultaneously on this heterostructure. A 20 nm layer of aluminum oxide grown by atomic layer deposition isolates the Hall bar top gate from the surface of the heterostructure. Hall measurements performed at  $\sim 2$  K show a mobility in the range of  $1\text{--}3 \times 10^4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  across an electron density range of  $2\text{--}6 \times 10^{11} \text{ cm}^{-2}$  (see Sec. 3.4.10). For the quantum dots, the gates are separated from the heterostructure surface by a 5 nm layer of aluminum oxide in a  $30 \mu\text{m}$  square around the dot region and a 20 nm layer elsewhere. Following the procedures described in Ref. [46], the gate design has three layers of overlapping aluminum isolated from one another by the self-oxidation of the aluminum metal, enhanced by an oxygen plasma ash.

A false-colored scanning electron micrograph of a device identical to the one measured is shown in Fig. 3.17(b). Each color: blue, green, and yellow, is a single layer of gates. For this publication, the left half of the device is used. The upper left channel is used as a quantum dot charge sensor for dots formed in the bottom channel.

Figure 3.17(c) shows a stability diagram of dots formed under or near the leftmost plunger gate (green layer) in the main channel. The majority of the dot measurements presented are performed using the last (leftmost) electron transition in this figure, near the magenta star. All dot measurements are performed in a dilution refrigerator with a base temperature below 50 mK.

The excited state spectrum of a singly occupied quantum dot is measured here by pulsed-gate spectroscopy [29, 52, 85–88], shown in Fig. 3.17(d). A square wave voltage is applied to the plunger gate of a dot at a frequency comparable to the tunnel rate to the electron reservoir. The charge sensor current is measured with a lock-in amplifier referenced to the fundamental frequency of the square wave. When the DC voltage of the gate is swept over the dot transition, the electron is loaded and unloaded into the dot as the dot's chemical potential, split by the square wave, straddles the fermi level of the reservoir. As the amplitude is increased, additional states such as the excited valley state and excited orbital state can

be loaded during the high voltage period of the wave, modifying the tunnel rate into the dot. These changes in tunnel rate lead to a changing lock-in response.

Figure 3.17(e) shows a highly-averaged line-cut of the data in Fig. 3.17(d) at a 16 mV square wave amplitude. The green curve is a numerical differentiation of the raw data in blue. The smaller valley splitting  $E_v$  and the larger orbital splitting  $E_{orb}$  are labeled with arrows. These peaks in the differentiated signal are fit to extract the voltage splittings using the methods described in Ref. [29]. The voltage splittings are then converted into energy splittings using a thermally-measured lever arm (see Sec. 3.4.11).

### 3.4.4 Experimental Results

Valley and orbital splittings are measured using pulsed-gate spectroscopy in two separately formed quantum dots, one under B2 and the other under P1 (labeled in the upper left inset of Fig. 3.18(a)). In the B2 formed dot, at two different voltage tunings of the surrounding gates, the valley splitting is tuned from 80 to 140  $\mu\text{eV}$  and the orbital splitting is tuned from 810 to 890  $\mu\text{eV}$ . For the P1 dot, more extensive measurements are performed and the dot is tuned in two distinct ways.

In one tuning scheme, following the method outlined in Ref. [29], the dot's lateral position is intentionally moved by asymmetrically changing the screening gate voltages. These gates, S1 and S2, shown schematically in the upper left inset to Fig. 3.18(a), are tuned in opposite directions so that the dot moves closer to the more positive gate and further away from the more negative gate. This has the added effect of changing the shape of the orbital in the plane of the 2DEG. The purpose of this tuning scheme is to change how and where the dot's wave function interacts with alloy disorder within the well or steps at the quantum well interface. The valley splitting results of this tuning scheme are shown in the filled diamond points in Fig. 3.18(a) as a function of the asymmetry of the screening gate voltages. Across these points, the plunger gate voltage is kept relatively constant between 905 and 915 mV. The orbital splitting is represented by the color of the points and shown in the legend at the

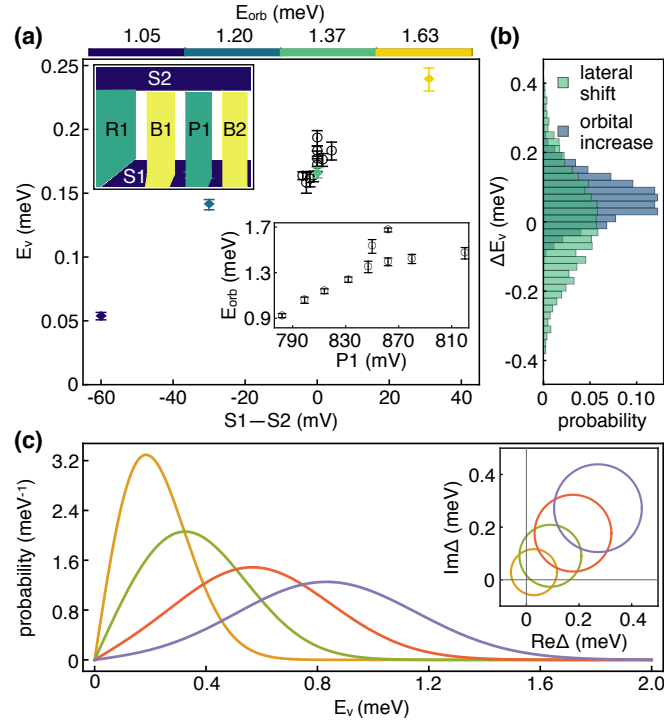


Figure 3.18: (a) Valley splitting  $E_v$  of the P1 quantum dot as a function of the screening gate asymmetry S1–S2 (gate schematic shown in the upper left inset). By shifting the balance between S1 and S2 (filled diamonds), the dot position is shifted between the two gates and  $E_v$  is tuned by a factor of 4. Alternatively, the screening gates are tuned in the same direction (open black circles), changing the lateral confinement and vertical electric field while maintaining the dot position. The valley splitting tuning by this method is small. For the filled diamonds, the orbital splitting  $E_{orb}$  is shown in the legend above. For the open black circles,  $E_{orb}$  is shown as a function of P1 in the lower right inset. (b) Distribution of the valley splitting change  $\Delta E_v$  from dot tuning, calculated in 2000 one-dimensional tight-binding simulations containing atomistic alloy disorder. To estimate the change due to shifting the dot (green),  $E_v$  is calculated at two lateral positions separated by 20 nm, with a lateral confinement  $\hbar\omega = 1.3$  meV. To estimate the change due to squeezing the dot (blue),  $E_v$  is calculated with  $\hbar\omega = 0.9$  meV and again with  $\hbar\omega = 1.7$  meV. (c) Probability distribution for the total valley splitting in a quantum well with a 1.8 nm period Ge oscillation, assuming atomistic alloy disorder. The orange, green, red, and purple curves correspond to average Ge concentrations in the well of 5%, 10%, 15%, and 20%. The inset shows the standard deviation of the valley splitting contribution in the complex plane due to alloy disorder, offset from zero by the valley splitting of the Ge oscillations calculated in Fig. 3.16(c). The main figure in (c) shows Rician distributions of the inset.

top of the figure. Here, low to high orbital splitting corresponds with low to high voltage on gate S1, from -180 to -135 mV (S2 is tuned from -120 to -165 mV). As shown, this tuning scheme leads to a wide range in valley splitting.

In the other tuning scheme, following the method outlined in Ref. [30], the dot's lateral position is kept constant while the confinement and vertical electric field are changed. This is achieved by tuning the screening gates, S1 and S2, by a voltage depending on their lever arm to the dot. The voltages are tuned 'symmetrically' such that the voltage change on each gate affects the dot equally. Making both gate voltages increasingly negative forces the electron transition to a more positive voltage on the plunger gate, P1. As shown in Ref. [30], this has the effect of increasing the lateral confinement and the vertical electric field at the quantum dot. The orbital splitting for this tuning method is shown in the inset of Fig. 3.18(a), plotted as a function of P1. The orbital splitting is largely tunable and generally tracks with increasing P1, as expected. As the screening gates have nearly identical lever arms to the dot, the difference in voltage between S1 and S2 is small across all tunings. The valley splitting results of this tuning scheme are shown by the open circles in Fig. 3.18(a) as a function of the S1 - S2 difference. In this tuning scheme, the valley splitting is relatively stable compared to the change from moving the dot.

### 3.4.5 Tight-Binding Simulations and Alloy Disorder

To validate our interpretation of the differences between these two tuning schemes, we replicate them using one-dimensional (1D) tight-binding simulations [98]. A set of 2000 three-dimensional heterostructures with atomistic alloy disorder are generated. Each heterostructure has a lateral size of  $100 \times 120$  nm, and each lattice site is populated by either Si or Ge atoms, probabilistically chosen by the expected concentrations for each layer. The valley splitting is calculated by averaging over a lateral area given by the orbital splitting and performing a 1D tight-binding simulation on the resulting averaged alloy concentration along the growth direction.

To replicate the lateral shift tuning, this calculation is performed at two averaged locations separated by 20 nm with a lateral confinement of  $\hbar\omega = 1.3$  meV. The size of the lateral shift is chosen by adapting the lateral movement calculated in Ref. [29] to the change

in screening gate voltages reported in Fig. 3.18(a). The valley splitting difference between the two calculated points of these 2000 iterations is shown as a probability distribution in Fig. 3.18(b) by the green bars. Naturally, this distribution is centered around  $\Delta E_v = 0$ , but has a wide distribution. This nicely matches the large changes in valley splitting we see in the colored points in Fig. 3.18(a).

To replicate the change in lateral confinement, these 1D tight-binding calculations are repeated, and the lateral confinement is changed from 0.9 to 1.7 meV while maintaining the dot's position. These results are shown in the blue bars in Fig. 3.18(b). For this tuning, the increase in orbital confinement results in a high probability of a small increase in the valley splitting. Similar to the open black circle points in Fig. 3.18(a), the expected valley splitting change is much smaller than the change due to lateral movement.

Tuning the valley (or singlet-triplet) splitting of a Si/SiGe quantum dot through gate voltage changes has been reported several times [21, 26, 27, 29, 30]. Notably, these previous investigations have shown valley splitting tunability of 15% with a maximum  $E_{VS} = 213 \mu\text{eV}$  [27] or 140% tunability with a maximum  $E_{VS} = 87 \mu\text{eV}$  [29]. Here, we show  $> 440\%$  tuning of the valley splitting with a maximum  $E_{VS} = 239 \mu\text{eV}$ . The large maximum value of the valley splitting is supported by the predicted  $\approx 82 \mu\text{eV}$  contribution from the Ge oscillations.

As Fig. 3.18(b) shows, alloy disorder can significantly modify the valley splitting measured in a quantum dot. The potential  $V(z)$  in Eq. (3.21), which couples the valley states and creates the valley splitting, can be separated into a term due to the expected heterostructure potential  $V_1(z)$  and a term due to alloy disorder  $V_2(z)$ . The valley splitting can then be separated into two components,  $E_{VS} = 2|\Delta^{(1)} + \Delta^{(2)}|$ . We can write the term due to alloy disorder as

$$\Delta^{(2)} = \frac{a_0}{4} \frac{\Delta E_c}{1 - x_b} \sum_{l=1}^{n_l} e^{2ik_0 z_l} (x_l - \bar{x}_l) |\Psi(z_l)|^2 \quad (3.24)$$

where  $\Delta E_c$  is the conduction band offset of the SiGe barrier,  $x_b$  is the Si concentration of the barrier, the sum is over the layers in the well,  $x_l$  is the Si concentration in layer  $l$ , and  $\bar{x}_l$  is the expected Si concentration in that layer. Given an expected Si concentration throughout

the well, we can estimate the variance within a layer, assuming a binomial distribution. The valley splitting due to the expected potential,  $\Delta^{(1)}$ , is fixed, so the variance in the valley splitting is purely due to the alloy disorder. For a lateral dot size  $A$ , the valley splitting variance is

$$\mathbb{V}[E_{VS}] = \left( \frac{a_0}{4} \frac{\Delta E_c}{1 - x_b} \right)^2 \frac{a_0^2}{2A} \sum_{l=1}^{n_l} \bar{x}_l (x_l - \bar{x}_l) |\Psi(z_l)|^4. \quad (3.25)$$

The inset to Fig. 3.18(c) shows the standard deviations of the calculated valley splitting distributions due to alloy disorder in the complex plane. These Gaussian distributions are offset from zero by the contribution to the valley splitting of the oscillations, calculated from the  $q \approx 3.5$  results shown in Fig. 3.16(c). The probability curves shown in the main figure of Fig. 3.18(c) are Rician distributions of the results in the inset. As the concentration of germanium within the well increases, the average valley splitting increases, as does the probabilistic spread. The higher valley splitting results within each distribution can be considered alloy disorder which matches the  $q \approx 20$  wavevector. The orange curve in Fig. 3.18(c) is most similar to the heterostructure measured, showing an expected mean valley splitting of  $E_v \approx 230 \mu\text{eV}$ .

### 3.4.6 Conclusions

In conclusion, we have presented a new heterostructure with an oscillatory concentration of germanium within the quantum well. We presented a theoretical basis for how the Wiggle Well strongly couples the  $z$ -valley states in neighboring Brillouin zones or within a zone to increase the valley splitting. We reported experimental growth of a heterostructure with a 1.8 nm period Ge oscillation within the quantum well and presented Hall and quantum dot measurements in this heterostructure. We presented pulsed-gate spectroscopy of the excited state spectrum of a single-electron quantum dot and showed a large and widely tunable valley splitting through simple gate voltage changes. We supported this tunability with one-dimensional tight-binding calculations. We combined these calculated valley splitting

enhancements with an estimation of the alloy disorder to describe an expected distribution of the valley splittings in disordered heterostructures. The Wiggle Well is shown to be a viable strategy for valley splitting enhancement of Si/SiGe quantum dots.

### 3.4.7 Acknowledgments

This research was sponsored in part by the Army Research Office (ARO), through Grant Number W911NF-17-1-0274 and the Vannevar Bush Faculty Fellowship program sponsored by the Basic Research Office of the Assistant Secretary of Defense for Research and Engineering and funded by the Office of Naval Research through Grant No. N00014-15-1-0029. Development and maintenance of the growth facilities used for fabricating samples was supported by DOE (DE-FG02-03ER46028). We acknowledge the use of facilities supported by NSF through the UW-Madison MRSEC (DMR-1720415) and the MRI program (DMR-1625348). The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Army Research Office (ARO), or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation herein.

### 3.4.8 Appendix: Additional WW theory

Figure 3.19 shows the same results for the valley splitting contribution of the germanium oscillations as Fig. 3.16(c), but with a larger scale to show the top of the peaks near  $q \approx 20$ .

### 3.4.9 Appendix: Heterostructure Growth

The measured heterostructure is grown on a linearly graded SiGe alloy with a final 2  $\mu\text{m}$  layer of  $\text{Si}_{0.705}\text{Ge}_{0.295}$ . Prior to heterostructure growth, the SiGe substrate is cleaned and prepared as described in Ref. [25]. The substrate is loaded into the growth chamber and

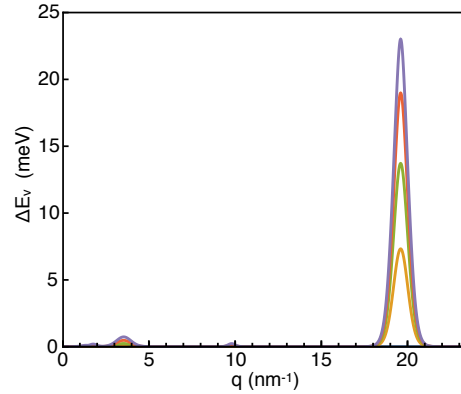


Figure 3.19: The contribution to the valley splitting  $\Delta E_v$  due to a sinusoidal Ge concentration in the quantum well as a function of the wavevector  $q$ . This is the same figure as Fig. 3.16(c), with a larger scale to show the top of the peaks at  $q \approx 20$ .

flash heated to 825 °C while silane and germane are flowing. The temperature is lowered to 600 °C, at which point a 550 nm 29.5% Ge alloy layer is grown. For the quantum well, the growth begins with a 10 second pulse of pure silane gas at 90 sccm. Then, 90 sccm of silane and 4.88 sccm of germane are introduced for 10.63 seconds followed by 10 seconds of pure silane. This SiGe–Si pulse sequence is repeated a total of 5 times. The pulse times are tuned to achieve a period of 1.8 nm and a peak Ge concentration of 9%. After the quantum well, a 60 nm  $\text{Si}_{0.705}\text{Ge}_{0.295}$  spacer is grown and the heterostructure is capped with a thin 1 nm layer of pure silicon.

### 3.4.10 Appendix: Fabrication Details and Hall Measurement

Hall bars and quantum dot devices were fabricated simultaneously on the same  $\sim 10$  mm chip. 15 nm aluminum oxide gate dielectric is grown by atomic layer deposition (ALD) at 200 °C. This oxide is etched by dilute HF in a 30  $\mu\text{m}$  square region centered around the dot region. Another 5 nm of aluminum oxide is then deposited. This results in 5 nm of deposited oxide over the dot region and 20 nm over the Hall bars. The chip then undergoes a 15 min, 450 °C forming gas anneal. The Hall bar gate metal is a bi-layer of titanium and palladium, patterned by photo-lithography. The quantum dot gate design has three layers

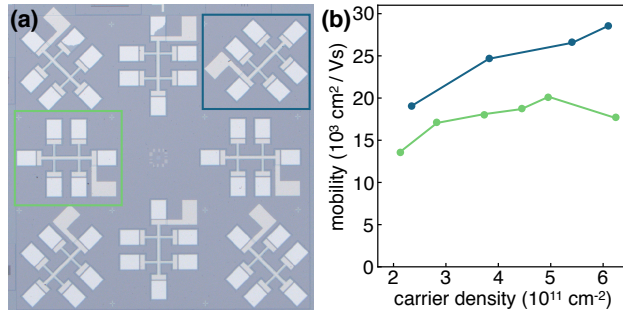


Figure 3.20: (a) Optical image of Hall bar devices measured. The length of the Hall bar between the central ohmics is 200  $\mu\text{m}$ . The Hall bar top gate is isolated from the heterostructure by 20 nm of ALD-grown aluminum oxide. All deposited metal is a Ti/Pd stack. (b) Transport mobility results of two Hall bar devices highlighted in (a), performed at  $\sim 2$  K.

of aluminum patterned by electron-beam-lithography. Each gate layer is isolated by the self oxidation of the aluminum, enhanced by a 15 min downstream oxygen plasma ash. Fig. 3.20 shows an optical image of the Hall bars measured and the transport mobility results of the measurements as a function of carrier density, measured at  $\sim 2$  K.

### 3.4.11 Appendix: Gate Lever Arms for Dot Tuning

The lever arm of the plunger gate P1 to the dot used for pulsed-gate spectroscopy is measured by thermally broadening the charge-sensed transition line. The charge-sensed electron charging transition is swept as the mixing chamber temperature is increased, and the current through the charge sensor is fit to [64]

$$I_{CS}(V) = A \tanh\left(\frac{\alpha(V - V_0)}{2k_B T_e}\right) + b * V + I_0, \quad (3.26)$$

where  $k_B$  is Boltzmann's constant,  $T_e$  is the electron temperature,  $\alpha$  is the lever arm, and  $A$ ,  $b$ ,  $V_0$  and  $I_0$  are additional fitting parameters. A term,  $T_e/\alpha$ , is extracted from each fit as a function of mixing chamber temperature,  $T_{MC}$ . This is fit to the phenomenological expression

$$\frac{T_e}{\alpha} = \frac{1}{\alpha} \sqrt{T_{MC}^2 + T_{e0}^2}, \quad (3.27)$$

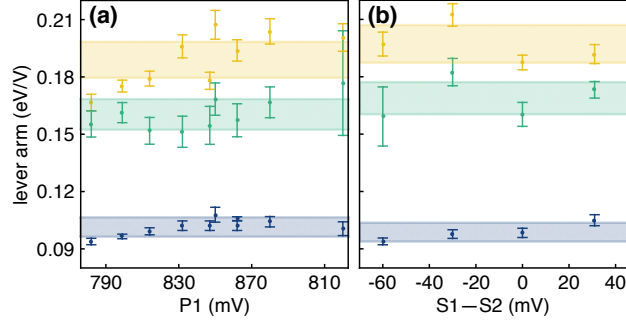


Figure 3.21: (a) Lever arms for S1 (yellow), S2 (green), and P1 (blue) of the ‘symmetric’ voltage tuning method described in the main text. (b) Lever arms for S1 (yellow), S2 (green), and P1 (blue) of the ‘asymmetric’ voltage tuning method described in the main text. In both plots, the shaded regions are  $\pm 5\%$  around the average.

and we extract a lever arm and a base electron temperature  $T_{e0}$  given  $T_{MC} = 0$ .

For the ‘symmetric’ tuning method where both screening gates S1 and S2 are changed in the same voltage direction, the lever arm is measured at every other voltage tuning. For voltage tunings where the P1 lever arm is not explicitly measured, the average of the two nearest tunings is used. For the ‘asymmetric’ tuning method where S1 and S2 are changed in opposite directions, the lever arm is measured at every tuning. Relative lever arms between a screening gate and P1 are determined by measuring the slope of a transition line as both gate voltages are changed. Using the absolute lever arm of P1 and the relative lever arms for the screening gates, their absolute lever arms to the dot are calculated.

Figure 3.21 shows these lever arms for both the ‘symmetric’ and ‘asymmetric’ tuning methods. As shown, the lever arms for all three gates stays within 5% of the average value for most tunings. There is no noticeable difference in the lever arms between the tuning methods, despite the significant difference in valley splitting tuning. This may indicate that this method of tracking the lever arms is not a sensitive enough technique to measure the lateral movement expected in the ‘asymmetric’ tuning scheme.

## Chapter 4

# Improvements and Alternatives to Quantum Dot Fabrication

In this chapter, we explore improvements and modifications to the fabrication of silicon quantum dot gate structures. The designs, material choices, and processing details of silicon quantum dots are constantly evolving. The motivators for this evolution are the desire for better control of quantum dot and qubit parameters, newer qubit designs, and lower charge noise. In silicon quantum devices, charge noise is a major limitation to better performing qubits. In single spin qubits with isotopically purified silicon quantum wells, charge noise can be the limiting factor to higher fidelities [42, 72]. At very low frequencies, charge drift can also affect the long term stability of qubits [71]. In Sec. 2.2.2, we presented an older ‘open’ quantum dot gate design and a newer overlapping aluminum gate design that has become the standard in the Eriksson group. In this chapter, we present three investigations into modifications to the gate fabrication. We begin with modifications to the material stack and processing of Hall bars to investigate the influence of oxide thickness, treatment, and distance to the 2DEG on the transport mobility. We then present the fabrication and measurement of a ‘donor-dot’ system, in which phosphorus ions are implanted into the 2DEG to create a hybrid system of donor and gate-defined quantum dots. We end this

chapter with a discussion of the progress towards SPARTA, a novel fabrication process to replace the overlapping aluminum gate design with etch-defined palladium gates.

## 4.1 Fabrication Changes for 2DEG Transport Mobility Improvements

### 4.1.1 Introduction to Mobility-Limiting Charge Defects

The quantum dot charge noise measurement described in Sec. 2.3.6 is a relatively simple procedure but requires a fabricated and tuned quantum dot device. Measurements of the mobility in Hall bars can give insight into the disorder which affects the 2DEG and scatters electrons, while requiring much less fabrication overhead [59]. By varying fabrication processes and measuring the resulting mobilities, the influence of these processes on the disorder can be inferred.

Scattering of electrons in a 2DEG can occur from impurities and roughness at the quantum well interface where the 2DEG forms but also from remote charge impurities which create an uneven potential in the 2DEG. Gate fabrication on the surface of the SiGe heterostructure is a potential source of charge impurities, through the use of amorphous (non-crystalline) oxides, material interfaces, and high-energy lithography processes. Remote impurity scattering at the surface is thought to come primarily from the interface between deposited oxides such as aluminum oxide and the silicon surface, as well as bulk impurities within the oxides themselves. Oxide deposition for Si/SiGe quantum dots is typically achieved through atomic layer deposition [115]. The precursor chemicals used to grow the oxide, such as trimethyl-aluminum (TMA) for aluminum oxide, can lead to unintended carbon impurities and oxygen vacancies [116]. These defects and impurities can lead to interface traps and two-level-systems (TLS) within the oxide [69, 70, 117]. High-energy electrons from electron-beam lithography as well as radiation from electron-beam metal evaporation have been shown to

increase oxide-silicon interface trap densities [118, 119].

Simply by increasing the distance between the 2DEG and the heterostructure surface, the influence of these remote impurities can be reduced. This is achieved by increasing the thickness of the SiGe spacer that separates the silicon quantum well from the surface. Multiple studies have shown that increasing the SiGe spacer thickness can increase the mobility of Hall bars [120, 121]. Decreasing the spacer thickness, however, can help with quantum dot control, as the surface gates are closer to the 2DEG and its electrostatic potential can be shaped with greater precision. Reducing the thickness of these amorphous oxide layers can also lead to better device performance and lowered charge noise, as there will simply be fewer bulk defects present in a thinner oxide layer [69]. Additionally, thermal treatments of oxide layers after deposition or growth has been shown to reduce the interface trap density and passivate dangling bonds. Low temperature (300 – 500 °C) anneals in the presence of forming gas ( $\text{H}_2 + \text{N}_2$ ) have been shown to increase mobilities and decrease measured charge noise in silicon quantum devices [70, 89, 122–124].

### 4.1.2 Fabrication Modifications

Here, we modify three fabrication parameters and explore their effects on the transport mobility of a Hall bar: thickness of the SiGe offset between the silicon quantum well and the surface, electron beam dose for the top gate lithography, and the presence of a forming gas anneal after oxide deposition. Although these modifications have been explored previously in the literature, differences in fabrication tools can lead to different results. We investigate these fabrication changes to qualitatively understand how they affect the performance of our devices specifically with the tools available to us.

Hall bars are fabricated on Si/SiGe heterostructures with three different offset thicknesses: 10.8, 21.6, and 38 nm. We define a ‘standard process’ fabrication, in which all lithography is achieved through electron-beam lithography at an exposure dose of  $500 \mu\text{C cm}^{-2}$  with a 30 kV e-beam source. The dielectric isolating the Hall bar top gate from the heterostructure

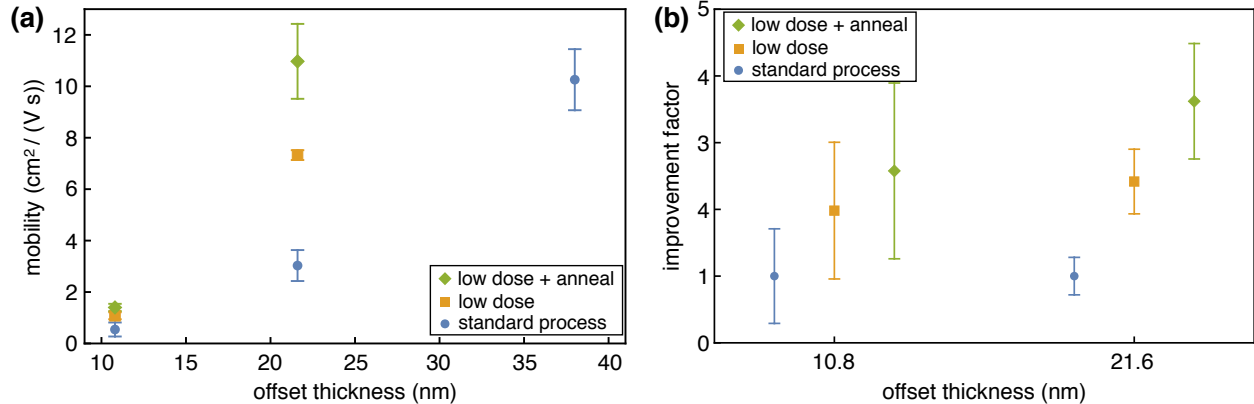


Figure 4.1: (a) Transport mobility at  $4 \times 10^{11} \text{cm}^{-2}$  for differently processed Hall bars at varying SiGe offset thicknesses. Deeper quantum wells tend to have higher mobility, due to their increasing distance from defects above the heterostructure. Lowering the electron-beam dose for the top gate lithography by 40% results in increased mobility. Adding an additional 15 min, 450 °C forming gas anneal after oxide deposition further increases the mobility. (b) Same data as in (a), but normalized to the performance of the standard process to better show the size of improvement for each fabrication change. Offset thicknesses are shifted from true values of 10.8 nm and 21.6 nm for visibility.

surface is 15 nm of aluminum oxide grown by atomic layer deposition at 150 °C in an ALD tool manufactured by Cambridge Nanotech. For a ‘low dose’ fabrication process, the electron-beam lithography dose for the top gate is lowered to  $300 \mu\text{C cm}^{-2}$ , a 40% reduction. This dose reduction is possible due to the wide clearing dose range for the PMMA (polymethyl methacrylate) resist used. Finally, the anneal is defined as a 15 min, 450 °C forming gas (5%  $\text{H}_2$ ) anneal after the oxide deposition. The forming gas anneal is performed in a Heatpulse 610 Rapid Thermal Annealer (RTA).

### 4.1.3 Results

Figure 4.1(a) shows the results of these modifications, as a measurement of the transport mobility of the Hall bar at a carrier density  $n_{2D} = 4 \times 10^{11} \text{cm}^{-2}$ . The blue circles correspond to the standard process fabrication, the orange squares correspond to fabrication at the lower dose, and the green diamonds correspond to a lower dose in addition to a forming gas anneal. The mobility increases with increasing offset thickness for the standard process, as expected.

This order-of-magnitude increase in the mobility is in agreement with previously published results [120]. The low dose and low dose + anneal fabrication processes are performed on heterostructures with the two thinner offsets. Reducing the dose and performing a forming gas anneal after oxide deposition results in a higher mobility for an offset thickness of 21.6 nm than the standard processed 38 nm heterostructure. Figure 4.1(b) presents the results for the two thinner offset heterostructures as fractional improvements in mobility over the standard heterostructure. Presented in this way, the standard process data points have a value of 1. This allows for better comparison between the two offset thicknesses, showing that the fractional improvement from lowering the dose and adding the post-oxide anneal is similar for each offset thickness.

These results serve to demonstrate how simple changes to fabrication processes can affect and improve the performance of Si/SiGe 2DEGs. After these measurements were completed, the standard fabrication procedure for quantum dots in the Eriksson group was modified to include forming gas anneals after oxide deposition. Additionally, use of electron-beam lithography was reduced whenever possible to avoid unnecessary damage. The improvements of these fabrication modifications, and their limits, serve as motivation for further innovation in device design and fabrication.

## 4.2 Localized Implantation of Phosphorus Atoms for Donor-Dot Qubits

### 4.2.1 Introduction to Donor Atom Quantum Dots

In this work, we have almost exclusively focused on *gate-defined* quantum dots, in which charge is confined into quantum dots via externally applied voltages on gates and quantum wells formed by a heterostructure. However, dopant atoms such as a phosphorus atom in silicon provide a steep electrostatic potential for one or two ‘donor’ electrons to be confined [10].

The electronic states of these dopants can then be controlled through gate voltages. Additionally, the nuclear spin of these dopants could be used for quantum computing, as originally proposed in Ref. [125]. A two-qubit gate between precisely placed phosphorus donor electrons within silicon has recently been achieved [126]. While these dopants provide excellent electrostatic confinement and often extremely long coherence of electron spin states, positioning and coupling the spins of multiple dopants is difficult due to their small size. For this reason, it has been proposed to use gate-defined quantum dots as an intermediary between dopant qubits [127]. When positioned near a heterostructure interface, electrons can be pulled off the dopant ion and into a gate-defined quantum dot, then moved or coupled to other quantum dots. These hybrid ‘donor-dot’ systems in which both dopants and gate-defined quantum dots are used can leverage both the long-coherence times of dopant qubits and the versatility and ease of control of gate-defined quantum dot qubits [128]. Coherent interaction between a phosphorus donor electron and a Si-MOS quantum dot electron has been shown, with a clear path forward towards control of dopant nuclear spins [129].

The positioning of dopants can be achieved via a scanning tunneling microscope (STM) during silicon growth or via ion implantation, where the dopants are ionized and accelerated towards the heterostructure. Using STM placement, the position of the dopant is very well controlled, with near atomic precision [130]. Using implantation, dopant placement is inherently more imprecise, due to the Poissonian distribution of the number of implanted dopants and the lateral straggle of dopants as they travel through the implanted material. There are several approaches to improve the lateral spread of dopants, such as the use of higher mass dopants or by implanting through resist, gate metal, or AFM cantilever nanostencils [131–134]. The exact number of dopants implanted can be measured in a number of ways, notably through transient current in an on-chip transistor or detection of secondary electron emission [135, 136].

Here, we present work towards coupling phosphorus dopants to gate-defined quantum dots in a Si/SiGe heterostructure. We present a fabrication method for implantation of

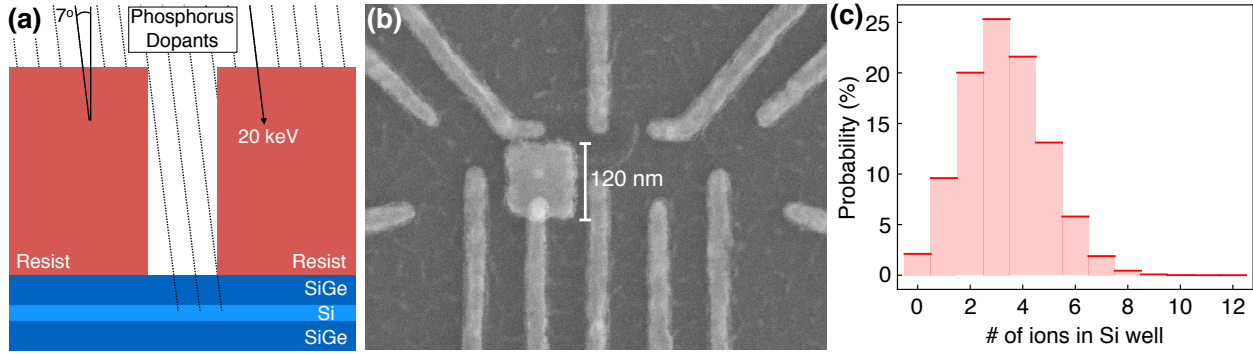


Figure 4.2: (a) Schematic representation of the implantation process. Phosphorus ions are implanted at 20 keV at a  $7^\circ$  angle. Electron-beam resist is used to mask the heterostructure and allow implantation only in a small area. (b) Implant window test. The 120 nm square shows a test of the implantation window aligned to the first layer of gates. Metal (titanium and gold) is deposited in both the implant window and the first layer gate pattern for this test. (c) Probability of the number of ions implanted within the quantum well for a 120 nm square window and an implantation dose of  $10^{11}$  ions  $\text{cm}^{-2}$ .

a small number of phosphorus ions and present evidence of dopant-like states coupled to gate-defined quantum dots.

## 4.2.2 Fabrication Methods of the Donor-Dot Device

The phosphorus dopants are placed into a Si/SiGe heterostructure through ion implantation. The area in which dopants are implanted is defined by a resist mask made with electron-beam lithography. Figure 4.2(a) shows a schematic of how the resist masks the Si/SiGe heterostructure. Phosphorus ions are accelerated to 20 keV and implanted at a  $7^\circ$  angle. This angle ensures that the ions interact and collide with the Si/SiGe lattice, reducing the chance of unintentionally deep implantation. The acceleration voltage is chosen based on the angle of incidence and the thickness of the SiGe spacer above the silicon quantum well to maximize the probability that the donors are stopped within the quantum well. The implantation depth is determined by a Monte-Carlo simulator called SRIM: Stopping and Range of Ions in Matter [137]. The SiGe spacer is thin, only 20 nm, to reduce the accelerating voltage necessary, reducing the statistical spread of the implantation depth. The resist mask

is  $\sim 150$  nm of PMMA, which is thick enough to avoid accidental implantation into regions outside of the implant window.

The implantation window is a  $120 \times 120$  nm square and the phosphorus ions are implanted prior to gate fabrication. To ensure alignment between the implant window and the quantum dots, palladium alignment markers are fabricated on the heterostructure prior to the implant window lithography. The implant window is aligned to these marks, which are later used again for gate alignment. Figure 4.2(b) shows a scanning electron microscope (SEM) image of a test of the implant window and the first layer of gates. Gold is deposited in the implant window for this test instead of phosphorus ions, showing the 120 nm size of the window and its alignment to the gates.

Using the distribution of implantation depths calculated with SRIM and the square area of the implant window, a implantation dose of  $10^{11}$  ions/cm<sup>2</sup> is chosen to achieve  $3 \pm 1$  phosphorus ions in the quantum well with 12 ions implanted in total. The probability of the number of phosphorus ions in the well is shown in Fig. 4.2(c). Although we only want to couple the quantum dot to a single dopant, this higher average probability is chosen to ensure successful implantation within the quantum well. After implantation, the implant window mask is stripped and the device is briefly annealed at 700 °C for 15 seconds to activate the dopants.

The quantum dot gate design is an ‘open’ design, as described in Sec. 2.2.2, consisting of a double quantum dot with quantum point contact (QPC) charge sensors on either side. Figure 4.3(a) shows the first layer depletion gates, with relevant gates and ohmic sources labeled. The gate metal is a bi-layer of titanium and gold and the gates are separated from the heterostructure surface by 15 nm of ALD grown aluminum oxide. The two central pockets between the tips of these first layer gates are the intended locations of the quantum dots. The left quantum dot pocket is the location of the implanted phosphorus, as shown in Fig. 4.2(b). The second layer of accumulation gates is shown in Fig. 4.3(b) and is isolated from the first layer by 80 nm of ALD grown aluminum oxide. The large gates on the left,

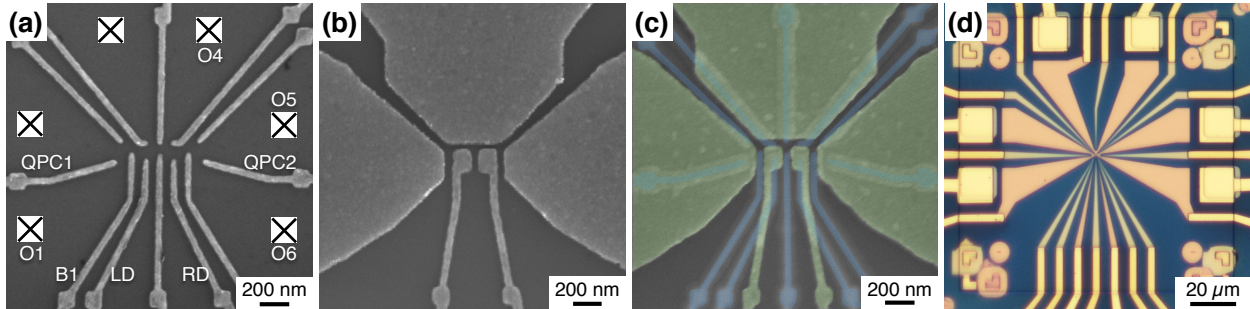


Figure 4.3: (a) SEM image of the first layer of depletion gates with ohmic sources and select gates labeled. The gates are isolated from the heterostructure by 15 nm of aluminum oxide. (b) SEM image of the second layer of accumulation gates. (c) Colorized SEM of both layers of gates. An 80 nm layer of aluminum oxide isolates the two layers of gates. The dots form under the two paddle-shapes of the second layer gates. (d) Optical image of active region of a fully fabricated device. All gate metal is a bi-layer of titanium and gold.

right, and top create electron reservoirs for the QPCs and the dots. The central two paddle-shaped gates accumulate electrons into the dots. Figure 4.3(c) shows a colorized SEM image of an aligned and completed device. Figure 4.3(d) shows an optical image of the active mesa region. The blue hue is caused by the thick  $\sim 100$  nm aluminum oxide. The quantum dots form at the very center of this image.

### 4.2.3 Quantum Dot Measurements of the Donor-Dot Device

A device with implanted dopants was measured in a dilution refrigerator with a base temperature below 100 mK. Quantum dots are formed in the central dot region to search for evidence of implanted dopants. Electrons coupled to dopants can be distinguished from electrons in a gate defined quantum dot in a few ways. First, dopants such as phosphorus only have three possible charge states, the ionized state  $D^+$ , the one-electron neutral state  $D^0$ , and two-electron state  $D^-$  [10]. Additionally, the strong confining potential results in a much larger charging energy (electrostatic energy required to add an additional electron) compared to gate-defined quantum dots. Finally, depending on the exact placement of the dopant, current transport through the dopant itself may be impossible as it may not have sufficient tunnel coupling to a source and a drain reservoir. We use these concepts to

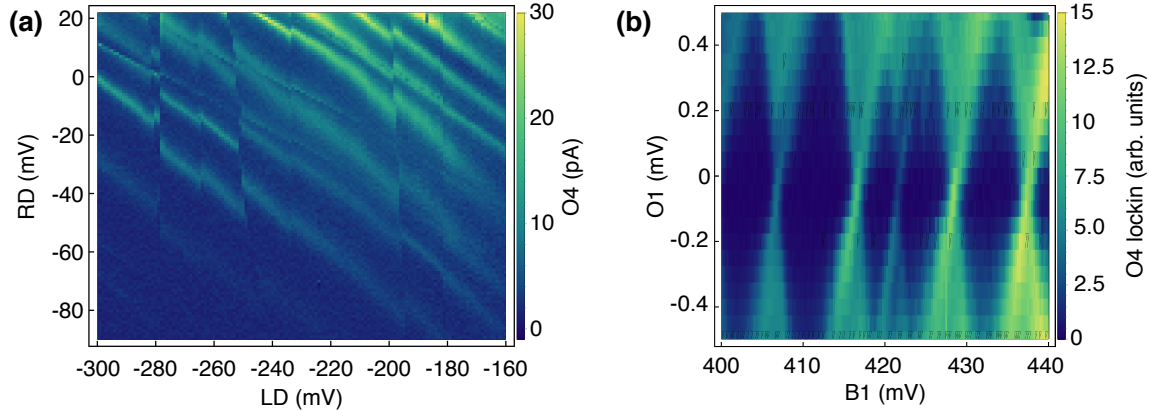


Figure 4.4: (a) Transport current of a centrally formed dot. Current flows from O1 to O4, labeled in Fig. 4.3(a). Sharp near-vertical transitions strongly coupled to the left dot gate show evidence for impurity states, possibly the implanted donors, near the dot. (c) Coulomb diamonds of a quantum dot formed in the left dot region, flowing current from O1 to O4. A 191 Hz ac voltage bias is applied to O1 and the output current from O4 is measured with a lock-in amplifier referenced to this frequency. A sharper diamond scoring through the center is potential evidence of an implanted phosphorus donor.

investigate the behavior of the donor-dot device.

Figure 4.4 shows two measurements of the donor-dot device investigated. In Fig. 4.4(a), a dot is formed centrally between gates LD and RD (labeled in Fig. 4.3(a)) and the Coulomb blockade oscillations of the current through the dot is measured. There are several near-vertical features which cause finite shifts in the Coulomb blockade peaks. These features show slightly different slopes and affect the central dot peak locations by different magnitudes, indicating they each originate from different locations. The overall slopes of these features indicate that they are closer to LD than RD, which is where the phosphorus dopants are implanted. There do not appear to be multiple transitions for each of these features in this voltage range, indicating a large charging energy or limited number of available states. Features such as this are sometimes described as ‘impurity’ states and could be formed by phosphorus dopants or other unintentional impurities within the heterostructure [48].

With this preliminary evidence of electronic dopant states towards the left side of the device, a single quantum dot is formed near gate LD. Figure 4.4(b) shows Coulomb diamonds of the current flowing through this quantum dot. At the center of this figure, a much narrower

diamond scores through the evenly spaced diamonds. As previously mentioned, the strong confinement of a dopant ion results in a large charging energy. Described in Sec. 2.3.3, the charging energy of a dot can be determined by the source-drain bias at which the finite-current diamonds intersect. Phosphorus donors in silicon should have a charging energy of order 40 meV [138]. Although the data here is insufficient for an accurate measurement of the charging energy of this central feature, it is certainly indicative of a much larger charging energy than the surrounding electron transitions ( $E_C \approx 0.5$  meV).

Further measurements of this device were hindered by sub-optimal design of the charge sensor QPCs. Simultaneous isolation of the quantum dots and formation of a sensitive QPC path proved to be incompatible, because the QPC gates were too narrow and too close to the barrier gates. A newer design, with wider QPC gates further separated from the nearby barrier gates, was designed to solve this issue. However, this newer design was never experimentally tested, as we moved on to focus on other projects.

#### 4.2.4 Outlook

The successful fabrication of an aligned implantation window and subsequent aligned gate fabrication is a crucial step towards the realization of a well controlled Si/SiGe donor-dot system. In future iterations, the gate design could be modernized (such as the overlapping aluminum gate design), and the fabrication window could be shrunk even more, if desired. Increasing the number of implanted dopants would improve the chances of a well-positioned donor, although it may reduce the coherence of the potential qubit system. Switching to a heavier dopant, such as antimony, would decrease the probabilistic spread of the implantation depth and lateral straggle. Finally, deterministic implantation of single donors through some *in-situ* detection method would improve the scalability of this approach. At present, this work aims to present a strategy for donor-dot integration into a standard Si/SiGe quantum dot fabrication process.

## 4.3 SPARTA: Subtractive Palladium Anneal-Ready Two-layer Architecture

### 4.3.1 Introduction

The gate design and fabrication of silicon quantum dot devices is constantly evolving. Although the overlapping aluminum gate design has been successfully implemented across the quantum dot community, the desire for lower charge noise and higher device yield has spurred investigations into alternative materials and fabrication processes. Palladium has been proposed and utilized as a replacement for aluminum as the gate metal by multiple research groups [139, 140]. Palladium, unlike aluminum, does not oxidize in atmospheric conditions, and so requires deposited dielectrics to isolate each layer. Titanium nitride, deposited via atomic layer deposition has also been explored as a replacement gate metal [141, 142]. With TiN, the gates are defined through a negative etch process, instead of an additive lift-off process. As the field of quantum dot based qubits grows, industrial manufacturing of all-optical lithography finFET-based quantum dot devices has recently been published, although these methods are typically out-of-reach for academic work [143]. These changes aim to reduce the use of noisy dielectrics, increase the precision and yield of the fabrication processes, and improve quantum dot control.

Here, we present a novel fabrication process named SPARTA: Subtractive Palladium Anneal-Ready Two-layer Architecture. As its name suggests, SPARTA consists of two layers of etch-defined Pd gates. The gate design is nearly identical to the overlapping aluminum design presented in Sec. 2.2.2. We explain the SPARTA process, explore the proposed benefits of SPARTA over the current standard of overlapping aluminum gates, and present the current progress towards the implementation of SPARTA in quantum dot fabrication. We include key fabrication insights and advances which make SPARTA a feasible process, as well as past and current challenges to successful implementation. We end with detailed guides to the unique fabrication processes involved for SPARTA.

### 4.3.2 SPARTA Fabrication

We begin with a discussion of the ‘S’ in SPARTA: subtractive. When gates are fabricated by subtraction, a blanket layer of gate metal is deposited across the device, followed by resist deposition and patterning. The gate metal is then etched away in the regions where the resist does not cover the surface, revealing the gate design. This is in contrast to typical additive gate fabrication, where the metal is deposited after resist patterning, followed by a lift-off process which removes the resist and any metal deposited on top, leaving only metal in the gaps between the patterned resist. Additive fabrication is typically achieved through positive-tone lithography and subtractive fabrication is achieved through negative-tone lithography.

Figure 4.5 shows a schematic comparison between positive and negative tone lithography. A mock design of a layer of quantum dot gates shows tightly packed finger gates and reservoir gates, similar to the overlapping aluminum gate design. Figure 4.5(a) presents a top-view of the patterned resist for positive-tone lithography, showing that the developed resist is everywhere except the desired gate locations. Figure 4.5(b) presents a similar view of the patterned resist for negative-tone lithography, showing that the resist covers only where gates should be patterned, exactly opposite to positive-tone lithography. Figure 4.5(c-d) shows a side view of these two approaches at the dotted lines in Fig. 4.5(a-b), respectively. When the desired gaps between gates are very narrow, the patterned resist for positive-tone lithography becomes very thin, *i.e.*, the resist is much taller than it is wide. These thin resist structures are prone to ‘sidewall collapse’, where the resist leans or falls over, impacting the gate patterning, as shown in Fig. 4.5(c) [144]. In contrast, narrowly spaced patterns with negative-tone lithography result in wide resist structures, as shown in Fig. 4.5(d). Therefore, when attempting to fabricate very tightly packed gates, a subtractive process which utilizes negative-tone lithography is superior to an additive one. In the SPARTA process, the three-layer overlapping aluminum gate design is replicated with only two layers by combining the second and third layer gates which define the reservoir, plunger, and barrier gates, into a

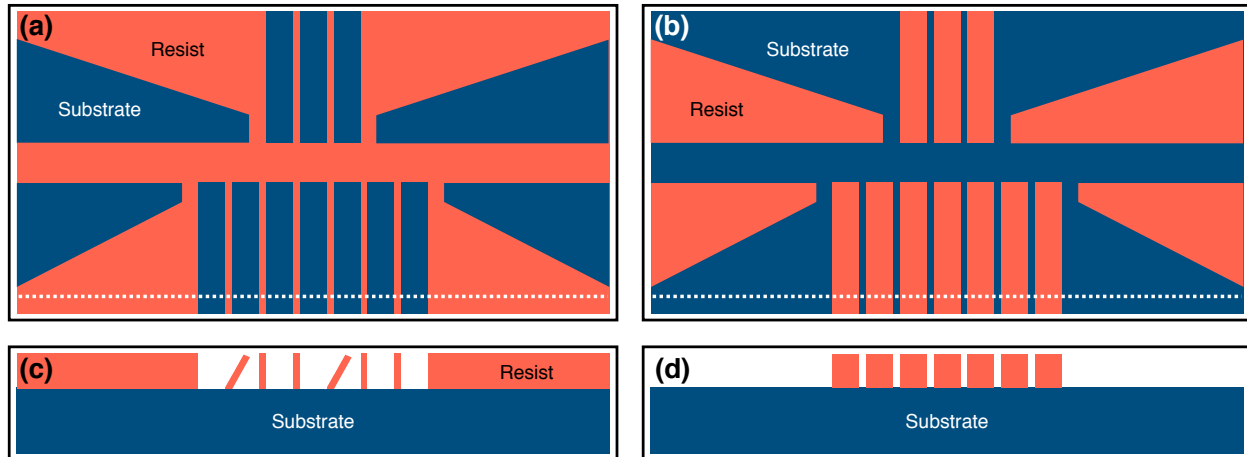


Figure 4.5: (a) Schematic representation of a positive-tone lithography process for a QD gate design (top view). (b) Schematic representation of a negative-tone lithography process for a QD gate design (top view). (c) Side view of the positive-tone lithography in (a) along the dotted line. The narrow resist columns between finger gates are prone to ‘sidewall collapse’, as shown by the tilted resist lines. (d) Side view of the negative-tone lithography in (b) along the dotted line. When defining wide gates with narrow gaps, the negative-tone process results in wide, stable resist columns.

single layer. The tight gate spacing is achieved through subtractive processing.

The chosen negative-tone resist for SPARTA gate fabrication is hydrogen silsesquioxane (HSQ). Unlike the polymer-based PMMA resists typically used for EBL, HSQ is an inorganic compound, consisting of silicon, oxygen, and hydrogen. When exposed to high energy electrons or photons, HSQ crosslinks into a glass-like structure [145]. Its small chemical structure allows for very small patterned features, with a resolution of about 5 nm [146]. The silicon oxide-like structure after exposure makes HSQ very resistant to etching and therefore a good candidate for subtractive processing. However, this also leads to the need for a hydrogen fluoride (HF) process to remove exposed and cross-linked HSQ. In addition, HSQ requires cold-storage ( $< 10\text{ }^{\circ}\text{C}$ ) to maintain an acceptable shelf life. It has been reported that storage at liquid nitrogen temperatures may extend the nominal performance lifetime of HSQ indefinitely [147]. HSQ is also very process dependent; the time between spinning the resist (HSQ is suspended in methyl isobutyl ketone) and exposure can significantly affect the resulting pattern. Machine learning techniques have even been used on dose test images

to quantify failure modes and improve proximity dose corrections for HSQ lithography of quantum dots [148]. Despite these process complications, its excellent resolution and etch resistance outweigh the costs.

We now consider the choice of Pd for the gate material, and contrast it to aluminum. Palladium is a noble metal, so under ambient conditions, no appreciable oxide forms on the Pd surface. In addition to the oxide that forms at the Al-air interface, Al has been shown to pull oxygen from oxide surfaces it is deposited onto. This can result in additional unintended oxide layers and interfaces, increasing strain and charged defects [139]. When deposited via electron-beam evaporation, Pd has a much smaller grain size than Al, below 10 nm. In comparison, the Al grain size, depending on growth conditions, is typically 20-40 nm. This smaller grain size aids in the fabrication of tightly packed gates, where the gaps between gates are intended to be as narrow as possible. Additionally, Pd has a relatively high melting point compared to Al. Anneals in forming gas, previously discussed in Sec. 4.1, can help to repair damage to oxide layers and interfaces after electron-beam lithography and metal deposition. With Pd gates, higher temperature anneals should be possible after gate fabrication. The ‘Anneal-Ready’ portion of SPARTA is in reference to this higher temperature tolerance.

Critically, Pd metal has a large work-function and when contacted with silicon, forms a Schottky barrier [149]. When applying a negative voltage to a Pd gate, no current will flow to the silicon. This property has been previously utilized in delta-doped Si/SiGe heterostructures with a single layer of Pd gates directly contacting the heterostructure surface [150]. Since only negative voltages are used in this device design, no dielectric layer is needed. In the SPARTA (or overlapping aluminum) design, the first layer of gates, previously referred to as the screening gates in this work, locally deplete the electrons to create one-dimensional channels where dots can form. These screening gates are typically operated at negative voltages. Without an aluminum oxide layer beneath these gates, which typically contain negatively charged defects [151], we argue that these screening gates could be operated exclusively at zero or negative voltages. Therefore, with SPARTA, we can remove the base

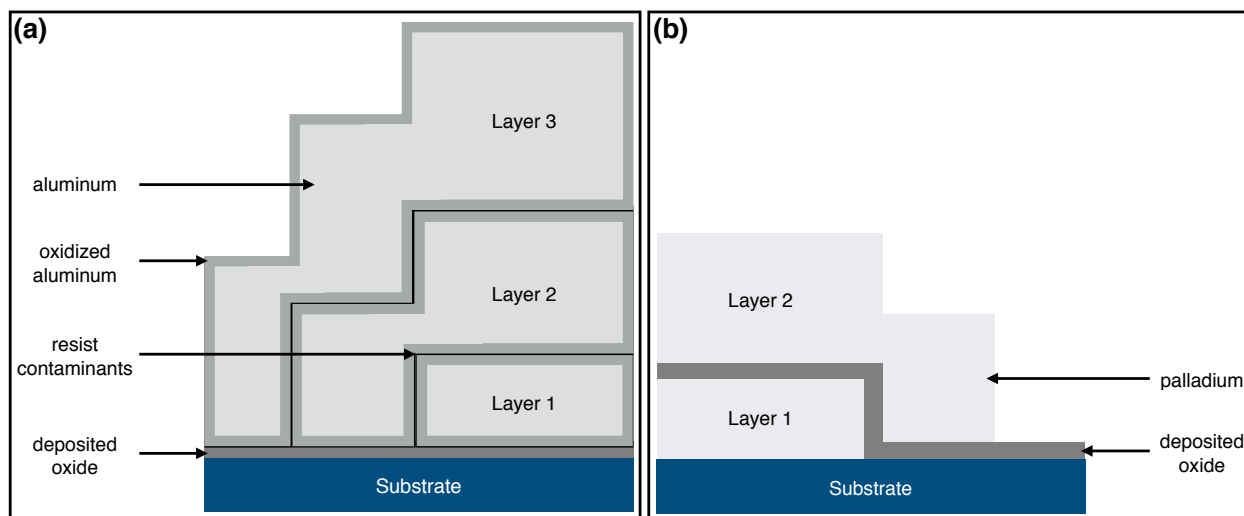


Figure 4.6: (a) Side view of the overlapping aluminum design. There are several layers and interfaces between the surface of the substrate and any gate layer. (b) Side view of the SPARTA layers. Leveraging the benefits of subtractive processing, gate layout, and gate material, there are fewer layers and interfaces between the substrate and either gate layer.

gate dielectric layer from the fabrication process. The first layer screening gates, made from Pd, are deposited directly on the heterostructure surface.

Figure 4.6 shows side view schematics comparing the three-layer overlapping aluminum process to SPARTA. In the Al process shown in Fig. 4.6(a), a deposited oxide is required below the first layer of gates and each gate layer is self-oxidized. In addition to the aluminum and oxide layers, a ‘contamination’ layer between all gates is added to the schematic. In an additive process, there is patterned resist on the substrate surface during metal evaporation to define where metal is deposited. This can lead to contaminants, such as underdeveloped resist, development solution, or otherwise, to be buried underneath the depositing metal. In contrast, in subtractive processing, surfaces can be aggressively cleaned prior to metal deposition, as there is no resist pattern present during deposition. Independent of the reduced number of fabrication layers, a subtractive process may be advantageous compared to an additive process due to the increased cleanliness of deposited layers alone.

Figure 4.6(b) shows a side view schematic of the SPARTA process. The first layer of gates is deposited directly onto the substrate, without any isolating dielectric. Following

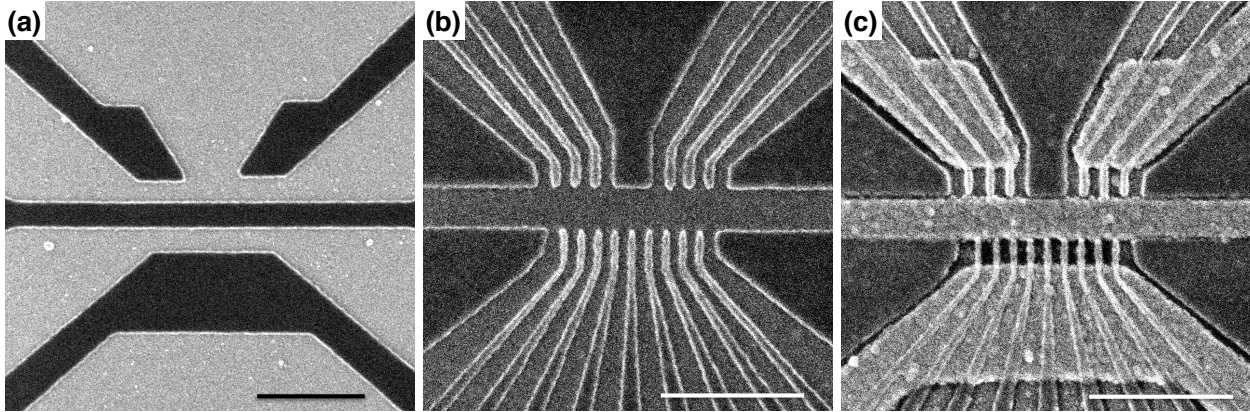


Figure 4.7: (a) SEM image of the first layer of SPARTA gates written with HSQ (dark) on palladium (light). (b) SEM image of the second layer of SPARTA gates written with HSQ (dark) on palladium (light). (c) SEM image of the second layer of SPARTA gates written with HSQ, aligned to the first layer of etched palladium gates. All scale bars are 500 nm.

the first layer etch (and strip of the HSQ by HF), an inter-layer dielectric is deposited, such as aluminum oxide. After oxide deposition, the sample can again be aggressively cleaned with solvents, an oxygen plasma, or otherwise, followed by the second layer gate deposition, patterning, and etch. Comparing the two fabrication processes in Fig. 4.6, SPARTA has many fewer layers. Critically, the number of interfaces is also drastically reduced. Charge noise is thought to be primarily due to charge traps at oxide interfaces, so reducing the number of interfaces here should reduce the charge noise in these devices.

Figure 4.7(a-c) show scanning electron microscope (SEM) images of the patterned first layer, second layer, and aligned layers of SPARTA, respectively. In Fig. 4.7(a), it is clear that the first layer of SPARTA is identical to the first layer of the overlapping aluminum design (see Fig. 2.7(c)). In this SEM image, HSQ (darker regions) is patterned on top of Pd. Figure 4.7(b) shows how the second layer of SPARTA incorporates the reservoir, plunger, and barrier gates into a single layer. The center-to-center pitch of the finger gates is 60 nm. Ideally, the gap between gates is as narrow as possible. Here, the gaps range between 10 – 20 nm. In Fig. 4.7(c), the device has been processed through the patterning of the second layer of gates. Although difficult to discern from this image, the first layer of gates is etched and the inter-layer oxide and second blanket layer of Pd are deposited. The

alignment between the two layers is apparent. The only remaining step is the etch of the second layer of gates.

There are several etch processes that could be utilized to define the Pd gates for SPARTA, none of which are yet fully optimized. An ideal etch for these gates would be a process which solely etches the gate metal while leaving the HSQ mask and underlying surface unaffected. The inertness of Pd results in very few possible etch chemistries.

One famous etchant of noble metals such as Pd is ‘aqua regia’, which is a solution of nitric acid and hydrochloric acid in a 1:3 ratio [152]. This etchant is extremely selective against silicon, silicon oxide, and aluminum oxide. However, wet etches (etches in liquid solution) are isotropic, meaning as they etch downward through a material, they also begin to etch sideways underneath the etch mask, which can result in the widening of etched regions. The first layer of gates, though, is quite simple and the patterning could be compensated to account for widening of the etched regions.

Another category of etches, plasma etching, ionizes liquid or gaseous chemical sources and directs a stream of the plasma towards the etch surface. Plasma etches are often more directional, meaning the etched features will not be widened beyond the etch mask. However, depending on etch parameters, plasma etches can cause damage to the etched devices or implant etchant atoms [153]. For Pd, there are a limited number of possible plasma etch chemistries that do not also etch silicon oxide, which would destroy the HSQ mask. One possible etch recipe that may be particularly selective against HSQ or aluminum oxide is an organic, methane-based etch [154]. Another possible etch is a chlorine or boron trichloride etch, although these etches tend to be a more physical than chemical etch process [155].

Finally, most materials can be etched well by an ion mill. Ion milling involves the acceleration of an inert ionized gas (typically argon) towards the etch target, resulting in the sputtering (etching) of the target. However, ion milling can result in significant damage to the substrate in the form of interface trap states [156]. Additionally, the etch selectivity of Pd over silicon oxide, when performed with the ion mill tool in the Wisconsin NFC, is only

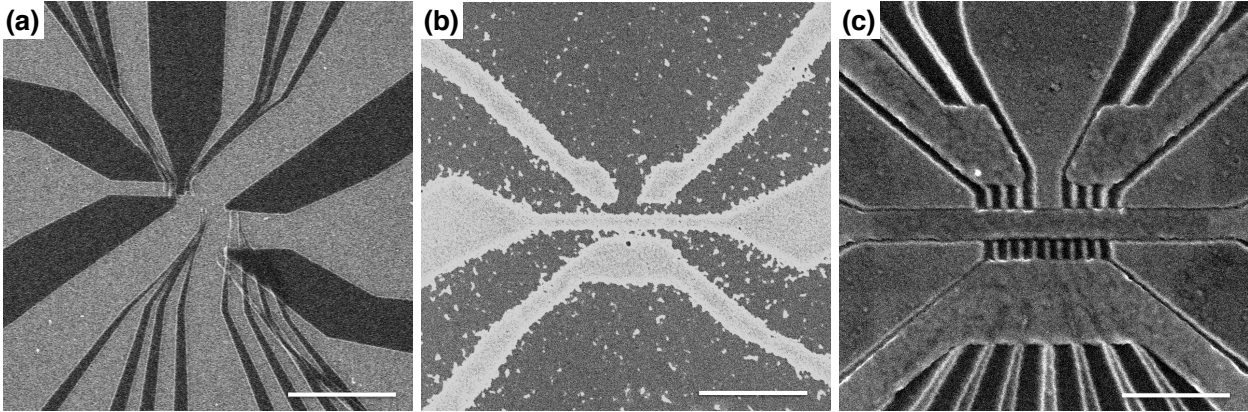


Figure 4.8: (a) SEM image of adhesion issues between HSQ and palladium, with a 1  $\mu\text{m}$  scale bar. This issue was solved with a polymer treatment to the palladium surface prior to HSQ deposition. (b) SEM image of etch issues with aqua regia and HF, with a 1  $\mu\text{m}$  scale bar. The first layer gate pattern is written in HSQ on a palladium surface and then etch transferred to the palladium with a dilute aqua regia etch. After a brief 10 second dip in dilute HF, the palladium metal appears to shed. (c) SEM image of a completed (but poorly etched) SPARTA device, with a 500 nm scale bar. Due to the thinness of the HSQ resist ( $\sim 40$  nm), the resist coverage over the first layer of gates is insufficient, resulting in complete removal of the second layer gate metal in those regions. A thicker HSQ layer or different etch process is needed for the second layer processing.

about a factor of 2. Despite this, ion mill etching was primarily used for the results shown here, including the etched first layer of gates shown in Fig. 2.7(c).

### 4.3.3 SPARTA Challenges

During the process development of SPARTA, several issues have surfaced, some of which have yet to be resolved. The first and most fundamental issue that arose is the adhesion of the HSQ to the Pd surface. HSQ fails to adhere well to Pd, and during development of the resist in solution, the exposed and cross-linked HSQ is prone to ‘float’ and reattach elsewhere. Figure 4.8(a) shows this adhesion issue on a test of the second layer of gates. The EBL dose is approximately correct, but the exposed HSQ has lifted off and shifted around the Pd surface. Fortunately, the adhesion of HSQ to various metallic surfaces has been investigated previously in Ref. [157]. In this report, a pre-treatment of a gold surface with select polymers improved the adhesion of HSQ. Here, we use poly (diallyldimethylammonium) chloride

(PDDA) to improve adhesion by submerging the Pd-coated substrate in an aqueous solution of this polymer prior to resist deposition. The successful patterning results in Fig. 4.7 were achieved with this surface pre-treatment method.

Although etching the first layer gates through a wet aqua regia process is promising, there have been unexpected chemical side-effects. Testing the aqua regia etch has been performed with a highly diluted solution (1:15 in water) and shown to successfully etch through the Pd at an acceptable rate (1 – 10 nm/min). However, when the HSQ mask is stripped in dilute HF (1:20), the patterned Pd appears to shed. This is shown in Fig. 4.8(b). The first layer gate pattern is clearly visible, but bits of Pd (light gray) have separated from the structure. The degree to which this occurs appears to be a function of time spent in the HF. It is possible that the aqua regia has penetrated the HSQ mask or the Pd, altering the etch resistance of the Pd in HF. Extended cleaning and rinsing of the sample between the Pd etch and the HSQ strip does not appear to improve the results. This phenomenon remains an open question.

With aqua regia causing unexplained issues, we rely exclusively on dry etches. As previously stated, ion milling was used for etch testing thus-far. While this was sufficient for the first layer etch, as shown in Fig 4.7(c), the thickness of the patterned HSQ is currently too thin for the second layer etch. Figure 4.8(c) shows a test device with the first and second layer gates fully etched. The second layer gate metal is nearly fully removed in the regions that overlap the screening gate layer. This is likely due to the HSQ resist thinning over the first layer gates during resist spinning due to the increased surface height. This effect could be mitigated by using a thicker film of HSQ, which is currently only  $\sim 40$  nm. In addition, switching to an etch process with greater selectivity against HSQ would reduce the chances of etching entirely through the resist layer.

SPARTA is a drastic departure from the standard fabrication processes currently used in the Eriksson group. Some fabrication issues are to be expected, and none of these presented limit the potential of SPARTA. Further process development with new designs, new materi-

als, or new processes could realize a fully fabricated and operational SPARTA quantum dot device. In particular, there may be a benefit to swapping the second layer of Pd gates with TiN gates deposited by atomic layer deposition. In this way, the second layer of gates could be deposited immediately following the ALD grown inter-layer dielectric without breaking vacuum. We hope that this work serves as motivation for future fabricators.

### 4.3.4 Fabrication Recipes for SPARTA

In this section, we present various fabrication recipes used during SPARTA testing.

#### Electron-beam lithography with HSQ

There are many different recipes for HSQ which have been proven to work using different bake temperatures and times, different electron-beam accelerating voltages and doses, and different development solutions, temperatures, and times. The recipe we present here was tested in the NFC cleanroom facility at UW-Madison and reflects the tools and processes available there. The HSQ used is a DOW Corning product named XR-1541, and is a 2% solution of HSQ in methyl isobutyl ketone (MIBK). The intended film thickness for this concentration is 30-60 nm and this recipe results in a  $\sim 40$  nm thick layer after development. HSQ is very temperature sensitive, and should be kept refrigerated at all times.

1. Thoroughly clean the surface that the HSQ will be deposited on. This typically involves solvent cleans and oxygen plasma ashes. The surface should be completely dry before HSQ deposition.
2. If depositing HSQ on a noble metal surface such as palladium, perform the surface pre-treatment described in the next recipe.
3. Working quickly but carefully, remove the HSQ resist from the fridge and apply drops of the solution to the sample mounted in a centrifugal resist spinner. Immediately spin

the sample at 5500 RPM and return the HSQ bottle to the fridge. Spin the sample for 30 seconds to create a thin film.

4. Bake the sample on a hot plate at 150 °C for 2 min, followed by another bake at 220 °C for 2 min.
5. As the time between resist spinning and electron-beam exposure can affect the dose, plan ahead and load into the electron-beam-lithography tool immediately.
6. Using a 100 keV EBL, the best dose for this HSQ process is around 2000  $\mu\text{C cm}^{-2}$ . Using proximity effect correction (PEC) software can improve dosing for patterns with tightly-packed large and small features. Expose the sample in the pattern desired.
7. The exposed HSQ is developed in a tetramethylammonium hydroxide (TMAH) solution. The chosen developer is Microposit CD-26, which is a 5% solution of TMAH with a 0.26N normality. Agitate the sample in CD-26 for 3 min, followed by a 3 min rinse in DI water with agitation. Blow dry with a nitrogen gun, but avoid acute angles with the sample (keep air flow perpendicular to sample surface). This is the step when adhesion issues may arise.
8. To increase etch resistance of the HSQ, the sample can be placed in a downstream plasma asher. Plasma ash at 250 W with 80 sccm  $\text{O}_2$  for 10 min.
9. To strip the exposed and developed HSQ resist, dip in dilute 20:1 buffered-oxide-etch hydrogen fluoride for  $\sim 15$  seconds, followed by a thorough DI water rinse and  $\text{N}_2$  dry.

### **Pre-treatment of a palladium surface for improved HSQ adhesion**

A polymer treatment of the palladium surface is performed prior to HSQ resist spinning to improve adhesion. The polymer used is PDDA: poly(diallyldimethylammonium chloride) in a water solution. For this work, PDDA was purchased from Sigma Aldrich at a concentration

of 20% PDDA in water by weight. The recipe for PDDA coating of a palladium surface is as follows.

1. Dilute the PDDA solution to  $\sim 2\%$  with DI water (15 mL PDDA solution + 150 mL H<sub>2</sub>O). Agitate the mixture and wait 5 min.
2. Briefly agitate the PDDA solution again. Gently submerge the palladium-coated sample into the solution and let soak for 15 min.
3. Remove the PDDA coated sample and briefly agitate in DI water. Too little agitation can leave too much PDDA on the surface, too much agitation can remove too much PDDA. Six ‘shakes’ in water seemed to yield good results.
4. Upon removal from rinse water, immediately dry with a strong blast of air from a nitrogen gun. It is critical that the excess PDDA is blown off the sample and does not leave dried water spots.
5. Bake the sample on a hot plate at 80 °C for 10 min.
6. Proceed with HSQ lithography (spin an HSQ film on the surface).

### **Ion-milling of palladium**

The ion mill available for this work uses an accelerated flow of argon atoms to sputter the sample and etch material from the surface. The sample mount is water cooled to avoid overheating of the sample. As mentioned in the HSQ recipe, a plasma ash prior to etching can improve the etch resistance of HSQ to the mill.

1. Load the sample into the ion mill chamber and pump the chamber below  $1 \times 10^{-6}$  torr.
2. Turn on the argon flow, at 2 sccm, resulting in a chamber pressure of  $\sim 5 \times 10^{-5}$  torr.
3. Follow the warm-up procedure of the tool to ensure good health of the filament. The milling parameters of the tool used for this work are as follows.

- Cathode filament current: 2.45 A
  - Discharge current/voltage: 0.13 A/38.0 V
  - Beam current/voltage: 15 mA/800 V
  - Accelerator current/voltage: 1 mA/160 V
  - Neutralizer emission current: 19 mA
  - Filament current: 5.14 A
4. Move the beam shutter and mill the sample for the appropriate amount of time. Palladium etches at about 5 nm/min.
  5. Vent the ion mill and remove the sample for further processing.

## Chapter 5

# Automation of Quantum Dot

## Measurements

As the complexity and utility of quantum dot devices increases, so does the challenge to control them. Even in the simplest designs, gate-defined quantum dot systems typically require at least three electrostatic gates per dot to control the dot's energy and coupling to other dots or reservoirs. Naturally, as the number of dots in a quantum dot system increases, the number of gate voltages to tune quickly becomes intractable for manual control. Thousands or millions of qubits are needed for the most exciting applications of quantum computers, [158–162]. In classical transistor integrated circuits, fabrication uniformity combined with intricate multiplexing allows for the drastic reduction of the number of control lines. For quantum dot devices in the near term, however, each gate voltage needs to be set and controlled individually.

Automation of initial device tuning and qubit control is a wide-ranging and growing field within quantum dot research. In this chapter in Sec. 5.1, we briefly present various automated tuning methods, including some which the Eriksson group is involved in advancing. The main topic of this chapter is the initial tuning of quantum dot devices into a regime in which other previously developed automation schemes can take over. We call this initial tuning ‘cold-

start tuning’, describing the process from the very first voltages set to the point at which charge-sensed quantum dots are formed. In Sec. 5.2, we present a detailed instruction set of the steps required for cold-start tuning. This is presented in a manner to aid in the scripting of these steps into an automated routine.

## 5.1 Auto-Tuning Methods

The tuning and control of quantum dot qubits is a large and complex task. Quantum dots are formed by precise control of electrostatic gates. The charge sensors are often quantum dots themselves. Qubits and multi-qubit gates are formed through control of the coupling, location, and occupation of these quantum dots. Each of these tasks requires dozen of decisions and voltage changes to control the gates. Presently, this is nearly always done heuristically, meaning a highly-trained researcher is responsible for these decisions. In the last several years, many different automation techniques have been developed to ease the burden of this wide-ranging set of tasks for control of quantum dot qubits.

### 5.1.1 Review of Automated Tuning Approaches

Published results on automated tuning methods have focused on different portions of the tuning requirements for quantum dots qubits. Some have focused on tuning *ab initio*, achieving a multi-dot system from initial voltage settings [163–165]. Others concentrate on the task of achieving a specific number of electrons in a quantum dot by identifying and counting transition lines [166, 167]. Creating a well-coupled double quantum dot system has been the target of work performed in collaboration between researchers at NIST and UW-Madison [101, 168]. With a double quantum dot system, there have been varying approaches to identifying and tuning the tunnel coupling between the dots and to the reservoirs [169–172]. Additionally, automated formulation of ‘virtual gates’ to ease qubit control has been demonstrated [173]. Finally, with well-formed and controlled qubits, there have been strategies presented for auto-

mated detection of single-shot readout and development of ideal multi-qubit gates [174,175].

The tools used for these automated tuning schemes vary. Some have relied exclusively on simple fittings, traditional computer vision techniques, and heuristically defined algorithms [163,167,169–171,173]. Alternatively, a host of machine learning based techniques have been utilized. Variational autoencoders (VAE), a type of deep generative modeling, have been used to characterize multi-dimensional voltage scans from sparse measurement to determine where next to measure or how to modify gate voltages for the desired tuning parameters [165,172,176]. Machine learning binary classifiers, in combination with traditional algorithms, have been used to separate well-performing and dysfunctional quantum dot devices [164]. Convolutional neural networks, which can be used to classify images, have been used to identify electron transitions in a quantum dot and classify the state of the system [166,177,178]. Smaller neural networks, such as deep neural networks with only a few fully-connected layers or feedforward neural networks, have also been used for quantum dot classification and electron transition identification, with the aim of ‘miniaturizing’ the required system for potential ‘on-chip’ implementation [168,179].

### 5.1.2 Automated Tuning Using Neural Network Classification of Quantum Dot States

The auto-tuning that we at UW–Madison have investigated and advanced, in collaboration with researchers at NIST, has focused on neural network approaches. One study utilizes a convolutional neural network (CNN), the other uses a smaller, fully-connected deep neural network (DNN). These are used to classify the state of a quantum dot system and tune to a desired state. The states are defined as the presence and location of dots in a double quantum dot system, *i.e.* electrons in a coupled double quantum dot, electrons confined to a single quantum dot, or no confined electrons at all.

The CNN approach uses two-dimensional scans of the two plunger gates in a double quantum dot device and classifies a small voltage scan ( $< 100 \text{ mV} \times 100 \text{ mV}$ ) as a double

dot, central single dot, single dot primarily coupled to a single plunger, or no dot (no transitions). The CNN is trained using data generated from a Thomas-Fermi calculation of typical quantum dot devices, which allows for a virtually unlimited amount of training data [178]. This state classification is used in tandem with an optimization routine to tune the gate voltages and move from one state to another (*e.g.* from a single dot to a double dot). This was used successfully in a live tuning session of a silicon quantum dot device [101]. This technique is limited by the differences between training data and real data, in particular, by the lack of noise in the training set. Adding various noise sources to the training data is currently under investigation, and shows improvement to the classification accuracy [180]. Another limitation to this approach is that collecting two-dimensional data is inherently more time consuming than one-dimensional scans.

The DNN approach aims to reduce the demands of data collection by collecting sparse one-dimensional voltage scans in higher dimensional gate space [168]. We call these voltage scans which emanate from a central point ‘rays’ and identify locations of charge transitions in the direction of the rays. The closest transition to the starting point of each ray is fed into a simple DNN with three hidden layers. The DNN is trained on rays generated from the same simulated data as the CNN approach. The output similarly describes the quantum dot state at the voltage point of the rays’ origin. Using the ray-based approach, the data collection can be reduced by  $\approx 70\%$  compared to the CNN approach while maintaining a high classification accuracy of  $\approx 90\%$ . This tuning method again uses an optimization routine to tune the voltages to the desired state. In addition to the reduction in required data collection, the ray-based approach more naturally extends to higher dimensions to include the tuning of barrier voltages or additional quantum dot gates. Theoretical bounds on the number of rays needed to classify a system in arbitrary higher dimensions have been devised [181].

Both of these neural-network tuning methods require a tuned charge sensor that is sensitive to the dots. Additionally, they require that the dot gate voltages are preliminarily tuned such that simple changes result in visible quantum dot transitions. The quantum dot

device must then already be determined to have well-functioning gates, tuned quantum dots, and tuned sensors. The next section focuses on the early tuning steps required to bridge the gap between the initial device turn-on and a voltage configuration which is ready for these neural network approaches.

## 5.2 Bridging the Gap Between Device Turn-On and Dot Manipulation: Cold-Start Tuning

In this section, we present the cold-start tuning procedure for a triple quantum dot device with the overlapping aluminum gate architecture. The end result of this tuning should provide a sufficient starting point for the neural-network based classification and tuning algorithms previously described. This device design, shown in Fig. 5.1, has two main dot channels, one for a charge sensor and the other for the triple dot system. Some of these steps are specific to the gate design and may require adaptation for use in other designs. The data presented here is acquired in the device described in Sec. 3.4. This section is designed as a tuning guide, but also as an instruction set that could be coded into an automated routine. For this reason, each step includes a discussion of fitting procedures or analysis scripts required to advance to the next step. Scripting these tuning steps obviously requires adequate measurement and scripting tools. A suggested software solution is Labber, which has python APIs for measurement scripting and is currently used in the Eriksson group [182].

Throughout these measurements, information about the functionality of the device such as turn-on voltages, amplifier biases, and gate tunings should be collected. It may be beneficial to store a library of meta-information containing gate names, the function of gates, and various information learned about each gate as tuning progresses. The results of early measurements are used to inform later measurements.

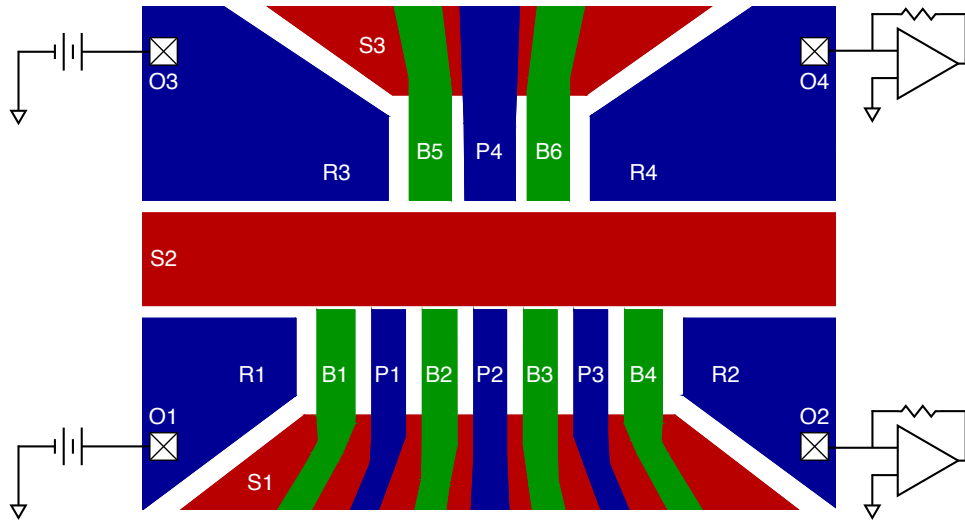


Figure 5.1: Example gate design for a triple dot device. This gate architecture is used as an example for cold-start tuning. All gates and voltage sources are labeled with standard names: screening (S), reservoir (R), plunger (P), barrier (B), and ohmic (O). The upper channel of this device is used as a charge sensor for the lower channel dots. The two ohmics on the left are used to source a voltage bias. The two ohmics on the right are used to measure the current with current pre-amplifiers.

### 5.2.1 Initialization

For this cold-start tuning routine, we aim to require as little prior knowledge of the device as possible. However, we make a few early assumptions. First, we assume the quantum dot device is loaded and cooled in a cryostat, with each gate and ohmic connected to dedicated voltage sources or current amplifiers. Using the triple dot device shown in Fig. 5.1 as an example, we assume ohmics O2 and O4 are connected to current pre-amplifiers and ohmics O1 and O3 are connected to voltage bias sources. The voltage sources for each gate should be selected with care; some gates, such as the plunger gate for a charge sensor, should be capable of very small voltage steps, useful for compensation of the charge sensor tuning. We also assume that preliminary gate leakage tests have been performed, such that we do not anticipate any gate-to-gate or gate-to-2DEG current flow. All gate voltages and ohmic biases are initially set to zero. For scripting, we assume that information about the function and location of each gate is passed to the auto-tuner.

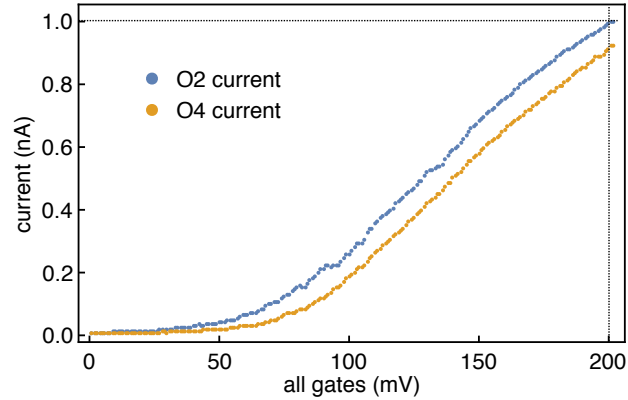


Figure 5.2: For global turn-on, all gate voltages are swept from 0 V to positive voltage while the current through O2 and O4 are measured (blue and orange points). For this measurement, the turn-on voltage is approximately 50 mV. The measurement is terminated when either current passes the set threshold, here set to 1 nA. With 100  $\mu$ V biases on each source ohmic (O1 and O3), this corresponds to  $\approx 100$  k $\Omega$  of resistance in the current paths.

## 5.2.2 Global Turn-On

The very first measurement of cold-start tuning is a ‘global’ turn-on of the entire device to uniformly accumulate a 2DEG underneath all gates. A small ( $\sim 100$   $\mu$ V) voltage bias is applied to both O1 and O3. All gate voltages, initially set to zero, are swept together to positive voltages while measuring the current flow into both O2 and O4. As the voltages are increased, a 2DEG should form in the device and current will flow between ohmics. This measurement can be terminated when the current in either amplifier reaches a threshold value. Terminating a measurement sweep upon crossing a measured threshold is a built-in feature within Labber.

An example global turn-on curve is shown in Fig. 5.2. For this measurement, the turn-on voltage is quite low, around or below 50 mV. The current through both measured ohmics, O2 and O4, is very similar, which indicates that 2DEG formation across the device is relatively uniform. The measurement is terminated at 200 mV, when the current through either ohmic surpasses 1 nA. For a 100  $\mu$ V bias, terminating the measurement at 1 nA would correspond to a resistance of 100 k $\Omega$ . If the current through each measured ohmic were very different, a new measurement could be run to continue increasing all gate voltages until all measured

currents reach a sufficient threshold. The turn-on voltage can be determined as the global gate voltage at which a sufficient current flows, *e.g.*, 50 pA. The separation in voltage between the turn-on current threshold and the measurement termination current threshold (50  $\rightarrow$  200 mV) will be used for determining the voltage range of later measurements. We call this the ‘global turn-on distance’, equal to 150 mV for Fig. 5.2.

### 5.2.3 Center Screening Gate Pinch-Off

In the standard overlapping aluminum gate design, there are two main channels for quantum dots, one for qubits and the other for charge sensors. A screening gate, labeled S2 in Fig. 5.1, is used to divide these channels. We want to isolate these two channels, so that we can determine individual turn-on voltages of reservoirs and finger gates, as well as bias offsets in the current pre-amplifiers.

To do so, the S2 gate voltage is swept to negative voltages while all other gate voltages remain at the final positive value of the global turn-on measurement. The voltage range to sweep S2 can be determined from the earlier measured global turn-on. Sweeping over a voltage range 3 – 4 $\times$  larger than the global turn-on distance is likely sufficient. At some low or negative voltage, the 2DEG underneath S2 will be depleted, leading to an increase in the resistance between the two sides of the device. This is effectively a turn-on curve for S2, but in reverse, leading to the name ‘pinch-off’. As the resistance between the two current paths rapidly increases, the overall current flow into each measured ohmic will change. This S2 pinch-off is shown in Fig. 5.3(a). Above pinch-off voltages, the two measured currents may slowly change with changing S2. Below pinch-off,  $-100$  mV in this figure, the current on either side is mostly unaffected by any further change to S2, as the accumulated S1 and S3 gates provide sufficiently wide low-resistance current paths.

Figure 5.3(b) shows numerical derivatives of the S2 pinch-off curves (smoothed with a moving average) in Fig. 5.3(a). At the pinch-off voltage, there is a large maximum (or minimum) as the resistance of each current path rapidly changes. These features can be used

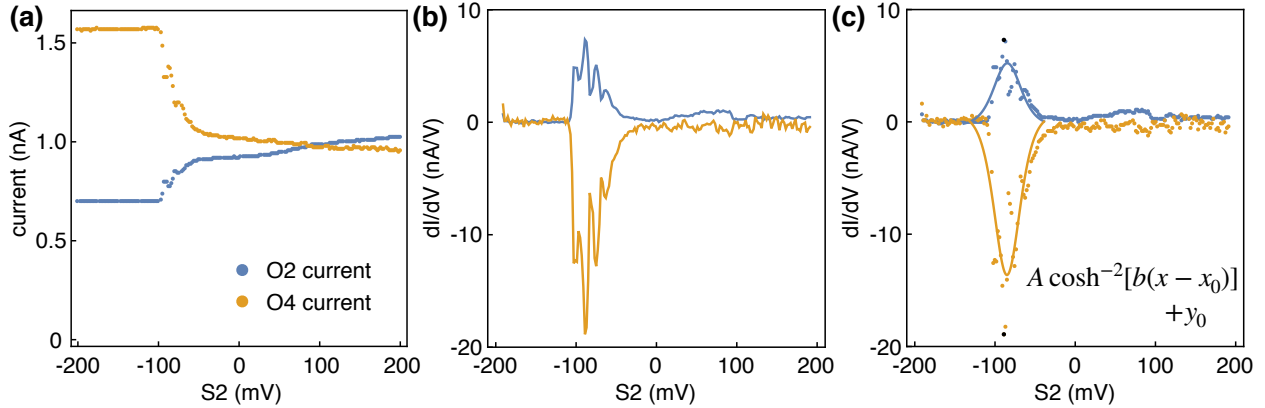


Figure 5.3: (a) Pinch-off of the central screening gate S2. Current through both sides of the quantum dot system (qubit and sensor sides) is measured as S2 is swept to negative voltages. At sufficiently low voltage, the resistance between each current path rapidly approaches infinity, isolating the two sides. The resistances of each current path changes, resulting in an abrupt and related change in the current through each measured path. This occurs here in the  $-50$  to  $-100$  mV range. Below pinch-off, the current through either side of the device is relatively independent of the S2 voltage. (b) Numerical derivative of the measurement in (a). The data is first smoothed with a 10 point moving average. Pinch-off of S2 occurs when the rapid changes in current flow on either side are correlated and opposite. (c) Fits (lines) to the differentiated data (points) around the point of maximum current change (black points). The fitting function is shown in the lower right.

to determine the pinch-off voltage for the central screening gate. Each current path should show large and opposite signed peaks in the differentiated signal at the pinch-off voltage. This can be determined automatically by selecting the point at which the sum of the squared  $dI/dV$  values of the two currents is maximum, shown in Fig. 5.3(c) by the black points. The differentiated pinch-off curve can be fit around these points using a  $\cosh^{-2}$  function, shown by the solid lines in Fig. 5.3(c). After this measurement, the S2 voltage can be set to a value sufficiently lower than pinch-off, determined by the width of the fits.

## 5.2.4 Ohmic Sweeps and Bias Compensation

DC current measurement in the Eriksson group is often achieved with the use of a current-to-voltage pre-amplifier, specifically the DL/Ithaco 1211 current pre-amplifier. These pre-amplifiers, as with most ammeters, are intended to have a low input resistance and are

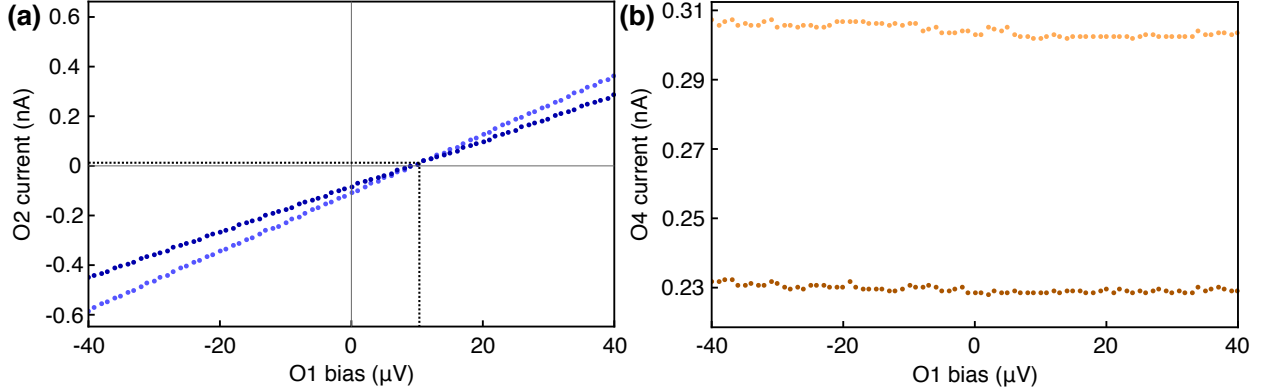


Figure 5.4: (a) O2 current as a function of O1 voltage bias for two different voltages on all gates except S2, which is pinched-off. The darker points are measurements at higher gate voltages. The slopes of these lines correspond to the resistance of the path. The intersection of the two curves, indicated with dashed lines, determines the voltage and current offset of the current pre-amplifier used to measure the O2 current. (b) O4 current as a function of O1 voltage bias for the same two sets of voltages on all gates in (a). The darker points are measurements at higher gate voltages. As S2 is fully pinched-off, the current through O4 is independent of the voltage bias on O1.

set to have zero voltage bias across the input such that the input is an effective ground. In practice, these current pre-amplifiers often have a small, but non-negligible voltage bias across the input. For accurate measurements of the resistance of a current path, we need to know and compensate for this unintended voltage bias.

With the central screening gate pinched off, each side of the device (qubit and sensor) is isolated so that each current path has a single source ohmic (O1 or O3) and a single drain ohmic (O2 or O4) where the current is measured. By independently varying the source bias and the resistance of the current path, we can determine the input voltage bias of the current pre-amplifier. This process is shown in Fig. 5.4. For the qubit side (bottom of Fig. 5.1), the source ohmic bias, O1, is swept, resulting in a linear slope of the current through O2 corresponding to the resistance of the path. The voltages on all gates (except S2) during this sweep are set to the terminating voltage of the global turn-on measurement. Reducing the voltages on these gates will increase the resistance of the device. Sweeping the bias on O1 again results in a different slope. These two measurements, before and after a change

to the gate voltages, are shown in Fig. 5.4(a). Ideally, these two curves should intersect at the origin. However, since the pre-amplifier reading the current through O2 has an intrinsic voltage bias, this intersection is shifted horizontally. This horizontal shift represents the amount the O1 bias must be adjusted to cancel out the bias from the pre-amplifier. Thus, the pre-amplifier voltage bias is the negative of this horizontal shift, approximately  $-10 \mu\text{V}$  for the data in Fig. 5.4(a). In addition to the voltage offset, there is typically a small current offset as well. This results in the intersection not occurring exactly at zero current.

These ohmic bias sweeps serve a second purpose as well. As the two sides of the device should be isolated after pinch-off of the central screening gate, the current through one side should be unaffected by changes in voltage bias of the other side. Figure 5.4(b) shows the current through the sensor side of the device as O1 is swept. The slopes are very flat, and so the resistance between the two sides is extremely high, as expected and desired.

For scripting of this tuning step, simple linear fits to the ohmic bias sweeps will suffice to determine voltage and current offsets of the current pre-amplifiers. The resistance of the S2 pinch-off can be calculated from the slopes of the current in the opposite channel. If a measurement fails to meet a set threshold, the voltage on S2 could be lowered and this step could be repeated.

### 5.2.5 Individual Channel Turn-On

With each channel isolated and the voltage offsets known, better estimations of the resistances of the current paths are possible. To ensure sufficient 2DEG accumulation in each channel, it is best to raise all voltages until a low resistance is achieved. This step is nearly identical to the global turn-on step, but only gates for a single channel are swept. For example, for the charge sensor channel, gates R3, R4, B5, B6, P4, and S3 would be swept. All other gates, including S2, would remain at their previous values. With the voltage offset measured in the previous step, the ohmic bias, in this case O3, would be set so as to achieve a known total voltage bias. Then, the resistance of the current path simply follows Ohm's

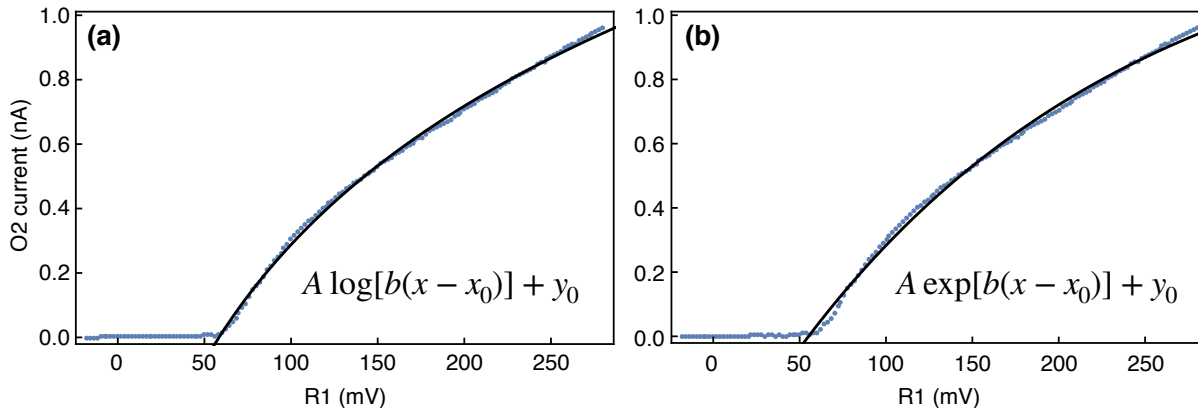


Figure 5.5: (a) Pinch-off curve for the reservoir gate R1, with a logarithmic fit to the non-zero data. (b) Same pinch-off curve as in (a), with an exponential fit.

law. The voltages in each channel are raised until a current threshold is reached. Although expected resistances will vary between devices and gate designs, increasing accumulation until the channel resistance is  $< 50 \text{ k}\Omega$  has been adequate in previous tests.

As the end result of this step may be increased voltages on many gates, it is prudent to re-measure the central screening gate pinch-off value. The procedure in Sec. 5.2.3 would be repeated again, to account for the possibility that the increased nearby voltages caused a change in the pinch-off behavior.

## 5.2.6 Individual Reservoir Turn-On / Pinch-Off

As tuning progresses, we move closer to understanding the behavior of individual gates. Under- or over- accumulated gates can affect the performance of nearby gates. For example, if a reservoir gate voltage is set too high, the barrier gate directly next to it may struggle to pinch off. Knowing this, we want to individually test the pinch-off of the reservoir gates. This is a simple process. The voltage on a reservoir gate is individually lowered until the current in the channel containing that reservoir drops below a specific threshold. The voltages on the reservoirs are then returned to the initial higher value determined in the previous step and the process is repeated for each additional reservoir gate. The pinch-off voltage could be determined simply from this current threshold.

This process is shown in Fig. 5.5 for the R1 reservoir gate. Both sub-figures show the same data but with different fits to the data in the region with non-zero current. Because the reservoir gates are large and taper significantly from the ohmic contacts to the dot region, the pinch-off is gradual. Both the logarithmic and exponential fits adequately match the curvature of the data. These fits may be useful to extract a better pinch-off voltage or determine the voltage to set for a specific resistance. In the high-voltage limit, these fits behave very differently, as the exponential fit will asymptote while the logarithmic fit will not. If the extrapolation to a saturation current is desired, the exponential fit is advantageous.

### 5.2.7 Triangle Plots

At this stage of the tuning process, each side of the device is fully accumulated, including the large screening gates S1 and S3. The function of the screening gates in this design is to locally deplete the 2DEG, such that only a narrow channel of conduction exists where the dots will form. The tuning steps in this subsection create these narrow current channels. The best way to visualize the formation of this narrow accumulation between the depleted screening gates is with a ‘triangle plot’. A triangle plot is a two-dimensional scan of both screening gates that define a channel, shown schematically in Fig. 5.6. Both gates naturally have a pinch-off voltage such that no current flows underneath the gate below that value. If current can flow *in-between* the gates, that current will be approximately evenly affected by the voltages on either gate. Thus, this region of current corresponding to conduction through the dot channel has a triangular shape, as shown in Fig. 5.6(b). We now describe an efficient method of choosing screening and finger gate voltages to achieve this narrow conduction channel which requires only three one-dimensional voltage sweeps.

#### Screening Gate Pinch-Offs

First, the pinch-off voltages for each screening gate must be determined. The pinch-off voltage for the central screening gate, S2, has previously been determined in Sec. 5.2.3, but

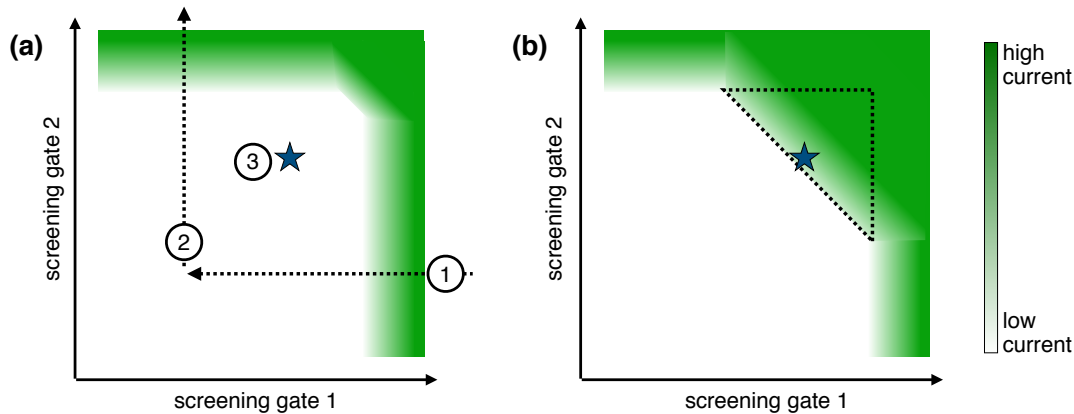


Figure 5.6: (a) Schematic of a typical triangle plot in the limit of no conduction through the narrow dot channel below screening gate pinch-off. The green regions represent current flow, with more current above the pinch-off values for the two screening gates. To achieve current flow only through the narrow channel between the screening gates, three one-dimensional scans are taken. The first two measurements (labeled with ① and ②) are scans of the pinch-off curves for each screening gate. Once the pinch-off voltages are determined, the screening gate voltages are set to values significantly below pinch-off, labeled with the star. The third measurement, labeled with ③, increases the voltages of all finger gates in the channel until current flows. (b) Schematic of the triangle plot after measurement ③. The dashed triangular region represents current through the narrow channel while both screening gates are pinched off. The star now represents an appropriate operating voltage point for dot formation.

could be repeated. For each pinch-off curve, the voltage on the other screening gate should be placed well below pinch-off. This is shown schematically in Fig. 5.6(a) with the two dotted lines. An example pinch-off curve of the S1 screening gate is shown in Fig. 5.7(a). The pinch-off voltage could be determined simply by a threshold current value. A more advanced method is to fit this curve. The dotted line in Fig. 5.7(a) shows a logistic fit to the data. A sigmoid-shaped fitting function is appropriate for sharp pinch-offs of screening and finger gates. This fitting procedure could be advantageous to determine the ‘width’ of the pinch-off curve. The voltages on the screening gates are then positioned in the pinched off region (starred point in Fig. 5.6). The voltage placement can be determined by the pinch-off width. For example, an appropriate pinched off screening gate voltage would be below pinch-off,  $1 - 2 \times$  the width of the pinch-off curve. Following this tuning procedure, this voltage configuration will likely not allow any current flow through the narrow channel, as shown in

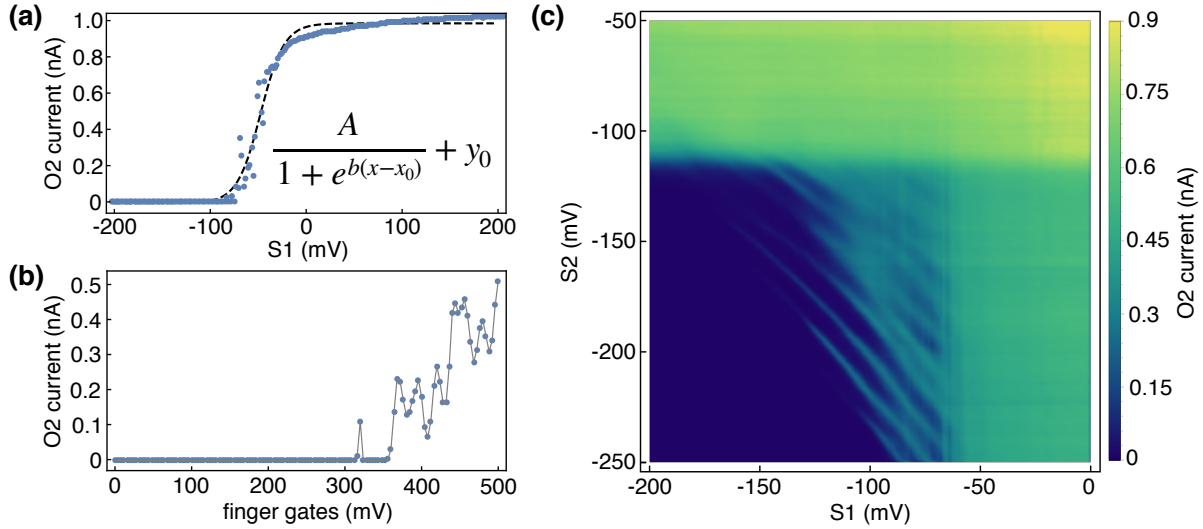


Figure 5.7: (a) Example pinch-off curve for the large screening gate of the qubit channel, S1. The dotted line is a logistic fit to the data using the function shown. (b) Example turn-on curve for conduction through the dot channel with both screening gates pinched off. The gray line connects the data points. This turn-on curve shows evidence of Coulomb blockade oscillations, as the channel is very narrow. (c) Example triangle plot of the qubit dot channel. The large rectangular regions to the right and top represent current flow underneath S1 and S2, respectively. At voltages below these regions, current flows through the narrow channel, as evidenced by the diagonal features. At very low voltages, no current flows.

Fig. 5.6(a). These screening gate voltages are the operating points for dot formation.

### Narrow Channel Turn-On

With no current flowing underneath either screening gate, we now need to accumulate a 2DEG in the narrow channel between them. This is achieved by increasing the voltage on all finger gates in the channel until current flows. For this gate design, the screening gate layer is the first deposited, closest to the heterostructure surface. Therefore, increasing the finger gate voltages should not affect the electric field underneath the screening gates, as they ‘screen’ any voltages that are applied above them. Figure 5.7(b) shows an example turn-on curve for the narrow channel. This turn-on curve is not as smooth as previous scans, as the narrow channel is prone to quantum behavior (quantized conductance plateaus or Coulomb blockade oscillations). The terminating voltage for this scan can be determined by a simple

current threshold.

### Full Triangle Plot

With both screening gates pinched off and current flowing through the narrow channel, we have achieved the desired current path. Figure 5.7(c) shows an example triangle plot with the desired conduction behavior. The diagonal features below pinch-off of each screening gate is current through the narrow channel. The striped nature of this current is evidence of Coulomb blockade oscillations. The slope of these features indicates that each screening gate equally affects the current through the channel, as expected. An appropriate operating point is centered in this triangular region. For scripting purposes, this two-dimensional scan is not necessary, as the terminating voltages of the previous step is the desired operating point, but can be useful as an audit of the performance of this channel tune-up process. We note that this channel accumulation procedure needs to be performed for both channels.

### 5.2.8 Finger Gate Pinch-Offs

With the narrow channel accumulated by the finger gate voltages, we now determine the individual pinch-off voltages for each gate. This is useful for setting up the approximate voltages needed for dot formation. Additionally, the finger gates are the most susceptible to ESD damage, poor alignment, or insufficient step coverage during fabrication which can affect gate performance. If gates show no pinch-off of the current, it may be due to these fabrication defects and grounds for rejection of the device.

The finger gate pinch-off is identical to earlier pinch-off measurements. Each finger gate is individually swept to lower or negative voltages until no current flows through the device. These pinch-off curves can look very different, due to their location (proximity to a reservoir) or fabrication discrepancies. Figure 5.8 shows pinch-off curves for four different finger gates. In Fig. 5.8(a-c), all three finger gates pinch-off, but with very different behavior. Figure 5.8(d) shows an example of a finger gate which fails to pinch-off, likely due to a break in the gate

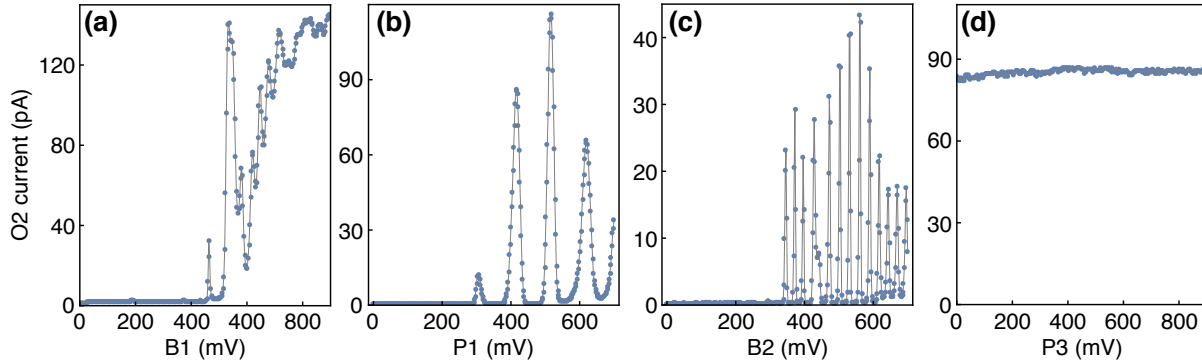


Figure 5.8: (a) Pinch-off curve for finger gate B1, showing some Coulomb blockade oscillations. (b) Pinch-off curve for finger gate P1, showing Coulomb blockade oscillations with likely a small lever arm between the gate and the dot. (c) Pinch-off curve for finger gate B2, with rapid Coulomb blockade oscillations, indicating a large lever arm between the gate and the dot. (d) Failure to pinch-off current with P3, likely due to a disconnected or poorly fabricated gate.

because of ESD damage or some fabrication error.

Automated analysis of these pinch-off curves is significantly more difficult than earlier steps. A simple threshold current to determine pinch-off may be acceptable for future measurements. For example, setting all finger gate voltages near, but above the pinch-off voltages should allow for quantum confinement with any particular pair of gates. However, more advanced detection of Coulomb blockade oscillations may be beneficial.

### 5.2.9 Wall-Wall Plots

Tuning up individual dots can be easily achieved through a ‘wall-wall plot’ (name originating in the Charlie Marcus research group). This is a two-dimensional plot of the barrier gates on either side of a plunger gate. With just the narrow channel accumulated and all finger gates set near to the pinch-off values, Coulomb blockade oscillations should be possible by reducing these barrier gate voltages to lower the tunnel rates into the dot and laterally define its extent. This is shown in Fig. 5.9(a) for the charge sensor side of the device. At high barrier voltages, the current flows through the dot freely. As the voltages are lowered, Coulomb blockade oscillations appear, and eventually current through the dot is blocked.

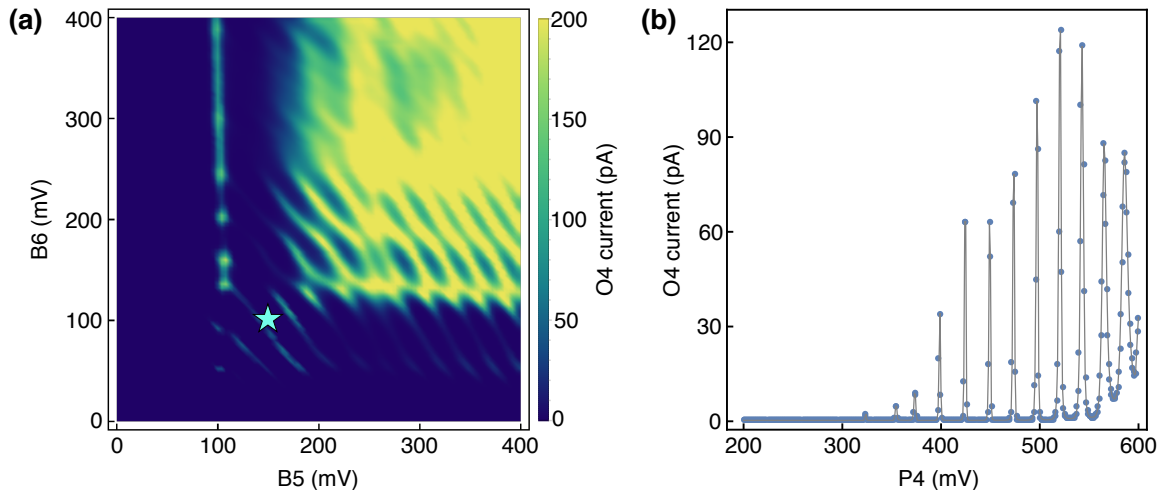


Figure 5.9: (a) ‘Wall-wall’ plot of the charge sensor dot barrier gates. The current through the dot is large at high voltages with large tunnel rates. At lower voltages, Coulomb blockade oscillations become more apparent as the tunnel rates lower. At sufficiently low voltages, the current through the dot is cut off. (b) Voltage sweep of the charge sensor plunger gate, with the barriers B5 and B6 operated at the starred point in (a). Strong Coulomb blockade oscillations are present, indicating this tuning is sufficient for operation as a charge sensor.

The range of voltages to sweep can be determined by the pinch-off locations and widths determined in the previous step.

The intent of this wall-wall plot is to determine suitable voltages for the barriers such that tunneling through the dot is finite. Advanced image analysis tools such as a linear Hough transformation (available in scikit-image python library [183]) may be able to identify the characteristic diagonal lines of the Coulomb blockade oscillations which occur under the plunger gate. This method would also allow for analysis of the slope of the oscillations with respect to the barrier gates, which can give insight into the lateral location of the dot. A simple current threshold may give an approximate location for dot operation.

Once the barrier voltage points are selected, a one-dimensional plunger sweep should reveal Coulomb blockade oscillations. Figure 5.9(b) shows this measurement for P4, with the barrier voltages set to the point shown by the star in Fig. 5.9(a). This process can be repeated for each plunger gate. If multiple plunger gates lie in the same channel, as on the qubit side of this device, the finger gate voltages should be returned to the values set in the

previous step after each dot formation because multi-dot formation will only allow current at triple points (see Sec. 2.3.7).

### 5.2.10 Transition to a Charge-Sensed Quantum Dot System

The end goal of this cold-start tuning is to achieve a system in which a more complex auto-tuner can take control, such as the deep-neural-network schemes described in Sec. 5.1.2. For these auto-tuners, the qubit dot channel must be charge sensed and in a voltage regime where dots can form. The end result of the previous tuning steps should be a charge sensing dot with strong Coulomb blockade oscillations and a dot channel with known barrier and plunger voltages to form individual dots. An operating voltage of the charge sensor plunger is easily achieved by selecting the highest sloped point. As described in Sec. 2.3.4, changes to qubit gate voltages affects the charge sensor due to the cross capacitance between all gates and dots. Measurements of the cross capacitance between qubit gates and the charge sensor dot allow for determination of a compensating voltage change of the charge sensor plunger to maintain adequate sensitivity.

Therefore, following this cold-start procedure should prepare the system for advanced auto-tuners. This can also be used as a device-screening process to determine which devices should be used for qubit formation and which devices should be discarded. In this intermediary stage of quantum dot device complexity and reproducibility, many devices may need to be fabricated and measured for viability before a fully functioning device is found. This initial tuning procedure, which only needs DC voltages and DC current measurements, may be suitable for a cryoprobe system which can measure many quantum dot devices in a single cooldown [184]. We hope that this section can be used as a guide to create an automated tuning procedure as well as helpful to those learning about tuning quantum dots.

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