Progress towards two-qubit devices in Si/SiGe heterostructures

by

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Abstract

Since being proposed almost 40 years ago, scientists across many disciplines have made great progress in the fields of quantum computation and quantum information. Instead of a classical bit (0 or 1), a quantum computer uses a two-level quantum system as a quantum bit or qubit. By controllably manipulating the quantum-mechanical properties of these qubits, a quantum computer could, for example, be used to simulate other, less well understood quantum systems, or to run certain classes of quantum algorithms that cannot be run on classical hardware.

In order to build a quantum computer, certain basic requirements must be met. As with a classical computer, logic gates are necessary to controllably manipulate qubits to perform calculations. One such requirement for a universal quantum computer is a two-qubit logic gate. This is an inherently quantum mechanical gate, which has no classical analog. For example, the controlled-not two-qubit gate will perform a not operation on the target qubit if and only if the control qubit is $|1\rangle$, else it does nothing to the target qubit. In either case, the control qubit is left unchanged and unmeasured. Being able to perform this gate with high fidelity is critical to creating a quantum computer.

In this dissertation, I present progress towards fabricating, characterizing, and manipulating two-qubit devices in Si/SiGe heterostructures. First, I motivate the use of quantum dot qubits hosted in Si/SiGe as a suitable platform for quantum computing. Then, I present characterization of Si/SiGe substrates and discuss fabrication of a quantum dot device. Next, I outline the electronics set up for measuring a quantum dot device in a dilution refrigerator. I then present results of two, published experiments which explore multi-qubit systems: one which demonstrates controllable tunnel coupling between a quantum dot an a nearby localized impurity, and the other which demonstrates state-conditional Landau-Zener-Stückelberg oscillations between capacitively coupled double quantum dots in a quadruple quantum dot device. Next I discuss fabrication and characterization of micromagnets for spin qubit applications. I finally conclude by discussing future research avenues towards realizing a robust, multi-qubit device in silicon.

Acknowledgements

Contrary to what television or movies may lead you to believe, science is a team sport. In team sports, despite how much you prepare individually, the only way to succeed is with the equal hard work and support of the the rest of your teammates and coaches. The same is true for science and especially for my graduate career. What I have accomplished would not have been possible without the help of a great many people. By providing scientific, technical, or emotional support as needed, I was able to successfully receive a Ph.D. and for that, I'm extremely grateful.

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Chapter 1

Introduction

1.1 A brief discussion of quantum computation

Computers are a cornerstone of today's society. Nearly every facet of our daily lives (professional, recreational, educational, etc.) requires interaction with a computer in some form or another. In each of these computers, the fundamental unit for information storage and computation is called a bit (from: binary digit). A bit can be in one of two states: 0 or 1. Physically, 0 and 1 typically correspond to low (near 0V) and high (∼5-15V) voltages in a CMOS circuit, or the orientation of the magnetic moment of a domain of some magnetic medium (e.g. a hard drive). Manipulation of bits is carried out by logic gates created from silicon transistors. By grouping billions of these transistors together in a processor, huge numbers of bits can be manipulated to perform the complex calculations required of the computer.

Similar to a classical bit, a two-level quantum bit (qubit) is described by its two basis states $|0\rangle$ and $|1\rangle$. Unlike a classical bit, a qubit state vector $|\psi\rangle$ is a linear superposition of the two states, [1]

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle, \tag{1.1}$$

where α and β are complex numbers satisfying the normalization condition $|\alpha|^2 + |\beta|^2 = 1$. Given these constraints, a qubit can be represented geometrically by the position of a vector on a 3-dimensional unit sphere called a Bloch Sphere. As shown in Fig. 1.1, the logical basis states $|0\rangle$ and $|1\rangle$ are placed on the poles of the sphere. In this representation, the qubit state can instead be

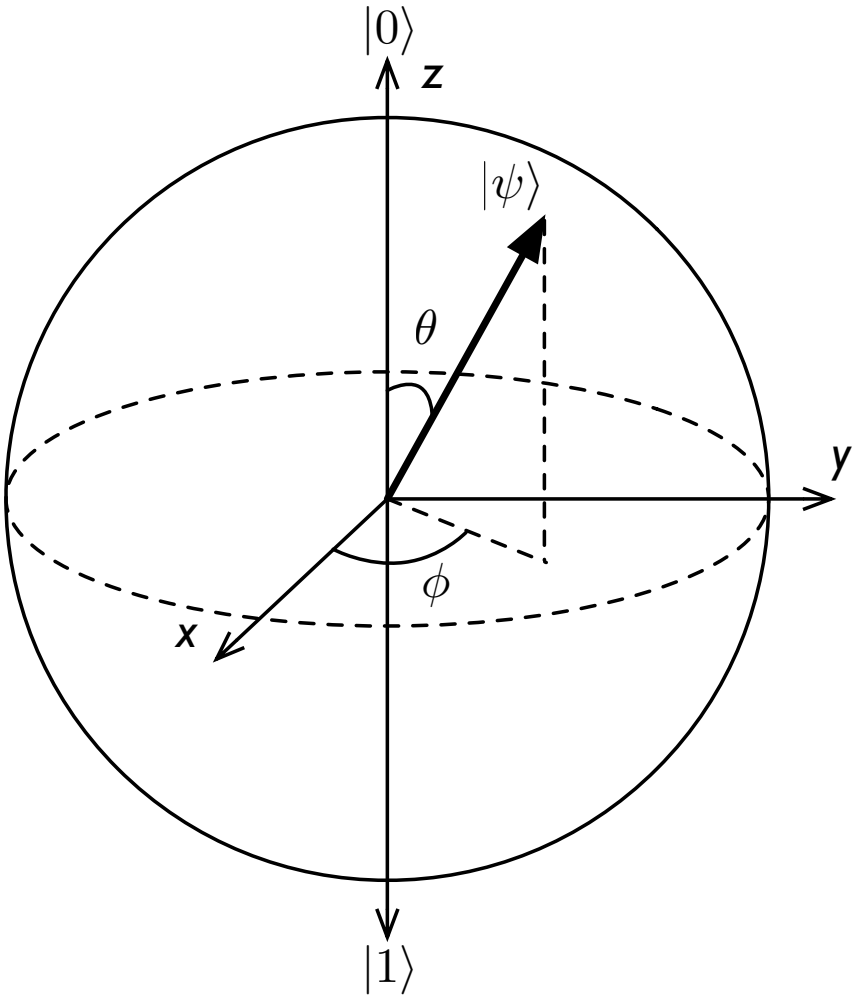

Figure 1.1: The Bloch sphere. A geometric representation of a qubit as a three dimensional unit sphere with the basis states $|0\rangle$ and $|1\rangle$ on the poles. The qubit state $|\psi\rangle$ can be written in terms of its position on the Bloch sphere as $|\psi\rangle = \cos\left(\frac{\theta}{2}\right)|0\rangle + e^{i\phi}\sin\left(\frac{\theta}{2}\right)|1\rangle$.

written as,

$$|\psi\rangle = \cos\left(\frac{\theta}{2}\right)|0\rangle + e^{i\phi}\sin\left(\frac{\theta}{2}\right)|1\rangle, \tag{1.2}$$

where θ and ϕ are real numbers.

Further deviation from classical bit behavior occurs when we consider measurement of the qubit. In a classical system, the bit is either a 0 (off) or a 1 (on). For a qubit, however, $|\psi\rangle$ is described by the linear superposition of our two basis states. This means we have a probabilistic chance of measuring $|0\rangle$ or $|1\rangle$. Put another way, if we were able to prepare many copies of our qubit $|\psi\rangle$ and measure each one, we'd obtain the result $|0\rangle$ with probability $|\alpha|^2$ and $|1\rangle$ with probability

$|\beta|^2$. Furthermore, measurement of each qubit collapses the quantum state. Suppose we prepare a new qubit $|\psi'\rangle = \alpha'|0\rangle + \beta'|1\rangle$, measure it, and obtain a result $|0\rangle$. If we then immediately remeasure this qubit, we obtain $|0\rangle$ with 100% probability. This loss of quantum information when measuring a qubit must be accounted for and leads to complications when considering initialization, manipulation, and readout techniques.

Similar to the classical case, qubits are manipulated with quantum gates. A 1-qubit gate is described by a unitary matrix operation (e.g. the Pauli gates). These gates differ from classical ones in that they are reversible. 1-qubit gates are not sufficient, however, for a quantum computer. Two-qubit gates are also necessary.

As with the one qubit case, we can write an arbitrary two-qubit state $|\psi'\rangle$ in terms of its four basis states,

$$|\psi'\rangle = \alpha_{00}|00\rangle + \alpha_{01}|01\rangle + \alpha_{10}|10\rangle + \alpha_{11}|11\rangle, \tag{1.3}$$

where we have a similar normalization condition $|\alpha_{00}|^2 + |\alpha_{01}|^2 + |\alpha_{10}|^2 + |\alpha_{11}|^2 = 1$. A two-qubit logic gate is an inherently quantum mechanical gate which has no classical analog. For example, the controlled-not two-qubit gate will perform a not operation on the target qubit if and only if the control qubit is $|1\rangle$, else it does nothing to the target qubit. In either case, the control qubit is left unchanged and unmeasured. Being able to perform this gate with high fidelity is critical to creating a quantum computer.

The extra information in and novel properties of quantum mechanical objects leads to some interesting results. Taking advantage of these, Peter Shor proposed an algorithm which could find the factors of a prime number in polynomial time. This is much faster than the best algorithm known on a classical computer. Quantum computing, then, offers interest not only to quantum physicists and engineers, but to computer scientists as well.

As this motivation is meant to be brief, please see Ref. [1, 2] for additional details.

1.2 Outline of this thesis

In chapter 2, we motivate the use of quantum dots hosted in Si/SiGe heterostructures as a means of realizing qubits for quantum computing research. Specifically we discuss which properties of

semiconductor hosted, quantum dot qubits make for a good qubit system. We then review the Hall effect as observed in a fabricated Hall bar on a Si/SiGe heterostructure as a means of characterizing substrates before fabrication of quantum dot devices. Finally we discuss the fabrication recipe used to create the quantum dot devices similar to those described in chapters 4 and 5 of this thesis.

Next, in chapter 3 we discuss measurement of a quantum dot device in a Triton 400 cryofree dilution refrigerator. The chapter begins with an overview of the Triton and the electrical and thermal considerations taken when installing measurement lines to ensure low noise properties at the sample. It continues by describing in detail the external measurement hardware required to manipulate and readout a qubit device. In addition to wiring schematics and circuit analyses for typical measurement hardware, particular care is taken to highlight the grounding schemes employed in each measurement circuit to minimize electrical pickup.

Chapter 4 contains the details of an experiment exploring transport through an impurity tunnel coupled to a quantum dot hosted in a Si/SiGe heterostructure. [3] By careful measurements of the the stability diagram, gate-voltage controllable tunnel coupling is demonstrated in a coupled quantum dot-impurity system. In addition, analysis of transport measurements as a function of varying device gate voltages allow for triangulation of the localized impurity, yielding a result consistent with an impurity located in the quantum well near the edge of the quantum dot. These results lend credibility to proposed future hybrid donor-quantum dot devices which can take advantage of both the tunability of quantum dots and the long coherence times of donor nuclear spins.

Next, chapter 5 reports the results of quadruple quantum dot device fabricated on a Si/SiGe heterostructure. [4] One of the necessary components of a quantum computer is a controlled two-qubit gate. In this experiment, we demonstrate state-conditional charge qubit oscillations. First, a double quantum dot charge qubit was formed in half of the device and full two-axis control demonstrated. Then, by measuring the detuning shift of one double quantum dot as a function of a changing charge configuration of the adjacent double quantum dot, a capacitive coupling strength of $\approx 75\mu eV$ was extracted. Finally, state-conditional Landau-Zener-Stückelberg oscillations are demonstrated. Due to the strong capacitive coupling, a π phase flip was observed in $\sim$80 ps.

In chapter 6, we discuss the motivation, fabrication, and magnetic characterization of two styles

of micromagnet for spin-qubit applications. First, the fabrication procedure for micromagnets by electron beam (e-beam) lithography is outlined. By including a custom magnetic substrate holder during physical vapor deposition (PVD) in an e-beam evaporator, the cobalt micromagnets are deposited in a static magnetic field which is aligned with the direction of the field to be applied during the experiment. Next, we report the results of vibrating-sample magnetometer (VSM) measurements to characterize bulk cobalt films deposited on witness chips present during micromagnet evaporation. Finally, we show magnetic force microscope images of the stray magnetic fields present in each of the example micromagnets.

Finally, in chapter 7 we discuss some current challenges in Si/SiGe qubit research and outline future research goals towards realizing a universal quantum computer.

Chapter 2

Qubits hosted in Si/SiGe heterostructures

2.1 Motivation

As described in the previous chapter, quantum computation and quantum information offer promising avenues to new discoveries in physics, engineering, and computer science. What then, is the best way to physically realize suitable quantum system for study? One possible approach is to use qubits formed in quantum dots hosted in semiconductor substrates. This is particularly attractive because the years of work already devoted to the classical computing field can be heavily leveraged to help develop a quantum computing analog. Since being proposed at the end of the 20^{th} Century, [5–7] much work has been done towards making good quantum dot qubits for quantum computing (e.g. by improving initialization, readout, and measurement techniques). [8–17] While important, it is unfortunately beyond the scope of a single thesis to cover the entire historical context of previous semiconductor qubit research. This chapter then, will instead only focus primarily on the fabrication and characterization of qubits in silicon-silicon/germanium (Si/SiGe) heterostructures.

Natural, crystalline silicon has a diamond lattice structure which is composed primarily of the stable, 0-spin isotope ^{28}Si ($\sim$92%). The conduction band minimum occurs at nonzero crystal

momentum, about 85% of the way to the Brillouin zone boundary and is six-fold degenerate. Germanium is also a Group IV element with a diamond lattice structure. Germanium, however, has about a 4% larger lattice constant than silicon, preventing no more than a few monolayers to be epitaxially grown before defects occur. The alloy $Si_{1-x}Ge_x$ has a lattice constant which changes roughly linearly from that of Si to that of Ge as x increases from 0 to 1.

In order to grow a heterostructure, we first start with a a silicon handle wafer. Silicon-germanium alloy is then grown, either by MBE or CVD, by systematically increasing the concentration of germanium introduced to the growth chamber. This increases the lattice constant of the alloy by introducing misfit dislocations. When the desired alloy concentration is reached ($\sim Si_{0.7}Ge_{0.3}$), growth continues for many microns to produce a large layer of the desired concentration of alloy. Next, germanium growth is interrupted and a thin ($\sim$ 10nm) silicon quantum well is grown. Finally, germanium is reintroduced and a buffer layer of alloy of a few tens of nanometers is grown at the same concentration as before. Growth completes with a thin sacrificial silicon cap at the top to protect the heterostructure composition at the interface.

When the heterostructure is constructed in this way, the silicon well is under tensile strain due to the increased lattice constants of the alloy layers above and below. This serves to break the 6-fold degeneracy of silicon's conduction band minimum by raising the energy of the 4 lateral valleys in x and y (heavier effective mass) while lowering the energy of the valleys in the z direction. [18] This 2-fold degeneracy is then broken again by the vertical confinement of the electrons within the quantum well owing to a difference in phase of the $+z$ and $-z$ valley wavefunctions. For further details, see Refs. [18–21].

As fabrication of a quantum dot device on a Si/SiGe heterostructure is a long and challenging process, there are many steps which must be completed in succession where the probability that any devices survive to completion is a strong function of the process yield at each step. In addition, a successfully fabricated device is not sufficient to make a qubit. The intrinsic properties of the heterostructure hosting the device play a large role in the expected dynamics of the quantum dot system. This chapter outlines the characterization of Si/SiGe heterostructures via Hall bar measurements as well as the steps necessary to fabricate the working quantum dot devices described

in this thesis.

2.2 Heterostructure characterization — Hall bars

In order to ensure the highest probability of creating a working quantum dot qubit device, it is useful to first characterize the Si/SiGe heterostructure that will host the experiment. This is done by creating a Hall bar on a piece of material nominally identical to the material to be used for the quantum dot device. Hall bars are fabricated by first creating a mesa by defining an etched trench around the region of interest on the heterostructure, then by creating ohmic contacts through ion-implantation and metallization, and finally by growing gate oxide and defining a top gate. Additional details for each of these steps are discussed in the next section.

By cooling the Hall bar below 4K and applying an out-of-plane external magnetic field B while a current flows along the length of the Hall bar, a Hall voltage is generated according to the Hall effect. Using the Hall effect, we can calculate the carrier density n and mobility μ for the electrons in the 2DEG of our heterostructure. As shown in Fig. 2.1, the Hall bar is defined by a length L and a width W. By applying a positive bias to the top gate, a 2DEG is accumulated. When an electric field is applied along the length of the Hall bar E_L, electrons in the 2DEG will flow with an average drift velocity $v_d = \mu E_L$. The voltage measured between two ohmic contacts along the bar is defined as V_L while a voltage measured between two ohmic contacts across the bar (transverse to the applied electric field E_L) is defined as V_H. The current I sourced along the Hall bar can be written as,

$$I = nWv_d e = n\mu E_L eW, \tag{2.1}$$

where e is the fundamental electron charge. From Lorentz's Law, we can relate the v_d to V_H,

$$ev_d B = -eE_H, \tag{2.2}$$

where $V_H = E_H W$. Using our initial definitions and plugging Eq. 2.2 into Eq. 2.1, we solve for n,

$$\begin{aligned} ev_d B &= -eE_H \\ e\mu E_L B &= -eE_H \\ \mu &= -\frac{E_H}{E_L B}, \\ I &= n\mu E_L eW \\ &= -\frac{nE_H E_L eW}{E_L B} \\ n &= -\frac{IB}{V_H e}. \end{aligned} \tag{2.3}$$

Thus, by sourcing a known current through the Hall bar and measuring the Hall voltage V_H as a function of magnetic field B, one can determine the carrier density n of the Hall bar. Once we know n, we can solve for μ by plugging Eq. 2.3 back into Eq. 2.1,

$$\begin{aligned} I = n\mu E_L eW &= \frac{n\mu V_L eW}{L}, \\ \mu &= \frac{IL}{nV_L eW} \\ &= \frac{IL}{V_L eW} \cdot -\frac{V_H e}{IB} \\ \mu &= -\frac{V_H L}{V_L W B}. \end{aligned} \tag{2.4}$$

Therefore, to find the mobility μ we must again know the Hall voltage V_H as a function of magnetic field B, as well as the initial voltage across the Hall bar V_L and the bar's dimensions L and W.

It is important to note that the carrier density and mobility derived from each measurement is a function of the top gate voltage applied to the Hall bar. In order to determine whether or not a heterostructure is suitable for fabricating a quantum dot device, "good" values of mobility and carrier density are chosen: $\mu > 40000\text{cm}^2/(\text{V}\cdot\text{s})$ at $n = 4 \times 10^{11}\text{cm}^{-2}$. While somewhat arbitrary, these numbers are chosen such that the mean free path ℓ_{Tr} of an electron in the 2DEG is much longer than the diameter of a typical quantum dot, [21]

$$\ell_{Tr} = \frac{\mu\hbar}{e}\sqrt{2\pi n} \gg 40nm. \tag{2.5}$$

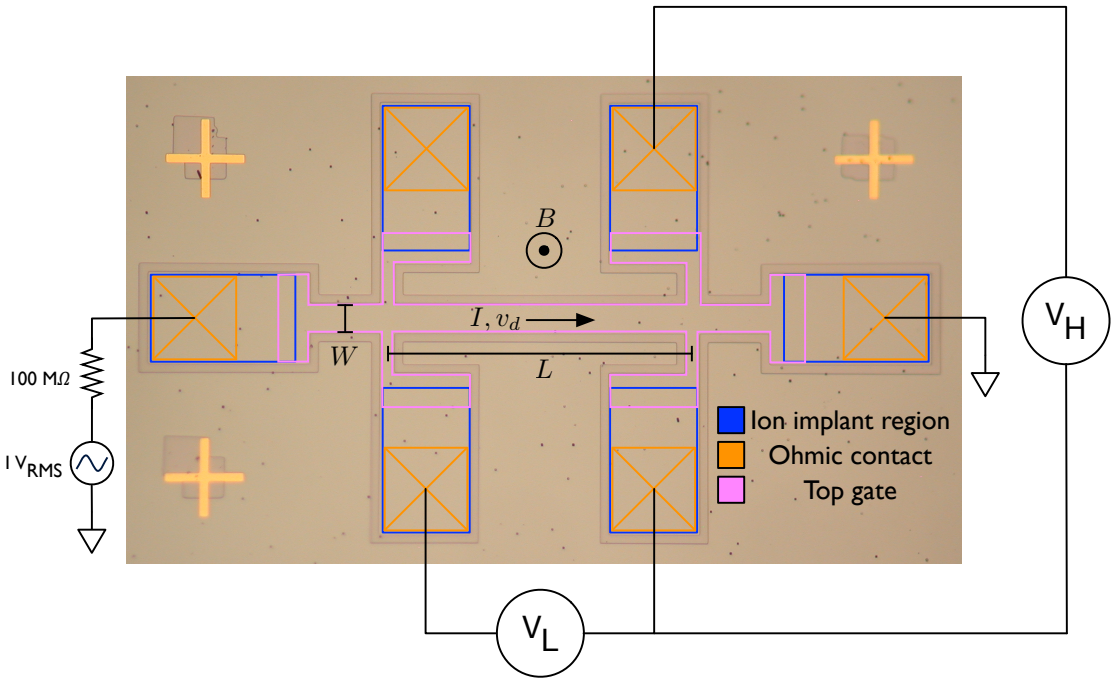

Figure 2.1: Schematic cartoon of a Hall bar. An optical image of the mesa trench for a Hall bar device on a Si/SiGe heterostructure. Superimposed on the image are the ion implantation regions, ohmic contacts, and top gate for a completed Hall bar.

2.3 Fabricating a quantum dot device

This chapter will outline in detail the fabrication procedure employed in creating the device in Chapter 4. [3] Though not identical in ordering, similar techniques to those in this section were also used to fabricate the device in Chapter 5. [4] For a more general review of fabrication considerations for devices on silicon heterostructures, see Ref. [22].

Four quantum dot devices can be fabricated on one 5mm×5mm chip of Si/SiGe heterostructure. Multiple chips are chosen from the Hall bar assessed material and processed in parallel to increase the resulting yield. Fabrication begins with the definition of etched alignment marks to identify each of the device quadrants on a chip. S1813 positive photoresist (Shipley Microposit S1800 Series) is spun onto each chip at 4000 RPM for 30 seconds and then soft baked at 90°C for 3 minutes. The samples are then exposed for two minutes on an MJB contact aligner through a quartz mask with the alignment mark pattern. Post-exposure, the chips are developed and rinsed for 60 seconds each in MF321 and dionized (DI) water before a hard bake is performend at 120°C for 3 minutes.

Finally, the samples are etched in a reactive ion etcher (RIE) with a 25W plasma of 25 sccm SF_6 and 1.8 sccm O_2 at 16mT for 4 minutes to define the alignment marks in the substrate. Before proceeding to the next step, the remaining photoresist is removed by soaking the chips in acetone for >1 hour followed by sonication, an isopropanol (IPA) rinse, and drying via compressed nitrogen (N_2). For the rest of this section, it is assumed these cleaning steps are performed after each step before proceeding. If additional cleaning is performed, it will be noted explicitly.

Next, the samples are prepared for ion-implantation to define the ohmic contact regions for the quantum dot devices. In the case of the device in Ref. [3], this step was performed a second time to directly implant donors near the regions where the quantum dots were expected to form. The ion-implantation regions are defined via a mask of patterned e-beam resist. A quad-layer of resist consisting of 3 layers of PMMA 495 A4, and one layer of PMMA 950 A2 (Microchem) is spun onto the chips. Each layer is applied by spinning the resist at 3500 RPM followed by a 90 second bake at 180°C. E-beam lithography is then performed using a converted LEO 1550 VP scanning electron microscope (SEM) using the Nanometer Pattern Generation System (NPGS). [23] By drawing the desired pattern for our ion-implantation regions along with our defined alignment marks in a drafting program such as AutoCAD and inputting them into the software, we can use NPGS to control the electron beam at the SEM. Then, by aligning to our etched marks and exposing our resist with a calibrated clearing dose ($550\mu C/cm^2$) in the implant region, we can later develop the resist away to define our mask. Post-exposure, samples are developed in a 3:1 IPA:MIBK solution (Microchem) for 60 seconds before being rinsed in IPA for 5 seconds and dried with N_2.

Samples are then mounted to a 3-inch silicon wafer via carbon tape and shipped out for commercial ion-implantation (Cutting Edge Ions LLC). There, the samples are implanted with $^{31}P^+$ phosphorus accelerated to 20keV towards the wafer at a 7° tilt relative to the wafer normal to avoid ion channeling. The delivered dose was 5×10^{15} ions/cm^2 and the wafer was not heated (i.e., implantation was performed at room temperature). The implantation dose is chosen such that the ohmic contact region will be doped with phosphorus at a concentration above the metal-insulator transition as determined by a Monte-Carlo simulator for the Stopping and Range of Ions in Matter (SRIM). [24, 25] By inputting the approximate thicknesses and densities of the layers of the

heterostructure, SRIM can simulate the expected ranges of the implanted ions. A simulation for a heterostructure with a 10nm silicon well and a 35nm SiGe buffer is shown in Fig. 2.2 for 20keV implanted $^{31}P^{+}$ phosphorus. The implanted dose is chosen such that the density of delivered phosphorus is $> 1 \times 10^{20}$ ions/cm^3 from the surface of the heterostructure all the way down through the quantum well. When the samples are returned, they are removed from the Si wafer and soaked over night in acetone before being cleaned in the normal way. If additional residue remains after the solvent soak, samples are cleaned further with an oxygen plasma in the RIE with a 50W plasma of 20 sccm O_2 at 20mT for 30 seconds. Chips are inspected and the process repeated if resist residue is still present. Finally, the samples are placed in a rapid thermal annealer (RTA). There, a bright light source heats the samples to 700°C in a forming gas atmosphere (5% H_2 in N_2) to activate the implanted ions. Activation entails providing the energy necessary to incorporate the implanted ions in the crystal lattice as well as repair the damage to the lattice due to the implantation.

After ion-implantation, ∼10nm of gate oxide (aluminum oxide, Al_2O_3) is deposited via atomic layer deposition (ALD). [26] First, the samples are prepared by removing the native silicon oxide that has grown through exposure of the to Si surface to air via a 15 second dip in 20:1 buffered oxide etchant (BOE or HF) followed by a DI water rinse. The samples are then placed immediately into the ALD tool (manufactured by Cambridge Nanotech) and pumped down to a few Torr in an atmosphere of N_2. The oxide is then grown at 150°C via ALD: a small volume of water is introduced to the heated reactor vessel and is allowed to adsorb to the surface of each chip before the excess is pumped out. Next a pyrophoric precursor, trimethylaluminum (TMA) is introduced in the same way as the water. The TMA interacts with the water in a self-limiting reaction leaving one monolayer of ALD grown alumina. By repeating this cycle of precursor applications, our gate oxide is grown one layer at a time until the desired thickness is reached.

Next, a mesa is defined for each quantum dot device. The mesa serves to disconnect the quantum well in the device region from the quantum well under the device control lines and bond pads in order to reduce cross-talk. This is done by etching a large trench around the device or "active" regions of the chips. The mesa etch is achieved by using an e-beam resist mask with the RIE. Using the same procedure as the ion-implantation step, the mesa trenches are defined at the

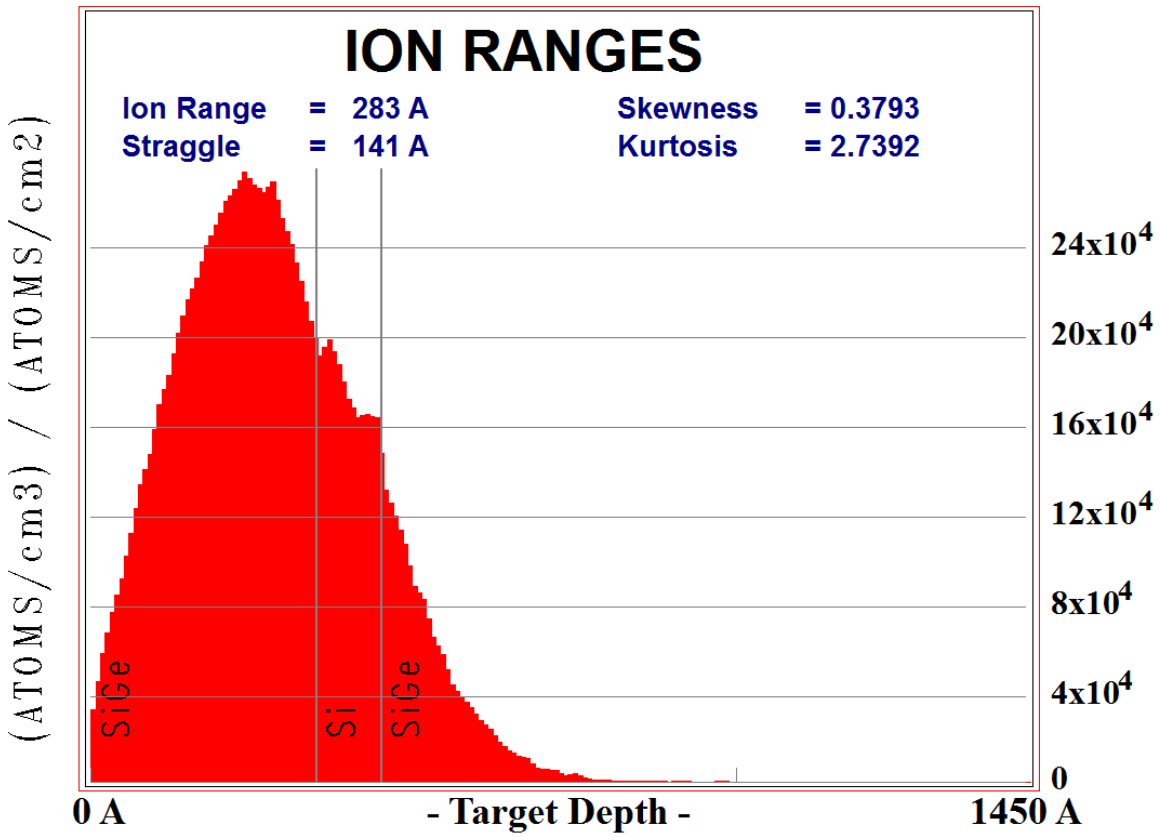

Figure 2.2: SRIM simulation for a phosphorus-implanted Si/SiGe heterostructure. SRIM simulation for 20keV phosphorus implanted on a 35nm deep, 10nm quantum well heterostructure at a 7° tilt. [25] Multiplying by a delivered dose of 5×10^{15} ions/cm^2 yields an expected continuous region of phosphorus with a density $> 1 \times 10^{20}$ ions/cm^3 from the surface through the quantum well.

SEM on a quad-layer of e-beam resist. After development, the height of the resist is measured using an atomic force microscope (AFM). Then, the samples are each dipped in a 20:1 BOE solution for 60 seconds and then rinsed in DI water to remove the underlying ALD gate oxide. Samples are next loaded quickly into the RIE and the tool is immediately pumped out to prevent oxide regrowth. In the RIE, the samples are etched with the same SF_6 recipe previously described for ~2 minutes. Then the samples are again measured in the AFM. By subtracting the pre-etch resist height from the post-etch total height, an approximate mesa etch depth can be determined. The etch must be deep enough to go through the well but not be so deep that two metal evaporations are required

to span the trench (< 200nm). If the etch must be repeated, an additional 15 second 20:1 BOE dip must be performed first to ensure no oxide is present before the etch. When the desired depth is achieved, the samples are placed in acetone and cleaned as described earlier in this section.

Following the creation of the mesa, the ohmic contacts and fine alignment marks are next defined. In this step, we seek to create a metal layer over a portion of our ion-implanted region to allow electrical access to the 2DEG. For efficiency, in this step we also define a smaller set of metal alignment markers that will later aid us in writing our device gates. First, the ohmic metallization region and fine alignment marks are defined via e-beam lithography on a quad-layer of resist using the SEM. After development, the samples are dipped in 20:1 BOE for 60 seconds and then rinsed in DI water to remove the underlying ALD gate oxide. The samples are then quickly placed into the PVD75 metal evaporator (Kurt J. Lesker) and immediately pumped down to prevent oxide regrowth. This is critical as any oxide that grows before metal deposition will prevent electrical contact to the substrate. Once base pressure is reached ($< 2 \times 10^{-6}$Torr), ~ 5nm of titanium (for adhesion) and ~ 40nm of gold (for its noble properties, notably no oxide growth in ambient conditions) are deposited onto the samples via e-beam evaporation. After the deposition is complete, samples are placed in acetone to remove the e-beam resist and lift-off the excess metal, leaving the ohmic contacts and alignment marks as desired.

Now we define the first layer of our quantum dot device. This is performed in two e-beam lithography steps. First, the initial layer of fine device gates are written on a bi-layer of e-beam resist. A bi-layer consists of one layer of PMMA 495 A2 and one layer of PMMA 950 A2 applied with the same recipe for each layer as the quad-layer stack. After development, the samples are descumed in a 10W O_2 plasma asher for 7 seconds to remove any remaining resist residue before being placed in the metal evaporator. Following evaporation of ~ 2nm of Ti and ~ 20nm of Au, liftoff is performed as before avoiding sonication if possible as there are now nanometer-sized gates on the substrates. The process is then repeated, this time for the bond pads and leads which connect to the fine device gates. The patterns are defined in a quad-layer of e-beam resist and developed, descummed, and placed in the evaporator as before. This time, ~ 20nm of Ti and $100 - 200$nm of Au are deposited and lifted off, depending on the depth of the mesa etch.

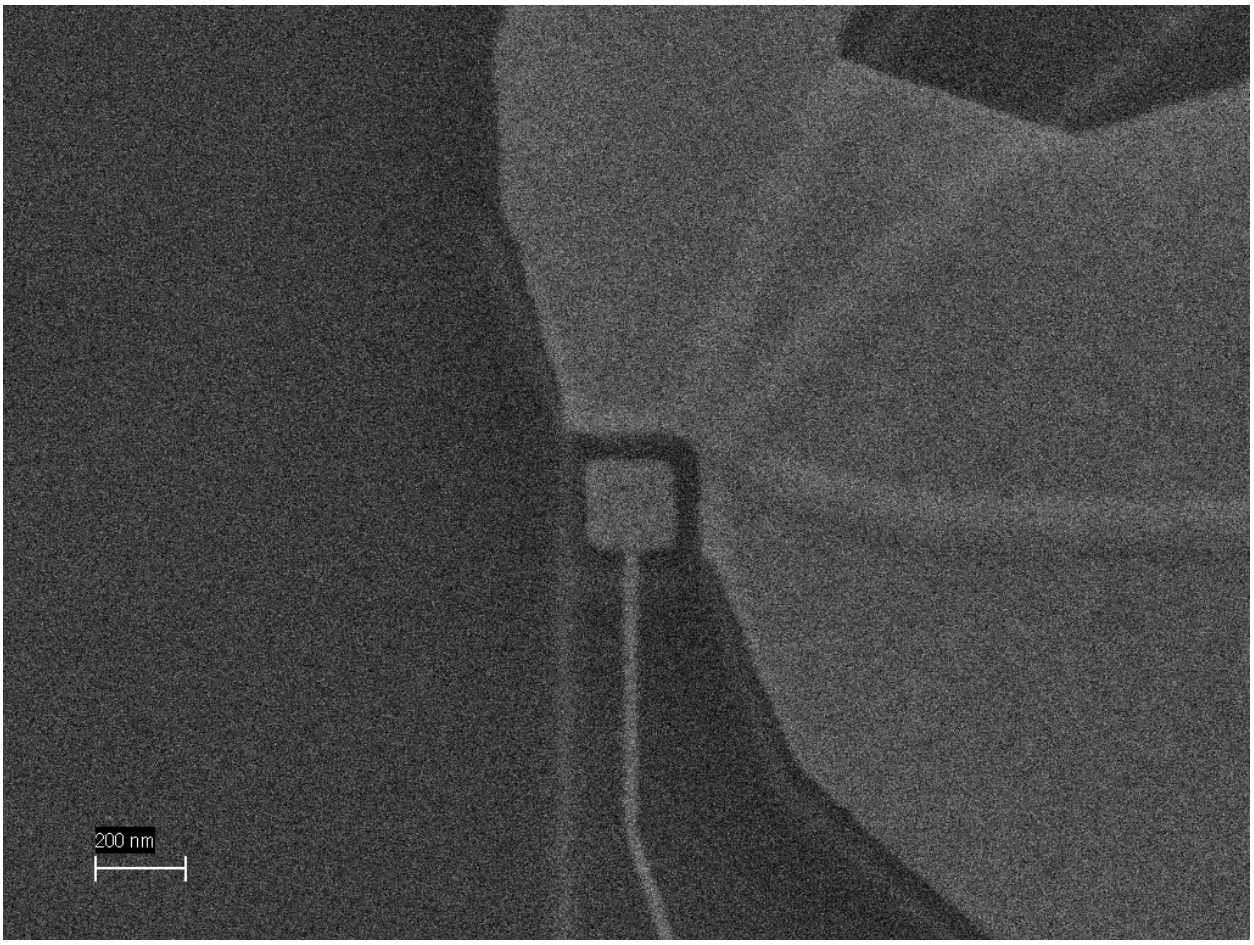

Figure 2.3: SEM-micrograph of the completed active region of a quantum dot device. This device is nominally identical to the one discussed in Ref. [3].

Before creating the second layer of our device, we must first electrically isolate it from the first. This is done by depositing a second layer of ALD grown aluminum oxide. Following the same procedure as before, but with no pre-growth BOE dip, 80nm of aluminum oxide is grown on each sample. Then the second layer of device gates are created using the same procedure as the first. An SEM-micrograph of the completed active region of a device nominally identical to the one discussed in Ref. [3] can be seen in Fig. 2.3.

Devices are completed by removing the 80nm of grown oxide from over the first layer bond pads to allow access when wirebonding. This is done first defining an etch mask via photolithography as previously described. After hard baking the mask, each sample is dipped twice in 15:1 BOE

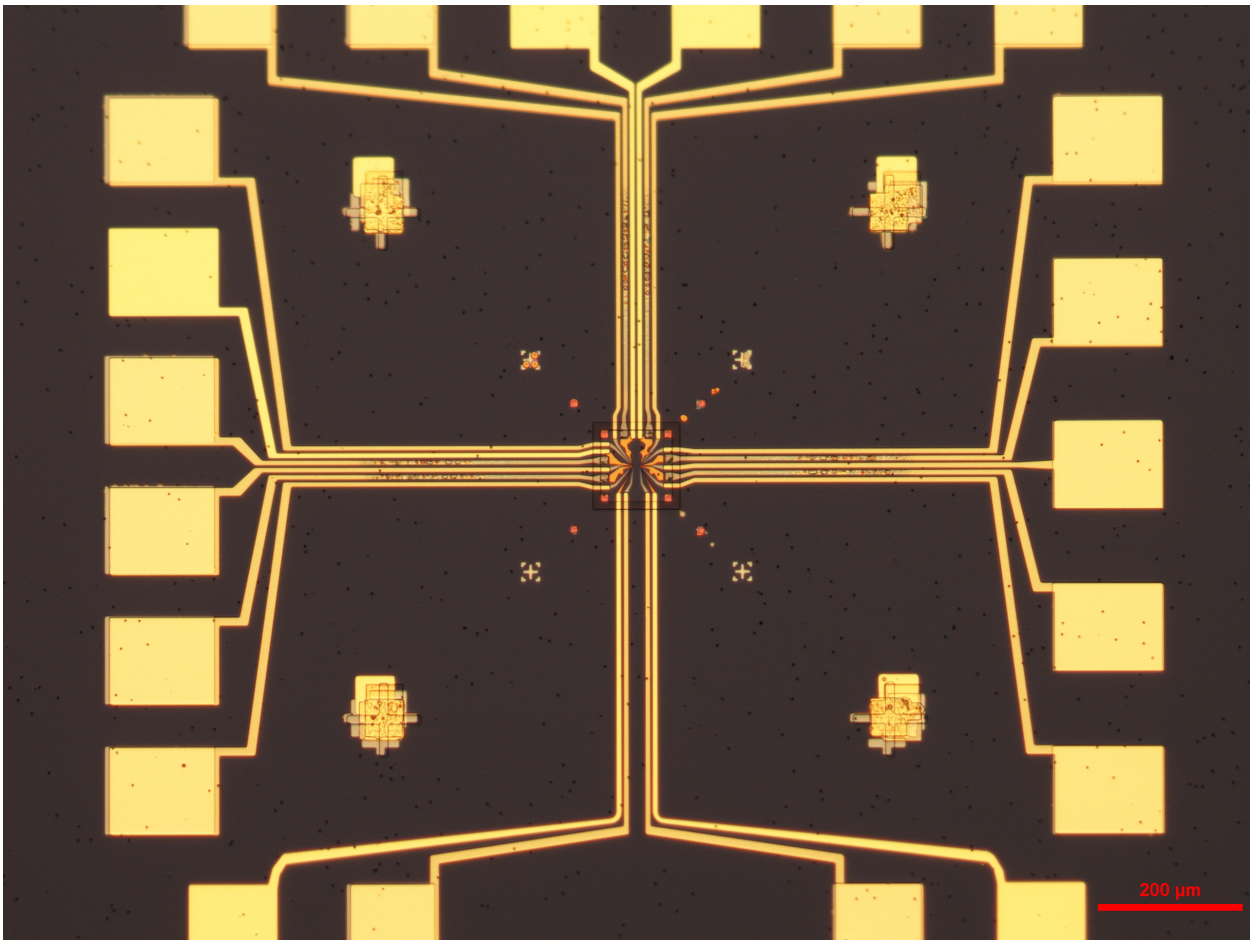

Figure 2.4: Optical photograph of a completed quantum dot device. This device is nominally identical to the one discussed in Ref. [3].

for 150 seconds each to remove all the oxide. After the wet etch and a final thorough clean, the samples are complete! An example of a completed device nominally identical to the one discussed in Ref. [3] can be seen in Fig. 2.4. The bond pads surround the device which is located in the center and too small to be visible at this magnification. The purple background hue is due to thin-film optical interference effects in the device oxide.

Chapter 3

Measuring quantum dot devices with the Triton 400 cryofree dilution refrigerator

3.1 Motivation

As will be shown in the next chapters, the energy scales relevant to quantum dot qubits are on the order of a few μeV to tens of meV. It is therefore necessary to cool samples to just above absolute zero in order to avoid thermal broadening ($100mK = 8.62\mu eV$). In addition, decoherence rates due to electron-phonon coupling are reduced as the temperature of the crystal lattice approaches zero. [27–29]

In order to achieve these low temperatures, qubit experiments are typically performed inside of a dilution refrigerator. Loading a device and cooling it is not sufficient however; DC and RF control lines are also required to enable device tuning and qubit manipulation. Great care must be taken installing these control lines as they must necessarily extend from the sample at a few tens of millikelvin all the way out of the fridge to measurement hardware at room temperature ($\sim$300K). Limiting the heat load and electrical noise introduced by the control wiring is critical for good qubit performance.

This chapter provides an overview of how a typical qubit experiment is realized in a Triton 400 cryofree dilution refrigerator. First, the layout of the Triton fridge itself is described. Next, we examine the control wiring within the Triton, paying particular attention to electrical and thermal noise reducing considerations. Finally, we discuss the external hardware required to control and manipulate a quantum dot device.

3.2 Fridge and internal wiring overview

Triton 400 summary

The Triton 400 cryofree dilution refrigerator is a commercial product sold by Oxford Instruments that is capable of achieving a base temperature of 10mK by circulating a mixture of ^{3}He/^{4}He gas. It does so without the use of liquid cryogens via a pulse-tube cooler. In order to reach such cold base temperatures, the fridge has various temperature stages and radiation shielding in the form of metallic cans. This is depicted schematically in Fig. 3.1.

On the outside of the fridge is the outer vacuum chamber (OVC). Everything within the OVC is much colder than room temperature and therefore under vacuum ($< 1 \times 10^{-4}$ mbar) to prevent minimized thermal conduction between plates. The next stage is the PT1 which is typically around 45 K. The PT1 plate is thermally isolated from the OVC via G-10 support rods which have poor thermal transport properties. Cooling of the PT1 plate is provided by the first stage of the pulse-tube cooler. In order to ensure that the PT1 stage (and all subsequent stages) has a constant temperature everywhere on the plate, oxygen-free, high thermal conductivity (OFHC) copper is used to construct the plate. The plate is also electroplated with gold to prevent corrosion.

The next stage is the PT2. The PT2 hangs from the PT1 plate and is connected again via G-10 support rods. Cooled by the second stage of the pulse-tube cooler, the PT2 plate is typically around 3 K during normal operation. In addition, the PT2 plate is thermally linked to the 5 T superconducting magnet installed in the Triton via an OFHC copper can. As pulse-tube cooler has a lot of cooling power, the PT2 and it's can are the main source of cooling when bringing the fridge down initially from room temperature.

After the PT2 comes the still. Typically around 750 mK, the still is the portion of the fridge where ^{3}He is preferentially pumped from the dilute mixture to continue to drive cooling in the mixing chamber. The still is hung from the PT2 plate by stainless steel support rods which have poor thermal transport properties.

From the still hangs the intermediate anchoring plate (IAP). The IAP has no active cooling power and serves mostly to structurally support the heat exchangers in the dilution circuit between the still and the mixing chamber. It also provides radiation shielding between the still and the mixing chamber plates. The IAP is typically around 100 mK during normal operation.

The final stage of the fridge is the mixing chamber. Here the mixture is present as a liquid which is separated into a ^{3}He rich and a ^{3}He poor phase in equilibrium. By pumping on the ^{3}He poor phase, ^{3}He from the rich phase is forced across the phase boundary in an endothermic process. This allows us to cool the final stage of the fridge to a base temperature of around 10 mK.

Internal wiring summary

To provide DC biases to device gates, 6 ribbons of constantan loom are installed in the Triton. Each ribbon features 12 twisted pairs of constantan wire woven in a special yarn, yielding a total of 72 DC bias lines. A ribbon of loom is represented by a single twisted pair of wires (red and black) in Fig. 3.1. Each ribbon of loom is soldered to a 24-way Fisher connector at the top of the fridge to allow for electrical access. Constantan is chosen as the wire material due to it's low thermal conductivity (15-20 times lower than copper). This limits the heat transferred between stages via the DC lines. The loom is thermalized on each stage of the fridge by clamping it between two heat-sunk, gold-plated, copper plates. The last stage which thermalizes in this way is the IAP. At the mixing chamber, each ribbon of loom is terminated as a 25-way micro-D connector. These micro-D's are connected next to a series of cold filter boards (1 per ribbon). The cold filter boards contain a 2-stage low-pass filter on each DC line to reduce electrical noise (R= 1kΩ, C = 330pF). After the filter board, the signals are passed into a copper powder box. The copper powder boxes contain a PCB which meanders each wire from a ribbon of loom over a large portion of the board, thereby increasing their surface area. The PCB is then embedded in copper powder particles and

enclosed in gold-plated copper box heat-sunk to the mixing chamber. The copper powder reduces any excess high-frequency ($\gtrapprox$ 100MHz with >50dB of attenuation at 1GHz [30]) noise due to significant skin-effect damping and the large available surface area that many small copper grains present. [30–32] It also serves to thermally sync the loom to the mixing chamber. The signals are finally carried down to the sample puck via three pairs of 25-way micro-D to 51-way nano-D wiring harnesses. The harnesses are each surrounded by a metal shroud which acts as a Faraday cage to maintain the filtering provided by the copper powder box.

In order to minimize electrical noise coupled into the system, very close attention is paid to our grounding scheme such that there is only one electrical ground that the whole measurement circuit is referenced from. This type of grounding scheme is called star ground; so called because there are many grounded lines, but each can be represented as a straight line extending from a single point without coming back or touching any other lines. Grounding the circuit in this way significantly reduces the number of ground loops present in the system. Ground loops are particularly damaging to qubit experiments due to the unwanted current flow they induce the measurement circuit. This arises in two ways. In the first case, two (or more) nominally identical ground points are referenced to multiple parts of the circuit. If there is any potential difference between these two ground points, no matter how small, a current will flow. In the second case, we consider two grounded lines which extend from the star ground and then later reconnect. This creates a closed loop of nominally grounded wire. From Faraday's law of induction, any changing magnetic flux through the area of the loop will induce a voltage, causing current to flow. Numerous sources of magnetic fields exist in every experimental lab, (including the experimenter themself!) so minimizing ground loops is paramount.

Star ground (or cold ground) is defined in our system at the cold filter boards. On each filter board, every low line that enters the board is tied to every other low line on that ribbon of loom via a ground plane on the PCB. Near the mounting screw holes on the PCB, the solder mask is removed so that the ground plane can be electrically connected to the copper mounting bracket attached to the mixing chamber. As all the filter boards are connected to the same mounting bracket, this defines the mixing chamber as the star ground. The Earth ground reference for the

star ground is provided by the measurement rack, and will be described later in this chapter.

DC signals are carried out of the fridge to the measurement rack by connecting a Fisher to D-shell (FTD) cable to the 24-way Fisher connector at the top of the fridge. Each twisted pair within a ribbon of loom is mapped to a twisted pair of copper wires within the FTD cable. A common shield surrounds all of the twisted copper pairs within the wire and is electrically connected to the body of the Triton on one end and to the body of the D-shell connector at the other end. It is important that this shield reference be carried to the measurement rack so that we continue to minimize electrical pick-up noise in our system.

To provide RF signals to a device, 8 semi-rigid, coaxial cables are installed in the Triton. The inner conductor of the coax is silver plated beryllium-copper, the dielectric is made from PTFE, and the outer conductor is cupronickel. These materials offer good RF-properties while being poor thermal conductors. The coax are divided into two groups of four and specified for "fast" ($>$ 18GHz) and "slow" ($<$ 18GHz) frequencies. As shown in Fig. 3.1, "fast" lines are light grey while the "slow" lines are dark. Frequency limitations for each set of coax are determined by the connector type at the top of the fridge. A 2.92 mm connector is used for the "fast" lines, while the "slow" lines use SMA instead. Cooling of the coax is achieved by thermally sinking the lines to each stage of the fridge. This is achieved in two ways: by connecting the lines to a connector feed through installed in each stage and by using attenuators. The first method ensures that the outer conductors of each coax are well sunk and electrically connected to the cold ground. This does little to cool the inner conductor however due to the thermal isolation provided by the PTFE dielectric. This is solved by our second cooling method. Both the inner and outer conductor of the attenuator are thermally connected to the body, proving cooling for both conductors of the coax. A total of 39dB of attenuation is provided on each line: -20dB on the PT1 plate, -10dB on the PT2 plate, -6dB on the still, and -3dB on the mixing chamber. Below the mixing chamber, the coax material is changed to copper for it's good thermal properties. After the last attenuator, some lines go straight to the PCB and some go to bias-tees. Bias tees allow for a DC bias to be applied to the RF signal before being connected to the sample PCB. The "slow" bias tees are only rated for $<$ 18GHz and require a 10kΩ resistor to be added in series to the DC input to provide

an impedance mismatch to prevent RF leakage up the DC control line. The DC signals are taken from a modified copper powder box which has pin headers in addition to a micro-D at it's output. For a given twisted pair, the high and low signal are taken from their respective pin-headers on the copper powder box PCB and routed to a bias tee via twisted copper wires. At the bias tee, the high signal line is soldered to the DC input while the low is bent back and not connected to anything. This prevents a ground loop while minimizing pickup in the DC line. After the bias tee, each line of coax terminates on the sample puck at an SMP connector.

Testing fridge wiring

DC Wiring Tests -

Using a Keithley2400 sourcemeter, perform all of the following measurements (in any order) to test all DC connections from the breakout boxes (BOBs) to their corresponding traces on a populated PCB without a sample. Record the results in the Triton notebook. *This is required every time the fridge is opened before cooling down again.* If the fridge is already cold, perform continuity (do the highs go to the correct pads on the PCB and do they all have similar measured resistance) and isolation (each line isolated from each other line (as appropriate) by $\geq$ 10 GΩ) checks for each signal line on your PCB before mounting your sample and loading the experiment:

1. **BOB High to PCB High continuity (Ω):** Check the continuity of a high signal from its input on BOB down to its corresponding trace on the PCB by measuring the resistance. All other BOB inputs should be shorted to ground. Expected resistance should be around 2.1 kΩ for all lines except those for the LED and bias-tees (*update when we measure*).

2. **BOB Low to Fridge continuity (Ω):** Check the continuity of a low signal from its input on the BOB to the body of the fridge. None of the other BOB inputs should be shorted.

3. **PCB High to fridge grounding (Ω):** Check the grounding of a high signal trace on the PCB by shorting its switch on the BOB and measuring the resistance from its trace to the fridge body with its BOB input shorted. None of the other BOB inputs should be shorted.

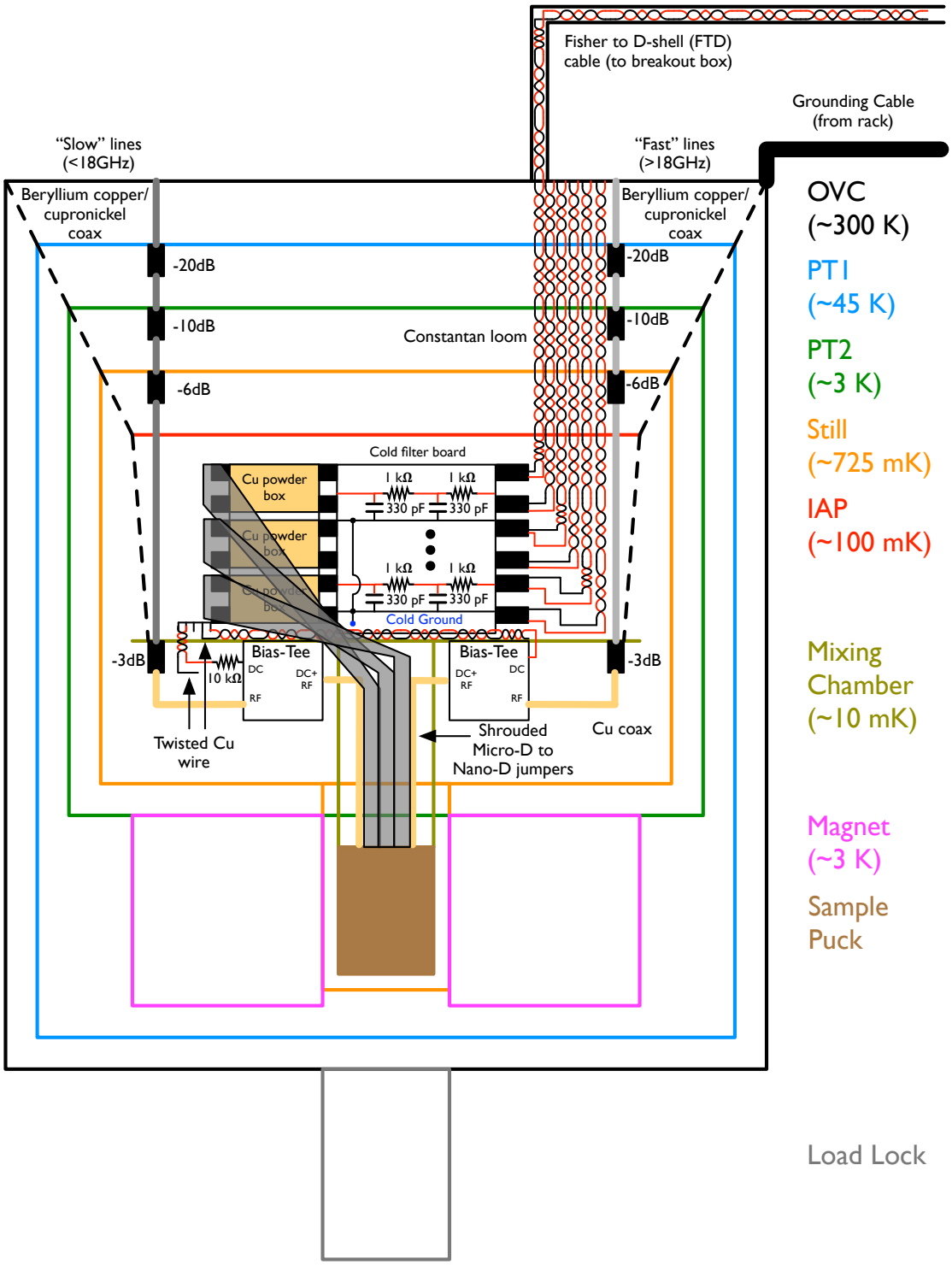

Figure 3.1: Triton wiring schematic.

4. **BOB High to fridge isolation (pA):** Check the isolation of a high signal from the fridge by applying a 10 V bias between the high signal on a BOB and the fridge body while measuring the current. All other BOB inputs should be shorted to ground. Isolation should be better than 10 GΩ ($\leq$ 1 nA of measured leakage). Expect the measured current to exhibit a nonzero decay time due to the RC time of the line.

5. **PCB High to fridge isolation (pA):** Check the isolation of a PCB high signal from the fridge by applying a 10 V bias between its trace and the fridge body while measuring the current. Measurement should be performed twice, once with all other BOB inputs shorted to ground and again with none of the other inputs shorted. Isolation should be better than 10 GΩ in both cases ($\leq$ 1 nA of measured leakage).

RF Tests -

Using a VNA or similar instrument, characterize the S_{21} transmission spectrum for each coax line in the fridge from the top to the bottom. When working with the VNA, be sure to use a grounding strap to avoid shocking and damaging the inputs. It's also best to use a torque wrench whenever possible to avoid overtightening any of your connections.

3.3 External wiring overview

Maintaining our wiring scheme to avoid ground loops outside of the fridge is of paramount importance and as such, careful thought must be applied when designing and adding electronics and measurement hardware to an experiment. This section outlines many of the external wiring setups common to the experiments discussed in this thesis, highlighting in particular the ground and shield configurations so as to avoid coupling excess noise into device measurements. When future experiments require new measurement strategies and hardware, the techniques employed in this section should be heavily considered and can be applied generally to other dilution refrigerators.

The measurement rack: experiment ground and hardware mounting considerations

As discussed in the internal wiring overview, a star ground strategy is employed in Triton measurement set-up to avoid forming ground loops. One of the "arms" of the star must be tied to an external ground to provide a reference for the entire system. External ground therefore is provided by the ground pin of the $120VAC$ building power supply connected to an uninterruptible power supply (UPS) mounted in the measurement rack as shown at the bottom of Fig. 3.2. Continuing from the UPS, a wire is then tied from an external ground reference pin on the back of UPS to the body of the measurement rack. From there, ground is connected to the top plate of the Triton fridge via a thick, braided copper cable attached to the rack. Finally, the ground reference is connected to the cold ground point on the mixing chamber via the stainless steel support rods connecting each plate inside the fridge.

Now we consider mounting hardware into the rack. There are two general types of hardware used on the Triton: homemade and commercial. Commercial hardware (such as the SIM928 voltage supplies manufactured by Stanford Research Systems) is mounted into the rack in the normal way with 10-32 screws or by sitting on a shelf. The equipment is powered via a power strip connected to the UPS. Homemade hardware requires a little bit more care. In many cases, the metal box which contains the homemade hardware serves as an electrical shield for the circuit. As such, it cannot be electrically connected to the rack or any other homemade box or a ground loop will form. To prevent this, homemade hardware where the boxes carry the shield are isolated from the measurement rack via nylon spacers and screws and from each other via Kapton tape.

Figure 3.2 shows a typical example of a populated measurement rack. Additional details for the homemade hardware are discussed below. If a second rack is required, an additional wire should be tied to the new rack from the old so that the new rack is grounded. Any equipment which requires power in the new rack should draw it from the UPS in the old rack.

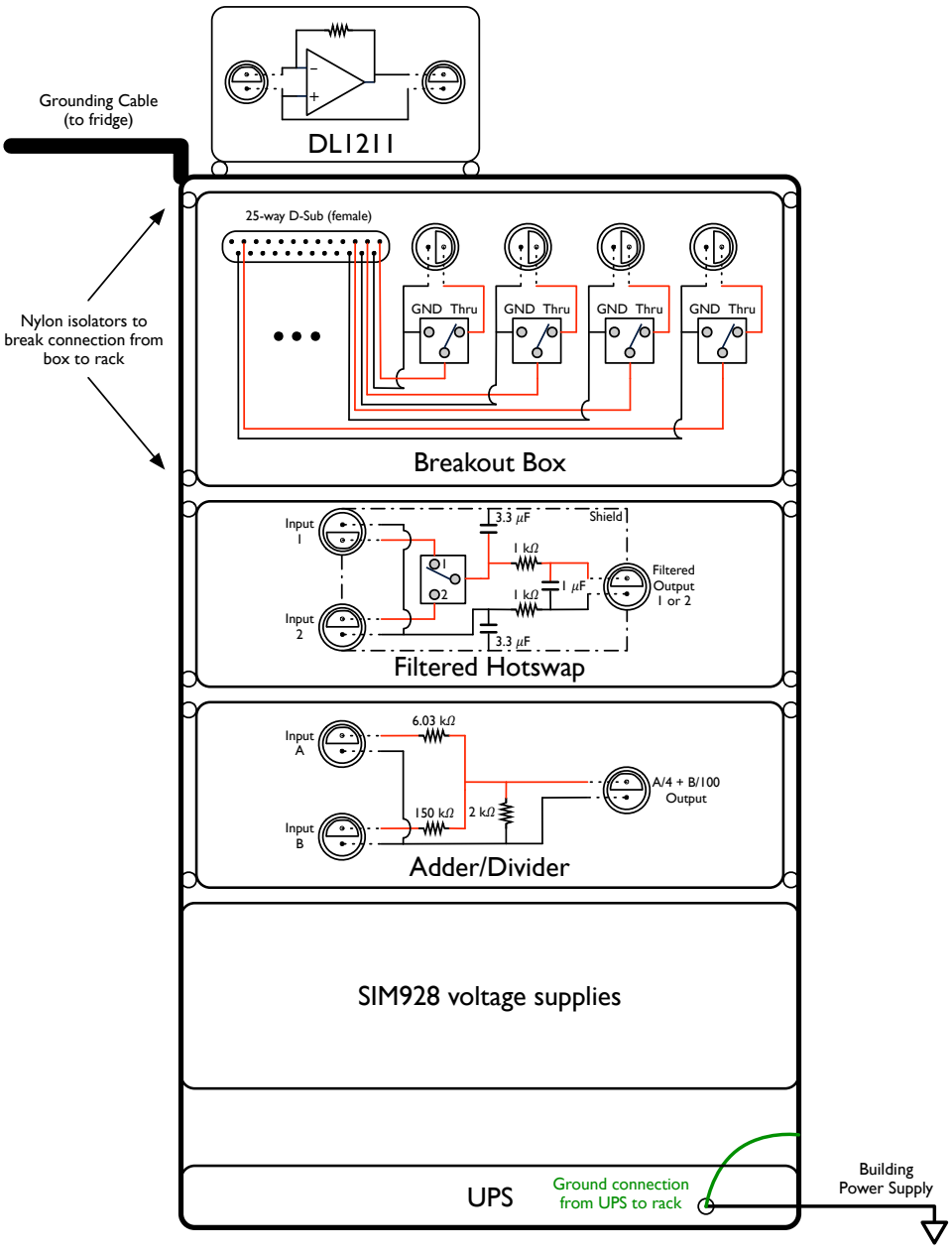

Figure 3.2: Schematic of a typical measurement rack.

Breakout box

Though connected to the measurement rack, the breakout box (BOB) is best thought of as a $300K$ DC access panel to the Triton OVC with the FTD cable acting as an electrical extension of the loom and OVC. The breakout box serves to "break out" each of the 12 twisted pairs within a ribbon of loom to 12 twin-BNC jacks for electrical access. As shown in Fig. 3.2, the high and low signal lines of each twisted pair are taken from adjacent pins on the 25-way D-shell and soldered to twin-BNC jacks through a one-pole, ten-position, make-before-break switch. The switch is limited to two positions as shown in the figure: GND - the high signal line connection to the twin-BNC jack is broken and tied to the low signal line inside the breakout box, thereby grounding the gate connected to that line, and Thru - the high and low inputs of the twin-BNC jack are connected through to the experiment. On the actual breakout boxes, the switch is in the GND position when it is pointing away from the twin-BNC jack while Thru will have the switch pointing directly at its jack.

Each breakout box is isolated from the measurement rack via nylon spacers and screws. The metal of the breakout box as well as the shields of the twin-BNC jacks are tied to the shield of the fridge via an alligator clip from a screw on the corner of the breakout box which is attached to the shell of the D-shell connector on the FTD cable. This prevents a ground loop from forming between the measurement rack and the breakout box while maintaining a shield around each twisted pair to as it "extends" further up the measurement chain away from the breakout box via twin-BNC cables.

Filtered hotswap and V/4 voltage division for biasing device gates

Defining and manipulating a quantum dot requires precise control of the biases applied to the electrostatic gates defined on the interface of the heterostructure. For experiments on the Triton, a SIM928 voltage supply (manufactured by Stanford Research Systems) is the primary means of providing a DC bias to device gates. Typical ratios of the change in the chemical potential of a dot to the change in a particular gate's voltage, or the lever arm α, are of the order of $\sim 100\mu eV/mV$. The voltage resolution of a SIM928 voltage supply however is only $\pm$1mV ($\pm$20V range), therefore

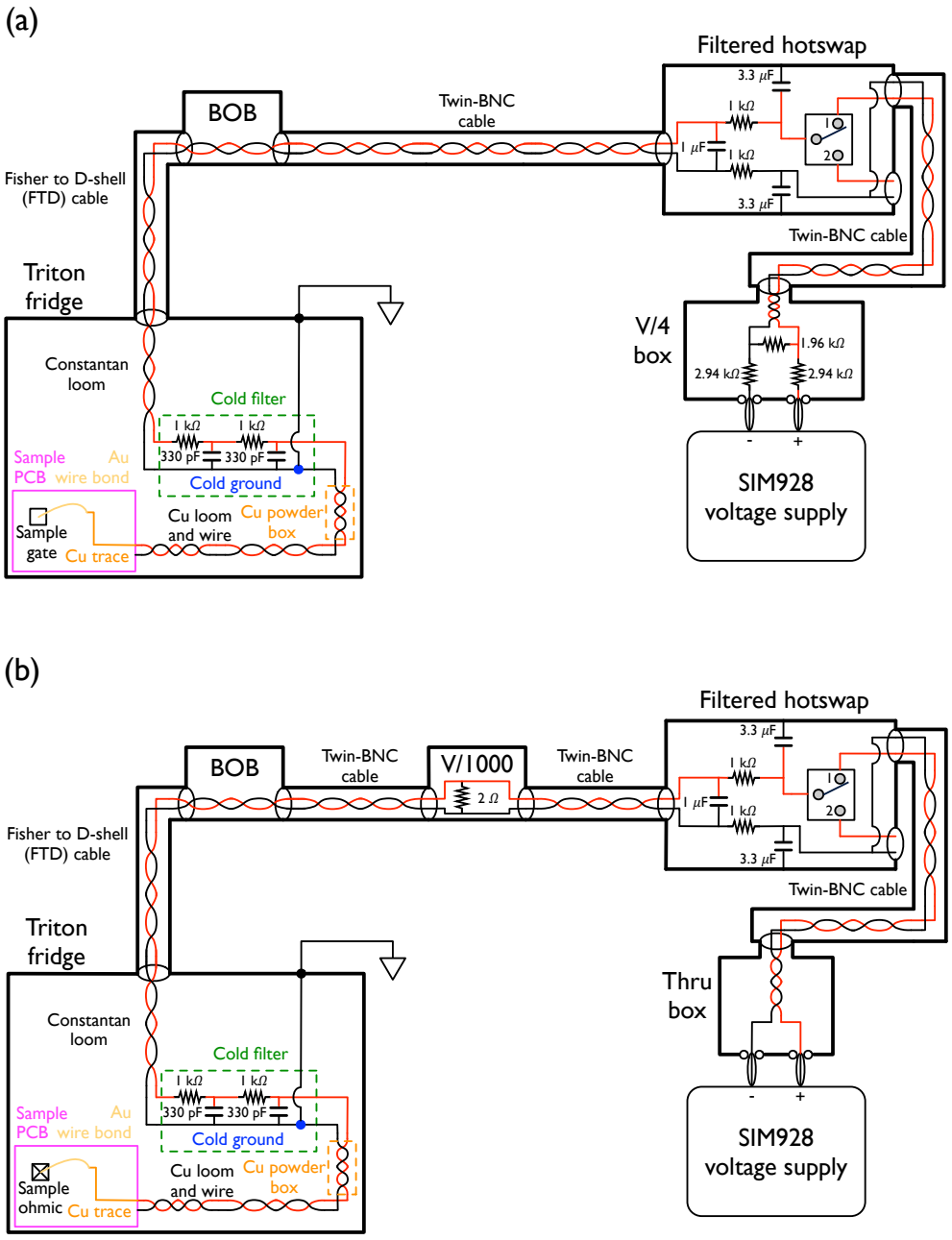

Figure 3.3: Measurement schematic for a V/4 box and a V/1000 box. **(a)** Measurement schematic for applying a V/4 divided voltage to a device gate. **(b)** Measurement schematic for applying a V/1000 divided voltage to a device ohmic.

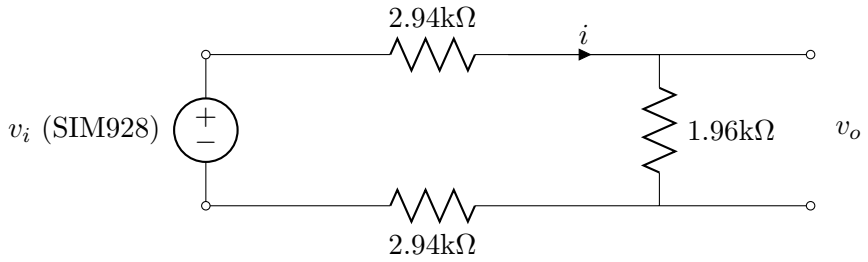

Figure 3.4: V/4 circuit analysis. A simplified version of the V/4 box circuit from Fig. 3.3(a) to analyze the output voltage of the circuit.

further voltage division is required. This is achieved by the use of a V/4 box. Besides applying a precise voltage, it is also critical that the noise on the applied voltage be low. This is achieved in part by a filtered hotswap. By adding a low-pass filter to the circuit, voltage noise on a gate's bias line is reduced.

As shown in Fig. 3.3(a), a filtered hotswap box is added between the breakout box and the V/4 box. The thick black lines represent electrical shield, thin black lines are signal low, and thin red lines are signal high. In a typical V/4 measurement set up, the shield extends from the body of the fridge via the FTD cable to the body of a breakout box in the measurement rack. From there, electrical shield is carried by the shield of a twin-BNC cable to the body of the filtered hotswap and then again to the body of a V/4 box via an additional twin-BNC cable. The shield ends at the V/4 box as the high and low signal banana jack inputs to the box are electrically isolated from the body of the box. Configuring the measurement chain in this way ensures that the high and low twisted pair in the fridge connected to the gate of interest maintains an unbroken shield all the way to the voltage supply while minimizing shield loops.

The V/4 voltage division applied to the circuit arises from the resistor network within the V/4 box as shown schematically in Fig. 3.4. For a given input voltage from the SIM928 voltage supply v_i, the output voltage v_o is divided in the following way,

$$v_o = i \cdot 1.96k\Omega, \tag{3.1}$$

$$i = \frac{v_i}{R_{Tot}} \tag{3.2}$$

$$i = \frac{v_i}{7.84k\Omega}, \tag{3.3}$$

$$v_o = \frac{v_i \cdot 1.96k\Omega}{7.84k\Omega} \tag{3.4}$$

$$v_o = \frac{v_i}{4}. \tag{3.5}$$

After passing through the V/4 box, the divided voltage from the SIM928 is applied to one of the two inputs of the filtered hotswap. The two inputs allow for a second voltage supply or piece of hardware to be connected to the experiment at the same voltage as the first. Then by flipping the switch, a "hot" swap of the voltage supplies is performed, connecting the second input through to the experiment and disconnecting the first. The active input of the hotswap is determined by a 1-pole, 10-position, make-before-break switch limited to two positions, 1 and 2, as shown in Figs. 3.2,3.3(a). Ignoring the second input, a simplified version of the filtered hotswap circuit is shown in Fig. 3.5. AC simulation of the output voltage v_o of this circuit (exactly as shown) in LTSpiceIV is given in Fig. 3.6. [33] Analyzing this figure yields the cutoff frequency f_c and RC time constant τ for the filter (*NB: The contribution to f_c (τ) from the V/4 box is ignored in this analysis as it lowers (raises) the resulting frequency (time constant) by* $< 1\%$). Noting the -3dB compression point, our cutoff frequency is determined to be $f_c = 25.1$Hz, corresponding to a time constant $\tau = (2\pi \cdot f_c)^{-1} = 6.34$ms.

V/1000 voltage division for biasing an ohmic contact

Precise control of the source-drain bias across a quantum dot system is critical for experiments as it provides an absolute energy scale against which dot energy to gate voltage lever arms can be calibrated. It is also important to be able to keep applied biases controllably small compared to the electron temperature of the 2DEG (100mK = $8.62\mu V_{RMS}$). By adding a resistive voltage divider to the measurement circuit, one can apply $\pm$20mV source-drain biases with a resolution of $\pm 1\mu$V.

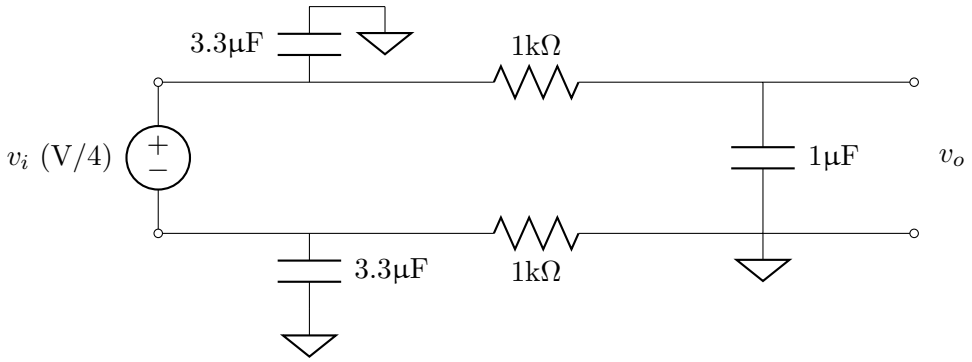

Figure 3.5: Filtered hotswap circuit for AC analysis. A simplified version of the filtered hotswap circuit from Fig. 3.3(a) to analyze the AC performance of the low-pass filter.

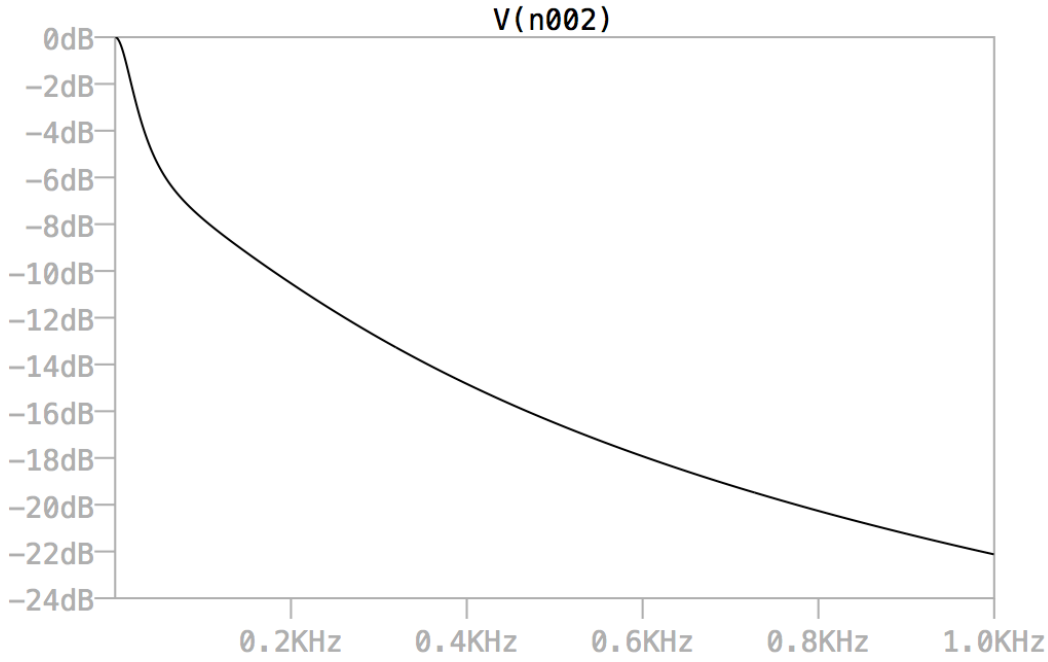

Figure 3.6: AC analysis of a filtered hotswap in LTSpiceIV. The solid black line is labeled by the left axis and shows the magnitude of the output voltage v_o in dB as a function of frequency. Noting the -3dB compression point yields a cutoff frequency of 25.1Hz. Simulation performed in LTSpice. [33]

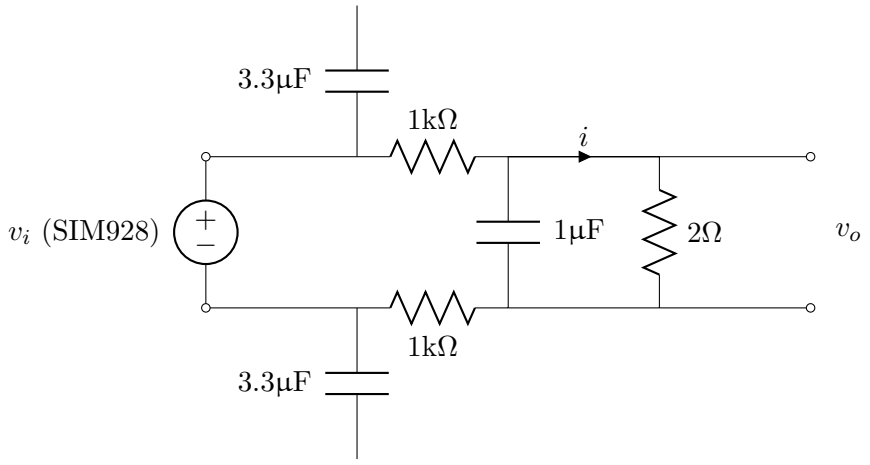

Figure 3.7: V/1000 circuit analysis. A simplified version of the V/1000 box circuit from Fig. 3.3(b) to analyze the output voltage of the circuit in the steady state.

As shown in Fig. 3.3(b), a V/1000 box is added after the filtered hotswap and before the breakout box. The placement of the V/1000 box within the circuit is critical as it relies on the resistors present in the previous boxes to provide the proper voltage division. The thick black lines represent electrical shield, thin black lines are signal low, and thin red lines are signal high. In a V/1000 measurement set up, the shield extends from the body of the fridge via the FTD cable to the body of a breakout box in the measurement rack. From there, electrical shield is carried by the shield of a twin-BNC cable to the body of the V/1000 box, then a filtered hotswap and then again to the body of a Thru box via additional twin-BNC cables. The shield ends at the Thru box as the high and low signal banana jack inputs to the box are electrically isolated from the body of the box. Configuring the measurement chain in this way ensures that the high and low twisted pair in the fridge connected to the ohmic of interest maintains an unbroken shield all the way to the voltage supply while minimizing shield loops.

The voltage division expected at the ohmic contact arises from a 2Ω resistor being placed between the high and low signal lines within the V/1000 box. As shown in a simplified circuit in Fig. 3.7, the resistors in the filtered hotswap combine with the resitors in the V/1000 box to yield a voltage division.

Ignoring the charged capacitors, for an applied voltage v_i from a SIM928 voltage supply, the output voltage v_o is divided by ∼1000 before being connected to the breakout box in the following

way,

$$
\begin{aligned}
v_o &= i \cdot 2\Omega, \\
i &= \frac{v_i}{R_{Tot}} \\
&= \frac{v_i}{2.002\mathrm{k}\Omega}, \\
v_o &= \frac{v_i \cdot 2\Omega}{2.002\mathrm{k}\Omega} \\
v_o &= \frac{v_i}{1001}.
\end{aligned} \tag{3.6}
$$

If any elements of this portion of the circuit are modified, the circuit should be reanalyzed to determine the new effective voltage division.

Measuring a current through a device with a DL1211 current preamplifier

Tune up and readout of a quantum dot device is performed in the following chapters through the measurement of a current flowing through the device. For example, coulomb blockade oscillations of a large multi-electron quantum dot are observed in the current flowing through the dot as a function of a changing gate voltage which modulates the dot's chemical potential. Typical currents through a quantum dot device are on the order of $10^{-8} - 10^{-14}$ amperes, requiring amplification before digitizing.

The amplifier used on the Triton is a Model 1211 current amplifier manufactured by DL Instruments (DL1211). Typical sensitivity specifications are shown in Table 3.1. As shown in Fig. 3.8, a DL1211 is added into the circuit after the breakout box. The thick black lines represent electrical shield, thin black lines are signal low, and thin red lines are signal high. In a current measurement, the shield extends from the body of the fridge via the FTD cable to the body of a breakout box in the measurement rack. From there, electrical shield is carried by the shield of a twin-BNC cable to the body of the metal box which encloses the amplifier. Following the signal, the shield is next carried from the output of the DL1211 enclosure via the shield of a twin-BNC cable to a Twin-BNC to BNC box connected to a model SR560 low-noise preamplifier manufactured by Stanford Research Systems (SR560). This box takes in a twin-BNC connection and breaks out the high and

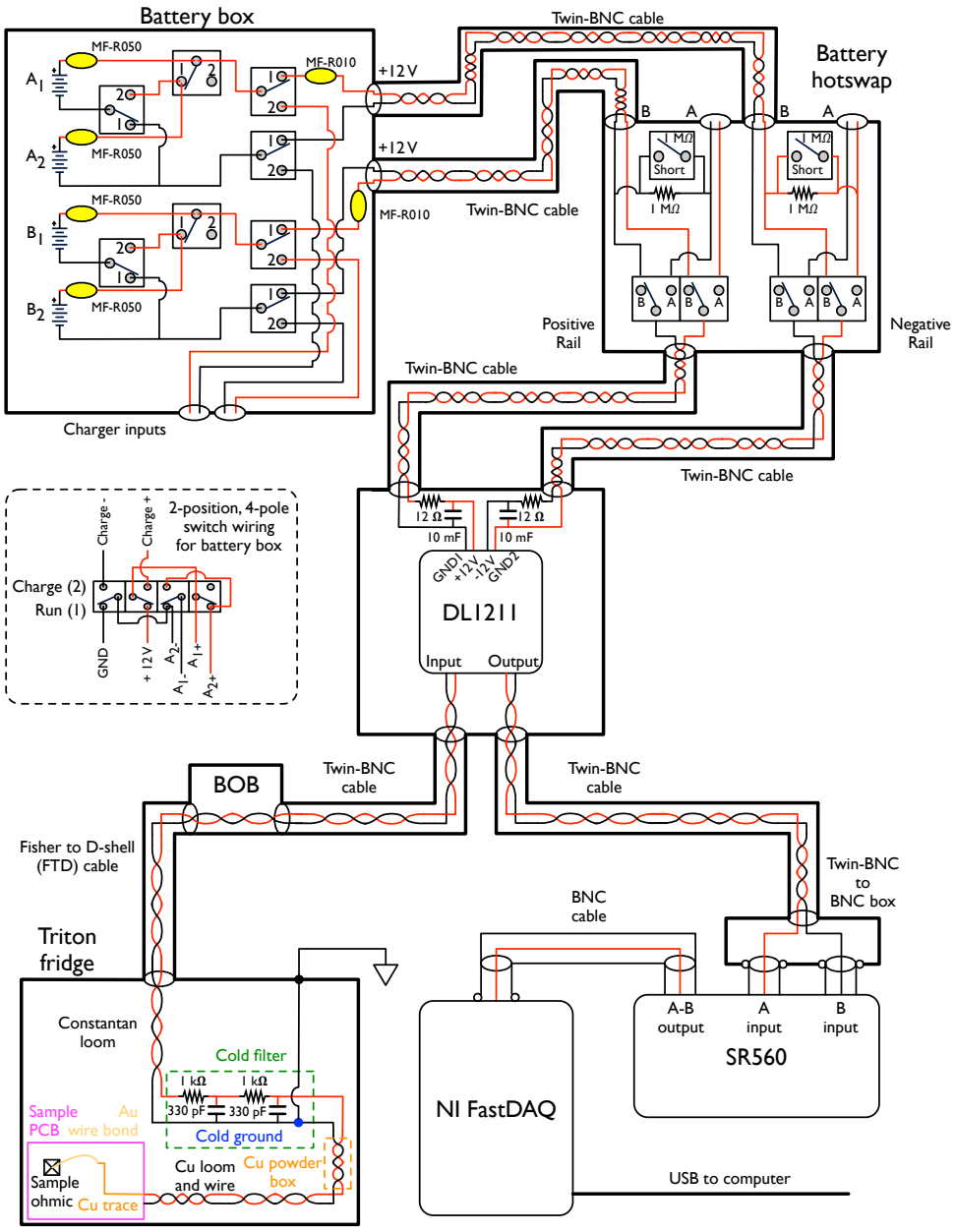

Figure 3.8: DL1211 measurement schematic.

low signal traces to each of the high pins of two BNC outputs. Shield is finally broken here at the Twin-BNC to BNC box, as the shields of the BNC outputs are isolated from the body of the box.

Sensitivity (A/V)	**Min. rise time (μs)**	**Input Z (Ω)**	**3dB BW (kHz)**	**Spectral noise density ($A_{RMS}/\sqrt{Hz}$)**
10^{-7}	25	200	25	60×10^{-15}
10^{-8}	40	2k	13	15×10^{-15}
10^{-9}	250	20k	4	5×10^{-15}

Table 3.1: DL1211 Specifications. Rise time, input impedance, 3dB BW, and spectral noise density is given for different values of sensitivity. Taken from Ref. [34].

On the other side of the amplifier enclosure, a custom external battery box is used to power the DL1211 instead of the building power supply. This is to avoid coupling excess noise into the measurement from a ground loop. The DL1211 requires two power inputs, one at +12V and the other at -12V. As shown at the top of Fig. 3.8, the battery box contains 4 battery packs, two for each input to the amplifier. Each battery pack consists of ten 1.2V nickel cadmium batteries connected in series to yield 12V with a total capacity of 1.8Ah. In addition to the batteries, the box includes two charging ports and two twin-BNC output ports. Two 2-position, 4-pole switches control the battery box's operation. The two switch positions are marked Run and Charge. When in the Charge position, the batteries are arranged in series and connected to the charge port for charging. When in the Run position, the batteries are arranged in parallel and output +12V with total capacity of 3.6Ah from each twin-BNC output. This yields a total run time for the DL1211 of $>$ 75 hours on one battery box before switching (a 1.2Ah battery runs the DL1211 for $>$ 25 hours [34]).

The +12V outputs from the battery box are next carried to the battery hotswap via two twin-BNC cables. The battery hotswap serves to swap battery boxes when their charge runs down without interrupting operation of the DL1211. The hotswap has four twin-BNC inputs, two 1-pole, 10-position, make-before-break switches limited to 2 positions only, and two 2-pole, 2-position, make-before-break switches. There are also two twin-BNC outputs. These are split to two switches, two inputs, and one output per voltage rail. Considering the positive rail first, the two inputs are labeled A and B. The high (red) connections from inputs A and B wired to one pole

of the 2-pole switch whose positions are marked as A and B as well. The position of the switch determines which input's high is connected to the output high. The low (black) connections from inputs A and B are wired in the same way to the other pole of the 2-position switch. In addition, a 1MΩ resistor is soldered between the low lines from each input before the switch. A 1-pole, 2-position switch is wired in parallel with the resistor such that when the switch is open, 1MΩ is between the adjacent low lines. When the switch is closed, the low lines are shorted. The -12V rail is identical to the +12V rail, except the high lines are tied with the resistor instead.

Given a set up that mirrors the one depicted in Fig. 3.8, batteries are swapped on the DL1211 by first connecting a second, charged battery box to the A input ports. The two switches on the positive and negative rail are then flipped from 1MΩ to Short. This ties the lows of the two batteries on each rail together to make them common. Next the switches on both rails are changed from B to A, swapping the battery powering the amplifier. Finally the first switches are returned to their original 1MΩ position and the depleted batteries can be disconnected and charged.

The health of the batteries is monitored by measuring the voltage between the high and low rails of each of the +12V outputs of the batteries (with their switches set to Run) both before and after they are swapped into the experiment. For a healthy, charged battery, the voltage at the +12V output should be greater than 14V. After running the DL1211 for ∼75 hours, the +12V output should still read greater than 12V. The voltage values should be recorded every time the batteries are swapped using a multimeter. If the measured voltage of a depleted battery starts to drop from swap to swap, the batteries should be replaced. In order to prevent unwanted damage to the batteries from accidental shorts during measurement of their voltages, polymeric positive temperature coefficient (PPTC) resettable fuses (manufactured by Bourns) have been installed in series into each of the battery boxes. Shown in Fig. 3.8 as a series of yellow ovals, these fuses contain conductive black carbon particles suspended in a lattice of a non-conductive, crystalline polymer. [35] At currents below a specified value (the hold current), the PPTC fuses are conductive with only a few Ohms of resistance. Above a different specified current value (the trip current), the fuse heats due to the dissipated power in the fuse (I^2R) and the polymer undergoes a phase transition to an amorphous state. In this condition, the black carbon particles are isolated from

each other which raises the resistance of the fuse by orders of magnitude, preventing current from flowing. Upon removal of the overcurrent condition, the fuse cools and the polymer returns to a crystalline state, reducing the resistance of the fuse back to a few Ohms. Specified values for the resettable fuses used on the Triton are shown in Table 3.2.

Model	I_{hold} **(A)**	I_{trip} **(A)**	**Initial Resistance Min. - Max. (Ω)**	**1 Hour Post-Trip Resistance (Ω)**	**Tripped Power Dissipation (W)**
MF-R010	0.10	0.20	2.50 - 4.50	7.50	0.38
MF-R050	0.5	1.0	0.41 - 0.77	1.17	0.75

Table 3.2: PPTC resettable fuse specifications. Taken from Ref. [35].

The outputs of the battery hotswap are labeled +12V positive rail and -12 negative rail and are carried to the DL1211 enclosure via two more twin-BNC cables. Inside the enclosure but before the current amplifier, a low-pass filter is installed on each rail to smooth any voltage changes from the power supply due to battery switching and reduce noise ($\tau = RC = 120ms,\ \ f_c = 1.33$Hz). The outputs of the low-pass filters are then connected to their corresponding inputs at the DL1211: GND1, +12, -12, GND2.

Typically, the battery, battery hotswap, and DL1211 enclosure are all mounted on top of the measurement rack as shown in Fig. 3.2. In order to prevent a ground loop, all three boxes are electrically separated from the rack by a large piece of wood, foam, or similar insulating material.

Finally, to measure a current from the DL1211 we use an SR560 as an isolation amplifier to isolate the measurement circuit from the PC where the data is stored. The two outputs from the Twin-BNC to BNC box are connected to the A and B inputs of the SR560. The amplifier is configured to perform a low-noise differential measurement, A-B, typically with a 3kHz low pass filter applied and unit gain (these can and should be changed depending on the conditions of the experiment). The resulting signal is applied to the center conductor of the SR560's BNC output. The outer conductor of the output BNC is tied to floating ground of the amplifier circuit. This high-level signal output can now be connected via a BNC cable to an NI FastDAQ data acquisition module manufactured by National Instruments without fear of generating a ground loop *within the measurement circuit.*

The NI USB-6216 model of the NI FastDAQ used on the Triton has 8 analog inputs with 16

bit resolution and 400kS/s (aggregate for multichannel measurments) maximum sampling rate for digitizing the output signal from our DL1211 current measurement. It is connected via USB to the measurement PC. As the ground reference signal from the SR560 is floating, a floating source (FS) circuit option is utilized on the DAQ (in fact all analog inputs on the DAQ are chosen to be set to floating source whether or not they are used). This circuit places a 5kΩ resitor with a 100pF capacitor in parallel between the outer conductor of the analog input and a common analog input signal ground. This sets the ground reference for the circuit to be defined by the SR560 instead of the power supply for the NI FastDAQ (ground referenced source or GS on the DAQ). As this signal ground is shared between all analog inputs, it is important to make sure excess charge doesn't build on unused inputs which would change the ground reference. This is mitigated by placing a 50Ω BNC terminator on one of the unused analog inputs.

Adder/divider box for coarse and fine gate voltage control

The adder/divider box allows for both coarse and fine gate voltage control. This is important when precise control of dot voltages is required (e.g. changing detuning between adjacent double dots). The adder/divider box has two inputs labeled A and B, and one output which provides the sum of the voltage applied at input A divided by ∼4 and the voltage applied at input B divided by ∼100.

As shown in Fig. 3.9(a), an adder/divider box is added before the filtered hotswap and breakout box. The thick black lines represent electrical shield, thin black lines are signal low, and thin red lines are signal high. In an adder/divider measurement set up, the shield extends from the body of the fridge via the FTD cable to the body of a breakout box in the measurement rack. From there, electrical shield is carried by the shield of a twin-BNC cable to the body of a filtered hotswap and then again to the body of the adder divider box. Finally the electrical shield is carried by the shield of two additional twin-BNC cables to two Thru boxes connected to SIM928 voltage supplies. As with the V/1000 circuit, the shield ends at the Thru box as the high and low signal banana jack inputs to the box are electrically isolated from the body of the box. Configuring the measurement chain in this way ensures that the high and low twisted pair in the fridge connected to the gate of interest maintains an unbroken shield all the way to the voltage supply while minimizing shield

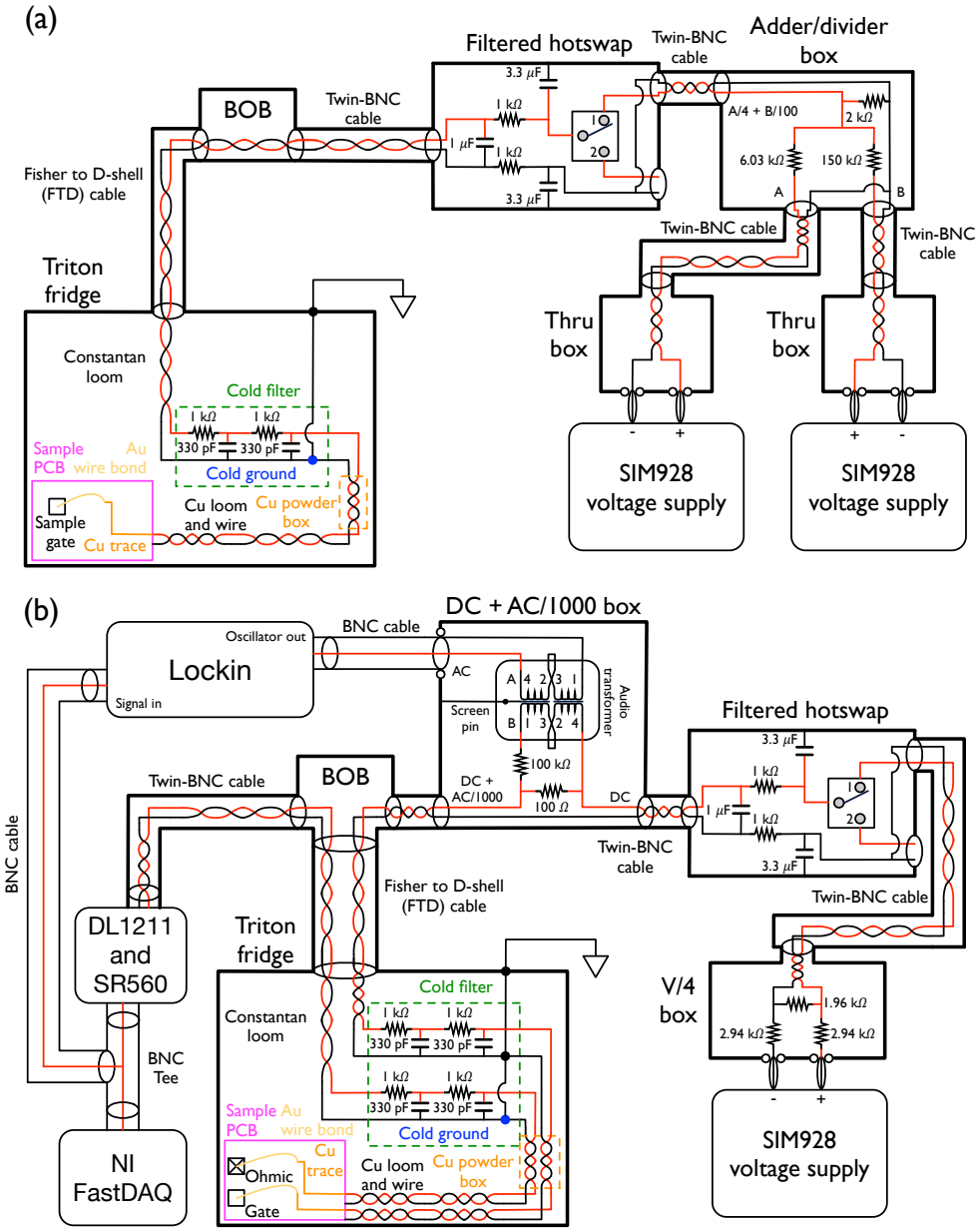

Figure 3.9: Measurement schematic for an adder/divider box and a DC + AC/1000 box. **(a)** Measurement schematic for applying a V/4 and V/100 divided voltages to a device gate for coarse and fine voltage control. **(b)** Measurement schematic for applying an AC/1000 divided voltage to a DC gate bias for a lockin measurement.

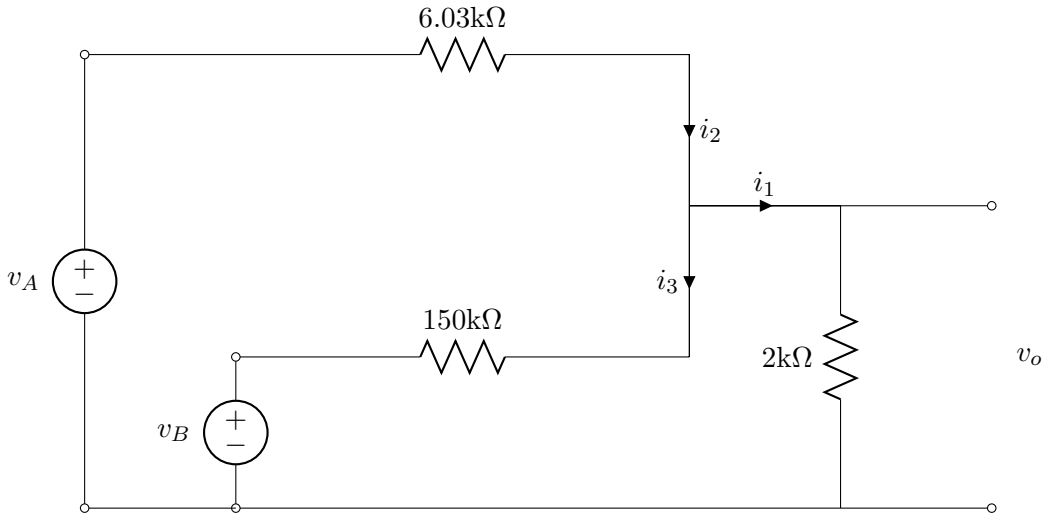

Figure 3.10: Adder/divider circuit analysis.

loops.

The voltage division expected at the device arises from resistor network within the adder/divider box. Because the adder/divider box is included in the circuit before the filtered hotswap, it's voltage divisions are insensitive to whatever corner frequency is chosen for the hotswap. Analyzing a simplified circuit as shown in Fig. 3.10 allows us to determine how the resistors in the adder/divider box provide a summed and resistively divided voltage to the output. From Kirchoff's laws, our currents are,

$$i_3 = \frac{i_1 \cdot 2\text{k}\Omega - v_B}{150\text{k}\Omega}, \tag{3.7}$$

$$i_2 = \frac{v_A - i_1 \cdot 2\text{k}\Omega}{6.03\text{k}\Omega}, \tag{3.8}$$

$$i_1 = i_2 - i_3. \tag{3.9}$$

The output voltage of the adder/divider circuit is determined by Ohm's law as $v_o = i_1 \cdot 2\text{k}\Omega$.

Plugging in our expressions from Eqs. 3.7-3.9 yields our final output voltage v_o,

$$\begin{aligned} i_1 &= i_2 - i_3 \\ i_1 &= \frac{v_A}{6.03\text{k}\Omega} - \frac{i_1 \cdot 2\text{k}\Omega}{6.03\text{k}\Omega} - \frac{i_1 \cdot 2\text{k}\Omega}{150\text{k}\Omega} + \frac{v_B}{150\text{k}\Omega} \\ \frac{v_o}{2\text{k}\Omega} &= \frac{v_A}{6.03\text{k}\Omega} - \frac{v_o}{6.03\text{k}\Omega} - \frac{v_o}{150\text{k}\Omega} + \frac{v_B}{150\text{k}\Omega} \\ v_o &= \left(\frac{v_A}{6.03\text{k}\Omega} + \frac{v_B}{150\text{k}\Omega}\right) \cdot \left(\frac{1}{2\text{k}\Omega} + \frac{1}{6.03\text{k}\Omega} + \frac{1}{150\text{k}\Omega}\right)^{-1} \\ v_o &= 0.2466 v_A + 0.0099 v_B. \end{aligned} \tag{3.10}$$

DC + AC/1000 box for applying an AC signal to a DC gate voltage

The DC + AC/1000 box is used to apply a small AC modulation on top of a DC gate bias. This is particularly useful when performing a measurement with a lock-in amplifier. A lock-in amplifier takes advantage of the fact that when integrating the product of two sinusoidal functions of different frequencies for a period of time longer than the periods of either sinusoid, the result is zero. In the context of a quantum dot measurement, a system with a lot of noise may make identifying a signal of interest difficult. By applying a small AC modulation to a device gate at a given frequency (where small implies that the feature of interest controlled by that gate is not broadened by the AC signal) and reading out the device current with a lock-in at that frequency, the signal may be recovered from the noise.

As shown in Fig. 3.9(b), a DC + AC/1000 box is added after the filtered hotswap and before the breakout box. The thick black lines represent electrical shield, thin black lines are signal low, and thin red lines are signal high. In a DC + AC/1000 lock-in measurement set up, the shield extends from the body of the fridge via the FTD cable to the body of a breakout box in the measurement rack. On one side of the circuit, electrical shield is carried by the shield of a twin-BNC cable to the body of the DC + AC/1000 box and then again to the body of the filtered hotswap box. Finally the electrical shield is carried by the shield of an additional twin-BNC cable to a V/4 box connected to a SIM928 voltage supply. As with the V/1000 circuit, the shield ends at the V/4 box as the high and low signal banana jack inputs to the box are electrically isolated from the body of the box. The other side of the circuit is simply a current measurement by a DL1211 current amplifier,

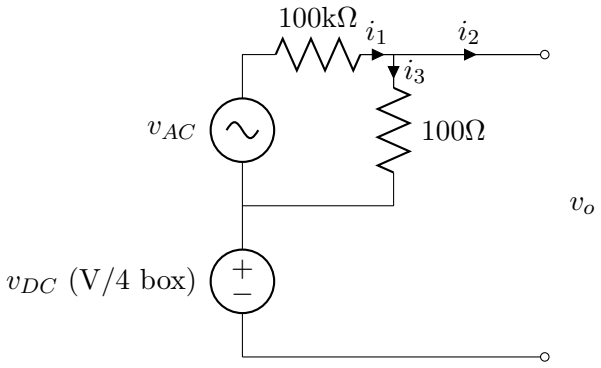

Figure 3.11: DC + AC/1000 box circuit analysis.

as described earlier in this chapter.

The DC + AC/1000 box has two inputs and one output. The DC input and summed and divided output are both connected to twin-BNC connectors. The AC input however is connected to the box via an isolated BNC connector. This prevents the ground (low) signal input from the AC source (e.g. the oscillator output from a lock-in) from being connected to the experiment shield forming a ground loop. The ground (low) input from the AC input must also be isolated from the signal low in the measurement circuit in order to avoid forming another ground loop. This is done by relying on a 1:1 audio transformer (30-30kHz, manufactured by Vigortronix) to inductively couple the AC signal into the measurement circuit.

The voltage expected at the device arises from resistor network within the DC + AC/1000 box. Analyzing a simplified circuit as shown in Fig. 3.11 allows us to determine how the resistors in the DC + AC/1000 box provide a summed and resistively divided voltage to the output. From Kirchoff's laws, our currents are,

$$i_3 = \frac{v_o - v_{DC}}{100\Omega}, \tag{3.11}$$

$$i_2 = i_1 - i_3, \tag{3.12}$$

$$i_1 = \frac{v_{DC} + v_{AC} - v_o}{100k\Omega}. \tag{3.13}$$

The output voltage of the DC + AC/1000 circuit is determined by plugging in our expressions

from Eqs. 3.11-3.13 and solving for our final output voltage v_o,

$$\begin{aligned} i_3 = \frac{v_o - v_{DC}}{100\Omega} &= i_1 - i_2 \\ \frac{v_o - v_{DC}}{100\Omega} &= \frac{v_{DC} + v_{AC} - v_o}{100k\Omega} - i_2 \\ v_o \cdot \left(\frac{1}{100\Omega} + \frac{1}{100k\Omega}\right) &= v_{DC} \cdot \left(\frac{1}{100\Omega} + \frac{1}{100k\Omega}\right) + \frac{v_{AC}}{100k\Omega} - i_2 \\ v_o &= v_{DC} + \frac{v_{AC}}{1001} - \frac{100000}{1001}\Omega \cdot i_2. \end{aligned} \tag{3.14}$$

We note that the first two terms of the right hand side of our solution in Eq. 3.14 are exactly what we desired, $v_o = v_{DC} + v_{AC}/1001$. We are left however with an additional term $-(99.9\Omega) \cdot i_2$ that we must reconcile. In the case where our DC + AC/1000 signal is connected to a device gate (as shown in Fig. 3.9(b)), $i_2 = 0A$ in the steady state due to the fact that a device gate represents an infinite impedance load (open circuit). Thus, we neglect the extra term and take the expected result. If however the DC + AC/1000 box is connected to an ohmic contact, $i_2 \neq 0A$ and our additional term can no longer be neglected. This results in a modified output signal from the DC + AC/1000 box where the magnitude of the deviation from the expected output value is determined by the resistance of the rest of the measurement circuit and the 2DEG of the device under test.

Chapter 4

Transport through an impurity tunnel coupled to a Si/SiGe quantum dot

Contents of this chapter reprinted from [3], with the permission of AIP Publishing: R. H. Foote, D. R. Ward, J. R. Prance, J. K. Gamble, E. Nielsen, B. Thorgrimsson, D. E. Savage, A. L. Saraiva, M. Friesen, S. N. Coppersmith, and M. A. Eriksson, "Transport through an impurity tunnel coupled to a Si/SiGe quantum dot," *Appl. Phys. Lett.*, vol. 107, p. 103112, 2015.

4.1 Introduction

Donors in silicon are a natural choice for qubits, [5] because their electron and nuclear spins have very long coherence times. [10, 12, 20, 36–38]Although donor-based quantum devices can be fabricated with near-atomically precise placement of donors, [39, 40] even when well-placed, it is difficult to control and change the tunnel couplings between them with gate voltages. In contrast, tunnel couplings are easily tunable in gate-defined quantum dots, and high-quality quantum dots hosting at least four different types of spin qubits have been demonstrated. [41–53] Moreover, the electrons in quantum dots can be displaced laterally simply by changing the voltages of the gates on the surface. [54] Because of the differences between donors and quantum dots, it is interesting to ask whether donors or other localized defects can be tunnel-coupled to gate-defined quantum dots in Si/SiGe heterostructures.

Here we report the observation of a controllable tunnel coupling between a localized electronic state and a gate-defined quantum dot formed in a Si/SiGe heterostructure. We present measurements of transport through the device, demonstrating controllable tunnel coupling between the quantum dot and the localized state. A set of stability diagram measurements enable a determination of the relative magnitude of the capacitance between the surface gates and both the quantum dot and the localized state. We report the expected electron density profiles in the quantum dot and the neighboring reservoirs. Combining the experimental results with 3D capacitive modeling based on the electron density profiles, we determine the most likely location of the localized state in the device. These results demonstrate that it is possible to control the tunnel rate between localized states and quantum dots, notwithstanding the dramatic difference in the characteristic length scales.

4.2 Results

A gate-defined quantum dot, shown in Fig. 4.1, was fabricated in a $Si/Si_{0.68}Ge_{0.32}$ heterostructure grown by chemical vapor deposition on a relaxed buffer layer with a surface smoothed by chemical-mechanical polishing. Measurements were performed in a dilution refrigerator with a mixing chamber temperature $T_{MC} < 30$ mK.

Fig. 4.1(c) shows Coulomb diamonds characteristic of Coulomb blockade with an average charging energy $E_c = 760$ μeV. By comparing this charging energy with the charging energies of few-electron Si/SiGe quantum dots, [55] we find that this quantum dot is in the many electron regime. We also obtain, from the excited states visible in Fig. 4.1(c), an estimate of the single-particle energy of about 380 μeV in this quantum dot. The data also enable the extraction of the proportionality constant (the lever arm) $\alpha_{G2} = 148$ μeV/mV between the voltage on gate G2 and the energy of the quantum dot.

The red arrows near the center of Fig. 4.1(c) highlight an additional sharp, isolated charging event. Over this range in gate voltage, 13 electrons are added to the main dot, yet only this one additional feature is observed. The capacitances between various gates and the object corresponding to this feature are different from those corresponding to the quantum dot. This difference is made

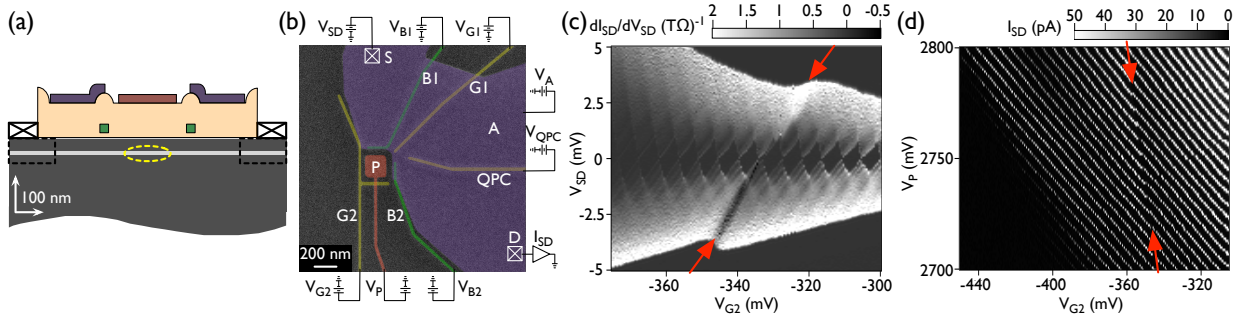

Figure 4.1: Device design and characterization. **(a)** Schematic side view of the device, showing a $Si/Si_{0.68}Ge_{0.32}$ heterostructure with a 10 nm Si well (light grey) and 32 nm SiGe offset (dark grey). Both the upper (purple and red) and lower (green) layers of gates are 2 nm titanium and 20 nm gold deposited by electron beam evaporation. The lower (upper) gates were deposited on 10 nm (90 nm) of atomic layer deposition grown aluminum oxide (light orange). Ohmic contacts S and D (denoted with ⊠ symbols) are 5 nm titanium and 40 nm gold on a region degenerately doped with phosphorus through the quantum well (black dashed boxes). Approximate location of the quantum dot and impurity are shown schematically by the yellow dashed oval. **(b)** False-color SEM of a device identical to the measured device. Upper gate A (purple) and paddle gate P (red) were positively biased to accumulate a two-dimensional electron gas in the reservoir and to control the energy of the dot, respectively. On the lower level, gates G1, G2, and QPC (yellow) were negatively biased to provide the confinement potential; gates B1 and B2 (green) controlled the tunnel barriers to the source (S) and drain (D) ohmic contacts (denoted with ⊠ symbols). **(c)** The derivative $dI_{\mathrm{SD}}/dV_{\mathrm{SD}}$ of the transport current with respect to the gate voltage V_{G2}, showing Coulomb diamonds. A sharp resonance, indicated by arrows, is observed, suggesting a localized state. **(d)** Coulomb blockade oscillations of the current I_{SD} at fixed $V_{SD} = 100$ μV. The jump indicated by arrows corresponds to the localized state in (c).

clear in Fig. 4.1(d), which reports the current through the quantum device as a function of the voltages on gate P and G2. The phenomenology of this plot is very similar to those observed in metal-oxide-semiconductor devices in which donors have been implanted: [56, 57] near the center of the scan, a series of shifts in the charge transitions of the dot can be observed; these shifts correspond to the feature marked by the red arrows in Fig. 4.1(c). The line through the gate voltage space spanned by V_P and V_{G2} connecting these shifts has a different slope than that of the Coulomb blockade peaks corresponding to the dot, confirming the presence of a nearby localized state that is not at the same physical position as the dot. The current at the intersection of the charge transitions between the dot and the localized state can be used to gain insight into the tunnel coupling between the localized state and the quantum dot; we show below that this current

is a repeatable function of the gate voltages in the device.

Figure 4.2(a) shows the source-drain current I_{SD} versus V_P and V_{B1}. The dashed black lines indicate the voltages at which the localized state charges, corresponding to the observed shift and gap in the Coulomb blockade peaks. The pattern of lines and slopes in Fig. 4.2(a) matches the expectation for a two site system, which here corresponds to the quantum dot and a localized state. [20] No current is observed along the black dashed lines in this figure, indicating that the localized state is not tunnel coupled to both the source and the drain. It is possible, however, that the localized state is connected to either the source or the drain, and this hypothesis is supported by the faintly visible line of current (white in the color scale) that sits at the position of the polarization line at each of the three main intersections in this stability diagram.

Figures 4.2(b,c) show a pair of triple points in this two-site system, for two different values of the voltage on gate B2. In both plots, there is no current along the black dashed lines corresponding to the charge transition of the localized site, confirming that the localized site is not tunnel-coupled to both the source and the drain. However, in Fig. 4.2(b), where $V_{\mathrm{B2}} = -402$ mV, current is observed along the polarization line; in contrast, no such current is observed in Fig. 4.2(c), where $V_{\mathrm{B2}} = -404$ mV. This current is studied in more detail in Fig. 4.2(d), where we report line cuts across the polarization line, as indicated by the gray dashed line in Fig. 4.2(b). Fig. 4.2(d) shows a dramatic evolution of the current along this path as V_{B2} is changed. For V_{B2} equal to either -398 or -401 mV, no peak in current occurs at the polarization line. In contrast, for intermediate values of V_{B2} = -399 and -400 mV, a prominent peak in current is observed at the position of the polarization line. The current peak is visible over a narrow voltage range in V_{B2}. Each line scan in Fig. 4.2(d) covers all values of detuning near and at the polarization line, yet only two of them (for specific values of V_{B2}) yield peaks in the measured current. Thus, the tunnel coupling is modified independently of the detuning energy.

The difference between the current peak shown in Fig. 4.2(d) and the conventional Coulomb peaks corresponding to the quantum dot is also highlighted by the temperature dependence of each peak. The inset to Fig. 4.2(e) shows the temperature dependence of the Coulomb blockade peak for the single dot, which is tunnel coupled to both the source and the drain, for gate voltages

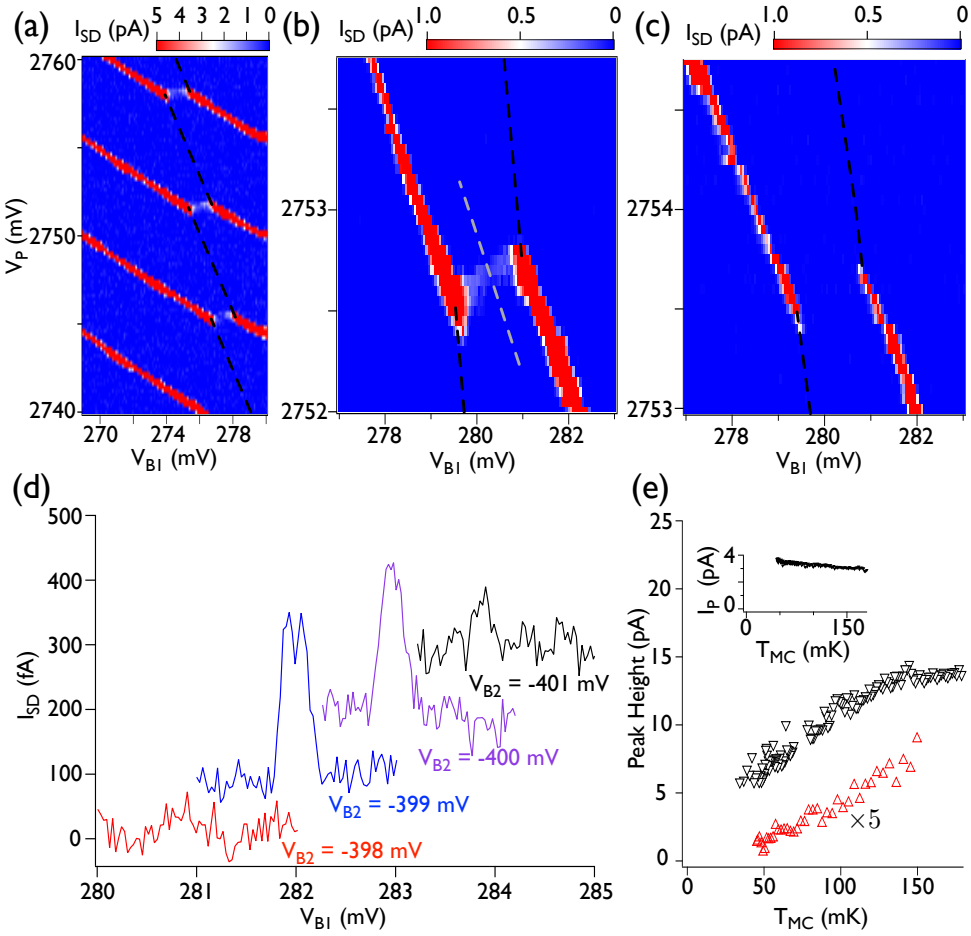

Figure 4.2: Control of tunnel coupling. **(a)** I_{SD} as a function of $V_{\rm P}$ and $V_{\rm B1}$, with $V_{B2} = -400$ mV, showing jumps in the Coulomb blockade transitions. A double dot-like stability diagram is revealed, including a weak polarization line. The localized state charge transitions are not visible and are shown schematically as black dashed lines. **(b) &** **(c)** High resolution scans across a polarization line, for $V_{B2} = -402$ mV in (b) and $V_{B2} = -404$ mV in (c). Current is present at the polarization line in (b) but not in (c). **(d)** Line scans across the polarization line as a function of $V_{\rm B1}$, acquired by sweeping $V_{\rm P}$ and $V_{\rm B1}$ simultaneously, following a path exemplified by the light gray dashed line in panel (b). The data for $V_{B2} = -398$ mV are not shifted; subsequent traces are offset vertically by 100 fA and laterally by 1 mV each. These plots, which were acquired in close succession in time, show that changing V_{B2} changes the tunnel couplings to the localized state, turning on and off current at the polarization line. (The overall conditions in this plot are slightly different than those in panels (b) and (c).) **(e)** Black triangles show the height of the main Coulomb blockade peak near the anticrossing with the localized state, and red triangles show the height of the current peak on the polarization line, both of which are strongly temperature dependent. *Inset:* Coulomb blockade peak height $I_{\rm P}$ far from the anticrossing with the localized state vs. temperature, showing behavior typical for a large dot at reasonably low temperature. [58]

such that the localized state is not involved in the transport. The current is nearly constant as a function of temperature, rising slightly as the temperature drops, consistent with a reasonably large quantum dot at temperatures T for which $kT \ll E_c$ (Ref. [58]). In the main panel of Fig. 4.2(e), the black inverted triangles show the temperature dependence of the main Coulomb blockade peak very close to the anticrossing with the localized state, and the red triangles show the temperature dependence of the current peak on the polarization line. In contrast with the behavior in the inset, both of these peaks increase strongly with increasing temperature. This behavior is consistent with a localized state tunnel coupled to the dot and one (but not both) of the reservoirs. Considering first the main Coulomb peak: on this peak, transport through the dot is allowed (by definition), whereas accessing the localized state requires thermal activation. At elevated temperatures, where transport through the impurity is activated, a significant and new parallel path to exit the dot is opened, increasing the total current by an amount that is comparable to the current in the absence of this new path. Considering the polarization line peak (which is more than 5 times weaker than the main Coulomb peak): this current is suppressed at low temperature. Although charge can shuttle between the dot and the localized state at no energy cost at this position in gate voltage space, it cannot tunnel to or from the leads—raising the temperature activates this process, but only more weakly than for the main Coulomb peak, because additional charge is forbidden on both the dot and the localized state.

To determine the location of the localized state, we combine transport measurements with electrostatic device modeling. [59, 60] As shown in Fig. 4.3(a), we acquire five stability diagrams, sweeping gate voltage V_P, which we use as our reference, as we step five other voltages: V_{G1}, V_{B1}, V_{G2}, V_{QPC}, and V_{B2}. For each scan, all other voltages are held fixed to their values at a central operating point. To interpret these data, we constructed an electrostatic device model in COMSOL Multiphysics, [61] using the device geometry from the experiment, as illustrated in Fig. 4.3(b). The model was solved in the Thomas-Fermi Approximation, [62, 63] with the self-consistent charge accumulation determined using a 2D density of states confined to a sheet at the Si-SiGe interface. We assumed a 2×2 carrier degeneracy due to (2) spin and (2) valley degrees of freedom. The computational domain was 3×5 μm laterally, and included a 100 nm air cap above

the oxide layer and 500 nm SiGe substrate below the silicon well. We used zero-field boundary conditions on the sides of the domain and the top of the air cap, and set the conduction band edge to the Fermi level at the bottom of the domain. In addition, we used voltages: $V_{G2} = -0.335$ V, $V_{B2} = -0.400$ V, $V_{QPC} = -0.100$ V, $V_{G1} = -0.104$ V, $V_{B1} = +0.270$ V, $V_A = +2.75$ V, and $V_P = +2.75$ V.

We approximate the dot and reservoir regions predicted by COMSOL as 5 nm thick metallic sheets at the 6×10^{11} cm^{-2} density contour (Fig. 4.3(b)), and we treat the localized state as a 1 nm radius metallic sphere. Given a placement of the localized state, we construct a capacitance model predicting each of the experimental stability diagrams. [64] We raster the localized state position across the device and compute as a fit metric a weighted sum-of-squared-differences between experimental and predicted values. We estimate the location of the localized state that is most consistent with the data shown in Fig. 4.3(a). In particular, we sum the squared differences of (1) the slope of the line connecting all of the "offsets" in the Coulomb blockade lines (the white dashed lines in Fig. 4.3(b)), and (2) the magnitude of the jump along the y-axis of a Coulomb blockade line due to the localized state. Type 1 quantities are unitless slopes whereas type 2 quantities have units of energy. To combine these into a single discrepancy metric, we found empirically that we needed to scale the type 2 quantities reported in meV by 1×10^8 to balance them with the quantities of type 1. Thus, the overall discrepancy metric is

$$DIS = \sum_{i=1}^{5} (PO_i - EO_i)^2 + 1 \times 10^8 \times \sum_{i=1}^{5} (PJ_i - EJ_i)^2, \tag{4.1}$$

where i indexes each of the five experimental slices shown in Fig. 4.3(a), PO and EO are the predicted and experimental type 1 offset quantities, and PJ and EJ are the predicted and experimental type 2 jump quantities respectively. The lower layer of Fig. 4.3(b) shows a cut of DIS along a plane 12 nm beneath the top of the strained Si well, identifying a region under the tip of gate G1 as the most likely region in the x-y plane to find the localized state. The DIS value is not very sensitive to the depth (z-coordinate) between 10 and 20 nm; the 12 nm data is shown.

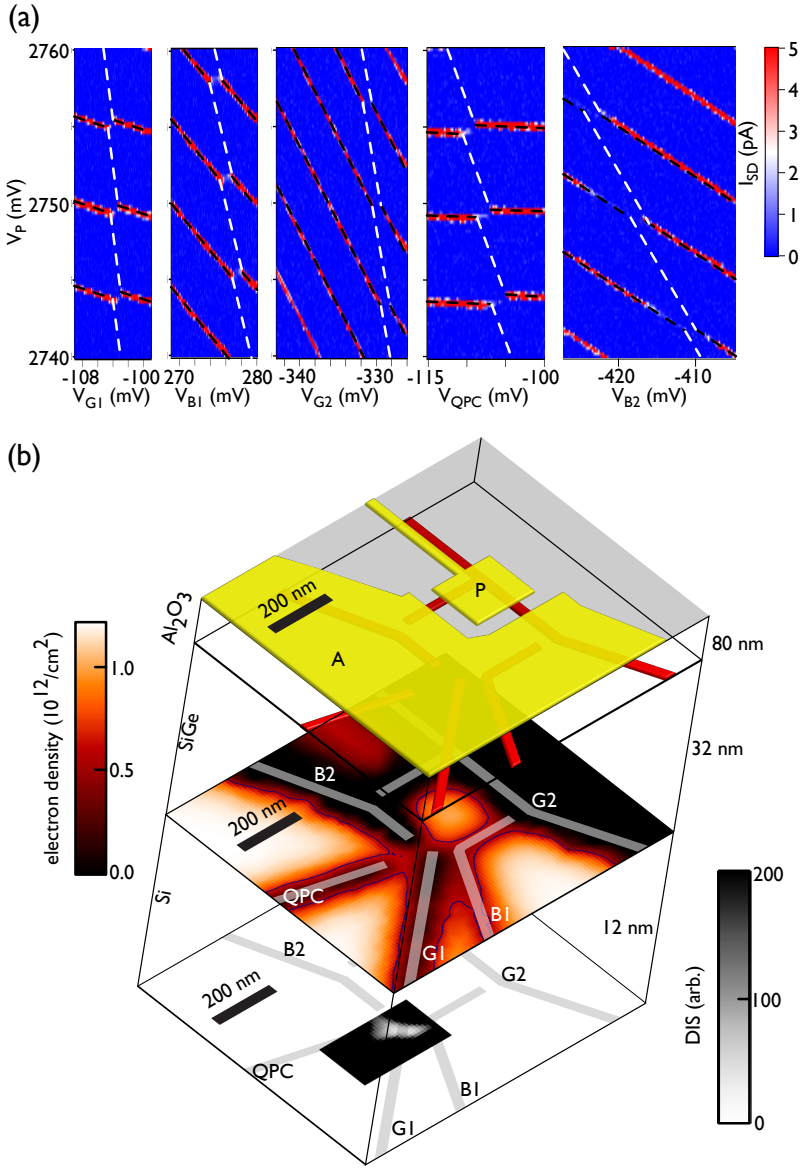

Figure 4.3: Locating the localized state by combining experiment and modeling. **(a)** Stability diagrams at fixed V_{SD} for several gate voltage pairs. The black dashed lines highlight Coulomb blockade transitions of the dot while the white dashed lines show the expected position of the unseen localized state charging event. **(b)** Results of 3D electrostatic modeling to determine the location of the localized state. The top layer shows the gate geometry of the device local to the dot. The middle layer shows the electron densities of the dot and leads as calculated by COMSOL, with the contour corresponding to 6×10^{11} cm^{-2} electron density. The bottom layer of the device shows the most likely location of the impurity, as determined by the discrepancy metric (Eq. (4.1)), directly under the tip of gate G1 near the lower Si/SiGe interface about 10 nm below the top of the quantum well.

4.3 Discussion

We propose a tunnel rate dependent model of our hybrid quantum dot-impurity system. Under typical device operation, the impurity is tunnel coupled to one of the leads and only very weakly tunnel-coupled to the dot. Under these conditions, a charging event of the localized state varies the electric field local to the dot, changing the Coulomb blockade condition and resulting in the familiar jump in the dot charge transition from Fig. 4.2(c). Changing the voltage of the tunnel barrier V_{B2} changes the dot-drain, impurity-drain, and dot-impurity tunnel rates. While the exact dependence on V_{B2} of each of these tunnel rates is complicated and difficult to predict, for certain gate voltage tunings, like those shown in Fig. 4.2(b), the dot-impurity tunnel rate increases, and the three tunnel rates together—especially the enhanced dot-impurity tunnel rate—allow for current through the normally blockaded region as well as enhancement of current corresponding to the dot charge transitions.

In conclusion, we have shown measurements and modeling of a tunnel coupled quantum dot-impurity system in a Si/SiGe heterostructure. We demonstrated tunable tunnel coupling between the impurity and the dot that is controlled by varying a nearby gate voltage, and we reported the temperature dependence of the coupled system. We also have found the most likely position of the localized stated through capacitive modeling, with the capacitances extracted from this model in good agreement with the experimental results. Moving forward, we propose that the use of quantum wells closer to the surface and gate electrodes placed more closely together should enable even finer control over the coupling between a localized state and a quantum dot.

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Chapter 5

State-conditional coherent charge qubit oscillations in a Si/SiGe quadruple quantum dot

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5.1 Introduction

Since being proposed theoretically [5, 6], much experimental and theoretical progress has been made towards the development of a scalable quantum computing architecture using electrically gated semiconductor quantum dot-based spin qubits [9, 20, 38, 41, 43, 45, 48–51, 65–75]. Two-qubit gates are essential, and capacitive coupling has been used in GaAs quantum dot-based spin qubits to demonstrate both conditional singlet-triplet exchange oscillations [76], and the generation of the entanglement of two neighboring singlet-triplet qubits [47]. Recently, one and two-qubit gate operations have been demonstrated in ^{28}Si-based quantum dot spin qubits [53, 77], harnessing

the substantial improvement in coherence time achievable through isotopic purification and the corresponding reduction in nuclear spin density. Improving gate speeds provides an alternative route to realize high fidelity single and multi qubit gates, and intensive efforts have been made to realize fast manipulation of semiconductor spin qubits by mixing the spin degrees of freedom with charge degrees of freedom through spin-orbit coupling or the introduction of micromagnets [42, 78, 79].

Motivated by the search for high-speed qubits with strong interactions, semiconductor quantum dot charge qubits also have been studied and qubit manipulations performed in both GaAs [80–83] and Si [84, 85], with typical charge qubit coherence times of the order of 100 ps to 10 ns. Strong capacitive coupling between double dots is essential for two qubit gates, and measured interdot capacitive couplings in GaAs quantum dots are in the range 25–120 μeV [86–88]. This capacitive coupling has been used to perform conditional rotations of a GaAs charge qubit [88], yet similar measurements so far have not been possible in silicon-based quantum dots. Moreover, dopant-free devices, which have recently become prevalent for Si/SiGe quantum dot qubits, require a blanketing array of metal electrodes that partially screen the capacitive coupling, making this issue all the more urgent. [13, 45, 50, 79, 89–91]

Here, we present measurements of a quadruple quantum dot formed in an undoped Si/SiGe heterostructure and demonstrate fast and charge-state-conditional coherent manipulation of two strongly coupled double quantum dots. Non-adiabatic pulsed gate techniques allow fast two-axis control of the double dot charge qubit formed. We show that the strong capacitive coupling ($>$ 18 GHz) between two sets of double quantum dots enables charge-state-conditional coherent Landau-Zener-Stückelberg interference with a conditional π phase flip time of approximately 80 ps, demonstrating progress toward realizing high-fidelity two-qubit control. Although we focus here on conditional coherent operations of a charge qubit, the measurement strategy and strong inter-qubit coupling deduced from the present study can also be directly applied to singlet-triplet [47] or hybrid quantum dot qubits [51, 72] where strong capacitive coupling will play an essential role in the realization of fast two qubit gates.

5.2 Results

We study a linear quadruple quantum dot formed in an undoped Si/SiGe heterostructure, as shown in Fig. 5.1(a). The dots are formed under the gates D_1 through D_4, approximately under the dashed line shown in Fig. 5.1(a), and for the experiments we report here, it is useful to describe the quadruple quantum dot as a pair of double quantum dots. The right double dot (RDD), formed under the gates D_3 and D_4, forms a charge qubit that will be manipulated coherently based on the charge state of the left double dot (LDD), which is formed under gates D_1 and D_2. Charge sensing is performed by two charge sensing quantum dots adjacent to the left (LSD) and right (RSD) hand sides of the quadruple dot array. The location of sensor RSD is close to the position that would naively be expected by examination of Fig. 5.1(a); to improve its charge sensitivity, sensor LSD is shifted to a position very close to the quadruple dot by careful tuning of the large number of gate voltages available on that side of the device. We monitor changes in the conductances g_{L} and g_{R} of sensor dots LSD and RSD, respectively, to monitor the electron occupations of double dots LDD and RDD. Figures 5.1(c) and 5.1(d) show charge stability diagrams for the LDD (**c**) and RDD (**d**), demonstrating control of the four dot occupations as a function of the four gate voltages V_{D1}, V_{D2}, V_{D3}, and V_{D4}. As we show in Supplementary Fig. 5.5(e), the tunnel coupling and the capacitive coupling between the LDD and RDD both are reduced when the LDD has lower electron occupation. Thus, we perform here coherent manipulation in the regime for which the LDD has a total electron occupation larger than (10,10).

We first show coherent two-axis control of an undoped Si/SiGe double dot charge qubit formed in the RDD. For this demonstration, the LDD energy detuning ε_{L} is kept >300 μeV so that the LDD charge occupation is not affected by the RDD manipulation pulses. The charge qubit states are defined as $|0\rangle_{\mathrm{R}} = |L\rangle$ (excess charge is on the left dot) and $|1\rangle_{\mathrm{R}} = |R\rangle$ (excess charge is on the right dot). The initial qubit state $|0\rangle_{\mathrm{R}}$ is prepared at negative RDD energy detuning ε_{R}. As shown schematically in Fig. 5.2(a)-(c), non-adiabatic control of the charge qubit is performed using abrupt changes in detuning energy with precise control of the pulse duration time as well as the amplitude. The pulses, generated using a Tektronix AWG70002A arbitrary waveform generator (AWG) with a rise time of 40 ps, are applied to gate D_3 through a commercial bias tee (Picosecond PulseLabs

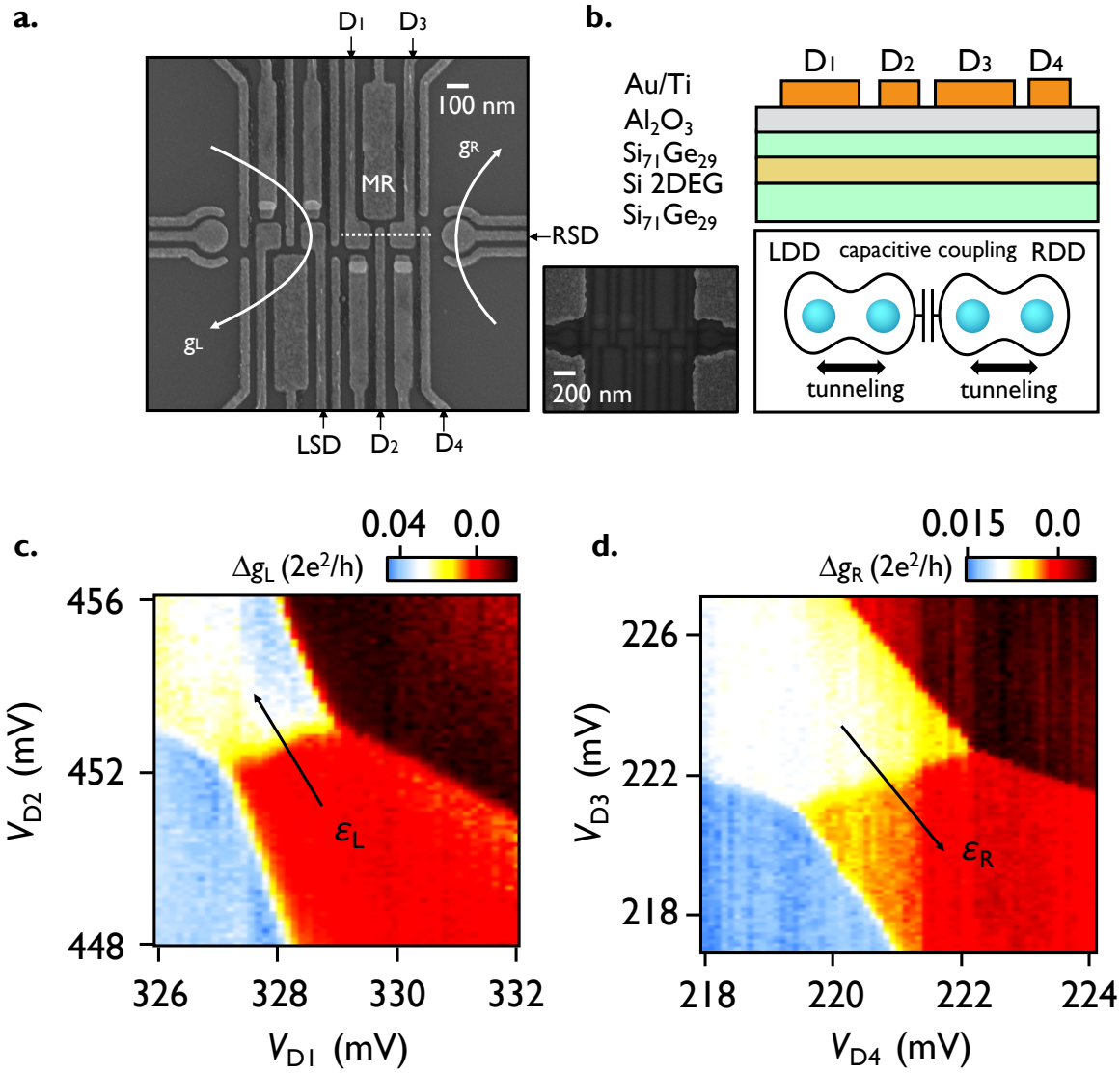

Figure 5.1: Si/SiGe device structure and charge stability diagrams of a pair of double quantum dots. **a.** Scanning electron microscope image and schematic labeling of a device lithographically identical to the one used in the experiment. For clarity, only the gates in the bottom level are shown in the main panel. The inset to Fig. 5.1(a) shows the completed device with top level gates. Conductances through the left and right sensor dots (LSD and RSD) were used to monitor the charge occupations in the left and right double dots. **b.** Schematic cross section through dashed line in Fig. 5.1(a) and diagram of a pair of double quantum dots formed under gates from D_1 to D_4. **c-d.** Charge stability diagrams of the left (**c**) and right (**d**) double dots, measured using conductance of LSD (g_{L}) and RSD (g_{R}), respectively. For clarity, a linear background was subtracted from the raw data and resultant conductance variations (Δg_{L} and Δg_{R}) are plotted.

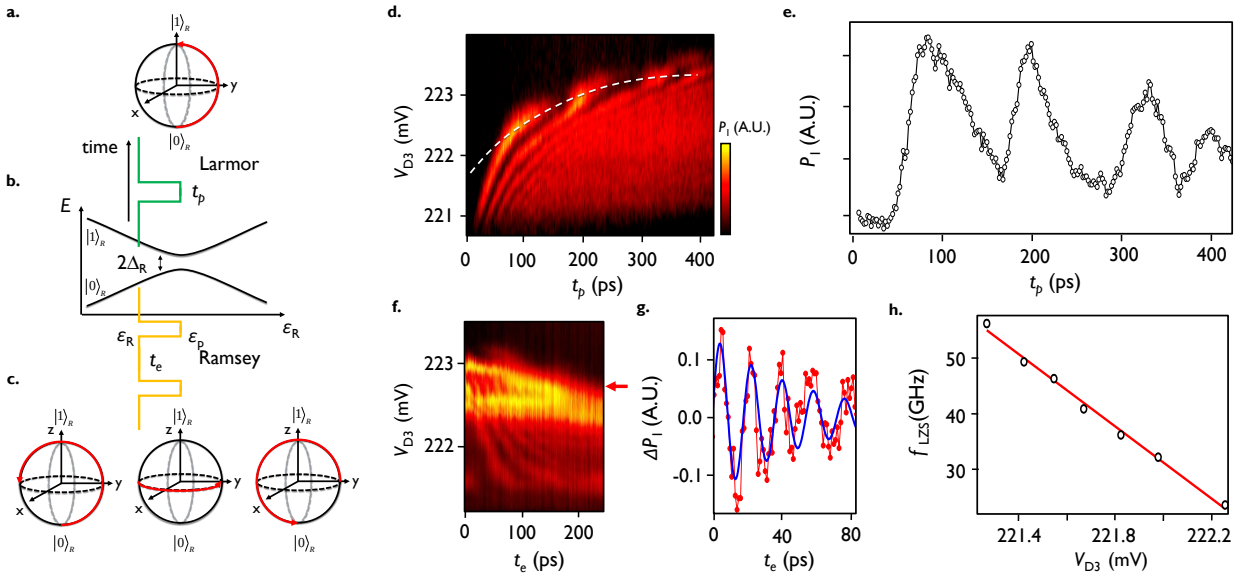

Figure 5.2: Demonstration of two-axis control of an undoped Si/SiGe charge qubit formed in the right double dot. **a.** Time evolution of the Bloch vector during a non-adiabatic DC-pulsed gate (Larmor oscillation). An abrupt change in the detuning ε_{R} from a negative value, where state $|0\rangle_{\mathrm{R}}$ is the eigenstate of the Hamiltonian, to ε_{P}=0 induces a rotation of the state around the X-axis of the Bloch sphere. **b.** Schematic energy level diagram of a double dot charge qubit with the pulse sequences for Larmor (X-axis rotation, green) and Ramsey (Z-axis rotation, orange) oscillation measurements. **c.** Schematic time evolution of Bloch vector during a Ramsey fringe measurement pulse sequence. A $X_{3\pi/2}$ pulse is applied to initialize the state on the XY plane of the Bloch sphere, and the state then evolves freely around the Z-axis for evolution time t_{e} with the rate $E_{01,\mathrm{R}}/h$ determined by the right qubit energy spliting $E_{01,\mathrm{R}} = \sqrt{{\varepsilon_{\mathrm{R}}}^2 + (2\Delta_{\mathrm{R}})^2}$. A second $X_{3\pi/2}$ pulse maps the Y-axis to the Z-axis, and the average charge occupation is measured via the conductance change of the RSD (see Fig. 5.1(a)) **d.** Coherent oscillation of uncalibrated probability P_1 in arbitrary units corresponding to Larmor oscillations (X-axis rotations) as a function of voltage on gate D_3, V_{D3} and pulse duration t_p of a single step pulse (see Fig. 5.2(a) - green pulse). **e.** Line cut along the contour shown as the white dashed line in **d.**, which corresponds to $\varepsilon_{\mathrm{R}} = 0$, showing coherent Larmor oscillations with coherence time about $T_2^* \approx 150$ ps. **f.** Demonstration of Z-axis control performed with a Ramsey fringe experiment (orange pulse in Fig. 5.2(b)). Uncalibrated P_1 as a function of V_{D3} and t_e. **g.** Line cut of the Ramsey fringe as a function of t_{e}. For clarity, a background probability variation of a third order polynomial in time was removed from the raw P_1, as shown in the Supplementary Fig. 5.7. The oscillations arise because of rotations of the Bloch vector about the Z-axis of the Bloch sphere. **h.** Landau-Zener-Stueckelburg (LZS) oscillation frequency f_{LZS} as a function of V_{D3} in the regime where the pulse tip detuning $\varepsilon_{\mathrm{p}} > \Delta_{\mathrm{R}}$. The red solid line shows a linear fit to $\Delta f_{\mathrm{LZS}} \approx \alpha_{\varepsilon_{\mathrm{R,D3}}} \Delta V_{\mathrm{D3}}$ with best fit parameter of gate D_3 lever arm $\alpha_{\varepsilon_{\mathrm{R,D3}}} \approx 32.5$ GHz/mV ≈ 135 μeV/mV.

5542-219). X-rotations on the Bloch sphere, shown in Fig. 5.2(a), correspond to oscillations between the qubit states $|0\rangle_{\rm R}$ and $|1\rangle_{\rm R}$. Changing the peak detuning ($\varepsilon_{\rm P}$) abruptly to $\varepsilon_{\rm P} = 0$, as shown by the green pulse in Fig. 5.2(b), yields in the ideal case an X-rotation on the Bloch sphere. At $\varepsilon = 0$ the Hamiltonian is $H = \Delta_{\rm R}\sigma_{\rm x}$, where $\Delta_{\rm R}$ is the tunnel coupling between D_3 and D_4, so the state evolves periodically in time at the Larmor frequency $2\Delta_{\rm R}/h$, where h is Planck's constant. In the experiment there is a finite rise time for the pulse at the sample, and the axis of rotation on the Bloch sphere will depend on the exact detuning value reached at each stage of the pulse, so that the schematic drawings in Figs. 5.2(a) and 5.2(c) are simpler than the case realized in the experiment. After a time evolution of duration $t_{\rm p}$, the final state is measured by abruptly changing the detuning back to negative $\varepsilon_{\rm R}$. We use the difference of the conductance of the RSD between $|0\rangle_{\rm R}$ and $|1\rangle_{\rm R}$ to determine a time averaged signal proportional to the probability P_1 of the state being in $|1\rangle_{\rm R}$ [51].

Figs. 5.2(d) and 5.2(e) show coherent oscillations of P_1 resulting from the non-adiabatic Larmor pulse sequences described above. In Fig. 5.2(d) we plot P_1 as a function of $t_{\rm p}$ and the gate voltage $V_{\rm D3}$, the latter of which determines the base level of $\varepsilon_{\rm R}$. In order to overcome a sampling time limitation of our AWG, we modified the pulse generation scheme to allow sub-picosecond timing resolution (see Supplementary Fig. 5.6). In Fig. 5.2(d), the path of the pulse maximum level detuning $\varepsilon_{\rm P} = 0$ is curved (see the white dashed curve following the maxima in Fig. 5.2(d), which is drawn by running a smooth curve through the oscillation peaks), most likely due to the finite rise time of the pulse and frequency-dependent attenuation in the microwave coaxial cable [81]. Fig. 5.2(e) shows a line cut through this path corresponding approximately to $\varepsilon_{\rm P} = 0$, revealing periodic oscillations in P_1 at a frequency of order 10 GHz, corresponding to $\Delta_{\rm R}/h \simeq 5$ GHz. We typically observe beating of the oscillations after $t_{\rm p} = 300$ ps. This likely arises because of the superposition of a reflected part of the pulse with the original pulse, modifying the detuning amplitude [51, 81].

The high frequency oscillations of P_1 in Fig. 5.2(d) for $V_{\rm D3} < 222$ meV arise from coherent Landau-Zener-Stückelberg (LZS) interference patterns [92, 93]. As $V_{\rm D3}$ becomes less positive in Fig. 5.2(d), the pulse maximum level detuning enters the regime $\varepsilon_{\rm P} > 0$, where the interdot tunnel

coupling acts as a beam splitter [52, 94]. Here, the splitting ratio between the upper and lower branches of the charge qubit dispersion is determined by the detuning ramp rate in comparison with the tunnel coupling. On the return edge of the pulse, the two different trajectories returning through the beamsplitter at $\varepsilon_{\mathrm{P}} = 0$ can coherently interfere.

The measurement of qubit state rotations about the Z-axis on the Bloch sphere, shown schematically in Fig. 5.2(c), can be performed using two $X_{3\pi/2}$ pulses. The qubit state is first prepared in the state $|-Y\rangle_{\mathrm{R}} = \sqrt{1/2}(|0\rangle_{\mathrm{R}} - i|1\rangle_{\mathrm{R}})$, by initializing to state $|0\rangle_{\mathrm{R}}$ and by performing an $X_{3\pi/2}$ rotation. The qubit state then acquires a relative phase $\varphi = e^{-it_{\mathrm{e}}\Delta E_{01,\mathrm{R}}/h}$, where t_{e} is the time spent between the two X rotations at the base value of the detuning and the qubit energy splitting $E_{01,\mathrm{R}} = \sqrt{{\varepsilon_{\mathrm{R}}}^2 + (2\Delta_{\mathrm{R}})^2}$. This phase evolution corresponds to a rotation of the qubit state around the Z-axis of the Bloch sphere. Figs. 5.2(f) and 5.2(g) show the resulting quantum oscillations of the qubit state around the Z-axis of the Bloch sphere. In Fig. 5.2(g), the line cut is taken at $V_{\mathrm{D3}} \sim 222.7$ mV in Fig. 5.2(f), corresponding to $\varepsilon_{\mathrm{P}} \approx 0$, and a smooth third order polynomial background oscillation was removed from the raw data for clarity [82, 84] (see also Supplementary Fig. 5.7). By fitting the data to an exponentially damped sinusoidal oscillation, we extract the Ramsey fringe oscillation frequency $f_{\mathrm{Ramsey}} \approx 56$ GHz and a coherence time $T_2^* \sim 51$ ps.

The gate voltage dependence of both the LZS interference and the Ramsey fringe frequencies provide accurate measures of the detuning lever arm. Fig. 5.2(h) shows the LZS oscillation frequency f_{LZS} as a function of V_{D3}. As these LZS oscillations are measured in the limit $\varepsilon_{\mathrm{P}} > \Delta_R$, we use an approximate form of the charge qubit energy level, $E_{01,\mathrm{R}} = \sqrt{\varepsilon_{\mathrm{R}}^2 + (2\Delta_{\mathrm{R}})^2} \approx \varepsilon_{\mathrm{R}} = hf_{\mathrm{LZS}}$, and fit the data to the form $\Delta f_{\mathrm{LZS}} = \alpha_{\varepsilon_{\mathrm{R,D3}}}\Delta V_{\mathrm{D3}}$ to determine the gate lever arm $\alpha_{\varepsilon_{\mathrm{R,D3}}}$ ≈32.5 GHz/mV≈135 μeV/mV.

We now discuss the measurement of the capacitive coupling between the double quantum dots. With the detuning lever arm calibrated as described above, the coupling strength can be measured by sweeping ε_{L} and ε_{R} through the LDD and RDD charge degeneracy points. Fig. 5.3 shows the LDD and RDD polarization lines, characterized by measuring the differential conductance of the left and right sensors, LSD (Fig. 5.3(a)) and RSD (Fig. 5.3(b)), as functions of the two critical variables, the detuning parameters for the LDD and RDD: ε_{L} and ε_{R}. We sweep ε_{L} and ε_{R} by

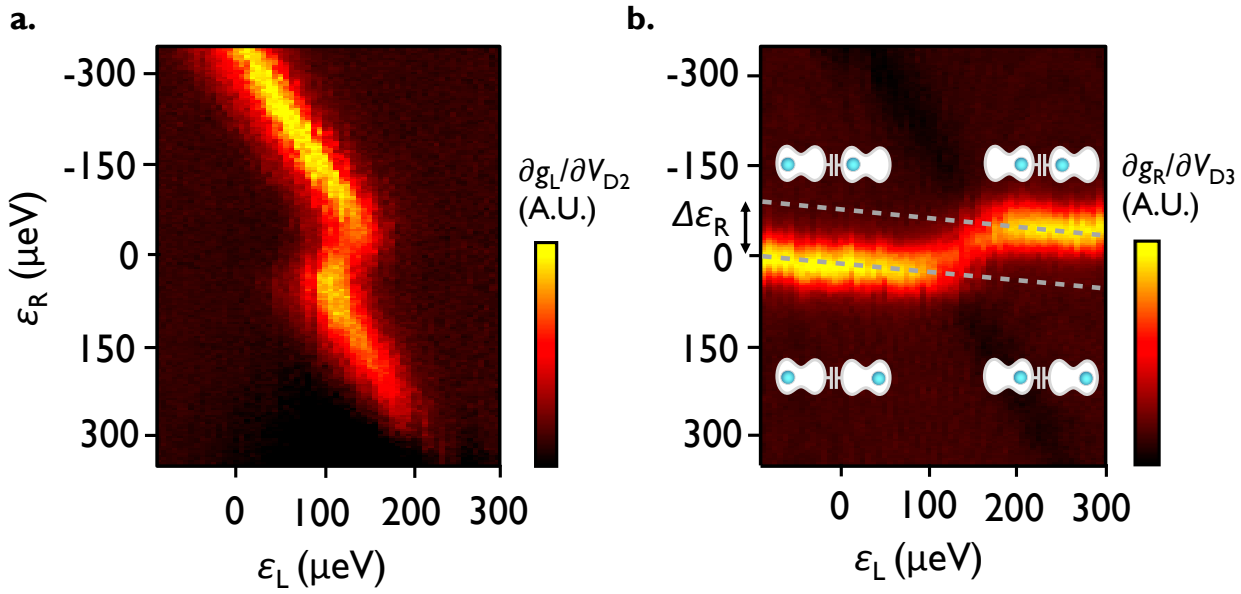

Figure 5.3: Measurement of capacitive coupling between two sets of double quantum dots. **a-b.** The left and right double dot polarization lines are characterized by measuring the LSD (**a**) and RSD (**b**) differential conductances as functions of the detunings ε_{L} and ε_{R}. A polarization line is identified by its large differential conductance. In **b**, a schematic diagram indicates the location of the excess charge in the capacitively coupled double quantum dots. The gray dashed lines represent the shift of RDD polarization line detuning ($\Delta\varepsilon_{\mathrm{R}} \approx 75$ μeV) due to one electron moving from the left dot to the right dot in the LDD.

controlling the voltages on (V_{D1}, V_{D2}) and (V_{D3}, V_{D4}), respectively. The positions of the excess charges (the electrons in each double dot that are free to move) are shown schematically as insets to Fig. 5.3(b). The coupled charge stability diagram reveals the four possible ground state charge configurations for an extra electron in each of the two double dots. The gray dashed lines in Fig. 5.3(b) show the RDD detuning energy shift ($\Delta\varepsilon_{\mathrm{R}}$) arising from the movement of a single electron from left to right in the LDD. The shift in this line is a direct measure of the energy shift in the RDD resulting from the capacitive coupling between the two double dots. From the energy calibrations reported above, we extract $\Delta\varepsilon_{\mathrm{R}} \approx 75$ μeV ≈ 18.3 GHz. This energy shift is the available detuning modulation for the performance of two-qubit gates in quantum dots of a size and separation similar to those studied here.

We now show that the capacitive coupling demonstrated above enables fast charge-state-

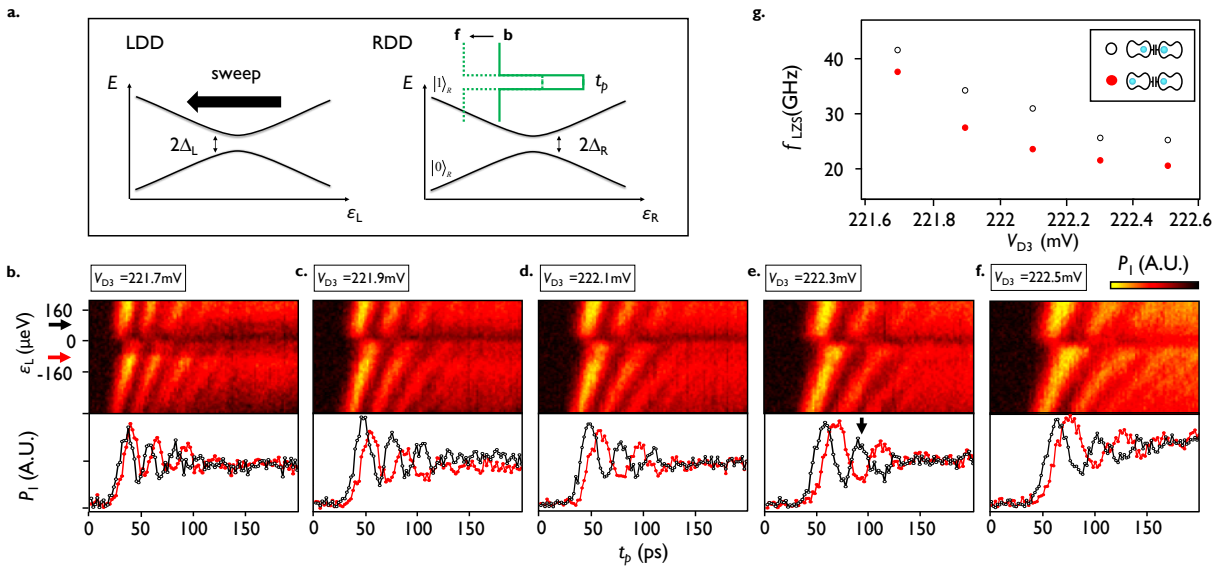

Figure 5.4: Charge state conditional coherent quantum interference. **a.** Schematic diagram of the pulse sequences used for the measurement of Landau-Zener-Stuckelberg (LZS) quantum interference in the right double dot (RDD) as a function of the detuning of the left double dot (LDD). **b-f.** Coherent LZS oscillations of uncalibrated P_1 as a function of the LDD detuning ε_L and pulse duration t_p with fixed base level of $V_{D3} = 221.7$ (**b**), 221.9 (**c**), 222.1 (**d**), 222.3 (**e**), and 222.5 mV (**f**). **g.** LZS interference frequencies, f_{LZS}, with $(0,1)_L$ - (black) and $(1,0)_L$ - (red) excess charge ground state of the LDD as functions of V_{D3}. The black arrow in **e** highlights the shift in the location of the peak in the probability that corresponds to a conditional π phase rotation achieved in ∼80 ps.

conditional phase evolution of a quantum dot charge qubit. We study LZS oscillations in the RDD in the presence of a slowly varying perturbation from the excess charge in the LDD. Fig. 5.4(a) illustrates schematically in green the pulse applied to the RDD for this experiment. The pulse is applied at a series of different values of ε_L (the vertical axis in Figs. 5.4(b)-(f)). The pulse minimum detuning is controlled using V_{D3}, and the pulse amplitude is held fixed at 210 μeV. In Figs. 5.4(b) to 5.4(f), we vary V_{D3} from 221.7 to 222.5 in steps of 0.2 mV. The effect of these steps is to change the energy in detuning of the maximum of the fast pulse, thus changing the frequency of the LZS oscillations. For example, the oscillations in Fig. 5.4(a) are much faster than those visible in Fig. 5.4(f). The physical origin of this variation is the energy difference between the two charge qubit states: in Fig. 5.4(a), the maximum of the pulse sits at large detunings, corresponding to a large energy difference between the states. In contrast, in Fig. 5.4(f), the pulse maximum sits at

detunings much closer to the charge qubit anticrossing, so that the energy difference between the charge qubit states is significantly smaller.

For each of these LZS oscillation measurements, $\varepsilon_{\rm L}$ is slowly swept from +180 to -320 μeV (see the vertical axis in the top panels of Figs. 5.4(b)-(f)). This variation in $\varepsilon_{\rm L}$ has two effects. First, the cross-talk between $\varepsilon_{\rm L}$ and the RDD results in a continuous shift in the detuning of the RDD, causing the LZS oscillations be tilted in each of the top panels of Fig. 5.4(b)-(f). Second (and this is the main result of Fig. 5.4), at $\varepsilon_{\rm L} = 0$, the excess charge occupation of the LDD changes abruptly from $(0,1)_{\rm L}$ to $(1,0)_{\rm L}$ — this change occurs quite abruptly at zero detuning of the LDD, as can be observed in Figs. 5.4(b)-(f). This change in the charge configuration of the LDD produces a sudden decrease in frequency in Figs. 5.4(b) to 5.4(f) at $\varepsilon_{\rm L} = 0$. This decrease in frequency reflects the decreased $\varepsilon_{\rm P}$ that the LZS pulse maximum detuning reaches, because of the effective change in the pulse minimum detuning energy.

The bottom panels of Figs. 5.4(b) to 5.4(f) show line cuts of the LZS oscillations in the RDD for the $(0,1)_{\rm L}$ LDD ground state (black arrow on the left in Fig. 5.4(b)) and $(1,0)_{\rm L}$ LDD ground state (red arrow on the left in Fig. 5.4(b)). At any given evolution time t_p, a phase change is clearly visible, and this phase change arises from the shift of one electron in the LDD. Using this effect, a charge-state-conditional π phase flip can be achieved in a time $t_{\rm p}$ as short as 80 ps, as indicated by the black arrow in Fig. 5.4(e).

Fig. 5.4(g) shows the difference in $f_{\rm LZS}$ between the cases when the LDD ground state is $(0,1)$ (black circles) and when this ground state is $(1,0)$ (red circles). The frequency differences vary from 7 to 10 GHz, and this plot can be used to infer the speed of a conditional phase (CPHASE) gate if full control over qubits in both the left and right double dots in a device like that shown here is realized in the future. We emphasize that the frequency changes observed here arise from competing effects: $f_{\rm LZS}$ of the RDD increases as we change a gate voltage to increase $\varepsilon_{\rm L}$, whereas $f_{\rm LZS}$ decreases as we cross zero detuning in the LDD, resulting in the motion of a single electron charge. Since we take line cuts at $\varepsilon_{\rm L} \approx \pm 80$ μeV to clearly show LZS oscillations in the $(0,1)_{\rm L}$ and $(1,0)_{\rm L}$ ground states, we believe that using a LDD detuning pulse amplitude $< 160\mu$eV, when LDD coherent manipulation is realized, can lead to a faster conditional phase gate than that estimated

here.

5.3 Discussion

Here we have demonstrated a strong capacitive coupling of ≈18 GHz between two double quantum dots in a linear quad dot array geometry, and this coupling enabled the observation of fast charge-state-conditional coherent oscillations with a conditional phase flip time of 80 ps. Coupling of this magnitude demonstrates a key physical interaction necessary for a two-qubit CPHASE gate. Moreover, because we measure single qubit X (Larmor) and Z (Ramsey) rotations with rotation frequencies also on the order of 10 GHz, one can envision universal quantum logic gates in semiconductor charge qubits that are all fast. Although we use abrupt changes in the baseline detuning here, resonant microwave control is also plausible [85], in which case a two-qubit controlled not gate (CNOT) could be implemented in analogy with Refs. [77]. We stress, however, that the full demonstration of two-qubit charge qubit gates remains as a challenge, as in this work coherent control of the LDD could not be achieved. A more compact gate geometry that enables greater tunability in the tunnel coupling, which could potentially be achieved using an overlapped Al/Al_2O_3 gate structure [13, 53], is a promising path towards achieving fully tunable tunnel couplings in both neighboring double quantum dots. Finally, we note that the strong capacitive coupling observed here is also a valuable resource with the potential to enable two-qubit gates in multi-electron spin qubits, including singlet-triplet [41, 47] and hybrid quantum dot qubits [51, 72, 95–97].

5.4 Materials and methods

Fabrication: The device heterostructure was grown using chemical vapor deposition (CVD) on commercially available SiGe substrates with a 29% Ge composition. The CVD growth sequence from the starting substrate was deposition of a strain-matched SiGe buffer layer followed by deposition of a 12 nm thick strained Si well. The well was capped by deposition of 50 nm of SiGe, followed by a few nanometers of sacrificial strained Si to cap the heterostructure.

Devices were fabricated using a combination of electron beam lithography (EBL) and pho-

tolithography. The device nanostructure was fabricated in two layers starting on a 15 nm gate dielectric of Al_2O_3 deposited by atomic layer deposition (ALD). The first layer of control gates was patterned in two EBL/metallization steps to improve the gate density, and the metal layers were Ti followed by Au. The second reservoir gate layer (see inset to Fig. 5.1(a)) is isolated from the first with another 80 nm layer of Al_2O_3 grown via ALD. The second gate layer was also metallized with Ti/Au. A third layer of Al_2O_3 was deposited over the second gate layer to protect the gates during subsequent fabrication steps. Ohmic contacts were fabricated using annealed P+ ion implants.

Measurement: The charge stability diagrams of the LDD and RDD are characterized by measuring the conductance changes through the left and right sensor dots (LSD and RSD, respectively, see Fig. 5.1(a)), which are operated at a fixed voltage bias of 50 μV, and the currents are measured with two current preamplifiers (DL Instruments model 1211). Supplementary Fig. 5.5 shows large scale charge stability diagrams and the positions of charge transitions of the LDD and RDD in the electron occupation regime used in the present experiment. For the manipulation of the RDD charge qubit, fast voltage pulses with repetition rate of 25 MHz are generated using two outputs of a Tektronix AWG70002A arbitrary waveform generator which are added to the dot-defining dc voltage through a bias tee (Picosecond Pulselabs 5546-107) before being applied to gate D_3. The conductance change through the right sensor dot (RSD) with and without the manipulation pulses, measured with a lock-in amplifier (EG&G model 7265), is used to determine the average charge occupation. For the measurement of changes in charge occupation probabilities resulting from fast manipulation pulses, we modulated the manipulation pulses with a low frequency ($\approx$777 Hz) square wave envelope, similar to the technique used in previous studies [85, 95]. We compare the measured signal level with the corresponding $|0\rangle_{\mathrm{R}}$ to $|1\rangle_{\mathrm{R}}$ charge transition signal level, calibrated by sweeping gate D_3 and applying a 777 Hz square pulse to gate D_3 with an amplitude the same as the manipulation pulses.

5.5 Acknowledgements

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5.6 Contributions

DRW fabricated the quantum dot device and developed the hardware and software for the measurements. DK performed electrical measurements with RHF and analyzed the data with MAE, MF, and SNC. DES and MGL prepared the Si/SiGe heterostructure. All authors contributed to the preparation of the manuscript.

5.7 Competing interests

The authors DRW, MAE, MF, and SNC are co-investors on a patent application related to some of the nanostructure designs described in this work. The remaining authors declare no conflict of interest.

5.8 Supplementary materials

Charge stability measurements

For measuring changes in charge occupation and charge qubit probabilities, we use two single electron transistors formed on the left and right hand sides of the linear quadruple dot array

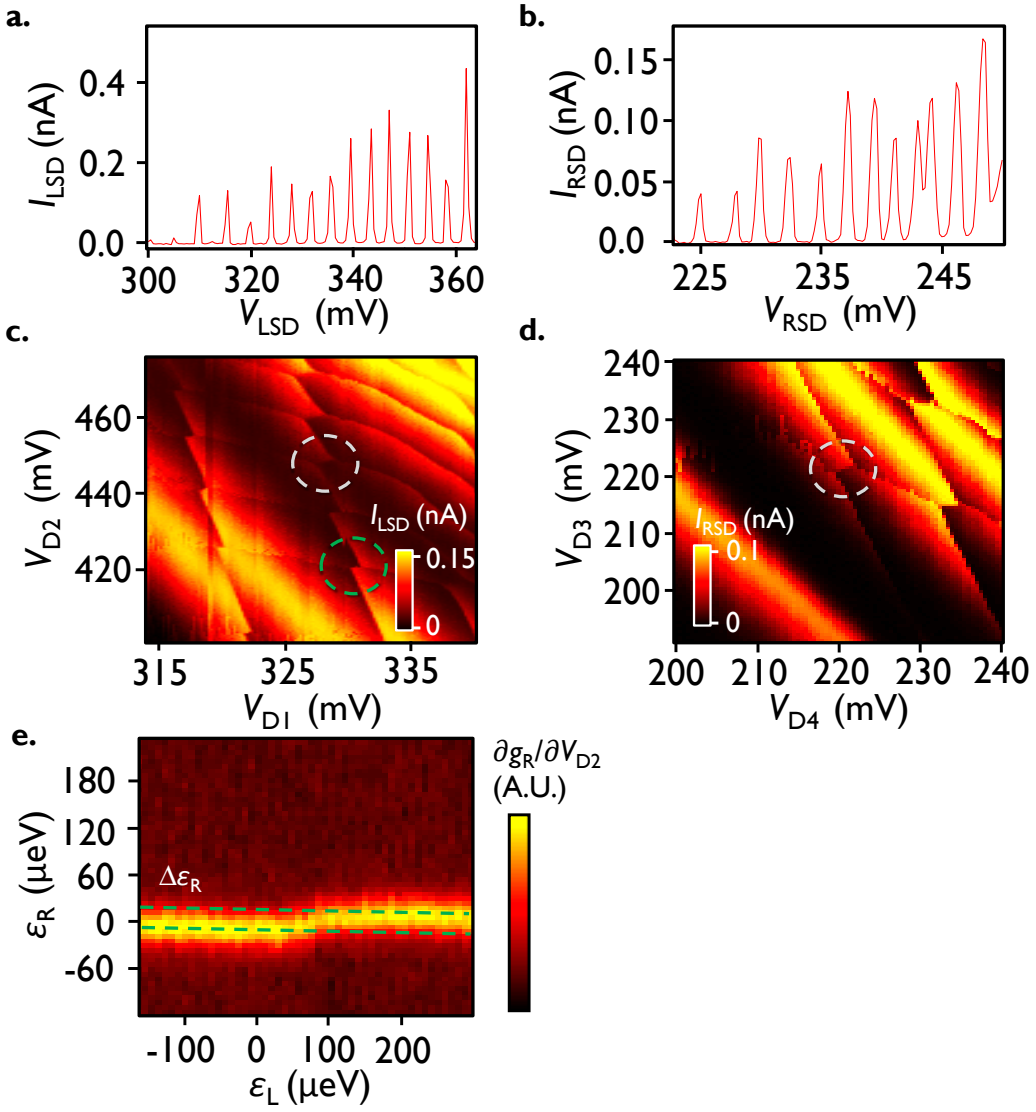

Figure 5.5: Measurement of charge stability diagrams of two pairs of double quantum dots. **a-b**, Coulomb peaks obtained by measuring I_{LSD} and I_{RSD}, the current through the single electron transistors formed by the left sensor dot (LSD) (**a**) and right sensor dot (RSD) (**b**) as a function of the appropriate gate voltage. **c-d**, Large scale stability diagrams of the left double dot (LDD) (**c**) and the right double dot (RDD) (**d**) measured by recording the conductance change of LSD and RSD, respectively, as a function of the relevant gate voltages. The white dashed circles show the charge configuration regions used for the current experiments. **e**, inter double dot capacitive coupling measurement with two fewer electrons in dot 2, corresponding to the charge configuration marked with the green dashed circle in **c**. The capacitive coupling in this case corresponds to a detuning shift of $\Delta\varepsilon_{\mathrm{R}} \approx 25\mu eV$, compared to 75 μeV at the position of the white dashed circle, shows that the coupling strength depends on dot occupation number and the gate voltages used to achieve those occupations.

(see Fig. 5.1(a), LSD and RSD, in the main text). Supplementary Figs. 5.5(a) and 5.5(b) show Coulomb blockade peaks of the charge sensors. By adjusting V_{LSD} and V_{RSD} to be near maxima of the current through LSD and RSD, the charge occupations in the D_1 and D_2 (D_3 and D_4) double dot can be measured using I_{LSD} (I_{RSD}). Supplementary Figs. 5.5(c) and 5.5(d) show the large scale charge stability diagrams of the left double dot (LDD, Fig. 5.5(c)) and right double dot (RDD, Fig. 5.5(d)), respectively. We find that both the tunnel coupling strength and the inter-double dot capacitive coupling are reduced as electrons are removed from the LDD. For example, we measure an inter-double dot capacitive coupling energy with two fewer electrons in dot 2 (at the position of the dashed green circle in Supplementary Fig. 5.5(c)). As shown in Supplementary Fig. 5.5(e), we measure a significantly decreased capacitive coupling of $\Delta\varepsilon_{\mathrm{R}} \approx 25\mu eV$, which can be compared to the 75 μeV value reported in the main text for the case with two more electrons in the dot. This general trend can also be inferred from inspection of the polarization lines in Supplementary Fig. 5.5(c). However, the tunnel coupling of the RDD can be maintained $>$ 10 GHz down to the few electron regime. For these experiments, we tune the LDD electron occupation number to be in the regime $>$ (10, 10). The regions of the charge stability diagrams used for the pulse experiments are denoted as white dashed circles in the Supplementary Figs. 5.5(c) and 5.5(d).

Pulse generation and probability measurement details

Manipulation pulse sequences are generated using a Tektronix AWG70002A arbitrary waveform generator (AWG). The minimum sampling time of 40 ps typically results in timing resolution that is not adequate to measure >10 GHz oscillations. To improve the timing resolution, we use both output channels of the AWG, as shown in Fig. 5.6. In this approach, channel one outputs a 10 ns duration pulse and channel two outputs an opposite polarity pulse delayed by the desired pulse width t_{p}, which is controlled by an analog skew control with timing resolution better than 1 ps. As the channel output is delayed, a short pulse with opposite polarity appears at about 10 ns, because of imperfect cancellation at the trailing pulse edge. Since this opposite pulse is in the measurement phase, it does not induce charge transitions. In order to keep the duration of this unwanted mismatch as short as possible, we adjust the total pulse duration of the channel to be

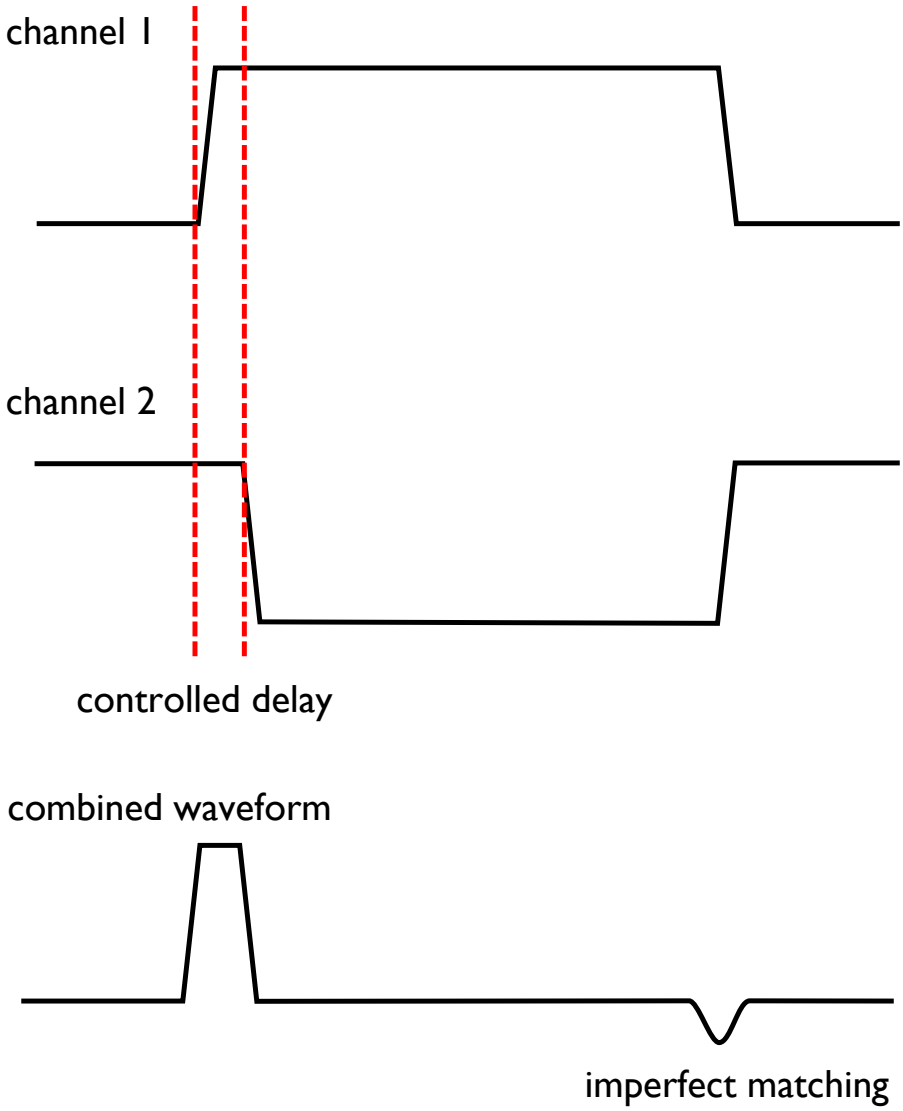

Figure 5.6: Pulse generation scheme. To overcome limitations in the sampling time of the pulse generator, very short pulses were obtained by generating a detuning pulse with duration of 10 ns using the first channel of the waveform generator, while a second pulse, delayed by t_{p} with opposite sign and duration 10 ns $- t_{\mathrm{p}}$ (rounded to nearest multiple of 40 ps), was generated using the second channel. The pulse width of the combined waveform is controlled by an analog delay of the second output channel, which has a timing resolution better than 1 ps. This cancellation procedure causes a small error and the end of the pulse, but the unwanted detuning variation at the falling edge of the pulse can be minimized modulo the sampling time of the waveform generator (40 ps, in this case).

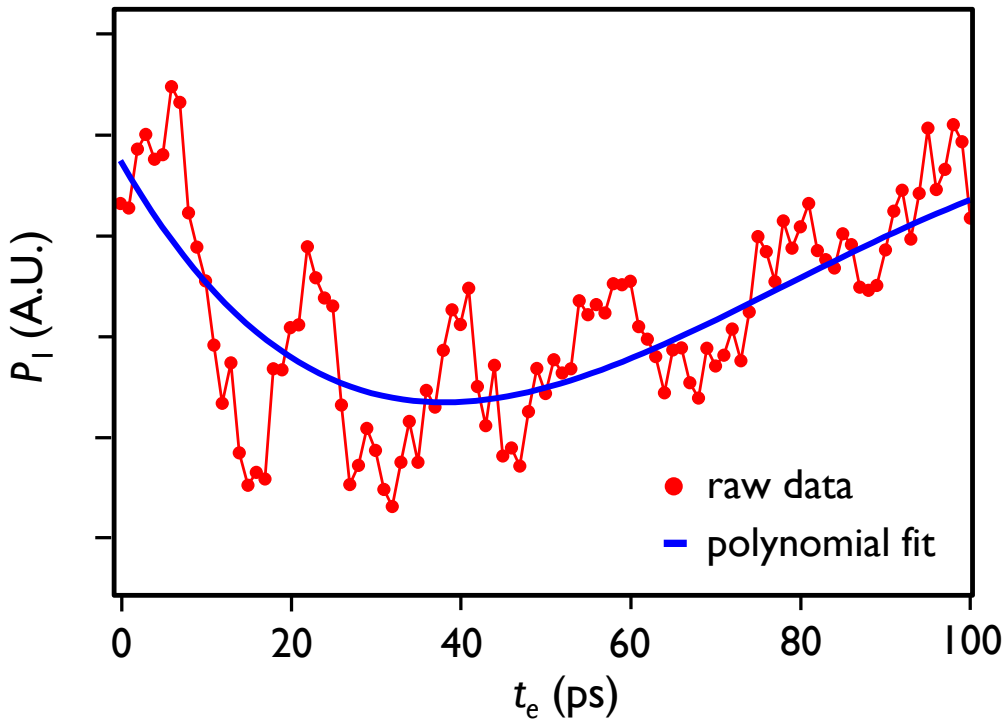

Figure 5.7: Background subtraction for the Ramsey fringe data. The red data points show coherent P_1 oscillations as a function of the free evolution time t_e. The blue solid curve shows a fit to the raw data using a third order polynomial. This smooth background variation is subtracted from the raw data shown in Fig. 5.2(g).

10 ns $- t_p$ rounded to nearest multiple of 40 ps.

In order to measure the charge qubit state probability, we adopt the general scheme described in previous work, where the difference was measured between a charge sensor's conductance with and without the manipulation pulses [51,85]. The data are acquired using a lock-in amplifier with a reference signal corresponding to the presence and absence of the pulses (lock-in frequency $\approx$ 777 Hz). The data are reported in arbitrary units, because the charge qubit relaxation time was not stable enough on long time scales to enable an absolute calibration.

Background removal in the Ramsey fringe data

Supplementary Fig. 5.7 shows the raw P_1 oscillation data corresponding to a Ramsey fringe measurement using two $X_{3\pi/2}$ pulses. The data typically show a smooth background variation in the

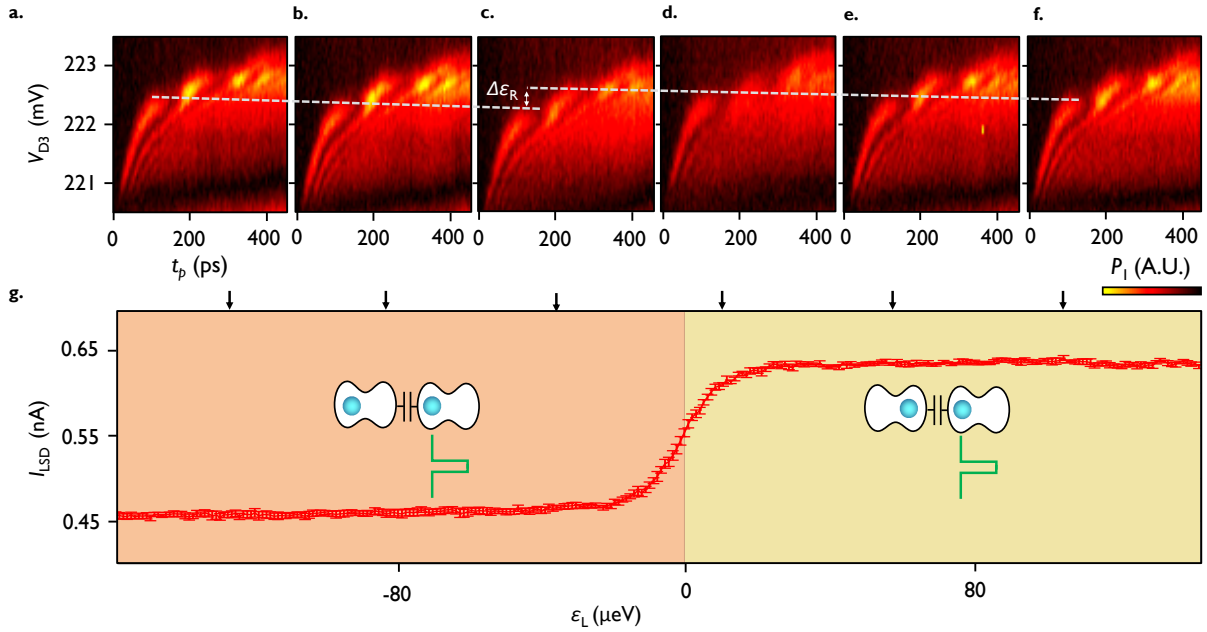

Figure 5.8: Variation of right double dot Larmor oscillation patterns as a function of the left double dot detuning. **a-f**, P_1 as a function of V_{D3} and pulse tip duration t_p for LDD detuning energy ε_L fixed near -100 (**a**) to +100 μeV (**f**). As ε_L is changed, the overall Larmor oscillation pattern shifts gradually due to the mutual capacitance between gates. However, the Larmor oscillation frequency is roughly constant from **a** to **f**. The effect of the LDD charge transition is evident by comparing **c** and **d**, where strong capacitive coupling results in a sudden shift of the pattern in the opposite direction (see $\Delta\varepsilon_R$ in Supplementary Fig. 5.8(c)). **g**, I_{LSD} as a function of LDD energy detuning ε_L showing the charge transition near ε_L=0. Black arrows on top show the values of ε_L where the RDD Larmor oscillation experiments in **a** to **f** are performed.

measured probability. This background is likely due to frequency dependent attenuation and inexact calibration of the state initialization and measurement pulse durations limited by sampling time of the AWG. When we analyze the data to extract the inhomogeneous coherence time T_2^*, we fit the background to a third order polynomial (blue solid curve in Supplementary Fig. 5.7) and subtract this polynomial from the raw data. The resultant high frequency oscillations are shown in Fig. 5.2(g) in the main text.

Charge state dependent Larmor oscillations

In the main text, we showed a coherent interference pattern with fixed RDD energy detuning ε_R as the LDD energy detuning ε_L is swept. Here we show the interference pattern as a function of ε_R

with ε_{L} fixed. Supplementary Figs. 5.8(a)-(f) show RDD Larmor oscillation patterns as a function of V_{D3} and the pulse duration t_p as the LDD detuning energy ε_{L} is varied from -100 (**a**) to +100 μeV (**f**). As ε_{L} is changed, the overall coherent oscillation pattern shifts because of capacitive cross talk. However, we find that the Larmor oscillation frequency of about 10 GHz is roughly constant from **a** to **f**. The effect of the LDD charge transition is evident when **c** and **d** are compared, where the strong capacitive coupling results in a sudden shift of the pattern in the opposite direction (see $\Delta\varepsilon_{\mathrm{R}}$ in Supplementary Fig. 5.8(c)). This explanation is supported by measurements of I_{LSD} (**g**) as a function of ε_{L}, showing that the charge transition indeed occurs in the LDD somewhere between panels **c** and **d**, providing evidence that the change in interference pattern frequency measured in the main text arises from a single electron transition.

Chapter 6

Micromagnets for spin qubits

6.1 Motivation

Utilizing the spin-degree of freedom of an electron hosted in silicon as a qubit is an attractive approach to building a quantum computer. Long coherence times and the possibility of dense device configurations (say compared to double-dot qubits) compatible with industrial fabrication procedures show promise for future implementations with larger numbers of spins. [17, 98, 99] Initialization and manipulation of electron spins is controlled through electron spin resonance (ESR) which requires both a static and varying magnetic field. Generating an AC magnetic field local to a quantum dot can be quite challenging, and it's coupling to the electron spin can be highly dependent on implementation.

One solution to this challenge is through the use of integrated micromagnets. By placing a micromagnet on a device local to the quantum dot, the slanting magnetic field generated by the micromagnet can be used for electrically driven ESR. [100] Applying an AC voltage to the gate which confines the electron within the quantum dot oscillates that electron through the out-of-plane component of the magnetic field gradient of the micromagnet, generating an effective AC magnetic field. The in-plane component of the micromagnet coupled with an applied external magnetic field sets the Zeeman splitting for the electron, allowing for addressability of multiple spins.

This chapter will discuss the fabrication and room temperature characterization of two types

of micromagnet designs introduced in the literature: the Wisconsin-Delft style micromagnet [17], and the Yoneda style micromagnet [101]. First the fabrication procedure is outlined. Next, characterization of deposited magnetic films using a vibrating-sample magnetometer is explained and corresponding measurements are presented. Finally, magnetic force microscopy is explained and corresponding measurements are presented revealing images of the stray fields generated by the two micromagnet designs in the absence of an applied external magnetic field.

6.2 Creating a micromagnet

There are many choices of magnetic material that can be used when fabricating a micromagnet, including the three naturally occurring magnetic elements: iron, nickel, and cobalt. For our work and in the work previously cited, cobalt is the element of choice. This is because of it's large saturated magnetization and it's relative ease of processing, especially via e-beam evaporation (PVD). For a more detailed explanation of magnetism in general, see Ref. [102].

Micromagnets are fabricated using the same e-beam lithography techniques described in chapter 2. Where the recipe diverges however is during the evaporation. Samples are loaded onto a homemade magnetic sample mount. Two large NdFeB magnets (surface field of $\sim$ 0.5T) are mounted on opposite sides of a channel with integrated clips. The magnets are oriented such that the "North" pole of one magnet faces the "South" pole of the opposite magnet across the channel. The micromagnet sample to be evaporated is then clipped into the channel such that it is centered between the two magnets and that the external magnetic field provided from the sample mount is parallel to the direction the magnetic field will take during the experiment.

Cobalt is then deposited onto the sample by e-beam evaporation. Evaporating a magnetic source in this way however must proceed slowly. An electron beam evaporator works by accelerating electrons expelled from a filament through a large potential (1-10 kV) and then directing them towards a source with a magnetic field via the Lorentz force. When evaporating a magnetic material such as cobalt however, this very same force proves a detriment as the beam is deflected at the source. This makes melting and evaporating cobalt very challenging. The beam position and power must be varied slowly as the local magnetic field at the source is a dynamic function of the condition

of the source.

Layout and design of a micromagnet optimized for electrically driven ESR in silicon quantum dot devices is discussed extensively in [101] and will not be reproduced here. Briefly however, there are two quantities of interest that we wish to optimize: the slanting (out-of-plane) magnetic gradient b_{sl} and the difference in the Zeeman energy between adjacent quantum dots ΔB_z. b_{sl} is generated by placing two rectangular slabs of cobalt across from each other (along the applied field axis) with a fixed gap width between them. ΔB_z arises from a "bridge" placed on one side of the gap: the magnetic field gradient generated by the "bridge" summed with the applied static magnetic field produces a different Zeeman splitting for each quantum dot. An example of a Yoneda style micromagnet can be seen in Fig. 6.1. For comparison, a Wisconsin-Delft style micromagnet can be seen in Fig. 6.2. It uses the same principles as the Yoneda style micromagnet to generate b_{sl} and ΔB_z except with three micromagnets instead of one. In this case, the "bridge" must be separated from the other magnets to avoid electrically shorting device gates.

6.3 VSM and MFM measurements of fabricated magnets

VSM characterization of bulk cobalt films

Many important bulk properties of ferromagnetic materials can be examined by measuring their characteristic hysteresis loop. A hysteresis loop is a plot of the magnetization M as a function of the applied magnetic field H. Some important properties of interest that can be extracted from a hysteresis loop are the saturated magnetization, remanence, and coercivity. The saturated magnetization M_0 is the maximum value of the magnetization that the sample can achieve (i.e. when $M = M_0$, increasing H further produces no change in magnetization). Remanence is a measure of the magnetic inductance B_r or magnetization M_r in a ferromagnetic material at $H = 0$ *after* magnetization. The coercive field H_c is the reverse magnetic field that needs to be applied to reduce the magnetic inductance or magnetization inside a magnetic sample to zero. These properties are of particular interest for a micromagnet near a quantum dot device as they correspond to the tunability of the magnetic field gradient present at a quantum dot due to the magnetization

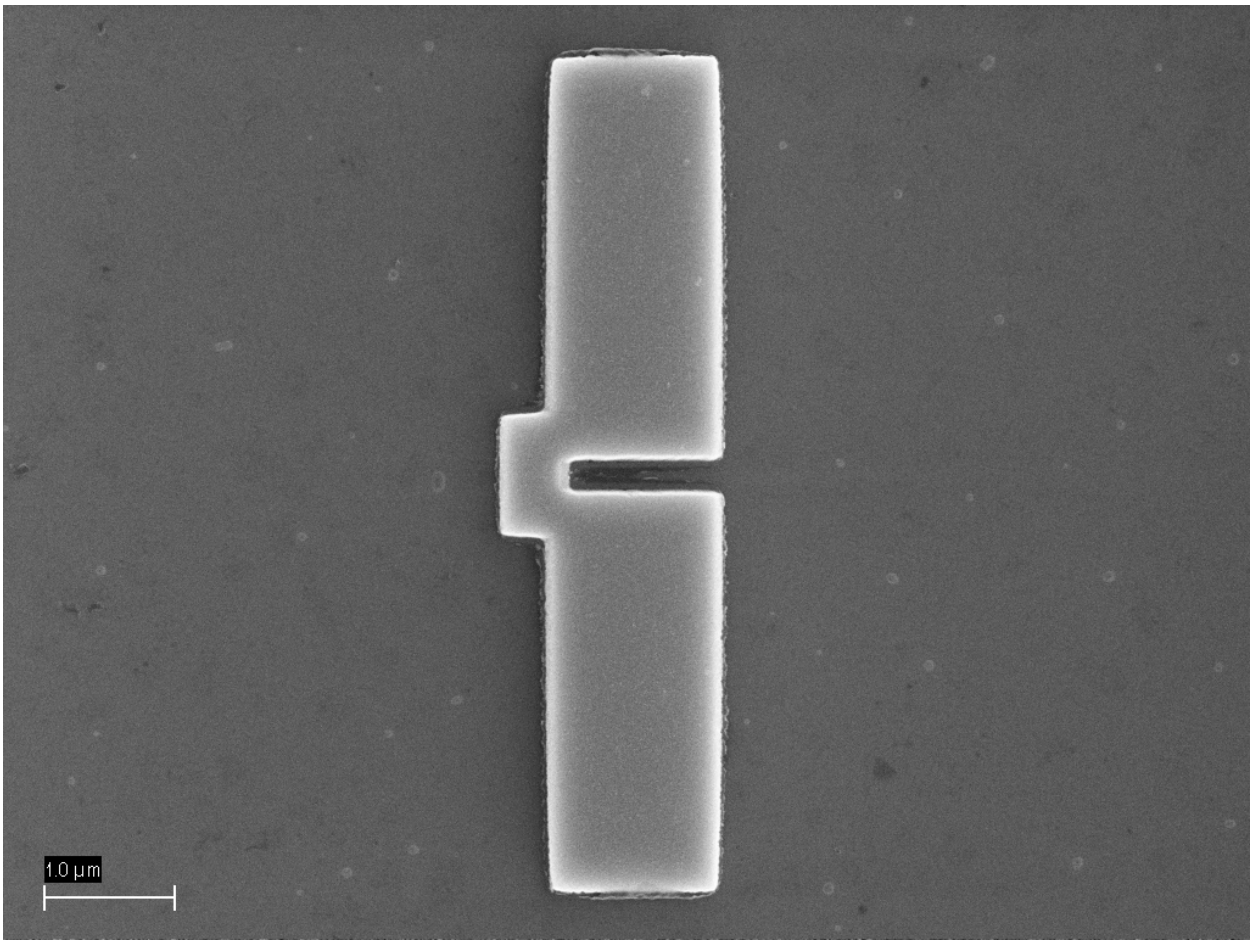

Figure 6.1: Electron micrograph of a fabricated Yoneda style micromagnet. [101] The micromagnet is composed of 5nm of evaporated titanium and 150nm of evaporated cobalt.

of the micromagnet, as a function of the applied external magnetic field.

In order to obtain a hysteresis loop for our evaporated cobalt samples, we make use of a Vibrating Sample Magnetometer (VSM). First described in 1959, [103] a VSM measures the magnetic moment m of a magnetic sample as a function of the applied magnetic field. The magnetic moment of a sample is related to its magnetization by its volume V as $m = MV$. A VSM works as follows: a magnetic sample to be measured is suspended by a non-magnetic rod between the poles of an electromagnet as shown in Fig. 6.3. The sample must be smaller than the poles of the electromagnet such that it experiences a uniform magnetic field. Mounted on the poles of the electromagnet are a set of RF-pickup coils. To perform a measurement, the sample is vibrated at a fixed frequency (84

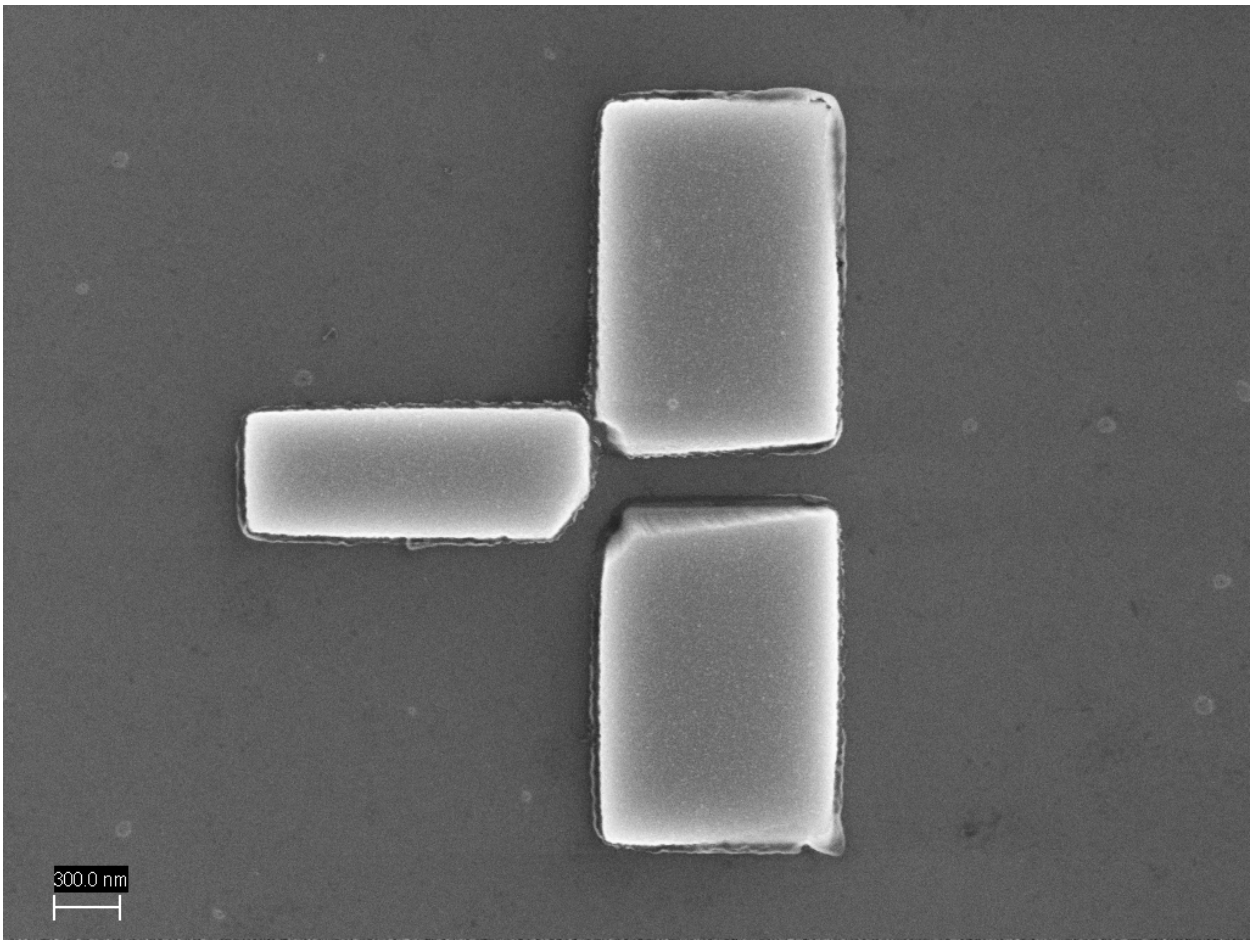

Figure 6.2: Electron micrograph of a fabricated Wisconsin-Delft style micromagnet. [17] The micromagnet is composed of 5nm of evaporated titanium and 150nm of evaporated cobalt.

Hz in our case) perpendicular to the direction of the applied magnetic field H_{app}. From Faraday's law of induction, the voltage induced in the RF-pickup coils V_{ind} is proportional to the change in magnetic flux Φ through the coils as,

$$V_{ind} = -N\frac{d\Phi}{dt}, \tag{6.1}$$

where N is the number of loops in the coil. As Φ is proportional to M which is proportional to m and if H_{app} is varied slowly, a lock-in measurement of the voltage through the coils at the sample vibration frequency will yield a hysteresis loop.

Unfortunately, we cannot use the VSM to measure the hysteresis loop for an individual micromagnet. While powerful, the VSM is only sensitive to magnetic moments as small as 10^{-5} –

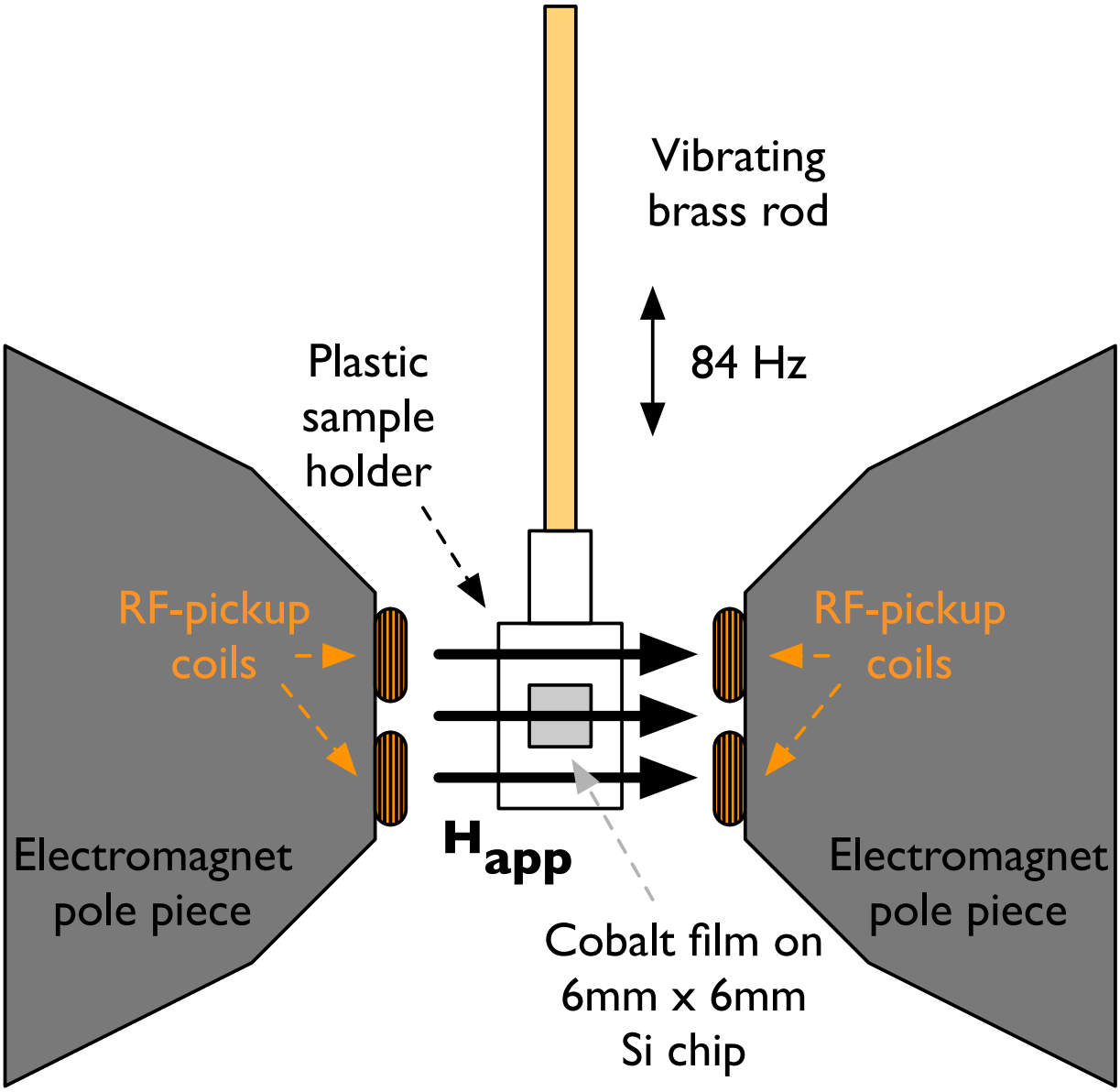

Figure 6.3: Schematic cartoon of a vibrating sample magnetometer (VSM). The bulk cobalt film sample to be characterized is vibrated between the poles of an electromagnet while the applied field H_{app} is slowly changed. By measuring the change in the induced voltage in the RF-pickup coils, a hysteresis loop can be generated showing the the magnetic moment m of the film as a function of H_{app}.

$10^{-6}emu$ ($10^{-8} - 10^{-9}A \cdot m^2$). [103] For a 150nm thick cobalt film and a given saturated magnetization $M_0 = 1.42 \times 10^3 emu/cm^3$, [102] the minimum area of cobalt needed to obtain a signal is $\sim 0.025mm^2$. Therefore, we include a witness chip ($\sim 36mm^2$) with our micromagnet samples during cobalt evaporations in order to obtain some characterization of the film deposited. The actual properties of the micromagnet in an applied magnetic field, especially M_r and H_c, are expected to be different from that of the bulk film due to the small size and shape anisotropy.

Figure 6.4 shows the results for a VSM measurement of an evaporated film of 5nm titanium (for adhesion) and 150nm cobalt on a ∼6mm × ∼6mm Si chip. Marked on the plot are the points which represent the saturated magnetic moment (m_o), coercive field ($H_c = 270$ Gauss), and remanant magnetic moment ($m_r \approx 0.75m_0$). For comparison, Fig. 6.5 shows the results for a VSM measurement of an evaporated film of 30nm of cobalt on a ∼6mm × ∼6mm Si chip. As with the previous, m_0, H_c, and m_r are marked on the hysteresis loop.

MFM characterization of micromagnets

While the VSM can reveal many important bulk properties of our cobalt films, as discussed in the previous section, it is not sensitive enough to characterize an individual micromagnet. Instead, we use a different technique to gain insight into the magnetic properties of our micromagnets: Magnetic force microscopy (MFM). MFM is a modification of a standard atomic force microscopy (AFM) experiment. In AFM, a small cantilever with an extremely sharp tip is vibrated near resonance over the surface of a sample of interest. The tip is brought close to the surface and then rastered in the x-y plane. A laser is then reflected off the back of the cantilever onto a photodetector. As the AFM tip is moved across the sample, interactions between the tip and the surface will change the response of the cantilever to the drive which will be observed by a change in signal on the photodetector. By monitoring these changes in the cantilever motion due to surface interactions, the AFM is capable of sub-nanometer resolution measurements (e.g. surface roughness or z-heights thin metal gates on a quantum dot device).

Considering the dynamics of our AFM measurement in more detail, the resonant frequency ω_0

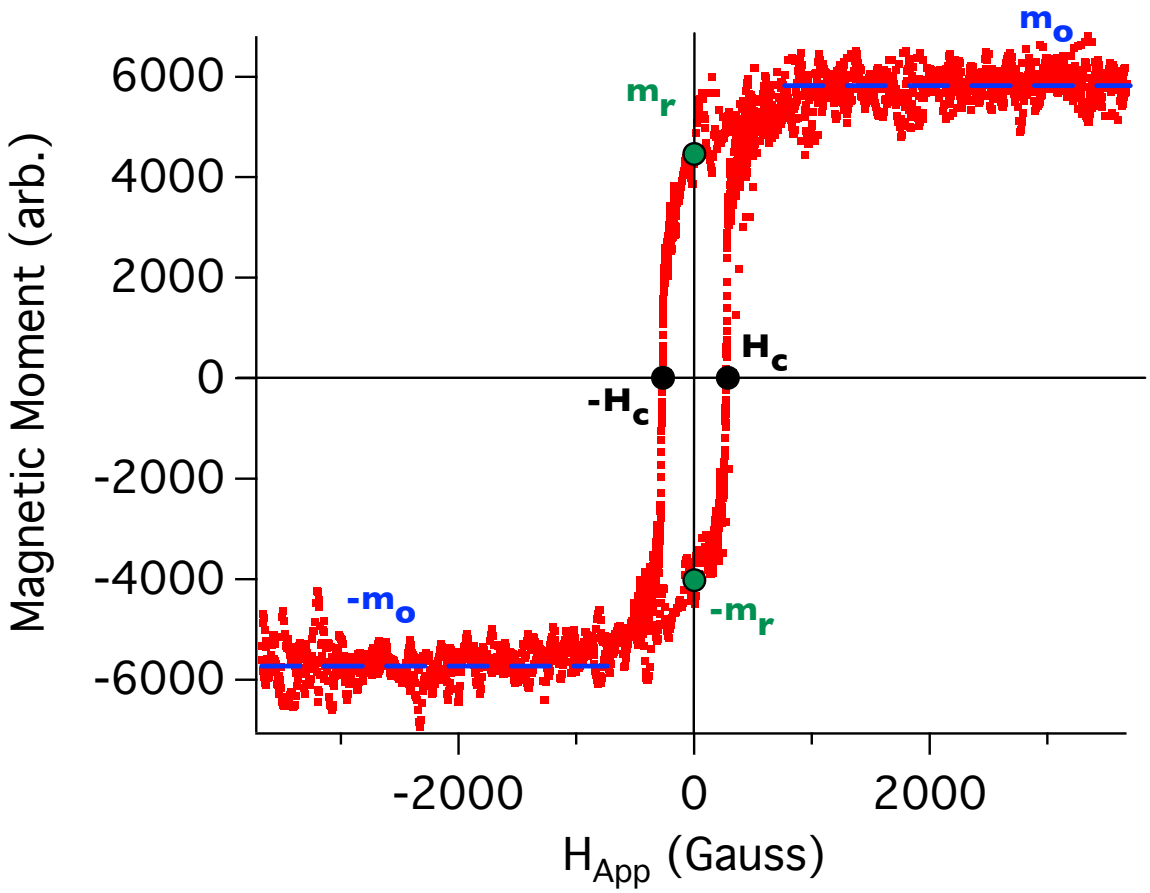

Figure 6.4: Hysteresis loop for a 150nm cobalt bulk film.

of the cantilever is given by,

$$\omega_0 = \sqrt{\frac{k}{m}}, \tag{6.2}$$

where k is the spring constant and m is the effective mass. Following [104], if the cantilever is oscillated at a frequency $\omega \neq \omega_o$ with an amplitude δ_0, the tip of the cantilever will also oscillate with some amplitude δ with a phase shift ϕ relative to ω. The equation of motion which describes the resulting signal at the photodetector due to the motion of the cantilever tip is given as,

$$\frac{\partial^2 d}{\partial t^2} + \frac{\omega_0}{Q}\frac{\partial d}{\partial t} + \omega_0^2(d - d_0) = \delta_0\omega_0\cos(\omega t), \tag{6.3}$$

where $d(t)$ describes the tip sample distance, d_0 is the tip-sample distance at zero drive amplitude and Q is the overall quality factor. Q includes not just the properties of the cantilever itself, but

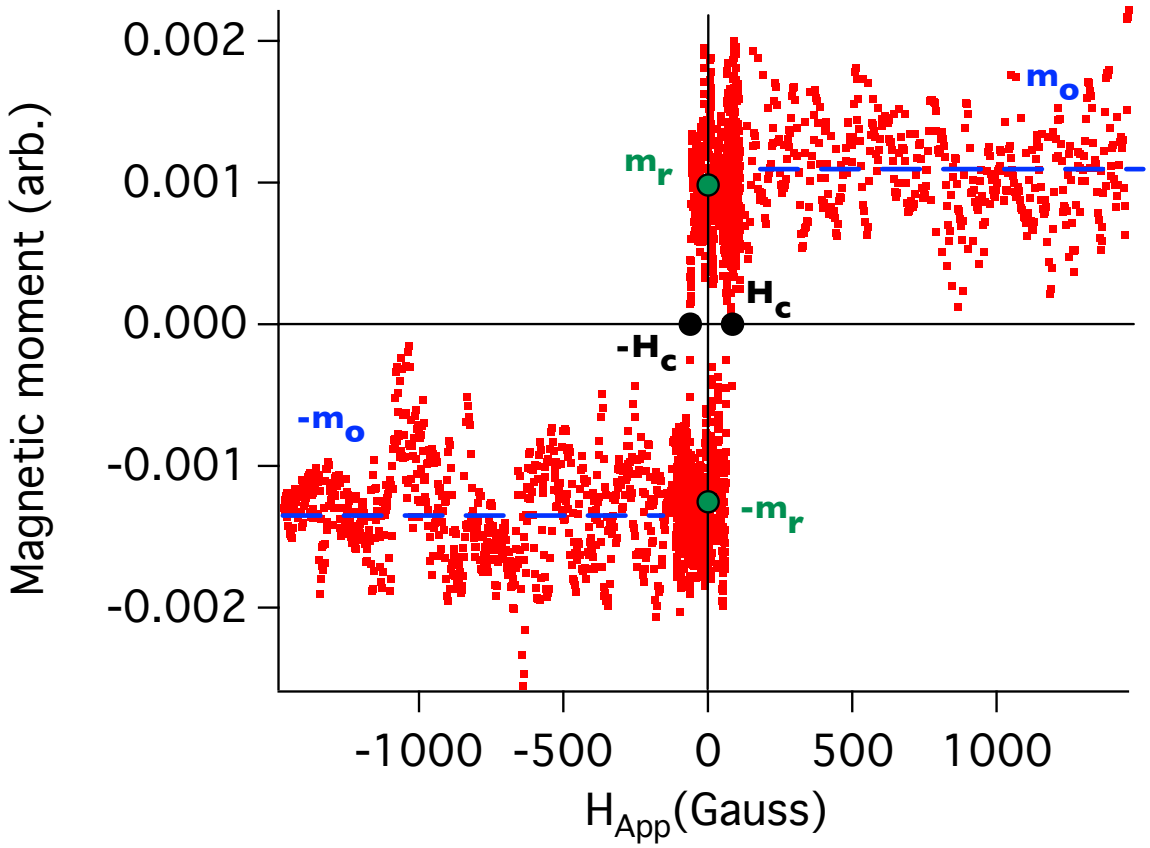

Figure 6.5: Hysteresis loop for a 30nm cobalt bulk film.

the damping γ from the environment as well as,

$$Q = \frac{m\omega_0}{2\gamma}. \tag{6.4}$$

For a forced oscillator, the steady state solution for $d(t)$ is,

$$d(t) = d_0 + \delta\cos(\omega t + \phi). \tag{6.5}$$

Thus we find the the amplitude and phase shift of our cantilever to be,

$$\delta = \frac{\delta_0\omega_0^2}{\sqrt{(\omega^2 - \omega_0^2)^2 + 4\gamma^2\omega^2}}, \tag{6.6}$$

$$\phi = \arctan\frac{2\gamma\omega}{\omega^2 - \omega_0^2}. \tag{6.7}$$

This result clearly ignores any tip-sample interactions. For $\delta_0 \ll d_0$, the force on the AFM tip as a function of the distance between the tip and the surface $F(d)$ can be considered to only

depend on the change in force along z. This approximation results in an effective change in the spring constant of our cantilever as,

$$k_{eff} = k - \frac{\partial F}{\partial z}. \tag{6.8}$$

Plugging Eq. 6.8 into Eq. 6.2 yields a new resonance frequency for the cantilever,

$$\omega = \omega_0 \sqrt{1 - \frac{1}{k}\frac{\partial F}{\partial z}}. \tag{6.9}$$

Assuming $\partial F/\partial z \ll k$, we finally find that the change in the resonant frequency of the cantilever due to tip-surface interactions $\Delta\omega$ is given by,

$$\Delta\omega = -\frac{1}{2k}\frac{\partial F}{\partial z}\omega_0. \tag{6.10}$$

Similarly the change in the phase shift of the cantilever due to tip-surface interactions $\Delta\phi$ is found to be,

$$\frac{\Delta\phi}{\Delta\omega_0} = \left.\frac{\partial\phi}{\partial\omega}\right|_{\omega_0}, \tag{6.11}$$

$$\Delta\phi = -\frac{Q}{k}\frac{\partial F}{\partial z}. \tag{6.12}$$

What happens then if we consider a small magnetic dipole attached to the tip of our cantilever? Similar to the AFM, by scanning this magnetic cantilever across the sample at a fixed height above the surface, we are now sensitive to changes in the *magnetic force* on the tip due to magnetic material on sample. This is MFM.

Continuing to follow [104], the magnetic force $\overline{F}$ felt by each magnetic moment m in the tip of the MFM probe due to a magnetic sample's stray field $\overline{H}$ in the absence of external free current is,

$$\overline{F} = \mu_o(\overline{m}\cdot\nabla)\overline{H}. \tag{6.13}$$

The force density $\overline{f}$ is given by the force on each magnetic moment times the number N of magnetic dipoles per unit volume,

$$\overline{f} = N\overline{F} = \mu_0(\overline{M}\cdot\overline{\nabla})\overline{H}. \tag{6.14}$$

The total force on the tip is found by a volume integral over the force density. Taking the approximation that the MFM tip can be considered as a single magnetic dipole with moment m_z, the

change in the phase shift due to tip-sample interactions for an MFM measurement is,

$$\Delta\phi = -\mu_0 \frac{Q}{k} m_z \frac{\partial^2 H_z}{\partial z^2}. \tag{6.15}$$

Thus, a change in the phase shift of a driven MFM tip will map the second derivative of the stray field of our magnetic sample.

Performing an MFM measurement proceeds as follows: an AFM measurement is performed in a line scan along x using the MFM tip. This yields the z-height data for that particular line scan. Now to perform a clean MFM measurement, the tip is raised a fixed distance above the surface (lift height) which tracks with the features measured by the previous AFM scan. This is to remove physical and atomic interactions between the tip and the surface during the MFM scan ensuring that any change in the phase shift of the cantilever is due solely to the stray magnetic fields from the sample. The tip is then stepped in y and the process repeats.

Figure 6.6 shows the results of an MFM scan of a Yoneda style micromagnet with a lift height of 60nm. On the micromagnet itself, a "leopard print" pattern can be observed. This is indicative of a multi-domain magnet which is to be expected given it's size. Of particular interest is the varying magnitude of the stray field in the gap of the magnet which is critical for electrically driven ESR. Similar results can also be seen for an MFM scan of a Wisconsin-Delft style micromagnet in Fig. 6.7.

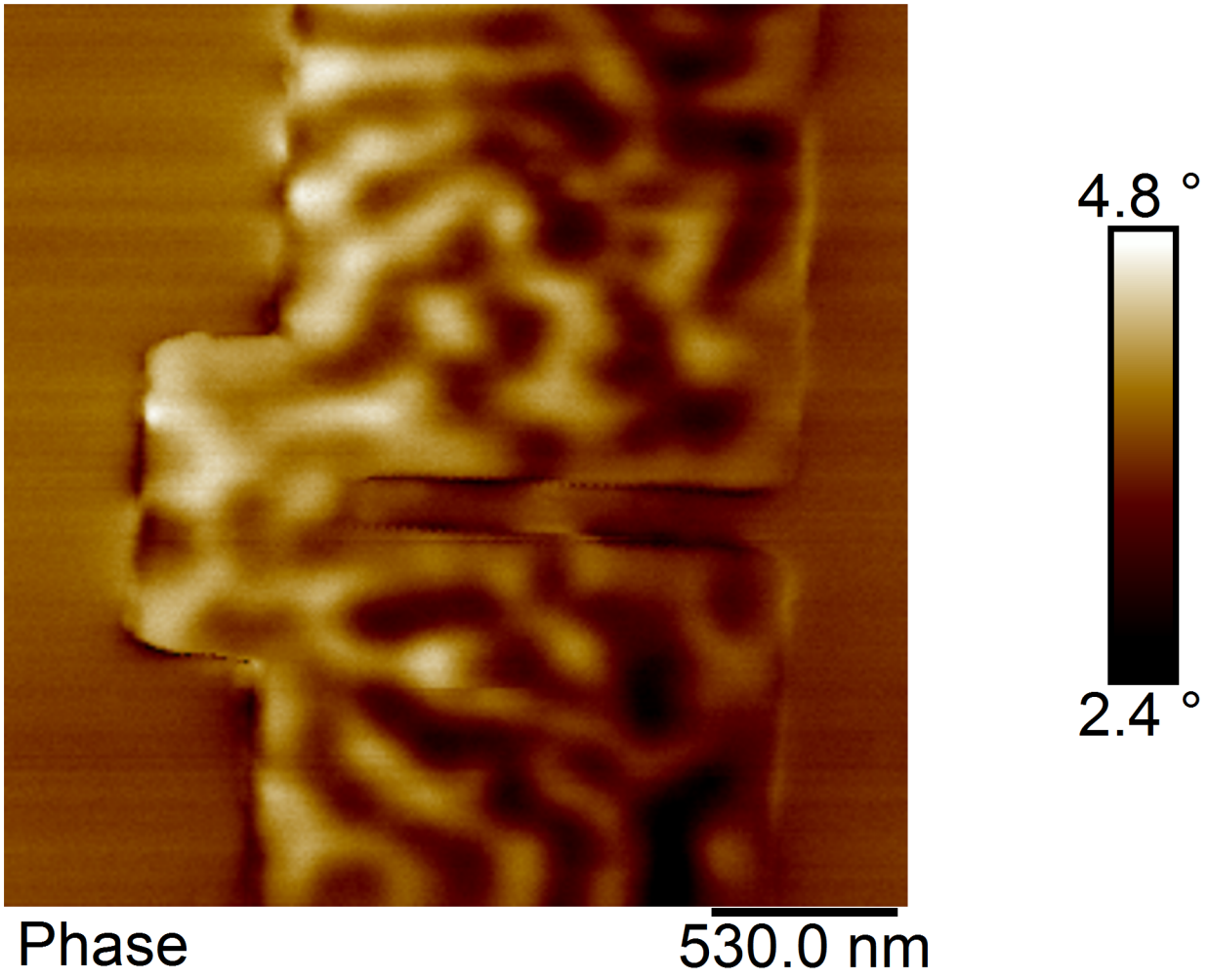

Figure 6.6: MFM data for a Yoneda style micromagnet.

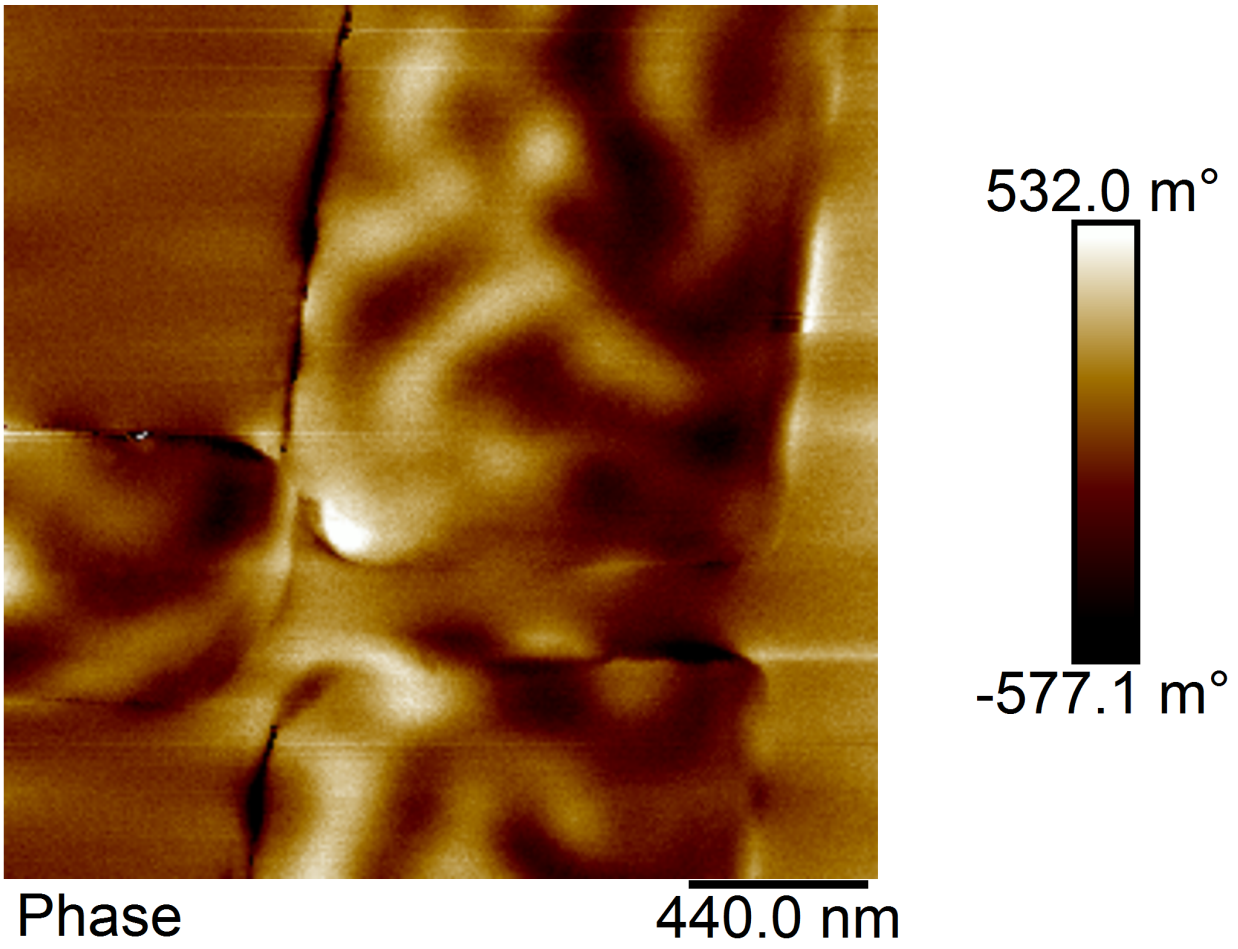

Figure 6.7: MFM data for a Wisconsin-Delft style micromagnet.

Chapter 7

Future work

While significant progress has been made, there are still many obstacles ahead to realizing a fault-tolerant, universal quantum computer. In Si/SiGe, material growth and characterization have presented significant challenges. As discussed previously, a good qubit has basis states that are well separated in energy from other levels to maximize control and minimize leakage. In a silicon-based qubit however, we not only have our orbital levels due to confinement, but valley states as well. Any steps or roughness present at the quantum well interface can have drastic effects on the magnitude of the valley splitting as a function of lateral position of the dot, potentially leading to unexpected decoherence. [105] This is a potential scalability problem, as individually tuning each qubit to accommodate differences in valley splittings for each dot in a multi-million qubit computer may be untenable. In addition to continued work on growth techniques, research into engineering the valley physics of heterostructures could yield a promising path to future qubit implementations. [106]

Another potential research avenue lies in device design and architecture. The experiments presented in this thesis use an older, more open style of device layout. Confinement gates are lithographically defined as Ti/Au nanowires on one layer of the device while accumulating reservoir and dot gate paddles are defined on an upper layer, with each layer separated by a thick, electrically isolating oxide. While this style of device offers a lot of flexibility with multiple gates being used to serve multiple purposes in the device, it ultimately will fail as the number of qubits scales up

(the device in Ref. [4] requires ~ 30 DC lines to operate two double-dot qubits). An alternative is to use overlapping aluminum gates instead. [53, 99, 107] Because of the native, insulating oxide which grows around each aluminum device wire after exposure to air or an oxygen plasma, gates no longer need to be spatially separated; they can lie right on top of one another. This has the advantage of a smaller overall design footprint, which is attractive when considering scaling. [108] Furthermore, device gates now have increased sensitivity and control (they are all now closer to the 2DEG), potentially leading to improvements to one- and two-qubit gate fidelity which is crucial to realizing a universal quantum computer.

Qubit implementation is also an area which deserves future consideration. As referenced earlier in this thesis, there are many different types of qubits that can be formed in quantum dots hosted in silicon heterostructures (e.g. spin, charge, singlet-triplet, and exchange-only qubits). The best choice for a fault-tolerant, semiconductor-based quantum computer remains to be seen, but a good candidate for future study is the quantum dot hybrid qubit. [96] This qubit architecture is composed of three electrons in a double quantum dot and can be thought of as a hybrid of a charge and a spin qubit. Fast, two-axis gate manipulations are realized with all electrical control. [51, 85, 95] Furthermore, coherence times of the qubit in the far-detuned, spin-like regime have been shown to be significantly extended through engineering of the qubit's internal parameters to make it less sensitive to charge noise. [15] Recent work suggests that fast, two-qubit gates can be enabled through strong capacitive coupling between adjacent hybrid qubits. [4] These properties make the quantum dot hybrid qubit an attractive candidate for future research towards a universal quantum computer.

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