Fabrication of Grafted UWBG Bipolar Devices

By

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To Madison,

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Abstract

In this dissertation, the fabrication of Heterojunction Bipolar Transistors (HBTs) and PN junction diodes using Ultra Wide BandGap (UWBG) materials is explored, demonstrated and tested. Specifically, working HBTs composed of n-AlGaAs/p-GaAs/p-GaAsP/n-GaN and p-AlGaAs/n-GaAs/p-C(diamond) and a PN diode of p-Si/n-Ga_2O_3 were fabricated and characterized, exhibiting excellent IV-characteristics. The fabrication of abrupt heterojunctions, such as GaAsP/GaN, GaAs/diamond, and Si/Ga_2O_3 with high quality, was made possible through the semiconductor grafting technique. This method fundamentally removes he limitation on material selections for forming heterojunctions. The demonstrated GaN, diamond HBT and Ga_2O_3 PN junction diode pave the way for high-power and high-speed devices applications in electric vehicles (EV), cloud computing, photovoltaic devices, and artificial intelligence (AI) systems, enabling more efficient and sustainable technological advancements.

In the first chapter, current trends in semiconductor devices and their applications are explored, emphasizing the need for a paradigm shift from silicon-based devices to compound semiconductor or UWBG-based applications. The semiconductor grafting technique is introduced as a novel approach to address one of the biggest challenges in utilizing compound material or UWBG semiconductors for device applications: forming heterojunctions with semiconductors of abrupt lattice mismatch. The chapter then suggestes how the semiconductor grafting technique can be applied to the fabrication of HBTs and PN junction diodes, discussing technical challenges and their solutions.

The second chapter investigates the fabrication of grafted p-AlGaAs/n-GaAs/p-C (diamond) HBT. A newly developed transfer-printing technique—double-flip transfer—is

introduced to address concerns related to the remaining AlAs layer after undercutting p-AlGaAs/n-GaAs nanomembranes. Additionally, surface treatment on diamond samples are discussed to lower the electron affinity and reduce valence band discontinuity between n-GaAs and p-C. Following successful fabrication, the diamond HBT features a DC gain of up to 2000. Further characterizations are needed to improve the yield of diamond HBT.

In the third chapter, an n-AlGaAs/p-GaAs/p-GaAsP/n-GaN HBT is demonstrated, featuring a DC gain of around 80. By employing the semiconductor grafting technique, six different types of n-GaN substrates are seamlessly integrated with four types of nanomembranes, resulting in four different combinations of HBT. The only functioning HBT is composed of the n-AlGaAs/p-GaAs/p-GaAsP membrane and the GaN substrate with a high doping concentration on the surface. The IV characteristics are analyzed, examining the effects of surface treatment using ALD and a thin doping concentration layer on GaN substrate. These results will provide insights into developing high-yield GaN HBTs for high-speed and high-voltage applications.

In the fourth chapter, PN junction diodes of n-type $\beta - Ga_2O_3$ integrated with p-type silicon are explored, along with $\beta - Ga_2O_3$ Schottky diodes created through the semiconductor grafting techniques. While most published PN junction diodes have utilized p-type sputtered oxide materials, such as NiOx and Cu_2O, for forming heterojunctions with $\beta - Ga_2O_3$, this study features the novelty of forming epitaxy-like heterojunctions by grafting p-type silicon nanomembrane onto n-type Ga_2O_3. The high interface quality in the grafted heterojunctions is measured by EELS and STEM.

Finally, the last chapter of the dissertation briefly summarizes possible future work, conclusions, and insights derived from these studies. The semiconductor grafting technique offers a revolutionary method for fabricating bipolar devices employing UWBG materials, which will be

applied in future device applications, such as artificial intelligence, cloud computing, electric vehicles, and photovoltaic devices. This groundbreaking approach will contribute to the development of more efficient and sustainable technologies in various fields.

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Chapter 1

Introduction

In 2022, the entire semiconductor market was valued at around 580 billion USD [1, 2], while compound semiconductors, such as silicon carbide, gallium nitride, and gallium oxide, etc., were accounted for 40.5 billion USD, representing less than 10% of the entire semiconductor market. [3] The remaining 90% of the market size consisted of the silicon-based semiconductor industry. Despite the superiority of compound materials, which will be discussed in this chapter later, applications and developments of the compound materials have been relatively underdeveloped compared to those of silicon semiconductors [4-6]. For example, in 2016, the most advanced III-V semiconductor devices only contained a few thousand components per chip [7, 8]. Focusing on more specific functions of device applications, 87% of the high-power semiconductor devices market is based on mature silicon technology [9], while more than 90% of the photovoltaic cell devices in the markets utilize silicon as their most important material [10]. Two major reasons contributed to the huge success of silicon in the modern chip industries. The first one is the stability

of silicon dioxide, maintaining a great quality under high temperatures. Silicon dioxide is grown and used for Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs). Second, the economic advantage has contributed to the dominant position of silicon in the markets. Silicon is the second most abundant element on Earth. Silicon makes up 27.7% of the mass of the Earth's crust [81]. The mature technology of fabricating integrated circuit chips on silicon wafers has contributed to silicon's near-monopoly. This technology has been developed since 1955, when the first MOSFETs were commercialized [12 13]. Historians and sociologists argue that the Digital Revolution, also known as the Third Industrial Revolution, has been made possible by the rapid and aggressive growth of the markets of silicon-based devices in the last century [14, 15]. This trend is partly illustrated by Dr. Gordon Moore's iconic observation called "Moore's Law," which states that "every two years, the number of electrical components such as transistors in a dense integrated circuit doubles [16]." Even though the empirical observation was formulated more than five decades ago, it is still valid today, reflecting the exponential nature of the miniaturization of silicon devices [17, 18]. With these advantages and the surge of demand in the market, the silicon chip market is projected to grow to 1034 billion USD by 2031 [19]. To meet the increasing demand for better-performing chips, big semiconductor manufacturers—Samsung Electronics, TSMC and Intel—have already declared the development of MOSFETs with a node size smaller than 2nm, which is only eleven times as larger as the diameter of a single silicon atom [19, 20]. Namely, the size of the devices approaches the fundamental limit of silicon-based devices.

Despite the enormous growth of silicon-based semiconductor markets, the innovation of silicon devices through miniaturization is becoming harder due to the physical bottom line drawn by quantum mechanics [21]. Even if the engineering barriers, such as high heat dissipation and high leakage currents in devices of a few Angstroms' dimensions, are solved, the Compton

wavelength of an electron defines the smallest dimension of possible transistors [21]. If Dr. Moore's prediction keeps valid, then the node length of transistors will converge to the quantum limit in 2036 [21]. However, it is obviously forecasted that there will be even more needs for larger storage, faster computing, and higher efficiency for cloud computing, Artificial-Intelligence (AI), Electric Vehicle (EV) and green energy/carbon-neutral trends to fight climate change beyond 2036 [22-27]. In addition, AI applications generate data of 80 exabytes each year, and this is expected to increase to 845 exabytes by 2025 [22]. Thus, demand for computing hardware such as CPU, GPU and memory chips will increase by 10 to 15 percent by 2025 [22]. This trend not only intensifies the need for a larger volume of storage and higher speed of processors but also requires efficient heat dissipation that cannot be achieved with the material properties of silicon [27]. In terms of high-power applications, power capability (V_B^2/R_{on}) and maximum operating temperature are not desirable for the future demand of power electronics [12]. Furthermore, international regulations and movements to fight global warming that causes climate change are one of the most powerful driving factors calling for innovation in semiconductor devices [29-32]. To reduce pollutant emissions from internal combustion engines in cars, many governments, including the United States, the United Kingdom and Europe Union, encourage or force the automotive industries to prepare for a transition toward total electrification of vehicles [33-35]. Especially, the U.S. Department of Energy set a goal of the development of high-power converters that will be utilized in EV/HEV with power densities as high as 14.1kW/kg and efficiencies greater than 98% [36]. This cannot be achieved with traditional silicon power devices due to silicon's limit of physical properties [36]. The development of silicon-based solar cells is at its saturation while the efficiencies of silicon Photo-Voltaic devices (PV) are approaching the fundamental limit of the material [10]. It has been suggested that the intrinsic limit of silicon PV devices is around 29%,

while one of the latest crystalline silicon solar cells has an efficiency of 26.7% [10]. Despite this ultimate challenge for better PV devices with silicon, the demand for renewable energies has been increasing rapidly. Whereas only 12% of electricity was generated from renewable sources in 2000 in the EU, the number has increased to 37.5% today [48]. To keep up with these trends toward fast and efficient devices, a paradigm shift for developing semiconductor devices is inevitable rather than depending mostly on silicon materials.

Table 1.1 *The material characteristics of silicon and WBG materials. The Figure of Merits of the materials rather than silicon are normalized based on those of silicon [82].*

	Si	GaAs	4H-SiC	GaN	Diamond	$\beta - Ga_2O_3$
Bandgap (eV)	1.1	1.43	3.25	3.4	5.5	4.85
Dielectric constant, ϵ	11.8	12.9	9.7	9	5.5	10
Breakdown field (MV/cm)	0.3	0.4	2.5	3.3	10	8
Electron mobility, μ ($cm^2/V \cdot s$)	1480	8400	1000	1250	2000	300
Electron Saturation velocity, v_s (10^7 cm/s)	1	1.2	2	2.5	1	1.8-2
Hole mobility ($cm^2/V \cdot s$)	450	400	120	30-100	2000	1.3
Thermal conductivity ($W/cm \cdot K$)	1.5	0.5	4.9	2.3	20	0.1-0.3
Johnson = $E_c^2 V_s^2/4\pi^2$	1	1.8	278	1089	1110	2844
Baliga= $\epsilon\mu E_c^3$	1	14.7	317	846	24660	3214
Keyes= $\lambda[(cV_s)/(4\pi\epsilon)]^{1/2}$	1	0.3	3.6	1.8	41.5	0.2

One of the obvious choices to meet the future requirements for better devices and overcome the challenge posed on silicon-based industries is to fabricate devices by using Wide-BandGap (WBG) materials, such as Silicon Carbide (SiC), Gallium Nitride (GaN), Gallium Oxide ($\beta - Ga_2O_3$), and diamond (C) that are superior compared to silicon in terms of material properties [37-40]. Their characteristics are summarized in Table 1.1. For power electronics, device performances are directly affected by material properties such as carrier mobilities, critical field strength, intrinsic concentration, and thermal conductivity [41-43]. High electron and hole

mobilities greatly reduce the switching recovery time, which leads to higher switching frequency. Faster-switching means that there can be fewer passive components on IC chips, which reduces the cost of manufacture [44]. Furthermore, a high breakdown field offers chances to operate with high voltage and current without compromising the stability of devices [45]. Low intrinsic concentration also plays a key role in increasing operation temperature along with high thermal conductivity [46]. The WBG materials in Table 1.1 are perfect candidates for high-power and high-speed applications owing to their superior properties [47]. Furthermore, it is required to use III-V materials in tandem structures for PV applications to exceed the fundamental efficiency of silicon-based photovoltaic devices [49]. Thus, the usage of WBG materials is also essential for PV applications.

However, using these materials presents its own set of challenges, such as the relatively less mature technology for fabricating WBG-based devices. For instance, the cost of growing wafer-scale substrates for these materials is significantly higher than that for silicon [50, 51]. Most of all, the biggest and most fundamental challenge is forming heterojunctions with other semiconductors. To design advanced semiconductor devices, it is critical to form heterojunctions between semiconductors with different band gaps. These heterojunctions are essential for creating solar cells, lasers, bipolar transistors, and field-effect transistors [52-54]. Namely, heterojunctions are basically building blocks to make devices, such as Bipolar Junction Transistors (BJTs), MOSFET and Schottky Junction Diodes (SJDs) [55]. Due to the heterogeneous nature of heterojunctions, a lattice mismatch between two materials is a major concern. The interface between two materials must maintain high quality with a minimum density of defects. Poor interface quality leads to defects that create trapped energy states on the interface, acting as recombination centers. This can cause a reduced on/off ratio, an Ideality Factor (IF) for diodes,

and a low gain for transistors [53]. One method for fabricating heterojunctions is the epitaxial growth of one semiconductor on another semiconductor with a minimal difference in lattice parameters [56]. This limit greatly reduces the potential for using these materials because even a slightly higher lattice mismatch can cause several defects, including stacking faults and dangling bonds [60-61]. The requirement for a lattice match restricts the number of possible combinations of semiconductors for compound semiconductors. For example, GaN only has been exclusively used with AlGaN and InGaN for high-power applications through conventional epitaxy. Likewise, GaAs has been usually used with AlGaAs and InGaAs for forming heterostructures.

Naturally, there have been a few technologies developed to form heterojunctions without worrying about a lattice-match. The first one is direct bonding of wafers [57-59]. Two smoothly polished wafers with an abrupt lattice mismatch are preprocessed through chemical and dry cleaning etc. Then, one of the wafers is placed on the top of the other, and they are bonded at room temperature. Then, the fused wafers are annealed, and the interface forms heterojunctions. It has been shown that the wafer-fused interface suffers vast amounts of defects, such as unfilled dangling bonds, fixed charges, trapped particles and weak bonding [62-64]. Because there is no buffer layer between the two wafers, atoms of each side freely diffuse to the other side when being annealed at high temperatures, which degrades the quality of the surface even more [65]. The performances of the diodes and Heterojunction Bipolar Transistors (HBTs) fabricated on bonded wafers are not as good as the devices fabricated by using the continuous epitaxy [66-68]. The second of the technologies is to transfer thin two-dimensional materials, such as graphene, hBN, MoS_2, WSe_2, and fluorographene on foreign semiconductor substrates to fabricate diodes, HBT, and MOSFET [69, 70]. There still exist engineering challenges to control the synthesis of the 2D materials and manipulate the interface conditions due to their 2D nature [71, 72]. Most of all, it is

still difficult and expensive to grow two-dimensional materials whose size is up to the wafer scales, which is necessitated to meet the demand from the chip markets [68]. The final and most notable one is the semiconductor grafting technique.

Table 1.2 *The diodes fabricated by the semiconductor grafting technique and their performances.*

Nanomembrane	Substrate	I_{on}/I_{off} @1V	Ideality factor	Reference
p-Si	n-GaAs	7.9×10^9	1.07	[55]
p-GaAs	n-GaN	1.1×10^6	1.13	[55]
p-Ge	n-Si	1.5×10^8	1.02	[55]
p-Si	n-GaN	4.1×10^8	1.14	[55]
n-GaAs	p-C	1.27×10^9(@3V)	1.85	[11]
p-GaAsP	n-GaN	1.84×10^8	1.1	This work
p-Si	n-Ga_2O_3	3.15×10^7	1.13	This work

This technique has proven that more than 7 combinations of semiconductors with very high quality can be formed without worrying about an abrupt lattice mismatch, as organized in Table 1.2. The process flow of the grafting technique proceeds in the following order. First, deposit an ultra-thin oxide layer on any semiconductor substrate. Second, produce wafer-scale Nano-Membranes (NMs) whose thickness can vary from dozens of nanometers to several micrometers. Finally, transfer the sheets of NM picked up by PDMS onto the prepared semiconductor substrate. The ultra-thin layer between two semiconductors plays a crucial role by filling up dangling bonds on the interface [73-75]. The theoretical model has suggested that an ideality factor n of grafted diodes is calculated in the following equation when a density of states between a nanomembrane and a substrate is given as D_{ssn} [55].

$$n = 1 + \frac{1.81 \times 10^{-13}}{\epsilon_{ri}} W_i D_{ssn}$$

, where W_i is a thickness of a depletion region. It has been measured that a density of states on grafted interfaces can be low up to $\sim 10^{11}/eV \cdot cm^2$ for silicon surfaces [55]. Provided W_i is 1nm, then the ideality factor, n, is expected to be around 1.01-1.05. One of the most important part of the equation is that it does not involve with materials being utilized for heterojunctions. Regardless of what kinds of materials are forming heterojunctions, a diode performance is determined by a density of defect. Not only have the devices integrating silicon/germanium heterojunctions shown one of the lowest ideality factors and highest I_{on}/I_{off} ratio, but also the diode combinations of Si/GaN, GaAs/GaN and Si/Ga_2O_3 that had been impossible to fabricate through the conventional epitaxy have shown the record-breaking diode performances with a low ideality factor and a high on/off ratio. Their performances are well summarized in Table 1.2.

One of the most prominent applications of the semiconductor grafting technique is Heterojunction Bipolar Transistors (HBTs). By incorporating a heterojunction between an emitter and a base semiconductor in Bipolar Junction Transistors (BJTs), the HBTs acquire the benefits of higher gain and higher doping concentrations in base regions. HBTs generally feature several advantages over Field-Effect Transistors (FET) for low-noise, high-frequency, and high-power applications because HBTs have a higher conductance g_m, greater linearity, better threshold uniformity, a larger maximum oscillation frequency f_{max}, and higher breakdown voltages compared to FETs [53, 76, 77]. Exploiting these characteristics of HBTs, they are commonly used in automotive radar systems where high-power efficiency is necessary and wireless communication systems, including cellular devices [78-80]. However, single HBTs that have a single heterojunction in only an emitter-base junction also suffer several disadvantages. One disadvantage of single HBTs is high offset V_{ce} in the saturation region. If V_{ce} is low enough for single HBTs, the current from the base, Ib, cannot easily penetrate through an emitter-base

heterojunction because of its heterogeneous nature. Thus, electric current goes from a base to a collector instead, making the base-collector current negative, which eventually decreases the I_c current. Thus, a larger V_{ce} is necessary to turn on the transistors, which reduces the output signals. Furthermore, a material with a lower band gap than that of an emitter material is usually incorporated for a base to improve performance. However, a base with a lower band gap has a lower breakdown voltage on a base-collector junction due to the lower band gap. To improve the performance of a single HBT, a base and collector junction can also be made of materials that have different lattice structures. The HBTs that have heterojunctions on both emitter-base and base-collector junctions are called Double Heterojunction Bipolar Transistors (DHBT). By incorporating another heterojunction as a base-collector junction along with an emitter-base junction, DHBTs can have two major advantages over single HBTs: low offset voltage at a saturation region and a high breakdown voltage of a base-collection junction. For a DHBT, a base-collector junction also suppresses a collector current that compensates for the suppression effect of the EB heterojunction. Thus, the offset voltage of V_{ce} is reduced compared to that of single HBTs. Another advantage of DHBTs is the high breakdown voltage of base-collector junctions when wide-bandgap materials are used for collectors. Despite the advantages of DHBTs that play a very important role in high-power applications, they also come with their own engineering challenges—Discontinuity of conduction bands on the base-collector junctions which is also called "band-bending."

The band-bending effect prevents electrons in a base from being collected in a collector. In a single HBT, the current of electrons collected to a collector, I_{nC}

$$I_{nC} = \frac{A_E q D_n n_{po}}{L_n} cosech\left(\frac{W}{L_n}\right)\left\{\left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right] - \coth\left(\frac{W}{L_n}\right)\left[\frac{n_p(W)}{n_{po}} - 1\right]\right\}$$

If a base-collector junction is a homojunction, $\frac{n_p(W)}{n_{po}} = \exp\left(\frac{qV_{BC}}{kT}\right)$. On the other hand, consider the case where there exists a discontinuity in the conduction bands, ΔE_c when a heterojunction is incorporated in the base-collection junction. Then, there is a stronger internal electric field generated in the junction because of the discontinuity. Thus, more electrons are diffused from the collector to the base, which increases the density of electrons at the base region, $n_p(W)$. As $n_p(W)$ gets higher, the current of the electrons collected I_{nC} becomes even lower, which leads to degraded performance of HBTs, leading to a lower DC gain. To suppress the band-bending effect, substrate semiconductors must be treated in a special way. In the following chapters, novel ways to lower the discontinuity of conduction bands on the base-collector junction will be introduced with experimental measurements. The processes include integrating triple compound materials on junctions, treating substrates with ozone plasma, and conducting Atomic Layer Deposition (ALD). By solving the engineering challenge to suppress the band-bending effect, DHBTs utilizing AlGaAs, GaAs, and GaAsP as the emitters and the bases, GaN and diamond as the collector, respectively, have been demonstrated with a high DC gain of up to 80. Additionally, DHBTs that was deemed to be impossible, p-AlGaAs/n-GaAs/p-diamond, has been fabricated, showing the DC gain up to 2000.

$\beta - Ga_2O_3$ is also one of the most promising WBG materials. While there have been many pieces of research on growing n-type doped $\beta - Ga_2O_3$, p-type doping of the material with high quality has been essentially not possible. Due to this issue, the development of Ga2O3 as a power application has usually been focused on unipolar devices such as MOSFETs and SJDs despite the superior properties of the material. By using the grafting technique, bipolar p-n junction heterostructures have been fabricated with p-type silicon and n-type $\beta - Ga_2O_3$ with record-high

diode performances, opening up the new possibility toward HBT integrating $\beta - Ga_2O_3$ as a collector.

The rest of the contents of this dissertation is organized in the following order. First, HBTs with a diamond as a collector and III-V materials as a base and an emitter are demonstrated in Chapter 2. The characterization methods of diamond materials are demonstrated with the experimental results, focusing on how to reduce band-bending on the diamond substrates. Notably, the newly developed double-flip transfer is introduced as a way to graft nanomembranes on external semiconductor substrates. The IV characteristics of the AlGaAs/GaAs/diamond, including the high DC gain up to 2000, are discussed along with the potential of the research and the prospect for the future development of diamond HBTs. Second, diodes and HBTs utilizing GaN as a collector are introduced with the method of fabrication and characterization in Chapter 3. The band-bending effect of several GaN substrates is discussed in terms of device designs, followed by analyzing the IV characteristics of the fabricated diodes and HBTs, including Gummel plots. Then, the potential of the devices will be discussed along with research topics for the future. Third, the p-n bipolar heterojunction diodes of n-type $\beta - Ga_2O_3$ and p-type silicon are presented with the method of fabrication in Chapter 4. The experimental results of material characterizations, including TEM and EELS, are shown and analyzed. Along with them, the IV characteristics, such as diode performances and C-V measurements, are measured and studied. The prospect of possible DHBT incorporating $\beta - Ga_2O_3$ as a collector is also discussed.

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Chapter 2

Fabrication and Characterization of AlGaAs/GaAs/C DHBT by Nanomembrane Grafting

2.1. Introduction

Diamond(C) is an Ultra-Wide Band Gap (UWBG) material that has superior electrical and thermal properties, which make it suitable for applications of high-power, high-frequency, high-temperature, and high-voltages [1-3]. Its breakdown voltage is three times as high as that of gallium nitride, while the thermal conductivities are thirteen times that of silicon [4]. Its carrier mobility surpasses those of other III-V compound materials except for the electron mobility of GaAs [5]. Owing to these characteristics, the figure of merits of diamonds are highest among those of the semiconductor materials that have been used for high-power applications, as shown in Table 1.1. Schottky diodes and FETs have been demonstrated with high breakdown voltages at high temperatures [6-9]. However, electronic devices with outstanding performance that utilize diamonds are mostly unipolar devices, due to the challenges associated with achieving n-type doping in intrinsic diamonds. For n-type donors such as nitrogen and phosphorous, the ionization

energy levels are too high for effective activations [10-11]. Although bipolar PIN junction diodes with limited performance have been developed and published [12-13], high DC gain bipolar transistors, including BJTs and HBTs, have not yet been achieved. To circumvent the difficulty of efficiently doping diamonds with n-type dopants, a novel approach— the semiconductor grafting technique—has been employed to fabricate HBTs, using p-type doped diamonds as collectors [3]. Since the technique for growing n-type doped gallium arsenide with high electron mobility is well-developed, n-type GaAs nanomembranes can be grafted onto p-type diamonds using a few cycles of ultra-thin oxide layers between them [14]. By forming an n-GaAs/p-diamond heterojunction with ultra-thin oxides in between, PN junction diodes are achieved with high quality on the interface [3]. In the previous research, p-AlGaAs/n-GaAs/p-diamond HBTs were designed and fabricated by using the grafted p-AlGaAs/n-GaAs nanomembranes on p-diamond substrates. However, transistor performances could not be obtained despite the successful demonstration of emitter-base and base-collector diodes in the devices. One reason for the isolation of the emitter-base and base-collector junctions is the presence of residual AlAs layers that were not fully wet-etched after the release of the p-AlGaAs/n-GaAs nanomembrane layers. To overcome this challenge, the new grafting technique called “double flip transfer” has been developed and utilized to fabricate p-AlGaAs/n-GaAs/p-diamond HBTs. The other reason for the previous batch not having a DC HBT was high electron affinity (~0.3eV), which increased the discontinuity in the valence band, as shown in Figure 2.1. For the diamond used in this work, the surface electron affinity was adjusted to 80-100 meV through chemical cleaning and atomic layer deposition (ALD), significantly reducing the valence band energy barrier and facilitating hole collection in the reverse-biased collector. The newly fabricated HBTs utilizing diamond as a collector are presented, showing the high DC gain of ~2000.

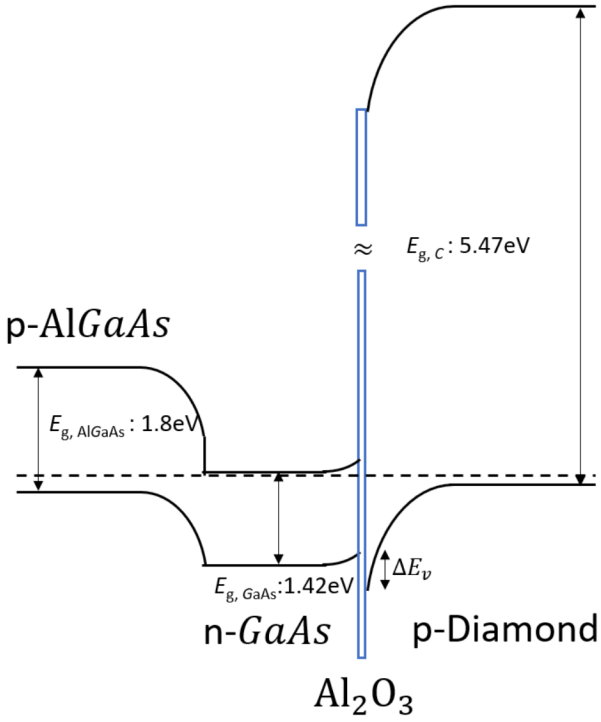

Figure 2.1 *The band diagram of p-AlGaAs/n-GaAs/p-C DHBT.*

2.2 Materials

Diamond

The p- layer and p+ layer of diamond were grown on a single crystal diamond substrate, as shown in Figure 2.2. The resistivity of p+ layer was measured to be $8.9 \times 10^{-2} \Omega \cdot \mathrm{m}$. After growing the p- layer, the surface had visually obvious defects of pits and scratches, as featured in Figure 2.3(a). Then, the surface of the diamond sample was treated by using Chemical Mechanical Polishing (CMP) for 120 minutes in order to make the surface smooth enough for transfer printing. The image after the CMP process is featured in Figure 2.3(b). Even though some scratches became less obvious, there were still mechanical defects left on the surface.

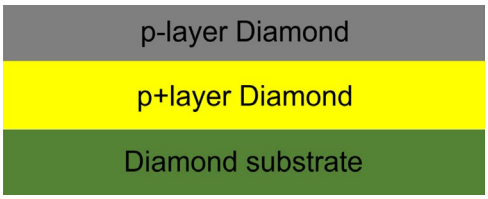

Figure 2.2 *The schematic diagram of the diamond sample utilized as a collector of p-AlGaAs/n-GaAs/p-C DHBT.*

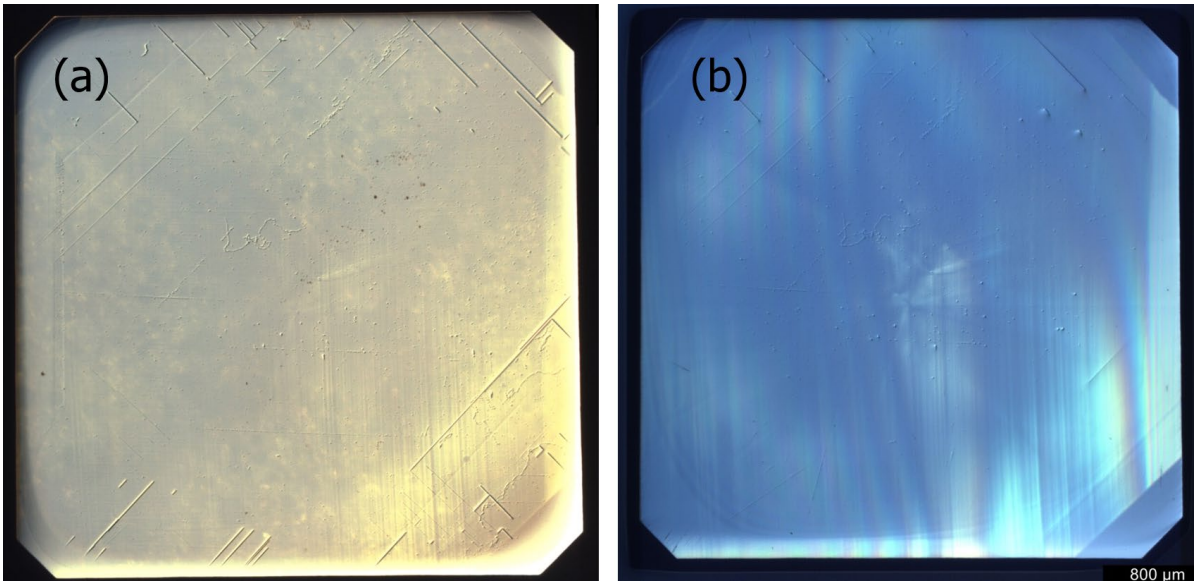

Figure 2.3 *(a) The diamond sample before the CMP process. (b) The diamond sample after 120 minutes of CMP.*

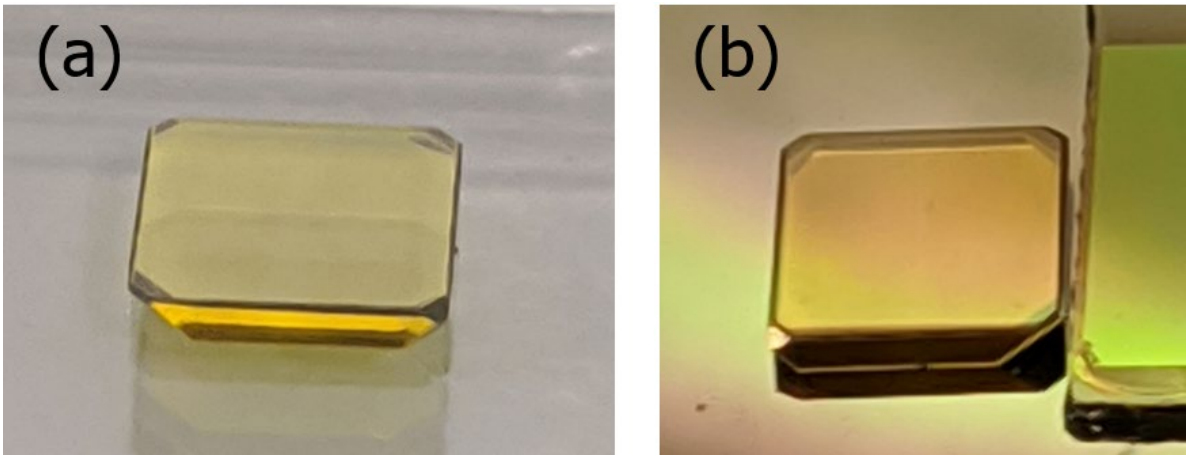

Figure 2.4 *(a) The diamond sample after the CMP process. (b) The diamond sample taken in the ALD chamber.*

p-GaAs/p-AlGaAs/n-GaAs naonomembrane

From the previous p-AlGaAs/n-GaAs/p-diamond DHBT, the conventional structure of GaAs/AlGaAs/GaAs nanomembranes (Figure 2.5(a)) was used. The additional measurement suggested that an additional AlAs layer exists between nanomembranes and the diamond surface [15]. The residual AlAs layer hampers electrons diffused from an emitter to be collected toward a collector because the hole mobility in p-GaAs is relatively low. To avoid this issue in the fabrication of the work, the nanomembrane samples of the inverted structure p-GaAs/p-AlGaAs/n-GaAs were grown through Metal Organic Chemical Vapor Deposition(MOCVD), as shown in Figure 2.8(b). In this structure, the base layer is on the top layer of the sample, and it directly contacts the p-diamond surface. In this way, there is no concern about extra AlAs layers between nanomembranes and the diamond surface. Furthermore, the thickness of a base region can be adjusted by dry etching before proceeding with releasing nanomembranes. The SIMS data is presented in Figure 2.6.

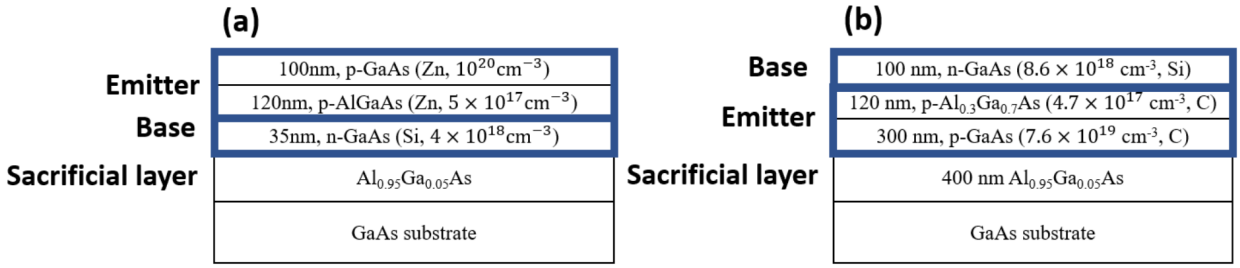

Figure 2.5 *The schematic diagram of the samples of (a) conventional p-GaAs/p-AlGaAs/n-GaAs/GaAs substrate (b) inverted n-GaAs/p-AlGaAs/p-GaAs/GaAs substrate.*

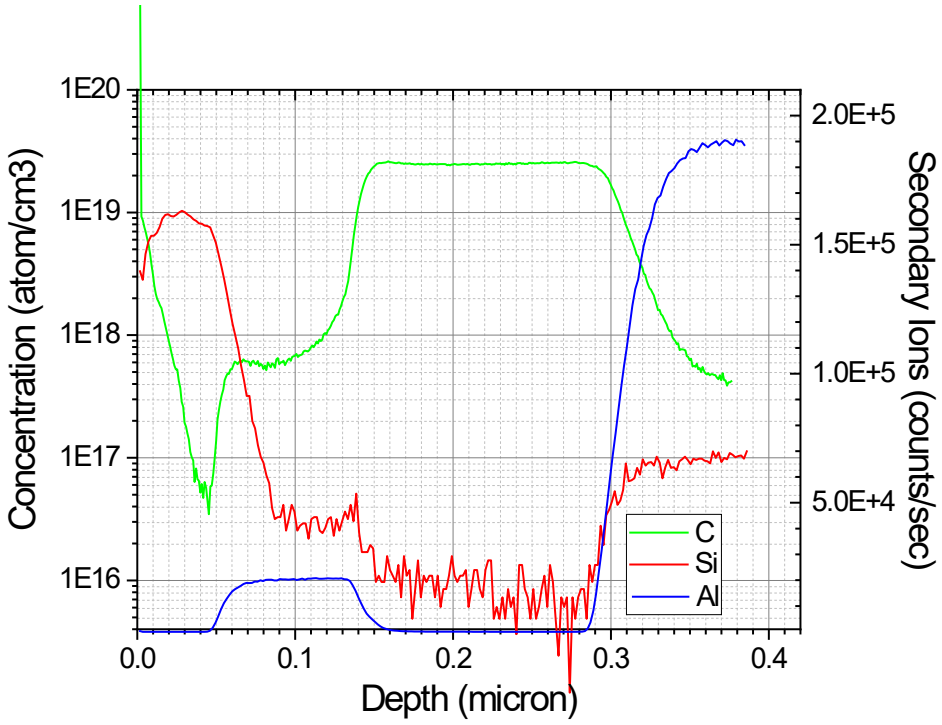

Figure 2.6 *The SIMS data of the sample of p-GaAs/p-AlGaAs/n-GaAs/GaAs substrate.*

2.3 Methods of Fabrication

a. Preparation of nanomembranes

The nanomembrane wafers were diced into 4cm by 4cm. Because the base layers were exposed to the air, unlike the conventional structure of nanomembranes (Figure 2.8(a)), the thickness of a base layer can be determined by etching the surface of the samples. For this batch, 20nm of the base layer was etched to make the base layer 25nm thick through an ICP etcher with a condition of RIE (60W), ICP (500W), BCl_3 (10sccm), Ar (5sccm), and 15mTorr for 14 seconds. Then, they were coated with S1813, followed by hole patterning through an MJB3 mask aligner with the condition of 5.5 mW/cm^2 for 30 seconds. The samples were developed in MF321 solution for one minute and, successively, etched by an ICP etcher for 210 seconds with the same

condition as the first etch. The sample with holes was placed into a 1:20 HF solution and left there for two hours.

b. Double-flip transfer

After the wet-etch process was completed, the samples were taken out of the HF solutions and directly put into DI water in a Teflon dish. Because the nanomembranes had been fully undercut, they would immediately float up on the surface of DI water. As the lattice parameter of GaAs is smaller than that of AlGaAs, the emitter side of the nanomembranes experiences compressive strains due to its thick GaAs layers (300nm) [16]. Thus, the emitter side of the floating nanomembrane is always facing down, as drawn in Figure 2.6. Then, a Teflon plate was brought close to the nanomembrane on DI water. Because of the hydrophobic nature of Teflon plates, the water surface makes a curve on the boundary, as described in Figure 2.6. Thus the nanomembrane rolled inside as the Teflon plate approached, and the base side was attached to the Teflon plate. This is the first flip of the double-flip transfer. Finally, the plate with the nanomembrane onto was taken out of DI water, then a square-shaped chunk of PDMS stamped the nanomembrane. Then, the PDMS with the nanomembrane was ready to conduct transfer printing on external substrates. In the meantime, the diamond sample was cleaned by rubbing with Q-tips in IPA, acetone, and DI water. After that, the nanomembrane was printed on the diamond substrates.

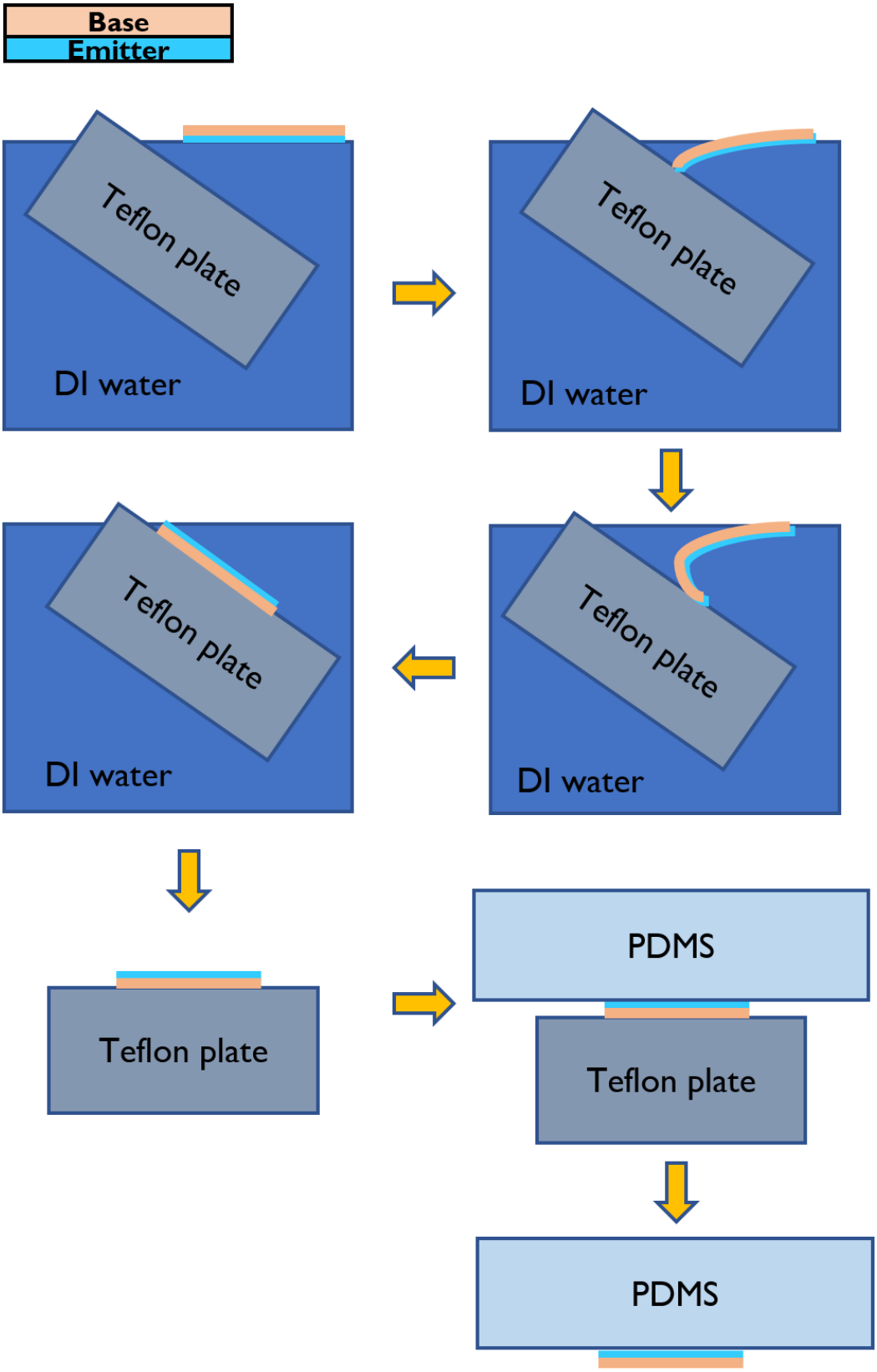

Figure 2.7 *The schematic diagram of the double-flip transfer.*

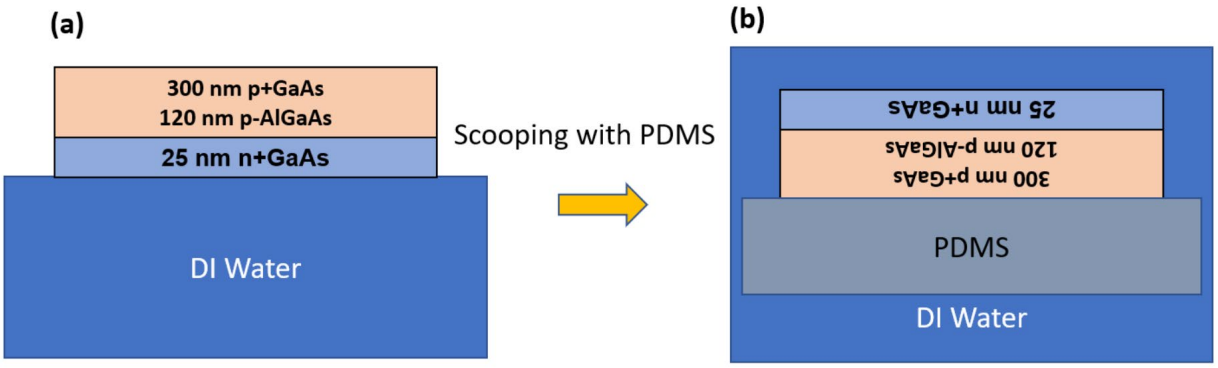

Figure 2.8 *(a) After nanomembranes are undercut, the nanomembranes immediately float up on the surface of DI water. At this point, n+GaAs (base layer) does already face down to the DI water. (b) After scooping with PDMS described in* ***Figure 2.10****, the p+GaAs layer is directly contacting the PDMS, so as for n+GaAs to be directly contacting the diamond sample.*

c. Annealing and O_2 plasma treatment

Rapid Thermal Annealing at 350℃ for 5 minutes was conducted on the transferred p-AlGaAs/n-GaAs/p-diamond sample in order to make a chemical bonding between the diamond and the nanomembrane. Then, the sample was treated with O_2 plasma of 100W for 20 seconds. Then, the sample became hydrophilic enough for proper photoresist coating.

d. Lithography and metallization

The negative photoresist, AZ5214, was coated on the diamond surface, using spinning of 2500rpm for 30 seconds, followed by baking the sample for 3 minutes at 95℃. Then, the sample was exposed under the emitter pattern for 2.2 seconds of 5.5 mW/cm^2 UV light, followed by baking it at 112℃ for 90 seconds. Then, the sample was exposed UV light of 5.5 mW/cm^2 without a mask for 25 seconds. The properly UV-exposed sample was brought into AZ917 developer to develop for 30 seconds. After confirming that the emitter pattern was developed properly and

clearly, then the sample was metallized with a metal stack of Ti/Pt/Au (15nm/50nm/100nm). The process was followed by a dry etch process, which is the most critical step in the entire process. Because the window of the etch process is less than 25nm, the thickness of etch was measured by AFM after every cycle of the dry-etch process. After the entire etch process, surface conductivity on the nanomembranes was measured. It was confirmed by the high electric currents that n+ GaAs was exposed. Then, a base metal stack of Pd/Ge/Au (30nm/40nm/100nm) was deposited on the sample. The process was followed by covering photoresists (S1827, 4000rpm, and 30 seconds) with base-mesa patterns, and the sample was exposed to UV-light of 5.5 $\mathrm{mW/cm^2}$ for 60seconds and developed in MF-321 for 90 seconds. Then, the patterned sample was dry-etched to remove nanomembranes not covered by the photoresist. Under the same photoresist pattern, the diamond was etched, using a 790 ICP etcher with the condition (RIE 250W, ICP 0W, CF_4 90sccm, O_2 2sccm and 50mT) until the p- layer of the diamond was fully etched and the p+ layer was exposed. Because there is a huge amount of difference in the resistivity between the p-layer and the p+layer on the surface, surface conductivity on the diamond was used as the criterion to confirm whether the p+ layer was exposed or not. After two etches for 6 minutes in total, the p+ layer of the diamond was fully exposed to the air, and the surface current was measured to be $\sim 10^{-3} A$. Then, the collector was metallized with a metal stack of Ti/Pt/Au (50nm/50nm/100nm). The process was directly followed by RTA of 350℃ for 15 seconds. The fabrication was finalized by passivating the entire sample depositing ALD layers of 80 cycles of $\mathrm{Al_2O_3}$.

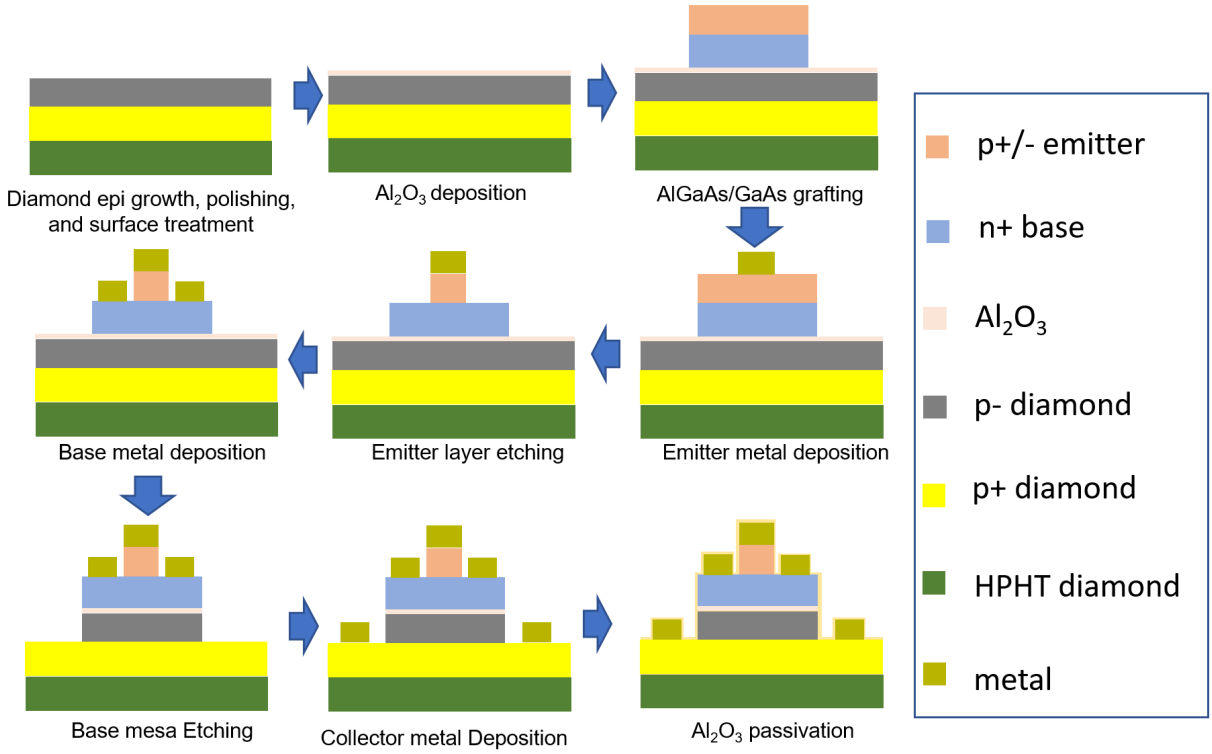

Figure 2.9 *The process flow of p+AlGaAs/n-GaAs/p-diamond DHBT.*

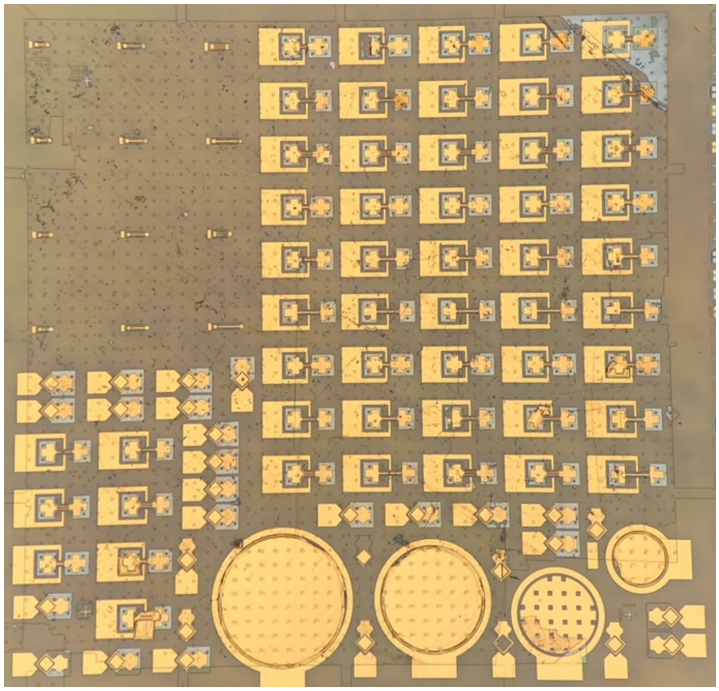

Figure 2.10 *p-AlGaAs/n-GaAs/p-Diamond DHBT.*

2.4 Results

a. AFM of p-GaAs/p-AlGaAs/n-GaAs nanomembranes

The double-flip transfer technique requires the n+ GaAs base layer to be exposed on the top surface of the nanomembrane wafers. One advantage of this fabrication process is the ability to adjust the base layer's thickness by dry-etching the nanomembrane samples before undercutting the sacrificial layers. Since the base layers directly contact the substrates, it is crucial to ensure that dry etching does not degrade the surface roughness. Plasma etching can create dangling bonds on a semiconductor surface, which can act as recombination centers [18]. The surface roughness of the samples before and after dry etching was measured using AFM, as shown in Figure 2.10. The results indicated that the surface quality did decrease, but it was still acceptable for transfer-printing without causing significant degradation to the final devices' performance.

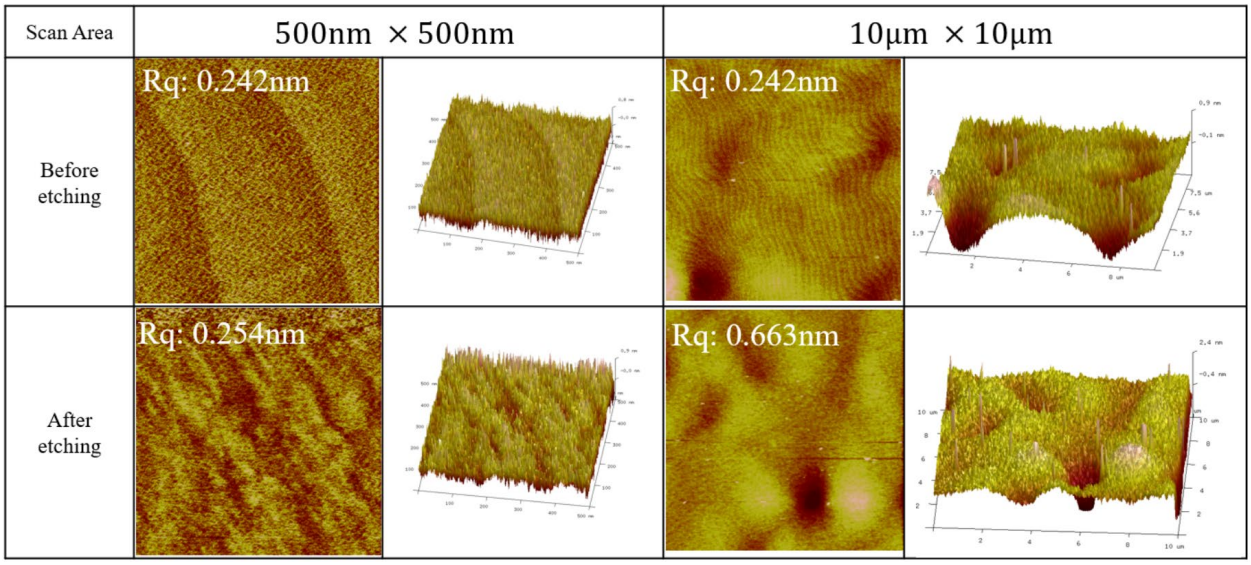

Figure 2.11 *The AFM results of the top surface (a base layer) of nanomembranes before undercut.*

b. CTLM of p-GaAs/p-AlGaAs/n-GaAs nanomembranes

The conductivity of n-GaAs base layers must be low enough to ensure fast switching speed and low thermal loss in bipolar transistors. To measure the surface conductivity of the nanomembranes, a CTLM pattern was deposited on the bare nanomembrane samples, as illustrated in Figure 2.11. Since the base layer thickness can be adjusted before fabrication, the conductivity was measured for various base thicknesses (65nm, 45nm, and 35nm), as shown in Figure 2.12. The results suggest that there is no significant difference in surface conductivity between the different thicknesses, and the current is high enough for use as a base layer in HBTs.

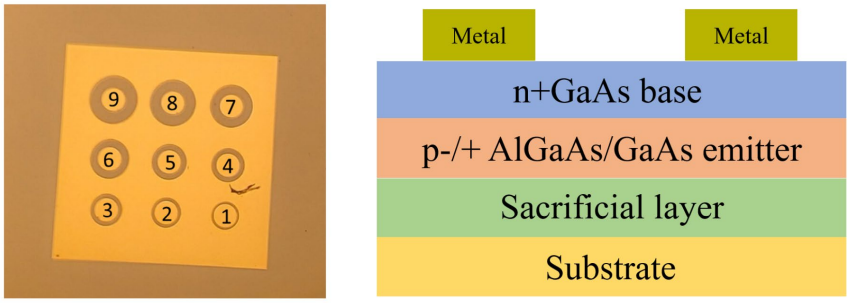

Figure 2.12 *The AFM results of the top surface (a base layer) of nanomembranes before the undercut.*

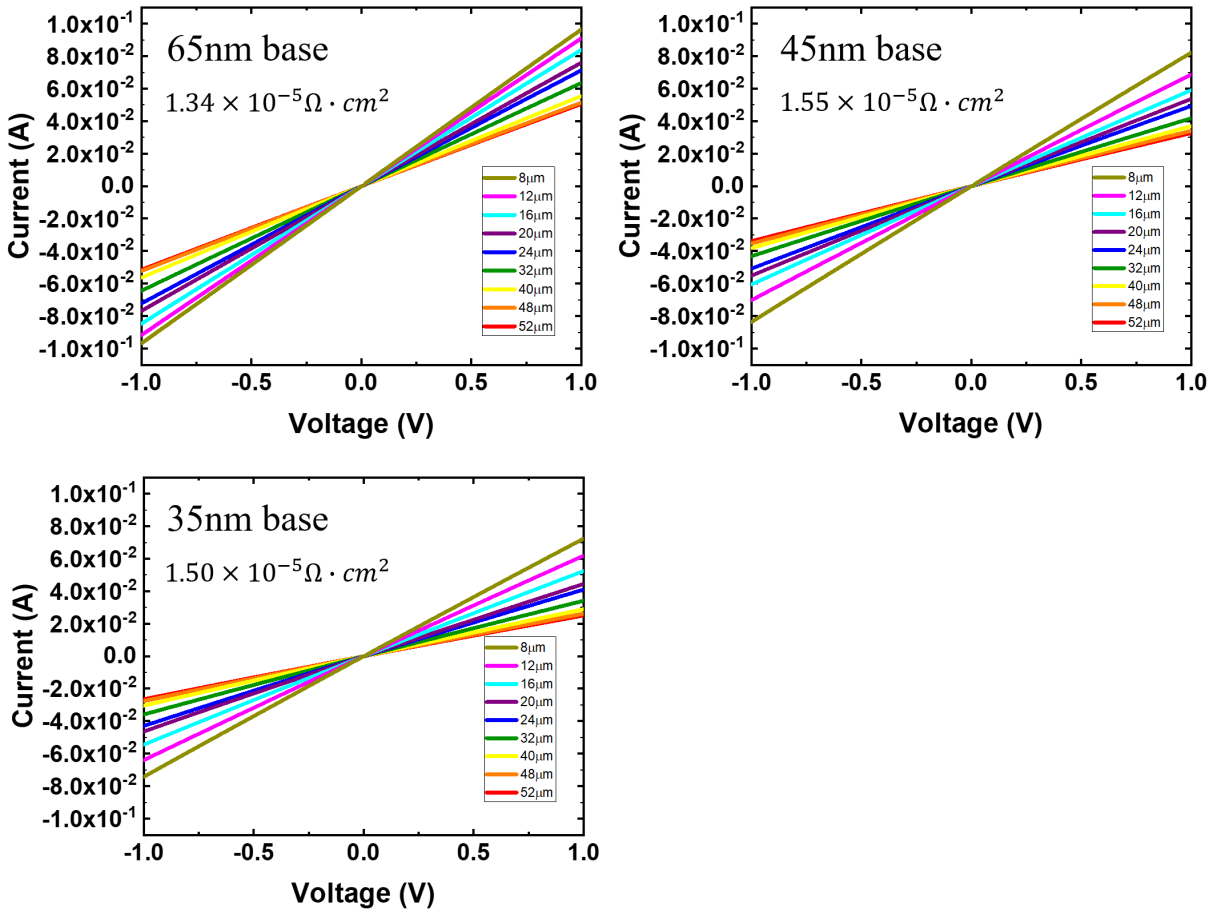

Figure 2.13 *The CTLM results of the samples with the base thickness of (a) 65nm, (b) 45nm, and (c) 35nm.*

c. Emitter-Base Diode IV characteristic of p-GaAs/p-AlGaAs/n-GaAs nanomembranes

As there is a transition layer between the p-AlGaAs (emitter) and n-GaAs (base), shown in Figure 2.13, tests were conducted on silicon substrates to determine the optimal distance from the bottom of the base layer for depositing base metals. This was done to ensure the HBT will have the best emitter-base IV characteristics. The results and test settings are summarized in Figure 2.13 and 2.14. The results showed almost no current in cases where the base metal was metallized 10-20nm apart from the substrate. This could be due to the metal stack being in the depletion region between the n+GaAs base and the silicon substrate. The rectification was optimal when the base metal was deposited slightly above the base layer. Consequently, a 45nm base with metallization at points 45-60nm above the diamond surface was utilized for the actual DHBT fabrication.

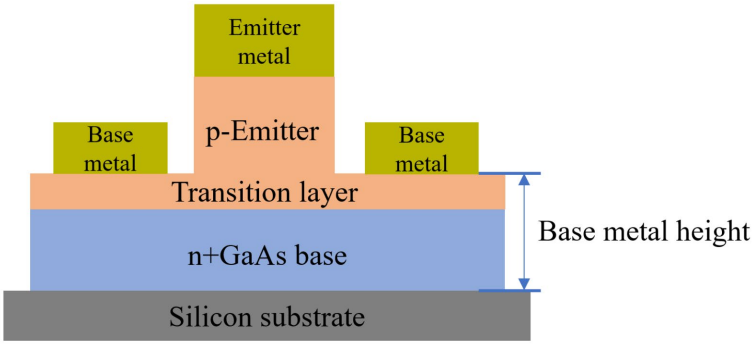

Figure 2.14 *The schematic diagram of EB diode transferred on silicon substrates.*

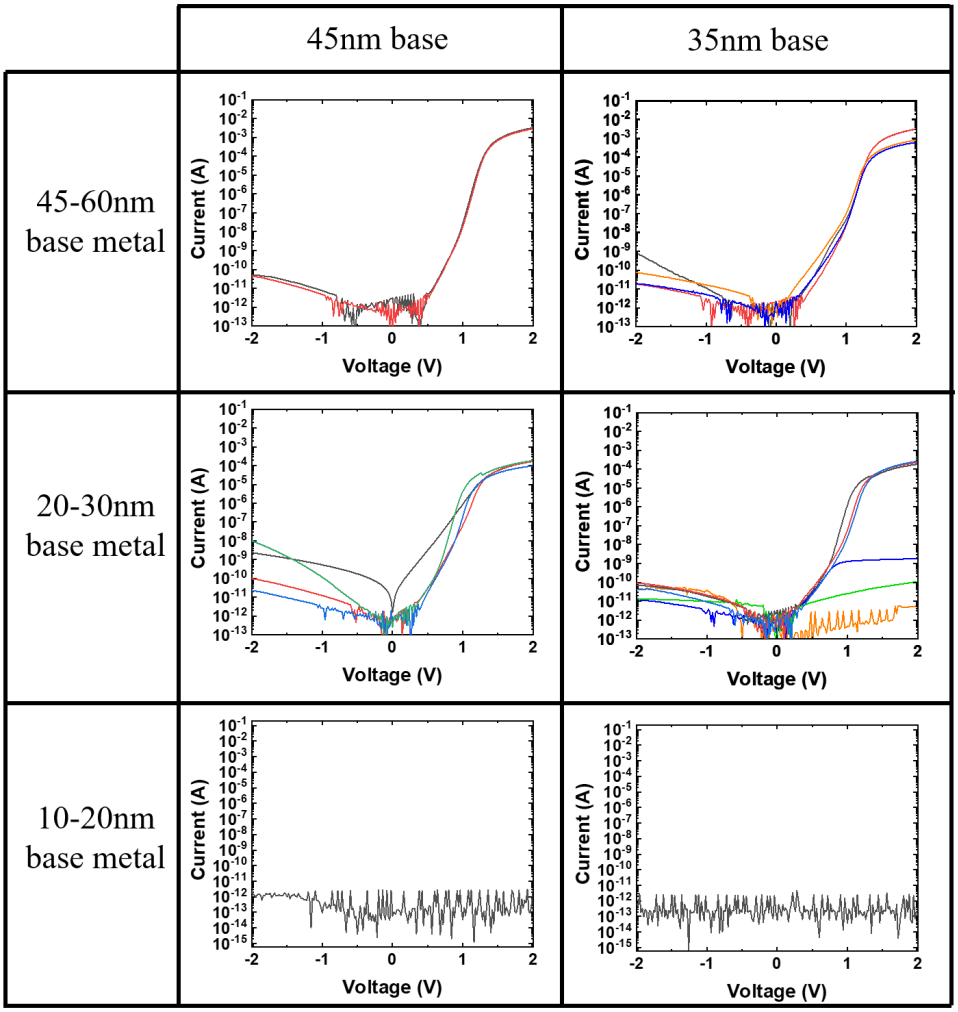

Figure 2.15 *The IV characteristics of EB diodes that have a base of 45nm and 35nm.*

c. AFM of p-diamond substrate

To increase the yield of grafting nanomembranes on substrates, the surface roughness should be low to ensure that the Van-der Waals force between the nanomembranes and the substrates is maximized. The AFM results of the measurements suggest that the surface of the diamond sample is smooth enough to proceed with effective grafting (Figure 2.15 and Figure 2.16).

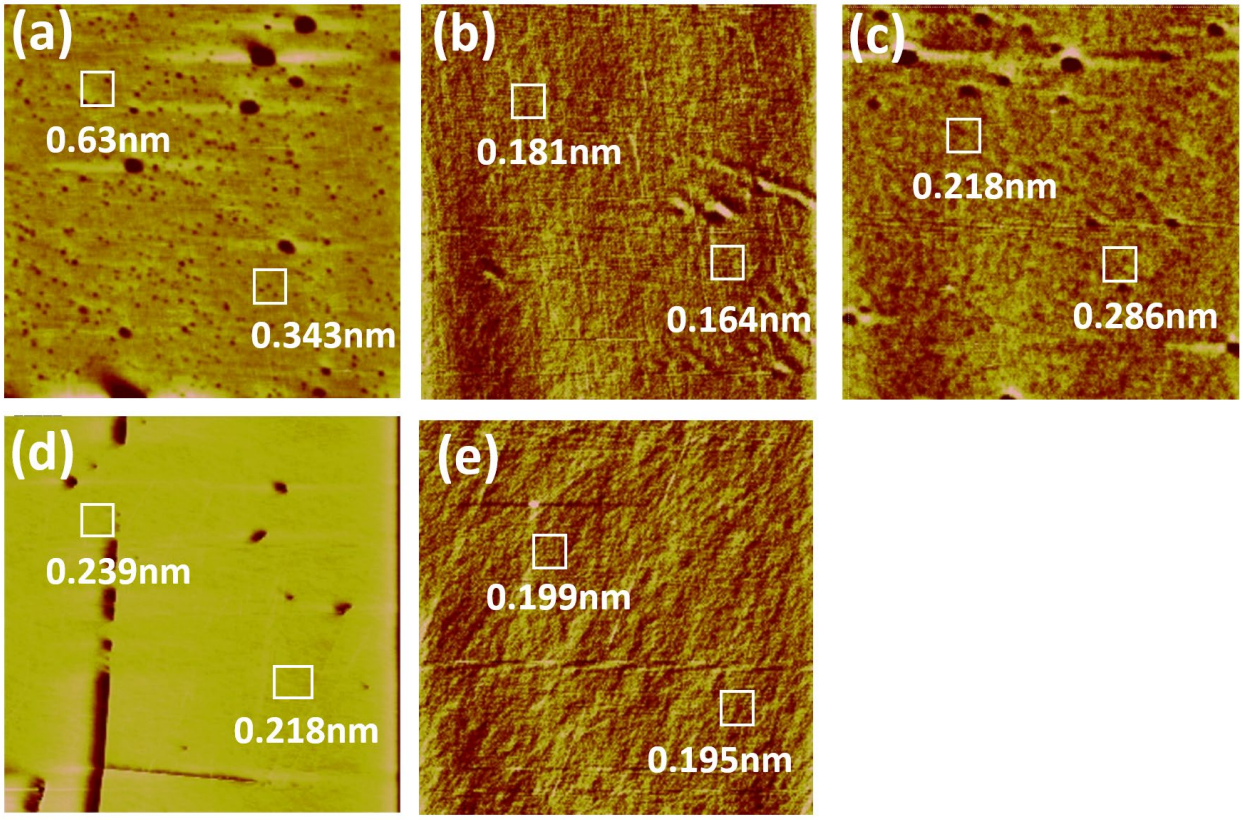

Figure 2.16 *The images of AFM on the diamond surface taken in the areas of* 100μm *by* 100μm. *The white squares of each figure represent the AFM scanning areas of* 10μm *by* 10μm *and the value below each square means the corresponding surface roughness. (a) The upper left side (b) The upper right side (c) The center, (d) The lower left, (e) The lower right side.*

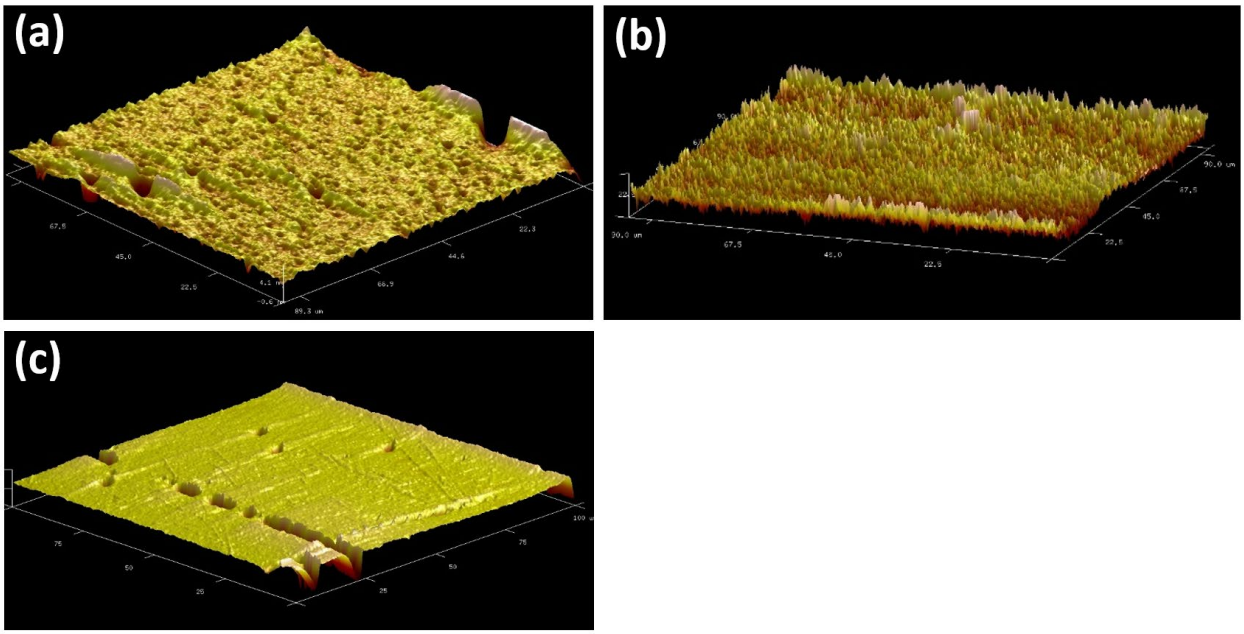

Figure 2.17 *The 3D visualization of the images featured in* ***Figure 2.5****. (a) The upper right side (b), The lower left side (c), and The lower right side.*

d. Engineering of the electron affinity of p-diamond substrate

The diamond sample was sonicated in boiled acid (H_2SO_4:HNO_3 3:1 at 100 °C, 20 minutes) and piranha solutions to clean the surface. The process was followed by ALD of pulsed H_2O at 350 °C to suppress the electron affinity of the diamond sample (Figure 2.4). After treating the diamond, the contact angle of a water drop on the diamond surface was measured to determine the electron affinity, as shown in Figure 2.17. The measured angle of 70.6 degrees suggested that the electron affinity was tuned to 80meV – 100meV which is lower than that of the diamond surface of the prototype of AlGaAs/GaAs/C HBT (0.3eV) [3].

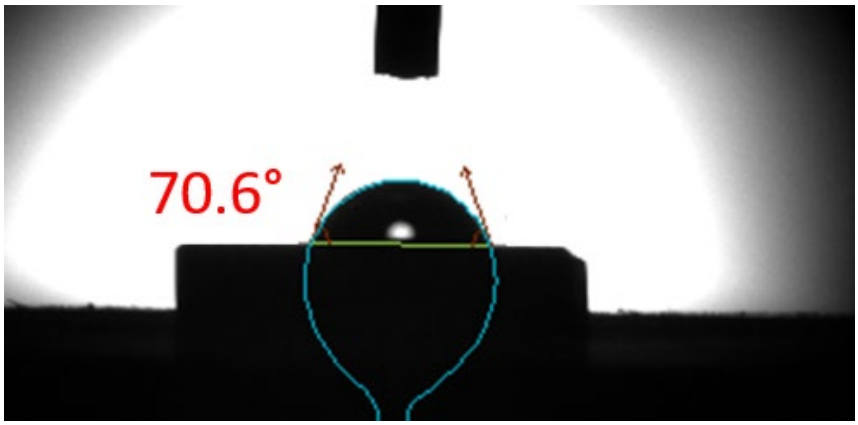

Figure 2.18 *(a) The side view taken when the contact angle with a waterdrop on the diamond substrate in order to estimate the electron affinity of the diamond.*

e. IV characteristics of p+GaAs/p+AlGaAs/n-GaAs/p-diamond

The HBT performance was measured as shown in Figure 2.20. The IF of the emitter-base diode is 2.19, while that of the base-collector diode is 1.71. The I_{on}/I_{off} ratios of emitter-base and base-collector diode are 5.96×10^1 and 2.24×10^4 at $\pm 1V$, respectively. The DC gain was measured to be around ~2000 at the voltage region in which I_b is higher than $10^{-10}A$. This is the first successful HBT of p+GaAs/p+AlGaAs/n-GaAs/p-diamond that could be only possible by utilizing the semiconductor grafting techniques. The high I_{on}/I_{off} ratios and the low IF of the BC diode essentially prove that the semiconductor grafting technique indeed created epitaxy-like bipolar junctions between GaAs and C(diamond), which was not possible by the conventional epitaxy.

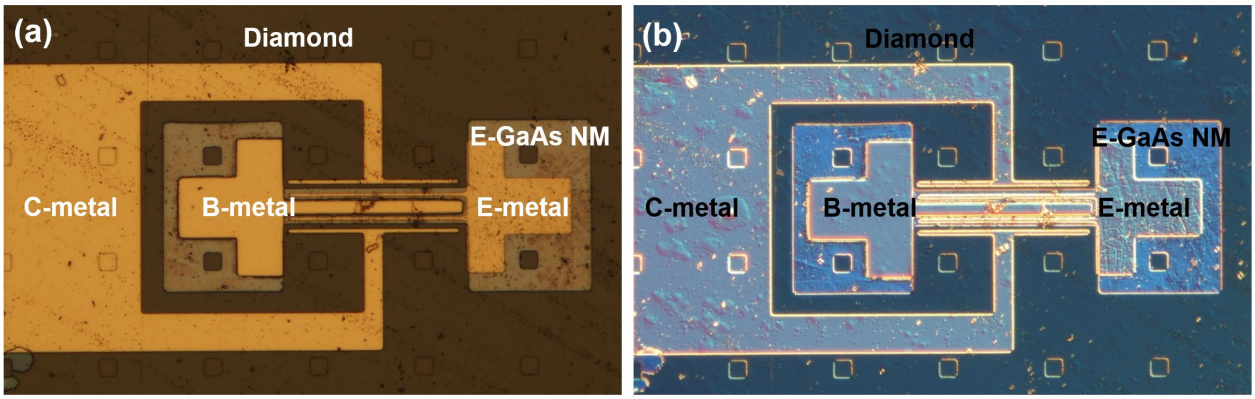

Figure 2.19 *(a) A microscopic image of individual HBT (b) A filtered image of the same HBT.*

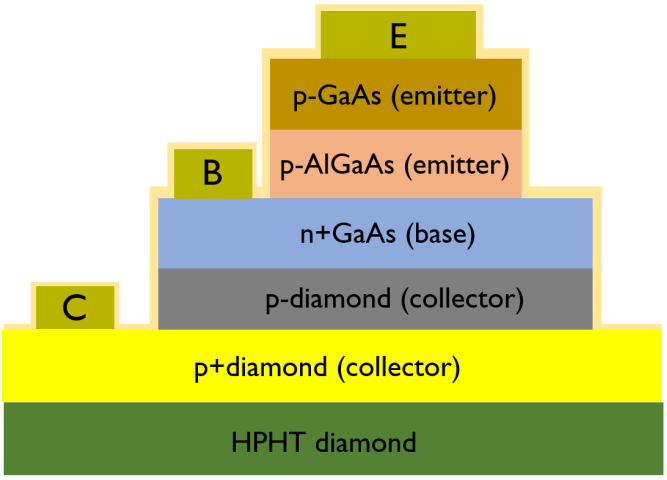

Figure 2.20 *(a) A microscopic image of individual HBT (b) A filtered image of the same HBT.*

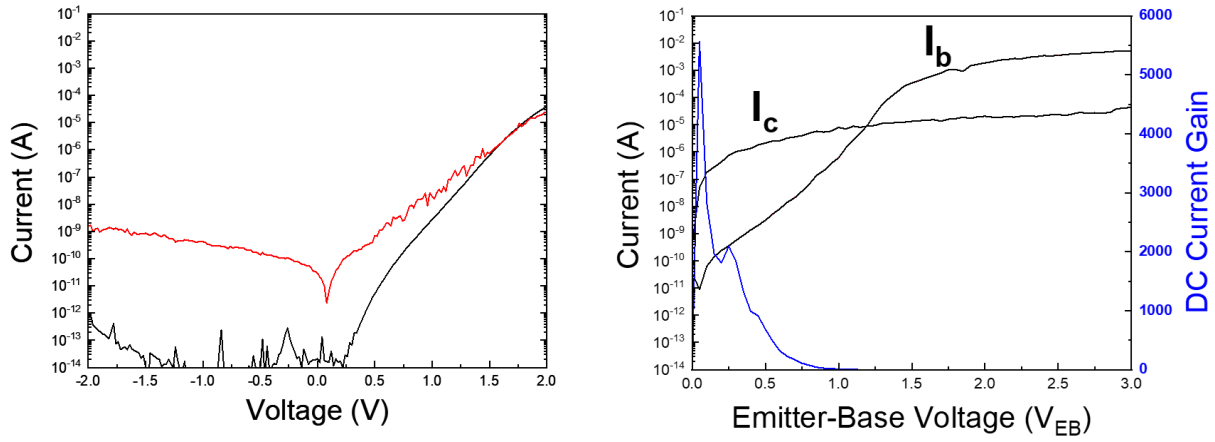

Figure 2.21 *(a) Diode performance (Red – EB diode and Black – BC diode) (b) HBT performance (Offset* $V_{cb} = 0V$*)*

2.5 Conclusion

The first DHBT of p-AlGaAs/n-GaAs/p-diamond has been demonstrated and tested with a record-high DC gain of around 2000 by the semiconductor grafting technique. To successfully fabricate the device, the electron affinity on the diamond substrate needed to be minimized to reduce the discontinuity in the valence band between the diamond substrate and the n+ GaAs layer. After the diamond was treated with chemical cleaning and depositing thin Al_2O_3 layers on the surface, the electron affinity was estimated by measuring the contact angle of a waterdrop placed on the diamond surface. The measurement suggested that the electron affinity of the diamond is tuned to 70-100meV, which produced the discontinuity in the valence band of up to around 80meV, which is lower than that of the previous batch of diamond HBT (~0.3eV) [3]. Then, the AFM was conducted to measure the surface roughness of both the diamond substrate (as a collector) and the n+ GaAs layer (as a base), which confirmed that they were smooth enough to form heterojunctions without significant defects (Figure 2.10 and 2.15). Then, the conductivity of base layers was measured by the CTLM method to ensure that the base layers contain a high concentration of n-type dopants. Then, the optimal base thickness and height of base metals from the substrate were determined by fabricating emitter-base junctions on a dummy substrate. This optimization was only made possible by the inverted nanomembrane structures whose base thickness can be adjusted by plasma etch before the fabrication. For the next step, the inverted structure of nanomembrane wafers was employed to produce the nanomembrane. In this structure, the base layer is exposed on the surface and the emitter layer is between the base layer and the sacrificial layer, unlike the conventional ones (Figure 2.5). In this way, the remaining AlAs sacrificial layer was not present on the base layer which must be kept in high quality without any extra layers for contacting the

diamond collector. To transfer print the nanomembrane of the inverted structure, the double-flip transfer was utilized as featured in Figure 2.6 and 2.7.

One of the fabricated DHBT showed the DC gain of up to 2000 (Table 2.1). However, the emitter-base diode performance demonstrated the low I_{on}/I_{off} ratio, and high IF factor, while the base-collector junction has relatively better diode performance. One of the reason for it is that the nanomembrane had been etched seven different times in order not to over-etch the nanomembrane. This essentially reduced the uniformity of etch, which made the fluctuation of emitter-base diode performance over the sample.

In the future, the device will be measured under high-speed, high-power, and high-temperature environments and its breakdown voltage to test if the device successfully reflects the characteristics of superior UWBG (diamond) and GaAs, including the carrier mobility of both materials and excessive critical field of the diamond material. Also, the yield needs to be higher by optimizing each step of the fabrication.

2.6 References

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Chapter 3

Fabrication and Characterization of AlGaAs/GaAs/GaAsP/GaN DHBT by Nanomembrane Grafting

3.1 Introduction

Gallium nitride (GaN) is one of the most promising materials replacing silicon for power electronics applications owing to its superior characteristics such as the larger band gap, the higher electron saturation velocity, and the excessive critical field compared to those of silicon [1-3]. These characteristics are roughly quantified in a few kinds of Figure of Merit such as Baliga's Figure of Merit(BFOM) [4], Johnson's Figure of Merit(JFOM) [5], and Keyes' Figure of Merit (KFOM) [6]. Even though the FOMs are defined based on the unipolar characteristics of materials, they provide insight into the relative comparison between silicon and large-bandgap materials on material characteristics. For example, Baliga's Figure of Merit(BFOM) of GaN is 846 times as high as that of silicon while Johnson's Figure of Merit(JFOM) is 1089 times that of silicon, which proves that GaN is more desirable than silicon in terms of high-power applications [7]. Despite these superior material characteristics, GaN-based devices have not been able to replace silicon-

based applications fully [1]. One of the reasons is that almost all commercialized GaN devices have been mainly unipolar devices such as FETs and HEMTs [8]. GaN bipolar transistors, such as BJT and HBT that have outstanding performances, have not been demonstrated in the last few decades. The most recent bipolar transistors, their features and IV characteristics are organized in Table 3.1.

There are three main challenges for fabricating GaN bipolar devices that exhibit excellent performances: lacking shallow acceptors [9], low hole mobility, and limited selections of materials for forming heterojunctions with GaN [10]. First, it is challenging to fully ionize acceptors, such as Mg and Zn atoms in bulk GaN due to their high ionization energy. This degrades the electrical performance due to too high resistance for high-speed and high-power applications. Even if hole concentrations are sufficient in bulk GaN, the bipolar devices suffer from low hole mobility [11], decreasing switching speed and increasing power loss in channels and noise signals in high-frequency operations [12]. Furthermore, the most critical challenge in demonstrating superior bipolar devices is a lack of selection of materials to form heterojunctions with GaN. Because of this requirement for a lattice match in the conventional method to form heterojunction—continuous epitaxy, the compound III-V materials such as InGaN and AlGaN have been almost exclusively integrated into GaN HBT systems, as shown in Table 3.1. If materials with different lattice structures, such as GaAs and silicon, are grown on GaN substrates, high-quality heterojunctions with a low density of states cannot be obtained because an abrupt difference in the lattice parameters creates dislocation defects and an enormous amount of dangling bonds on the surface [13].

In this chapter, the novel approach to resolve those difficulties in the fabrication of GaN bipolar devices is introduced—the semiconductor grafting technique [10]. Then, HBT that utilizes

GaN as a collector, GaAs/GaAsP as a base, and AlGaAs as an emitter is designed and demonstrated to achieve high DC gain. Because of the high degree of freedom in choosing materials for combinations of heterojunctions, the GaAs-compound material system (GaAsP and AlGaAs) has been selected solely for the sake of material characteristics [14]. In DHBT employing n-GaN as a collector, p-GaAs is the ideal choice for a base layer because it has higher electron mobility than AlGaN and InGaN. To reduce the discontinuity in the conduction band between GaAs and GaN, p-type graded GaAsP is additionally used between those materials because GaAsP has a lower electron affinity. Moreover, the material system of AlGaAs/GaAs, which is one of the most mature heterojunctions, can be fully utilized by adopting n-AlGaAs as an emitter layer in the GaN HBTs. As a result, the successfully demonstrated n-AlGaAs/p-GaAs/p-GaAsP/n-GaN DHBTs have shown the DC gain of up to 80 under low offset of V_{cb} (1V). Also, the BC diode performances of outstanding quality (the ideality factor of 1.10 and the on/off ratio of 1.84×10^8) in the DHBT prove that the abrupt heterogeneous junctions between GaAsP and GaN are at an excellent level that could neither be achieved by the conventional epitaxy nor by wafer-bonding. To accomplish fabrication of the AlGaAs/GaAs/GaAsP/GaN DHBT, two significant difficulties have been solved: reducing discontinuity in the conduction band between GaAs and GaN and releasing nanomembranes of fragile AlGaAs/GaAs/GaAsP.

The conduction band of a surface of GaN bends upward because of the polarity in bulk c-plane GaN. Upward band-bendings were measured by XPS results on the surface of GaN substrates [15]. Because of the abrupt heterogeneous junction between GaN and GaAs, the discontinuity in the conduction band essentially hampers electrons in the p-type GaAs layer from being collected by GaN. To reduce band bending, two methods have been adopted for successful fabrication. First, graded p-type GaAsP have been used between the p-type GaAs layer and the

GaN substrate. By doing so, the electron affinity of the base side lowers to compensate for the upward band bending on the collector side. Second, the upward band-bending may have been suppressed by featuring a thin high-doped layer on the surface of a low-doped layer, as shown in Figure 3.1.

On the other hand, releasing nanomembranes of AlGaAs/GaAs/GaAsP and transfer-printing them on the GaN substrates are highly tricky compared to those of both AlGaAs/GaAs and single GaAs layer because of the enormous difference in lattice parameters between GaAs and GaAsP. The difference in the lattice parameters between GaAs and $GaAs_{0.5}P_{0.5}$ is roughly 0.1 Å (1.8%) [16], whereas the difference between those of GaAs and $Al_{0.3}Ga_{0.7}As$ is ~0.002 Å (0.04%). The large difference makes the nanomembranes mechanically unstable and fragile in HF solution used for wet-etching of AlAs sacrificial layers. To overcome this challenge, a highly diluted HF solution (1:3200) was employed to wet-etch AlAs sacrificial layers. Moreover, the unique trick of cleaning picked-up nanomembranes on PDMS stamps has been developed to prevent water surface tension from breaking nanomembranes, which will be introduced later. As a result, free-standing nanomembranes of AlGaAs/GaAs/GaAsP have been successfully undercut and transfer-printed on the GaN substrates to achieve the world's first HBT of n-AlGaAs/p-GaAs/p-GaAsP/n-GaN.

In this chapter, all the demonstrated devices of GaN have been introduced and analyzed with their IV characteristics: Si/GaN diode, GaAs/GaN diode, AlGaAs/GaAs/GaN HBT and AlGaAs/GaAs/GaAsP/GaN DHBT. The goal is to test material properties and optimize the fabrication conditions which eventually would be used for the HBT fabrication. The list of the fabricated devices is presented in Tabl 3.4 in chronological order. First, the p-Si/n-GaN diodes were fabricated with well-characterized p-type silicon nanomembrane and the four NGC GaN and the KAUST GaN to test the IV-characteristics of the GaN samples. For the Si/KAUST GaN

samples, various conditions of ALD were chosen to compare the diode performances. Then, the nanomembranes of NGC p-GaAs were grafted on the four NGC GaN substrates to test the IV characteristics of the BC junctions of the target HBTs. After finishing the fabrications of all the diode devices, the first HBT sample was made by utilizing the NGC EB n-AlGaAs/p-GaAs nanomembranes and the NGC GaN substrates. The second batch of HBT immediately followed up by employing n-AlGaAs/p-GaAs/GaAsP as a nanomembrane and the NGC/Cree/KAUST6 GaN samples with various interface treatments. After completing the fabrication job of each device, the IV-characteristics were carefully measured by Keithley Analyzer.

Table 3.1. *The state-of-the-art transistors utilizing GaN with their key characteristics and performances.*

#	Device type	Doping [cm^{-3}]	Structures	J_c Current density [A/cm^2] or I_c Current [mA]	Gain	Breakdown voltage	Ref
1	BJT	E(n): 5×10^{17} B(p): 1.5×10^{17} C(n): 5×10^{17}	E: n-GaN B: p-GaN C: n-GaN	$I_c = 4.75mA$ $V_{ce} = 4V$ $I_b = 470\mu A$	10-40 $V_{cb} = 2V$	$12V$	Suzuki[17]
2	BJT	E(n): 4×10^{18} B(p): 2×10^{19} C(n): 2×10^{16}	E: n-GaN B: p-GaN C: n-GaN	$I_c = 20mA$ $V_{ce} = 10V$ $I_b = 5mA$ @RT	6 $V_{cb} = 0V$ @RT	N/A	Mishra[18]
3	HBT	E(n): 5×10^{18} B(p): 1×10^{19} C(n): 5×10^{16}	E: n-AlGaN B: p-GaN C: n-GaN	$I_c = 800mA$ $V_{ce} = 15V$ $I_b = 350\mu A$	3 $V_{cb} = 0V$	N/A	Mishra[19]
4	HBT	E(n): 1.6×10^{18} B(p): 5.9×10^{17} C(n): 1×10^{17}	E: n-AlGaN B: p-GaN C: n-GaN	$J_c = 8000A/cm^2$ $V_{ce} = 6.5V$ $I_b = 400\mu A$	90 $V_{cb} = 0V$	$98V$	Zhang[20]
5	HBT	E(p): 3×10^{19} B(n): 4×10^{18} C(p): UID	E: p-AlGaN B: n-GaN C: p-GaN	$I_c = 0.8mA$ $V_{ce} = 10V$ $I_b = 30\mu A$ @50℃	38 @RT	$>40V$ @590℃	Makimoto[21]
				$I_c = 0.5mA$ $V_{ce} = 10V$ $I_b = 700\mu A$ @590℃	3 @590℃		
6	HBT	E(n): 1×10^{18} B(p): 2×10^{19} C(n): 6×10^{15}	E: n-AlGaN B: p-GaN C: n-GaN	$I_c = 17mA$ $V_{ce} = 20V$ $I_b = 1mA$ @RT	20 $V_{cb} = 0V$ @RT	N/A	Mishra[22]
7	HBT	E(n): 5×10^{18}	E: n-AlGaN	N/A	100	N/A	Dupuis[23]

		B(p): 2×10^{17} C(n): 9×10^{16}	B: p-GaN C: n-GaN				
8	HBT	E(n): 1×10^{18} B(p): 2×10^{19} C(n): 5×10^{15}	E: n-AlGaN B: p-GaN C: n-GaN	$J_c = 800A/cm^2$ $V_{ce} = 20V$ $I_b = 500\mu A$	35 $V_{cb} = 0V$	$> 330V$	Mishra[24]
9	HBT	E(p): 3×10^{19} B(n): 1×10^{18} C(p): 4×10^{18}	E: p-AlGaN B: n-GaN C: p-GaN	$I_c = 1.25mA$ $V_{ce} = 15V$ $I_b = 50\mu A$	40 $V_{cb} = 65V$	$194V$	Makimoto[25]
10	HBT	E(p): 3×10^{19} B(n): 1×10^{19} C(p): UID	E: p-AlGaN B: n-GaN C: p-GaN	$I_c = 60\mu A$ $V_{ce} = 4V$ $I_b = 5\mu A$ @RT	20 @RT	N/A	Kobayashi[26]
				$I_c = 280\mu A$ $V_{ce} = 4V$ $I_b = 5\mu A$ @300℃	100 @300℃		
11	DHBT	E(n): 4×10^{19} B(p): 1×10^{19} C(n): 2×10^{17}	E: n-GaN B: p-InGaN C: n-GaN	$I_c = 7mA$ $V_{ce} = 12V$ $I_b = 500\mu A$	20 $V_{cb} = 5V$	N/A	Kobayashi[27]
12	DHBT	E(n): 1×10^{19} B(p): 1×10^{18} C(n): 1×10^{17}	E: n-GaN B: p-InGaN C: n-GaN	$J_c = 2800A/cm^2$ $V_{ce} = 5V$ $I_b = 500\mu A$ @RT	80 $V_{cb} = 0V$	90 @RT	Shen[28]
				$J_c = 600A/cm^2$ $V_{ce} = 5V$ $I_b = 500\mu A$ @250℃		$157V$ @257℃	
13	DHBT	E(n): 1×10^{19} B(p): 4×10^{18} C(n): 1×10^{17}	E: n-GaN B: p-InGaN C: n-GaN	$J_c = 16500A/cm^2$ $V_{ce} = 5V$ $I_b = 100\mu A$	100 $V_{cb} = 0V$ @RT	$105V$	Shen [29]
					50 $V_{cb} = 0V$ @150℃		
					37 $V_{cb} = 0V$ @250℃		
14	DHBT	E(n): 4×10^{19} B(p): 2×10^{19} C(n): 1×10^{17}	E: n-GaN B: p-InGaN C: n-GaN	$I_c = 50mA$ $V_{ce} = 10V$ $I_b = 50\mu A$	2000 $V_{cb} = 0V$	N/A	Kobayashi[30]
15	DHBT	E(n): 4×10^{19} B(p): 2×10^{19} C(n): 1×10^{17}	E: n-GaN B: p-InGaN C: n-GaN	$I_c = 65mA$ $V_{ce} = 12V$ $I_b = 50\mu A$ @RT	2000 @RT	N/A	Makimoto[31]
				$I_c = 80mA$ $V_{ce} = 12V$ $I_b = 500\mu A$ @300℃	300 @300℃		

3.2 Materials and Characterization

Devices/Materials

Six batches of GaN substrates that were grown from three different institutes were used, while four different batches of nanomembranes were utilized for the fabrications.

Table 3.2. *The list of nanomembrane wafers used in the research.*

NM	Layer	Material	Thickness(Å)	Doping(cm^{-3})
NM1 (Si)	**P+**	Si	1800	$p : 5 \times 10^{19}$ (Boron)
	Sacrificial layer	SiO_2	4000	-
	Substrate	Si	-	-
NM2 (GaAs)	**Base**	GaAs	4000	$p : 4 \times 10^{19}$
	Sacrificial layer	$Al_{0.95}Ga_{0.05}As$	3000	UID
	Substrate	GaAs	-	-
NM3 (AlGaAs/ GaAs)	**GaAs Emitter Cap**	GaAs	1000	$n : 6 \times 10^{18}$
	BE Grade Down	AlGaAs	300	$n : 7.14 \times 10^{17}$
	Emitter	$Al_{0.30}Ga_{0.70}As$	1200	$n : 7.14 \times 10^{17}$
	BE Grade Up	AlGaAs	300	$n : 7.14 \times 10^{17}$
	GaAs Spacer	GaAs	25	$n : 5 \times 10^{17}$
	Base	GaAs	800	$p : 4 \times 10^{19}$
	Sacrificial layer	$Al_{0.95}Ga_{0.05}As$	3000	-
	Substrate	GaAs	-	-
NM4 (AlGaAs /GaAs /GaAsP)	**GaAs Emitter Cap**	GaAs	1000	$n : 6 \times 10^{18}$
	BE Grade Down	AlGaAs	300	$n : 7.14 \times 10^{17}$
	Emitter	$Al_{0.30}Ga_{0.70}As$	1200	$n : 7.14 \times 10^{17}$
	Be Grade Up	AlGaAs	320	$n : 7.14 \times 10^{17}$
	Base	GaAs	500	$p : 4 \times 10^{19}$
	Base	0-50% GaAsP	300	$p : 1 \times 10^{17}$
	Sacrificial layer	$Al_{0.95}Ga_{0.05}As$	3000	-
	Substrate	GaAs	-	-

Table 3.3. *The list of GaN wafers used in the research.*

Substrate	**Layer**	**Material**	**Thickness(Å)**	**Doping(cm^{-3})**
GaN1 (NGC)	**N-**	Ga-rich GaN	2500	UID
	N+	N-rich GaN	2000	n+ : 6×10^{19}
	AlN Nucleation	AlN	-	-
	Substrate	SiC	-	-
GaN2 (NGC)	**N-**	Ga-rich GaN	2500	UID
	N+	N-rich GaN	2000	n+ : 6×10^{19}
	AlN Nucleation	AlN	-	-
	Substrate	SiC	-	-
GaN3 (NGC)	**N-**	N-rich GaN	2500	UID
	N+	N-rich GaN	2000	n+ : 6×10^{19}
	AlN Nucleation	AlN	-	-
	Substrate	SiC	-	-
GaN4 (NGC)	**N-**	Ga-rich GaN	2000	n- : 5×10^{17}
	N+	N-rich GaN	2000	n+ : 6×10^{19}
	AlN Nucleation	AlN	-	-
	Substrate	SiC	-	-
GaN5 (KAUST)	**N-**	N-rich GaN	2500	n- : 1×10^{18}(Si)
	N+	N-rich GaN	15500	n+ : 2×10^{19}(Si)
	Substrate	Sapphire	-	-
GaN6 (Cree)		GaN	2000	Grade down $1 \times 10^{19} \sim 1 \times 10^{17}$
	N-	GaN	2000	1×10^{17}
		GaN	3000	Grade up $1 \times 10^{17} \sim 2 \times 10^{19}$
	N+	GaN	11000	2×10^{19}
	Substrate	Sapphire	-	-

Table 3.4. *The list of devices demonstrated.*

Device type	Materials	Interface	Note
Diodes	Si/GaN5 (KAUST)	5c Al_2O_3	Reference for interface condition of AlN
	Si/GaN5 (KAUST)	10c Al_2O_3	Reference for interface condition of AlN
	Si/GaN5 (KAUST)	3c AlN /10c Al_2O_3	Test of the new ALD condition
	Si/GaN5 (KAUST)	9c AlN /10c Al_2O_3	Test of the new ALD condition
	Si/GaN1 (NGC)	5c Al_2O_3	Test of GaN grown at NGC

	Si/GaN2 (NGC)	5c Al_2O_3	Test of GaN grown at NGC
	Si/GaN3 (NGC)	5c Al_2O_3	Test of GaN grown at NGC
	Si/GaN4 (NGC)	5c Al_2O_3	Test of GaN grown at NGC
HBT	AlGaAs/GaAs/GaN3(NGC)	5c Al_2O_3	No band-bending suppression
	AlGaAs/GaAs/GaAsP/GaN4(NGC)	20c Al_2O_3	Band-bending suppressed by ALD
	AlGaAs/GaAs/GaAsP/GaN5(KAUST)	UV Ozone 3min 20c Al_2O_3 UV Ozone 3min	Band-bending suppressed by ALD/UV Ozone and high doping on GaN Band-bending: upward -0.112eV
	AlGaAs/GaAs/GaAsP/GaN6(Cree)	20c Al_2O_3	Band-bending: upward 0.053eV

3.3 Methods of Fabrication

a. Dicing Wafers for Nanomembrane and Substrates

Wafer of nanomembranes (silicon, GaAs, GaAs/GaAs, AlGaAs/GaAs/GaAsP):

The wafers of nanomembranes are 6 inches-sized (silicon) and 2 inches-sized (others). The samples were diced into square-shaped pieces of 4mm by 4mm, using ZH05 blades.

Wafer of GaN substrates (GaN5: KAUST, GaN6: Cree):

The samples were diced into square-shaped pieces of 6mm by 6mm, using R07 blades (GaN5: KAUST, GaN6: Cree) or VT07 blades(GaN1~4: NGC). Before dicing the samples, photoresists were coated onto the wafers to protect the surfaces from dust generated by dicing.

b. Preparation of GaN Substrates

The square pieces of GaN were ultra-sonicated in acetone and IPA for ten minutes, respectively. Then, the samples were manually scrubbed by Q-tips in acetone and IPA followed by being rinsed with water and dried with an N2 gun thoroughly. These steps are meant to remove dust and particles mechanically before proceeding into the chemical cleaning. For chemical

cleaning, the samples were dipped into Piranha solutions of 1:3 ratio of hydroperoxide and sulfuric acid. After ten minutes past, the samples were taken out and rinsed with water. The next step was to dip into a mixture of ammonium hydroxide, hydroperoxide and DI water (1:1:5) for ten minutes. Then, they were put into a solution of diluted hydrochloric acid (50%) for ten minutes. Finally, the samples were briefly dipped into a diluted hydrofluoric acid (25%) for one minute. Right after finishing the process of chemical cleaning, the samples were carefully carried into a bag of nitrogen to minimize the exposure to moist and oxygen in air. Then, the samples were treated with UV/Ozone for three minutes by using UV/Ozone Cleaner in NFC (only for KAUST 6) for 0.5ss. Right after cleaning with ozone and UV, the samples were taken to the glove box in which the Savannah ALD system is installed. Al2O3 was deposited on the substrates with TMA and water pulses of 20 cycles.

c. Preparation of Nanomembrane and Grafting Process

The samples were coated with S1813 by spinning at 2500rpm for thirty seconds, and baked for three minutes at 105C. Then, the nanomembrane pattern was exposed to UV light of 5.5mW for one minute and the samples were developed with being dipped in MF321 for one minute. The patterned nanomembrane samples were dry etched by using a Plasma Therm SLR series inductivley coupled plasma etcher (NGC EB GaAs/ p+GaAs/ GaAsP) or a 790 RIE etcher (Si NM) to punch through the holes to expose sacrificial layers of AlAs (SiO2) in the samples.

Silicon nanomembranes: The samples were brought into a diluted HF solution (1:1 = HF(49%) : DI water). Every one hour of undercut inside the HF solution, the SOI samples needed to be taken out and put into acetone for twenty minutes to make sure that HF spread underneath the nanomembranes. After 2 to 3 hours of undercut, the nanomembranes were fully etched. The

undercut samples were dipped into DI water to rinse the surface, and the nanomembranes were picked up by a piece of PDMS.

AlGaAs/GaAs and AlGaAs/GaAs/GaAsP nanomembranes: The samples were wet-etched inside a highly diluted HF solution. The optimized undercut recipe varies a lot by the thickness and compound ratio of nanomembranes. When they were taken out of the solution, the edge of a sheet of wiper was utilized to soak the HF solution. Then, the wet-etched sample was picked up by a piece of PDMS. After picking up with PDMS, residue of undercut on the nanomembranes must be removed with MF321.

(NGC EB GaAs / NGC p+GaAs) For these samples, a few drops of MF321 were dropped on the nanomembrane sitting on a piece of PDMS. Then, MF321 drops were removed by pipettes and dried by nitrogen wind. Then, the same procedure was repeated with DI water.

(NGC GaAsP) For the GaAsP sample, the lattice mismatch between GaAs and GaAsP layers makes the nanomembrane very fragile enough to be broken by a drop of MF321. Thus, a sheet of wiper was carefully placed on a PDMS stamp with a nanomembrane, and a drop of MF321 was dropped on the very spot onto the wiper. As soon as the sheet of wiper soaked the MF321 drop, the sheet was removed quickly. This method preserved the mechanical stability of highly fragile nanomembranes. The picked-up and cleaned nanomembranes on the PDMS piece were gently attached to the GaN substrates that had been treated beforehand by using the MJB aligner. After ten minutes past, the PDMS was carefully detached and removed by hands. The grafted nanomembranes on the substrates were annealed for five minutes at 350℃ through RTA.

d. Metallization and Dry etching

After successfully printing nanomembranes on the substrates, the HBT fabrication began with the emitter metal deposition (Pd/Ge/Au 30/40/100nm) on the GaAs Emitter cap layer. Copper must not be used for emitter metal because it burns easily when being plasma etched at the next step. Without spin-coating any photoresists, the samples GaAs nanomembranes were etched by using the Plasma Therm SLR series inductively coupled plasma (ICP) etcher to make the base layer of p+GaAs (or p+GaAsP) exposed for metallization. Because the margin of etching was so small at this step, extra cautions needed to be paid to make sure the exact amount of GaAs would be etched. After the base etch, the metal stacks of base (Ti/Pt/Au 15/30/100) were deposited. During the process, the quality of metal stacks of emitter and base had been confirmed to be sounding by measuring emitter to emitter and base to base IV characteristics. Furthermore, the EB diode performance was measured to make sure that the fabrication was all right. Then, the base-mesa etch followed the previous steps for metallization. The nanomembrane was fully removed by the same dry etch, then the GaN substrates were etched until the n+ layer of the substrates were completely exposed. The target amounts of etch were decided based on the SIMS data of each GaN substrate. The collector metal stacks (Ti/Al/Ti/Au 20/100/45/100nm) were deposited on the n+ GaN layer.

e. Passivation

The fabricated HBT devices were passivated at 250℃ with 80cycle of Al_2O_3.

3.4 Results

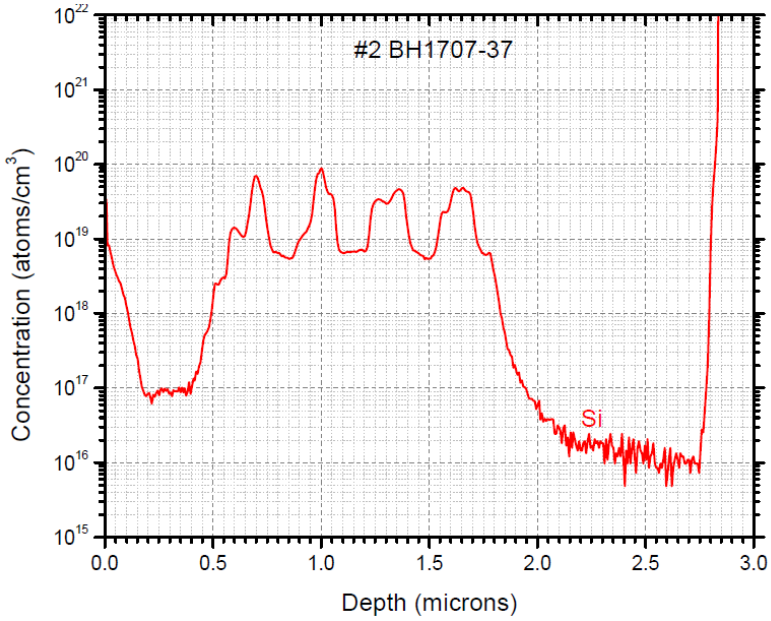


Figure 3.1. *The SIMS data of GaN6 (Cree).*

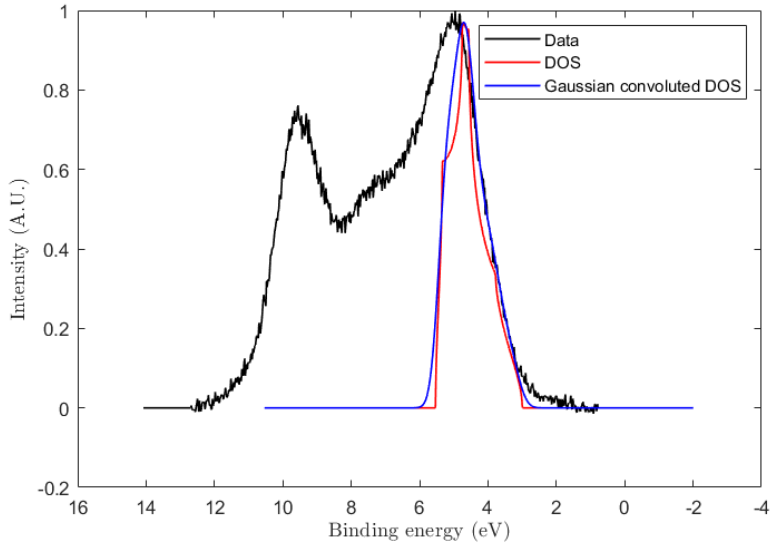


Figure 3.2. *The XPS data of GaN6 (Cree) after surface treatment. (Pass energy: 10eV, spot size: 400μm, dweel time : 40s, step: 0.02eV, C reference.) The XPS results determines that the upward band-bending is around 0.413eV when it is not treated. [15]*

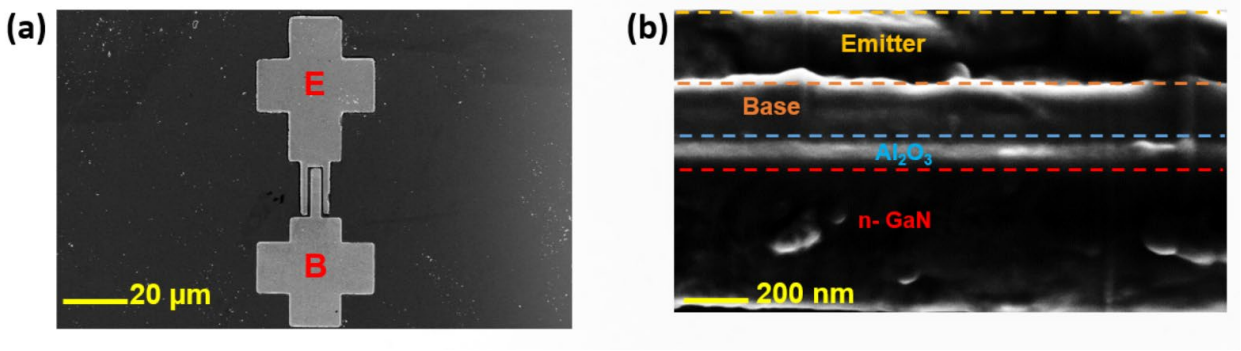
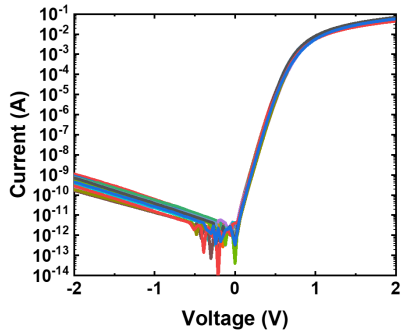
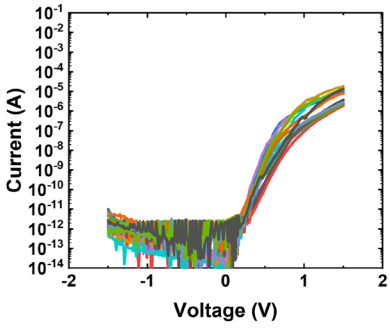
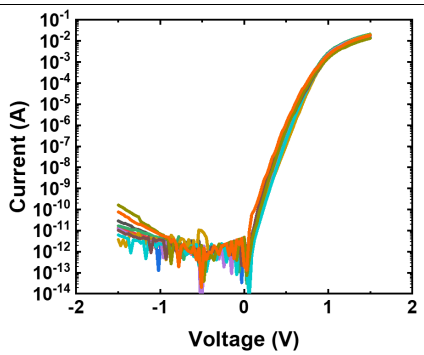
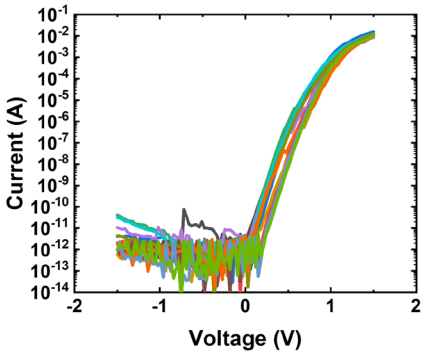
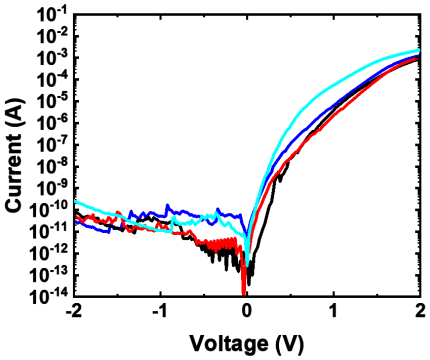
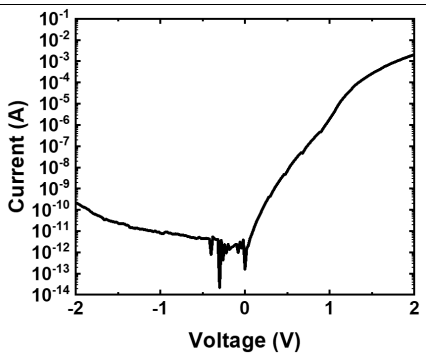
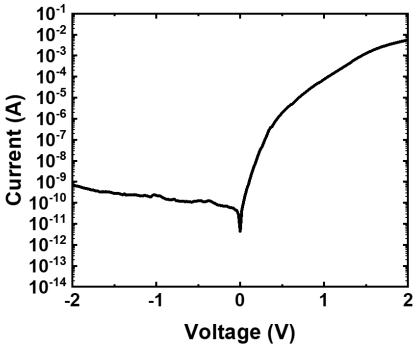


Figure 3.3. *(a) SEM Top view image of the device (b) the cross-sectional image.*

Table 3.5. *The IV characteristics of the diodes fabricated.*

Diodes	Interface	IV-characteristics
Si/GaN5 (KAUST)	5cycles Al_2O_3	
Si/GaN5 (KAUST)	10cycles Al_2O_3	
Si/GaN5 (KAUST)	3cycles AlN /10cycles Al_2O_3	

Si/GaN5 (KAUST)	9cycles AlN /10cycles Al_2O_3	
Si/GaN1 (NGC)	5cycles Al_2O_3	
Si/GaN2 (NGC)	5cycles Al_2O_3	
Si/GaN3 (NGC)	5cycles Al_2O_3	

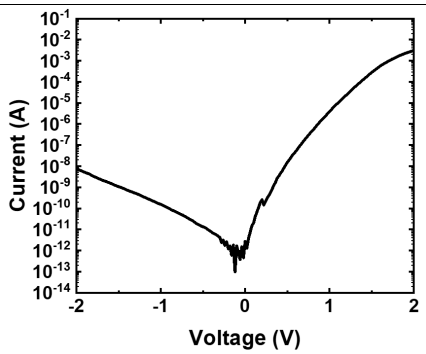
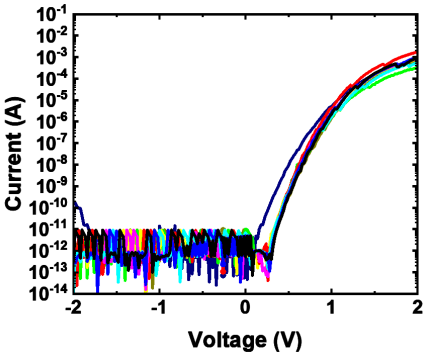
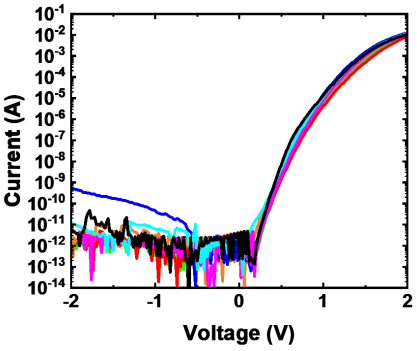
Si/GaN4 (NGC)	5cycles Al_2O_3	
GaAs/GaN3 (NGC)	5cycles Al_2O_3	
GaAs/GaN4 (NGC)	5cycles Al_2O_3	

Table 3.6. *The IV characteristics of the HBTs fabricated.*

<table>
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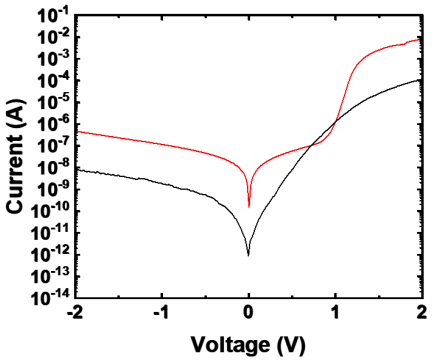
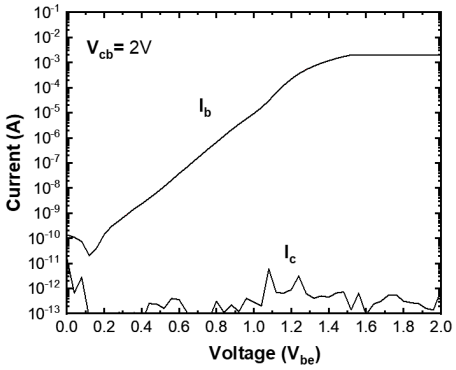
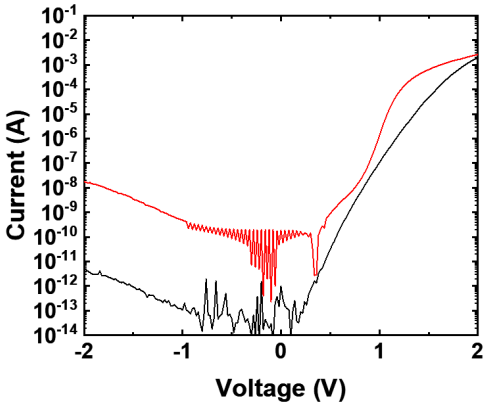
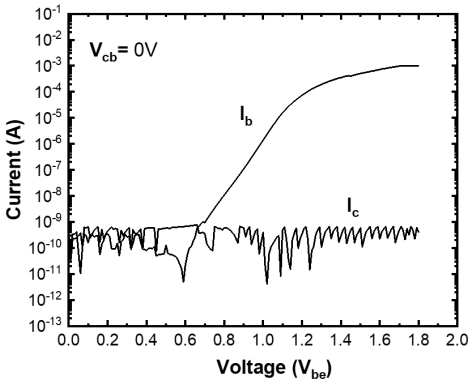
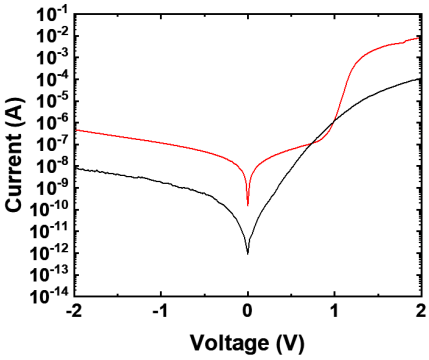
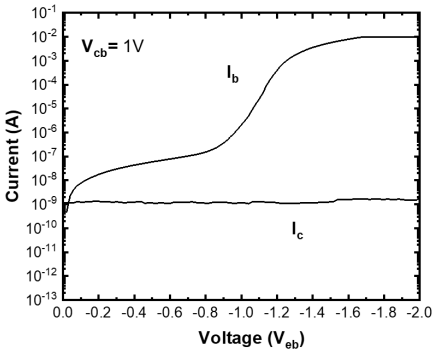
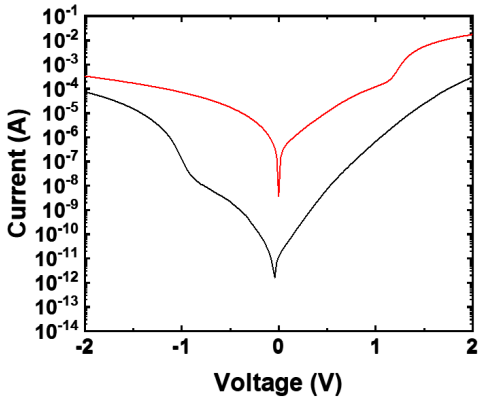
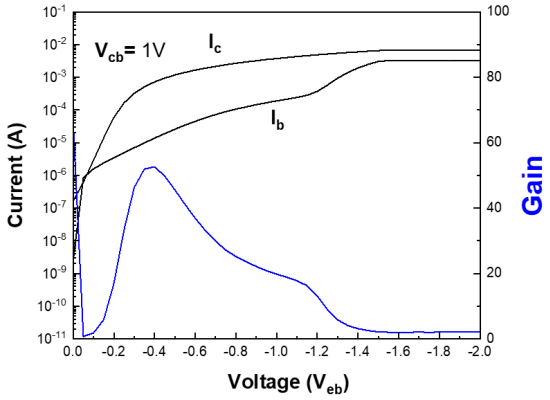
<tr><td>Diode Performance</td><td>HBT
Performance</td></tr>
<tr><td> 
</td><td> 
</td></tr>
<tr><td colspan="2">AlGaAs/GaAs/GaAsP/GaN4(NGC)</td></tr>
<tr><td>Diode Performance</td><td>HBT
Performance</td></tr>
<tr><td> 
</td><td> 
</td></tr>
<tr><td colspan="2">AlGaAs/GaAs/GaAsP/GaN5(KAUST)</td></tr>
<tr><td>Diode Performance</td><td>HBT
Performance</td></tr>
<tr><td> 
</td><td> 
</td></tr>
<tr><td colspan="2">AlGaAs/GaAs/GaAsP/GaN6(Cree)</td></tr>
<tr><td>Diode Performance</td><td>HBT</td></tr>
</table>

	Performance
	

3.5 Conclusion

Various kinds of diodes and HBT utilizing n-GaN substrates of different doping schemes are demonstrated and tested along the way toward the fabrication of n-AlGaAs/p-GaAs/p-GaAsP/n-GaN DHBTs as shown in Table 3.4. First, p-Si/n-GaN and p-GaAs/n-GaN diodes were fabricated to test if GaN substrates grown from NGC(MBE), KAUST and Cree (MOCVD) could properly work as n-type doped semiconductors in bipolar devices. Moreover, various ALD conditions on the interface between p-silicon and n-GaN were tested for the case of KAUST-grown GaN. As a result, they showed IV-performances of the on/off ratio up to ~10^8 and IF of ~1.2 with significant uniformity. To confirm how different conditions of ALD involving AlN layer on the interface affect the band bending on the side of n-GaN, additional experiments under low temperature will be necessary to erase the thermal effects.

Then, n-AlGaAs/p-GaAs/n-GaN DHBTs were fabricated to test transistor performance using NGC GaN substrates. Even though the DHBT showed record-breaking EB and BC diode performances, the same DHBT devices whose diodes worked did not demonstrate a DC gain higher than 1, which means that EB and BC diodes did not communicate each other. The reason

for that is the surface band-bending on the GaN substrate was too high for electrons to diffuse through the BC junctions. To resolve the issue, nanomembranes utilizing graded GaAsP layers that lowers electron affinity on the base side were used to reduce the discontinuity in the conduction bands (n-AlGaAs/p-GaAs/p-GaAsP/n-GaN). Then, the further step was taken to reduce the band-bending on the GaN side, utilizing the GaN substrate that have the capping layer with high doping concentrations. (GaN4, 5) For the other GaN substrate, the high doping concentration on GaN surfaces was employed to expect the upward band-bending would be reduced with depositing ultra-thin Al_2O_3 layers. (GaN6) As shown in Table 3.6, the DC gain higher than 1 was only obtained from HBT utilizing GaN6, even though the XRD results indicated that the upward band-bending of GaN5 (-0.112eV) is lower than that of GaN6 (0.053eV). As only GaN6 substrate has the high doping concentration on the surface, it may be concluded that the effect of a highly doped layer on surfaces plays a more significant role. This also indicates that more characterization and measurement will be necessary to fully understand how much the discontinuity in the conduction band affects DC gains in HBT.

In conclusion, the working n-AlGaAs/p-GaAs/p-GaAsP/n-GaN (GaN6, grown by Cree) could be successfully demonstrated with the DC gain of ~80. Additional measurements on the device will need to be conducted, such as measuring RF performance and breakdown voltage to confirm the potentially superior characteristics in high-power and high-frequency environments.

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Chapter 4

Fabrication and Characterization of p-Si/n-Ga_2O_3 Heterojunction by Nanomembrane Grafting

4.1 Introduction

$\beta - Ga_2O_3$ has superior physical characteristics for power applications. Several Figure of Merit of $\beta - Ga_2O_3$ are much higher than those of SiC and GaN, owing to the large band gap, higher dielectric constant, and huge breakdown voltage (Table 1.1). Unipolar devices such as Schottky diodes and MOSFETs utilizing beta-Ga2O3 have been demonstrated and tested, resulting in an enormously high I_{on}/I_{off} ratio of up to 10^8 and large breakdown voltage of up to 600V [1-27]. The state-of-the-art applications of Schottky diodes and MOSFETs for $\beta - Ga_2O_3$ have been organized in Table 4.1. However, there has not been found shallow p-type dopants without a strong self-localization of holes for $\beta - Ga_2O_3$, leading to the unavailability of effective p-type doped $\beta - Ga_2O_3$ [28]. This challenge posed on p-type doping rules out the possibility of p-n homojunction. Then, forming heterojunctions of $\beta - Ga_2O_3$ relies on other p-type doped materials

[29]. Because of a lattice mismatch, the candidates of p-type materials for forming a heterojunction with beta-Ga2O3 only have been considered among the oxide materials that can be epitaxially grown or sputtered on beta-Ga2O3 substrates such as NiOx and SnO [13-17]. The limited potential of the superior material significantly hinders the fabrication of bipolar junction transistors. In this chapter, the semiconductor grafting technique has been utilized to free up this limitation of lattice-mismatch and demonstrated p-Si/n-Ga2O3 diodes with the I_{on}/I_{off} ratio of 3.15×10^7 and ideality factor of 1.13. Considering the achievement of the first-ever heterojunction diodes of p-Si/n-Ga2O3, III-V materials such as GaAs that has excessive carrier mobilities can be applied by the semiconductor grafting technique along the pathway to successful fabrications of HBTs utilizing n-Ga2O3 and III-V compound materials.

Table 4.1. *The state-of-the-art diodes utilizing $\beta - Ga_2O_3$ with their key characteristics and performances.*

#	Device type	Doping [cm^{-3}]	Current density (A/cm^2)	V_{br}[V]	I_{on}/I_{off}	Ideality Factor	Notes	Ref
1	Schottky	n: 2×10^{17}	$10 A/cm^2$ $V = 1V$	58 ~73	10^5 $V = \pm 1V$	1.04	W/Au	[1]
2	Schottky	n: 6×10^{16} $\sim 8 \times 10^{17}$	$10^{-1} A/cm^2$ $V = 2V$	N/A	10^8 $V = \pm 2V$	N/A	Ni, Grown by the Czochralski method	[2]
3	Schottky	n: 1.7×10^{17}	N/A	N/A	10^6 $V = \pm 2V$	N/A	Ni	[3]
4	Schottky	n: $10^{17} \sim 10^{18}$	N/A	N/A	10^3 $V = \pm 1V$	1.82 @RT 1.2 @500℃ 1.42 @100℃	Au	[4]
5	Schottky	n: 3×10^{16} $\sim 5 \times 10^{16}$	$10^{-2} A/cm^2$ $V = 1V$	150	N/A	1.04 ~1.06	Pt/Ti/Au	[5]
6	Schottky	n: 1.1×10^{17}	$1 A/cm^2$ @400K $10^{-9} A/cm^2$ @100K	N/A	10^{10} $V = \pm 1V$ @400K	1.04	Ni	[6]
7	Schottky	undoped n: 4.1×10^{18}	$10^{-6} A/cm^2$ @RT $10^{-1} A/cm^2$ @225℃	210	N/A	3.38 @RT 1.21 @225℃	Ni/Au	[7]

8	Schottky	2.8×10^{17}	$10^{-2}\mathrm{A/cm^2}$ @RT $10^{-4}\mathrm{A/cm^2}$ @85K $V=1V$	N/A	N/A	3 @RT 1 @80K	Ni	[8]
9	Schottky	1.2×10^{17}	$10\mathrm{A/cm^2}$ $V=1V$	N/A	10^8 $V=\pm 1V$	1.01	Ni	[9]
10	Schottky	3.9×10^{18}	$10^2\mathrm{A/cm^2}$ $V=1V$	N/A	10^7 $V=\pm 1V$	1.4	Ni	[10]
11	Schottky	1.6×10^{18}	$10^{-2}\mathrm{A/cm^2}$ $V=1V$	N/A	10^6 $V=\pm 1V$	N/A	Cu	[11]
12	Schottky	1.2×10^{16}	$10^1\mathrm{A/cm^2}$ $V=1V$	N/A	N/A	N/A	Pt	[12]
13	PN diode	n- : 2×10^{16} n+: 4×10^{18} p: 1×10^{18}	$2\times 10^2\mathrm{A/cm^2}$ $V=2V$	1100 ~1500	N/A	1.31	Heterojunction p-Cu2O/n-Ga2O3 (sputtering)	[13]
14	PN diode	n: 5×10^{17} p: 1.1×10^{18}	$10^{-1}\mathrm{A/cm^2}$ $V=2V$	46	10^7 $V=\pm 2V$	~2	p-NiO epitaxially grown on n-Ga2O3	[14]
15	PN diode	n: 2×10^{19} p- : 10^{18} p+: 10^{19}	$10^{-1}\mathrm{A/cm^2}$ $V=1V$	8320	10^7 $V=\pm 1V$	N/A	p-NiOx sputtered on n-Ga2O3, power figure of merit : 13.2GW/m^2	[15]
16	PN diode	n- : 10^{17} n+: 10^{19} p: 10^{20}	$5\mathrm{A/cm^2}$ $V=2V$	N/A	N/A	N/A	a-Ir2O3/a-Ga2O3, epitaxy	[16]
17	PN diode	n : 2×10^{17} p: 2×10^{18}	$100\mathrm{A/cm^2}$ $V=1V$	66	2×10^8 $V=\pm 1V$	1.16	SnO/beta-Ga2O3	[17]

Table 4.2. *The state-of-the-art transistors utilizing $\beta - Ga_2O_3$ with their key characteristics and performances.*

#	Device type	Doping $[\mathrm{cm^{-3}}]$	$J_{DS}[mA/mm]$ or $I_{DS}[mA]$	Carrier mobility, μ $[cm^2/(V\cdot s)]$	V_{br}[V]	Notes	Ref
1	MESFET	7×10^{17}	$I_{DS}=15mA$ $V_{gs}=2V$ $V_{ds}=40V$ $L_g=4\mu m$ $L_{sd}=20\mu m$ @RT	300	257 $V_g=-30V$	Pontential of Ga2O3-based electrical devices	[18]
2	MOSFET	n(Sn): 7×10^{17} p(Si) : 5×10^{19}	$J_{DS}=35mA/mm$ $V_{gs}=4V$ $V_{ds}=40V$ $L_g=2\mu m$ $L_{sd}=20\mu m$ $W_g=500\mu m$ @RT	300	400 $V_g=-20V$ @RT 370 $V_g=-20V$ @250℃	Al2O3 20nm	[19]

3	MOSFET	n: 5.5×10^{17}	$J_{DS} = 5 \times 10^{-6} mA/mm$ $V_{gs} = 18V$ $V_{ds} = 10V$ $L_g = 1\mu m$ @RT	>70	N/A	Ga2O3 nanomembrane	[20]
4	MOSFET	n: 5.5×10^{17}	$J_{DS} = 25mA/mm$ $V_{gs} = -1V$ $V_{ds} = 10V$ $L_g = 1\mu m$ $L_{sd} = 8\mu m$	106	600	E-Fin	[21]
5	MOSFET	N/A	$J_{DS} = 5mA/mm$ $V_{gs} = -20V$ $V_{ds} = 10V$ $L_g = 2\mu m$ $L_{sd} = 3.4\mu m$	N/A	N/A	Two-finger	[22]
6	MOSFET	n(Sn): 3×10^{17} p(Si) : 5×10^{19}	$J_{DS} = 80mA/mm$ $V_{gs} = 4V$ $V_{ds} = 40V$ $L_g = 2\mu m$ $L_{sd} = 5\mu m$	70-95	750 $V_{gs} = -55V$	Field-plate	[23]
7	MOSFET	1.3×10^{18}	$J_{DS} = 90mA/mm$ $V_{gs} = 0V$ $V_{ds} = 8V$ $L_g = 0.7\mu m$ $L_{sd} = 3.8\mu m$	96	N/A	Recessed-gate	[24]
8	MOSFET	1.6×10^{18}	$J_{DS} = 475mA/mm$ $V_{gs} = 4V$ $V_{ds} = 100V$ $L_g = 2\mu m$ $L_{sd} = 15\mu m$	N/A	400	D-MOSFET	[25]
9	MOSFET	n-: 3×10^{16} n+: 3×10^{18}	$J_{DS} = 250A/cm^2$ $V_{gs} = 0V$ $V_{ds} = 1.3V$ $L_g = 1\mu m$	N/A	N/A	Vertical trench D-MOSFET	[26]
10	MOSFET	n : 10^{17}	$J_{DS} = 7000A/cm^2$ $V_{gs} = 0V$ $V_{ds} = 10V$ $L_g = 0.5\mu m$	N/A	185	Vertical Fin D-MOSFET	[27]

4.2 Materials

Ga_2O_3

The Si-type doped layer of $\beta - Ga_2O_3$ whose doping concentration is 2×10^{17} cm^{-3} was grown using Agnitron Technology's Agilis 500 metalorganic chemical vapor deposition (MOCVD) reactor on Sn-doped $\beta - Ga_2O_3$ substrates whose doping concentration is ~5×10^{18} cm^{-3} as shown in Figure 4.1. Trimethylgallium (TMGa), pure oxygen (5N), and silane diluted in nitrogen (SiH_4/N_2) were used as precursors and argon (5N) as carrier gas. The Ar and O_2 gasses were passed through point-of-use purifiers to reduce the impurity level to <1 ppm. Prior to loading the sample into the growth chamber, the substrate was cleaned using hydrofluoric acid (HF) for 30 minutes.

Silicon

The silicon-on-insulator with the box SiO_2 of 500nm thickness and the capping oxide of 48nm, as shown in Figure 4.1, was implanted with boron dopants whose dose is 3×10^{15} cm^{-2} and energy is 15keV. Then, the dopants were activated by annealing the SOI wafer at 950℃ for 40 minutes. The simulation result suggests that the doping concentration of the silicon layer is around $5 \times 10^{19} cm^{-3}$.

4.3 Methods of Fabrication

Si/Ga_2O_3 p-n diodes were fabricated which starts from cleaning the β-Ga_2O_3 substrates with the epitaxial layer. The substrate was dipped into acetone and sonicated for ten minutes. The same process was repeated but with isopropyl alcohol (IPA) instead of acetone. Right after sonication, the samples were taken into Piranha solution (96% H_2SO_4 : H_2O_2 = 3:1) and let them sit in the solution for ten minutes at room temperature. Then, the samples were thoroughly rinsed with deionized (DI) water for one minute. The same cleaning procedures were iterated with RCA1

solution (29% NH_4OH : 30% H_2O_2 : DI water =1:1:5) and RCA2 solution (37% HCl : DI water = 1:1) in sequence. Finally, the samples were dipped into diluted HF solution (49% HF : DI water = 1:20) for one minute and were named the "as-cleaned" sample (Figure 4.2(R1)). During the cleaning process of the Ga_2O_3 substrates, the thin p-Si nanomembrane was separately prepared. A conventional photolithography process was performed form a 9-by-9-μm square hole array pattern on the ~185 nm thick boron (B)-doped (5×10^{19} cm^{-3}) single crystalline Si thin film (Figure 4.2(D1)). The etching-holes through the whole Si layer were then fabricated by reactive-ion etching (RIE), followed by the removal of photoresist (Figure 4.2(D2)) [33]. Then, the patterned SOI was dipped inside 49% HF for 3.5 hours to remove the box oxide layer. After taken out, the SOI was dipped into IPA, and then into water for 1 min each to rinse off HF. Gentle N_2 air gun was used to dry the SOI before transferring the Si thin film on n- side of Ga_2O_3 receiver substrate. The transfer was done using PDMS stamps prepared with the monomer to crosslinker ratio of 4:1 and cured under 60 °C for 4 hours after quick degassing process (Figure 4.2(D3) and 2(R2)). Once the transfer was successfully done, the thermal annealing of 350 °C for 5 min was performed in RTA to form chemical bonding (Figure 4.2(R3)).

Another conventional photolithography was used to cast anode contact pattern on transferred p+ Si ("top" of the device), and then the e-beam deposition of Ni/Au/Cu/Au (10/5/100/10 nm) metal stack was followed to perform lift-off process (Figure 4.2(R4)). For isolation purpose per devices, exposed Si was dry etched using RIE (Figure 4.2(R5)). The device area for each p-n diode after isolation is 37×37 μm^2. Cathode contact was formed on n+ Ga_2O_3 surface by depositing Ti/Au/Cu/Au (10/5/100/10 nm) metal stack on the "bottom" of the device (Figure 4.2(R6)). Additionally, the thermal annealing of 600 °C for 10 seconds was performed for further study of comparing the electrical characteristics of before and after annealing.

The fabrication process for Ga_2O_3 Schottky diodes resembles that of Si/Ga_2O_3 p-n diodes, but much simpler as it does not incorporate SOI processing. With the same double-layered Ga_2O_3 substrate, a conventional photolithography was used to cast anode contact pattern on n- Ga_2O_3 ("top" of the device), followed with the e-beam deposition of Pt/Ti/Au/Cu/Au (10/10/5/100/10 nm) metal stack. The device area for each Schottky diode is 29 × 29 μm^2 (Figure 4.1(c)). Cathode contact was formed on n+ Ga2O3 by depositing Ti/Au/Cu/Au (10/5/100/10 nm) on the "bottom" of the device.

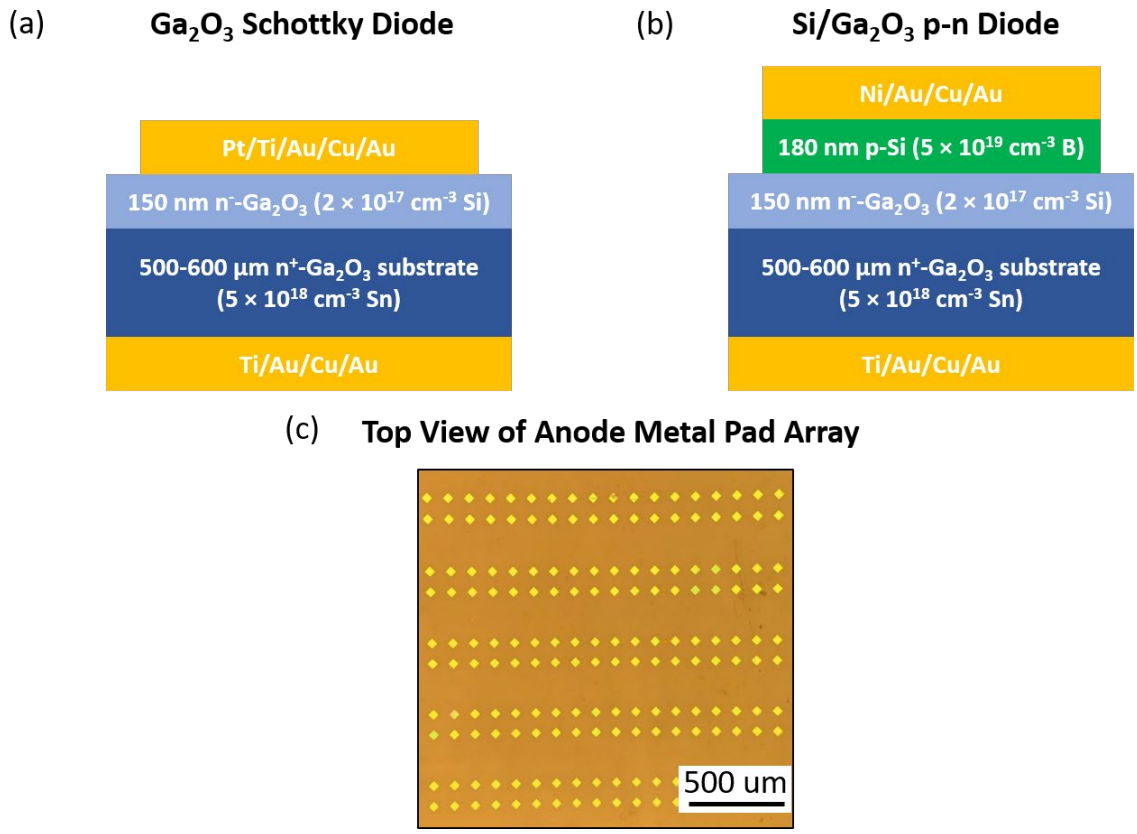

Figure 4.1 *The schematic device layer structure of (a) the Ga_2O_3 Schottky diode and (b) the Si/Ga_2O_3 p-n diode. (c) The optical image of the top anode metal pad array.*

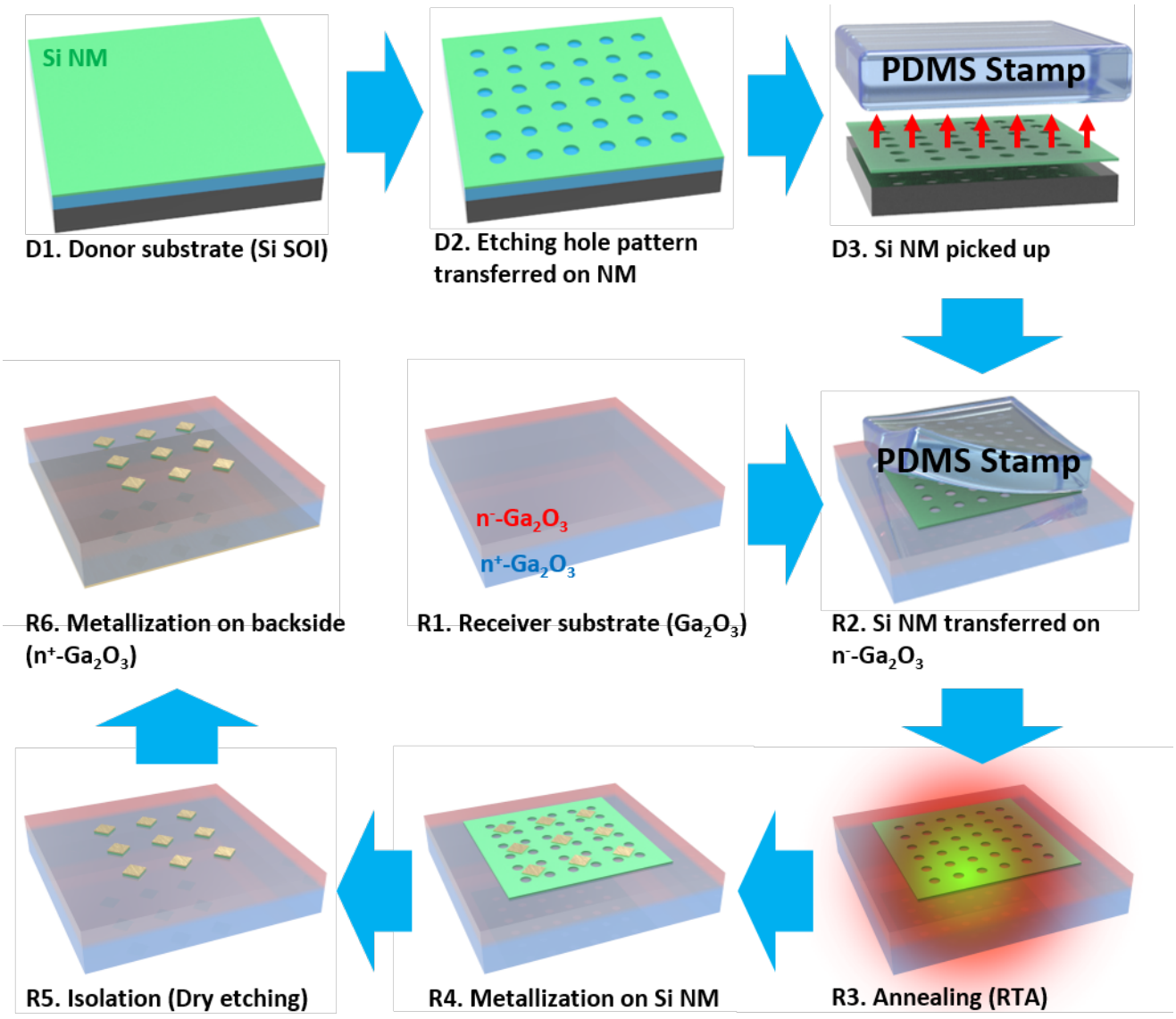

Figure 4.2. *The fabrication process flow of the Si/Ga_2O_3 p-n diode. (D1)-(D3) The fabrication of the donor Si NM on SOI. (R1)-(R2) The transfer-printing of the Si NM onto the receiver Ga_2O_3 substrate. (R3)-(R6) The following fabrication of the Si/Ga_2O_3 p-n diode.*

The current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the devices were measured by Keithley 4200 semiconductor characterization system. The device breakdown characteristics were measured using HP 4155B semiconductor parameter analyzer.

The transmission electron microscopy (TEM) lamella were prepared using a Thermo Fisher Scientific (TFS) Helios G4 dual-beam focused ion beam (FIB) system equipped with an EasyLift manipulator for the transfer of the lamella to the Omniprobe FIB grid. To protect the surface morphology of the device, the electron beam-assisted carbon (C) and Pt deposition, followed by the Ga ion beam-assisted Pt deposition were performed prior to the Ga ion milling. 30 kV Ga ion milling was used for the bulk milling, followed by 5 kV and 2 kV Ga ion milling, i.e. low kV cleaning, to remove the damaged layer created by the 30 kV Ga ion milling.

Scanning transmission electron microscopy (STEM) micrographs were acquired using a Thermo Fisher Scientific (TFS) Themis Z aberration-corrected electron microscope operated at 300 keV. The convergence semi-angle of 21 mrad and the collection semi-angle of 70-200 mrad were used for the high-angle annular dark-field (HAADF) image acquisition. Electron energy loss spectroscopy (EELS) analysis was performed using a Gatan Continuum electron energy loss spectrometer and image filter and K3 electron direct detector. The collection semi-angle of 50 mrad was used to acquire the EELS spectra.

The X-ray photoelectron spectroscopy (XPS) characterizations of the as-cleaned sample were performed using a Thermo Scientific K Alpha X-ray Photoelectron Spectrometer with Al K_α X-ray source ($h\nu$ = 1486.6 eV). The sample was carried in a zip bag filled with N_2 during the transportation from the lab to the XPS instrument to minimize the influence of air. It took about 10 min from moving the sample out of the HF solution to sending it into the XPS chamber. The instrument was calibrated by Au $4f_{7/2}$ peak at 84.0 eV. The following settings were applied to the spectrometer: 10 eV pass energy, 400 μm spot size, 5 s dwell time, and 0.05 eV step size. The auto-height of the sample stage was done only once at the start of the experiment. The Ga 3d, O 1s, and C 1s peaks were measured as the first set of data. The second set of data was obtained

following a 30-s etching from the ion gun with 1 keV ion energy and 2 mm raster size. And the third set of data was measured after another 30-s ion-gun etching.

4.4 Results

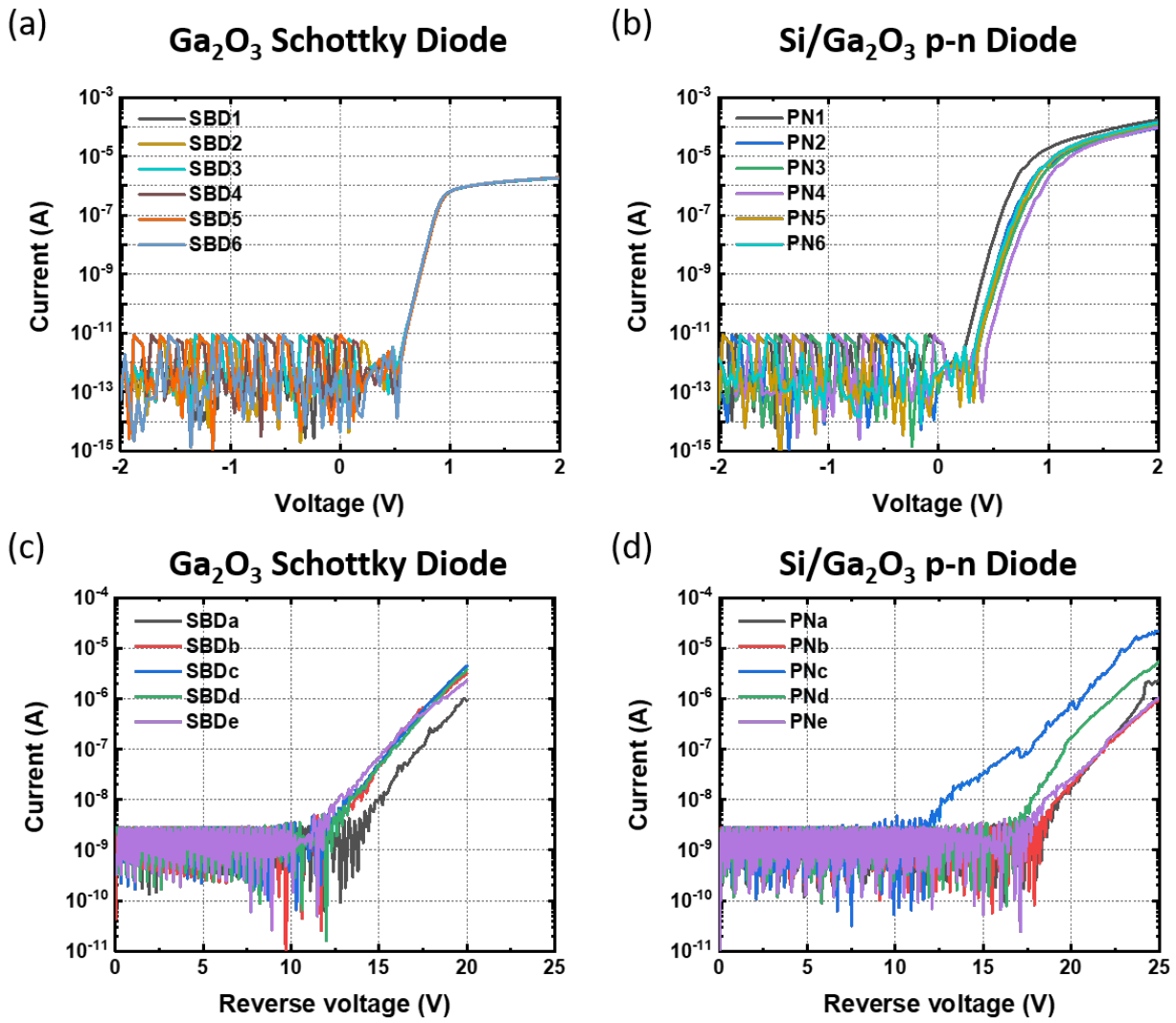

Figure 4.3. *The statistical I-V characteristics of (a) the Ga_2O_3 Schottky diodes and (b) the Si/Ga_2O_3 p-n diodes between ± 2 V. The statistical reverse bias characteristics of (c) the Ga_2O_3 Schottky diodes and (d) the Si/Ga_2O_3 p-n diodes.*

Both Schottky diodes and p-n diodes have been fabricated on the same n-type Ga_2O_3 epi (Figure 4.1). The I-V characteristics of both types of diodes are shown in Figure 4.3. The Schottky diodes (Figure 4.3(a)) show better consistency in I-V characteristics than p-n diodes (Figure 4.3(b)) under the forward bias due to the simplicity of the Schottky diode fabrication process. The ideality factors were calculated and listed in Table 1. The ideality factors of the Schottky diodes are lower than those of pb diodes due to no recombination in the depletion region [34]. As for performance under high reverse bias, p-n diodes (Figure 4.3(d)) show lower reverse leakage compared with Schottky diodes (Figure 4.3(c)), which makes the p-n diodes ideal for applications such as high-power devices and photodetectors. The Schottky barrier height ϕ_B is calculated to be 1.31 eV from the device SBD6 data with the ideal thermionic emission model [34] and the Richardson constant A^* of 41 A/cm^{2}K^2 for β-Ga_2O_3 [35].

Table 4.3 Summary of the ideality of (a) the Ga_2O_3 Schottky diodes and (b) the Si/Ga_2O_3 p-n diodes.

(a) Ga_2O_3 Schottky Diode

Device #	SBD1	SBD2	SBD3	SBD4	SBD5	SBD6
Ideality factor	1.09	1.10	1.16	1.13	1.10	1.08

(b) Si/Ga_2O_3 p-n Diode

Device #	PN1	PN2	PN3	PN4	PN5	PN6
Ideality factor	1.13	1.17	1.36	1.26	1.24	1.22

C-V characteristics were also measured to study the interface quality, i.e., the density of states, of the Si/Ga_2O_3 p-n diodes. As shown in the Fig 4(a), a new device layout with a larger device area (2.79×10^4 μm^2) was adopted to increase the device capacitance and reduce the relative uncertainty of the capacitance measurement. The fabrication process is the same as that of the

devices shown in Figure 4.3. The C-V characteristics show little frequency dependence between 10 kHz and 2 MHz (Figure 4.4(b)), indicating the interface quality is relatively good. Simulations of the Si/Ga_2O_3 p-n diode structure (Figure 4.1(b)) with different interface defect densities were performed with the device simulator Atlas from Silvaco technology computer-aided design (TCAD). A variation of the capacitance against the frequency was observed for interface defect density above 7×10^{12} cm^{-2} (Figure 4.4(c)) within the same frequency range as the C-V measurement (Figure 4.4(b)). It indicates the upper limit of the interface defect density. We also calculated the interface defect density from the ideality factor of the p-n diode with the method we developed in our previous work [36]. The interface defect density is estimated to be $1\text{-}3 \times 10^{12}$ cm^{-2} from the ideality factor of the device PN1 (1.13) with an interfacial amorphous layer thickness of 2.5 nm (Figure 4.5) and the dielectric constant ranging between 3.9 (SiO_2 [37]) and 10.43 (β-Ga_2O_3 [38]). This result agrees with the observation from the C-V measurement.

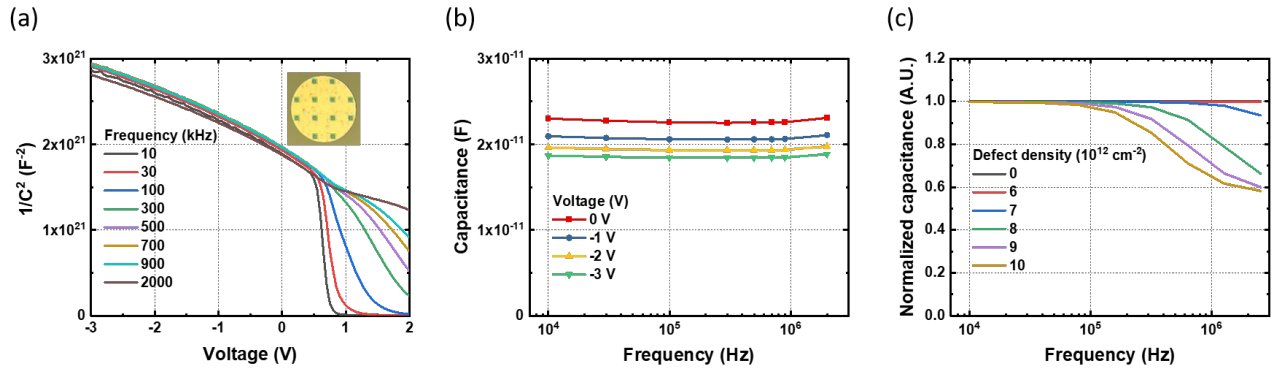

Figure 4.4 *(a) The C-V characteristics of the Si/Ga_2O_3 p-n diode under multiple frequencies. The inset shows the optical image of the device fabricated for the C-V measurement. (b) The capacitance-frequency plots of the Si/Ga_2O_3 p-n diode under various biases. (c) The simulated*

capacitance-frequency plots of the Si/Ga_2O_3 p-n diode under 0 bias with different interface defect densities.

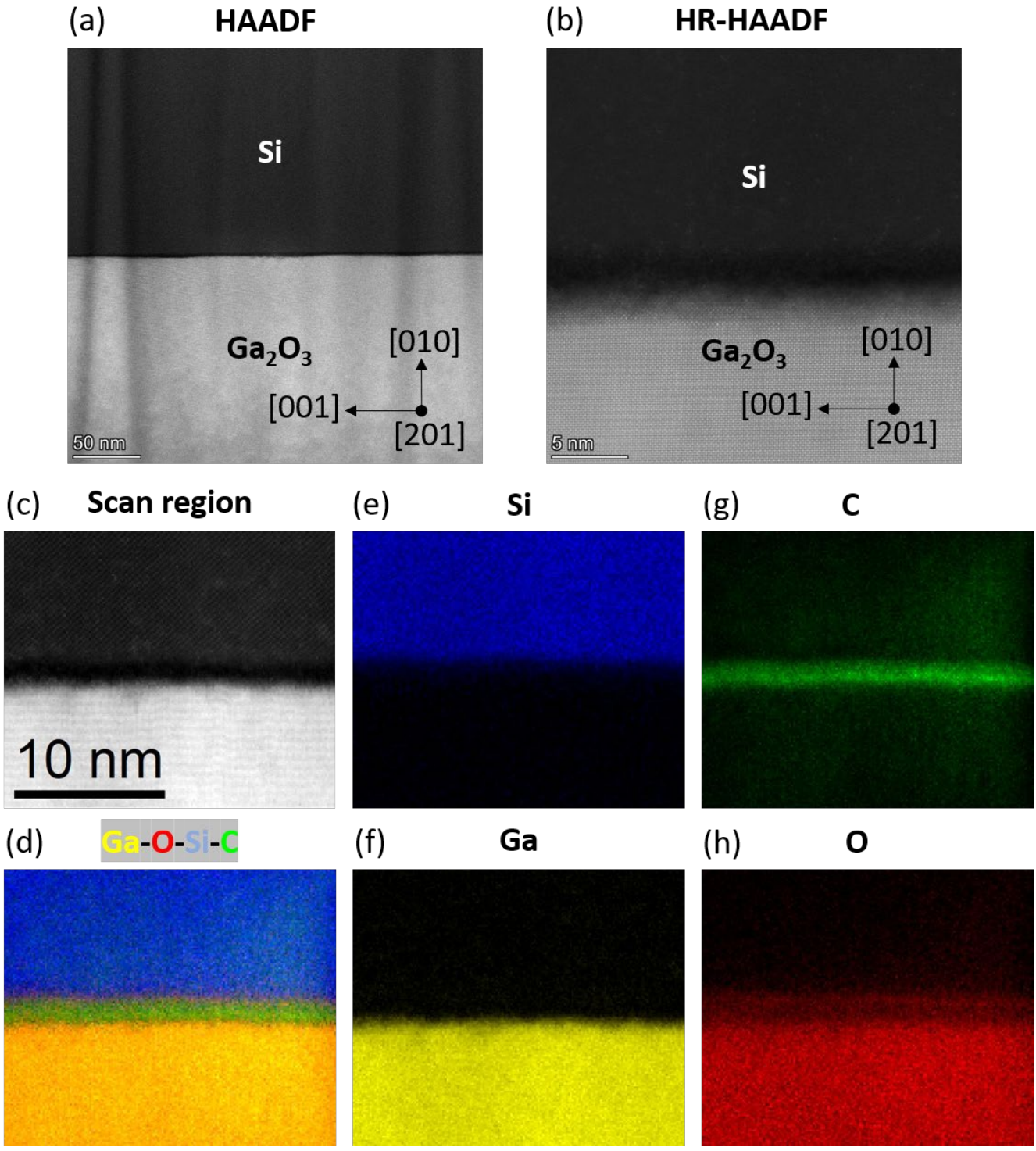

Figure 4.5 *STEM imaging and EELS elemental mapping: (a) The HAADF image and (b) the HR-HAADF image showing the cross-sectional view of the p-Si/n-Ga_2O_3 device. (c) The scan region of the EELS mapping. (d) The fake color image showing the distribution of the corresponding element (Ga-O-Si-C) at the interface. (e)-(h) The EELS maps of Si, Ga, interfacial C, and O elements, respectively.*

STEM imaging and EELS mapping were conducted to study the interfacial topology and elemental distribution (Figure 4.5). The lamella was cut along Ga_2O_3 [001] and viewed along the Ga_2O_3 [201]. The overview (or low magnification) high angle annular dark-field (HAADF)-STEM image shows a relatively flat interface (Figure 4.5(a)). The high-resolution (HR)-HAADF image clearly shows the β-Ga_2O_3 lattice structure along the [201] axis (Figure 4.5(b)). The interfacial amorphous layer is estimated to be ~2.5 nm thick. The EELS results identify the interfacial SiO_2 and residue-C for the TEM lamella investigated (Figure 4.5(c)-(h)). It is speculated that the SiO_2 was formed by the interaction between Si and Ga_2O_3 during the annealing process after the NM transfer. And the residue-C is confirmed to be from the Si NM by the XPS measurement of the as-cleaned Ga_2O_3 substrate (Figure 4.6). And the IPA residue during the Si NM fabrication process (Figure 4.2(D2) and 2(D3)) can be the source of the C.

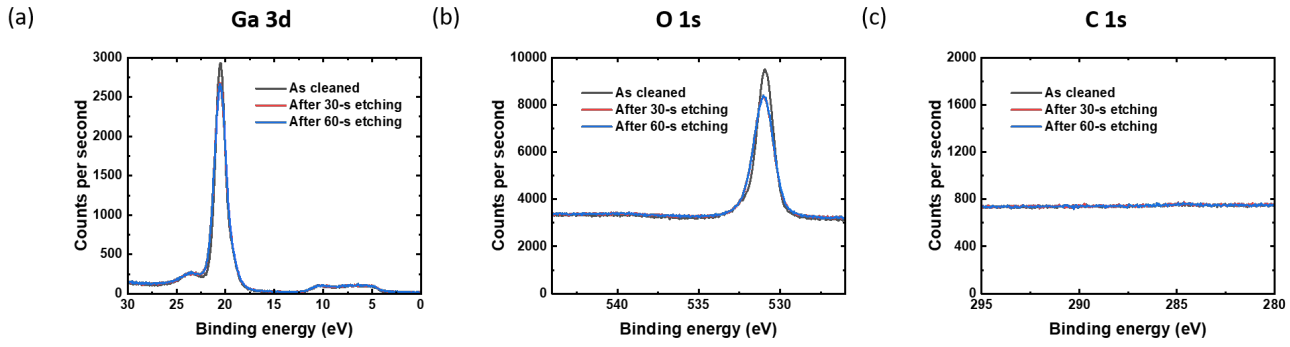

Figure 4.6 *The (a) Ga 3d, (b) O 1s, and (c) C 1s XPS spectra of the Ga_2O_3 substrate. A 30-s ion-gun etching was conducted between each measurement.*

XPS spectra (Figure 4.6) were taken to investigate the electron state difference between the as-cleaned Ga_2O_3 surface (by chemicals as described in the experiment section) (Figure 4.2(R1)) and the ion-beam-cleaned one. Three measurement were taken. The first measurement was done on the as-cleaned sample while the latter two were done following a 30-s ion-gun etching after the last measurement. Because auto-height was only performed at the beginning of the experiment, the absolute intensity of the spectra can be compared among the three measurements. As clearly shown in Figure 4.6(a) and 6(b), the two measurements after the ion-beam etching are almost identical while the initial measurement on the as-cleaned sample is different from the other two. The observation indicates that there exists an ultrathin (~1 nm) surface layer on the β-Ga_2O_3 substrate. Based on the device performance and the calculation of the interfacial defect density, one speculation is that this ultrathin layer serves as a interfacial passivation layer similarly to the interfacial ultrathin ALD-Al_2O_3 applied in our other grafted devices [36, 39-44]. And no C have been observed on the Ga_2O_3 surface (Figure 4.6(c)) (to the instrumental resolution limit of the XPS), indicating that the residue-C observed in the EELS mapping is from the top Si NM.

4.5 Conclusions

In this work, we fabricated grafted Si/Ga_2O_3 p-n diodes and measured their I-V characteristics. Ga_2O_3 Schottky diodes were also fabricated as comparison. The C-V measurement were performed to evaluate the interface quality of the grafted Si/Ga_2O_3 structure. The interface defect density was estimated to be in the scale of 1-3 × 10^{12} cm^{-2} from both I-V and C-V characteristics. STEM images and EELS maps showed the topology and elemental distribution at the grafted Si/Ga_2O_3 interface. A uniform interface with a thin layer (~2.5 nm) of interfacial

amorphous layer was observed. The XPS spectra of the Ga_2O_3 revealed the existence of an ultrathin surface layer on the Ga_2O_3 substrate. This ultrathin layer was speculated to serve as an interfacial passivation layer in the grafted structure.

4.6 References

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Chapter 5

Conclusions and Future Directions

In this dissertation, the fabrication of bipolar devices utilizing diamond, GaN and Ga_2O_3 have been demonstrated and discussed, along with their IV-characteritsics. For each device, the heterojunctions that have never been possible before were achieved through the semiconductor grafting technique. Additionally, the discontinuity of the conduction band (or the valence band) has been successfully addressed by employing thin high-doping concentration layers on substrates, surface treatment of ALD, utilizing graded compound materials (GaAsP), and developing the novel technique—the double-flip transfer.

In Chapter 2, I demonstrated and tested the p-AlGaAs/n-GaAs/p-diamond DHBT with a record-high DC gain of around 2000 by employing the semiconductor grafting technique. Key steps in the successful fabrication of the device included minimizing the electron affinity on the diamond substrate to reduce valence band discontinuity and conducting the double-flip transfer. The inverted structure of nanomembrane was utilized to circumvent the adverse effect of the

remaining scarificial layer on the GaAs and diamond heterojunction. Although the diamond DHBT showed impressive DC gain, the emitter-base diode performance had a low I_{on}/I_{off} ratio and a high IF factor, which was attributed to the reduced uniformity of etch. Future work will involve testing the device under high-speed, high-power, and high-temperature conditions, measuring its breakdown voltage. Furthermore, efforts should be made to improve device yield by optimizing the fabrication process. The successful development of this DHBT reflects the promising characteristics of diamond and GaAs materials, showcasing their potential for high-performance applications.

In Chapter 3, the development of GaN-based DHBT (n-AlGaAs/p-GaAs/p-GaAsP/n-GaN) for power electronics applications has been discussed and demonstrated, with a DC gain of up to 80 under a low offset of V_{cb}=1V. In order to address the effect of the discontinuity in the conduction band between GaAs layers and GaN substrates, a graded GaAsP layer was employed at the interface. Additionally, surface treatment was conducted on the surface of the GaN substrate, along with utilizing a high-doping concentration layer on the GaN surface to suppress upward band-bending. Although further characterization and measurements are required to understand the band-bending suppression mechanism of surface treatment and the thin n+ layer on the GaN substrates, the successful demonstration of a working n-AlGaAs/p-GaAs/p-GaAsP/n-GaN HBT indicates the potential of this approach in high-power and high-frequency environments. Future work should focus on additional measurements, such as RF performance and breakdown voltage. The insights gained from this research can pave the way for further optimization and advancements in GaN-based power electronics applications.

In Chapter 4, the fabrication of grafted Si/ Ga_2O_3 p-n diodes was successfully demonstrated. This achievement opens up possibilities for the integration of high-performance III-V materials

for future Ga_2O_3-based bipolar devices, such as HBT, by overcoming the limitations of lattice mismatch through the semiconductor grafting technique. The I-V characteristics of the grafted diodes were measured, yielding a high I_{on}/I_{off} ratio of 3.15×10^7 and an ideality factor of 1.13. The C-V measurements were performed to assess the interface quality of the grafted Si/ Ga_2O_3 structure. The interface defect density was estimated to be in the range of $1 - 3 \times 10^{12} cm^{-2}$ from C-V characteristics. Future works include studying the passivation effect of an uniform thin layer on the interface, which was measured by STEM images and EELS maps.