Topology, Modeling and Analysis of Bridge of Bridge DC-AC and AC-DC Power Converters

By

Justin Kyle Reed

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The dissertation is approved by the following members of the Final Oral Committee:

Giri Venkataramanan, Professor, Electrical Engineering
Thomas Jahns, Professor, Electrical Engineering
Bulent Sarlioglu, Assistant Professor, Electrical Engineering (Adjunct)
Yehui Han, Assistant Professor, Electrical Engineering
Robert Lorenz, Professor, Mechanical Engineering

Abstract

The bridge of bridge converter (BoBC) topology is a recent addition to the family of power converters. Inherently modular and multilevel, the BoBC is also a flexible topology that employs "building blocks" for realizing power conversion throughout an extremely wide range of power, voltage, current and applications. However, its use has so far been extremely limited and its capabilities, limitations and fundamental behavior largely unexplored. This research therefore builds a generalized topological framework for the analysis and design of the BoBC, focusing on dc-ac and ac-dc power conversion. Using this framework, techniques for sizing converter components such as capacitors and switches are developed. Dynamic phasor modeling in *dq* coordinates suitable for multilevel converters of arbitrary size permits the use of time-invariant visualization and enables the use of the BoBC in high-performance applications such as motor drives. A case study laboratory-scale converter validates the predicted multilevel behavior, and computer simulations confirm model accuracy.

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To Jasper

May you keep on smiling

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Nomenclature

AC	Alternating Current
ADC	Analog to Digital Converter
BoB	Bridge of Bridge
BoBC	Bridge of Bridge Converter
BJT	Bipolar Junction Transistor
BV	Bidirectional Voltage
BC	Bidirectional Current
BES	Bidirectional Energy Storage
CAN	Controller Area Network
CC	Cross Coupling
CSC	Current Source Converter
CSEB	Capacitive Storage Embedded Bridge
DC	Direct Current
ECC	Energy Conservation Constraint
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FB	Full Bridge

HB	Half Bridge
HEV	Hybrid Electric Vehicle
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
IPC	Interprocessor Communications
ISEB	Inductive Storage Embedded Bridge
ISR	Interrupt Service Routine
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LTI	Linear Time-Invariant
M2C	Modular Multilevel Converter
MERS	Magnetic Energy Recovery Switch
MMLC	Modular Multilevel Converter
M^2LC	Modular Multilevel Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OC	Overcurrent
OV	Overvoltage
PF	Power Factor
PM	Permanent Magnet
PSPWM	Phase-Shifted PWM
PV	Photovoltaic

PWM	Pulse Width Modulation
QC	Q-cell
SFB	Semi-Full Bridge
SHOTS	Scalar Higher-Order Term Suppression
SID	Standard Identifier
SMES	Superconducting Magnetic Energy Storage
SPDT	Single Pole Double Throw
SVM	Space Vector Modulation
UC	Unidirectional Current
UES	Unidirectional Energy Storage
UV	Unidirectional Voltage, alt. Undervoltage
VSC	Voltage Source Converter
ZSC	Z-Source Converter
θ	Low frequency ac phase offset
φ_{ac}	Power factor angle
ω_{ac}	Fundamental ac frequency, in rad/sec
C_S	Bridge energy storage capacitor
d_B	Bridge duty ratio
d_1, d_2	Duty ratio of individual switches within full bridge CSEB
I_{ac}	Terminal ac current, in rms
i_B	Bridge current, in rms
I_{base}	Base current for normalization

i_{Cs}	Capacitor current
i_D	Diode current
I_{dc}	Terminal dc current
i_S	Switch current
j	$\sqrt{-1}$
k_{arm}	Parallel interleaving coefficient per arm
k_{str}	Series interleaving coefficient per string
k_{tr}	Voltage transfer ratio
L_B	Bridge inductance
M	Modulation index
n_{br}	Number of branches connected to dc terminal
n_p	Number of parallel-connected strings per branch
n_s	Number of series-connected Q-cells per string (or branch if n_p=1)
P_{ac}	AC terminal power, in rms
P_{dc}	DC terminal power
R_a	"Active resistance" gain of SHOTS controller
R_{ac}	AC load resistance
R_B	Resistance of bridge inductor
R_{eff}	Effective resistance
R_S	Load resistance on energy-storage side of bridge, and/or bridge losses
S_B	Apparent power per unit bridge, in rms
V_{ac}	AC output voltage per unit bridge, in rms

$V_{ac,tot}$	AD output voltage at converter terminals, in rms
v_B	External bridge voltage
v_{Bi}	Internal bridge voltage
V_{dc}	DC input voltage per unit bridge
$V_{dc,tot}$	DC input voltage at converter terminals
V_L	Bridge inductor voltage
V_S	Bridge capacitor voltage
$V_{S,dc,tot}$	Sum total of series-connected CSEB capacitor voltages per branch
Z_{ac}	AC bus impedance
Z_{dc}	DC bus impedance

Chapter 1 Introduction

This chapter provides a general introduction to dc/ac converter topologies. Objectives of this work are outlined, and a brief synopsis of the individual chapters is provided.

1.1 Overview of dc-ac converter topologies

Of all types and forms of electrical power conversion, perhaps the most frequently required functionality is between direct current (dc) and alternating current (ac). Both forms of electricity are abundant in modern society and neither shows any sign of giving up ground. For example, the ac form has been utilized with great success particularly in rotating machinery, power transmission, and power distribution systems [1], whereas the dc form is naturally present in batteries, photovoltaic (PV) systems [2], and fuel cells [3]. Naturally, the integration of these and plentiful other energy exchange systems require dc-ac converters to deliver power from the source to the load.

With an obvious demand for dc-ac power conversion systems, a wide variety of both fundamentally and incrementally novel power converter topologies continue to be proposed in the literature. Unfortunately, using historically available commercial products as a measurement, the vast majority of fundamentally new dc-ac and ac-dc converter topologies have had limited success. In fact, only two basic solid state converter topologies have been commonly used – the current source converter (CSC) and the voltage source converter (VSC), commonly with two or at times a few more levels.

Two additional topologies have been recently proposed – the Z-source converter (ZSC) and the bridge of bridge converter (BoBC). While as of this writing, neither has seen significant commercial use, the publication record of the ZSC and BoBC indicates that they show the most promise and interest by academics and industry members alike, and so they are considered along with the CSC and VSC.

Fundamentally, all 4 topologies are capable of performing in multiphase ac systems of arbitrary phase number. Therefore, the 4 topologies are discussed in the context of a single-phase ac system with no loss of generality regarding multiphase use. Furthermore, all topologies are suitable for use in either unidirectional or bidirectional power flow applications with minimal or no modifications from the circuit diagrams shown. The discussion therefore makes no assumptions regarding power flow directionality.

1.1.1 Classical converter topologies

Early switched mode dc-ac power conversion systems utilized the CSC topology [4, 5], characterized by a current source (inductor) on the dc bus, shown in Fig. 1-1. One reason for the phenomenal success of this topology was that its behavior was well-aligned with the strengths of the switching devices available at the time. That is, thyristors, thyratrons, mercury arc valves, and the like could be triggered into conduction but could not be actively turned off (commutated). Instead, the converters typically relied upon the ac waveform itself to force the devices into commutation by careful timing of switching events with respect to the ac current zero crossings.

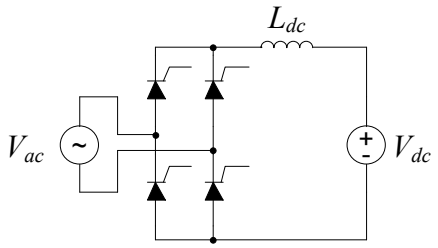


Fig. 1-1. Current source converter topology for single phase ac-dc power conversion realized with thyristors.

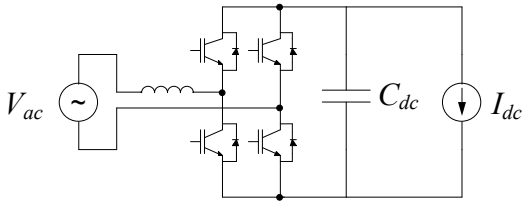


Fig. 1-2. Voltage source converter topology for single phase ac-dc power conversion realized with IGBTs.

After the introduction of high power self-commutating switches, such as bipolar junction transistors (BJTs), the CSC largely fell out of popularity in preference for the VSC, which is characterized by a voltage source (capacitor) on the dc bus [6, 7]. By exchanging the bulky and lossy inductor with the capacitor, much more desirable cost, weight and efficiency traits are achieved. This topology is shown in Fig. 1-2, realized with modern insulated gate bipolar transistors (IGBTs). The VSC now dominates the commercial market of dc-ac converters, except at extremely high power levels where thyristor-based switches are still popular [8].

1.1.2 Z-source converter

The ZSC is a more recent addition to the family of dc-ac topologies, primarily characterized by an impedance network on the dc bus [9]. By utilizing both capacitors

and inductors in the network, phenomena such as shoot-through in the VSC are given new functionality such as voltage boosting. It also provides additional flexibility in the use of current and voltage sources on the ac and dc sides. However, additional reactive elements are required, including two inductors that can contribute non-negligible cost to the system. In the literature, the ZSC has seen considerable analysis [10] and has been applied to a variety of areas including fuel cells [9] and hybrid electric vehicles (HEVs) [11] but is not yet known to have commercial applications.

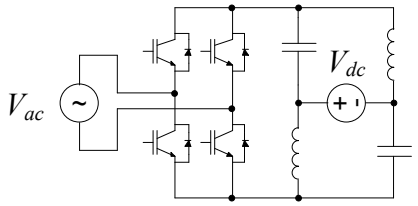


Fig. 1-3. Z-source converter topology for single phase ac-dc power conversion with current-stiff ac bus.

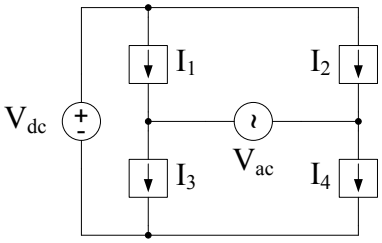


Fig. 1-4. Generalized dc-ac BoBC topology for single phase ac-dc power conversion.

1.1.3 Bridge of bridge converter

The final dc-ac converter topology is the BoBC [12], also known by Marquardt as the modular multilevel converter (MMLC, M^2LC or M2C) [13], the chainlink converter by Oates [14], and the magnetic energy recovery switch (MERS) by Shimada [15]. The

various converter names correspond to different implementations; the M2C is presented in the literature as using very specific *submodules*, and is often applied to HVDC conversion, while the MERS uses the same circuits for controlling resonant circuits. The BoBC concept, however, is not limited to any of these single applications; in fact it encompasses all such applications, because the BoBC concept is based purely on distributed, controlled energy sources for modulating power throughput.

The BoBC is shown in Fig. 1-4 and comprises 4 converter branches, in this case each behaving as a controllable current source, to modulate power throughput. This is a relatively new topology, having been introduced in 2003 [16], and its capabilities, limitations, dynamics and control are current research topics under active investigation [8, 12-14, 16-98]. The BoBC has several very desirable attributes, namely its minimal inductance requirements; the capability of full buck and boost operation, regardless of power flow direction, and without the use of a transformer; and it is naturally fault tolerant. Furthermore, the converter branches may consist of any number of smaller conversion units in series and/or parallel, providing a multilevel architecture with additional flexibility, fault tolerance, and further reduction of inductance requirements using interleaving techniques. The BoBC is therefore an attractive topology for a wide range of dc-ac converters across all power levels, frequencies, voltages, currents and applications. In very recent years, the BoBC has seen an explosion of popularity in the literature. However, nearly all such publications examine only a very small set of BoBC applications and topics, illustrating that the dc-ac BoBC has yet to be thoroughly explored from a generalized standpoint.

Among the BoBC literature for dc-ac applications, the dominant theme is on high voltage direct current (HVDC) power transmission converters [8, 13, 36, 39-41] and other high power applications using 3-phase ac [26, 29, 31, 42, 99]. Like the ZSC, the BoBC is not limited to use in dc-ac converters, having been applied to ac-ac power converters [20-23, 43-45, 100-102], ac series compensation [46, 103-111], ac shunt compensation [37, 46-49, 51, 112], electric machine drives [53, 58, 66-68], and a handful of specialized applications [8, 15, 44, 46, 69, 113-115]. The BoBC concept has also been extended to a unique ac-ac converter called the Hexverter [70], a detailed discussion of which is beyond the scope of this work.

A certain number of publications can be applied to a general BoBC topology and are therefore of direct interest to defining the objectives of this research. An excellent survey of the salient developments within the BoBC literature is [71], which includes topics such as converter models that incorporate various levels of detail, the use of Space Vector Modulation (SVM) [25, 26] versus staircase modulation [72] in high power converters and Pulse Width Modulation (PWM) in lower power converters, and control strategies of all BoBC types. A detailed analysis of BoBC system dynamics with a considerable amount of behavioral insight is provided in [60]. A separate work focuses on the frequency-domain analysis [73]. Huang et al discuss various distributed BoBC controller communications options in [74].

Just like any power converter, a wide variety of modeling approaches can be applied to the BoBC, including averaged bridge modeling [12, 41], state space using the abc frame [75][34], state space in dq0 frame [38, 76], and αβ modeling applied to motor

drives [66]. DQ0 modeling has also been applied to nonlinear control schemes representing specific frequencies [77].

Generally speaking, converter models are used to determine the sizing of the converter elements. A very instructive research for sizing of components and calculation of losses is that of Allebrod, Hamerski and Marquardt [13]. However, these calculations focus on HVDC converters for 3-phase ac and are therefore not applicable to the general BoBC topology. A related work by Bernet et al is [19]. Since the writing of the original version of this document, capacitor sizing was proposed [78], also by Bernet. Another design-oriented investigation, specific to ac drives, is [67].

Many works also cover much lower-level implementation topics, such as the various possible modulation schemes. For example, [80] is a survey of PWM methods to determine how many bridges to connect within a branch, to realize the desired voltage waveform, but leaves open the subject of which capacitors to switch high and low to provide capacitor charge balancing. Another survey is [99]. In the classical BoBC implementation in HVDC applications, staircase modulation is often used to leverage the very high numbers of levels and low switching frequencies of medium-voltage switches [72]. Using smaller, faster switches enables PWM methods, such as Phase-Shifted PWM (PSPWM) [81], an alternative PWM strategy [82], and reduced switching frequency modulation [83]. Different still is bang-bang/hysteretic control and modulation, discussed in [54, 85].

As will be shown later in this dissertation, a large number of control “handles” are provided within a BoBC that can be used to govern its behavior. As such, the BoBC can

be an extremely complex device and achieving satisfactory control of its energy states and terminal quantities is of utmost importance. Furthermore, the BoBC plant is inherently nonlinear, which can lead to in-depth control system analyses. For example, interactions between multiple control schemes are investigated in [59]. A variety of works present nonlinear control schemes, for example [79, 86, 87] describe a nonlinear approach to encompass all aspects of current and voltage control, and [88] proposes a model predictive control methodology. Finally, control schemes can be leveraged to maximize certain effects such as minimizing bridge capacitance [90] or direct modulation of capacitor voltage ripple [61].

Particular attention has been paid to the problem of capacitor voltage balancing within the BoBC. Salient voltage balancing schemes include Marquardt's sorting algorithm [25], which selects bridge switching states depending on the polarity of branch current and each capacitor's relative value, e.g. the lowest capacitor voltages get increased and the highest voltages decreased. This scheme has been adopted by a number of researchers including Saeedifard and Iravani [91] and Bernet et al [18, 19, 32, 33]. Reference [32] highlights that only one bridge within a branch incurs PWM switching at a given time, with the other bridges locked in their respective switching states.

Akagi et al proposed a PWM-based balancing scheme [48, 49], which utilizes averaging over positive and negative portions of the branch current waveforms to affect the commanded bridge voltages of *all* bridges within each branch simultaneously, leading to high effective switching frequencies but requiring higher controller computational throughput. This method determines switch duty ratios based on commanded capacitor

voltages, load voltages, branch voltages and reference quantities. Other control methods are also proposed in Akagi's work, based on other quantities such as branch currents and output currents. As proposed, these control methodologies require a centralized controller. A closely related version of the Phase-Shift PWM (PSPWM) scheme inherently balances capacitor voltages [92].

Angquist et al proposed the use of the common mode current, defined with respect to the dc supply side, to modulate capacitor voltages at the branch level [17]. An alternative method by the same authors was documented in [55, 56, 64], wherein the total branch capacitor voltage is estimated from the ac output current waveform rather than by measuring the voltages directly, and each individual capacitor voltage is controlled by comparing to this estimated total. Contrary to the method's naming, this system does comprise a closed loop control scheme. This research group has also proposed a modulation scheme that inherently balances the capacitor voltages [62]. Reference [89] proposes the use of physically different Voltage Correcting Modules to modulate the common mode current and Wang et al [93] propose a resonance-based approach to capacitor voltage control.

When mentioned, the vast majority of BoBC papers only present one or two fundamental bridge circuits. However, even though a large number of alternatives do exist, they are essentially absent from the literature. As of this writing, the few exceptions are: a fault tolerant bridge with a third switch [94], other fault tolerant designs [28], a 3-level bridge [31], or a bridge using inductive energy storage [95]. Reed and

Venkataramanan proposed a complementary variation to the two fundamental bridge circuits [76, 96], which will be described in Section 2.3.2.

Though these contributions have definite value and utility, as a whole they fall short of providing a complete and unified framework for the analysis and design of generalized BoBCs, particularly from the perspective of arbitrary ac phase numbers and buck/boost ratios. Another shortcoming of this body of literature is a clear understanding of the internal dynamics using an operating point model; despite their shortcomings, operating point models are well-understood and provide the design engineer with intuition regarding how design parameters can affect the converter dynamics. Nonlinear models and controls that can completely represent the converter, while sometimes useful, are inherently more complex and therefore tend to lack transparency, preventing the design engineer from truly understanding the underlying system.

To this end, the works of Ludois and Venkataramanan permit a more sophisticated understanding of the BoBC [41, 97, 98]. In fact, one salient point raised throughout their investigations is that a capacitor voltage control loop is not necessary because the BoBC behaves like a cascaded buck-boost converter, and the inner capacitor voltage is determined by the terminal duty ratios. While a very simple and powerful notion, these works did not investigate these behaviors beyond simple scalar converter modeling. Among other goals, this dissertation seeks to improve the understanding of BoBC dynamics and behavior by expanding on the modeling sophistication.

1.2 Objectives

The primary objective of this work is to present a generalized framework for modeling and analysis of dc-ac BoB power converters during PWM operation. This is divided into the following:

1. present and analyze the basic BoBC "building blocks,"
2. develop guidelines for the interconnection of building blocks,
3. propose a process for BoBC design,
4. propose a basic BoBC control methodology,
5. develop component stress models,
6. derive a low-frequency dynamic phasor model,
7. explore dynamic behavior of BoBC using phasor model,
8. extend modeling to converters with arbitrary numbers of levels,
9. demonstrate and validate the work for a single-phase dc-ac converter.

These objectives will be met using an appropriate combination of analytical, simulation and experimental methods.

1.3 Chapter overview

Chapter 2 begins with the fundamental rules regarding the use of the BoBC "building blocks" and demonstrates through example how general BoBCs must operate based upon these rules. Two families of building blocks are then presented in detail, including their governing dynamic models, and the optimal building blocks for typical power converters are chosen.

Chapter 3 develops a converter-wide scalar steady-state model of the BoBC based on prior art and a small number of simplifying assumptions. A design process is presented and stress models for the capacitors and switches are developed along with the steady-state model and a simple nomogram-based method to determine suitable CSEBs for a given set of BoBC terminal characteristics. Capacitor sizing equations are also derived. An improved accuracy model is presented, which may be used when the simplifying assumptions are not valid. Frequency content of the steady-state model is investigated and a scalar closed loop current control methodology is presented to mitigate unwanted frequencies within the BoBC.

Chapter 4 develops a single-bridge dynamic phasor model of the BoBC using the *dq* coordinate system with dc components, which facilitates the converter's use in multiphase ac systems, particularly ac drives. Dynamic behavior is explored using small-signal stability analysis of eigenvalues and transfer functions over a range of closed loop controller gains.

Chapter 5 extends the single-bridge model to multiple levels, with examples of 2 and 3 series-connected bridges, and extensions to arbitrary numbers of bridges. Small-signal analysis demonstrates the scaling of eigenvalues as more bridges are added.

Chapter 6 validates the converter modeling presented throughout the previous chapters using a combination of simulation and experimental results using a laboratory-scale prototype converter. Detailed information is provided regarding both the design of the main power bridge components and the design and construction of the remaining hardware systems.

Chapter 7 concludes by summarizing all contributions and outlining the future work on the BoBC.

Chapter 2 Bridge of Bridge Topologies

A variety of BoBC topologies may be constructed from a variety of "building blocks" called Q-cells. This chapter first describes the general motivation, concepts, and guidelines for developing BoBCs, with several generalized topology examples. Examples of various Q-cells which may be used to construct the converters are then presented and discussed.

2.1 BoBC building blocks

The bridge of bridge approach to power conversion may consist of branches of relatively small, 2-terminal power converter building blocks referred to as Q-cells (QCs). Briefly, the role of the Q-cell is to source and sink reactive power at multiple frequencies in order to control power flow; this role is further developed throughout this chapter. By combining Q-cells into branches comprising series strings and/or parallel arms, increased voltage blocking and/or current carrying capacity may be realized as illustrated in Fig. 2-1. Voltage blocking capability increases as the number of Q-cells in a series string increases or as more parallel arms are connected in series. Similarly, current handling capability increases as the number of parallel Q-cells in an arm, or as more series strings, are connected in parallel.

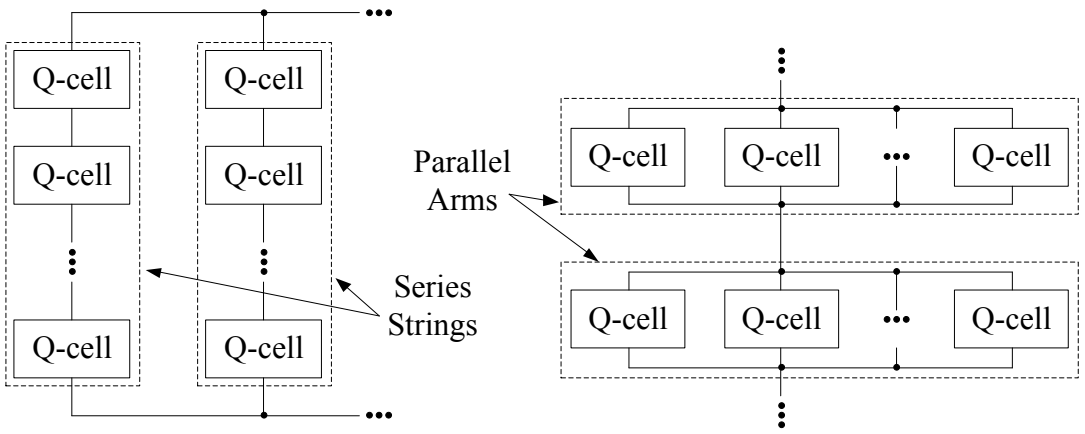


Fig. 2-1. Example branches consisting of series string and parallel arm configurations of Q-cells for realizing increased voltage blocking and/or current carrying capacity.

Furthermore, each Q-cell is assumed to be a closed system of components with only 2 power terminals – there are no separate power sources to source or sink real power. This statement carries with it the implication that **energy must be conserved within each Q-cell, i.e. Q-cells themselves cannot sink or source any real power** (aside from any converter losses). This property, hereby referred to as the Energy Conservation Constraint (ECC), is fundamental to all BoB power conversion systems and is developed throughout this thesis.

It is convenient to classify Q-cells with respect to their terminal characteristics in order to develop their interconnections. Instantaneous Q-cell power $S(t)$ is defined as the product of the terminal voltage $v(t)$ and current $i(t)$,

$$S(t) = v(t)i(t). \qquad 2\text{-}1$$

In a regulated power conversion system, often one of the terminal quantities is established as the controlled variable and the other is the uncontrolled (but known/measured) variable. Of primary importance, then, is whether a Q-cell behaves as a

controllable voltage source, or as a controllable current source. In either case, the source ultimately behaves as a reactive power source because the ECC dictates that real power must be zero. In other words, a given Q-cell will have either a specified voltage across its terminals or a specified current through its terminals, in addition to sourcing the same amount of power that it sinks. Generic two terminal devices used in power converters are often described as being "voltage stiff" and "current stiff." The term "stiffness" signifies a quantity – voltage or current – that cannot be instantaneously changed in the two-terminal device. That is, a "current stiff" Q-cell maintains current flow through its two terminals, while a "voltage stiff" Q-cell maintains a voltage across its two terminals. These properties imply limitations on di/dt and dv/dt, not on i and v themselves. Indeed, Q-cells, in general, may exhibit certain stiffness characteristics due to their internal filter and/or energy storage components. Although it may be convenient to control voltages across voltage stiff Q-cells or current through current stiff Q-cells, such a feature is not absolutely essential in order to achieve power flow regulation. They are required, however, to have specified and/or controllable terminal characteristics regarding either voltage or current, free of net internal energy transfer. Thus, in describing the attributes and operation of BoBCs with arbitrary ratings, the Q-cells may be assumed to behave as ideal controllable voltage and/or current sources with infinite bandwidth.

Furthermore, interconnections of Q-cells along a branch within a BoBC must adhere to fundamental principles that arise from Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) that govern series and parallel operation. That is, similar to ordinary voltage and current sources, **Q-cells behaving as *independent* controllable**

current sources may not be connected in series and Q-cells behaving as *independent* controllable voltage sources may not be connected in parallel. It is possible, however, to control an entire arm as a single voltage source, or an entire string as a single current source, without violating their fundamental properties. Besides this aspect, any number of Q-cells may be interconnected to form strings and/or arms. It is straightforward to see how the BoB approach inherently facilitates multilevel and modular architectures. The manner in which the Q-cell arms and strings can be effectively combined into fully functional BoBCs is discussed in the next section.

2.2 Evolution of the essential BoBC topological structure

A simple converter realized using a controlled current source branch to transfer power between two independent dc voltage sources is shown in Fig. 2-2a. Another perfectly valid example, albeit a less common one, would be a controlled voltage source connected in parallel (shunt) with two independent current sources, illustrated in Fig. 2-2b. That is, both cases exhibit controllable power flow. The former example is examined in-depth.

In the case of Fig. 2-2a, the controllable current source branch may comprise any combination of Q-cells in any configuration of series and/or parallel arms as long as the combination is ultimately a controlled current source. This simple primitive converter fails to operate successfully because net energy transfer between V_{dc1} and V_{dc2} can only occur when I_1 also contains dc components. Since any practical converter will have $V_{dc1} \neq V_{dc2}$, then I_1 will incur real power flow equal to $P_{I1} = (V_{dc1} - V_{dc2})I_1$, violating ECC.

(a) (b)

Fig. 2-2. Primitive Case example A of power flow control using (a) a controllable current source I_1, or (b) a controllable voltage source V_1.

On the other hand, when one of the independent voltage sources is ac, as illustrated in Fig. 2-3, the instantaneous power absorbed by I_1 may be expressed as the product of the voltage across the I_1 branch and the total current through it,

$$S_{I1}(t) = \left(V_{dc} - \sqrt{2}V_{ac}\cos(\omega t)\right)\left(I_{dc} + \sqrt{2}I_{ac}\cos(\omega t + \phi)\right), \qquad 2\text{-}2$$

where the constants V_{dc} and I_{dc} represent the dc voltage and current; V_{ac} and I_{ac} represent the ac rms voltage and current; and ω and φ represent the fundamental ac frequency and power factor angle, respectively. $S_{I1}(t)$ can be simplified into the form $S_{I1}(t) = P_{I1} + Q_{I1}(t)$, where

$$P_{I1} = V_{dc}I_{dc} + V_{ac}I_{ac}\cos(\phi) \qquad 2\text{-}3$$

$$\text{and } Q_{I1}(t) = \sqrt{2}V_{dc}I_{ac}\cos(\omega t + \phi) + \sqrt{2}I_{dc}V_{ac}\cos(\omega t) + V_{ac}I_{ac}\cos(2\omega t + \phi). \qquad 2\text{-}4$$

The real power component $P_{I1}(t)$ may be made zero by maintaining a proper balance of dc and real ac power, while the reactive power $Q_{I1}(t)$ must be provided internally by I_1. Even though the power transfer function between the independent voltage sources may be realized as appropriate, the sources V_{ac} and V_{dc} incur significant reactive power flow (ac current through V_{dc} and vice-versa), since the sum of both ac and dc components flow

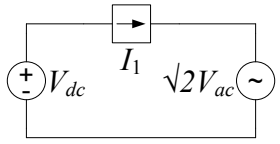


Fig. 2-3. Primitive Case example B of power flow control using a controllable current-stiff source I_1.

through each source. This behavior is rather undesirable and may not be supported by the independent sources.

If both sources are ac, as shown in Fig. 2-4, the general case permits power flow control between the sources using I_1, although a special case exists when the ac source frequencies are equal but the magnitudes of the voltages and phase of the voltages are arbitrary. This is analogous to two single-phase ac voltage sources in series with an inductor – a familiar circuit to power engineering – where the real power flow is controlled by the phase difference and the reactive power flow is controlled by the difference in voltage magnitudes.

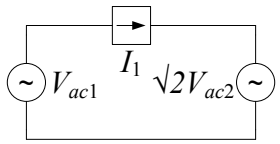


Fig. 2-4. Primitive Case example C of power flow control using a controllable current-stiff source I_1.

However, when the current-stiff source I_1 is an arbitrary 2-terminal device instead of an inductor, the behavior is not as intuitive. With the definitions

$$i_1(t) = \sqrt{2} I_1 \cos(\omega t + \varphi) \qquad 2\text{-}5$$

$$v_{ac1}(t) = \sqrt{2}V_{ac1}\cos(\omega t) \qquad 2\text{-}6$$

$$v_{ac2}(t) = \sqrt{2}V_{ac2}\cos(\omega t + \theta), \qquad 2\text{-}7$$

the instantaneous power is expressed as

$$\begin{aligned} S_{i1}(t) &= \sqrt{2}I_1\cos(\omega t+\phi)\left[\sqrt{2}V_{ac1}\cos(\omega t)-\sqrt{2}V_{ac2}\cos(\omega t+\theta)\right] \\ &= 2V_{ac1}I_1\cos(\omega t)\cos(\omega t+\phi)-2V_{ac2}I_1\cos(\omega t+\theta)\cos(\omega t+\phi) \\ &= V_{ac1}I_1\left[\cos(2\omega t+\phi)+\cos(\phi)\right]-V_{ac2}I_1\left[\cos(2\omega t+\theta+\phi)+\cos(\phi-\theta)\right] \\ &= V_{ac1}I_1\left[\cos(\phi)-\frac{V_{ac2}}{V_{ac1}}\cos(\phi-\theta)\right]\ldots \\ &\quad +V_{ac1}I_1\left[\cos(2\omega t+\phi)-\frac{V_{ac2}}{V_{ac1}}\cos(2\omega t+\phi+\theta)\right] \end{aligned} \qquad 2\text{-}8$$

or $S_{i1}(t) = P_{i1} + Q_{i1}(t)$, where

$$P_{i1} = V_{ac1}I_1\left[\cos(\phi)-\frac{V_{ac2}}{V_{ac1}}\cos(\phi-\theta)\right] \qquad 2\text{-}9$$

$$\text{and } Q_{i1}(t) = V_{ac1}I_1\left[\cos(2\omega t+\phi)-\frac{V_{ac2}}{V_{ac1}}\cos(2\omega t+\phi+\theta)\right]. \qquad 2\text{-}10$$

By Eq. 2-9, real power P_{i1} can only be conserved when

$$\theta = \varphi - \cos^{-1}\left(\frac{V_{ac1}}{V_{ac2}}\cos(\varphi)\right). \qquad 2\text{-}11$$

When this condition is satisfied, S_{i1} becomes purely reactive.

Similar to the ac-dc power transfer case, this case also leads to significant reactive power transfer across the independent voltage sources, which is rather undesirable and may not be supported by the independent sources.

In order to overcome the problem of reactive power loading from the independent sources, a bridge configuration may be used. The circuit shown in Fig. 2-5 shows four controlled current-stiff source branches I_1-I_4, in a full bridge configuration, which control power flow between V_{dc} and V_{ac}. The preceding discussion may be extended to show that such a configuration does not violate the ECC. This is also true when load and source are both ac but at different frequencies. Furthermore, the placement of dc and ac sources may readily be interchanged without violating the ECC.

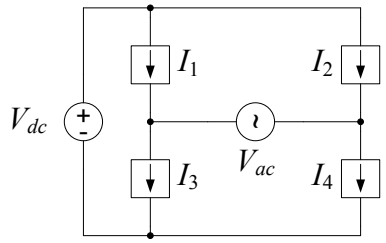


Fig. 2-5. Case example D with BoBC formed by controllable current-stiff sources $I_1 - I_4$.

Fig. 2-6 illustrates the current components among the converter branches with dc current as dashed gray loops and the fundamental ac current as solid gray loops. In this topology, while the controlled current branches carry both dc and the fundamental ac frequency, the current through V_{dc} is only at dc – purely dashed – and the current though V_{ac} is only at the ac fundamental frequency – purely solid. This behavior may be accomplished through careful control of the converter branches.

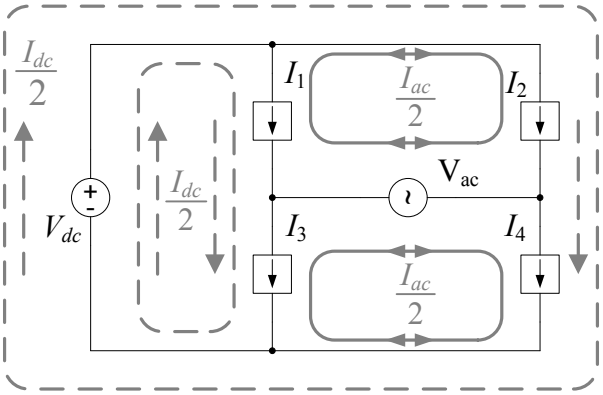


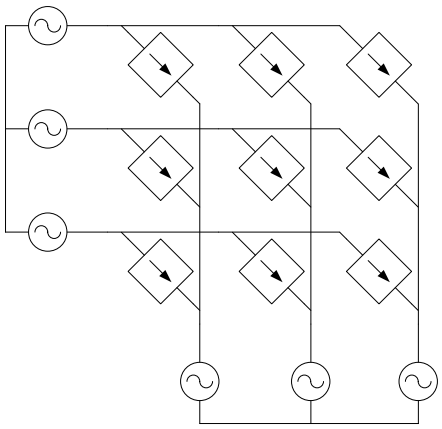
Fig. 2-6. Current flow in example dc-ac BoBC

These examples illustrate the role of the controlled current branch, which provides energy storage capability at multiple frequencies simultaneously while sourcing or sinking zero real power. Specifically, in Fig. 2-5, each controlled current branch sinks a specified amount of real power at dc while also sourcing the same amount of real power at the ac fundamental frequency to the load. This results in a net loss of real power in V_{dc} and a net gain of real power in V_{ac}. In other words, the power flow within the BoBC itself is purely reactive. As such, the amount of energy storage required for a given application is a function of how much power throughput is required and the frequencies at which the reactive power flows.

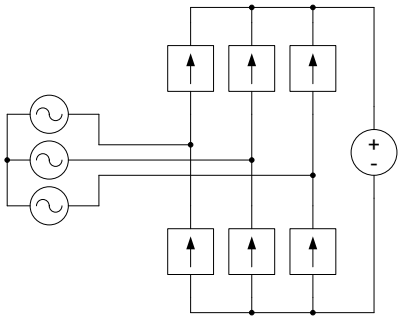
It is well-known in power engineering that bulk capacitors and inductors tend to decrease in size as the ac operating frequency increases due to a decreasing amount of energy stored per ac half-cycle. High ac frequencies are often desirable in BoBCs for the same reason, which effectively reduces energy storage requirements within the Q-cells. While conventional high-power converters utilize large components with significant parasitic elements, which limit operation to low ac frequencies, the BoBC is less

vulnerable to this frequency limitation; its multilevel and modular architecture permits the use of many lower-power converters built from smaller components with much smaller parasitic elements and therefore are capable of operating at significantly higher ac frequencies. This results in high-power, high-frequency converter designs with minimal internal energy storage, and is a key advantage of the BoBC topologies over conventional designs when the fundamental ac frequency is a free design parameter.

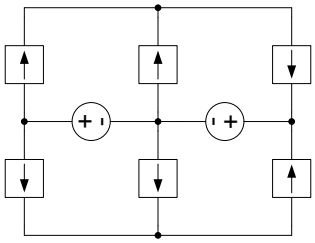
The BoBC approach may be used to realize larger, more sophisticated power conversion functions, such as a 3-phase ac-ac matrix converter, 3-phase ac-dc converter, and dc-dc converter with ac link, all illustrated in Fig. 2-7. It is worth reemphasizing that, although all of these examples show Q-cells functioning as controlled current source branches, Q-cells may also function as controlled voltage source branches. In fact, when the input and output are both independent current-stiff devices, power flow must be controlled using a controlled voltage source. The following section presents and examines many Q-cells that may be used for realizing both types of controlled branches.



(a)



(b)



(c)

Fig. 2-7. Several potential BoBC topologies. (a) 3-phase matrix converter, (b) 3-phase ac to dc converter, (c) dc-dc converter with ac link.

2.3 Q-cell types

BoBC Q-cells are actively controlled circuits that supply energy storage. As such, it is reasonable to assume that these circuits contain inductors, capacitors, and active and passive switches. The Q-cells may be built from these components into various forms of the capacitive storage embedded bridge (CSEB) and the inductive storage embedded bridge (ISEB) [95], with or without fault tolerance [28, 94], or even in multilevel configurations [31]. In fact, there is no limitation to the type of energy storage, nor the stiffness provided by each Q-cell. Therefore, an electromechanical energy storage bridge is also shown to demonstrate the flexibility of this converter architecture.

Besides the type of energy storage contained in the bridge, the bridges can also be classified according to the voltage and current polarities that may be accommodated at the two bridge terminals. This classification is made according to Fig. 2-8, in terms of bidirectional or unidirectional voltage (BV, UV) and bidirectional or unidirectional current (BC, UC). It is worth mentioning that unidirectional voltage and unidirectional current (UVUC) Q-cells are not possible due to the ECC. Further bridge classifications

may be established based on whether the bridges utilize unidirectional energy storage (UES) or bidirectional energy storage (BES).

The circuits shown in this section depict idealized conditions with SPDT switches as well as with IGBT switches. There is no limitation to how these switches are realized, and can involve the use of MOSFETs, IGCTs, or other self-commutating switching devices/circuits. How the switches are realized also depends on whether the energy

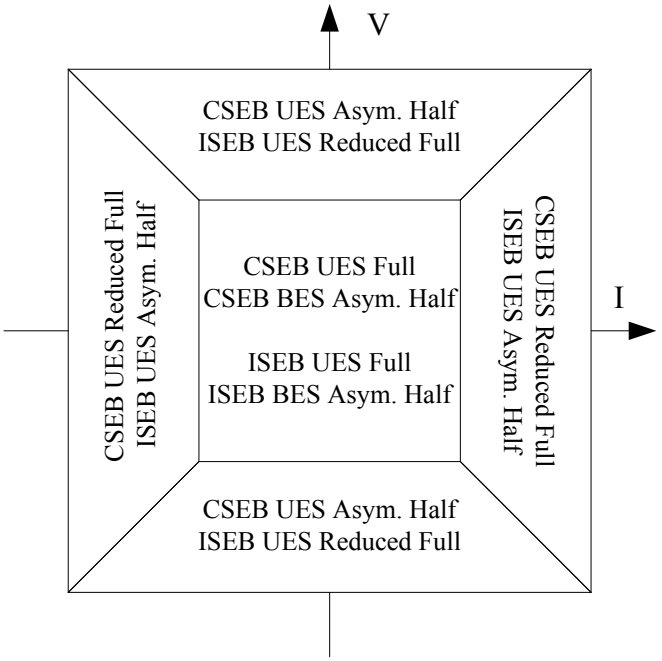


Fig. 2-8. Bridge terminal voltage and current characteristics of CSEB and ISEB Q-cell types.

storage is unidirectional or bidirectional, therefore realizations for both cases are shown in the following discussion.

2.3.1 CSEB full bridge

The CSEB full bridge is a current-stiff Q-cell that utilizes capacitive energy storage, as shown in Fig. 2-9. Its current-stiff nature requires that the Q-cell be placed across an effective voltage source to properly control the power flow. Depending on the position of the SPDT switches, the bridge can impart a positive, negative, or zero voltage on the circuit. Likewise, the bridge inductor current then imparts a positive, negative or zero change on the capacitor charge. The bridge capacitor and switches act as a controlled voltage source, imparting a voltage across L_B (dependent upon the surrounding circuit as well) in order to control i_B, in turn acting as a controlled current-stiff source. The SPDT switch positions illustrated are for switch values of 1. Realizations for the SPDT switches are illustrated in Fig. 2-10 and Fig. 2-11.

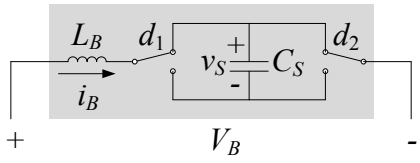


Fig. 2-9. CSEB full bridge circuit with ideal SPDT switches.

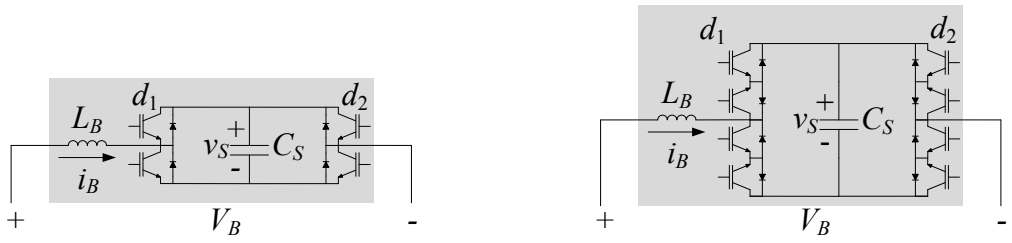


Fig. 2-10. CSEB full bridge circuit with SPDT switches realized using IGBT switches for (a) UES and (b) BES.

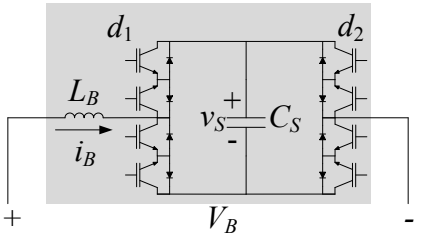


Fig. 2-11. An equivalent CSEB full bridge circuit with an alternative SPDT switch realization for BES.

The governing differential equations for the full bridge CSEB are:

$$L_B \frac{di_B}{dt} = V_B - d_B v_S \qquad 2\text{-}12$$

$$C_S \frac{dv_S}{dt} = d_B i_B, \qquad 2\text{-}13$$

where d_B represents the bridge duty cycle, a combination of both switch duty cycles:

$$d_B = d_1 - d_2. \qquad 2\text{-}14$$

The individual switch duty cycles are limited to $0 \le d_1 \le 1$ and $0 \le d_2 \le 1$, therefore the bridge duty cycle for the full bridge CSEB is limited to:

$$-1 \le d_B \le 1. \qquad 2\text{-}15$$

The full bridge CSEB terminals have no limitations regarding the direction of current flow, and as already mentioned, the terminals can have a positive or negative voltage. This bridge is therefore a BVBC bridge in both UES and BES versions. Since the UES full bridge CSEB has the same terminal characteristics as the BES full bridge CSEB while requiring fewer components, it would be the preferred realization.

2.3.2 CSEB semi-full bridge

In many applications where either the source or load is ac, full 4-quadrant operation may not be necessary; unidirectional terminal voltage or current may be sufficient. The semi-full bridge (SFB) can be used when bidirectional voltage and unidirectional current are required (BVUC). The IGBT realizations are shown in Fig. 2-12; its ideal SPDT switch model is identical to Fig. 2-9 because SPDT switches are not limited to any direction of current flow. BoBCs using the SFB may reverse the direction of power flow by reversing the polarity of terminal voltage, since the current polarity is fixed.

The governing differential equations for the SFB CSEB are identical to Eqs. 2-12 through 2-15 with the added limitation

$$i_B \geq 0. \qquad 2\text{-}16$$

Similar to the CSEB full bridge, the CSEB SFB has the same terminal characteristics in the UES and BES realizations, while the UES realization requires fewer components. The preferred realization is therefore the UES semi-full bridge CSEB.

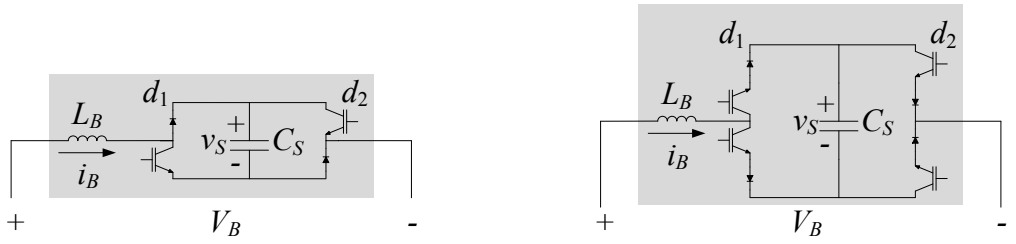


Fig. 2-12. CSEB semi-full bridge circuit IGBT realization for (a) UES and (b) BES.

2.3.3 CSEB half bridge

Another possible bridge circuit is the half bridge (HB) CSEB, as seen in Fig. 2-13 and Fig. 2-14. The UES bridge, in Fig. 2-14a, may only exhibit unidirectional terminal voltage, therefore by the ECC, the terminal current must be bidirectional. On the other hand, the BES bridge, in Fig. 2-14b, also requires bidirectional terminal current but for another reason – to provide bidirectional current to the capacitor. Therefore, the UES bridge is UVBC, while the BES bridge is BVBC.

This circuit also shares the governing equations 2-12 and 2-13, and has the limitation

$$0 \le d_B \le 1. \qquad 2\text{-}17$$

BoBCs using the HB may reverse the polarity of power flow by reversing the polarity of current, since the voltage polarity is fixed.

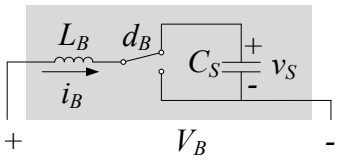


Fig. 2-13. CSEB HB circuit with an ideal SPDT switch.

(a) (b)

Fig. 2-14. CSEB HB with IGBT switches for (a) UES, and (b) BES.

2.3.4 ISEB full bridge

Applying circuit duality principles to the CSEB full bridge, one can arrive at the ISEB full bridge circuit of Fig. 2-15. The bridge is voltage-stiff with a controlled current-stiff source in parallel, imparting a zero average current through C_B, and as shown in Fig. 2-16, can be designed to utilize unidirectional or bidirectional current (UES or BES, respectively) in the energy storage inductor. Like the CSEB full bridge, the ISEB full bridge is capable of bidirectional bridge voltage and current (BVBC).

The governing equations for the full bridge ISEB are:

$$C_B \frac{dv_B}{dt} = I_B - d_B i_S \qquad 2\text{-}18$$

$$L_S \frac{di_S}{dt} = d_B V_B , \qquad 2\text{-}19$$

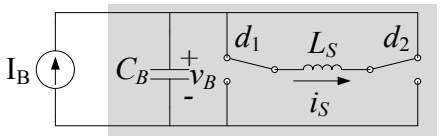
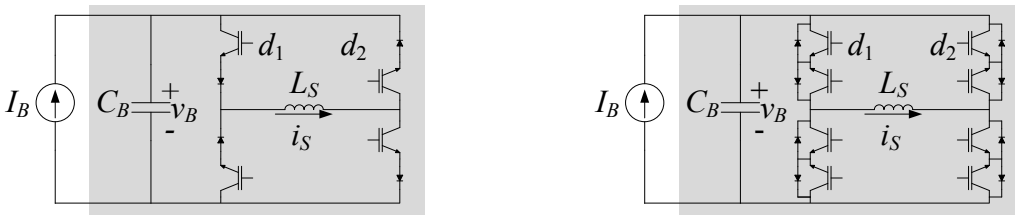


Fig. 2-15. ISEB full bridge circuit with an ideal SPDT switch.



(a) (b)

Fig. 2-16. ISEB full bridge with IGBT switches for (a) UES, and (b) BES.

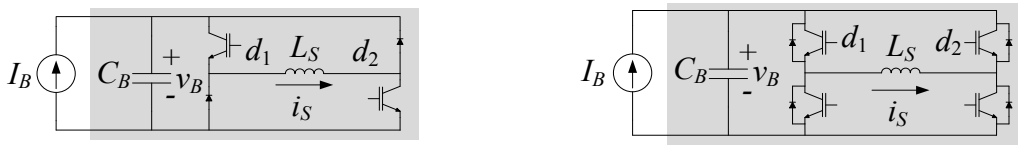
where d_B is defined as in Eq. 2-14 and 2-15. Similar to the full bridge CSEB, the full bridge ISEB achieves the same terminal characteristics regardless of whether using UES or BES realizations. Therefore, the UES full bridge ISEB is the preferred full bridge ISEB realization.

2.3.5 ISEB semi-full bridge

Similar to the reduction of the CSEB full bridge, the ISEB full bridge can be reduced to provide unidirectional bridge voltage and bidirectional bridge current (UVBC), seen in Fig. 2-17, with both UES and BES realizations. The governing equations are the same as the ISEB full bridge (Eqs. 2-18 and 2-19). In this case, the additional restriction becomes

$$v_B \geq 0 . \qquad 2\text{-}20$$

Because the UES realization achieves the same terminal characteristics as the BES realization, and requires fewer components, it is the preferred realization.



(a) (b)

Fig. 2-17. ISEB SFB circuit IGBT realization for (a) UES and (b) BES.

2.3.6 ISEB half bridge

Again in a similar fashion as the CSEB half bridge, the ISEB half bridge is shown in Fig. 2-18 and Fig. 2-19. Note that the bridge voltage must be bidirectional in order to maintain ECC for the UES realization. The bridge is therefore BVUC. When using BES, the terminal voltage still requires bidirectionality in order to impart a zero average voltage across the energy storage inductor.

The ISEB half bridge is governed by Eqs. 2-17 through 2-19 with the additional constraint

$$I_B > 0 \qquad \text{2-21}$$

for the UES realization.

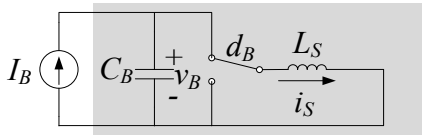
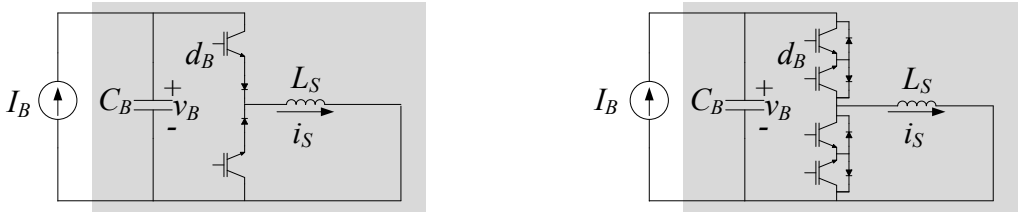


Fig. 2-18. ISEB HB with ideal SPDT switches.



(a) (b)

Fig. 2-19. ISEB half bridge circuit IGBT realization for (a) UES and (b) BES.

2.3.7 Q-cells for other energy storage types

The bridge energy storage need not be purely electrical; mechanical, chemical, or other energy storage methods are also theoretically possible. For example, a flywheel driven by a brushed permanent magnet (PM) dc motor is one possibility, shown in Fig. 2-20, with a minimal storage bus capacitance to provide adequate voltage stiffness in the presence of motor inductance. The Q-cell type may be freely modified to provide freedom in how the dc motor is connected (series, shunt, separately excited). Energy storage may also be provided by the terminal inductance (field and/or armature depending on connection type) in addition to the total rotor inertia. Further possibilities may lie in multiphase brushless rotating machine topologies, such as synchronous PM machines, other forms of electromechanical energy storage, or electrochemical energy storage such as batteries.

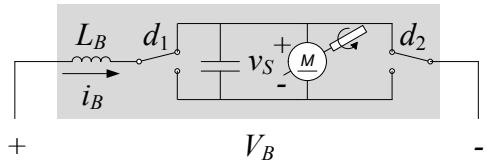


Fig. 2-20. Idealized electromechanical flywheel full bridge using dc machine.

2.3.8 Summary of Q-cell terminal characteristics

To help guide the designer in choosing the appropriate type of Q-cell for a given application, the terminal characteristics of all presented CSEB and ISEB Q-cells are

summarized in Table 2-1. The table shows whether any given Q-cell is capable of (C), or requires (R), unidirectional voltage (UV), bidirectional voltage (BV), unidirectional current (UC), or bidirectional current (BC) at its terminals. A blank indicates that the characteristic is not possible for that Q-cell.

Table 2-1. ISEB and CSEB Q-cell terminal characteristics using UES or BES. (R=Required, C=Capable, Blank=Impossible).

	UV	BV	UC	BC
CSEB UES Full Bridge	C	C	C	C
CSEB UES Semi-Full Bridge		R	R	
CSEB UES Half Bridge	R			R
CSEB BES Half Bridge	C	C		R
ISEB UES Full Bridge	C	C	C	C
ISEB UES Semi-Full Bridge	R			R
ISEB UES Half Bridge		R	R	
ISEB BES Half Bridge		R	C	C

2.4 CSEB vs. ISEB

One valuable method of quantifying the value of a particular converter topology is to compare its losses (efficiency) with other candidate topologies. For a given duty ratio, it can be seen by inspection that the ISEB exhibits higher losses than the CSEB due to the presence of additional semiconductors through which the inductor current must flow.

Should reverse-blocking IGBTs be used, rendering the additional semiconductors unnecessary, the ISEB still has the disadvantage of requiring significant inductance, which is generally more costly in volume, weight and monetary value than capacitance. Furthermore, for a duty ratio of zero – when the stored energy should not change – the CSEB incurs an energy loss due to the very small dc leakage current in its capacitor, whereas the ISEB incurs an energy loss due to the inductor ESR and the semiconductor voltage drop(s), which can be substantial. Therefore, the CSEB will be the generally preferred Q-cell type.

There are some situations when the CSEB may not be preferable. For example, a specific application may have current sources on the input and output, or other applications where a controlled voltage source is needed. Or, inductive energy storage may be a set requirement, such as when developing a converter for superconducting magnetic energy storage (SMES) systems [15].

Generally, however, the advantages of the CSEB outweigh those of the ISEB. Therefore, the remainder of this thesis focuses on the application of CSEBs to BoB power converter design.

2.5 Unidirectional vs. bidirectional energy storage

Generally, UES is preferred over BES. However, when deciding between the two, the BoBC designer should be aware of several key issues. First, for a given amount of terminal current or voltage, a BES Q-cell may use a smaller storage device than its UES

counterpart because the change in stored energy is permitted to be much greater in the bidirectional case.

However, as the purpose of a Q-cell is to store energy while modulating its terminal characteristics, the Q-cell must also have energy stored for it to perform its modulation function. In BES Q-cells, the stored energy will contain zero crossings, during which time the Q-cell is unable to modulate. These periods are brief but cannot be neglected. This limitation suggests the use of BES with resonant circuits at the converter terminals, because the zero crossings are expected and do not pose any functionality issues.

Third, the only BES bridge circuits presented here that also achieve a functional benefit compared to their UES counterparts are the CSEB and ISEB asymmetrical half bridges. However, the parts counts of both BES half bridge circuits are equal to those of the UES full bridges. Therefore, aside from the two points mentioned above, there is no benefit to using a BES Q-cell. Their use is therefore quite limited and is not considered any further.

2.6 Summary

The general function of a BoBC is to perform power conversion between multiple frequencies by realizing reactive power sources and sinks using Q-cells. This chapter has presented the minimal basic elements of BoBCs necessary for achieving this task, including the ECC and Q-cell interconnection guidelines. The topological structure of BoBCs was shown, as well as the fundamental principles for their operation resulting from this structure. Examples of simple BoBCs – both proper and improper – were

shown to illustrate the topological structure and the resulting current and power flows. More complex converters, such as the 3-phase matrix converter, 3-phase ac to dc converter, and dc-dc converter with ac link were illustrated.

The converter building blocks, known as Q-cells, mainly comprising the controlled current source (CSEB) and controlled voltage source (ISEB) were discussed, modeled and analyzed. A third type of block, the electromechanical flywheel full bridge, was also proposed to illustrate the flexibility of energy storage methods in generalized BoBCs. Finally, the merits and drawbacks of the CSEB and ISEB, for both UES and BES cases, were discussed and showed that the UES CSEB Q-cells are generally the preferred BoBC building blocks.

Chapter 3 Steady-State Scalar Modeling and Design of Practical BoBCs

This chapter presents two steady-state circuit models for practical, realizable BoBCs in a dc-ac configuration, which are based upon the CSEB circuit model originally proposed in [12] (the applicability to ac-dc conversion is a logical extension). The first model is a simplified analytical solution to the dynamic equations of the unidirectional capacitor voltage CSEB converter with sinusoidal excitation at the ac port. This simplified model is based on basic assumptions that generally hold true for typical design realizations of BoBCs. In the event that a particular converter design fails these simplifying assumptions, a more exact analytical solution to the circuit is also presented. Both models are useful for determination of component stresses and converter waveforms during the design phase, eliminating the need to perform tedious time-domain solutions in a circuit simulator.

A suitable scalar control methodology is also presented for maintaining the assumed frequency content of the simplifying assumptions. This control methodology lays the groundwork for additional modeling in later chapters.

In addition to presenting the BoBC theory of operation and derivations of solutions to various circuit models, this chapter also provides a nomogram-based design approach that makes the solutions presented herein into a convenient form useful for designers of

BoBCs. The design methodology is therefore presented in parallel with the theory, in order from the most simple and approximate forms, leading towards most accurate and therefore more complicated forms.

3.1 CSEB average circuit model

Building upon the dynamic model in Eqs. 2-12 and 2-13, the circuit model used herein is adapted from [12] and is reproduced in Fig. 3-1. Fig. 3-1a represents a single CSEB Q-cell, while Fig. 3-1b represents a branch comprising a n_s by n_p series-parallel combination of CSEB Q-cells respectively. This CSEB model is used to develop a model for an entire polyphase dc/ac converter, such as that shown in Fig. 2-5, with unidirectional capacitor voltage. The duty ratio d_B for a single CSEB may vary continuously between -1 and 1 for a full bridge (or 0 and 1 for an asymmetric half bridge) when using an averaged model, or may be replaced in the switching model with a switching function that is only equal to the values -1, 0 or 1 (likewise, 0 or 1 for an asymmetric half bridge).

As discussed in Chapter 2, the CSEB, or a collection of CSEB Q-cells in series/parallel combination, behaves as a controlled current source. This source is controlled by modulating the voltage across the bridge inductance, which in turn is accomplished by varying the product of the duty ratio and capacitor voltage. At first glance, it may seem that modulating the duty ratio sinusoidally will give a sinusoidal current output. To an extent this is true; however, the voltage drop across the branch inductance can be significant, which contributes to additional duty ratio frequency and

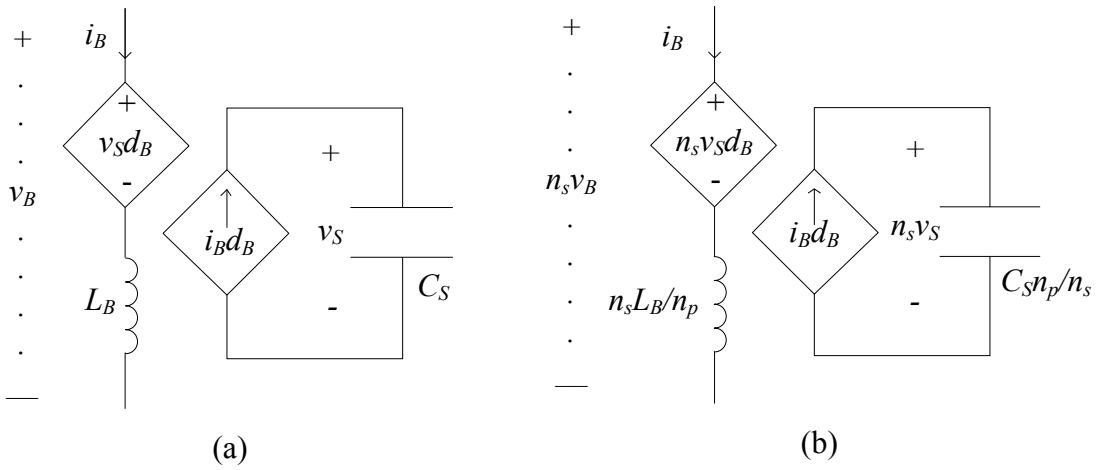


Fig. 3-1. Averaged CSEB model of (a) one Q-cell and (b) a series-parallel branch of n_s by n_p Q-cells.

phase components. Furthermore, the capacitor current is also a function of the duty ratio; therefore, the capacitor voltage is time-varying and if these variations are substantial, the resulting voltage across the inductor will contain additional, undesired frequency components, and thus so will the output current. Some of these variations will be accounted for in the complete analytical CSEB solution. However, under typical design conditions such as a stiff dc bus voltage and low bridge inductance (and/or low fundamental ac frequency), the model may be simplified and a sinusoidally varying duty ratio with an appropriate dc bias will often result in a satisfactory sinusoidal current output. Some higher order frequency effects are not practically feasible to implement, therefore a scalar control methodology will be presented which maintains the desired voltage and current waveforms by augmenting the open loop dc + fundamental ac duty ratio components.

3.2 BoBC Design Using Steady-State Analytical Averaged CSEB Solutions

As discussed in Chapter 2, the converter branches of a dc/ac BoBC carry dc and ac current components. Hence, the bridge current may be expressed as the sum of these components. The dc/ac BoBC shown in Fig. 3-2 with n_{br} branches connected to each dc terminal and an arbitrary and uniform number of CSEBs per branch (arms and/or strings) is now considered. Using the branch numbering scheme of the figure, where (j,k) represents the branch between dc source j and ac source k, total currents in branches (1,k) and (2,k), $i_{(1,k)}$ and $i_{(2,k)}$ respectively, are defined as

$$i_{(1,k)}(t) = \frac{I_{dc}}{n_{br}} + \frac{\sqrt{2}I_{ac}}{2}\cos\left(\omega_{ac}t - \varphi_{ac} - \frac{2\pi}{n_{br}}(k-1)\right) \qquad 3\text{-}1$$

$$i_{(2,k)}(t) = \frac{I_{dc}}{n_{br}} - \frac{\sqrt{2}I_{ac}}{2}\cos\left(\omega_{ac}t - \varphi_{ac} - \frac{2\pi}{n_{br}}(k-1)\right), \qquad 3\text{-}2$$

where I_{dc} and I_{ac} represent the constant magnitudes of the dc and ac currents as shown in the figure and φ_{ac} is the power factor angle. Throughout this work all converter voltage and current variables are expressed as rms quantities with respect to neutral. Using this topological approach, the constant $n_{br} \geq 2$, with index variable k bounded by $1 \leq k \leq n_{br}$. For brevity the ac phase offsets may be expressed as

$$\theta_k = \frac{2\pi}{n_{br}}(k-1). \qquad 3\text{-}3$$

The individual CSEB bridge currents in branches (1,k) and (2,k), $i_{B(1,k)}$ and $i_{B(2,k)}$ respectively, are then expressed as their total branch currents divided by the number of CSEBs (or CSEB strings) in parallel, n_p:

$$i_{B(1,k)}(t) = \frac{i_{(1,k)}(t)}{n_p} = \frac{I_{dc}}{n_{br} n_p} + \frac{I_{ac}}{\sqrt{2} n_p} \cos\left(\omega_{ac} t - \varphi_{ac} - \theta_k\right) \tag{3-4}$$

$$i_{B(2,k)}(t) = \frac{i_{(2,k)}(t)}{n_p} = \frac{I_{dc}}{n_{br} n_p} - \frac{I_{ac}}{\sqrt{2} n_p} \cos\left(\omega_{ac} t - \varphi_{ac} - \theta_k\right). \tag{3-5}$$

For calculating the branch voltages, i.e. the voltages across each branch, a definition is made wherein the neutral points of the dc and ac sides are set as the mean of both the dc and ac sources, respectively. Thus, the two nodes may be considered to nominally be at equipotential whether or not a galvanic connection exists. In this way, the branch voltages and currents are determined by relatively few circuit components and the remainder of the converter network can be neglected. Expressing the branch voltages of Fig. 3-2 using KVL yields

$$v_{(1,k)}(t) = V_{dc} - \sqrt{2} V_{ac} \cos\left(\omega_{ac} t - \theta_k\right) \tag{3-6}$$

$$v_{(2,k)}(t) = V_{dc} + \sqrt{2} V_{ac} \cos\left(\omega_{ac} t - \theta_k\right), \tag{3-7}$$

leading to the *external bridge voltage* definitions

$$v_{B(1,k)}(t) = \frac{V_{dc}}{n_s} - \frac{\sqrt{2} V_{ac}}{n_s} \cos\left(\omega_{ac} t - \theta_k\right) \tag{3-8}$$

$$v_{B(2,k)}(t) = \frac{V_{dc}}{n_s} + \frac{\sqrt{2} V_{ac}}{n_s} \cos\left(\omega_{ac} t - \theta_k\right), \tag{3-9}$$

where n_s denotes the number of CSEBs in series per branch.

The voltage produced by the controlled voltage source *within* each CSEB is termed the *internal bridge voltage* and is given by

$$v_{Bi(j,k)}(t) = d_{B(j,k)}(t) v_{S(j,k)}(t), \tag{3-10}$$

which may also be split into its dc and ac components

$$v_{Bi(j,k)}(t) = V_{Bi(j,k),dc} + \sqrt{2} v_{Bi(j,k),ac}(t). \tag{3-11}$$

The difference between the internal and external bridge voltages is the inductor voltage, which can be potentially neglected. This is discussed further in Section 3.2.3.

Finally, the real power components at the converter terminals are given by

$$P_{dc} = 2 V_{dc} I_{dc} \tag{3-12}$$

$$P_{ac} = V_{ac} I_{ac} n_{br} \cos(\phi_{ac}). \tag{3-13}$$

Furthermore, the currents and voltages associated with the other branches would differ only in their phase offsets in their ac components. Thus, all CSEBs and their constituent components can be assumed identical under balanced operating conditions. Therefore, the design process for component sizing is shown for branch (1,1) and the results are directly applicable to all other branches.

Included in Fig. 3-2 are the bus impedances Z_{dc} and Z_{ac} to represent source non-idealities and varying ac loads, respectively. Z_{dc} is included in particular for completeness because the BoBC does not require ideal sources to be connected to the CSEB terminals for achieving full functionality. However, its presence is neglected in the analysis of this work. Z_{ac}, on the other hand, plays an integral role within the BoBC power conversion functionality, primarily as the ac load resistance R_{ac}.

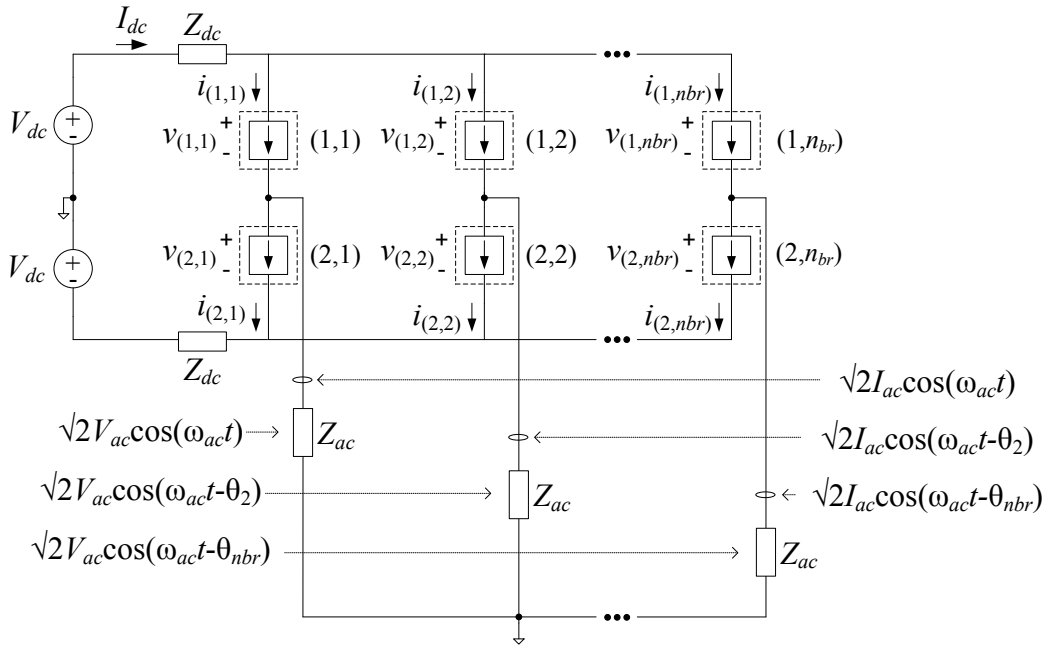


Fig. 3-2. Example polyphase dc/ac BoBC. The ac phase shifts of $(k-1)2\pi/n_{br}$ are abbreviated as θ_k for brevity.

The notional design procedure for the considered type of BoBC is shown in Fig. 3-3. The backbone for this procedure is the development of the simplified and improved average circuit models developed in this chapter. The remainder of this chapter is dedicated to the development of analytical models that accompany the notional design steps outlined in the figure.

3.2.1 Preliminary choice of CSEB type

A first-run determination of the type of CSEB to use in the converter may be made based purely on the desired terminal voltage and current of the BoBC. Eqs. 3-4 through 3-7 show that the instantaneous voltage and/or current may be purely positive, purely

negative, or bidirectional over time. Particular conversion schemes may require particular bridge configurations. For example, ac-ac conversion requires both bidirectional voltage and current capability, which would be reflected in the terminal voltage and current equations. Finally, certain bridge configurations may require multiple types of CSEBs, particularly those with more complex interconnections, such as in Fig. 2-7c.

Whatever the case, these terminal characteristics may be used to make a preliminary choice of which type of CSEB to use, and Table 2-1 may be used to guide this process. With the type of CSEB known, appropriate limits for d_B are now established and the components per Q-cell are known.

3.2.2 Q-cell design: custom or standard

The next step in designing a BoBC is deciding whether to use custom or standard Q-cell designs. The inherent modularity of the BoB approach encourages high volume production of these multipurpose bridge circuits, thus the design of new Q-cells may not be necessary as existing designs may already be available in the professional community. If existing Q-cell designs are available then the designer must calculate the number of Q-cells necessary to realize the branch terminal voltage and current specifications; in other words, calculate n_p and n_s in order to keep within the defined Q-cell limits.

Alternatively, if standard designs are not appropriate for the intended application, or are not available, then a new Q-cell design must be created. This provides the designer with even more flexibility but the starting point is less clear. For example, the branch

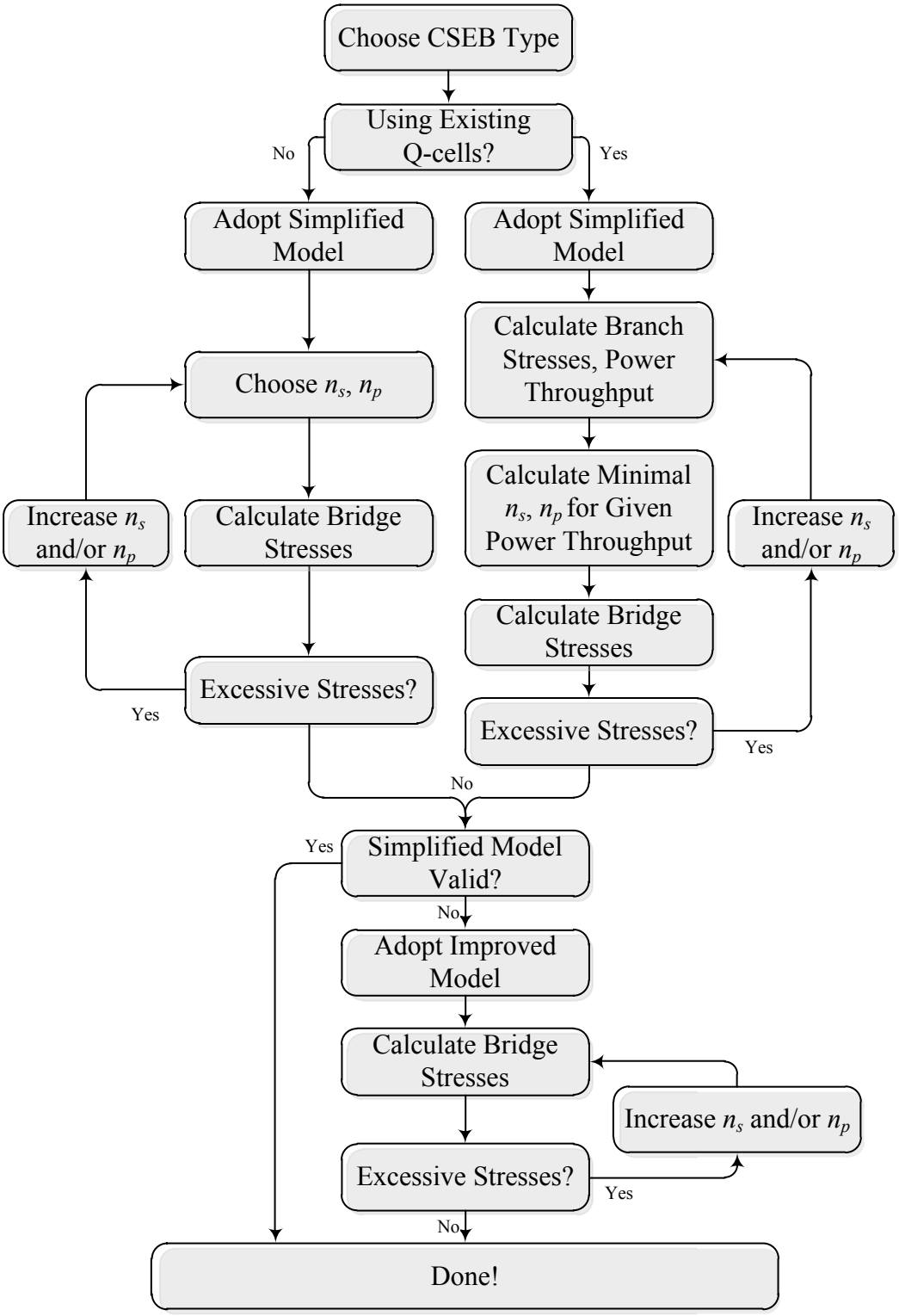


Fig. 3-3. Suggested BoBC design process using simplified and improved average circuit models.

terminal voltage and current ratings are known specifications, but the voltage and current per Q-cell (and likewise, the number of Q-cells comprising each branch) are free design variables.

A starting point may be achieved by considering the cost of the converter based on the Q-cell components; utilizing mass-produced components can significantly drive down the total converter cost. Metrics may thus be developed for calculating cost of Q-cell components, which can then be used to determine the number of Q-cells per converter branch. One example is a "cost per rated volt-amp" for finding inexpensive switching devices. Of course, other starting points may also be used depending on the circumstances.

In any case, after values for n_s and n_p have been selected, more accurate steady-state modeling may be used to calculate Q-cell component stresses.

3.2.3 Simplified model

A simplified mathematical model is developed based on two approximations and one assumption. First, the capacitor voltage always varies to some degree with time, however the capacitance is usually large such that the dc voltage component is far greater than the ac components. The first approximation is therefore

$$v_S(t) \approx \frac{V_{S,dc,tot}}{n_s}, \qquad 3\text{-}14$$

where $V_{S,dc,tot}$ is a constant that represents the sum total of dc capacitor voltages across the entire branch.

Referring back to Eq. 2-12, the bridge inductance and/or fundamental ac frequency is often small, therefore the inductive voltage drop may be neglected in comparison with the remaining voltage components of the loop. Using the example of converter (1,1), the second approximation is therefore

$$n_s v_{Bi(1,1)} = n_s v_{S(1,1)} d_{B(1,1)} \approx n_s v_{B(1,1)} = V_{(1,1)} = n_s V_{dc} - \sqrt{2} n_s V_{ac} \cos\left(\omega_{ac} t\right). \qquad 3\text{-}15$$

Combining Eqs. 3-14 and 3-15, the duty ratio d_B may be split into dc and ac components,

$$d_{B(1,1)}\left(t\right) = D_{B,dc} - \sqrt{2} D_{B,ac} \cos\left(\omega_{ac} t\right) = \frac{n_s V_{dc}}{V_{S,dc,tot}} - \frac{\sqrt{2} n_s V_{ac}}{V_{S,dc,tot}} \cos\left(\omega_{ac} t\right). \qquad 3\text{-}16$$

In order to maintain reasonable bounds on d_B, the capacitor voltage is chosen to be slightly greater than the minimum required value according to Eq. 3-15. A dc bus modulation variable M is used for this purpose, which is always less than unity and for worst-case design purposes, may be set to 0.9. This relationship may be expressed using the actual dc and ac bridge voltages or using the transfer ratio k_{tr},

$$V_{S,dc,tot} = \frac{1}{M}\left(n_s V_{dc} + \sqrt{2} n_s V_{ac}\right) = \frac{n_s V_{dc}}{M}\left(1 + \frac{\sqrt{2}}{k_{tr}}\right), \qquad 3\text{-}17$$

where k_{tr} is defined as

$$k_{tr} = \frac{V_{dc}}{V_{ac}} \approx \frac{n_{br} I_{ac} \cos\left(\phi_{ac}\right)}{2 I_{dc}}, \qquad 3\text{-}18$$

leading to the alternate duty ratio definition

$$d_{B(1,1)}\left(t\right) = \frac{M}{k_{tr} + \sqrt{2}}\left(k_{tr} - \sqrt{2}\cos\left(\omega_{ac} t\right)\right), \qquad 3\text{-}19$$

where the role of M as that of a *modulation index* becomes clear. These relationships provide appropriate approximations for d_B and $V_{S,dc,tot}$ based on given circuit voltages. Furthermore, the limits of d_B set by the choice of CSEB type can be verified. Eq. 3-14 may also be used to calculate an estimate of n_s based on capacitor voltage rating limits.

Note also that the ac/dc current relationships in Eq. 3-18 may not always hold true. For example, if each bridge consumes real power and/or derives its logic-level power from its power terminals, the input power would be greater than output power, leading to an imbalance in Eq. 3-18. However, the relationship in the equation remains useful for design purposes, assuming zero power draw on each CSEB.

Apparent power throughput per CSEB may also be calculated, which provides a reference for the amount of power processing capability required by each Q-cell. Starting with the rms values for the bridge voltage and current,

$$V_{B(j,k),rms} = \sqrt{V_{dc}{}^2 + 2V_{ac}{}^2} = V_{dc}\sqrt{1+\frac{2}{k_{tr}{}^2}} \qquad 3\text{-}20$$

$$I_{B(j,k),rms} = \sqrt{\left(\frac{I_{dc}}{n_{br}n_p}\right)^2 + \left(\frac{\sqrt{2}I_{ac}}{2n_p}\right)^2} = \frac{I_{dc}}{n_{br}n_p}\sqrt{1+\frac{2k_{tr}{}^2}{\cos\left(\phi_{ac}\right)^2}}\,, \qquad 3\text{-}21$$

the apparent power throughput of each CSEB is

$$S_{B(j,k),rms} = V_{B(j,k),rms} I_{B(j,k),rms}\,. \qquad 3\text{-}22$$

To aid in the design of each bridge, Eq. 3-18 may be used with the peak bridge current,

$$I_{B(j,k),\mathrm{pk}} = \frac{I_{dc}}{n_p n_{br}} + \frac{\sqrt{2}I_{ac}}{2n_p} \qquad 3\text{-}23$$

to determine the peak current using the relevant design parameters

$$I_{B(j,k),\mathrm{pk}} = \frac{I_{dc}}{n_p n_{br}}\left(1+\frac{\sqrt{2}k_{tr}}{\cos(\varphi_{ac})}\right). \qquad 3\text{-}24$$

3.2.3.1 Bridge capacitor design

The bridge capacitor is subjected to voltage and current stresses, which require quantification in order to apply them properly to realize their energy storage function. Once the capacitor current profile is known, the capacitance may be chosen to limit capacitor voltage excursions within acceptable limits during steady-state operation. The average voltage stress on an individual capacitor is already known, equal to $V_{S,dc,tot}/n_s$.

The individual capacitor current i_{Cs} may be calculated using Eqs. 2-13 and 3-4,

$$i_{Cs(1,k)}(t) = C_S\frac{dv_{S(1,k)}}{dt} = d_{B(1,k)}(t)\left(\frac{I_{dc}}{n_p n_{br}}+\frac{I_{ac}}{\sqrt{2}n_p}\cos(\omega_{ac}t-\phi_{ac}-\theta_k)\right), \qquad 3\text{-}25$$

which can be expressed using Eq. 3-16 as

$$\begin{aligned} i_{Cs(1,k)}(t) = {} & \frac{I_{dc}V_{dc1}}{n_{br}n_p n_s V_S} - \frac{I_{ac}V_{ac}}{2n_p n_s V_S}\cos(\phi_{ac}) + \frac{I_{ac}V_{dc1}}{\sqrt{2}n_p n_s V_S}\cos(\omega_{ac}t-\phi_{ac}-\theta_k)\ldots \\ & -\frac{\sqrt{2}I_{dc}V_{ac}}{n_{br}n_p n_s V_S}\cos(\omega_{ac}t-\theta_k) - \frac{I_{ac}V_{ac}}{2n_p n_s V_S}\cos(2\omega_{ac}t-\phi_{ac}-2\theta_k)\ . \end{aligned} \qquad 3\text{-}26$$

The first two terms are both time invariant and, when integrated over time, reflect the converter energy balance. Therefore, when the ECC is observed, these terms cancel and leave the time varying terms. For unity (or near-unity) power factor, the time varying components reduce to

$$i_{Cs(1,k)}(t) = \left(\frac{I_{ac} V_{dc1}}{\sqrt{2} n_p n_s V_S} - \frac{\sqrt{2} I_{dc} V_{ac}}{n_p n_s n_{br} V_S} \right) \cos(\omega_{ac} t - \theta_k) - \left(\frac{I_{ac} V_{ac}}{2 n_p n_s V_S} \right) \cos(2\omega_{ac} t - 2\theta_k) \ . \quad 3\text{-}27$$

For simplicity, this expression may be normalized in terms of k_{tr}. Assuming near-unity power factor and zero bridge losses, the parameter is equal to

$$k_{tr} = \frac{V_{dc}}{V_{ac}} \approx \frac{n_{br} I_{ac}}{2 I_{dc}} . \quad 3\text{-}28$$

Rewriting the capacitor current in terms of k_{tr} , M and I_{dc} yields

$$i_{Cs(1,k)}(t) = I_{base} \ i_{Cs(1,k),norm}(t), \quad 3\text{-}29$$

where the base current is

$$I_{base} = \frac{I_{dc}}{n_{br} n_p} \quad 3\text{-}30$$

and the normalized capacitor current is

$$i_{Cs(1,k),norm}(t) = \frac{M}{k_{tr} + \sqrt{2}} \left[\sqrt{2} \left({k_{tr}}^2 - 1 \right) \cos(\omega_{ac} t - \theta_k) - k_{tr} \cos(2\omega_{ac} t - 2\theta_k) \right]. \quad 3\text{-}31$$

The capacitor rms current, similarly normalized to I_{base}, is expressed as

$$i_{Cs,rms,norm} = \frac{M}{k_{tr} + \sqrt{2}} \sqrt{{k_{tr}}^4 - \frac{3}{2} {k_{tr}}^2 + 1} \ . \quad 3\text{-}32$$

An illustration of $i_{Cs(1,1),norm}$ as a function of the electrical angle with $M = 0.9$ is shown in Fig. 3-4. It may readily be observed that the shape, rms, and peak values (indicated by a circle along each waveform) all vary with k_{tr}, with a minimum occurring at $k_{tr} = 1$. It

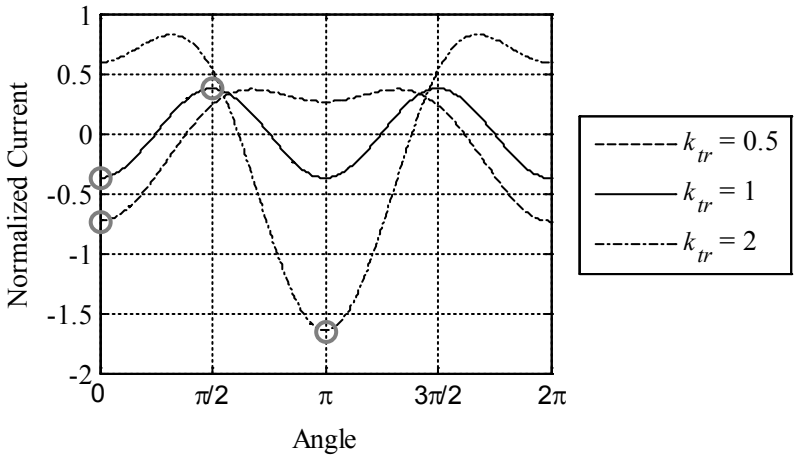


Fig. 3-4. Variation of capacitor current vs. electrical angle for 3 values of transfer parameter k_{tr}. The 4 circled locations indicate the occurrence of peak current values.

may also be observed that the location of the peaks may occur at different electrical angles depending on the value of k_{tr}.

These quantities are also illustrated in Fig. 3-5, which shows their dependency on k_{tr}. The figure clearly shows that choosing a k_{tr} near 1 minimizes capacitor current excursions and hence minimizes variations in the stored charge in the capacitor.

If the assumption of unity power factor is invalid, the capacitor current equation becomes more complex and is rather less insightful for design purposes. Therefore, charts which illustrate the dependency of $i_{Cs,peak,norm}$ and $i_{Cs,rms,norm}$ on k_{tr} and power factor are plotted conveniently using nomograms shown in Fig. 3-6 and Fig. 3-7, respectively.

After using the figures to find the necessary normalized quantities, they may be scaled and redimensionalized by I_{base},

$$i_{Cs,peak} = I_{base}\, i_{Cs,peak,norm} \qquad 3\text{-}33$$

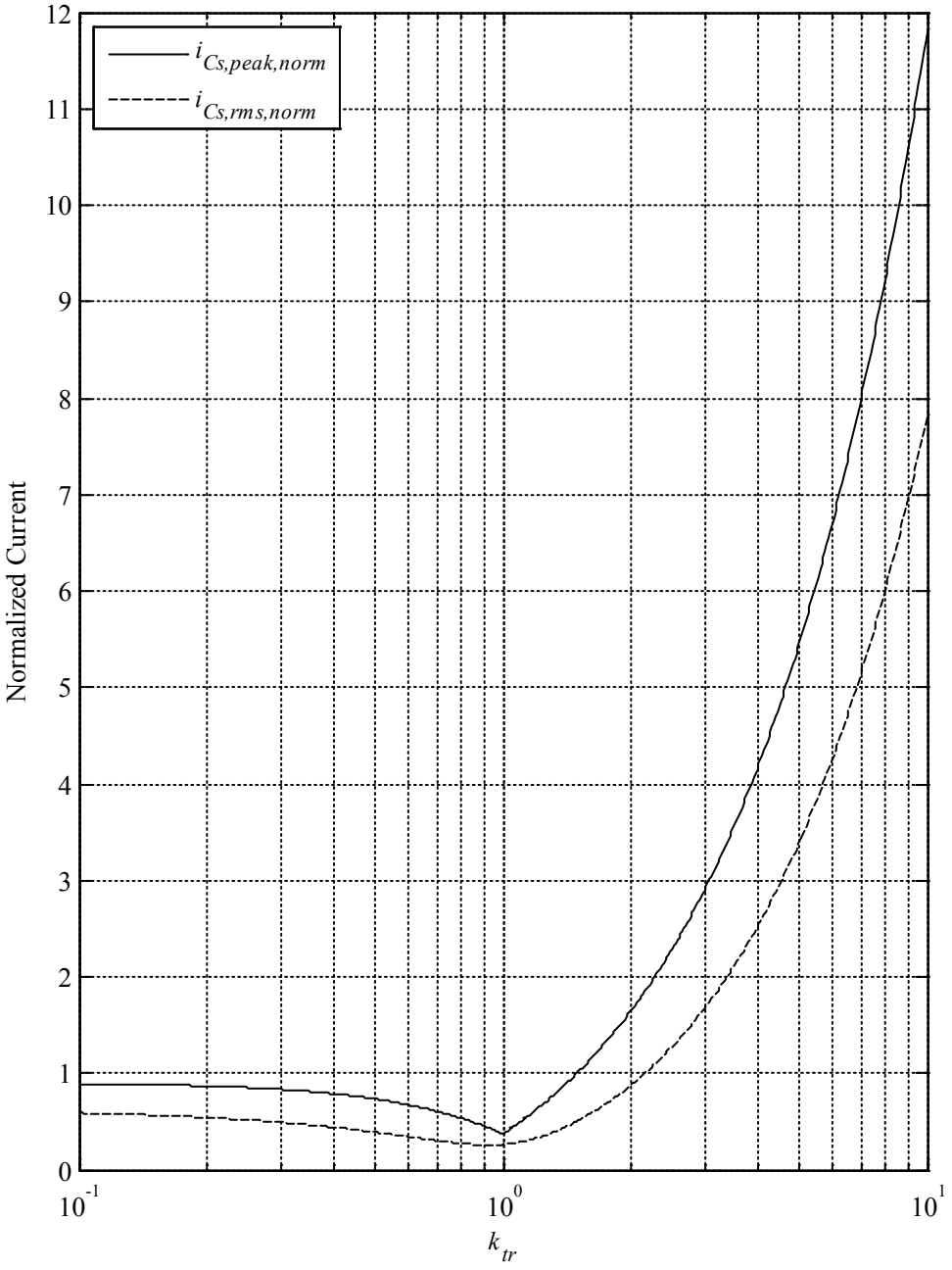


Fig. 3-5. Variations of important storage capacitor sizing quantities at unity power factor for different values of k_{tr}, all normalized to I_{base}. This figure assumes $M = 0.9$ but other values may be extracted by linearly scaling, e.g. $M = 0.3$ curves may be found by multiplying the y-axis by 0.3/0.9=1/3.

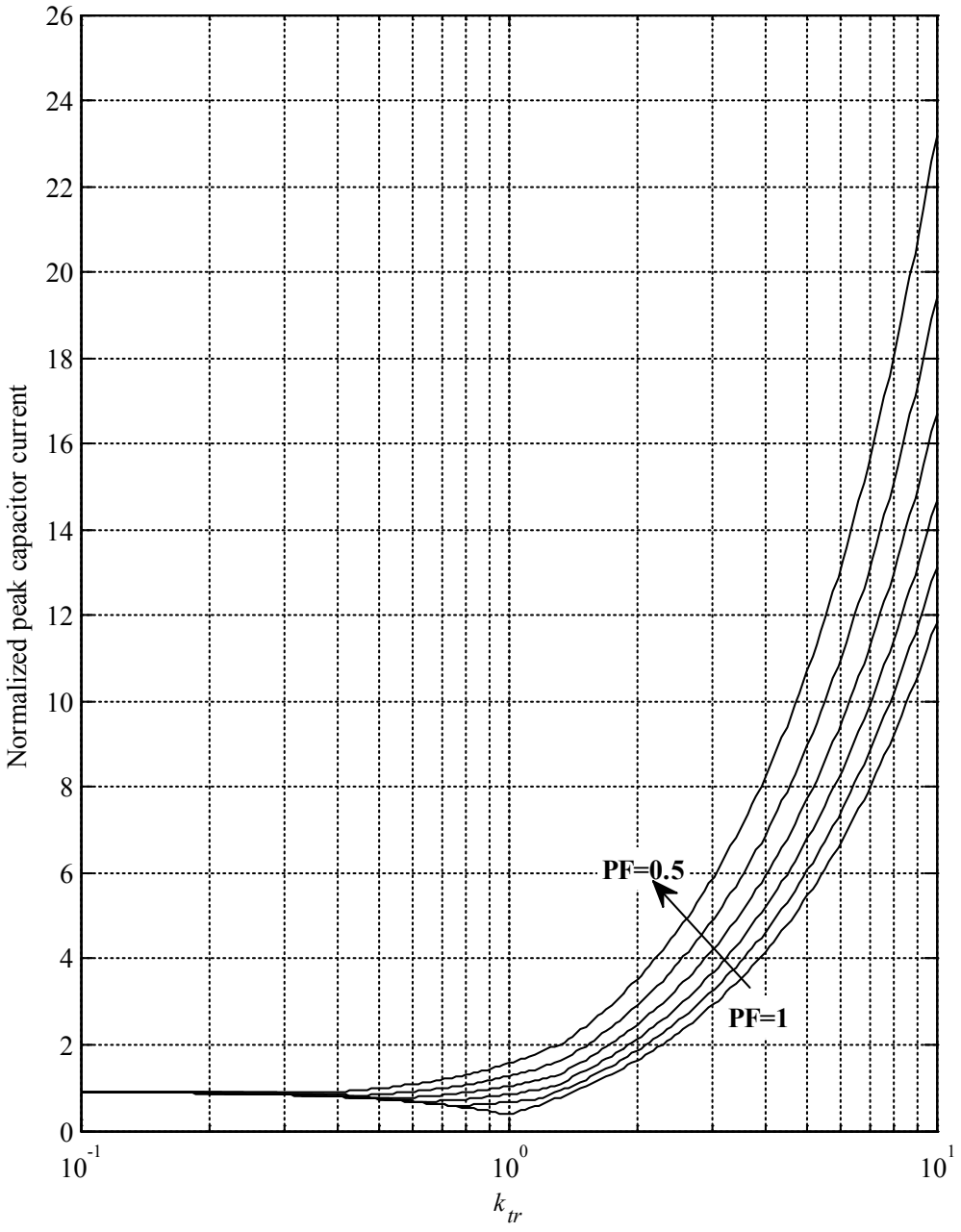


Fig. 3-6. Variation of peak capacitor current $i_{Cs,peak,norm}$ values as a function of k_{tr}, normalized to I_{base}, and with linearly decreasing power factor. The minimum normalized current is 0.37 at k_{tr} = 1 and unity power factor.

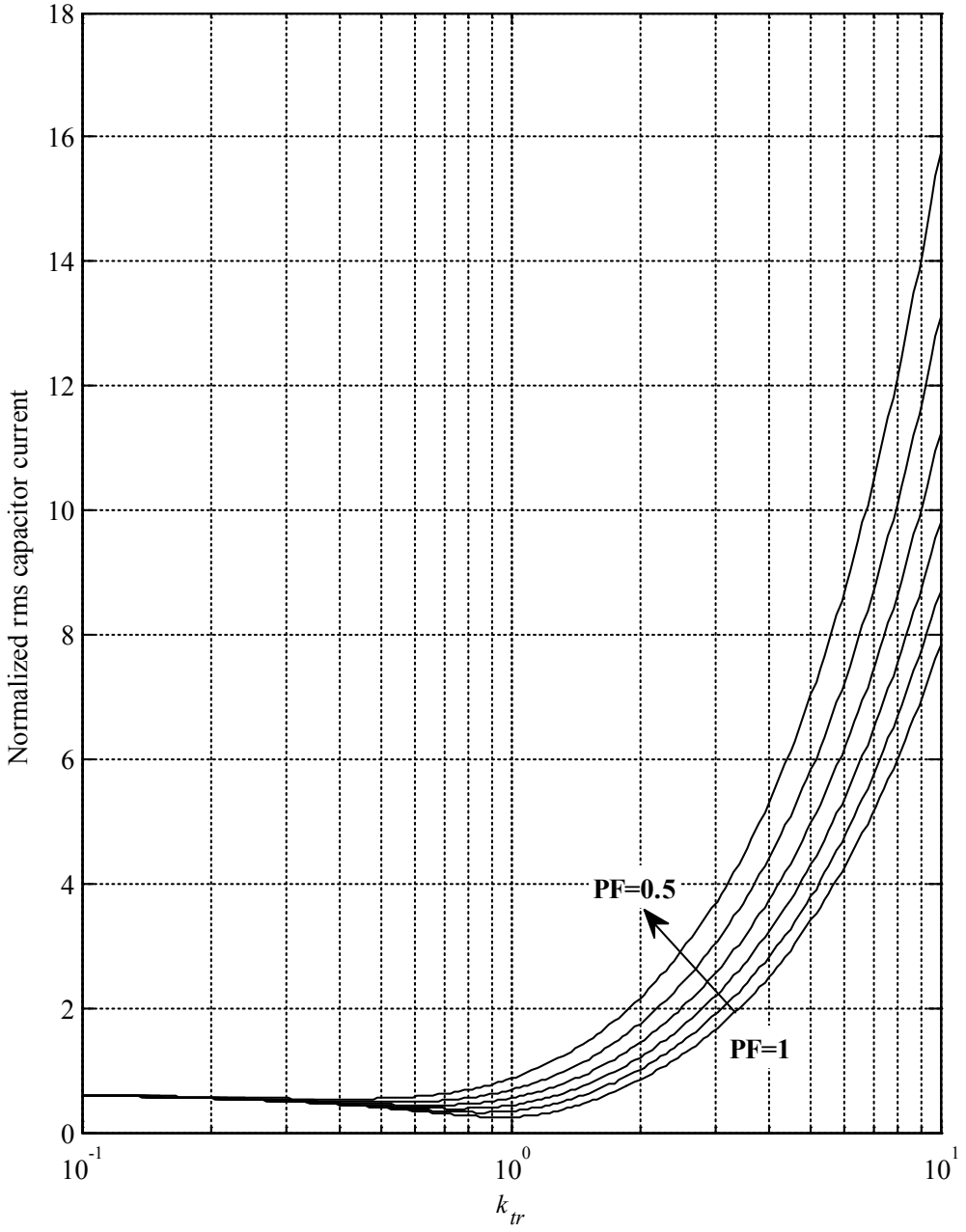


Fig. 3-7. Variation of rms capacitor current $i_{Cs,rms,norm}$ values as a function of k_{tr}, normalized to $I_{Cs,norm}$, and with linearly decreasing power factor. The minimum normalized current is 0.26 at k_{tr} = 0.93 and unity power factor.

$$i_{Cs,rms,norm} = I_{base}\, i_{Cs,rms,norm}\,. \qquad 3\text{-}34$$

3.2.3.2 Bridge switch sizing

The bridge switches (and diodes) are also subject to voltage and current stress and must be sized accordingly. Neglecting secondary effects such as ringing due to stray inductance and capacitor ESR, the maximum instantaneous voltage across any switch in a CSEB is V_S.

For calculation of switch thermal stresses under steady-state operation, the average switch current is used, which may be calculated using the average model presented in this chapter in conjunction with the circuit diagrams of Fig. 3-8. First, the average device currents for the asymmetrical half bridge are calculated, followed by those of the full bridges.

The asymmetrical half bridge upper switch and diode share the capacitor current, which was previously derived, in the negative and positive directions, respectively. The

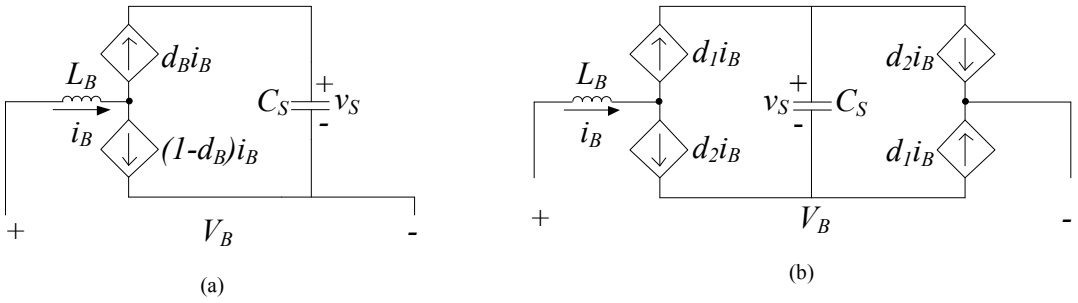


Fig. 3-8. Average model for calculating average voltages and currents of switches in the CSEB (a) asymmetrical half bridge and (b) full bridge and semi-full bridge.

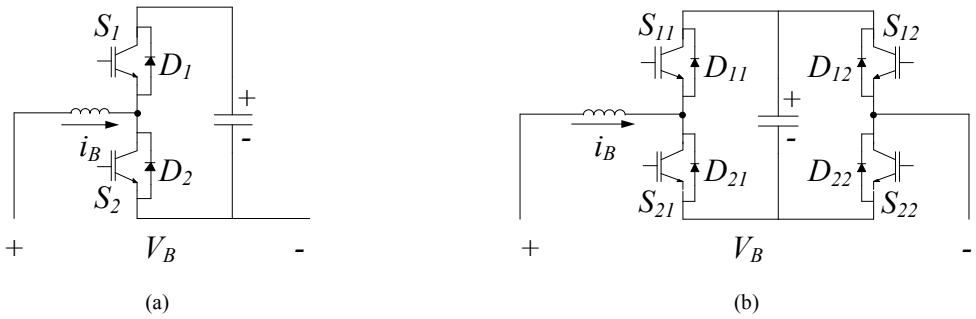


Fig. 3-9. Switch and diode naming of (a) asymmetrical half bridge and (b) full bridge or semi-full bridge CSEBs.

combined upper switch and diode current may be expressed for any power factor angle as

$$d_B i_B = I_{base} \frac{M}{k_{tr} + \sqrt{2}} \left(k_{tr} - \sqrt{2}\cos(\omega_{ac} t)\right)\left(1 + \frac{\sqrt{2} k_{tr}}{\cos(\varphi_{ac})}\cos(\omega_{ac} t - \varphi_{ac})\right). \quad 3\text{-}35$$

Likewise, the lower switch and diode share the difference of the bridge and capacitor currents, in the positive and negative directions, respectively, leading to the expression

$$(1 - d_B) i_B = I_{base}\left[1 - \frac{M\left(k_{tr} - \sqrt{2}\cos(\omega_{ac} t)\right)}{k_{tr} + \sqrt{2}}\right]\left(1 + \frac{\sqrt{2} k_{tr}}{\cos(\varphi_{ac})}\cos(\omega_{ac} t - \varphi_{ac})\right). \quad 3\text{-}36$$

Of course, each dependent current source in Fig. 3-8 represents one switch and one diode, as represented in Fig. 3-9. Because each device only permits current flow in one direction, the device currents may be separated into their positive and negative polarities:

$$i_{S1} = -d_B i_B u(-d_B i_B) \quad 3\text{-}37$$

$$i_{D1} = d_B i_B u(d_B i_B) \quad 3\text{-}38$$

$$i_{S2} = (1 - d_B) i_B u((1 - d_B) i_B) \quad 3\text{-}39$$

$$i_{D2} = (d_B - 1) i_B u((d_B - 1) i_B). \quad 3\text{-}40$$

Calculating the time average of the normalized instantaneous currents for each device yields curves such as those in Fig. 3-10 through Fig. 3-12. A worst-case value of $M = 0.9$ was again chosen for the figures. Note that because the average current through a capacitor is always zero, S1 and D1 average currents must be equal, as shown in Fig. 3-10. Curves representing the normalized rms device currents can be found in Appendix A.

In the case of the full bridge CSEB, the average switch currents may be affected by the modulation technique employed because any given switch current depends on either d_1 or d_2, not on d_B, and is therefore sensitive to the use of "zero states" where $d_1 = d_2$. To aid in the design process, this work assumes that the simplest possible modulation method is used, where $d_1 = 1 - d_2$ and zero states are not employed. This modulation scheme results in the duty ratios

$$d_1 = \frac{1}{2} + \frac{d_B}{2} \tag{3-41}$$

$$d_2 = \frac{1}{2} - \frac{d_B}{2}. \tag{3-42}$$

The currents may then be calculated as

$$d_1 i_B = I_{base}\left[\frac{1}{2} + \frac{M\left(k_{tr} - \sqrt{2}\cos(\omega_{ac}t)\right)}{2\left(k_{tr} + \sqrt{2}\right)}\right]\left(1 + \frac{\sqrt{2}k_{tr}}{\cos(\varphi_{ac})}\cos(\omega_{ac}t - \varphi_{ac})\right) \tag{3-43}$$

$$d_2 i_B = I_{base}\left[\frac{1}{2} - \frac{M\left(k_{tr} - \sqrt{2}\cos(\omega_{ac}t)\right)}{2\left(k_{tr} + \sqrt{2}\right)}\right]\left(1 + \frac{\sqrt{2}k_{tr}}{\cos(\varphi_{ac})}\cos(\omega_{ac}t - \varphi_{ac})\right), \tag{3-44}$$

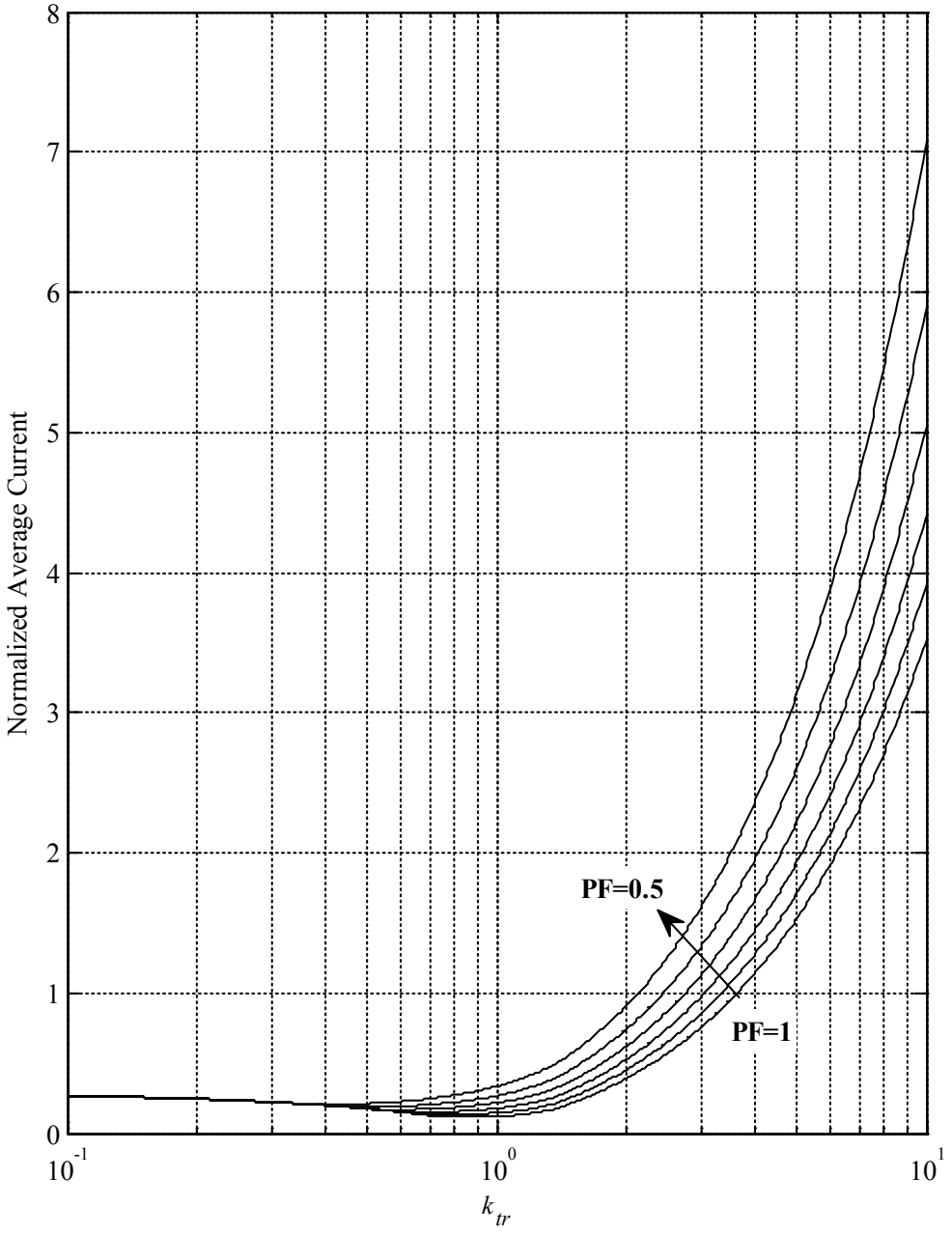


Fig. 3-10. Variation of normalized average current through S1 or D1 as a function of k_{tr} for $M = 0.9$ and varying power factor. The minimum value is approximately 0.11 at $k_{tr} = 0.86$ and unity power factor.

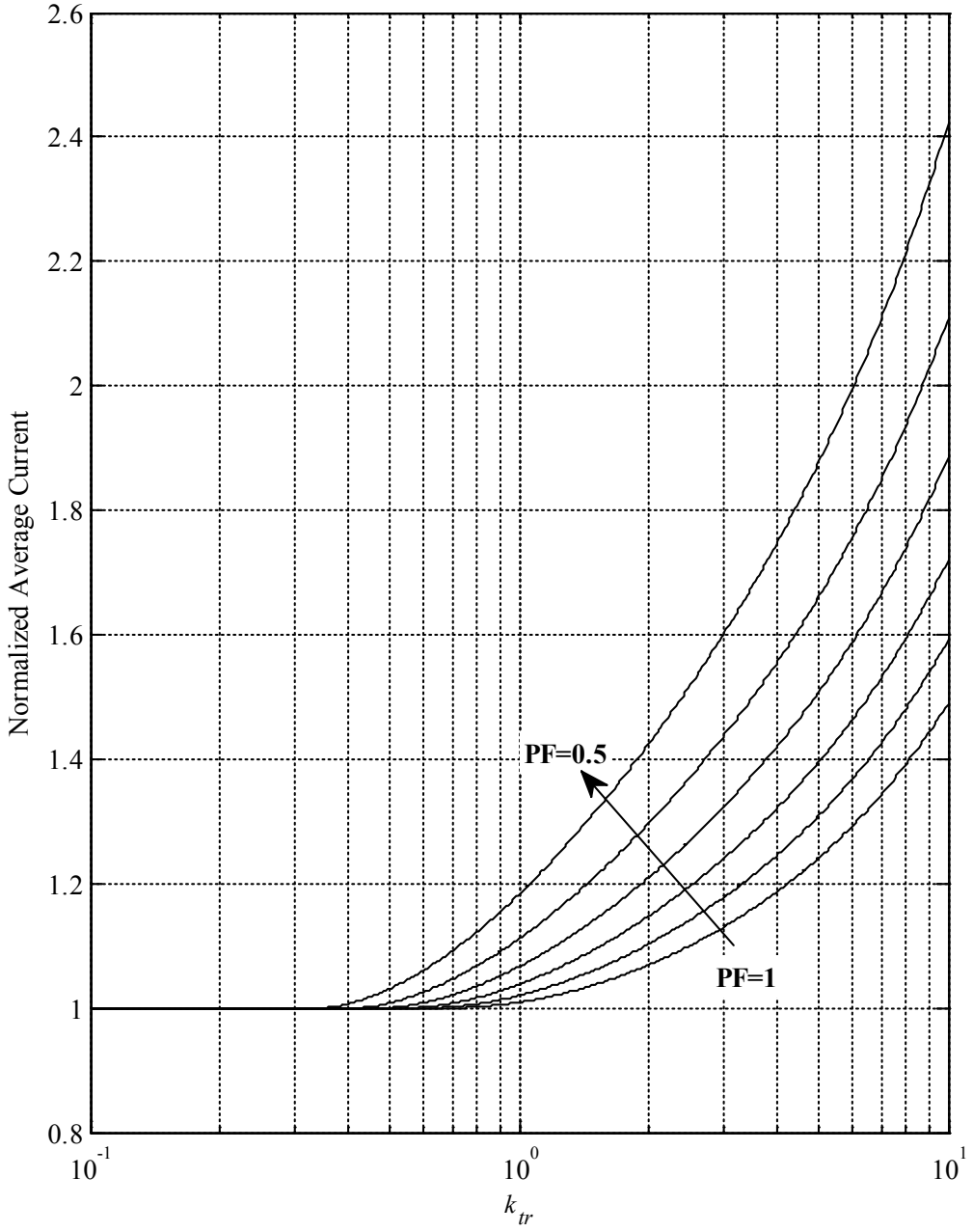


Fig. 3-11. Variation of normalized average current through S2 as a function of k_{tr} for $M = 0.9$ and varying power factor. The minimum value is 1.

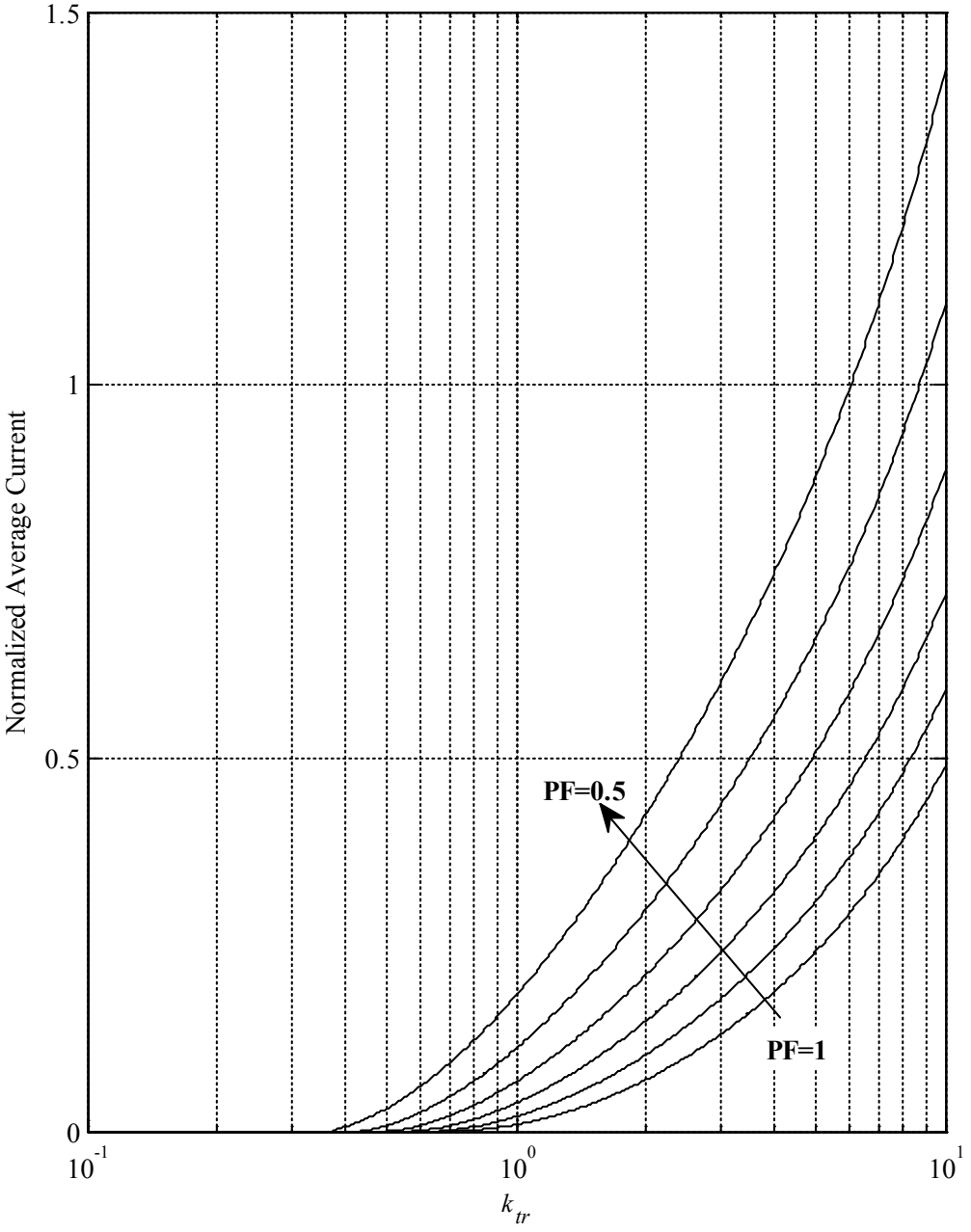


Fig. 3-12. Variation of normalized average current through D2 as a function of k_{tr} for $M = 0.9$ and varying power factor. The minimum value is 0, encountered at $k_{tr} = 0.707$ for unity power factor.

which are then split among the 8 devices with the relations

$$i_{S11} = i_{S22} = -d_1 i_B u(-d_1 i_B) \quad 3\text{-}45$$

$$i_{D11} = i_{D22} = d_1 i_B u(d_1 i_B) \quad 3\text{-}46$$

$$i_{S21} = i_{S12} = d_2 i_B u(d_2 i_B) \quad 3\text{-}47$$

$$i_{D21} = i_{D12} = -d_2 i_B u(-d_2 i_B). \quad 3\text{-}48$$

The normalized average device currents are shown in Fig. 3-13 through Fig. 3-16.

Particular attention should be paid to where the curves of the figures intersect zero current – if a power converter is designed to always operate with zero current in certain components, those components can be eliminated. These figures represent the current through S11, S22, D12 and D21, which form the difference between the CSEB full bridge and semi-full bridge. Therefore, these figures may be used to determine which full bridge CSEB circuit to use based on the known circuit constraints such as ac voltage, dc voltage and power factor. A figure summarizing these considerations into a comprehensive map of which CSEBs can be used for given values of k_{tr} and power factor is shown in Fig. 3-17. Figures of the normalized rms device currents can be found in Appendix B.

3.2.1 Improved accuracy model

Once the basic operating conditions and component ratings of the converter have been established with the simplified average model, if the key assumptions turn out to be invalid, an improved accuracy average model may be used. This model is an analytical

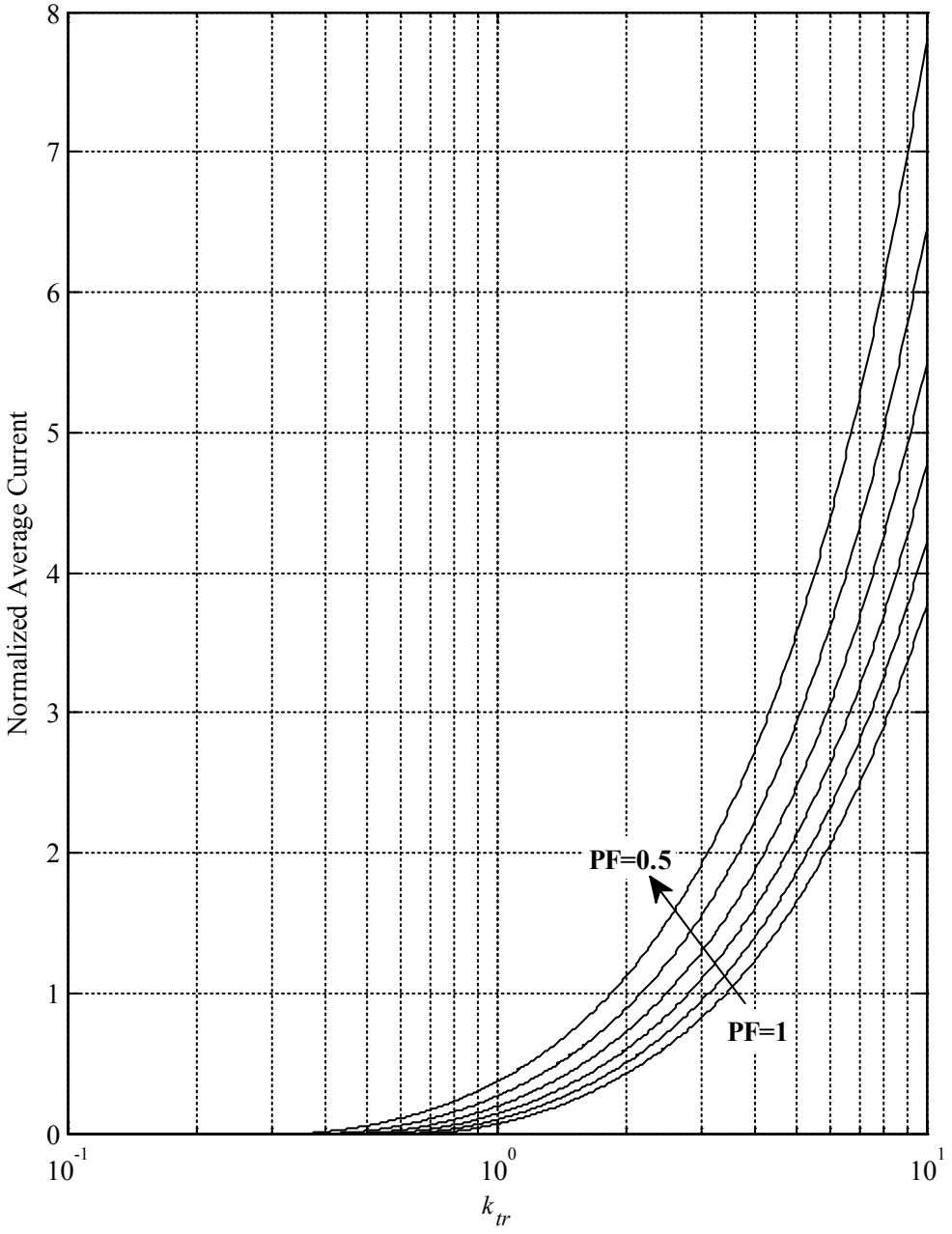


Fig. 3-13. Variation of normalized average current through S11 or S22 as a function of k_{tr} for $M = 0.9$ and varying power factor. The minimum value is 0, encountered at $k_{tr} = 0.707$ for unity power factor.

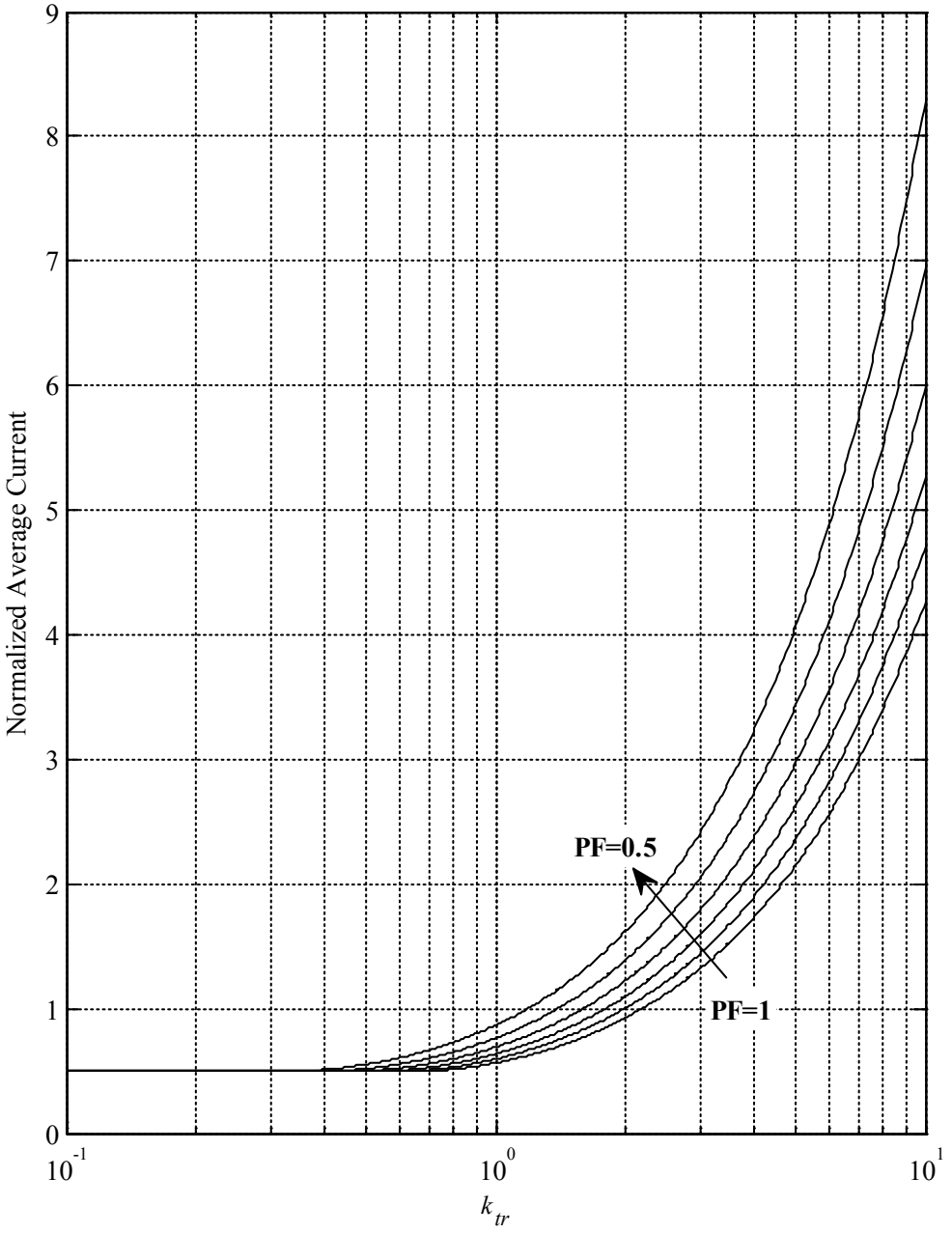


Fig. 3-14. Variation of normalized average current through D11 or D22 as a function of k_{tr} for $M = 0.9$ and varying power factor. The minimum value is 0.5.

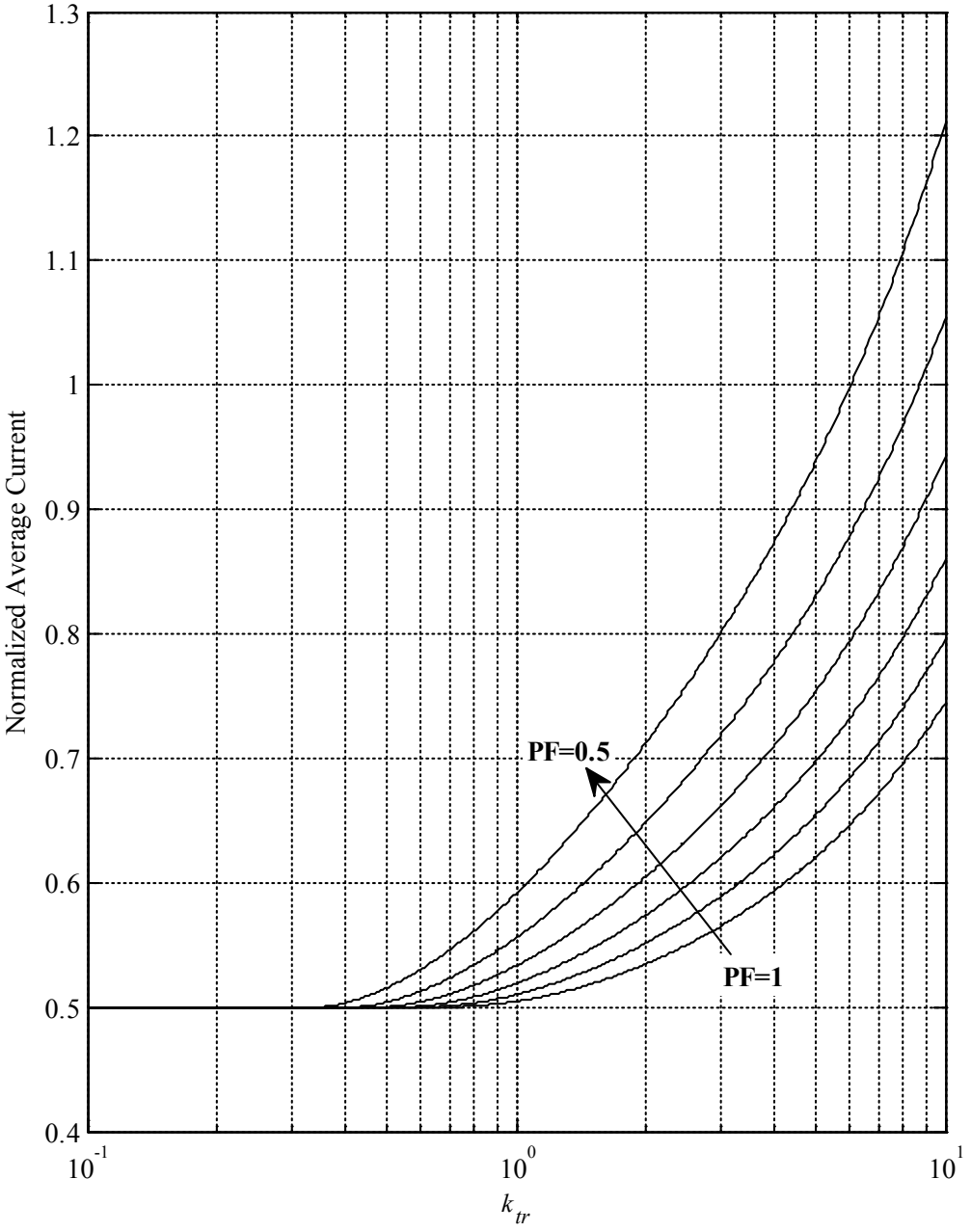


Fig. 3-15. Variation of normalized average current through S21 or S12 as a function of k_{tr} for $M = 0.9$ and varying power factor. The minimum value is 0.5.

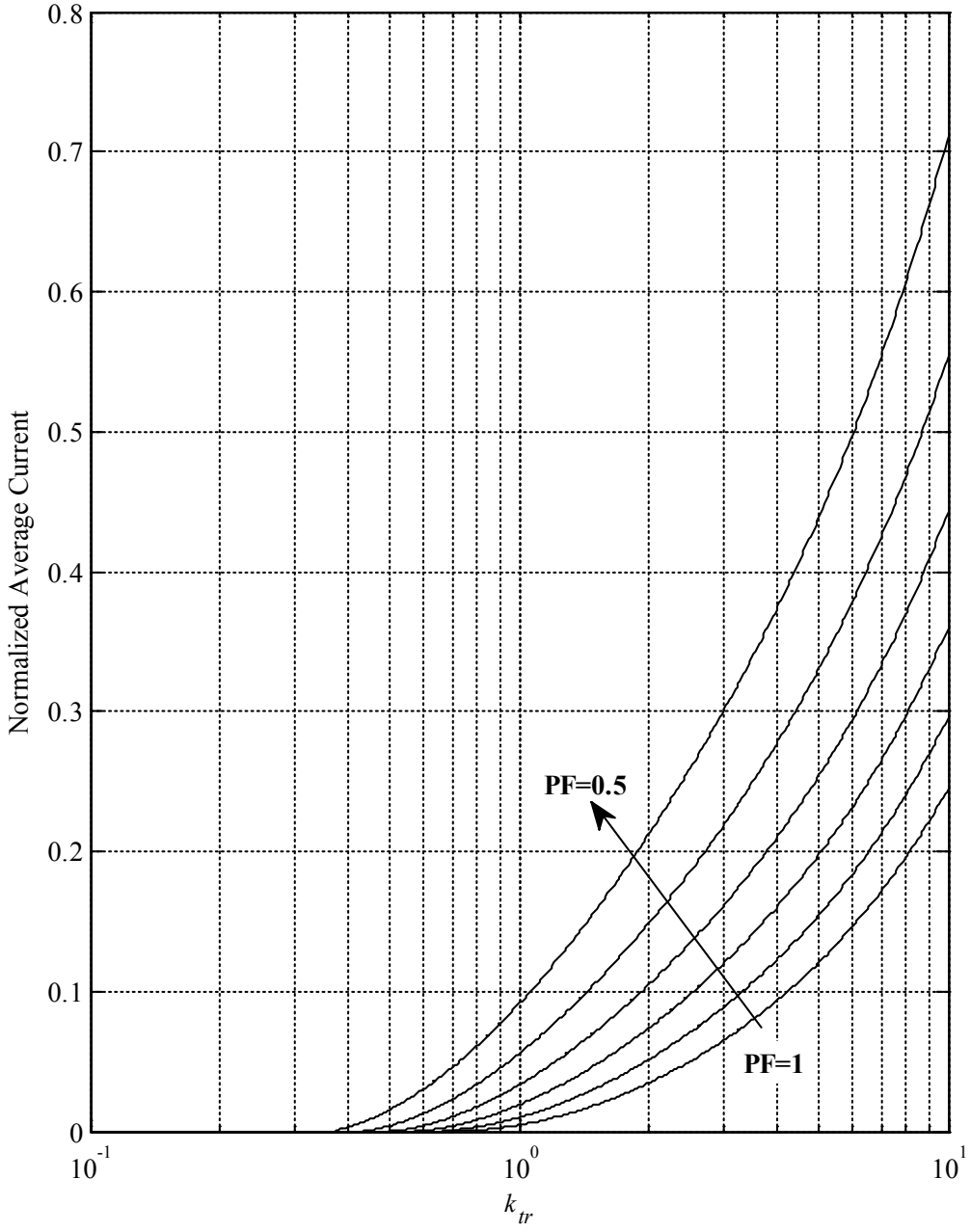


Fig. 3-16. Variation of normalized average current through D21 or D12 as a function of k_{tr} for $M = 0.9$ and varying power factor. The minimum value is 0, encountered at $k_{tr} = 0.707$ for unity power factor.

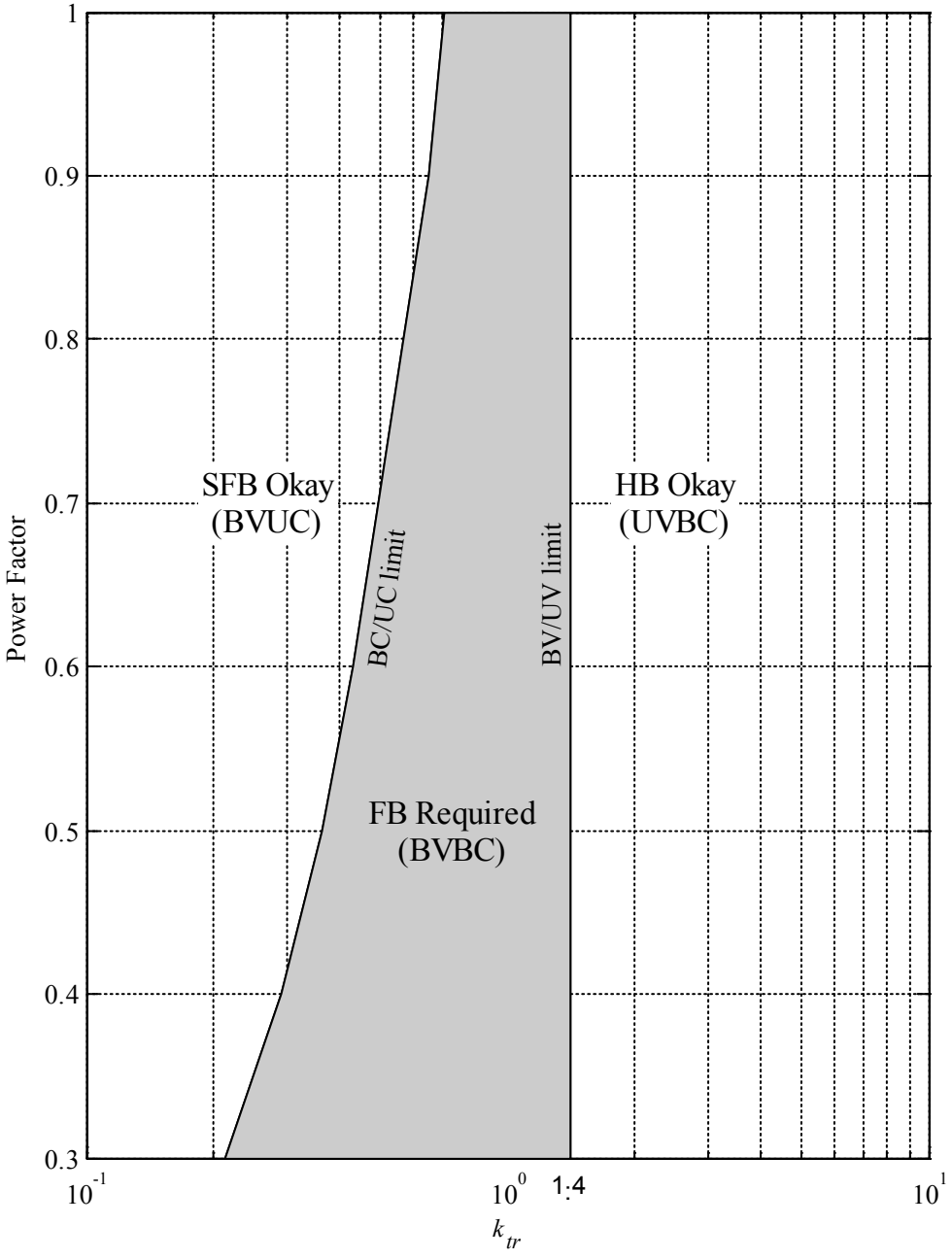


Fig. 3-17. Map of suitability of 3 main CSEB designs based on k_{tr} and power factor.

solution to the converter average model differential equations without any simplifying assumptions on capacitor ac ripple voltage or inductor ac voltage drop. Due to the more complicated nature of the improved model, the design/analysis process does not benefit significantly from the design variables k_{tr} and M; for example, the inductive voltage drop cannot be expressed in terms of either variable. In this case, normalized per unit descriptions are discarded in favor of the physical parameters.

The solution can be found starting with the CSEB dynamic model Eq. 2-13, which may be solved for d_B and combined with Eq. 2-12 to yield

$$L_B \frac{di_B(t)}{dt} = v_B(t) - C_S v_S(t) \frac{dv_S(t)}{dt} \frac{1}{i_B(t)}. \tag{3-49}$$

This may be rearranged as

$$v_S(t) \frac{dv_S(t)}{dt} = \frac{i_B(t)}{C_S} \left(v_B(t) - L_B \frac{di_B(t)}{dt} \right). \tag{3-50}$$

Combining with Eqs. 3-4 and 3-8 and rearranging produces the differential equation

$$\begin{aligned} v_S(t) \frac{dv_S}{dt} = & \left[\frac{2I_{dc} + n_{br} I_{ac} \cos(\omega_{ac} t - \phi_{ac})}{2C_S n_p n_{br}} \right] \cdot \\ & \left[V_{dc} - \sqrt{2} V_{ac} \cos(\omega_{ac} t) + \frac{\omega_{ac} L_B I_{ac}}{2n_p} \sin(\omega_{ac} t - \phi_{ac}) \right], \end{aligned} \tag{3-51}$$

which may then be explicitly integrated by separation of variables. This provides the analytical solution to the capacitor voltage v_s of the individual CSEBs,

$$v_S(t) = \sqrt{\frac{2}{C_s} \begin{bmatrix} E_{Cs,dc} + P_B t + E_{B,Vq} \sin(\omega_{ac} t) + \dots \\ E_{B,Id} \cos(\omega_{ac} t - \phi_{ac}) + E_{B,Iq} \sin(\omega_{ac} t - \phi_{ac}) + \dots \\ E_{B,ac} \sin(2\omega_{ac} t - \phi_{ac}) + E_{B,Lb} (1 - \cos(2\omega_{ac} t - 2\phi_{ac})) \end{bmatrix}}, \tag{3-52}$$

where the coefficients are defined as:

$$E_{Cs,dc} = \frac{C_S V_{S,dc,tot}^{\ 2}}{2}, \qquad P_B = \frac{2V_{dc}I_{dc}}{n_{br}n_p} - \frac{V_{ac}I_{ac}}{n_p}\cos\left(\phi_{ac}\right), \qquad \text{3-53 (a-b)}$$

$$E_{B,Vq} = \frac{-2\sqrt{2}V_{ac}I_{dc}}{n_p n_{br}\omega_{ac}}, \quad E_{B,Id} = \frac{-\sqrt{2}L_B I_{ac}I_{dc}}{n_{br}n_p^{\ 2}}, \quad E_{B,Iq} = \frac{V_{dc}I_{ac}}{\sqrt{8}n_p\omega_{ac}}, \qquad \text{3-53 (c-e)}$$

$$E_{B,ac} = \frac{-V_{ac}I_{ac}}{2n_p\omega_{ac}}, \quad \text{and} \quad E_{B,Lb} = \frac{L_B I_{ac}^{\ 2}}{2n_p^{\ 2}}. \qquad \text{3-53 (f-g)}$$

Having solved for the capacitor voltage, all other circuit quantities may be found analytically from the governing differential equations. For example, while they are omitted here for brevity, the full closed-form solutions for the capacitor current and the duty ratio – using no approximations – can readily be found using either Eq. 2-12 or 2-13 with Eq. 3-52.

Even though this analytical model is purely scalar and does not use the *dq* coordinate scheme, the *dq* terminology (direct and quadrature) is used for naming some coefficients to help distinguish them from each other with regards to their relative phases. That is, $E_{B,Vq}$ represents the bridge capacitive energy that is in quadrature with the bridge voltage ac component, $E_{B,Id}$ represents the bridge capacitive energy inline with the bridge current, and $E_{B,Iq}$ represents the bridge capacitive energy in quadrature with the bridge current.

The energy constant $E_{Cs,dc}$ is a mathematical result of the integration and represents the total average (dc) energy stored in the string of CSEB capacitors with units of Joules.

Typically the converter is designed such that this dc bias is very large compared to all other constants and coefficients in Eqs. 3-52 and 3-53, rendering

$$v_S(t) \approx \frac{V_{S,dc,tot}}{n_s}. \qquad 3\text{-}54$$

The power constant P_B represents the real power flow in the converter in Watts and must equal zero by the conservation of power limitation discussed in Chapter 2. If this criterion is not satisfied, it can be seen that the P_B term causes the average capacitor voltage to change, potentially reducing to zero or growing without bounds until physical damage occurs. Conversely, real power flow can be adjusted during start-up, shut-down or other transient events in order to control the average capacitor voltage.

The terms $E_{B,Vq}$, $E_{B,Id}$, and $E_{B,Iq}$ represent the pulsing of capacitive energy (in Joules) due to the combination of ac and dc power flows within the converter. $E_{B,ac}$ represents the pulsing of capacitive energy due exclusively to the ac power flow, and $E_{B,Lb}$ represents the pulsing of capacitive energy due the energy exchange between the bridge inductor and capacitor.

Typical BoBCs take advantage of small bridge inductance L_B, thus $E_{B,Id}$ and $E_{B,L}$ can often be neglected compared to $E_{B,Iq}$ and $E_{B,ac}$, respectively. It may be observed that by adopting the approximations and assumptions of the simplified model, the complete average model equations break down into those of the simplified model.

3.3 Frequency content of steady-state models

The BoBC plant is inherently a nonlinear system and two different models have been proposed to predict the system behavior. While convenient to understand the very basic

system design constraints, both the simplified and improved accuracy models are only basic representations of the true underlying plant. The actual time-domain waveforms could include additional frequencies that may or may not be negligible, which is worth investigation.

The branch current is determined by the voltage across the branch inductance; to produce a dc + fundamental ac current waveform, the inductor voltage must have a corresponding fundamental ac component and zero harmonics. Likewise, the capacitor voltage is determined by the current through it, and to produce a dc + fundamental ac + 2nd harmonic ac voltage requires corresponding fundamental + 2nd harmonic current components, with zero additional harmonics.

To illustrate the potential of undesirable harmonic content, first assume that the V_S waveform contains only the dominant dc, fundamental and 2nd harmonic components as predicted by the analytical models,

$$v_S(t) = V_{S,dc} + V_{S,ac,1}\cos(\omega_{ac}t - \theta_{V1}) + V_{S,ac,2}\cos(2\omega_{ac}t - \theta_{V2}). \qquad 3\text{-}55$$

Rather than use a very complex duty ratio as shown in Eq. 3-52, which is computationally intensive to produce and ineffective against disturbances and parameter variations, assume instead that a very simple duty ratio is used, where

$$d_B(t) = D_{B,dc} + D_{B,ac}\cos(\omega_{ac}t - \theta_D). \qquad 3\text{-}56$$

The inductor voltage is then defined as

$$V_L = V_{dc} - V_{ac}\cos(\omega_{ac}t - \theta_{ac}) - d_B(t)v_S(t) - R_B i_B(t). \qquad 3\text{-}57$$

The product of $d_B(t)$ and $v_S(t)$ expands this expression to

$$\begin{aligned} V_L(t) = {} & V_{X,dc} + V_{X,ac1}\cos(\omega_{ac}t - \theta_{X1}) \\ & + V_{X,ac2}\cos(2\omega_{ac}t - \theta_{X2}) + V_{X,ac3}\cos(3\omega_{ac}t - \theta_{X3}) \\ & - R_B i_B(t), \end{aligned} \qquad 3\text{-}58$$

where $V_{X,i}$ and θ_j are determined by a combination of the D_B and V_S parameters.

In steady-state the inductor voltage at dc and ω_{ac} will be balanced by the dc and ac source/load voltages. However, no such voltages exist to balance out the $2\omega_{ac}$ and $3\omega_{ac}$ harmonics; these branch current components are limited only by the branch impedance at those frequencies, e.g.

$$I_{B,ac,2} = \frac{DV_{ac,2}}{R_B + j2\omega_{ac}L_B}. \qquad 3\text{-}59$$

With very small branch impedances, even the slightest duty ratio error could result in significant, undesired branch currents, especially at undesired frequencies. Should any undesired frequencies appear in the current, these frequencies will also be reflected into the capacitor current through the same nonlinear duty ratio effect, which would then be reflected again into the inductor voltage, and so on.

To confirm the need for such a method, a converter is simulated using the parameters in Table 3-1. The converter uses open loop duty ratio control in accordance with Eq. 3-56. Waveforms of the intended branch current trajectory and the actual waveform are shown. Clearly the branch current contains a very high level of unintended harmonics, which contribute to losses and device stresses. Moreover, the actual branch current is bidirectional, whereas the desired branch current is purely positive; therefore, the harmonic-rich current waveform creates an artificial need for FB CSEBs versus SFBs, adding cost and complexity to the system.

Table 3-1. Converter simulation parameters to demonstrate harmonic content.

V_{dc}	f_{ac}	L_B	R_B	R_{ac}	R_S	C_S	V_S	$I_{B,ac,d}$
15 V	60 Hz	66 µH	0.03 Ω	15 Ω	2250 Ω	5000 µF	90 V	1.1 A

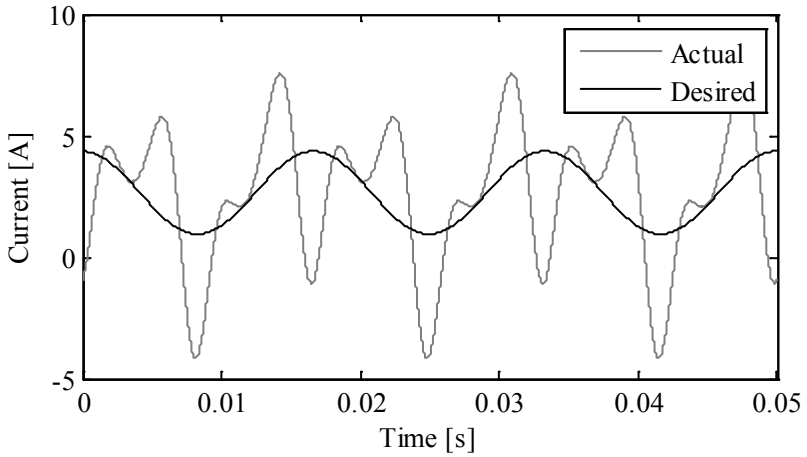


Fig. 3-18. Actual vs. desired branch current for open loop operation of converter using parameters in Table 3-1. Significant undesired harmonics are observed in the actual waveform.

3.4 Scalar Higher Order Terms Suppression (SHOTS) Control

Prior work [12] has shown that a simple proportional gain may be used in a scalar control methodology to modulate inductor currents along an intended dc + ac fundamental trajectory and suppress the higher order terms from all state variables through a wide operating regime. The integration of such a Scalar Higher Order Terms Suppression (SHOTS) controller into a single-bridge BoBC branch is shown in Fig. 3-19.

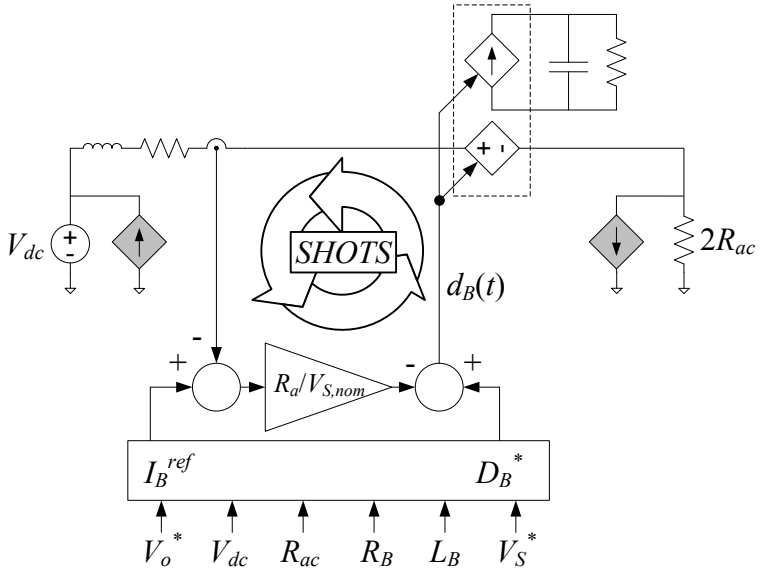


Fig. 3-19. Structure of Scalar Higher Order Terms Suppression (SHOTS) control.

The SHOTS controller accepts command inputs for the dc and ac duty ratios. These are then used to construct the scalar duty ratio command $d_B^*(t)$ for the bridges within the BoBC using Eq. 3-16. By closing the loop on the branch current, additional (but small) frequency components are injected into the scalar duty ratio, which serves to suppress any higher order branch currents, and in turn suppress higher order frequencies in all BoBC state variables. The SHOTS controller concept may be interpreted as a notch filter at dc and the ac fundamental, providing significant damping, dynamic stiffness, and ultimate rejection of all other frequencies. This is the primary reason why the controller gain is given as an "active resistance" R_a, given units of ohms through a division by nominal capacitor voltage $V_{S,nom}$.

A branch current reference term $i_B^{ref}(t)$ provides the controller with a current reference, which is calculated directly from the duty ratios and converter parameters, e.g.

V_{dc}, R_{ac}, estimated capacitor voltage $\hat{V}_S$, etc. The *ac* and *dc* current reference components are readily calculated from Eqs. 3-16 and 3-60:

$$I_{B,dc} = \frac{V_{dc}}{2R_B} - \sqrt{\frac{V_{dc}^2}{4R_B^{\,2}} - \left(\frac{R_B + 2R_{ac}}{R_B}\right) I_{B,ac,d}^{\,2} - \frac{V_S^2}{R_s R_B}} \qquad 3\text{-}60$$

To illustrate the effectiveness of SHOTS control, the above simulations are repeated but using R_a = 0.15 produces near-ideal branch current waveforms, shown in Fig. 3-20. Though not as important to the power transfer process, a dramatic reduction in the capacitor current waveform is visible in Fig. 3-21.

The use of the SHOTS controller has a visible and effective benefit to the BoBC waveform quality. By suppressing the undesired harmonics in branch current and capacitor voltage, the SHOTS controller may be integrated into the BoBC to produce a simpler system and facilitate higher levels of power converter modeling and control. Further performance improvements may be achieved using state estimators, observers, disturbance input decoupling (DID), and the like [116, 117].

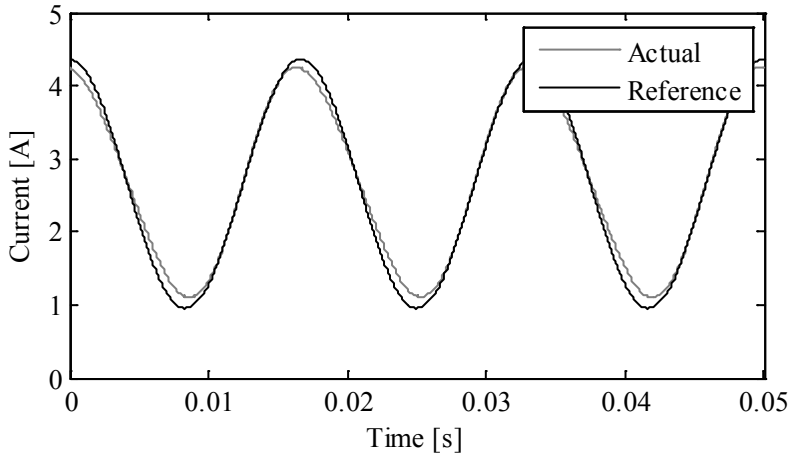


Fig. 3-20. Branch current using SHOTS controller with R_a = 0.15.

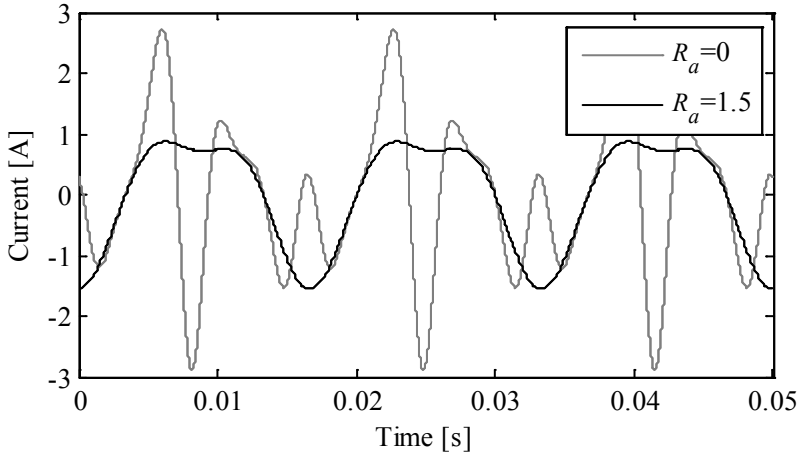


Fig. 3-21. Effect of SHOTS controller on capacitor current $i_{Cs}(t)$.

3.5 Summary

Simplified and detailed steady-state circuit models of a dc/ac BoBC with n_{br} ac phases have been presented, based on the CSEB average model proposed in [12]. Formulas for the branch currents, voltages and duty ratios have been shown, from which the proposed model equations are derived. The converter and CSEB (if applicable) design process has been described in detail, beginning with the choice of which CSEB type to utilize for a given application and a discussion of how the availability of existing Q-cells can simplify the overall converter design process.

The simplified model utilizes two design variables, k_{tr} and M, which control the dc, ac, and capacitor voltages, and allow the adoption of a per-unit system based on the dc terminal voltage and/or current. Furthermore, the model equations include the variables

n_s and n_p, which accommodate the series and parallel connection, respectively, of CSEBs within each converter branch.

Capacitor design considerations have been presented, including the effects of k_{tr} on the time-domain capacitor currents and the overall impact of the design variables and ac power factor on capacitor sizing. Design curves for rms capacitor current and peak capacitor currents have been provided for both the CSEB topologies.

Similar switch sizing design curves for varying k_{tr} and ac power factor have also been shown for the three types of CSEBs at M = 0.9. The current rating of the full bridge switches depends on the modulation scheme employed, therefore a straightforward modulation scheme based on complementary switch operation without zero states has been adopted.

An improved accuracy model, based on the explicit solution of the capacitor voltage, has also been shown. Although this model is less helpful for preliminary design of converters from scratch, it may be used when the simplified model's assumptions do not hold, such as when branch inductance is large.

An additional benefit of obtaining the CSEB analytical solution can be seen in the multiple frequency components of Eq. 3-52. That is, when designing a power converter, the capacitor voltage, current, and/or duty ratio may have non-characteristic waveform shapes depending on the magnitude of ac and dc components, inductance, frequency, etc. These non-characteristic waveforms may appear counterintuitive while examining converter operation and designing regulators for quantities carrying multiple frequency components.

Waveforms containing even small amounts of multiple frequency components, e.g. in capacitor voltage, have been shown to be capable of producing very large amounts of harmonics in the branch currents. These unwanted current components can increase converter losses, stresses, and potentially even impair the power conversion process by injecting these currents into equipment connected to the converter.

An effective harmonic mitigation method was proposed, called Scalar Higher Order Terms Suppression (SHOTS), which comprises a proportional-gain scalar current regulation loop. A current reference provides a dc+ac current trajectory, based on the duty ratio inputs, for the converter follow.

By integrating a SHOTS controller into the BoBC, a system is built which still accepts dc and fundamental ac duty ratio inputs, but which reliably outputs dc + fundamental ac currents into the load resistance. This results in a relatively simple, more-ideal system and facilitates higher levels of power converter modeling, which is the subject of the following chapter.

Chapter 4 Dynamic Phasor Modeling

The presence of ac waveforms within BoBCs motivates the use of phasor modeling to describe BoBC behavior and understand its inner dynamics. Previous BoBC dynamic models used scalar approaches [41], which are only able to capture a portion of the converter dynamics, e.g. fundamental ac frequency behavior is not represented.

The BoBC is an ideal candidate for being modeled in a very scalable way because the topology may be applied to an ac system with an arbitrary number of phases with an arbitrary number of bridges. Therefore, by adopting a phasor model with orthogonal components, a generalized CSEB-based dc-ac polyphase converter model can be developed.

This chapter presents a dynamic model of CSEB-based BoBCs using phasors in the *dq* coordinate system and the synchronous reference frame. The dc waveform components are easily integrated and complete the model. This model builds the framework for the development of multilevel branch modeling, the subject of Chapter 5.

4.1 General phasor circuit modeling

AC quantities of arbitrary amplitude and phase are often modeled as phasors, and the application of phasors to represent the dynamics of three-phase dc-ac power converters has been well-documented by the literature for many decades [5, 118]. Furthermore, their

application to single phase power converters in the context of Fourier analysis to convert each time domain dynamic variable into their corresponding dynamically varying amplitude and phase for various frequencies has been developed further [119]. In this approach, considering all phasor components in their respective synchronous reference frame, all ac quantities thus appear as dc quantities.

To establish a framework for calculating circuit quantities in the dynamic phasor model, a phasor $\underline{F}$ that represents an arbitrary ac circuit quantity is considered in the complex plane with phase angle φ and rotational velocity ω (counterclockwise), as shown in Fig. 4-1, which may be represented mathematically in the stationary reference frame by

$$\underline{F}^s = |\underline{F}|e^{j(\omega t+\varphi)} = \left(F_d + jF_q\right)e^{j\omega t}, \qquad 4\text{-}1$$

where $j = \sqrt{-1}$. Any vector or phasor in the complex plane is described in terms of its *d* and *q* (real and imaginary) components. Complex quantities are denoted with an underline and all phase angles are measured with respect to the first (A) phase of the ac source, corresponding to the *d*-axis.

Placed in the synchronous reference frame, also rotating at velocity ω, the same phasor is represented as

$$\underline{F}^e = \underline{F}^s e^{-j\omega t} = \left(F_d + jF_q\right)e^{j\omega t}e^{-j\omega t} = F_d + jF_q = |F|e^{j\varphi}. \qquad 4\text{-}2$$

The time domain or scalar representation of $\underline{F}$, denoted by $f(t)$, may be determined from the complex phasor as its real component by

$$f^s(t) = \mathrm{Re}\left\{\underline{F}^s\right\} = \sqrt{F_d{}^2 + F_q{}^2}\cos\left(\omega t + \phi\right). \qquad 4\text{-}3$$

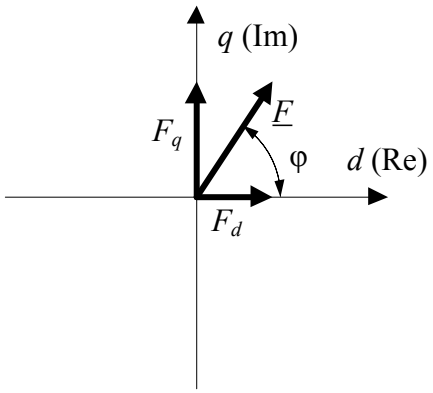


Fig. 4-1. Arbitrary phasor $\underline{F}$, rotating counterclockwise at frequency ω in stationary reference frame. Equivalently, $\underline{F}$ is viewed as stationary in the synchronous reference frame, which also rotates counterclockwise at ω.

By modeling the circuit quantities using phasors, the ac quantities may thus be expressed in their synchronous reference frame(s) as time invariant quantities, greatly simplifying the system model and its subsequent development of control techniques.

As with all phasor modeling approaches, in converting the variables to frequency domain components, a perfect representation of all frequency components of an arbitrary waveform would require an infinite number of phasors. However, such a perfect representation may not be necessary to achieve an adequate representation of the physical system, much less desirable from a modeling complexity standpoint. Rather, exclusively modeling the frequencies at which power transfer occurs permits the modeling of power transfer while maintaining relative simplicity of the overall converter model [120]. As such, a balance between performance and simplicity may be achieved.

The accuracy of the dynamic phasor model in the BoBC may also be maximized using a SHOTs controller integral to the converter, which limits the frequency content of the state variables and therefore the number of dynamic phasors to model. A

transformation to phasor representation of the circuit from its scalar representation, and thus the averaged circuit modeling of Chapter 3, is sought using dc components and ac components represented in the *dq* coordinate system in the complex plane, where the *d* (direct) component is represented by the positive real axis and the *q* (quadrature) component by the positive imaginary axis.

The scalar converter circuit diagram illustrated in Fig. 3-2 is again considered in the model development. Isolating an individual converter bridge of an arbitrary branch yields the circuit diagram of Fig. 4-2, where current sources i_1 and i_2 represent the current components from other arm/string currents that serve to negate the ac and dc components in the bridge current i_B from being drawn from the dc and ac voltage sources respectively. While the presence of i_1 and i_2 are included in the figure to enforce the notion that a pure dc current must flow through V_{dc} and a purely ac current through R_{ac}, they do not play a substantial role in the dynamics of the power converter when all branches are appropriately balanced. As shown in the figure, for modeling purposes the ac load resistance R_{ac} for a single ac phase leg is split into two resistors for each branch, where each resistor is $2R_{ac}$ because each branch supplies half of the ac load current.

4.2 Phasor circuit model development

In dc-ac BoBCs, as shown in Chapter 3, power transfer occurs at ω_{ac} and dc. While the bridge inductor currents carry substantial ac and dc components, the energy storage

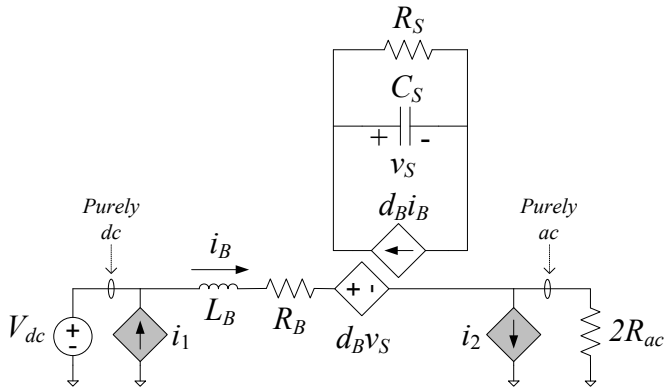


Fig. 4-2. Scalar CSEB circuit model of an arbitrary bridge between V_{dc} and the load resistance R_{ac}. When branches are appropriately balanced, the load impedance is effectively doubled to $2R_{ac}$, since each branch sources half of the load current as indicated in Fig. 3-2.

capacitors hold substantial dc voltage components. Therefore, appropriate selection of d and q components for phasors at ω_{ac} are required for the bridge inductor current in the model, in addition to dc components, while dc components may be sufficient to represent voltage dynamics of the energy storage capacitor. The only other frequency that appears in the steady state modeling identified in Chapter 3 is $2\omega_{ac}$, which occurs in the capacitor and switch currents. As discussed in Chapter 3, if the second harmonic or other frequency components are indeed very small in comparison to the dc and fundamental components, then they may be safely neglected.

The bridge (or inductor) current, from Eqs. 3-4 and 3-5, contains dc and ac components, which must be instantaneously equal to the real components of its complex phasor representation in the stationary reference frame. Using the example of bridge (1,1), which may also be easily applied to all other bridges, the bridge current

$$i_{B(1,1)}(t) = I_{B,dc} + \sqrt{2} I_{B,ac} \cos\left(\omega_{ac} t - \varphi_{ac}\right) \qquad 4\text{-}4$$

may also be expressed as

$$i_{B(1,1)}(t) = \mathrm{Re}\left\{ I_{B,dc} + \sqrt{2}\,\underline{I^{s}_{B,ac}}(t) \right\}, \qquad 4\text{-}5$$

where

$$\underline{I^{s}_{B,ac}}(t) = \left(I_{B,ac,d} + jI_{B,ac,q} \right) e^{j\omega_{ac}t}. \qquad 4\text{-}6$$

A typical phasor diagram of the bridge current and ac voltage is shown in Fig. 4-3. Note that the ac component variables, whether voltages, currents or duty ratios, all refer to rms values.

Such a representation may be extended to all other ac quantities within an arbitrary bridge, thus defining the following quantities:

$$\underline{D^{s}_{B,ac}}(t) = \left(D_{B,ac,d} + jD_{B,ac,q} \right) e^{j\omega_{ac}t} \qquad 4\text{-}7$$

$$\underline{V^{s}_{Bi,ac}}(t) = \underline{D^{s}_{B,ac}}(t) V_S. \qquad 4\text{-}8$$

All phase angles are measured with respect to the ac load resistor voltage (and current for unity power factor). Note that the converter is fully capable of connecting to non-unity power factor loads, however in this work, only unity power factor is assumed, so as to simplify the theoretical developments. Therefore, the ac load comprises only resistors R_{ac}. Finally, the model includes the assumption that the energy storage capacitor voltage may be approximated largely by its dc component (which follows from a reasonably sized capacitor C_S)

$$V_S = V_{S,dc}. \qquad 4\text{-}9$$

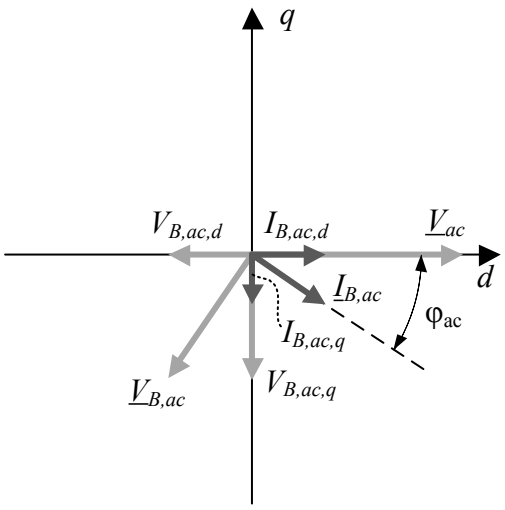


Fig. 4-3. Phasor diagram of typical bridge voltage and current of circuit shown in Fig. 4-4. Currents are shown in dark gray and voltages are shown in light gray.

The scalar circuit model quantities are subsequently found as the real part of the sum of the dc and the phasor components in the stationary reference frame:

$$d_B(t) = \mathrm{Re}\left\{D_{B,dc} + \sqrt{2}\left(D_{B,ac,d} + jD_{B,ac,q}\right)e^{j\omega_{ac}t}\right\} \tag{4-10}$$

$$v_{Bi}(t) = \mathrm{Re}\left\{V_{Bi,dc} + \sqrt{2}\underline{V^s_{Bi,ac}}(t)\right\} = d_B(t)V_S\,. \tag{4-11}$$

The resulting inductor voltage is found to be

$$\begin{aligned} L_B\frac{d}{dt}\left(I_{B,dc} + \sqrt{2}\underline{I^s_{B,ac}}(t)\right) = V_{dc} - R_B\left(I_{B,dc} + \sqrt{2}\underline{I^s_{B,ac}}(t)\right) - V_{Bi,dc} \\ -\sqrt{2}\underline{V_{Bi,ac}}(t) - 2\sqrt{2}R_{ac}\underline{I^s_{B,ac}}(t). \end{aligned} \tag{4-12}$$

With the bridge current also known, the components can be grouped by type (dc, ac direct or real, ac quadrature or imaginary) to expose their relationships:

$$L_B\frac{dI_{B,dc}}{dt} = V_{dc} - R_B I_{B,dc} - D_{B,dc}V_S \tag{4-13}$$

$$L_B \frac{dI_{B,ac,d}}{dt} = \omega_{ac} L_B I_{B,ac,q} - \left(R_B + 2R_{ac}\right) I_{B,ac,d} - D_{B,ac,d} V_S \qquad 4\text{-}14$$

$$L_B \frac{dI_{B,ac,q}}{dt} = -\omega_{ac} L_B I_{B,ac,d} - \left(R_B + 2R_{ac}\right) I_{B,ac,q} - D_{B,ac,q} V_S \,. \qquad 4\text{-}15$$

When implementing SHOTS control as discussed in Section 3.4, each duty ratio is assigned a commanded value indicated by an asterisk, e.g. $D^*_{B,ac,d}$, plus a proportional error term which is a function of the actual bridge current and the reference value,

$$D_{B,ac,d} = D^*_{B,ac,d} - R_a \left(I^{ref}_{B,ac,d} - I_{B,ac,d}\right) \qquad 4\text{-}16$$

$$D_{B,ac,q} = D^*_{B,ac,q} - R_a \left(I^{ref}_{B,ac,q} - I_{B,ac,q}\right) \qquad 4\text{-}17$$

$$D_{B,\mathrm{dc}} = D^*_{B,\mathrm{dc}} - R_a \left(I^{ref}_{B,\mathrm{dc}} - I_{B,\mathrm{dc}}\right). \qquad 4\text{-}18$$

The capacitor current is the product of two phasor quantities, expressed as

$$C_S \frac{dV_S}{dt} = \left(I_{B,dc} + \underline{I^s_{B,ac}}(t)\right)\left(\overline{D_{B,dc} + \underline{D^s_{B,ac}}(t)}\right), \qquad 4\text{-}19$$

which, by Eq. 4-9, must consist entirely of real, dc components. Therefore, the expression is rewritten as

$$C_S \frac{dV_S}{dt} = D_{B,dc} I_{B,dc} + D_{B,ac,q} I_{B,ac,q} + D_{B,ac,d} I_{B,ac,d} \qquad 4\text{-}20$$

which, in the steady state, is equal to zero. The equation is rewritten further by including any nominal losses occurring within the circuit, represented as a resistive load R_S across the capacitor,

$$C_S \frac{dV_S}{dt} = D_{B,dc} I_{B,dc} + D_{B,ac,\mathrm{q}} I_{B,ac,\mathrm{q}} + D_{B,ac,d} I_{B,ac,d} - \frac{V_S}{R_S} \qquad 4\text{-}21$$

The phasor circuit model shown in Fig. 4-4 directly results from the above equations. While the capacitor current model does include q-axis components, which are zero by definition, they are included for the sake of completeness because the inductor voltage model still requires a q-axis component to compensate for the inductor voltage drop.

It should be noted that, while many dynamic phasor models use complex state variables to simplify the mathematical representation [118], such representations are merely 2-dimensional; the presence of a dc component in the phasor circuit model of this chapter requires an additional dimension (akin to a zero-sequence component) that is not trivial to include. Therefore the dynamic phasor model proposed in this chapter separates the d, q, and dc components into separate equations with purely real-valued state variables.

4.2.1 Steady state dynamic phasor model solution

The average (dc) voltage across an inductor must equal zero, which specifies that

$$V_{dc} = D_{B,dc} V_S + R_B I_{B,dc} . \qquad 4\text{-}22$$

Furthermore, since a resistive load is assumed, the ac load current $\underline{I_{B,ac}}$ lies entirely in the d-axis, hence active power flow is produced by $I_{B,ac,d}$ which is produced by $V_{iB,ac,q}$ and the inductive reactance, in addition to $V_{iB,ac,d}$ and the load resistance. Therefore, in the steady state,

$$I_{B,ac,d} = \frac{-V_{Bi,ac,q}}{\omega_{ac} L_B} = \frac{-D_{B,ac,q} V_S}{\omega_{ac} L_B} = -\frac{-V_{Bi,ac,\mathrm{d}}}{R_B + 2R_{ac}} = \frac{-D_{B,ac,\mathrm{d}} V_S}{R_B + 2R_{ac}} , \qquad 4\text{-}23$$

$$D_{B,ac,q} = \frac{\omega_{ac} L_B}{R_B + 2R_{ac}} D_{B,ac,d} . \qquad 4\text{-}24$$

Assuming adequate current regulation, the steady state solution for the dynamic model is

$$R_B I_{B,dc}{}^2 - I_{B,dc} V_{dc} + \left(R_B + 2R_{ac}\right) I_{B,ac,d}{}^2 + \frac{V_S{}^2}{R_S} = 0\,, \qquad 4\text{-}25$$

which is straightforward to solve for the dc current,

$$I_{B,dc} = \frac{V_{dc}}{2R_B} - \sqrt{\frac{V_{dc}^2}{4R_B{}^2} - \left(\frac{R_B + 2R_{ac}}{R_B}\right) I_{B,ac,d}{}^2 - \frac{V_S^2}{R_s R_B}}\,. \qquad 4\text{-}26$$

4.2.2 Change of design variables to dynamic phasor variables

During the BoBC design phase of Section 3.2, the dimensionless variables k_{tr} and M were used. These variables may be converted into the rms duty ratios using the following relationships from Eqs 3-16 and 3-19. Note that these relationships are only approximate, and their accuracy is determined by many factors, such as L_B, R_B, etc.

$$D_{B,dc} \approx \frac{M \cdot k_{tr}}{k_{tr} + \sqrt{2}} \qquad 4\text{-}27$$

$$D_{B,ac} \approx \frac{M}{k_{tr} + \sqrt{2}} \qquad 4\text{-}28$$

4.3 Circuit and state block diagrams

The circuit diagram for the dynamic phasor model of one open loop branch, containing only one bridge, is shown in Fig. 4-4. The same plant is shown with an actual scalar SHOTS controller in Fig. 4-5. Note that these models differ from the SHOTS-

enabled scalar model of Fig. 3-19 only in the use of d, q, and dc duty ratio and reference current variables, versus the scalar ac + dc variables. While Fig. 4-5 represents the actual

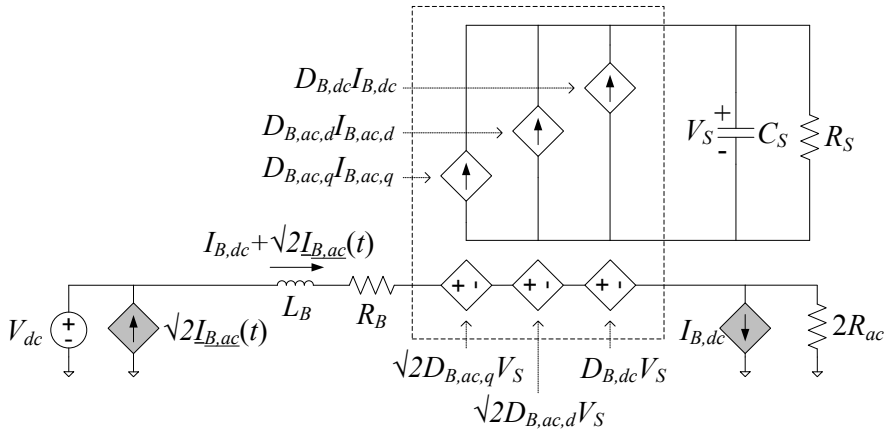


Fig. 4-4. Dynamic phasor model of individual CSEB circuit, illustrating dc, ac direct and ac quadrature quantities explicitly.

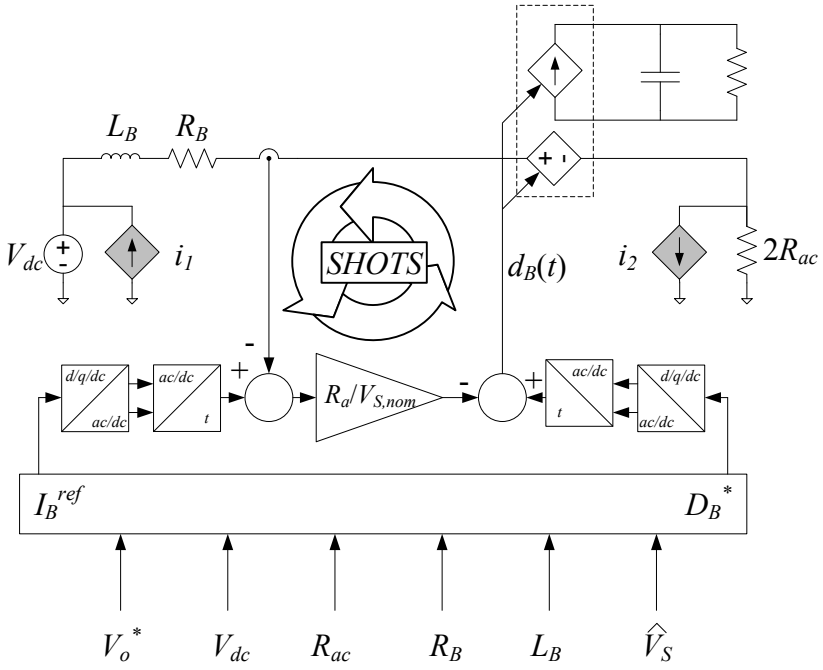


Fig. 4-5. Actual closed loop current control implementation within individual CSEB.

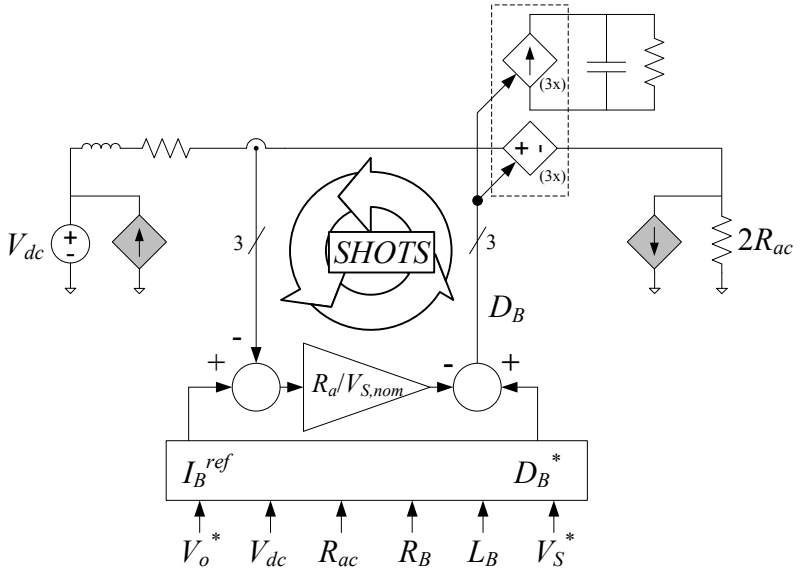


Fig. 4-6. Effective closed loop current control implementation within individual CSEB.

(scalar) system, when the SHOTS controller is properly functioning, the undesired frequency components are effectively eliminated; therefore, the transformations between d/q/dc components and the time domain may be neglected, yielding the representation of Fig. 4-6. The figure portrays 3 separate but overlapping/cross-coupled control loops, which are fully described by the nonlinear state block diagram in Fig. 4-7. These principles will be expanded upon in Chapter 5.

4.4 Small signal dynamic phasor model

A small signal bulk branch model may be established, which lumps together all bridges of one branch, and evaluated at a steady-state operating point. In this model, small-signal variables are denoted with δ, state variables comprise the 3 branch current

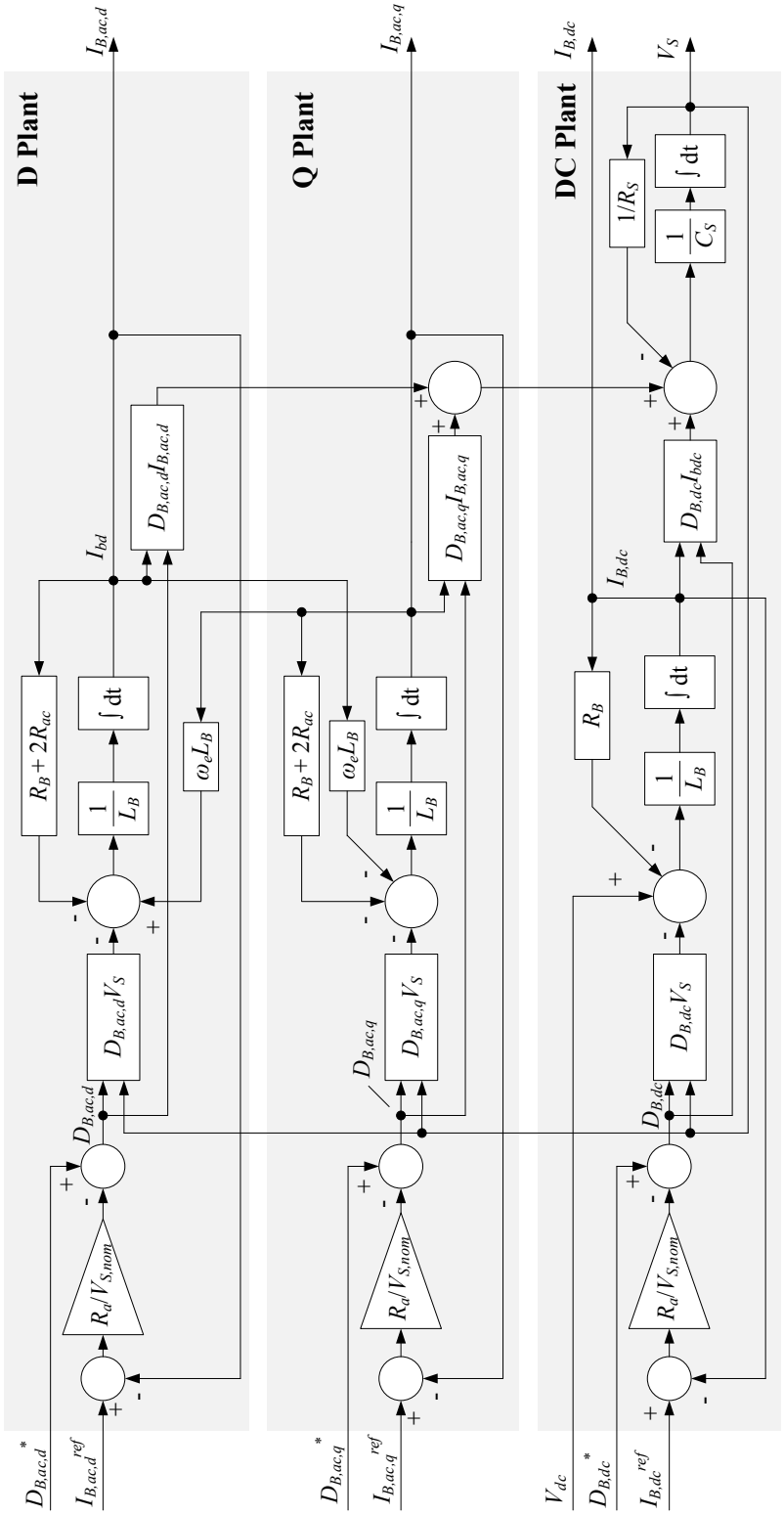


Fig. 4-7. Full nonlinear state block diagram for SHOTS-enabled single bridge branch.

axes plus 1 capacitor voltage, and inputs include commanded duty ratios, branch current reference terms, and dc input voltage.

Starting with the plant dynamic model of Eqs. 4-13 through 4-15 plus 4-21, and applying duty ratio definitions 4-16 through 4-18 yields

$$\begin{aligned}\frac{d}{dt}\delta I_{B,ac,d} = \delta I_{B,ac,d}\left[\frac{-R_a V_S/V_{S,nom} - R_B - 2R_{ac}}{L_B}\right] + \omega_{ac}\delta I_{B,ac,q} \\ +\delta V_S\left[\frac{-D^*_{B,ac,d} + R_a\left(I^{ref}_{B,ac,d} - I_{B,ac,d}\right)/V_{S,nom}}{L_B}\right] \\ +\delta D^*_{B,ac,d}\left[\frac{-V_S}{L_B}\right] + \delta I^{ref}_{B,ac,d}\left[\frac{R_a V_S}{L_B V_{S,nom}}\right]\end{aligned} \qquad 4\text{-}29$$

$$\begin{aligned}\frac{d}{dt}\delta I_{B,ac,q} = -\omega_{ac}\delta I_{B,ac,d} + \delta I_{B,ac,q}\left[\frac{-R_a V_S/V_{S,nom} - R_B - 2R_{ac}}{L_B}\right] + \\ \delta V_S\left[\frac{D^*_{B,ac,\mathrm{q}} + R_a\left(I^{ref}_{B,ac,q} - I_{B,ac,q}\right)/V_{S,nom}}{L_B}\right] \\ +\delta D^*_{B,ac,q}\left[\frac{-V_S}{L_B}\right] + \delta I^{ref}_{B,ac,q}\left[\frac{R_a V_S}{L_B V_{S,nom}}\right]\end{aligned} \qquad 4\text{-}30$$

$$\begin{aligned}\frac{d}{dt}\delta I_{B,\mathrm{dc}} = \delta I_{B,dc}\left[\frac{-R_a V_S/V_{S,nom} - R_B}{L_B}\right] \\ +\delta V_S\left[\frac{-D^*_{B,dc} + R_a\left(I^{ref}_{B,dc} - I_{B,dc}\right)/V_{S,nom}}{L_B}\right] \\ +\frac{V_{dc}}{L_B} + \delta D^*_{B,dc}\left[\frac{-V_S}{L_B}\right] + \delta I^{ref}_{B,dc}\left[\frac{R_a V_S}{L_B V_{S,nom}}\right]\end{aligned} \qquad 4\text{-}31$$

$$\begin{aligned}\frac{d}{dt}\delta V_S = {} & \delta I_{B,ac,d}\left[\frac{D^*_{B,ac,d}}{C_S} - \frac{R_a}{C_S V_{S,nom}}\left(I^{ref}_{B,ac,d} - 2I_{B,ac,d}\right)\right] \\ & + \delta I_{B,ac,\mathrm{q}}\left[\frac{D^*_{B,ac,q}}{C_S} - \frac{R_a}{C_S V_{S,nom}}\left(I^{ref}_{B,ac,q} - 2I_{B,ac,q}\right)\right] \\ & + \delta I_{B,dc}\left[\frac{D^*_{B,dc}}{C_S} - \frac{R_a}{V_{S,nom}}\left(I^{ref}_{B,dc} - 2I_{B,dc}\right)\right] + \delta V_S\left[\frac{-1}{R_S C_S}\right] \\ & + \delta D^*_{B,ac,d}\left[\frac{I_{B,ac,d}}{C_S}\right] + \delta D^*_{B,ac,q}\left[\frac{I_{B,ac,q}}{C_S}\right] + \delta D^*_{B,dc}\left[\frac{I_{B,dc}}{C_S}\right] \\ & + \delta I^{ref}_{B,dc}\left[\frac{-R_a I_{B,dc}}{C_S V_{S,nom}}\right] + \delta I^{ref}_{B,ac,d}\left[\frac{-R_a I_{B,ac,d}}{C_S V_{S,nom}}\right] + \delta I^{ref}_{B,ac,q}\left[\frac{-R_a I_{B,ac,q}}{C_S V_{S,nom}}\right].\end{aligned} \tag{4-32}$$

This model may be represented much more compactly using matrices. Beginning with the small signal state vector x and input vector u,

$$x = \begin{bmatrix} \delta I_{B,ac,d} \\ \delta I_{B,ac,q} \\ \delta I_{B,\mathrm{dc}} \\ \delta V_S \end{bmatrix} \qquad u = \begin{bmatrix} V_{dc} \\ \delta D^*_{B,ac,d} \\ \delta D^*_{B,ac,q} \\ \delta D^*_{B,dc} \\ \delta I^{ref}_{B,ac,d} \\ \delta I^{ref}_{B,ac,q} \\ \delta I^{ref}_{B,dc} \end{bmatrix} \tag{4-33}$$

the system dynamics may be expressed as

$$\dot{x} = Ax + Bu\,, \tag{4-34}$$

where

$$A=\begin{bmatrix} \frac{-R_aV_S}{L_BV_{S,nom}}-\frac{R_B}{L_B}-\frac{2R_{ac}}{L_B} & \omega_{ac} & \cdots \\ -\omega_{ac} & \frac{-R_aV_S}{L_BV_{S,nom}}-\frac{R_B}{L_B}-\frac{2R_{ac}}{L_B} & \\ 0 & 0 & \\ \frac{D^*_{B,ac,d}}{C_S}-\frac{R_a\left(I^{ref}_{B,ac,d}-2I_{B,ac,d}\right)}{C_SV_{S,nom}} & \frac{D^*_{B,ac,q}}{C_S}-\frac{R_a\left(I^{ref}_{B,ac,q}-2I_{B,ac,q}\right)}{C_SV_{S,nom}} & \end{bmatrix}$$

$$\begin{bmatrix} 0 & \frac{-D^*_{B,ac,d}}{L_B}+\frac{R_a\left(I^{ref}_{B,ac,d}-I_{B,ac,d}\right)}{L_BV_{S,nom}} \\ \cdots & 0 & \frac{-D^*_{B,ac,q}}{L_B}+\frac{R_a\left(I^{ref}_{B,ac,q}-I_{B,ac,q}\right)}{L_BV_{S,nom}} \\ & \frac{-R_aV_S}{L_BV_{S,nom}}-\frac{R_B}{L_B} & \frac{-D^*_{B,dc}}{L_B}+\frac{R_a\left(I^{ref}_{B,dc}-I_{B,dc}\right)}{L_BV_{S,nom}} \\ & \frac{D^*_{B,dc}}{C_S}-\frac{R_a\left(I^{ref}_{B,dc}-2I_{B,dc}\right)}{C_SV_{S,nom}} & \frac{-1}{R_SC_S} \end{bmatrix} \quad 4\text{-}35$$

$$B=\begin{bmatrix} 0 & \frac{-V_S}{L_B} & 0 & 0 & \frac{R_aV_S}{L_BV_{S,nom}} & 0 & 0 \\ 0 & 0 & \frac{-V_S}{L_B} & 0 & 0 & \frac{R_aV_S}{L_BV_{S,nom}} & 0 \\ \frac{1}{L_B} & 0 & 0 & \frac{-V_S}{L_B} & 0 & 0 & \frac{R_aV_S}{L_BV_{S,nom}} \\ 0 & \frac{I_{B,ac,d}}{C_S} & \frac{I_{B,ac,q}}{C_S} & \frac{I_{B,dc}}{C_S} & \frac{-R_aI_{B,ac,d}}{C_SV_{S,nom}} & \frac{-R_aI_{B,ac,q}}{C_SV_{S,nom}} & \frac{-R_aI_{B,dc}}{C_SV_{S,nom}} \end{bmatrix}. \quad 4\text{-}36$$

4.5 Simplified state block diagram

A simplified visualization of the dynamic model is provided in Fig. 4-8. This diagram omits some features, such as ω_{ac} cross-coupling within $I_{B,ac,d}$ and $I_{B,ac,q}$ states. However,

the simplifications are convenient because block diagrams with higher levels of n_s quickly become quite complex, as will be shown in Chapter 5. The capacitor voltage V_{S1} is shown with dashed lines only to make the overlaying arrows more visible.

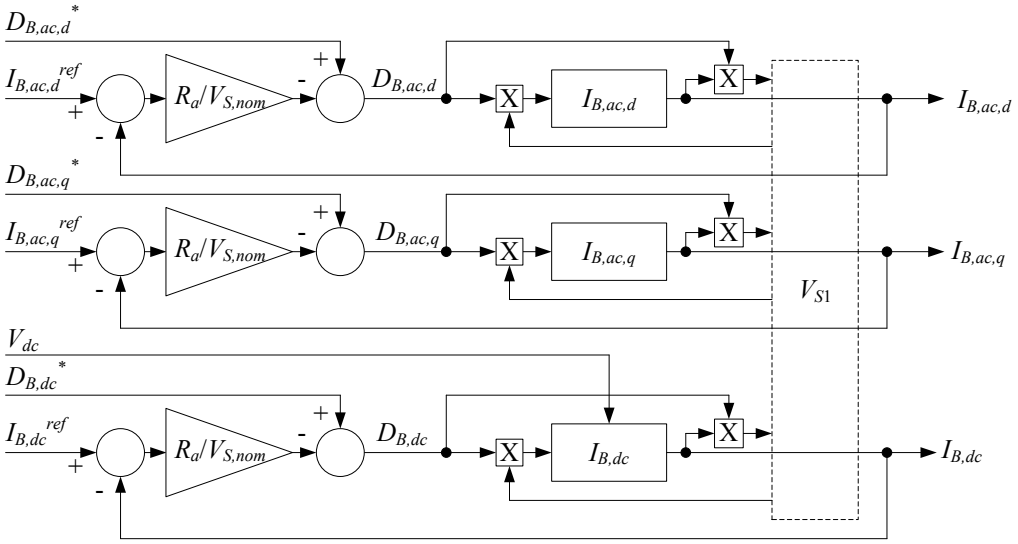


Fig. 4-8. Simplified closed loop dynamic phasor model of individual CSEB.

4.6 Dynamic Analysis of Bulk D/Q/DC model

The eigenvalues of the model may be calculated for specific steady-state operating points. This investigation considers a converter with the parameters and operating point given in Table 4-1, with SHOTs gain $0 \le R_a \le 0.15$. Branch currents are assumed to follow their intended trajectories regardless of R_a. The eigenvalues at the extrema are shown in Table 4-2, and an eigenvalue migration plot over the same range of R_a is shown in Fig. 4-9, including a close-up near the imaginary axis in Fig. 4-10.

Table 4-1. Converter parameters for dynamic analysis.

V_{dc}	f_{ac}	L_B	R_B	R_{ac}	R_S	C_S	V_S	$I_{B,ac,d}$
5 V	60 Hz	22 μH	0.01 Ω	2.7 Ω	750 Ω	5000 μF	30 V	0.71 A

Table 4-2. Eigenvalues at one operating point, with and without SHOTS controller.

$R_a = 0$	$R_a = 0.15$
$-4.0\text{x}10^4 + \text{j}60$ Hz	$-4.1\text{x}10^4 + \text{j}60$ Hz
$-4.0\text{x}10^4 - \text{j}60$ Hz	$-4.1\text{x}10^4 - \text{j}60$ Hz
-36 + j71 Hz	-5.8 Hz
-36 - j71 Hz	$-1.2\text{x}10^3$ Hz

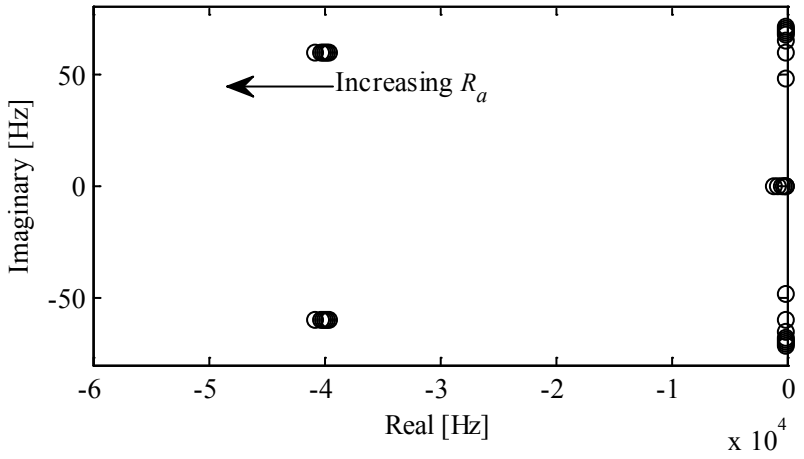
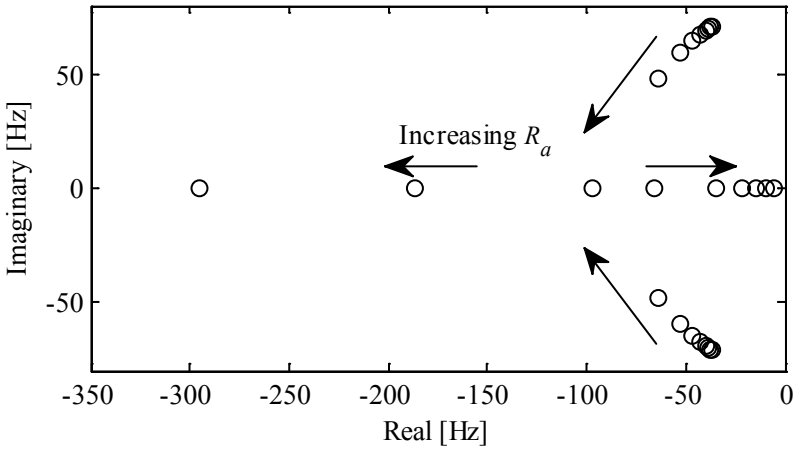


Fig. 4-9. Eigenvalue migration over the range $0 \le R_a \le 0.15$ for all 4 eigenvalues.

4.6.1 Eigenvalue locations

One pair of well-damped complex eigenvalues is located with the imaginary part at the fundamental frequency, as shown in Fig. 4-10, with a real component that varies slightly with R_a. This frequency component is expected from the cross-coupling of the ac



(b)

Fig. 4-10. Eigenvalue migration over the range $0 \le R_a \le 0.15$ showing close-up near imaginary axis.

components in the dynamic phasor model. The imaginary components are equal and opposite because the state variables are all real-valued.

The other pair of eigenvalues can be either entirely real or complex depending on R_a. While the exact location also varies with other damping terms such as R_S, R_B and R_{ac}, the natural frequency may be determined quite easily. First, the determinant of A is solved from Eq. 4-35 assuming zero damping:

$$\Delta(s) = \frac{C_S L_B}{\left(D_{B,\mathrm{dc}}\omega_{ac}\right)^2} s^4 + \frac{{D_{B,dc}}^2 + {D_{B,ac,d}}^2 + {D_{B,ac,q}}^2 + C_S L_B {\omega_{ac}}^2}{\left(D_{B,dc}\omega_{ac}\right)^2} s^2 + 1 \qquad 4\text{-}37$$

A simple, undamped pair of oscillators may be modeled as

$$\left(\frac{s^2}{{\omega_{ac}}^2} + 1\right)\left(\frac{s^2}{{\omega_{LC}}^2} + 1\right) = \frac{s^4}{{\omega_{ac}}^2 {\omega_{LC}}^2} + \left(\frac{1}{{\omega_{ac}}^2} + \frac{1}{{\omega_{LC}}^2}\right) s^2 + 1. \qquad 4\text{-}38$$

Treating ω_{ac} as a known constant and setting Eqs. 4-37 and 4-38 to be approximately equal yields

$$\omega_{LC}{}^2 \approx \frac{D_{B,dc}{}^2}{L_B C_S}. \qquad 4\text{-}39$$

For the specific case of the parameters in this section, ω_{LC} is approximated as 79.9 Hz, which is extremely well-correlated with the exact undamped solution of $\omega_{LC} = \sqrt{36^2 + 71^2} = 79.6$ Hz. Products of matched eigenvalue pairs are known to remain approximately constant regardless of their damping terms, therefore Eq. 4-39 also provides the migration trajectory of these eigenvalues.

Two sets of eigenvalues therefore exist: one representing the converter operation around 60 Hz, and the other representing the resonance between the branch inductance and the bridge capacitance as a function of dc duty ratio. The actual open loop eigenvalues do contain a small amount of damping due to R_{ac}, R_B and R_S. Additional damping is provided with R_a. This is seen in Fig. 4-10 and Fig. 4-10, where an increase of R_a causes the 60 Hz poles to migrate further into the left half plane, while the LC tank eigenvalues tend to lose their resonant behavior and increase damping, ultimately providing an overdamped response. The system is always stable within the given range of R_a. Based on these observations, R_a may be chosen to provide a well-damped system.

4.7 Effect of SHOTS on transfer functions

The increased damping from implementing SHOTS may be visualized using the transfer function $V_S/d_{B,ac,d}$, which is shown in Fig. 4-11 for $R_a = 0$ and $R_a = 0.15$. The

open loop curve has the expected resonant behavior around 80 Hz, which is eliminated in the closed loop curve, which instead exhibits a clean, first-order roll-off at 5.8 Hz. The eigenvalue migration plot indicates that the resonant pole pair from the open loop transfer function will turn into two purely real poles in the closed loop transfer function. However, the first-order roll-off indicates otherwise.

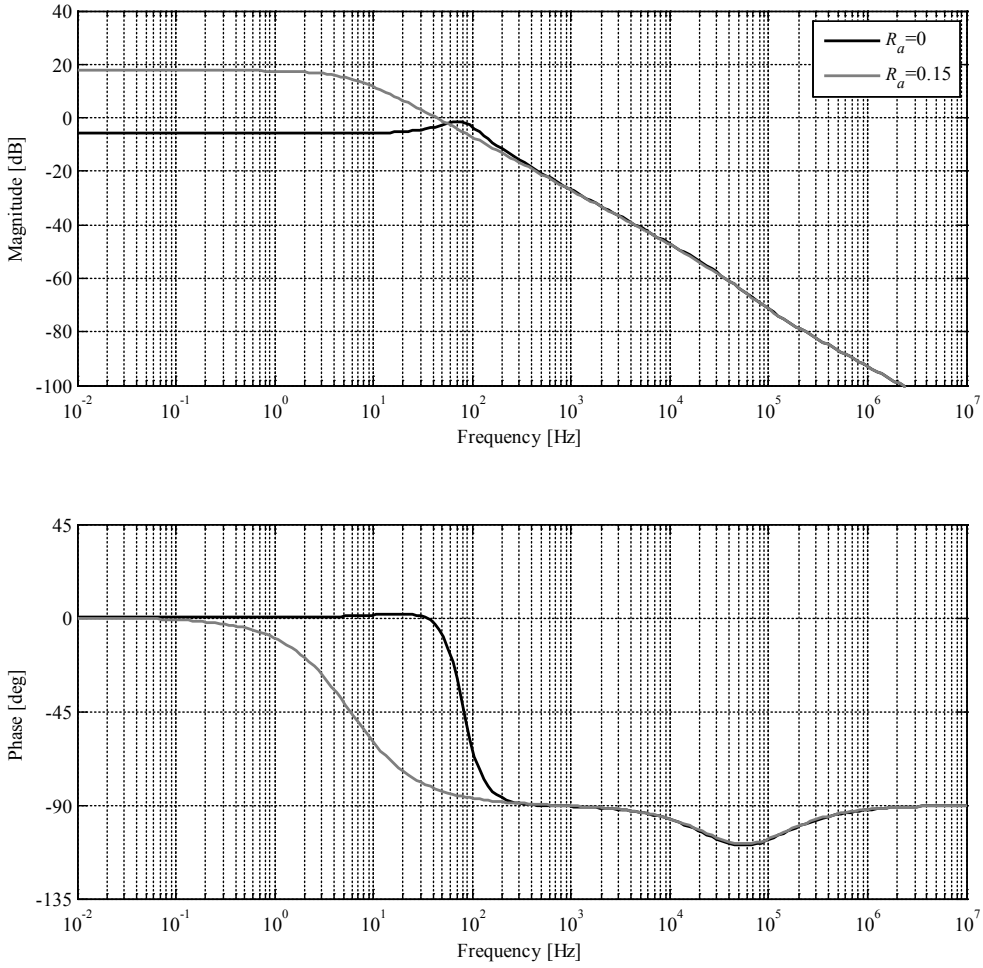


Fig. 4-11. Transfer function of $V_S/d_{B,ac,d}$ comparing open loop dynamics with closed loop SHOTS controller dynamics.

The answer lies in the system zeros. Though subtle, a very slight phase lead is shown in the open loop transfer function around 20 Hz, indicating a LHP zero. In closed loop operation, this zero cancels out the higher-frequency real pole of the resonant pair, leaving only the low frequency pole.

The SHOTS controller has little effect on the transfer functions at higher frequencies.

4.8 Summary

A dynamic phasor model of the BoBC has been developed, which includes ac (direct, quadrature) and dc components of voltage and current. For maximum utility, this model has also been expressed in matrix and Cartesian forms. The need for a harmonic component mitigation method was demonstrated, and a suitable scalar control methodology called Scalar Higher Order Terms Suppression (SHOTS) was presented and demonstrated as effective. Detailed design equations representing the full nonlinear and small signal dynamics were presented. An analysis of the eigenvalues, including their approximate locations, their migration with respect to SHOTS gain R_a, and their effect on transfer function behavior, was presented and discussed. Based on these results, R_a may be chosen to provide a well-damped system.

This dynamic phasor model represents a significant improvement on previous modeling efforts, which are scalar in nature [41]. As a consequence, this is the first known BoBC bridge model to incorporate details of the fundamental frequency ac dynamics, making it a prime candidate for use in motor drives, microgrids, or other high-performance applications.

Chapter 5 Multilevel Branch Modeling

This chapter extends the bridge modeling of Chapter 4 to model an entire branch as a series connection of bridges. For the sake of simplicity, this chapter assumes that each branch comprises a single series-connected string of bridges (n_p = 1). The modeling proposed within this chapter may straightforwardly be extended to higher values of n_p.

5.1 Extending the scalar circuit model

The modularity of the proposed bridge construction, e.g. bridges that are essentially identical and are each built with an inductor, provides straightforward extensions to higher values of n_s. Each bridge as presented in Chapter 4 is considered a "per unit bridge" for a given input voltage V_{dc} and output voltage V_{ac}, which is closely related to k_{tr}. Therefore, during the system design process, the number of bridges is largely determined by the actual terminal voltages $V_{dc,tot}$ and $V_{ac,tot}$ divided by V_{dc} and V_{ac} of the "per unit bridge,"

$$n_s = \max\left(\left\lceil \frac{V_{dc,tot}}{D_{B,dc}V_S} \right\rceil, \left\lceil \frac{V_{ac,tot}}{D_{B,ac}V_S} \right\rceil\right). \qquad 5\text{-}1$$

Therefore, with a value of n_s established, there are n_s capacitor voltage states and 3 inductor current states. However, the total branch inductance comprises n_s inductors of

equal value in accordance with the unit bridge L_B. Likewise, for a given V_{dc} and R_{ac} at the unit bridge level, adding a second bridge would require doubling V_{dc} and R_{ac}, etc.

With these scaling attributes in mind, branches with n_s=2 and n_s=3 are graphically modeled in Fig. 5-1 through Fig. 5-6, as both dynamic phasor models and simplified state block diagrams. This chapter is dedicated to the analysis of these two values of n_s, with indications and trends of scaling to higher values. A summary of circuit parameters for all n_s=1 through n_s=3 converters is shown in Table 5-1. The table indicates parameters for the same operating point per bridge, regardless of n_s.

Table 5-1. Circuit parameter summary for n_s=1 through 3 for one operating point.

	Units	$n_s = 1$	$n_s = 2$	$n_s = 3$
$V_{dc,tot}$	V	5	10	15
I_{dc}	A	0.79	0.79	0.79
$V_{ac,tot}$	V	1.9	3.9	5.8
$R_{ac,tot}$	Ω	2.7	5.5	8.2
$I_{ac,d}$	A	0.71	0.71	0.71
$V_{S,tot}$	V	30	60	90
$L_{B,tot}$	μH	22	44	66
$R_{B,tot}$	Ω	0.01	0.02	0.03
C_S[1]	μF	5000	5000	5000
R_S[1]	Ω	750	750	750
$P_{ac,tot}$	W	5.4	11	16.4

[1] Values for C_S and R_S are given as per-bridge.

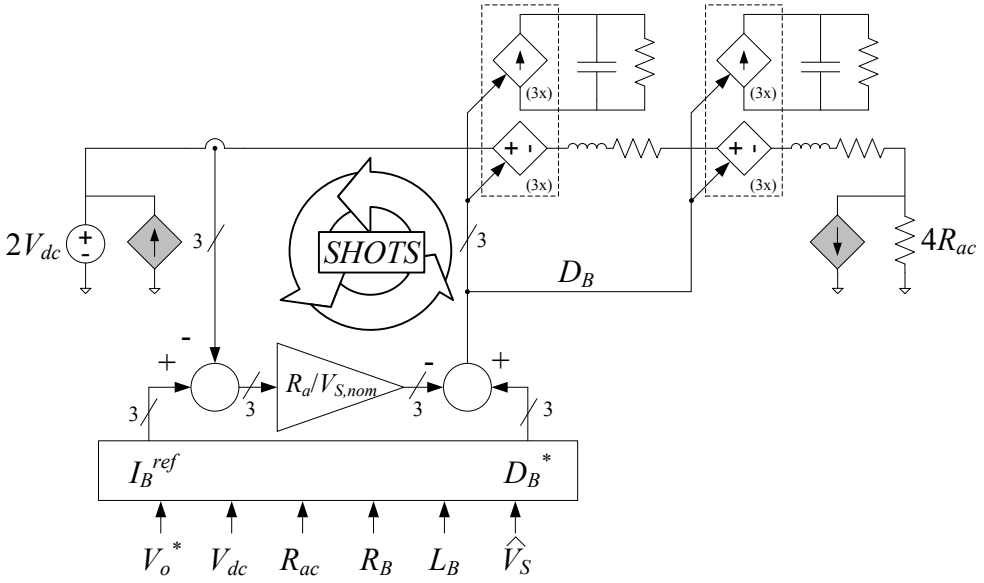


Fig. 5-1. Dynamic phasor model of branch with n_s=2.

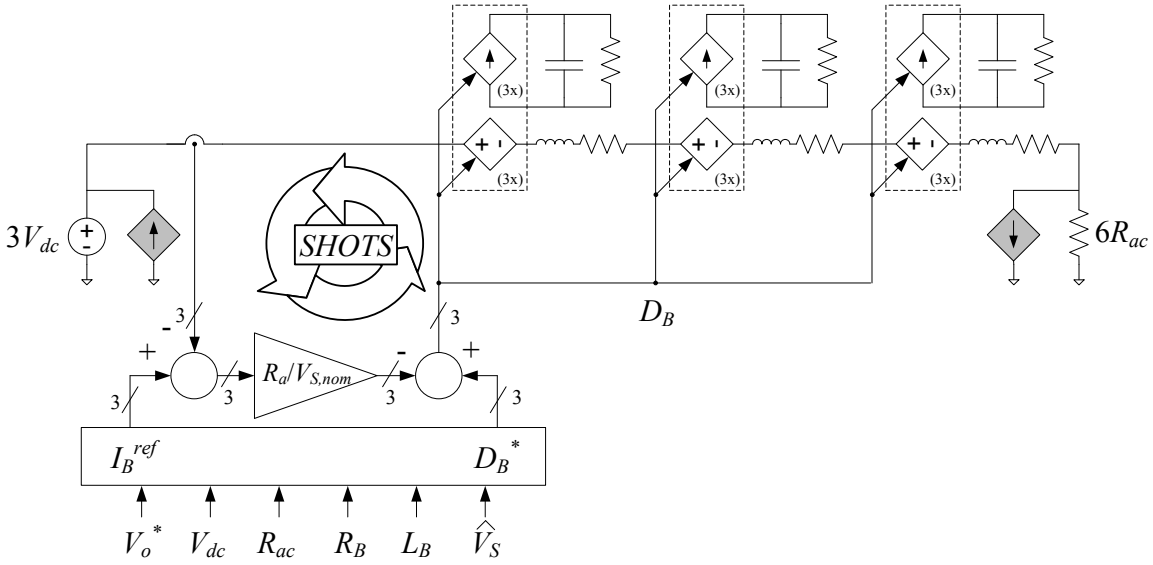


Fig. 5-2. Dynamic phasor model of branch with n_s=3.

5.2 2-Series branch (n_s=2)

A branch containing two series-connected bridges represents the simplest multilevel BoBC embodiment. It is presented here with an integral SHOTS controller based on the control motivation presented in the previous chapter. The DQ circuit model is first developed, followed by a nonlinear block diagram and small signal state space model. Steady-state solutions to the state space model are provided with eigenvalue analysis.

5.2.1 DQ equivalent circuit

Applying the DQ circuit modeling of Chapter 4 to the circuit of Fig. 5-1 yields the following dynamic model equations:

$$2L_B \frac{dI_{B,dc}}{dt} = 2V_{dc} - D_{B,dc,1}V_{S1} - D_{B,dc,2}V_{S2} - 2R_B I_{B,dc} \quad 5\text{-}2$$

$$2L_B \frac{dI_{B,ac,d}}{dt} = 2\omega_{ac} L_B I_{B,ac,q} - D_{B,ac,d,1}V_{S1} - D_{B,ac,d,2}V_{S2} - \left(2R_B + 4R_{ac}\right) I_{B,ac,d} \quad 5\text{-}3$$

$$2L_B \frac{dI_{B,ac,q}}{dt} = -2\omega_{ac} L_B I_{B,ac,d} - D_{B,ac,q,1}V_{S1} - D_{B,ac,q,2}V_{S2} - \left(2R_B + 4R_{ac}\right) I_{B,ac,q} \quad 5\text{-}4$$

$$C_{S1} \frac{dV_{S1}}{dt} = D_{B,ac,d,1} I_{B,dc} + D_{B,ac,q,1} I_{B,ac,q} + D_{B,ac,d,1} I_{B,ac,d} - \frac{V_{S1}}{R_{S1}} \quad 5\text{-}5$$

$$C_{S2} \frac{dV_{S2}}{dt} = D_{B,dc,2} I_{B,dc} + D_{B,ac,q,2} I_{B,ac,q} + D_{B,ac,d,2} I_{B,ac,d} - \frac{V_{S2}}{R_{S2}} \quad 5\text{-}6$$

The duty ratios of both bridges assume the same values as in the single bridge case,

$$D_{B,ac,d,1} = D_{B,ac,d,2} = D^*_{B,ac,d} - \frac{R_a}{V_{S,nom}}\left(I^{ref}_{B,ac,d} - I_{B,ac,d}\right) \quad 5\text{-}7$$

$$D_{B,ac,\mathrm{q},1} = D_{B,ac,q,2} = D^{*}_{B,ac,\mathrm{q}} - \frac{R_a}{V_{S,nom}}\left(I^{ref}_{B,ac,\mathrm{q}} - I_{B,ac,\mathrm{q}}\right) \quad 5\text{-}8$$

$$D_{B,\mathrm{dc},1} = D_{B,dc,2} = D^{*}_{B,\mathrm{dc}} - \frac{R_a}{V_{S,nom}}\left(I^{ref}_{B,\mathrm{dc}} - I_{B,\mathrm{dc}}\right). \quad 5\text{-}9$$

5.2.2 State block diagram

A full nonlinear state block diagram of the open loop n_s = 2 branch is shown in Fig. 5-3, as an extension to the n_s = 1 case of Fig. 4-4. A simplified nonlinear state block diagram is shown in Fig. 5-4, which is an extension from Fig. 4-8. The primary difference between the n_s=2 and n_s=1 cases is that multiple bridges exist, represented by one additional capacitor and additional V_{dc} input to the $I_{B,dc}$ plant. The additional inductance and resistance terms are implied within the 3 current plants in Fig. 5-4.

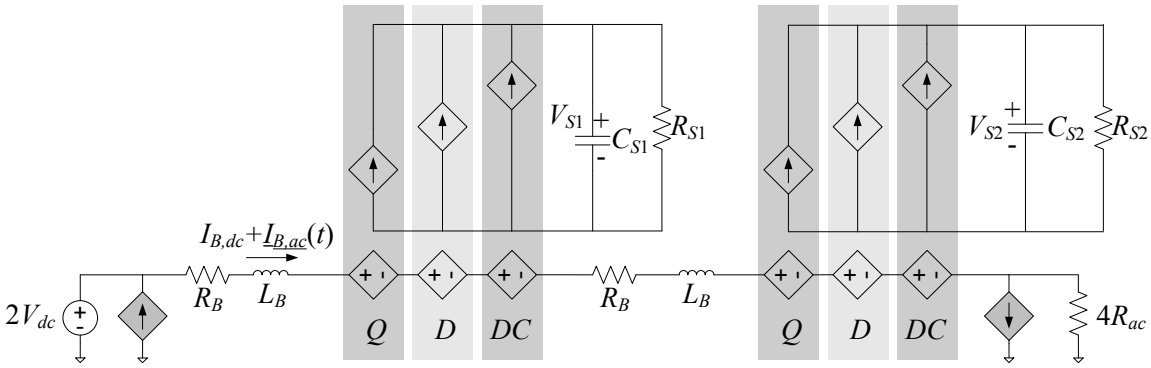


Fig. 5-3. Open loop dynamic phasor model of n_s=2 branch circuit.

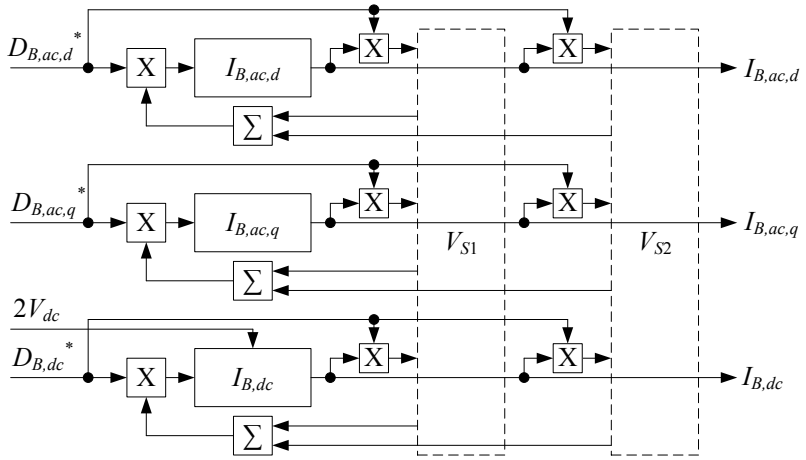


Fig. 5-4. Simplified closed loop nonlinear state block diagram for n_s=2.

5.2.3 State space model

The nonlinear dynamic models of Section 5.2.1 may be evaluated at an operating point to yield insight into the plant's dynamics. The resulting operating point model equations are:

$$\begin{aligned}\frac{d}{dt}\delta I_{B,ac,d} = {} & \delta I_{B,ac,d}\left[-\frac{R_a}{2L_B V_{S,nom}}\left(V_{S1}+V_{S2}\right)-\frac{R_B}{L_B}-\frac{2R_{ac}}{L_B}\right]+\omega_{ac}\delta I_{B,ac,q} \\ & +\left(\delta V_{S1}+\delta V_{S2}\right)\left[\frac{-D^*_{B,ac,d}}{2L_B}+\frac{R_a}{2L_B V_{S,\mathrm{nom}}}\left(I^{ref}_{B,ac,d}-I_{B,ac,d}\right)\right] \\ & +\delta D^*_{B,ac,d}\left[\frac{-V_{S1}-V_{S2}}{2L_B}\right]+\delta I^{ref}_{B,ac,d}\left[\frac{R_a\left(V_{S1}+V_{S2}\right)}{2L_B V_{S,nom}}\right]\end{aligned} \qquad 5\text{-}10$$

$$\frac{d}{dt}\delta I_{B,ac,\mathrm{q}} = -\omega_{ac}\delta I_{B,ac,d} + \delta I_{B,ac,q}\left[\frac{-R_a}{2L_B V_{S,nom}}\left(V_{S1}+V_{S2}\right)-\frac{R_B}{L_B}-\frac{2R_{ac}}{L_B}\right] + \left(\delta V_{S1}+\delta V_{S2}\right)\left[\frac{-D^*_{B,ac,q}}{2L_B}+\frac{R_a}{2L_B V_{S,nom}}\left(I^{ref}_{B,ac,q}-I_{B,ac,q}\right)\right] + \delta D^*_{B,ac,q}\left[\frac{-V_{S1}-V_{S2}}{2L_B}\right]+\delta I^{ref}_{B,ac,q}\left[\frac{R_a\left(V_{S1}+V_{S2}\right)}{2L_B V_{S,nom}}\right] \tag{5-11}$$

$$\frac{d}{dt}\delta I_{B,dc} = \delta I_{B,dc}\left[\frac{-R_a}{2L_B V_{S,nom}}\left(V_{S1}+V_{S2}\right)-\frac{R_B}{L_B}\right] + \left(\delta V_{S1}+\delta V_{S2}\right)\left[\frac{-D^*_{B,dc}}{2L_B}+\frac{R_a}{2L_B V_{S,nom}}\left(I^{ref}_{B,dc}-I_{B,dc}\right)\right] + \frac{V_{dc}}{L_B}+\delta D^*_{B,dc}\left[\frac{-V_{S1}-V_{S2}}{2L_B}\right]+\delta I^{ref}_{B,dc}\left[\frac{R_a\left(V_{S1}+V_{S2}\right)}{2L_B}\right] \tag{5-12}$$

$$\frac{d}{dt}\delta V_{S1} = \frac{\delta I_{B,ac,d}}{C_{S1}}\left[D^*_{B,ac,d}-\frac{R_a}{V_{S,nom}}\left(I^{ref}_{B,ac,d}-2I_{B,ac,d}\right)\right] + \frac{\delta I_{B,ac,q}}{C_{S1}}\left[D^*_{B,ac,q}-\frac{R_a}{V_{S,nom}}\left(I^{ref}_{B,ac,q}-2I_{B,dc,q}\right)\right] + \frac{\delta I_{B,dc}}{C_{S1}}\left[D^*_{B,dc}-\frac{R_a}{V_{S,nom}}\left(I^{ref}_{B,dc}-2I_{B,dc}\right)\right]+\delta V_{S1}\left[\frac{-1}{R_{S1}C_{S1}}\right] + \delta D^*_{B,ac,d}\left[\frac{I_{B,ac,d}}{C_{S1}}\right]+\delta D^*_{B,ac,q}\left[\frac{I_{B,ac,q}}{C_{S1}}\right]+\delta D^*_{B,dc}\left[\frac{I_{B,dc}}{C_{S1}}\right] + \delta I^{ref}_{B,dc}\left[\frac{-R_a I_{B,dc}}{C_{S1}V_{S,nom}}\right]+\delta I^{ref}_{B,ac,d}\left[\frac{-R_a I_{B,ac,d}}{C_{S1}V_{S,nom}}\right]+\delta I^{ref}_{B,ac,q}\left[\frac{-R_a I_{B,ac,q}}{C_{S1}V_{S,nom}}\right] \tag{5-13}$$

$$\begin{aligned}\frac{d}{dt}\delta V_{S2} = &\frac{\delta I_{B,ac,d}}{C_{S2}}\left[D^*_{B,ac,d} - \frac{R_a}{V_{S,nom}}\left(I^{ref}_{B,ac,d} - 2I_{B,ac,d}\right)\right] \\ &+\frac{\delta I_{B,ac,q}}{C_{S2}}\left[D^*_{B,ac,q} - \frac{R_a}{V_{S,nom}}\left(I^{ref}_{B,ac,q} - 2I_{B,dc,q}\right)\right] \\ &+\frac{\delta I_{B,dc}}{C_{S2}}\left[D^*_{B,dc} - \frac{R_a}{V_{S,nom}}\left(I^{ref}_{B,dc} - 2I_{B,dc}\right)\right] + \delta V_{S2}\left[\frac{-1}{R_{S2}C_{S2}}\right] \\ &+\delta D^*_{B,ac,d}\left[\frac{I_{B,ac,d}}{C_{S2}}\right] + \delta D^*_{B,ac,q}\left[\frac{I_{B,ac,q}}{C_{S2}}\right] + \delta D^*_{B,dc}\left[\frac{I_{B,dc}}{C_{S2}}\right] \\ &+\delta I^{ref}_{B,dc}\left[\frac{-R_a I_{B,dc}}{C_{S2}V_{S,nom}}\right] + \delta I^{ref}_{B,ac,d}\left[\frac{-R_a I_{B,ac,d}}{C_{S2}V_{S,nom}}\right] + \delta I^{ref}_{B,ac,q}\left[\frac{-R_a I_{B,ac,q}}{C_{S2}V_{S,nom}}\right]\end{aligned} \qquad 5\text{-}14$$

For the state and input vectors

$$x = \left[\delta I_{B,ac,d} \quad \delta I_{B,ac,q} \quad \delta I_{B,dc} \quad \delta V_{S1} \quad \delta V_{S2}\right]^T \qquad 5\text{-}15$$

$$u = \left[V_{dc} \quad \delta D^*_{B,ac,d} \quad \delta D^*_{B,ac,q} \quad \delta D^*_{B,dc} \quad \delta I^{ref}_{B,ac,d} \quad \delta I^{ref}_{B,ac,q} \quad \delta I^{ref}_{B,\mathrm{dc}}\right]^T \qquad 5\text{-}16$$

the state space matrices resulting from the operating point model equations above are given as

$$
A=\begin{bmatrix}
\frac{-R_a\left(V_{S1}+V_{S2}\right)}{2L_BV_{S,nom}}-\frac{R_B}{L_B}-\frac{2R_{ac}}{L_B} & \omega_{ac} & 0 & \cdots \\
-\omega_{ac} & \frac{-R_a\left(V_{S1}+V_{S2}\right)}{2L_BV_{S,nom}}-\frac{R_B}{L_B}-\frac{2R_{ac}}{L_B} & 0 & \\
0 & 0 & \frac{-R_a\left(V_{S1}+V_{S2}\right)}{2L_BV_{S,nom}}-\frac{R_B}{L_B} & \\
\frac{D^*_{B,ac,d}}{C_{S1}}-\frac{R_a\left(I^{ref}_{B,ac,d}-2I_{B,ac,d}\right)}{C_{S1}V_{S,nom}} & \frac{D^*_{B,ac,\mathrm{q}}}{C_{S1}}-\frac{R_a\left(I^{ref}_{B,ac,\mathrm{q}}-2I_{B,ac,q}\right)}{C_{S1}V_{S,nom}} & \frac{D^*_{B,dc}}{C_{S1}}-\frac{R_a\left(I^{ref}_{B,dc}-2I_{B,dc}\right)}{C_{S1}V_{S,nom}} & \\
\frac{D^*_{B,ac,d}}{C_{S2}}-\frac{R_a\left(I^{ref}_{B,ac,d}-2I_{B,ac,d}\right)}{C_{S2}V_{S,nom}} & \frac{D^*_{B,ac,\mathrm{q}}}{C_{S2}}-\frac{R_a\left(I^{ref}_{B,ac,\mathrm{q}}-2I_{B,ac,q}\right)}{C_{S2}V_{S,nom}} & \frac{D^*_{B,dc}}{C_{S2}}-\frac{R_a\left(I^{ref}_{B,dc}-2I_{B,dc}\right)}{C_{S2}V_{S,nom}} &
\end{bmatrix}
$$

$$
\begin{bmatrix}
\frac{-D^*_{B,ac,d}}{2L_B}+\frac{R_a\left(I^{ref}_{B,ac,d}-I_{B,ac,d}\right)}{2L_BV_{S,nom}} & \frac{-D^*_{B,ac,d}}{2L_B}+\frac{R_a\left(I^{ref}_{B,ac,d}-I_{B,ac,d}\right)}{2L_BV_{S,nom}} \\
\frac{-D^*_{B,ac,q}}{2L_B}+\frac{R_a\left(I^{ref}_{B,ac,q}-I_{B,ac,q}\right)}{2L_BV_{S,nom}} & \frac{-D^*_{B,ac,q}}{2L_B}+\frac{R_a\left(I^{ref}_{B,ac,q}-I_{B,ac,q}\right)}{2L_BV_{S,nom}} \\
\frac{-D^*_{B,dc}}{2L_B}+\frac{R_a\left(I^{ref}_{B,dc}-I_{B,dc}\right)}{2L_BV_{S,nom}} & \frac{-D^*_{B,dc}}{2L_B}+\frac{R_a\left(I^{ref}_{B,dc}-I_{B,dc}\right)}{2L_B} \\
\frac{-1}{R_{S1}C_{S1}} & 0 \\
0 & \frac{-1}{R_{S2}C_{S2}}
\end{bmatrix}
\qquad 5\text{-}17
$$

$$B = \begin{bmatrix} 0 & \frac{-V_{S1}-V_{S2}}{2L_B} & 0 & 0 & \\ 0 & 0 & \frac{-V_{S1}-V_{S2}}{2L_B} & 0 & \\ \frac{1}{L_B} & 0 & 0 & \frac{-V_{S1}-V_{S2}}{2L_B} & \cdots \\ 0 & \frac{I_{B,ac,d}}{C_{S1}} & \frac{I_{B,ac,q}}{C_{S1}} & \frac{I_{B,dc}}{C_{S1}} & \\ 0 & \frac{I_{B,ac,d}}{C_{S2}} & \frac{I_{B,ac,q}}{C_{S2}} & \frac{I_{B,dc}}{C_{S2}} & \end{bmatrix}$$

$$\begin{bmatrix} \frac{R_a\left(V_{S1}+V_{S2}\right)}{2L_B V_{S,nom}} & 0 & 0 \\ 0 & \frac{R_a\left(V_{S1}+V_{S2}\right)}{2L_B V_{S,nom}} & 0 \\ 0 & 0 & \frac{R_a\left(V_{S1}+V_{S2}\right)}{2L_B V_{S,nom}} \\ \frac{-R_a I_{B,ac,d}}{C_{S1} V_{S,nom}} & \frac{-R_a I_{B,ac,q}}{C_{S1} V_{S,nom}} & \frac{-R_a I_{B,dc}}{C_{S1} V_{S,nom}} \\ \frac{-R_a I_{B,ac,d}}{C_{S2} V_{S,nom}} & \frac{-R_a I_{B,ac,q}}{C_{S2} V_{S,nom}} & \frac{-R_a I_{B,dc}}{C_{S2} V_{S,nom}} \end{bmatrix} \qquad 5\text{-}18$$

Due to the existence of multiple capacitor voltages, a total (branch) capacitor voltage may be defined:

$$V_{S,\text{tot}} = V_{S1} + V_{S2} \qquad 5\text{-}19$$

This capacitor voltage is useful for representing the bulk capacitor voltage within the branch, providing the same amount of information as was available in Chapter 4. The remaining state space matrices are therefore

$$y = \begin{bmatrix} \delta I_{B,ac,d} \\ \delta I_{B,ac,q} \\ \delta I_{B,dc} \\ \delta V_{S,avg} \end{bmatrix} \quad C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 \end{bmatrix} \tag{5-20}$$

$$D = 0 \tag{5-21}$$

5.2.4 Steady state solution

The steady state solution to the state space equations may again be determined by setting the dynamic model derivative terms to zero. Assuming equal capacitors C_{Sx} and duty ratios of d, q, and dc components that are across both bridges,

$$C_{S1} = C_{S2} \tag{5-22}$$

$$D_{B,ac,d,1} = D_{B,ac,d,2} = D_{B,ac,d} \tag{5-23}$$

$$D_{B,ac,q,1} = D_{B,ac,q,2} = D_{B,ac,q} \tag{5-24}$$

$$D_{B,dc,1} = D_{B,dc,2} = D_{B,dc} \tag{5-25}$$

yields

$$\frac{V_{S1}^2}{R_{S1}} = \frac{V_{S2}^2}{R_{S2}} \tag{5-26}$$

Therefore, also setting $R_{S1} = R_{S2} = R_S$, and assuming unity power factor produces

$$V_{S1} = V_{S2} = V_S \tag{5-27}$$

$$D_{B,ac,q} = \frac{-\omega_{ac} L_B I_{B,ac,d}}{V_S} \tag{5-28}$$

$$D_{B,ac,d} = \frac{-\left(R_B + 2R_{ac}\right) I_{B,ac,d}}{V_S} \tag{5-29}$$

$$D_{B,dc} = \frac{V_{dc} - R_B I_{B,dc}}{V_S} \tag{5-30}$$

$$I_{B,dc} = \frac{V_{dc}}{2R_B} - \sqrt{\frac{V_{dc}^2}{4R_B^{\,2}} - \left(\frac{R_B + 2R_{ac}}{R_B}\right) I_{B,ac,d}^{\,2} - \frac{V_S^{\,2}}{R_S R_B}} \tag{5-31}$$

Note that these equations are identical to those representing the single bridge n_s=1 case (Eqs. 4-22, 4-23 and 4-26), which underscores the notion of modularity within the BoBC.

5.2.5 Eigenvalue study

The dynamics of the multilevel system are investigated by analyzing the eigenvalues. The same operating point of each bridge as Section 4.6 is used but with n_s = 2. The chosen parameter set is intended to best represent a change in system dynamics between two converters, which differ only in the number of bridges contained therein. As a consequence, the terminal dc voltage and ac resistance are both doubled, and all other parameters are identical. A summary of parameters is shown in Table 5-2, which yields the eigenvalues shown in Table 5-3.

These sets of eigenvalues maintain the stabilization pattern observed in Chapter 4 with increasing R_a, wherein the complex pair associated with the LC tank becomes purely real. Note the new eigenvalue, which is associated with the RC time constant of the new bridge. Furthermore, the remaining eigenvalues associated with the fundamental frequency and the LC tank are identical to the smaller systems already investigated.

Table 5-2. Converter parameters for dynamic analysis of n_s=2.

$2V_{dc}$	f_{ac}	$2L_B$	$2R_B$	$2R_{ac}$	R_S	C_S	V_S	$I_{B,ac,d}$
10 V	60 Hz	44 µH	0.02 Ω	5.5 Ω	750 Ω	5000 µF	30 V	0.71 A

Table 5-3. Eigenvalues for n_s=2, with and without SHOTS controller.

$R_a = 0$	$R_a = 0.005$
$-4.0\text{x}10^4 + j60$ Hz	$-4.1*10^4 + j60$ Hz
$-4.0\text{x}10^4 - j60$ Hz	$-4.1*10^4 - j60$ Hz
-36 + j71 Hz	-5.8 Hz
-36 – j71 Hz	$-1.2*10^3$ Hz
-0.042 Hz	-0.042 Hz

5.3 3-Series branch (n_s=3)

The same techniques may be employed for the 3-series branch as for the 2-series branch. The DQ circuit model is first developed, followed by a nonlinear block diagram and state space model. Steady-state solutions to the state space model are provided, and eigenvalue analysis and transfer functions derived.

5.3.1 DQ equivalent circuit

Using the same methods employed previously, the n_s = 3 branch is modeled as in Fig. 5-6, with the following dynamic model equations:

$$3L_B \frac{dI_{B,dc}}{dt} = 3V_{dc} - D_{B,dc,1}V_{S1} - D_{B,dc,2}V_{S2} - D_{B,dc,3}V_{S3} - 3R_B I_{B,ac,d} \qquad 5\text{-}32$$

$$3L_B \frac{dI_{B,ac,d}}{dt} = -\left(3R_B + 6R_{ac}\right) I_{B,ac,d} + 3\omega_{ac} L_B I_{B,ac,q} - D_{B,ac,d,1} V_{S1} - D_{B,ac,d,2} V_{S2} - D_{B,ac,d,3} V_{S3} \quad 5\text{-}33$$

$$3L_B \frac{dI_{B,ac,q}}{dt} = -3\omega_{ac} L_B I_{B,ac,d} - \left(3R_B + 6R_{ac}\right) I_{B,ac,q} - D_{B,ac,q,1} V_{S1} - D_{B,ac,q,2} V_{S2} - D_{B,ac,q,3} V_{S3} \quad 5\text{-}34$$

$$C_{S1} \frac{dV_{S1}}{dt} = D_{B,ac,d,1} I_{B,dc} + D_{B,ac,q,1} I_{B,ac,q} + D_{B,ac,d,1} I_{B,ac,d} - \frac{V_{S1}}{R_{S1}} \quad 5\text{-}35$$

$$C_{S2} \frac{dV_{S2}}{dt} = D_{B,dc,2} I_{B,dc} + D_{B,ac,q,2} I_{B,ac,q} + D_{B,ac,d,2} I_{B,ac,d} - \frac{V_{S2}}{R_{S2}} \quad 5\text{-}36$$

$$C_{S3} \frac{dV_{S3}}{dt} = D_{B,dc,3} I_{B,dc} + D_{B,ac,q,3} I_{B,ac,q} + D_{B,ac,d,3} I_{B,ac,d} - \frac{V_{S3}}{R_{S3}} \quad 5\text{-}37$$

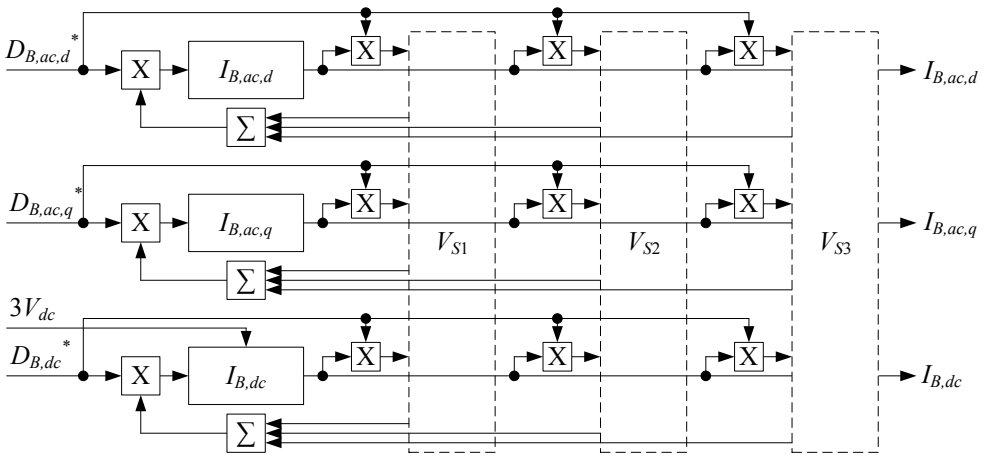


Fig. 5-5. Simplified nonlinear state block diagram for n_s=3.

5.3.1 State block diagram

A simplified closed loop nonlinear state block diagram is shown in Fig. 5-5, and a full open loop nonlinear state block diagram of a $n_s = 3$ branch is shown in Fig. 5-6. The primary difference between $n_s = 2$ and 3 are the additional R_{ac}, R_B, L_B and V_{dc} terms.

5.3.1 State space model

The nonlinear dynamic models of Section 5.3.1 may be evaluated at an operating point to yield insight into the plant's dynamics. The resulting equations are:

$$\begin{aligned}\frac{d}{dt}\delta I_{B,ac,d} = {} & \delta I_{B,ac,d}\left[\frac{-R_a\left(V_{S1}+V_{S2}+V_{S3}\right)}{3L_B V_{S,nom}} - \frac{R_B}{L_B} - \frac{2R_{ac}}{L_B}\right] + \omega_{ac}\delta I_{B,ac,q} \\ & + \left(\delta V_{S1}+\delta V_{S2}+\delta V_{S3}\right)\left[\frac{-D^*_{B,ac,d}}{3L_B} + \frac{R_a\left(I^{ref}_{B,ac,d} - I_{B,ac,d}\right)}{3L_B V_{S,nom}}\right] \\ & + \delta D^*_{B,ac,d}\left[\frac{-V_{S1}-V_{S2}-V_{S3}}{3L_B}\right] + \delta I^{ref}_{B,ac,d}\left[\frac{R_a\left(V_{S1}+V_{S2}+V_{S3}\right)}{3L_B V_{S,nom}}\right]\end{aligned} \qquad 5\text{-}38$$

$$\begin{aligned}\frac{d}{dt}\delta I_{B,ac,\mathrm{q}} = {} & -\omega_{ac}\delta I_{B,ac,d} + \delta I_{B,ac,q}\left[\frac{-R_a\left(V_{S1}+V_{S2}+V_{S3}\right)}{3L_B V_{S,nom}} - \frac{R_B}{L_B} - \frac{2R_{ac}}{L_B}\right] \\ & + \left(\delta V_{S1}+\delta V_{S2}+\delta V_{S3}\right)\left[\frac{-D^*_{B,ac,q}}{3L_B} + \frac{R_a\left(I^{ref}_{B,ac,q} - I_{B,ac,q}\right)}{3L_B V_{S,nom}}\right] \\ & + \delta D^*_{B,ac,q}\left[\frac{-V_{S1}-V_{S2}-V_{S3}}{3L_B}\right] + \delta I^{ref}_{B,ac,q}\left[\frac{R_a\left(V_{S1}+V_{S2}+V_{S3}\right)}{3L_B V_{S,nom}}\right]\end{aligned} \qquad 5\text{-}39$$

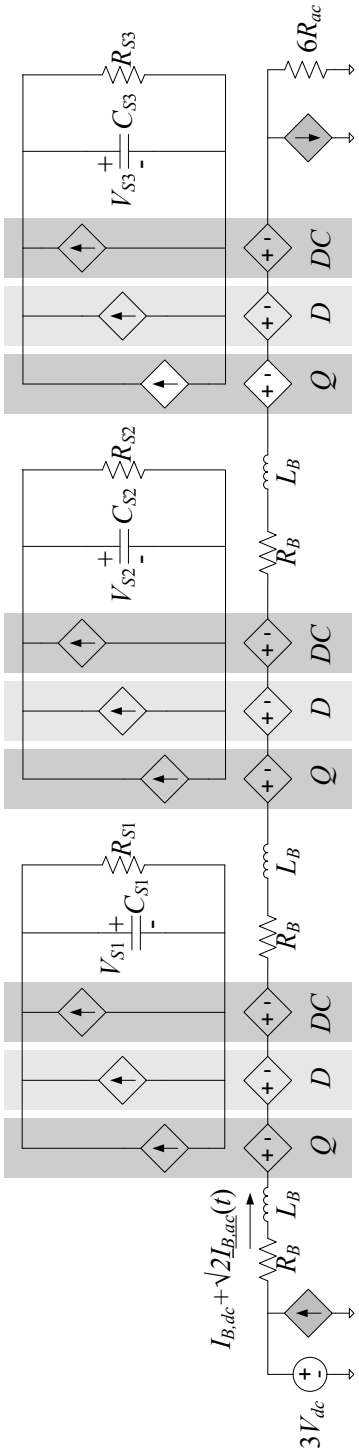


Fig. 5-6. Open loop dynamic phasor model of n_s=3 branch circuit.

$$\frac{d}{dt}\delta I_{B,dc} = \delta I_{B,dc}\left[\frac{-R_a\left(V_{S1}+V_{S2}+V_{S3}\right)}{3L_B V_{S,nom}} - \frac{2R_B}{L_B}\right] + \left(\delta V_{S1}+\delta V_{S2}+\delta V_{S3}\right)\left[\frac{-D^*_{B,dc}}{3L_B} + \frac{R_a\left(I^{ref}_{B,dc}-I_{B,dc}\right)}{3L_B V_{S,nom}}\right] + \frac{V_{dc}}{L_B} + \delta D^*_{B,dc}\left[\frac{-V_{S1}-V_{S2}-V_{S3}}{3L_B}\right] + \delta I^{ref}_{B,dc}\left[\frac{R_a\left(V_{S1}+V_{S2}+V_{S3}\right)}{3L_B V_{S,nom}}\right] \quad 5\text{-}40$$

$$\frac{d}{dt}\delta V_{S1} = \delta I_{B,ac,d}\left[\frac{D^*_{B,ac,d}}{C_{S1}} - \frac{R_a\left(I^{ref}_{B,ac,d}-2I_{B,ac,d}\right)}{C_{S1}V_{S,nom}}\right] + \delta I_{B,ac,q}\left[\frac{D^*_{B,ac,q}}{C_{S1}} - \frac{R_a\left(I^{ref}_{B,ac,q}-2I_{B,ac,q}\right)}{C_{S1}V_{S,nom}}\right] + \delta I_{B,dc}\left[\frac{D^*_{B,ac,d}}{C_{S1}} - \frac{R_a\left(I^{ref}_{B,dc}-2I_{B,dc}\right)}{C_{S1}V_{S,nom}}\right] - \frac{\delta V_{S1}}{R_{S1}C_{S1}} + \delta D^*_{B,ac,d}\left[\frac{I_{B,ac,d}}{C_{S1}}\right] + \delta D^*_{B,ac,q}\left[\frac{I_{B,ac,q}}{C_{S1}}\right] + \delta D^*_{B,dc}\left[\frac{I_{B,dc}}{C_{S1}}\right] + \delta I^{ref}_{B,dc}\left[\frac{-R_a I_{B,dc}}{C_{S1}}\right] + \delta I^{ref}_{B,ac,d}\left[\frac{-R_a I_{B,ac,d}}{C_{S1}}\right] + \delta I^{ref}_{B,ac,q}\left[\frac{-R_a I_{B,ac,q}}{C_{S1}}\right] \quad 5\text{-}41$$

$$\frac{d}{dt}\delta V_{S2} = \delta I_{B,ac,d}\left[\frac{D^*_{B,ac,d}}{C_{S2}} - \frac{R_a\left(I^{ref}_{B,ac,d}-2I_{B,ac,d}\right)}{C_{S2}V_{S,nom}}\right] + \delta I_{B,ac,q}\left[\frac{D^*_{B,ac,q}}{C_{S2}} - \frac{R_a\left(I^{ref}_{B,ac,q}-2I_{B,ac,q}\right)}{C_{S2}V_{S,nom}}\right] + \delta I_{B,dc}\left[\frac{D^*_{B,ac,d}}{C_{S2}} - \frac{R_a\left(I^{ref}_{B,dc}-2I_{B,dc}\right)}{C_{S2}V_{S,nom}}\right] - \frac{\delta V_{S2}}{R_{S2}C_{S2}} + \delta D^*_{B,ac,d}\left[\frac{I_{B,ac,d}}{C_{S2}}\right] + \delta D^*_{B,ac,q}\left[\frac{I_{B,ac,q}}{C_{S2}}\right] + \delta D^*_{B,dc}\left[\frac{I_{B,dc}}{C_{S2}}\right] + \delta I^{ref}_{B,dc}\left[\frac{-R_a I_{B,dc}}{C_{S2}}\right] + \delta I^{ref}_{B,ac,d}\left[\frac{-R_a I_{B,ac,d}}{C_{S2}}\right] + \delta I^{ref}_{B,ac,q}\left[\frac{-R_a I_{B,ac,q}}{C_{S2}}\right] \quad 5\text{-}42$$

$$\begin{aligned}\frac{d}{dt}\delta V_{S3} = {} & \delta I_{B,ac,d}\left[\frac{D^*_{B,ac,d}}{C_{S3}} - \frac{R_a\left(I^{ref}_{B,ac,d} - 2I_{B,ac,d}\right)}{C_{S3}V_{S,nom}}\right] \\ & + \delta I_{B,ac,q}\left[\frac{D^*_{B,ac,q}}{C_{S3}} - \frac{R_a\left(I^{ref}_{B,ac,q} - 2I_{B,ac,q}\right)}{C_{S3}V_{S,nom}}\right] \\ & + \delta I_{B,dc}\left[\frac{D^*_{B,ac,d}}{C_{S3}} - \frac{R_a\left(I^{ref}_{B,dc} - 2I_{B,dc}\right)}{C_{S3}V_{S,nom}}\right] - \frac{\delta V_{S1}}{R_{S3}C_{S3}} \\ & + \delta D^*_{B,ac,d}\left[\frac{I_{B,ac,d}}{C_{S3}}\right] + \delta D^*_{B,ac,q}\left[\frac{I_{B,ac,q}}{C_{S3}}\right] + \delta D^*_{B,dc}\left[\frac{I_{B,dc}}{C_{S3}}\right] \\ & + \delta I^{ref}_{B,dc}\left[\frac{-R_a I_{B,dc}}{C_{S3}}\right] + \delta I^{ref}_{B,ac,d}\left[\frac{-R_a I_{B,ac,d}}{C_{S3}}\right] + \delta I^{ref}_{B,ac,q}\left[\frac{-R_a I_{B,ac,q}}{C_{S3}}\right]\end{aligned} \quad 5\text{-}43$$

For the state and input vectors

$$x = \begin{bmatrix}\delta I_{B,ac,d} & \delta I_{B,ac,q} & \delta I_{B,dc} & \delta V_{S1} & \delta V_{S2} & \delta V_{S3}\end{bmatrix}^T \quad 5\text{-}44$$

$$u = \begin{bmatrix}V_{dc} & \delta D^*_{B,ac,d} & \delta D^*_{B,ac,\mathrm{q}} & \delta D^*_{B,dc} & \delta I^{ref}_{B,ac,d} & \delta I^{ref}_{B,ac,q} & \delta I^{ref}_{B,dc}\end{bmatrix}^T \quad 5\text{-}45$$

the state space matrices resulting from the equations above are given in Eqs. 5-48 and 5-49.

The total capacitor voltage in the branch is similarly defined:

$$V_{S,\mathrm{tot}} = V_{S1} + V_{S2} + V_{S3} \quad 5\text{-}46$$

The remaining state space matrices are therefore

$$y = \begin{bmatrix}\delta I_{B,ac,d} \\ \delta I_{B,ac,q} \\ \delta I_{B,dc} \\ \delta V_{S,avg}\end{bmatrix} \quad C = \begin{bmatrix}1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1\end{bmatrix} \quad D = 0 \quad 5\text{-}47$$

$$
A=\begin{bmatrix}
\frac{-R_a\left(V_{S1}+V_{S2}+V_{S3}\right)}{3L_BV_{S,nom}}-\frac{R_B}{L_B}-\frac{2R_{ac}}{L_B} & \omega_{ac} & 0 & \cdots \\
-\omega_{ac} & \frac{-R_a\left(V_{S1}+V_{S2}+V_{S3}\right)}{3L_BV_{S,nom}}-\frac{R_B}{L_B}-\frac{2R_{ac}}{L_B} & 0 & \cdots \\
0 & 0 & \frac{-R_a\left(V_{S1}+V_{S2}+V_{S3}\right)}{3L_BV_{S,nom}}-\frac{R_B}{L_B} & \cdots \\
\frac{D^*_{B,ac,d}}{C_{S1}}-\frac{R_a\left(I^{ref}_{B,ac,d}-2I_{B,ac,d}\right)}{C_{S1}V_{S,nom}} & \frac{D^*_{B,ac,\mathrm{q}}}{C_{S1}}-\frac{R_a\left(I^{ref}_{B,ac,\mathrm{q}}-2I_{B,ac,q}\right)}{C_{S1}V_{S,nom}} & \frac{D^*_{B,dc}}{C_{S1}}-\frac{R_a\left(I^{ref}_{B,dc}-2I_{B,dc}\right)}{C_{S1}V_{S,nom}} & \cdots \\
\frac{D^*_{B,ac,d}}{C_{S2}}-\frac{R_a\left(I^{ref}_{B,ac,d}-2I_{B,ac,d}\right)}{C_{S2}V_{S,nom}} & \frac{D^*_{B,ac,\mathrm{q}}}{C_{S2}}-\frac{R_a\left(I^{ref}_{B,ac,\mathrm{q}}-2I_{B,ac,q}\right)}{C_{S2}V_{S,nom}} & \frac{D^*_{B,dc}}{C_{S2}}-\frac{R_a\left(I^{ref}_{B,dc}-2I_{B,dc}\right)}{C_{S2}V_{S,nom}} & \cdots \\
\frac{D^*_{B,ac,d}}{C_{S3}}-\frac{R_a\left(I^{ref}_{B,ac,d}-2I_{B,ac,d}\right)}{C_{S3}V_{S,nom}} & \frac{D^*_{B,ac,\mathrm{q}}}{C_{S3}}-\frac{R_a\left(I^{ref}_{B,ac,\mathrm{q}}-2I_{B,ac,q}\right)}{C_{S3}V_{S,nom}} & \frac{D^*_{B,dc}}{C_{S3}}-\frac{R_a\left(I^{ref}_{B,dc}-2I_{B,dc}\right)}{C_{S3}V_{S,nom}} & \cdots
\end{bmatrix}
$$

$$
\begin{bmatrix}
\frac{-D^*_{B,ac,d}}{3L_B}+\frac{R_a\left(I^{ref}_{B,ac,d}-I_{B,ac,d}\right)}{3L_BV_{S,nom}} & \frac{-D^*_{B,ac,d}}{3L_B}+\frac{R_a\left(I^{ref}_{B,ac,d}-I_{B,ac,d}\right)}{3L_BV_{S,nom}} & \frac{-D^*_{B,ac,d}}{3L_B}+\frac{R_a\left(I^{ref}_{B,ac,d}-I_{B,ac,d}\right)}{3L_BV_{S,nom}} \\
\frac{-D^*_{B,ac,q}}{3L_B}+\frac{R_a\left(I^{ref}_{B,ac,q}-I_{B,ac,q}\right)}{3L_BV_{S,nom}} & \frac{-D^*_{B,ac,q}}{3L_B}+\frac{R_a\left(I^{ref}_{B,ac,q}-I_{B,ac,q}\right)}{3L_BV_{S,nom}} & \frac{-D^*_{B,ac,q}}{3L_B}+\frac{R_a\left(I^{ref}_{B,ac,q}-I_{B,ac,q}\right)}{3L_BV_{S,nom}} \\
\frac{-D^*_{B,dc}}{3L_B}+\frac{R_a\left(I^{ref}_{B,dc}-I_{B,dc}\right)}{3L_BV_{S,nom}} & \frac{-D^*_{B,dc}}{3L_B}+\frac{R_a\left(I^{ref}_{B,dc}-I_{B,dc}\right)}{3L_B} & \frac{-D^*_{B,dc}}{3L_B}+\frac{R_a\left(I^{ref}_{B,dc}-I_{B,dc}\right)}{3L_B} \\
-1/R_{S1}C_{S1} & 0 & 0 \\
0 & -1/R_{S2}C_{S2} & 0 \\
0 & 0 & -1/R_{S3}C_{S3}
\end{bmatrix}
\qquad \text{5-48}
$$

$$B=\begin{bmatrix} 0 & \frac{-V_{S1}-V_{S2}-V_{S3}}{3L_B} & 0 & 0 \\ 0 & 0 & \frac{-V_{S1}-V_{S2}-V_{S3}}{3L_B} & 0 \\ \frac{1}{L_B} & 0 & 0 & \frac{-V_{S1}-V_{S2}-V_{S3}}{3L_B} \\ 0 & \frac{I_{B,ac,d}}{C_{S1}} & \frac{I_{B,ac,q}}{C_{S1}} & \frac{I_{B,dc}}{C_{S1}} \\ 0 & \frac{I_{B,ac,d}}{C_{S2}} & \frac{I_{B,ac,q}}{C_{S2}} & \frac{I_{B,dc}}{C_{S2}} \\ 0 & \frac{I_{B,ac,d}}{C_{S3}} & \frac{I_{B,ac,q}}{C_{S3}} & \frac{I_{B,dc}}{C_{S3}} \end{bmatrix} \cdots$$

$$\begin{bmatrix} \frac{R_a\left(V_{S1}+V_{S2}+V_{S3}\right)}{3L_BV_{S,nom}} & 0 & 0 \\ 0 & \frac{R_a\left(V_{S1}+V_{S2}+V_{S3}\right)}{3L_BV_{S,nom}} & 0 \\ 0 & 0 & \frac{R_a\left(V_{S1}+V_{S2}+V_{S3}\right)}{3L_BV_{S,nom}} \\ \frac{-R_aI_{B,ac,d}}{C_{S1}V_{S,nom}} & \frac{-R_aI_{B,ac,q}}{C_{S1}V_{S,nom}} & \frac{-R_aI_{B,dc}}{C_{S1}V_{S,nom}} \\ \frac{-R_aI_{B,ac,d}}{C_{S2}V_{S,nom}} & \frac{-R_aI_{B,ac,q}}{C_{S2}V_{S,nom}} & \frac{-R_aI_{B,dc}}{C_{S2}V_{S,nom}} \\ \frac{-R_aI_{B,ac,d}}{C_{S3}V_{S,nom}} & \frac{-R_aI_{B,ac,q}}{C_{S3}V_{S,nom}} & \frac{-R_aI_{B,dc}}{C_{S3}V_{S,nom}} \end{bmatrix} \quad 5\text{-}49$$

5.3.2 Steady state solution

Setting the dynamic model derivative terms to zero and assuming equal capacitors C_{Sx} and duty ratios of d, q, and dc components that are across both bridges,

$$C_{S1} = C_{S2} = C_{S3} \quad 5\text{-}50$$

$$D_{B,ac,d,1} = D_{B,ac,d,2} = D_{B,ac,d,3} = D^*_{B,ac,d} - R_a\left(I^{ref}_{B,ac,d} - I_{B,ac,d}\right) \quad 5\text{-}51$$

$$D_{B,ac,q,1} = D_{B,ac,q,2} = D_{B,ac,q,3} = D^*_{B,ac,q} - R_a\left(I^{ref}_{B,ac,q} - I_{B,ac,q}\right) \quad 5\text{-}52$$

$$D_{B,\mathrm{dc},1} = D_{B,dc,2} = D_{B,dc,3} = D^*_{B,\mathrm{d}c} - R_a\left(I^{ref}_{B,\mathrm{dc}} - I_{B,\mathrm{d}c}\right) \quad 5\text{-}53$$

yields

$$\frac{V_{S1}}{R_{S1}} = \frac{V_{S2}}{R_{S2}} = \frac{V_{S3}}{R_{S3}} \quad 5\text{-}54$$

Therefore, also setting $R_{S1} = R_{S2} = R_{S3} = R_S$ and assuming unity power factor produces

$$V_{S1} = V_{S2} = V_{S3} = V_S \quad 5\text{-}55$$

$$D_{B,ac,q} = \frac{-\omega_{ac} L_B I_{B,ac,d}}{V_S} \quad 5\text{-}56$$

$$D_{B,ac,d} = \frac{-\left(R_B + 2R_{ac}\right) I_{B,ac,d}}{V_s} \quad 5\text{-}57$$

$$D_{B,dc} = \frac{V_{dc} - R_B I_{B,dc}}{V_S} \quad 5\text{-}58$$

$$I_{B,dc} = \frac{V_{dc}}{2R_B} - \sqrt{\frac{V_{dc}^2}{4{R_B}^2} - \left(\frac{R_B + 2R_{ac}}{R_B}\right){I_{B,ac,d}}^2 - \frac{{V_S}^2}{R_S R_B}} \quad 5\text{-}59$$

5.3.3 Eigenvalue study

The dynamics of the multilevel system are investigated by analyzing the eigenvalues. The same operating point as previous analyses is used but with $n_s = 3$ and constant total

power load through R_S. A summary of parameters are shown in Table 5-4, which yields the eigenvalues shown in Table 5-5.

These sets of eigenvalues maintain the stabilization pattern observed in Chapter 4 with increasing R_a, wherein the complex pair associated with the LC tank becomes purely real. Note the new eigenvalue, which is associated with the RC time constant of the new bridge, and is identical to the other RC eigenvalue due to bridge symmetry. Furthermore, the remaining eigenvalues associated with the fundamental frequency and the LC tank are identical to the smaller systems already investigated.

Table 5-4. Converter parameters for dynamic analysis of n_s=3.

$3V_{dc}$	f_{ac}	$3L_B$	$3R_B$	$3R_{ac}$	R_S	C_S	V_S	$I_{B,ac,d}$
15 V	60 Hz	66 μH	0.03 Ω	8.2 Ω	750 Ω	5000 μF	30 V	0.71 A

Table 5-5. Eigenvalues for n_s=3 at one operating point, with and without SHOTS controller.

$R_a = 0$	$R_a = 0.15$
$-4.0\text{x}10^4$ + j60 Hz	$-4.1*10^4$ + j60 Hz
$-4.0\text{x}10^4$ - j60 Hz	$-4.1*10^4$ - j60 Hz
-36 + j71 Hz	-5.8 Hz
-36 – j71 Hz	$-1.1*10^3$ Hz
-0.042 Hz	-0.042 Hz
-0.042 Hz	-0.042 Hz

5.4 Eigenvalue scaling trends

The eigenvalues of all 3 cases of n_s may be examined for identifying patterns and therefore indications of scaling towards higher values of n_s. The data from Sections 4.6, 5.2.5 and 5.3.3 are repeated together below in

Table 5-6 and Table 5-7. The tables indicate that, in fact, the eigenvalues of the fundamental frequency and the LC tank remain unchanged across varying n_s values.

Table 5-6. Summary of eigenvalue without SHOTS ($R_a = 0$)

$n_s = 1$	$n_s = 2$	$n_s = 3$
$-4.0\text{x}10^4 + \text{j}60$ Hz	$-4.0\text{x}10^4 + \text{j}60$ Hz	$-4.0\text{x}10^4 + \text{j}60$ Hz
$-4.0\text{x}10^4 - \text{j}60$ Hz	$-4.0\text{x}10^4 - \text{j}60$ Hz	$-4.0\text{x}10^4 - \text{j}60$ Hz
-36 + j71 Hz	-36 + j71 Hz	-36 + j71 Hz
-36 - j71 Hz	-36 – j71 Hz	-36 – j71 Hz
	-0.042 Hz	-0.042 Hz
		-0.042 Hz

Table 5-7. Summary of eigenvalues with SHOTS ($R_a = 0.15$)

$n_s = 1$	$n_s = 2$	$n_s = 3$
$-4.1\text{x}10^4 + \text{j}60$ Hz	$-4.1*10^4 + \text{j}60$ Hz	$-4.1*10^4 + \text{j}60$ Hz
$-4.1\text{x}10^4 - \text{j}60$ Hz	$-4.1*10^4 - \text{j}60$ Hz	$-4.1*10^4 - \text{j}60$ Hz
-5.8 Hz	-5.8 Hz	-5.8 Hz
$-1.2\text{x}10^3$ Hz	$-1.2*10^3$ Hz	$-1.2*10^3$ Hz
	-0.042 Hz	-0.042 Hz
		-0.042 Hz

To investigate why the eigenvalues remain constant (with the exception of any additional RC terms), the n_s=2 state space A matrix (considering all components) is considered. Starting with the general structure of

$$A=\begin{bmatrix} \frac{-R_{eff,ac}}{L_B} & \omega_{ac} & 0 & \frac{-D_{B,ac,d,1}}{2L_B} & \frac{-D_{B,ac,d,2}}{2L_B} \\ -\omega_{ac} & \frac{-R_{eff,ac}}{L_B} & 0 & \frac{-D_{B,ac,q,1}}{2L_B} & \frac{-D_{B,ac,q,2}}{2L_B} \\ 0 & 0 & \frac{-R_{eff,dc}}{L_B} & \frac{-D_{B,dc,1}}{2L_B} & \frac{-D_{B,dc,2}}{2L_B} \\ \frac{D_{B,ac,d,1}}{C_{S1}} & \frac{D_{B,ac,q,1}}{C_{S1}} & \frac{D_{B,dc,1}}{C_{S1}} & \frac{-1}{R_{S1}C_{S1}} & 0 \\ \frac{D_{B,ac,d,2}}{C_{S2}} & \frac{D_{B,ac,q,2}}{C_{S2}} & \frac{D_{B,dc,2}}{C_{S2}} & 0 & \frac{-1}{R_{S2}C_{S2}} \end{bmatrix}, \qquad 5\text{-}60$$

where the individual elements refer to generalizations of the elements in Eq. 5-17, it is seen that this form does not provide transparency of eigenvalue location. Row operations cannot generally be used to determine eigenvalue location, as this is known to actually change the eigenvalues [121]. However, similar matrices share eigenvalues [122]; therefore, to facilitate the identification of the eigenvalues, a matrix similarity transformation Q is proposed:

$$A_{mod}=Q^{-1}AQ, \qquad 5\text{-}61$$

where Q contains a third order identity matrix combined with a lower triangular block matrix of ones:

$$Q = \begin{bmatrix} [I_3] & [0] \\ [0] & \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 \end{bmatrix}. \qquad 5\text{-}62$$

For compactness, A is abbreviated

$$A = \begin{bmatrix} \frac{-R_{eff,ac}}{L_B} & \omega_{ac} & 0 & \frac{-k_1}{2} & \frac{-k_2}{2} \\ -\omega_{ac} & \frac{-R_{eff,ac}}{L_B} & 0 & \frac{-l_1}{2} & \frac{-l_2}{2} \\ 0 & 0 & \frac{-R_{eff,dc}}{L_B} & \frac{-m_1}{2} & \frac{-m_2}{2} \\ K_1 & L_1 & M_1 & \frac{-1}{R_{S1}C_{S1}} & 0 \\ K_2 & L_2 & M_2 & 0 & \frac{-1}{R_{S2}C_{S2}} \end{bmatrix}, \qquad 5\text{-}63$$

leading to

$$A_{\text{mod}} = \begin{bmatrix} \frac{-R_{eff,ac}}{L_B} & \omega_{ac} & 0 & \frac{-k_1-k_2}{2} & \frac{-k_2}{2} \\ -\omega_{ac} & \frac{-R_{eff,ac}}{L_B} & 0 & \frac{-l_1-l_2}{2} & \frac{-l_2}{2} \\ 0 & 0 & \frac{-R_{eff,dc}}{L_B} & \frac{-m_1-m_2}{2} & \frac{-m_2}{2} \\ K_1 & L_1 & M_1 & \frac{-1}{R_{S1}C_{S1}} & 0 \\ K_2-K_1 & L_2-L_1 & M_2-M_1 & \frac{-1}{R_{S1}C_{S1}}-\frac{1}{R_{S2}C_{S2}} & \frac{-1}{R_{S2}C_{S2}} \end{bmatrix}. \qquad 5\text{-}64$$

When assuming/approximating identical bridges (duty ratios, resistors, capacitors, etc.), the various *k*, *K*, *l*, *L*, *m*, and *M* terms become equal, yielding

$$A_{\text{mod}} \approx \begin{bmatrix} \frac{-R_{eff,ac}}{L_B} & \omega_{ac} & 0 & -k & \frac{-k_2}{2} \\ -\omega_{ac} & \frac{-R_{eff,ac}}{L_B} & 0 & -l & \frac{-l_2}{2} \\ 0 & 0 & \frac{-R_{eff,dc}}{L_B} & -m & \frac{-m_2}{2} \\ K_1 & L_1 & M_1 & \frac{-1}{R_S C_S} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{R_S C_S} \end{bmatrix} \qquad 5\text{-}65$$

or, equivalently,

$$A_{\text{mod}} \approx \begin{bmatrix} \frac{-R_{eff,ac}}{L_B} & \omega_{ac} & 0 & \frac{-D_{B,ac,d}}{L_B} & \frac{-D_{B,ac,d}}{2L_B} \\ -\omega_{ac} & \frac{-R_{eff,ac}}{L_B} & 0 & \frac{-D_{B,ac,q}}{L_B} & \frac{-D_{B,ac,q}}{2L_B} \\ 0 & 0 & \frac{-R_{eff,dc}}{L_B} & \frac{-D_{B,dc}}{L_B} & \frac{-D_{B,dc}}{2L_B} \\ \frac{D_{B,ac,d}}{C_S} & \frac{D_{B,ac,q}}{C_S} & \frac{D_{B,dc}}{C_S} & \frac{-1}{R_S C_S} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{R_S C_S} \end{bmatrix} \qquad 5\text{-}66$$

Two key observations about A_{mod} are made:

1) The upper-left 4x4 submatrix is equal to the 4th order system of Chapter 4, therefore 4 of the 5th order system's eigenvalues are identical to those of the 4th order system, and

2) The zero elements in the 5th row comprise a 1x4 zero block matrix. The attributes of determinants indicate that the 5th column elements may be disregarded, leading to an eigenvalue exactly at the diagonal element, i.e. $s = \frac{-1}{R_S C_S}$.

By simple extension, the use of the proposed similarity transformation may be applied to a converter with an arbitrary number of bridges. The observations above give rise to the notion that, for a BoBC with n_s series-connected bridges, two eigenvalues independent of n_s will be related to ω_{ac}; another two independent of n_s will be related to L_B, C_S and R_a; and n_s-1 will be located at -1/$R_S C_S$. Or, simply, adding one bridge to a branch only adds one eigenvalue at -1/$R_S C_S$.

5.5 Summary

This chapter expanded upon the "unit bridge" modeling of Chapter 4 to include the BoBC's multilevel nature for the specific cases of n_s = 2 and n_s = 3, including the SHOTS controller. Several simplified diagrams were presented to illustrate how the fundamental system components (plants) scale to higher and higher levels, while still maintaining relative clarity.

The full nonlinear dynamic models of the multilevel systems were developed from their respective equivalent circuits. These models were then evaluated at an operating point and presented in state space form with the steady state solutions, which were identical to their n_s=1 counterparts from Chapter 4 due to the inherent modularity and scalability of the BoBC.

Eigenvalue analysis confirmed system stability over a range of R_a for both system embodiments, and scaling of the eigenvalues for all 3 cases of n_s demonstrated clear patterns for extending the model to greater levels of complexity. Finally, a mathematical scaling relationship was established for predicting eigenvalues of higher order systems.

Chapter 6 Model Validation

This chapter validates the analytical developments presented in previous chapters using both averaged model circuit simulations and a hardware converter. The hardware converter was designed with flexibility in mind, to facilitate the exploration of topological behavior across an operating space, rather than designed for use in a specific application with an established set of terminal characteristics.

6.1 Converter specifications and representations

A common set of converter specifications was established across analytical, simulation and experimental platforms to facilitate comparison. These design specifications for the converter as a whole are shown in Table 6-1, and specifications for the CSEBs are shown in Table 6-2.

The converter was intended as a demonstrator of the generalized topological functionality, versus a converter for a specific application. Therefore, the converter design was focused on the CSEBs rather than on the desired terminal quantities. For example, the presence of variable dc and ac duty ratios implies a variable k_{tr}, and therefore variable $n_s V_S$ and $n_s V_{ac}$ for a given $n_s V_{dc}$. As discussed in Chapter 3, the

converter real power rating is also a function of k_{tr}, thus a power rating for the generalized topological power converter demonstrator cannot be established.

Table 6-1. Converter design specifications (in rms where applicable).

Parameter	Value
n_s	3
$n_s V_{dc}$	10 V to 30 V
$n_s V_{ac}$	$\leq$ 20 V
$n_s R_{ac}$	8.2 Ω
I_{dc}	$\leq$ 3.5 A
$\cos(\varphi_{ac})$	1
n_{br}	2
F_s[2]	300 kHz
k_{tr}	$< \sqrt{2}$

Table 6-2. Design parameters for CSEBs within the converter.

Parameter	Value
Type	Semi-Full bridge
F_s[2]	100 kHz
V_S	20 V to 55 V
C_S	5000 µF
R_S	750 Ω

The circuit topology is shown in Fig. 6-1. To reduce the system order and simplify analysis, comparisons are drawn based on a single branch, with the entire converter being considered a straightforward extension of the one branch. This is a reasonable approach when the branches are not cross-coupled, e.g. the input and output of each branch shares a common node such as ground. Nevertheless, an inherent property of the BoBC is the

[2] Pertains only to the hardware/experimental converter.

cancelation of dc and ac components across branches, as depicted in Fig. 4-2, hence simulating or experimentally constructing just one branch would yield an inaccurate representation of the system. For this reason, overall converter representations may vary slightly between analytical, simulation and hardware platforms, but the motivation is to achieve an accurate branch-level representation for subsequent analysis.

6.2 Design of candidate power converter

The converter design parameters, component values and stresses are calculated according to the design process outlined in Fig. 3-3.

6.2.1 Calculation of design parameters

Before designing the converter components a set of design parameters must be calculated in the simplified model, with the most important being the voltage transfer ratio from Eq. 3-18,

$$k_{tr,\min} = \frac{15V}{20V} = 0.75 . \qquad 6\text{-}1$$

At first glance, the SFB CSEB seems to not be a viable option because $k_{tr} > 1/\sqrt{2}$, which implies bidirectional current flow through each bridge. However, this is actually not true because of the presence of R_S, which adds losses and increases the dc branch current to supply those losses, without increasing the ac branch current.

To reestablish the limits of k_{tr}, the converter is no longer assumed 100% efficient; rather, the conservation of energy equation becomes:

$$\frac{V_{dc}I_{dc}}{n_{br}} = \frac{V_{ac}I_{ac}}{2}\cos\left(\varphi_{ac}\right) + \frac{n_s {V_S}^2}{R_S}, \qquad 6\text{-}2$$

which leads to a more accurate relationship between I_{ac} and I_{dc}, which then gives alternative limits on k_{tr} for the SFB,

$$k_{tr} \le \left(\frac{V_{dc}I_{dc}}{V_{dc}I_{dc} - n_s n_{br} {V_S}^2 / R_S}\right)\frac{\cos\left(\varphi_{ac}\right)}{\sqrt{2}}. \qquad 6\text{-}3$$

This relationship can be used in an iterative fashion to determine the actual limits on k_{tr}, using reasonable assumptions for the variables throughout the design process. At this stage, knowing that k_{tr} is only slightly greater than the limit of 0.71 is satisfactory.

Assuming a total nominal energy storage capacitor voltage $V_{S,dc,tot}$ of

$$V_{S,dc,tot} = 90V \qquad 6\text{-}4$$

results in a modulation index (using Eq. 3-17) of

$$M = \frac{15V}{90}\left(1 + \frac{\sqrt{2}}{0.75}\right) = 0.48, \qquad 6\text{-}5$$

which is less than the M = 0.9 target used throughout Chapter 3 but advantageously provides ample room for variation of design parameters in this exploratory BoBC. With $V_{S,dc,tot}$ defined, V_S is also known.

$$V_S = 30V \qquad 6\text{-}6$$

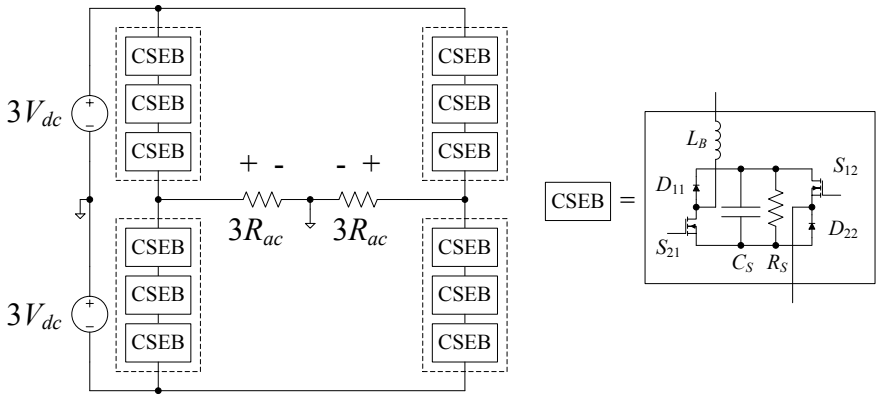


Fig. 6-1. Topology of converter under investigation, showing DC→AC with single ac phase split across two grounded load resistors.

Using a custom Q-cell design, values of n_s and n_p are taken as

$$n_s = 3 \qquad 6\text{-}7$$

$$n_p = 1 \qquad 6\text{-}8$$

to permit the use of low voltage MOSFETs for realizing high switching frequencies. For example, automotive devices with nominal 60V rating are often available in large quantities. The resulting converter topology is shown in Fig. 6-1.

6.2.2 Capacitor design

The base current is calculated from Eq. 3-30 in Section 3.2.3.1,

$$I_{base} = 1.75 \text{ A.} \qquad 6\text{-}9$$

From Fig. 3-5, the normalized rms and peak capacitor currents, as well as the peak capacitor charge are determined. The capacitor current is linearly related to M, therefore the capacitor current calculations using nomograms based on $M = 0.9$ may be adapted for $M = 0.48$ using a multiplicative factor of (0.48/0.9).

$$i_{Cs,rms,norm} = 0.3*(0.48/0.9) = 0.2 \quad 6\text{-}10$$

$$i_{Cs,peak,norm} = 0.6*(0.48/0.9) = 0.32 \quad 6\text{-}11$$

resulting in physical capacitor design values of

$$i_{Cs,rms} = 0.35 \text{ A} \quad 6\text{-}12$$

$$i_{Cs,peak} = 0.56 \text{ A} \quad 6\text{-}13$$

6.2.3 Switch design

Average currents for the SFB devices S_{21}, D_{11}, S_{12} and D_{22} as illustrated in Fig. 6-1 are found using Fig. 3-13 through Fig. 3-16, resulting in

$$i_{S12} = i_{S21} = 0.5 \cdot 1.75 = 0.88 \text{ A} \quad 6\text{-}14$$

$$i_{D11} = i_{D22} = 0.5 \cdot 1.75 = 0.88 \text{ A}. \quad 6\text{-}15$$

The rms switch currents are also found from Fig. 8-7 in the Appendix:

$$i_{S12,\text{rms}} = i_{S21,\text{rms}} = 0.64 \cdot 1.75 = 1.12 \text{ A} \quad 6\text{-}16$$

6.3 Hardware description

A significant portion of this work was dedicated to the design, implementation, construction and testing of a hardware BoBC. This hardware platform comprised a number of digitally controlled CSEBs, a digital Converter Controller, a communications platform, and a hardware protection system.

The BoBC used in this research is differentiated from other BoBC implementations seen in the literature in two significant ways. First, each CSEB contains its own intelligence to acquire sensing data and generate gate signals, making it capable of

distributed control. This stands in contrast to other implementations, which rely on a centralized controller to provide gate signal generation to a potentially large number of CSEBs. While the BoBC used in this research does use a centralized Converter Controller, in this work its primary use was as a communications platform to interface the commanding PC (via USB) to the CAN bus.

The second differentiating aspect of this BoBC implementation is the use of locally-generated housekeeping power for the intelligence on each CSEB, derived from V_S. This feature increases scalability of the BoBC, as it eliminates the need for ancillary power supplies with high voltage isolation capability. Since the BoBC scales into the hundreds of MW or higher, integrating these housekeeping power supplies into each CSEB represents a savings of potentially hundreds of units (or greater), increasing reliability and reducing cost.

Additional details of each BoBC component are given in the following subsections.

6.3.1 CSEB design

At its most basic level, the CSEB is a simple power electronics bridge circuit as has been presented in this dissertation. However, realizing this basic behavior as a component of a larger power electronics device requires incorporating a great deal of additional functionality into each CSEB to ensure that it can operate safely, predictably and consistently as a collective converter. These added functions introduce a need for

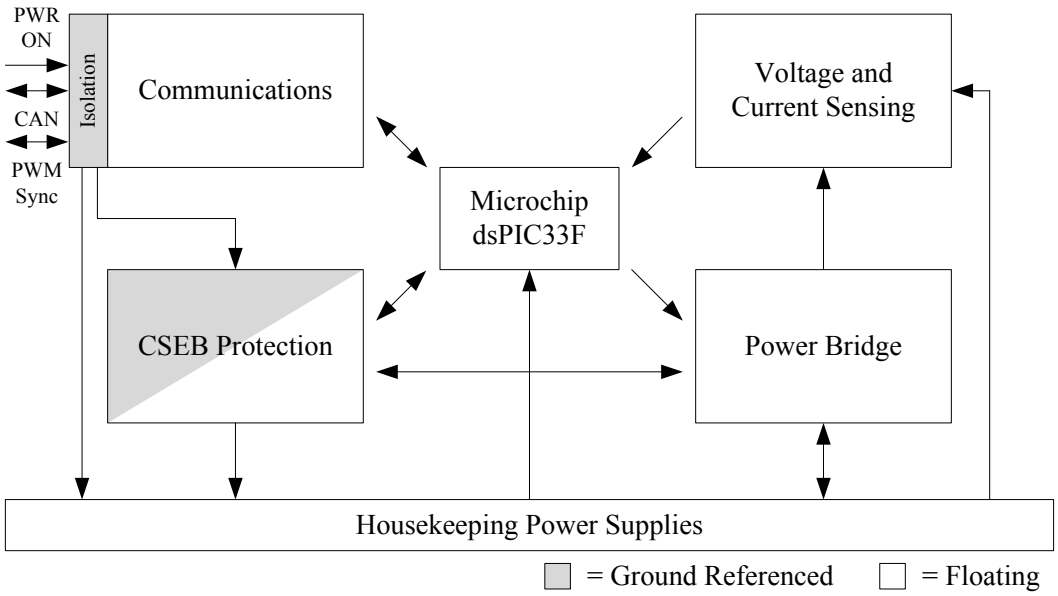


Fig. 6-2. CSEB functional block diagram of experimental BoBC.

computational intelligence on each CSEB beyond the level typically required of a relatively simple power bridge circuit. A block diagram of the implemented CSEB functionality is shown in Fig. 6-2. Figs. 6-3 and 6-4 show the top and bottom of a populated CSEB PCB, respectively.

At the heart of each CSEB is a 64-pin, 50 MIPS Microchip dsPIC33FJ64GS606 microcontroller with integrated CAN controller, high speed PWM controller (resolution down to 1.04ns), 10-bit ADCs, and some 5V-tolerant pins. The logic of each CSEB is referenced to the negative terminal of the bulk energy storage capacitor V_S within the power bridge. Therefore, the communications bus must provide isolation between the CSEB logic reference and the communications bus reference, which is chosen as ground.

6.3.2 Communications Platform

As mentioned above, the communications platform includes two buses. The first is a Controller Area Network (CAN) bus to facilitate communication across CSEBs, and the second is a PWM synchronization bus to maintain one unified PWM counter across all CSEBs within the converter.

CAN was chosen for its relatively high bandwidth of 1 Mbps, inherent support for message arbitration, and resistance to electromagnetic interference (EMI). While no bandwidth requirement was formally established for this converter, it was realized that a bandwidth of at least several hundred kbps could be useful for control and/or data signals between bridges. Even with this bandwidth, having a relatively high number of bridges (12) all communicating on the same bus, and all potentially turning on and sending "hello" messages at exactly the same time would quickly saturate the CAN bus. Therefore, assigning priorities to the messages was attractive. Each message frame includes a Standard Identifier (SID) in addition to 0-8 bytes of data payload. At the physical level, bits are represented as dominant (0) and recessive (1), where the bus data lines are naturally at 1 but each CAN node (CSEB) can pull the bus to 0. Therefore, by comparing the actual bus state with the intended state while sending messages, any node can immediately detect if a higher priority message is being sent by another node. In this situation the overridden node stops trying to send, waits, and retries until it succeeds.

Finally, the physical CAN bus is differential, with CANH and CANL data lines. This ensures that any common mode voltage induced into the data lines from an EMI source,

e.g. the converter's high frequency switching, does not interfere with the CAN messages themselves.

While a great deal of programming effort throughout the world has produced a number of CAN messaging standards, each with its own set of strengths and weaknesses, some open source and some proprietary, none of these standards was adopted for the hardware. Instead, a low-level set of messages was developed based on the unique needs of the hardware converter. This set of messages is shown in Table 6-3.

Each CSEB has send/receive capabilities on the PWM synchronization bus and may be programmed to use either function depending on its location within the converter, using an identifier set by its DIP switch.

Each CSEB must protect itself from overvoltage (OV), undervoltage (UV), overcurrent (OC), and other types of faults, because the CSEBs themselves are not in complete control of their terminal currents; other bridges and converter terminal behavior both impact the terminal current of a given CSEB. Furthermore, the protection function must also be maintained throughout a communications bus failure, so the CAN bus itself cannot be completely relied upon for this function. One illustrative example is a CSEB that incurs a CAN communications failure while the converter is in operation. When the fault occurs, even if the CSEB detects the fault, it can't send a message to the bus to halt

the converter[3]. Since the converter is in operation, significant dc current flows through the CSEB terminals. Leaving the CSEB uncontrolled in this circumstance will cause the dc current to flow through the diodes, charging up the capacitor C_S, and leading to overvoltage damage to CSEB components. The protection functions are discussed in more detail in Section 0.

The CSEB circuits provide voltage and current sensing functionality, both for enabling closed loop V_S and/or I_B control if desired, and for providing CSEB self-diagnostic capabilities to ensure all voltage buses have an appropriate voltage.

The power bridge function represents the core of this thesis and includes the energy storage capacitor C_S, bridge inductor L_B, and gate drives. The components may be selectively populated to represent the 3 basic CSEB types: Full Bridge, Semi-Full Bridge, or Half Bridge.

Enabling all of these functions are the housekeeping power supplies. These supplies provide power at 12V, 5V and 3.3V for the various functional blocks, plus isolated 12V power for the high side gate drivers in the power bridge. All of these voltage rails are derived from V_S and can be enabled two ways. First, a 5V PWR_ON signal on the CAN bus will turn on all housekeeping supplies. Second, as an OV protection function, if V_S

---

[3] In theory the other CAN nodes should detect such a communications fault but there is no guarantee without a comprehensively designed and implemented CAN communications protocol, which is beyond the scope of this work.

Table 6-3. CAN messages used in hardware.

Type	SID	data[0]	data[1]	data[2]	data[3]	Description
Info	0x200	0	x	x	x	Request for bridges to say hello
Info	0x200	1	x	x	x	ADC voltage data request
Cmd	0x80	[ID] [1]	x	x	x	Decrease DC conduction period
Cmd	0x80	[ID] [2]	x	x	x	Increase DC conduction period
Cmd	0x80	3	x	x	x	Fault reset
Cmd	0x80	4	db_dc low	db_dc high	x	Set dc duty ratio
Cmd	0x80	5	db_ac low	db_ac high	x	Set ac duty ratio
Cmd	0x80	6	ID#	x	x	Trip relay on ID# board
Cmd	0x80	7	ac_period	db_ac step size	x	AC angle reset
Cmd	0x80	8	x	x	x	Increment AC duty ratio
Cmd	0x80	9	x	x	x	Decrement AC duty ratio
Fault	0x100	x	x	x	x	Fault mode (send to all bridges)
Fault	0x100	[ID] [1]	x	x	x	OV fault (report from a bridge)
Fault	0x100	[ID] [2]	x	x	x	OC fault (report from a bridge)
Fault	0x100	[ID] [3]	x	x	x	Comm fault (report from a bridge)
Fault	0x100	[ID] [4]	x	x	x	UV fault (report from a bridge)
Data	0x300	[ID] [0]	x	x	x	Hello

[ID] = [0 0 ID5 ID4 ID3 ID2 ID1 ID0]

x = Don’t care

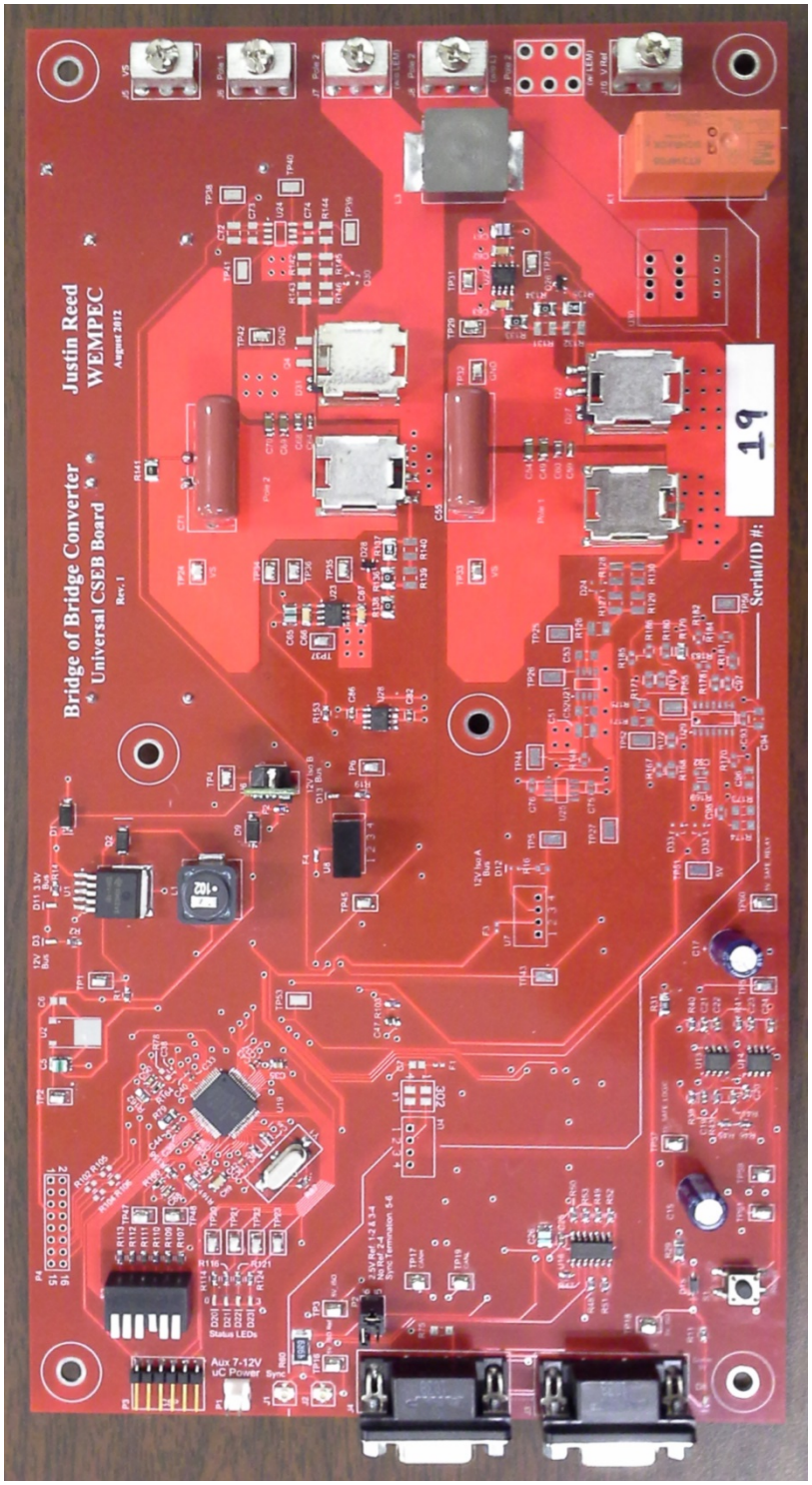


Fig. 6-3. Top of populated CSEB PCB.

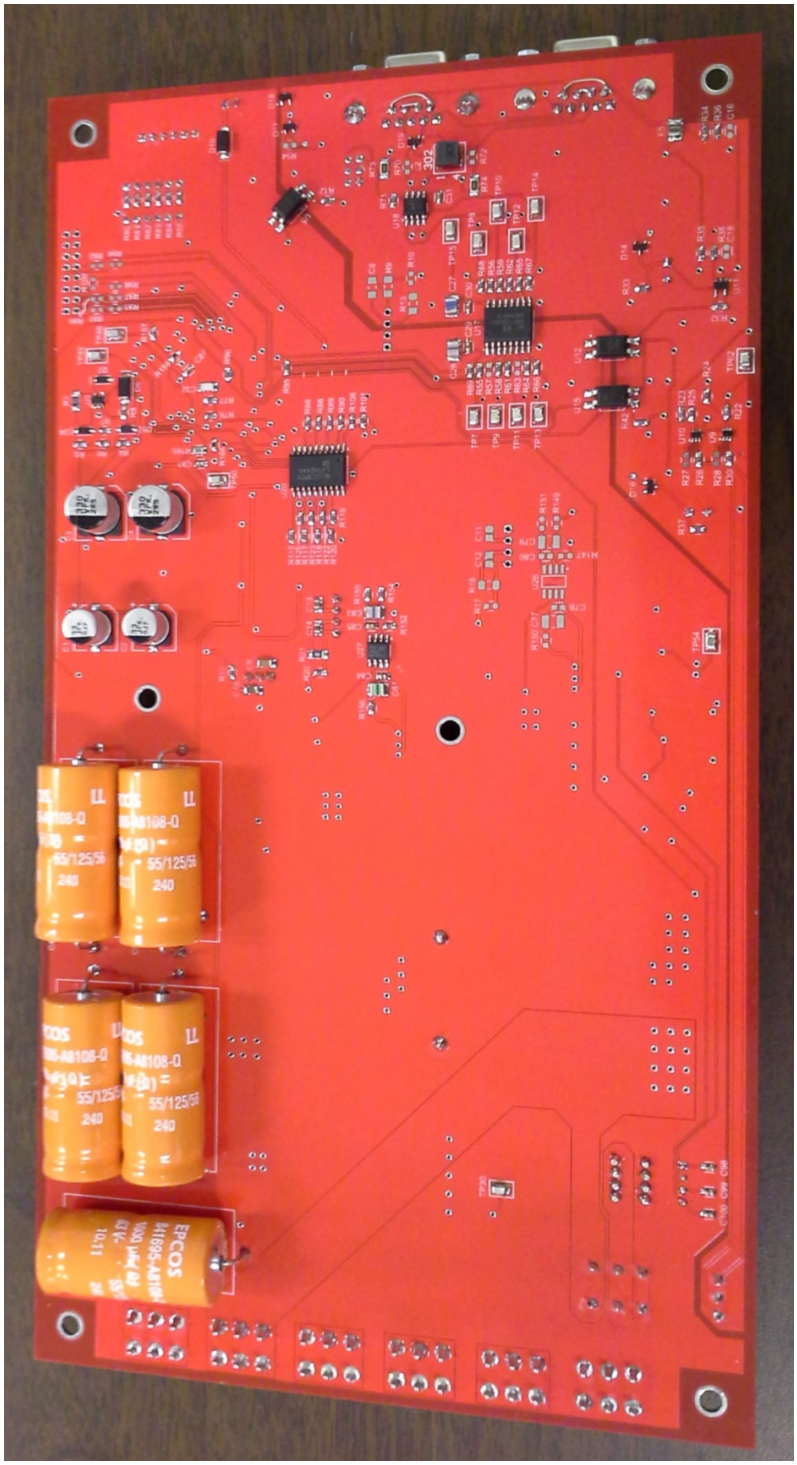


Fig. 6-4. Bottom of populated CSEB PCB.

exceeds ~55V, the housekeeping supplies will automatically turn on so that the CSEB can assess its situation and protect itself from damage.

Finally, though not included explicitly in the diagram, each CSEB also contains 4 LEDs with testpoints for debugging purposes and a header for customized expansion capabilities using UART or SPI functions.

6.3.3 CSEB protection

As mentioned above, each CSEB contains its own circuitry to protect it in case of a hardware or software failure. The presence of a CAN communications bus can greatly simplify the protection functionality, since any CSEB can announce a fault to the others and the entire converter can effectively shut down very quickly. However, a fault in the communications bus itself is a real possibility, and presents particular challenges. Therefore, hardware functionality is also provided to protect each CSEB from damage in case of specific failure modes including communications bus failure.

Should the communications bus fail, caused by an overvoltage or overcurrent of a CSEB's local 5V communications power bus, that power bus voltage will then collapse. This condition is detected and a signal is sent to the microcontroller through an optoisolator so that any PWM switching can be disabled. Simultaneously, two 555 timers add a delay before latching a relay closed that is attached to the two CSEB power terminals; this is very important, since any use of switches while the power terminals are shorted out will short circuit V_S through the relay. Functionality is also included to allow

the microcontroller to latch its own relay closed if it deems it necessary. With the CSEB effectively removed from the converter, V_S cannot increase and any remaining voltage on the CSEB will dissipate through a bleed resistor.

Two possible scenarios exist for overvoltage of V_S. The first is that a firmware malfunction within a CSEB causes an overvoltage during converter operation, either during proper operation, during a fault, or other condition. In this scenario, the V_S signal is compared against a reference value set in firmware of approximately 50V, and if this limit is exceeded, a comparator internal to the microcontroller (U19) will flag a PWM fault. This fault flag will immediately halt all PWM and cause the power switches to enter a "zero voltage" state, wherein the capacitor C_S can only discharge through R_S.

The second possible scenario for overvoltage of V_S is that the overvoltage occurs while the CSEB housekeeping power is turned off. This can happen, for example, if branch current is flowing but a CSEB within that branch loses its communications bus, causing V_S to rise uncontrollably. Should this happen, a hardware circuit based around comparator U3 will detect $V_S > 55$V and force the housekeeping power to turn on. During startup, the CSEB firmware will then detect the overvoltage condition and automatically enter into a "zero voltage" state. In both scenarios the CSEB will signal the fault state with LEDs and attempt to send fault messages over CAN.

Another possible failure mode is undervoltage (UV) of V_S, wherein $V_S < 12$V. This condition causes the gate driver supply voltages to also incur an undervoltage condition, and therefore the MOSFETs can enter into their linear conduction mode, incur significant

losses, and fail prematurely. Though uncommon, this failure has occurred during testing of the prototype hardware. Should V_S fall below 10V while the housekeeping power is turned on, the microcontroller will immediately halt all PWM, enter into a fault mode and announce the fault mode over CAN.

The final failure mode is overcurrent of the CSEB. Not all CSEBs are populated with current sensors, and therefore not all are suited to detect an overcurrent condition. Therefore, any CSEB with a current sensor that detects an overcurrent condition will enter into a fault mode and then send a CAN message indicating the fault and signal the fault with LEDs. All other CSEBs will receive the message and enter their own fault mode. In contrast to the OV failure mode where the CSEB terminals are essentially short-circuited to prevent C_S from charging, in OC mode the switches impress full positive V_S on the CSEB terminals, causing a negative di_B/dt and therefore bringing i_B to zero.

The microcontrollers' PWM modules contain two different fault modes: a general fault mode and an overcurrent fault mode, which are very flexible and may be entered through a variety of means. On any given CSEB, the aforementioned sources can cause a fault: local overvoltage (OV), local overcurrent (OC), local undervoltage (UV) of 12V bus, the reception of a CAN fault message from the Converter Controller, reception of OC, OV, or UV fault messages over CAN from other CSEBs, and a fault on a CSEB's local communications power bus. Finally, the microcontroller of each CSEB can cause the local relay to latch closed if needed, although this functionality was not realized in firmware. Fig. 6-5 shows how four fault-related pins on the microcontroller are utilized

in order to realize the necessary fault protection. Note that whenever one PWM channel's Interrupt Service Routine (ISR) runs due to a fault, another fault is deliberately generated on the other channel to force all PWM switches into the proper states.

6.3.1 Converter hardware structure

At a higher level, the CSEBs form the collective converter, the interconnection of which is shown in Fig. 6-8. A PC communicates with the Converter Controller over a standard USB connection (using either a text-based terminal for manual operation or a custom interface for automated operation, e.g. MATLAB). At a minimum, the Converter Controller functions as an interface between the USB interface and the CAN bus. The Converter Controller also provides the 5V PWR_ON signal to the CSEBs through the CAN bus to enable the housekeeping supplies and turn the converter on. All communications buses – CAN, USB and PWM synchronization – are ground-referenced. Note that the PWM synchronization does not involve the Converter Controller. As mentioned above, each CSEB has send/receive capabilities on this bus and may be programmed to use either function depending on its location (DIP switch identifier) within the converter.

A photo of the overall converter, including CSEBs and Converter Controller, is shown in Fig. 6-9.

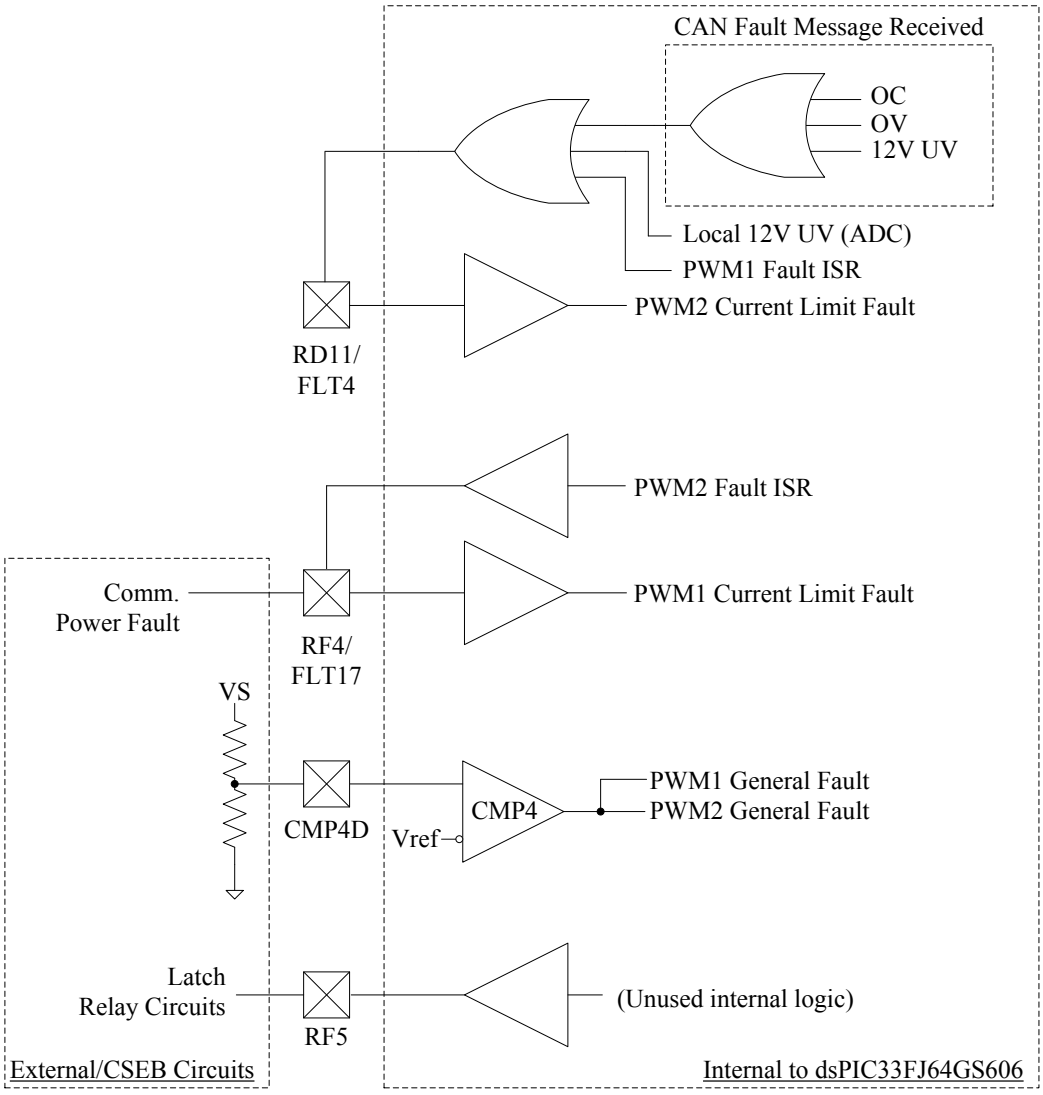


Fig. 6-5. Assignment of fault pins of CSEB microcontroller.

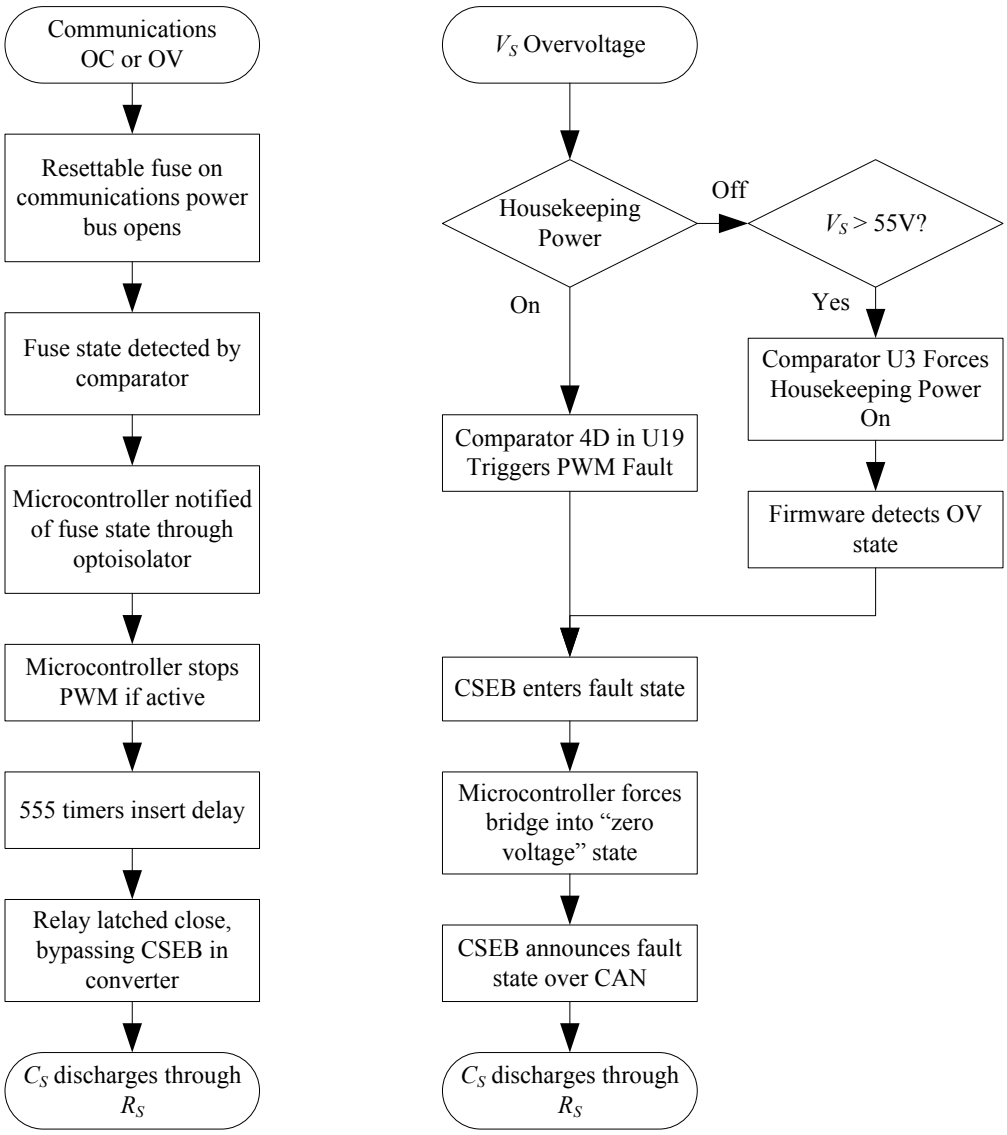


Fig. 6-6. High level interconnection structure of BoBC highlighting communications

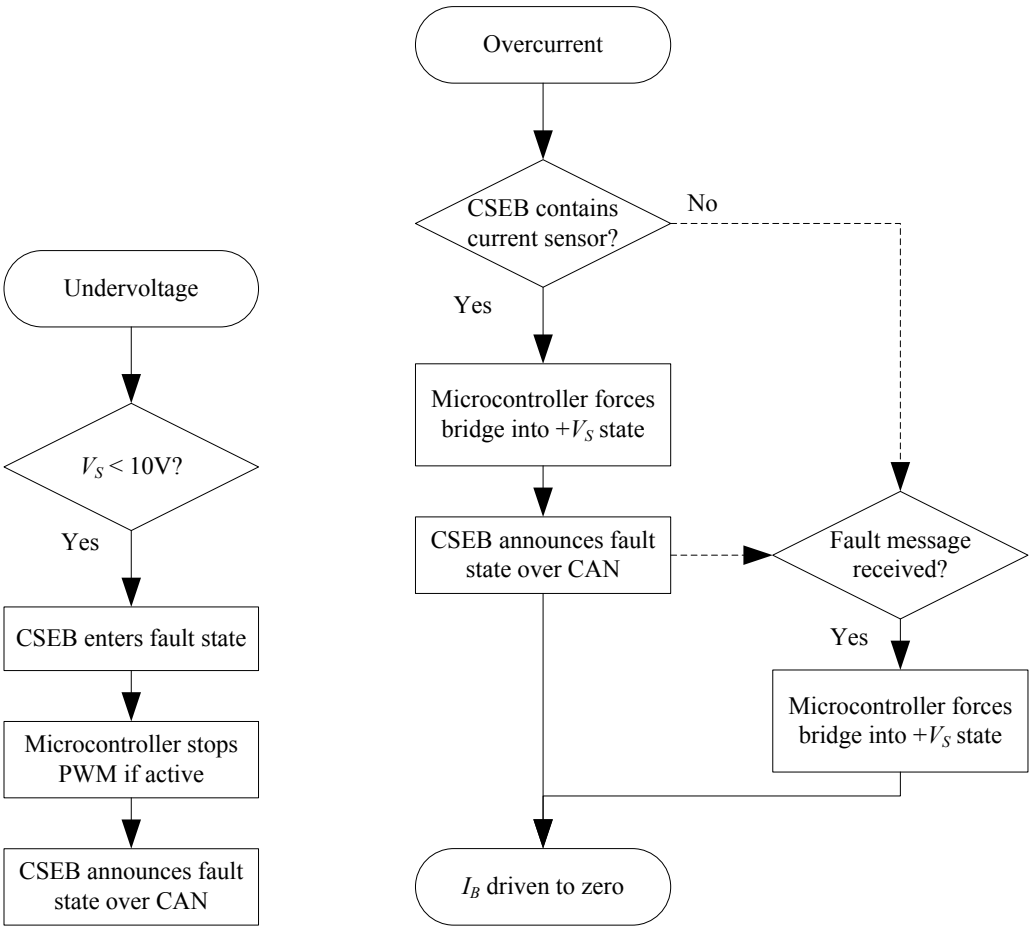


Fig. 6-7. High level interconnection structure of BoBC highlighting communications

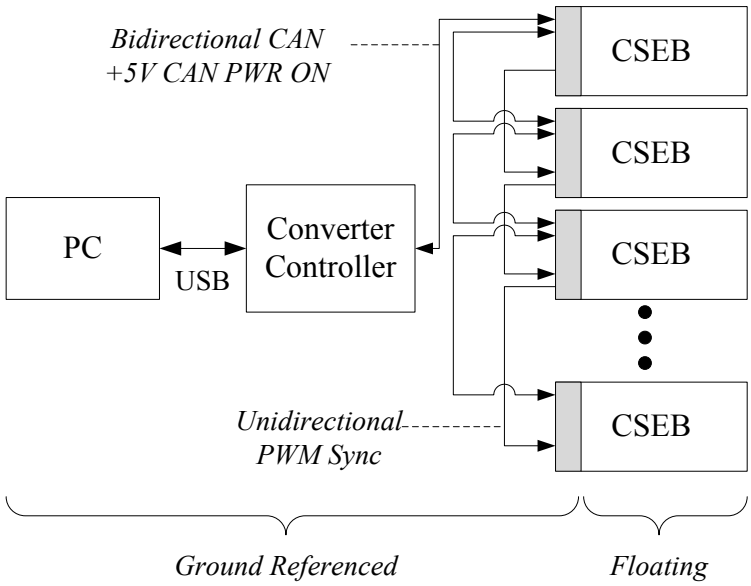


Fig. 6-8. High level interconnection structure of BoBC highlighting communications capabilities.

6.3.1 Converter controller design

The Converter Controller may also be used for data acquisition, providing closed-loop control of terminal voltages and/or currents, additional communications (CAN, Ethernet, etc.), manual converter interfacing using pushbuttons, providing user feedback through LEDs, data storage on SD cards, ac and dc contactor interfacing, and encoder interfacing. These functions were not utilized during the experimental phase of this work but their capabilities exist in the Converter Controller hardware design.

At the heart of the Converter Controller is a Texas Instruments F28M35 Concerto dual core microcontroller, mounted on a TI controlCARD for modularity, which connects

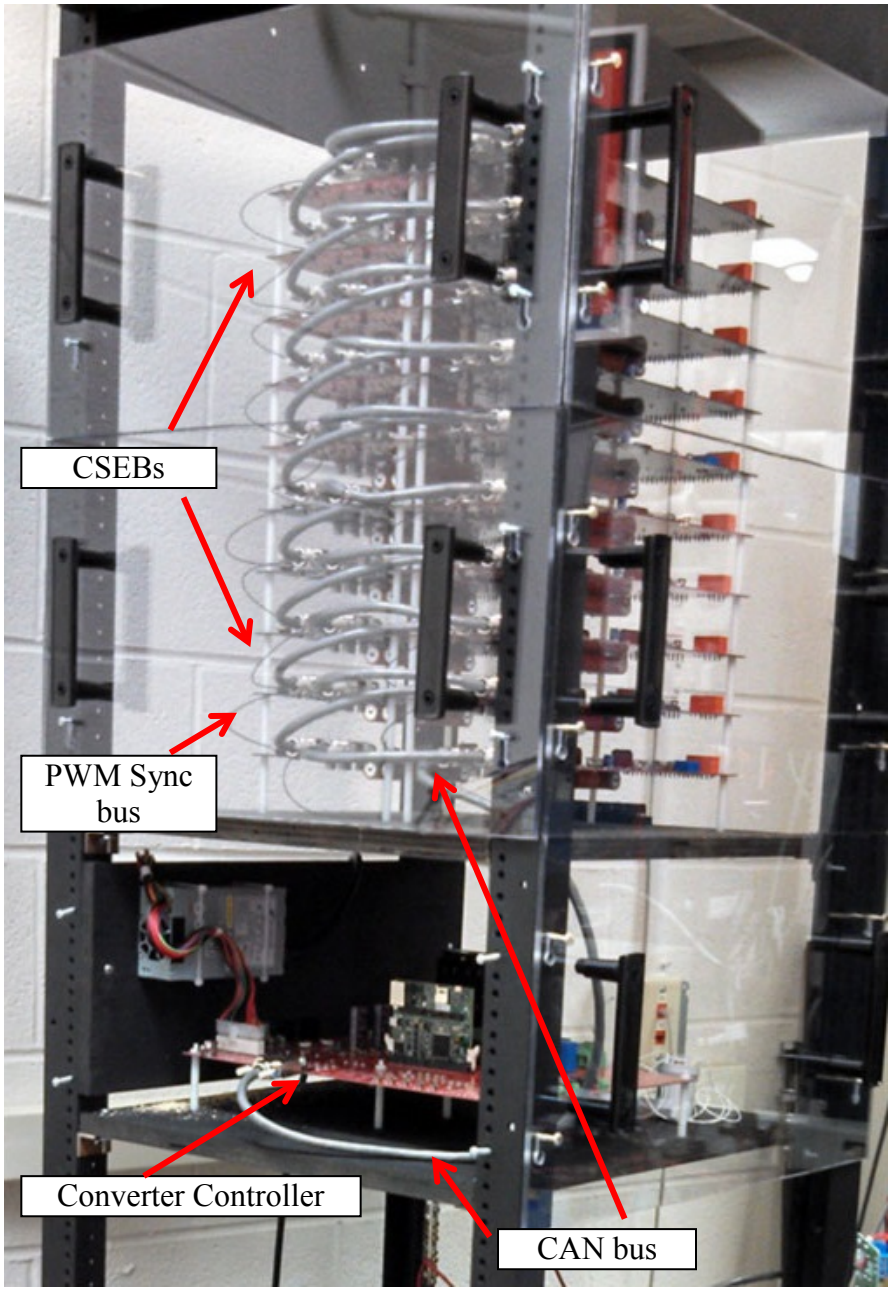


Fig. 6-9. Hardware implementation of BoBC, showing high level interconnection.

to the Converter Controller PCB through a 100-pin DIMM connector. The microcontroller contains ARM Cortex M3 and TMS320C28 cores, with Interprocessor Communications (IPC) shared RAM, as shown in Fig. 6-10. Although both cores share the same pins, the M3 is the master and starts up at power-on while holding the C28 in reset, then starts the C28 and grants access to any pins as needed by the C28 programming. The F28M35 is a complex device and the reader is directed to the TI reference literature for more information.

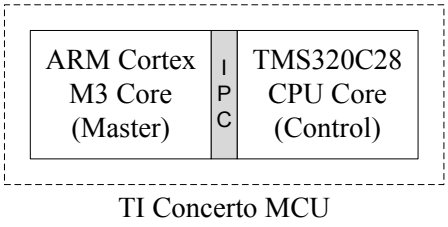


Fig. 6-10. TI F28M35 Concerto microcontroller structure.

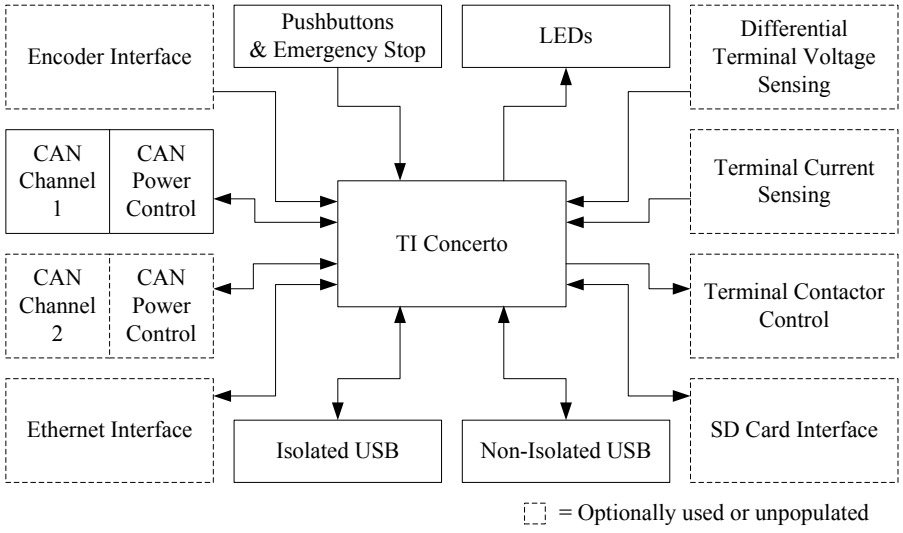


Fig. 6-11. Converter Controller functional block diagram of experimental BoBC.

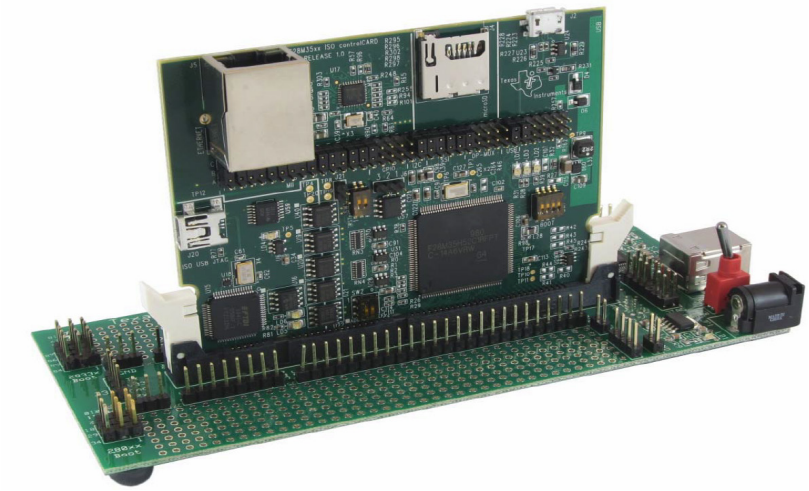


Fig. 6-12. Texas Instruments Concerto F28M35 controlCARD, seated in an evaluation board[4]. Normally the controlCARD is seated in the Converter Controller board to provide full control over the BoBC components and communications platform.

6.4 Branch-level simulation platform

The averaged circuit of a single branch was modeled in MATLAB/Simulink version 2011a using the PLECS Blockset version 3.2.7. The model is shown in Fig. 6-14 and Fig. 6-15. An initialization script was also utilized for convenient adjustment of circuit parameters, which is shown in Appendix C. While the goal of the simulation is to analyze and validate the model of a single branch, in fact two branches are included, arranged in a half bridge configuration. This allows for cancelation of dc current components at the ac resistive output of the two branches.

[4] See F28M35xx Info Sheet, June 13th 2012. Image copyright 2012 Texas Instruments.

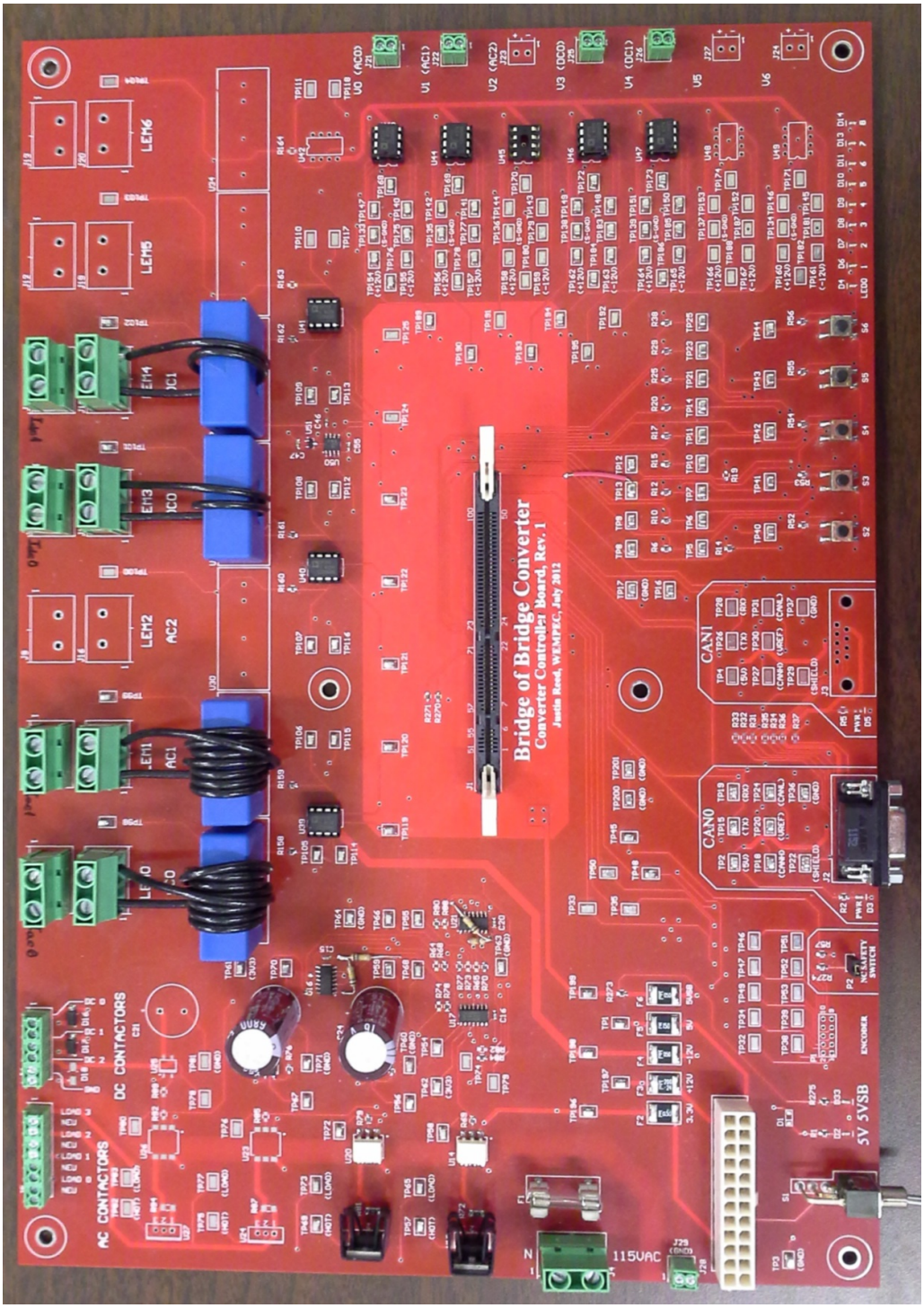


Fig. 6-13. Populated Converter Controller PCB.

Note also that the simulations represent the actual physical circuit with scalar quantities, independent of any dynamic phasor models presented elsewhere in this dissertation. Therefore, any nonlinearities or other non-ideal BoBC behavior will be represented in these averaged model simulation waveforms.

The Simulink model can be used in open loop or closed loop by varying SHOTS controller gain R_a. The model includes a ramp function for the dc duty ratio, which can be used to gradually establish a steady state operating point. The duty ratio and current reference blocks contain the following functions:

```
function [dB1,dB2] = Duty(params, theta)
    dB_dc = params(1);
    dB_ac = params(2);
    dB1 = dB_dc - sqrt(2)*dB_ac*cos(theta);
    dB2 = -dB_dc - sqrt(2)*dB_ac*cos(theta);
end
```

```
function [Idc,Iac] = Ib(params, theta)
    I_base = params(1);
    k_tr = params(2);
    pf_angle = params(3);
    Idc = I_base;
    Iac = I_base*k_tr*sqrt(2)/cos(pf_angle)*cos(theta-pf_angle);
end
```

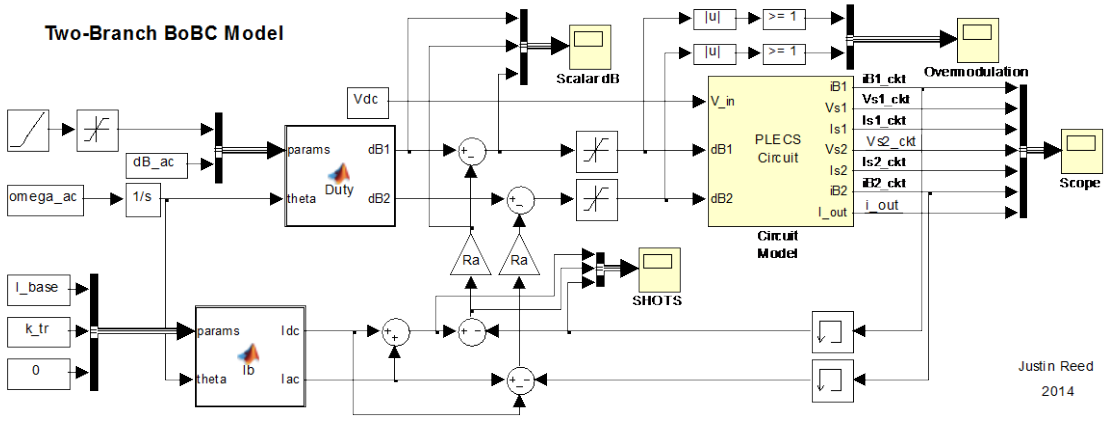


Fig. 6-14. Simulink model of single BoBC branch, containing PLECS circuit model.

6.5 Verification of models

6.5.1 Semi-full bridge topology

The SFB was proposed in Chapter 3 as being a full bridge CSEB limited to unidirectional current flow, but capable of bidirectional voltage waveforms at its terminals. Experimental results at the dc operating point in Table 6-4 confirm the predicted behavior. Zero states are not implemented, therefore both switches on each bridge utilize the same duty ratio and gate signal. Gate signals are series interleaved across bridges. The bridge duty ratio $d_{B,ac}$ is calculated from the switch duty ratios d_1 and d_2 using Eqs. 3-41 and 3-42.

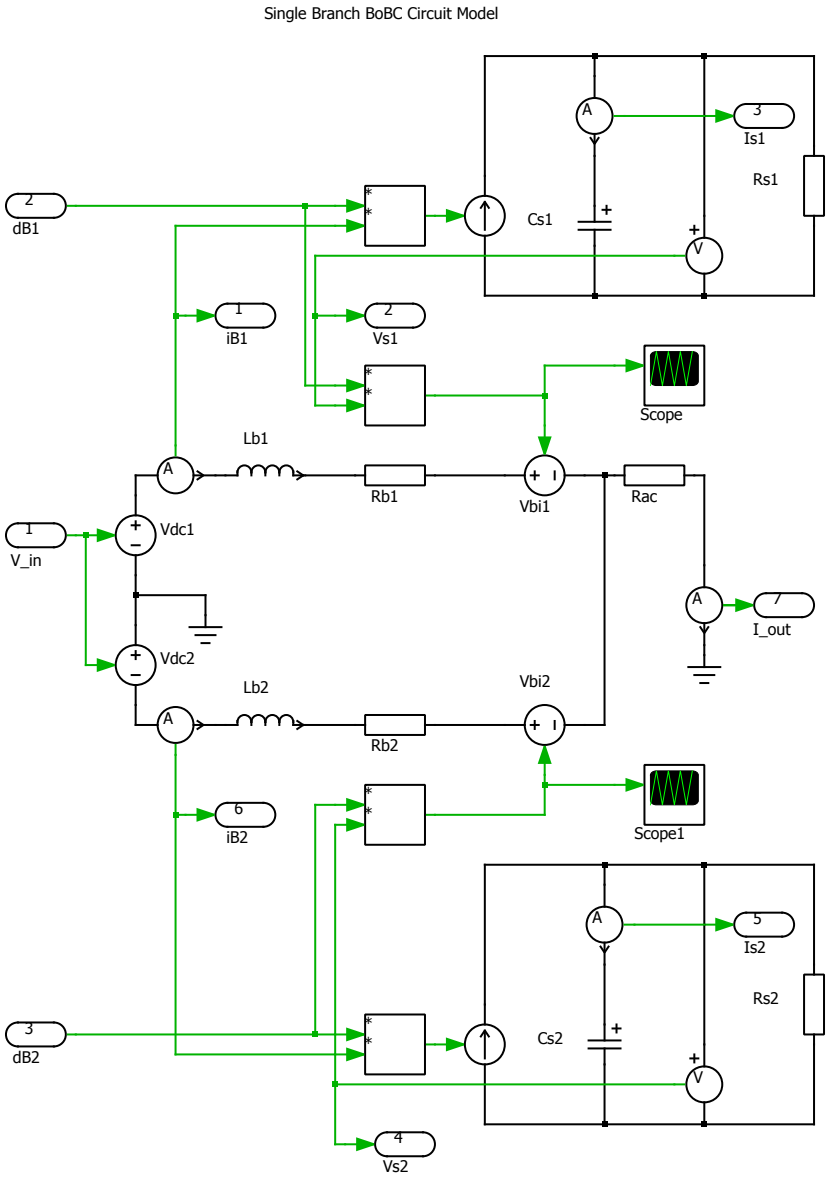


Fig. 6-15. PLECS nonlinear circuit model within Simulink branch model.

Table 6-4. DC operating point for validation of SFB BVUC characteristics.

$n_s V_{dc}$	$d_{B,dc}$	d_1, d_2	V_S	n_S	$n_s F_S$	$n_s L_B$	R_S
15 V	16.8%	57.9%	~30 V	3	300 kHz	66 µH	750 Ω

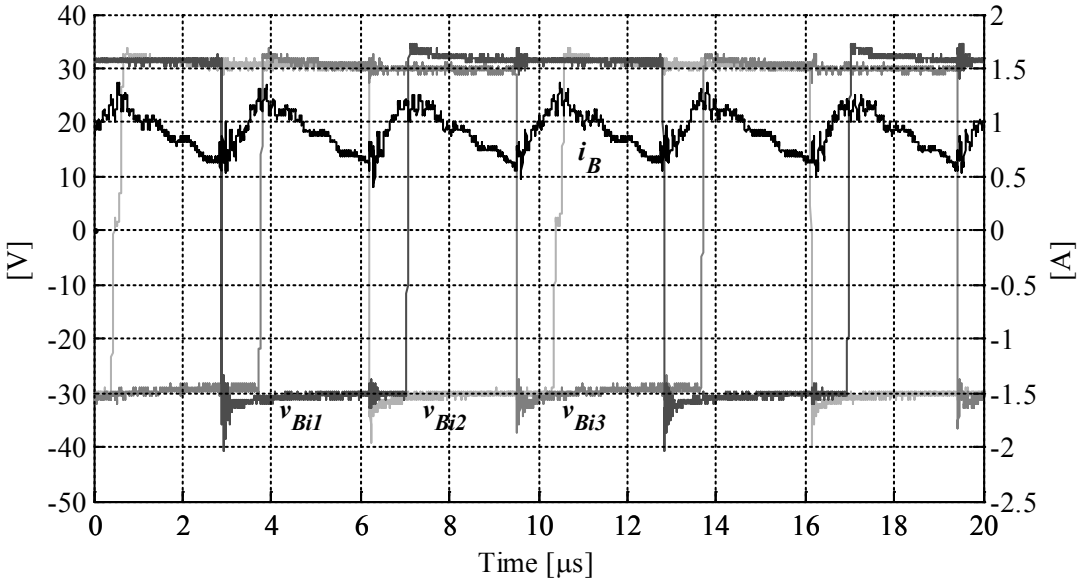


Fig. 6-16. Experimental SFB waveforms showing bidirectional internal bridge voltages v_{Bi} and unidirectional branch current i_B for the operating point in Table 6-4.

6.5.2 Capacitor sizing

In order to validate the capacitor sizing equations from Section 3.2.3.1, the significance of SHOTS control on the branch and capacitor currents is first established. Single bridge circuit simulations were implemented using scaled parameters representative of n_s=3, under both open loop (R_a = 0) and closed loop SHOTS control (R_a = 0.005). The operating point is shown in Table 6-5. Frequency components were extracted using the Fast Fourier Transform (FFT) function within the PLECS scope block, and are shown in Fig. 6-17.

The figure shows that implementing SHOTS control essentially eliminates the 120 Hz i_B and 180 Hz v_S components, which are unnecessary and undesirable frequency components, which are not modeled in this work, and therefore can invalidate the proposed capacitor sizing methodology. The methodology, however, is well-founded on reasonable assumptions, namely that i_B should contain only dc and 60 Hz components, since power transfer only occurs at these frequencies and significant harmonic content can increase losses and interfere with acceptable frequency content at the converter ports. SHOTS control closes the loop solely around the branch current; therefore, by eliminating the 120 Hz i_B component, the 180 Hz v_S component is also eliminated.

Quantifying this benefit is Table 6-6, which shows the reduced rms value of both i_B and i_{Cs} as a result of using a SHOTS controller. The % reduction in rms current is shown in addition to the "% loss reduction," calculated as the square of the actual reduction and is useful for illustrating how significantly I^2R losses in L_B and C_S can be reduced.

To illustrate the necessity of using SHOTS control for capacitor current sizing, actual waveforms showing the substantial difference between the analytical capacitor current predictions (used in the sizing equations) and the open loop capacitor current are shown in Fig. 6-18.

In light of these results, validating the proposed capacitor sizing methodology clearly requires the use of SHOTS control to mitigate the unwanted capacitor current components.

Table 6-5. Converter simulation and analytical model parameters.

$3V_{dc}$	f_{ac}	$3L_B$	$3R_B$	$3R_{ac}$	$3R_S$	$C_S/3$	$3V_S$	$I_{B,ac,d}$
15 V	60 Hz	66 µH	0.03 Ω	8.2 Ω	2250 Ω	1667 µF	90 V	1.4 A

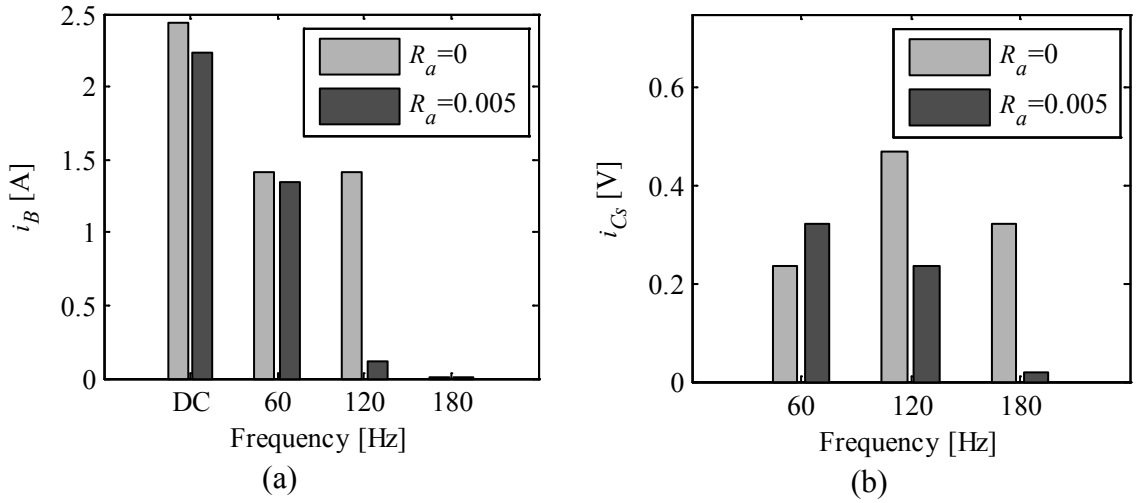


Fig. 6-17. Effect of SHOTS control on (a) i_B and (b) i_{Cs}. Effective elimination of the undesirable 120 Hz i_B and 180 Hz v_S components is observed.

Table 6-6. Reduction in rms currents resulting from use of SHOTS controller.

	$R_a = 0$	$R_a = 0.005$	Reduction	Loss Reduction
$i_{B,rms}$	3.15 A	2.61 A	17.1 %	31.3 %
$i_{Cs,rms}$	0.616 A	0.397 A	35.6 %	58.5 %

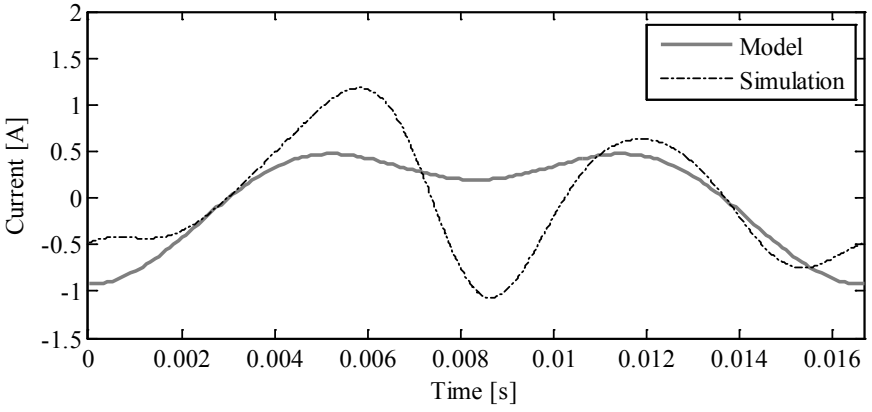


Fig. 6-18. Capacitor current mismatch between analytical predictions and simulation results for operating point in Table 6-5 without using SHOTS controller.

The capacitor current is modeled using Eq. 3-27 across a variety of operating points, resulting in the data points of Table 6-7, and the analytical modeling verification plot of Fig. 6-19. Time domain waveforms of several operating points from Table 6-7 are shown in Fig. 6-20. The k_{tr} parameter is calculated as a ratio of dc and ac duty ratios, and M is

Table 6-7. Capacitor current model verification

$d_{B,dc}$	$d_{B,ac,rms}$	k_{tr}	M	$I_{dc}/2$ [A]	$I_{Cs,rms}$ [A] (model)	$I_{Cs,rms}$ [A] (sim.)
0.157	0.015	10.6	0.18	0.005	0.0085	0.0128
0.157	0.06	2.64	0.24	0.12	0.0463	0.0467
0.157	0.12	1.32	0.33	0.43	0.0621	0.0720
0.157	0.18	0.90	0.41	1.07	0.128	0.1222
0.157	0.24	0.66	0.50	1.87	0.329	0.3104
0.157	0.3	0.53	0.58	2.94	0.716	0.6739

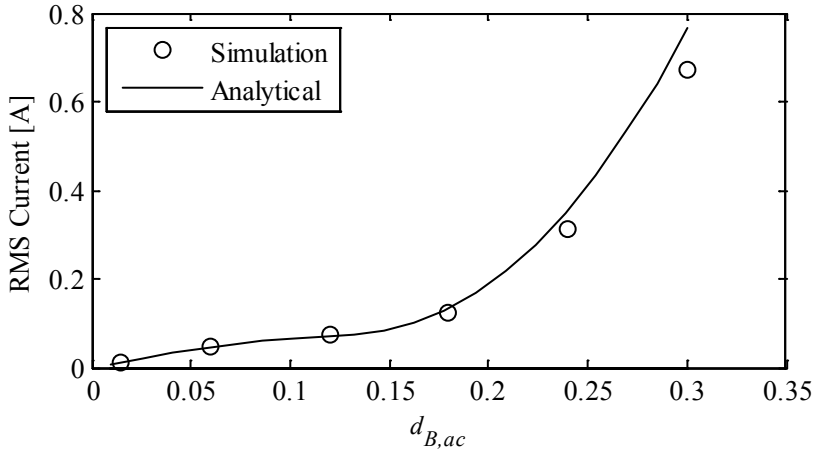


Fig. 6-19. Validation of capacitor current model using simulations.

calculated from k_{tr} and $d_{B,ac}$. The I_{dc} parameter is calculated assuming zero power consumed in the bridges themselves ($R_S = \infty$), therefore a direct calculation of I_{dc} from I_{ac} using $d_{B,ac}$, V_S and k_{tr} is valid.

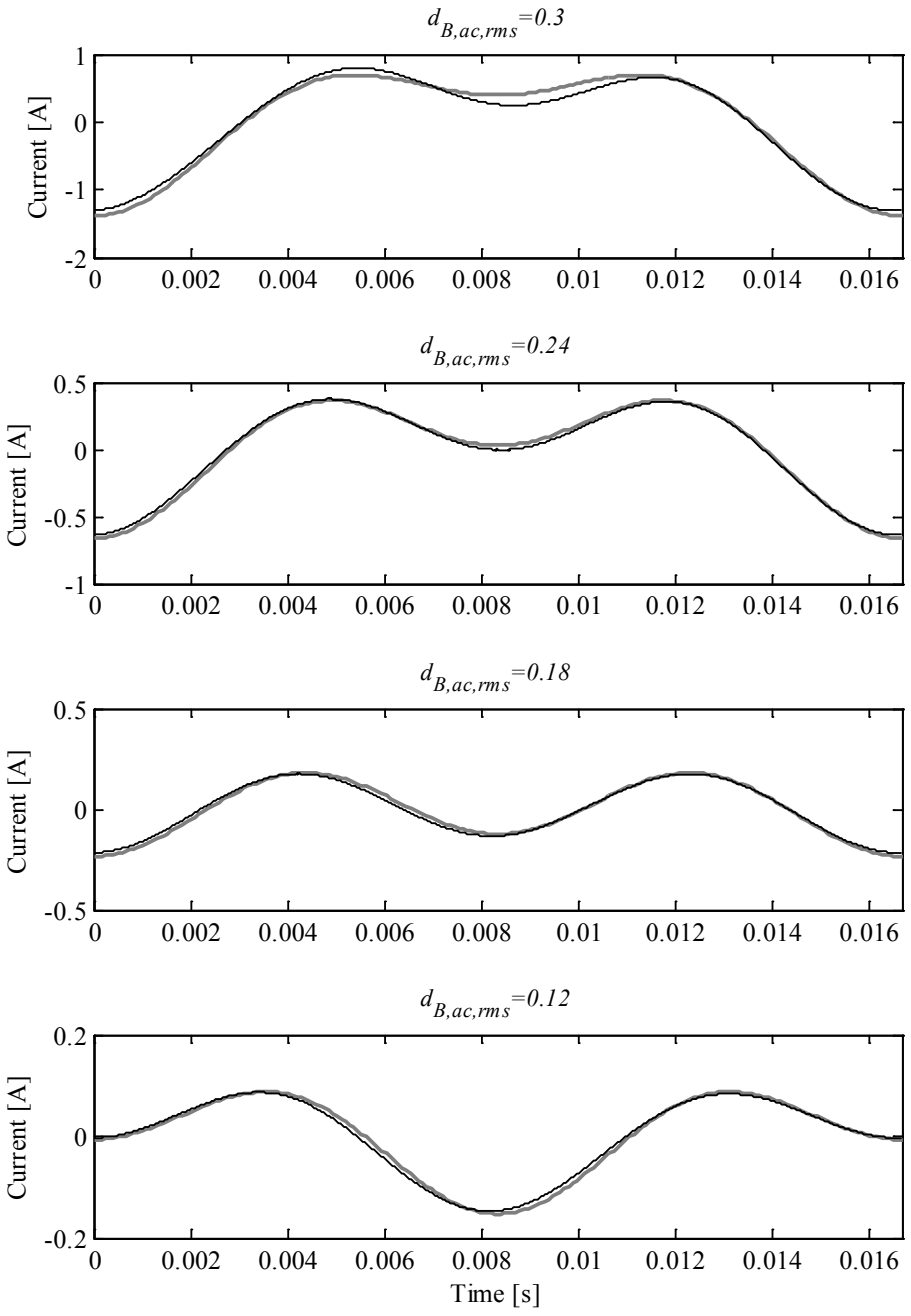


Fig. 6-20. Capacitor current waveforms from circuit simulations (black) and analytical model (gray).

6.5.3 Scalar circuit model

Verification of the relationships between the open loop duty ratios and the capacitor voltage are provided by comparing the analytical model (dc portion of Eq. 3-16) with simulations and experimental results over varying ac duty ratio, using the n_s=3 parameters from Table 6-5. As predicted by the equations, little to no relationship exists, although reduced V_S at high values of $d_{B,ac}$ can be attributed to the voltage drop across R_B. Note that the input voltage, nominally 15V, is reduced to 14.1V for analytical and simulation calculations to compensate for diode forward voltage drops from the dc power supply used in the experimental results.

Table 6-8. Effect of $d_{B,ac}$ on V_S.

			$3V_S$		
$d_{B,dc}$	$d_{B,ac}$	$3V_{dc}$	Analytical	Simulation	Experimental
0.1573	0.000	14.1	89.64	89.66	89.7
0.1573	0.015	14.1	89.64	89.65	89.7
0.1573	0.060	14.1	89.64	89.63	89.8
0.1573	0.120	14.1	89.64	89.58	88.8
0.1573	0.180	14.1	89.64	89.41	86.8
0.1573	0.240	14.1	89.64	88.90	84.1
0.1573	0.300	14.1	89.64	88.29	81.6

6.5.4 Waveforms

Experimental, simulation, and analytical ac output current waveforms are shown in Fig. 6-21 through Fig. 6-23, which represent three ac duty ratio operating points from Table 6-8. All waveforms show excellent correlation with analytical predictions.

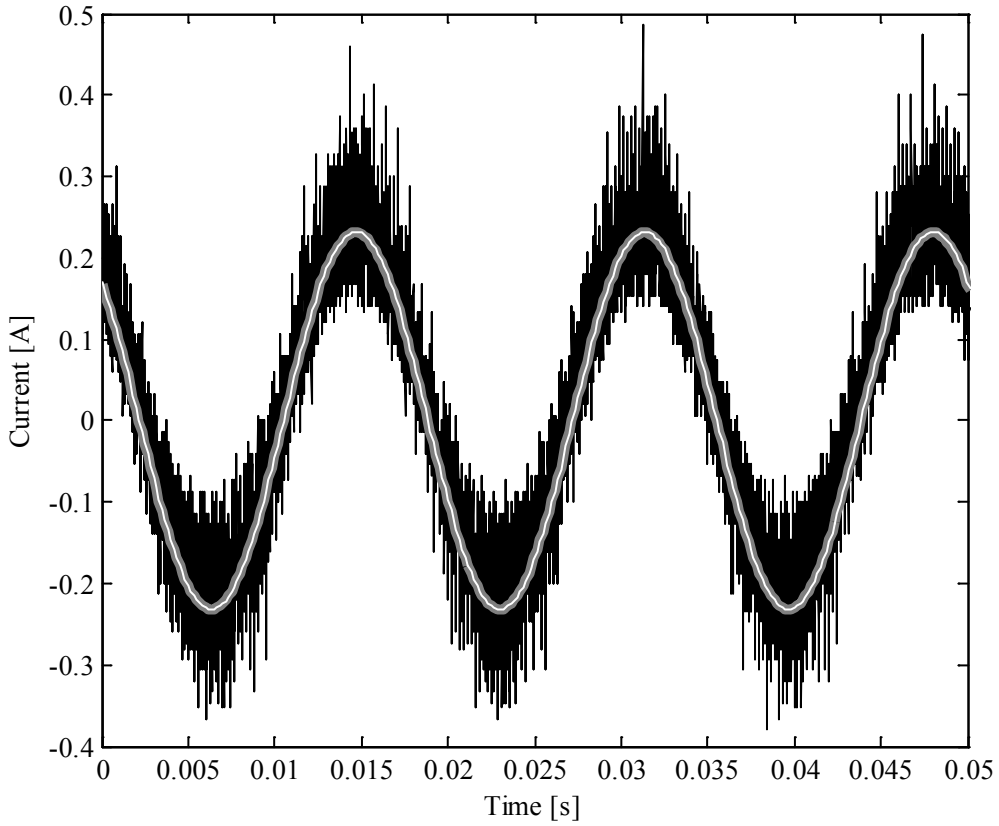


Fig. 6-21. I_{ac} output current waveforms for $d_{B,ac}$ = 0.015 operating point from Table 6-8. Note that the analytical waveform is the thin white line directly on top of the thick gray line, denoting the simulation waveform.

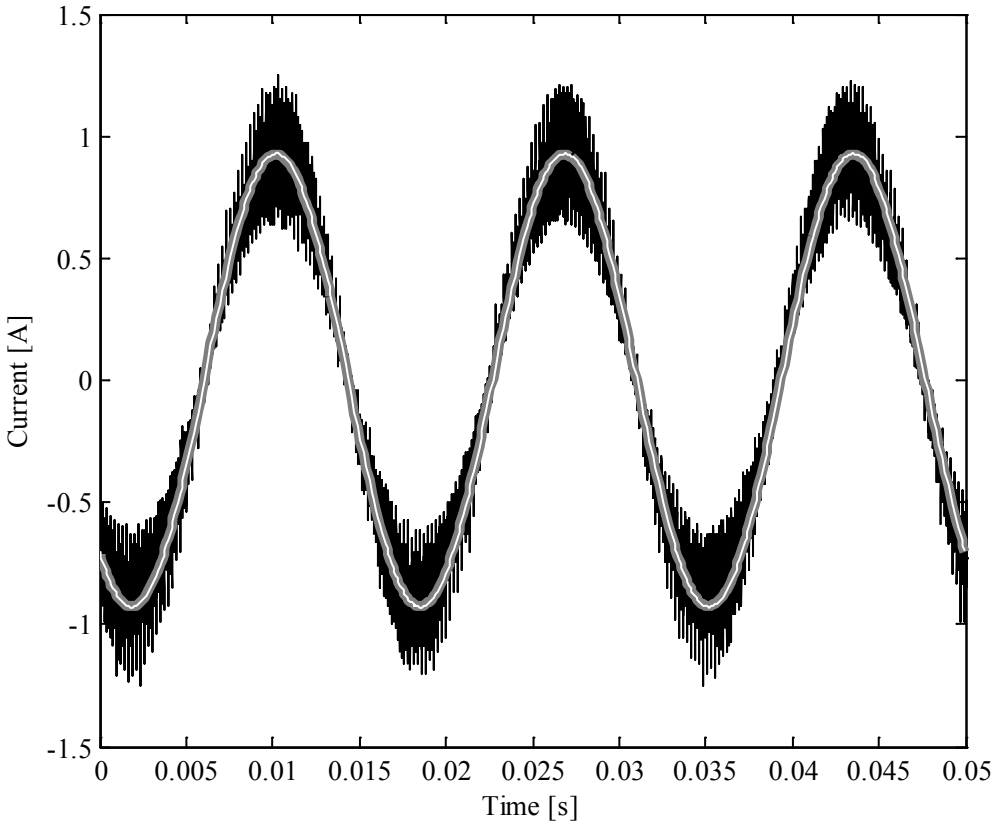


Fig. 6-22. I_{ac} output current waveforms for $d_{B,ac}$ = 0.06 operating point from Table 6-8. Note that the analytical waveform is the thin white line directly on top of the thick gray line, denoting the simulation waveform.

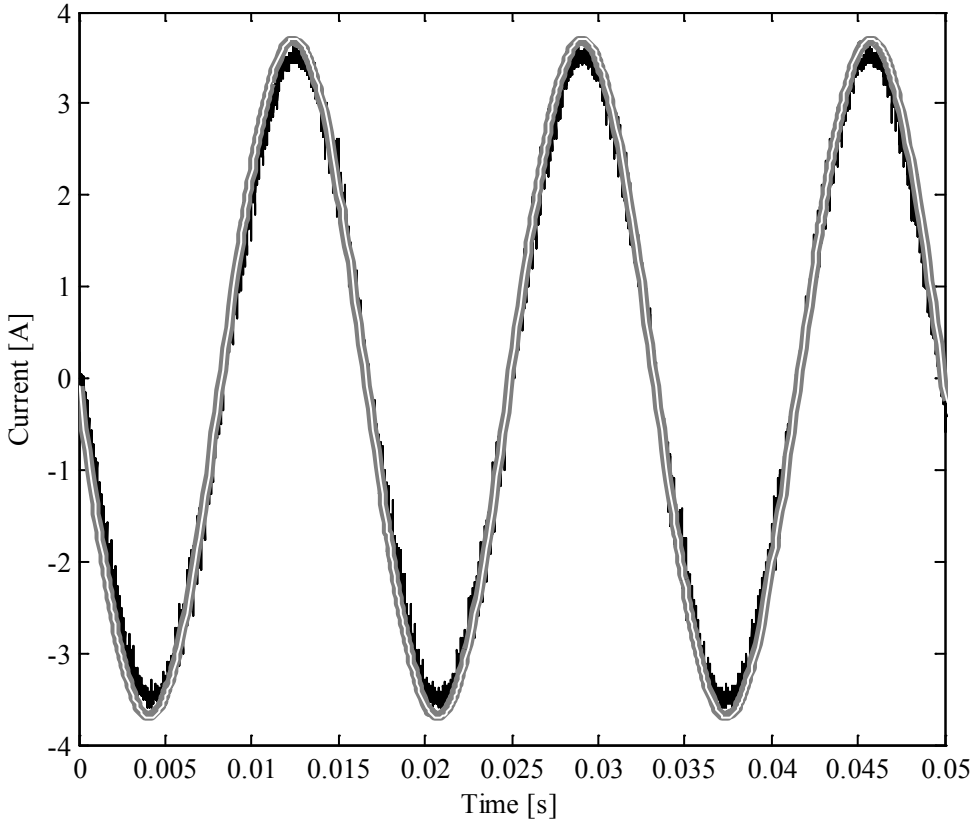


Fig. 6-23. I_{ac} output current waveforms for $d_{B,ac}$ = 0.24 operating point from Table 6-8. Note that the analytical waveform is the thin white line directly on top of the thick gray line, denoting the simulation waveform.

6.5.5 Operating point analysis

The effect of duty ratios $d_{B,dc}$ and $d_{B,ac,d}$ on V_S are predicted with the analytical model, i.e. Eq. 4-22. These relationships are verified using simulations and experimental results. The effect of the dc duty ratio $d_{B,dc}$ on V_S is shown in Table 6-9 and the effect of the ac

duty ratio $d_{B,ac}$ on V_S is shown in Table 6-10. In all cases the analytical, simulation and experimental results show exceptional correlation. It is expected that additional, unmodeled loss components such as higher R_B, switching losses, etc. are responsible for a reduction of V_S at higher loads, however the models still exhibit very good accuracy throughout. Note that the input voltage, nominally 15V or 30V, is reduced to 14.1V and 29.1V, respectively, for analytical and simulation calculations to compensate for diode forward voltage drops from the dc power supply used in the experimentation.

Table 6-9. Effect of $d_{B,ac}$ on V_S.

				$3V_S$		
$d_{B,dc}$	$d_{B,ac,d}$	$d_{B,ac,q}$	$3V_{dc}$	Analytical	Simulation	Experimental
0.1573	0.000	~0	14.1	89.64	89.66	89.7
0.1573	0.015	~0	14.1	89.64	89.65	89.7
0.1573	0.060	~0	14.1	89.64	89.63	89.8
0.1573	0.120	~0	14.1	89.64	89.58	88.8
0.1573	0.180	~0	14.1	89.64	89.41	86.8
0.1573	0.240	~0	14.1	89.64	88.90	84.1
0.1573	0.300	~0	14.1	89.64	88.29	81.6

Table 6-10. Effect of $d_{B,dc}$ on V_S.

				$3V_S$		
$d_{B,dc}$	$d_{B,ac,d}$	$d_{B,ac,q}$	$3V_{dc}$	Analytical	Simulation	Experimental
0.4224	0.000	~0	29.1	68.89	68.91	68.55
0.3992	0.000	~0	29.1	72.90	72.91	72.59
0.3539	0.000	~0	29.1	82.23	82.25	81.65
0.2717	0.000	~0	29.1	107.1	107.1	106.4
0.2146	0.000	~0	29.1	135.6	135.6	134.7

6.5.6 Eigenvalue verification

Given the complexity of the converter system, the verification of the d/q/dc operating point models for the single phase system in hardware and software is a challenging proposition. Therefore computer simulations are used to verify the dynamic models.

Time domain waveforms of the bridge dynamics, e.g. transient response, may be constructed from the LTI model of Eq. 4-35 [123] to provide verification of the operating point model's eigenvalues. Using the *n*-dimensional state space system model of states **x**, the system dynamics are represented by the eigenvalues λ_i, which have associated eigenvectors φ_{ij}. As outlined in [123], the time-domain response of a state variable to a perturbation is given by

$$\Delta x_i(t) = \varphi_{i1} c_1 e^{\lambda_1 t} + \varphi_{i2} c_2 e^{\lambda_2 t} + \ldots + \varphi_{in} c_n e^{\lambda_n t}, \qquad 6\text{-}17$$

where φ_{ij} are the right eigenvectors of the state space matrix *A*, denoted in matrix form as

$$\boldsymbol{\varphi}_\mathbf{i} = \begin{bmatrix} \varphi_{1i} & \varphi_{2i} & \ldots & \varphi_{ni} \end{bmatrix}^T. \qquad 6\text{-}18$$

The c_i are the initial conditions of each complex exponential response term, which are given by

$$c_i = \boldsymbol{\psi}_\mathbf{i} \Delta \mathbf{x}(0), \qquad 6\text{-}19$$

where $\boldsymbol{\psi}_\mathbf{i}$ denotes the left eigenvectors of *A*.

Verification of the "per unit" bridge model is accomplished by comparing the full circuit simulation transient response with the operating point model response using three

values of R_a, representing underdamped (see Fig. 6-24), near-critically damped (see Fig. 6-25), and overdamped (see Fig. 6-26) conditions.

The stimulus for all figures is a +10% step change in V_S in otherwise steady-state conditions. The simulations show clear 60 Hz and 120 Hz voltage ripple, which is expected of the actual system. These frequencies do not appear in the analytical model because they are not modeled.

The parameters for all three data sets, besides the varying R_a, are shown in Table 6-5.

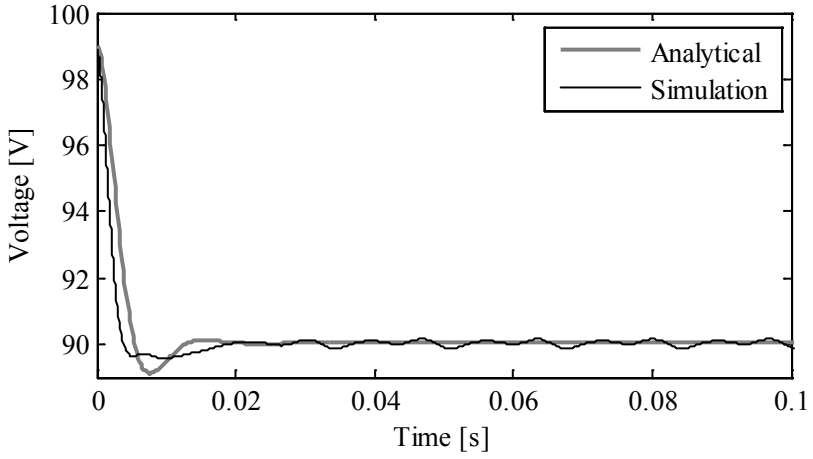


Fig. 6-24. Underdamped transient response of nonlinear simulations and linear analytical model for R_a = 0.003. LC eigenvalues lie at -47.1 +/- j64.6 Hz.

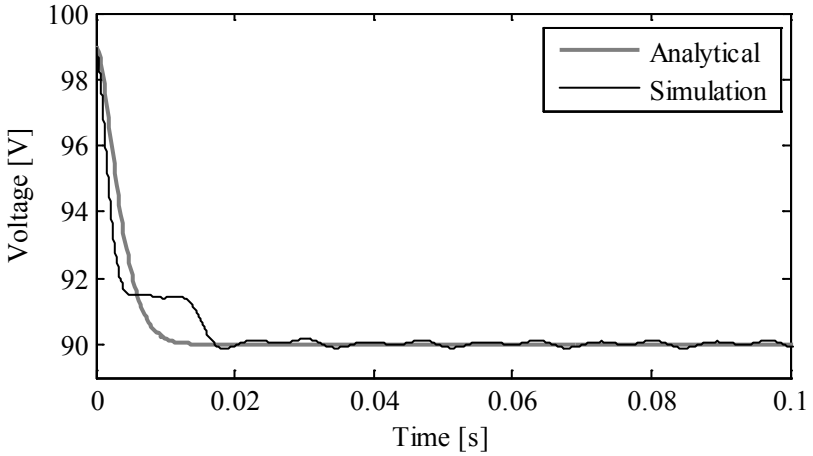


Fig. 6-25. Near-critically damped transient response of nonlinear simulations and linear analytical model for R_a = 0.0105. LC eigenvalues lie at -74.2 +/- j29.9 Hz.

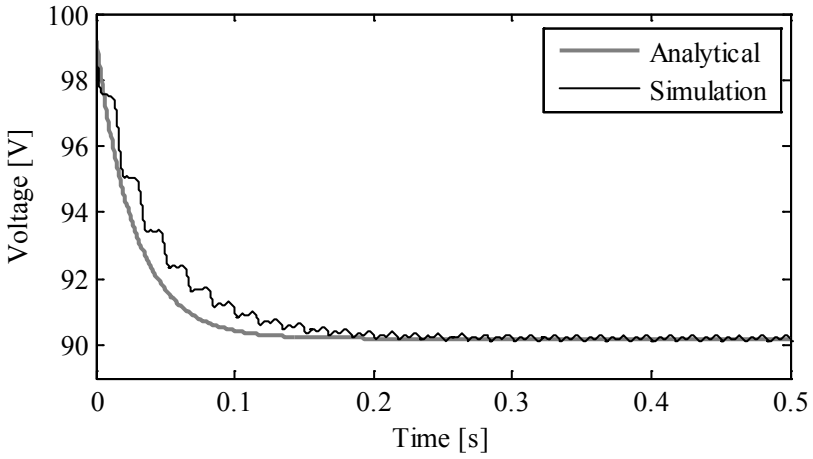


Fig. 6-26. Overdamped transient response of nonlinear simulations and linear analytical model for R_a = 0.15. LC eigenvalues lie at -5.8 Hz and -1.1kHz.

6.5.7 Multilevel eigenvalue verification

Repeating the analysis in the previous section for n_s = 3, verification of the model is accomplished by comparing the full circuit simulation transient response with the operating point model response, this time using R_a=0.15. The simulated circuit model is a straightforward multilevel version of Fig. 6-14 and Fig. 6-15, shown in Fig. 6-27 and Fig. 6-28, respectively.

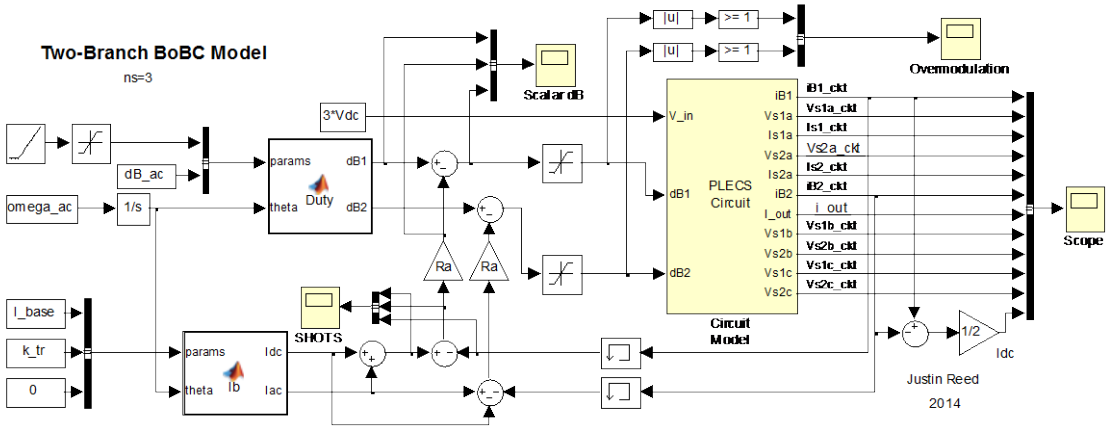


Fig. 6-27. Simulink model of single BoBC branch with n_s=3, containing multilevel PLECS circuit model.

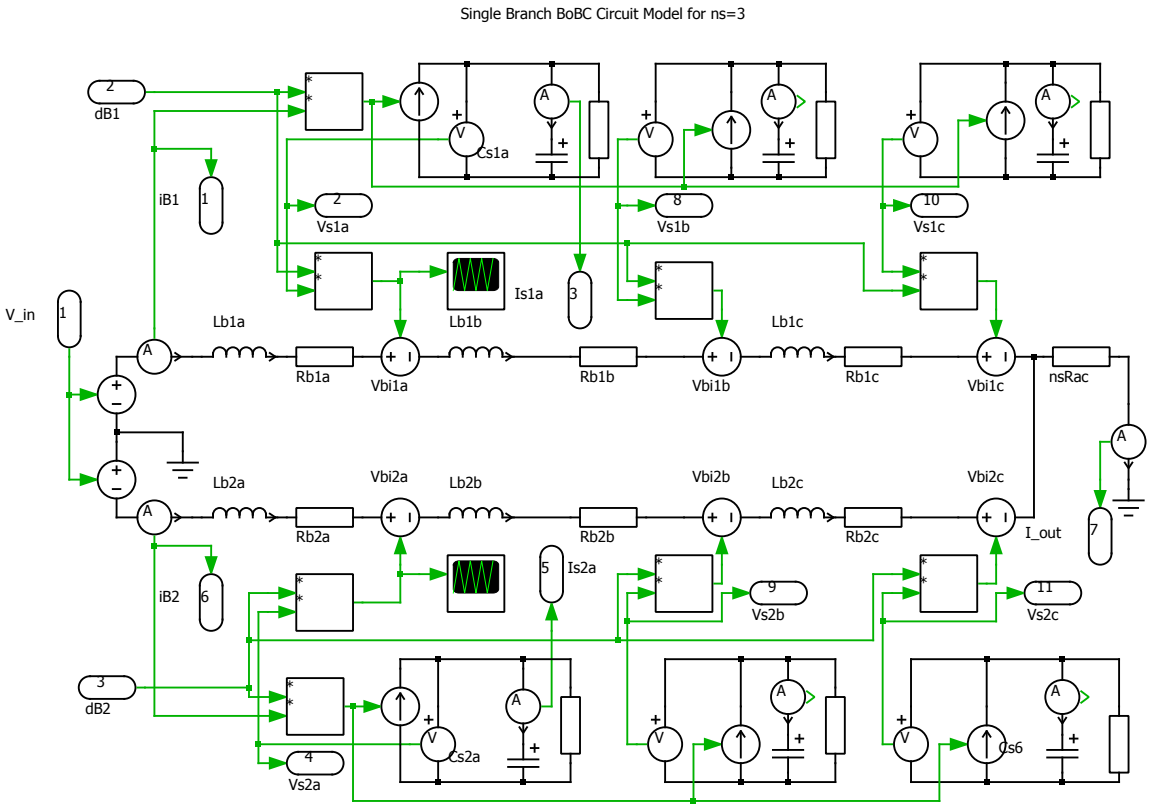


Fig. 6-28. PLECS nonlinear circuit model for n_s=3 branch, contained within Simulink branch model.

The parameters for all three data sets are again found in Table 6-5, however the bridge parameters are no longer lumped together, e.g. V_S = 30V for each bridge. Again, the stimulus for the figure is a +10% step change in one V_S state in otherwise steady-state conditions, including the two other V_S states. The simulations still show 60 Hz and 120 Hz voltage ripple as expected.

Fig. 6-29 shows the response of all 3 capacitor voltages to a +10% step change in V_{S1a}. A close-up of t=0 is shown in Fig. 6-30. The figures show excellent correlation between simulations and analytical predictions.

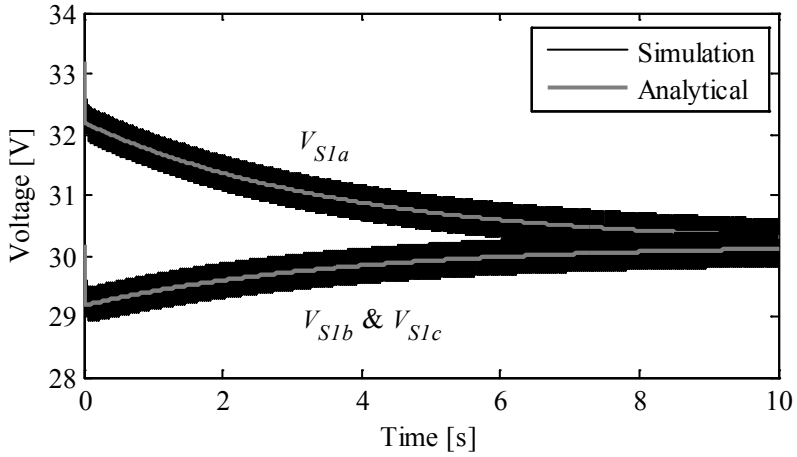


Fig. 6-29. Transient response of all 3 capacitor voltages using nonlinear simulations and linear analytical model for R_a = 0.15.

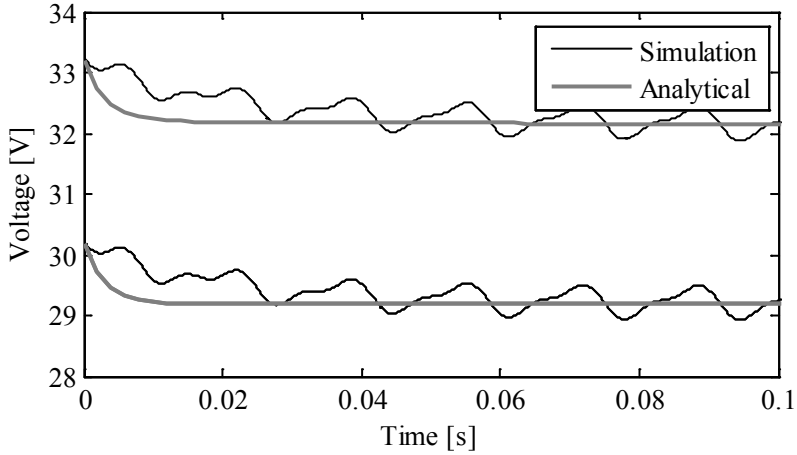


Fig. 6-30. Close-up of transient response of all 3 capacitor voltages using nonlinear simulations and linear analytical model for R_a = 0.15.

6.6 Summary

A comprehensive validation of the models presented in this research was performed in this chapter using averaged model simulations and experimental results. The design parameters of the laboratory-scale power converter prototype were presented using the design methodology outlined in Chapter 3. An overview of the higher-level functionality of each bridge circuit board was then presented, including details of the communications platform, bridge self-protection system, and overall converter hardware structure. The increased scalability of the hardware converter was highlighted, namely the localized intelligence on each CSEB and the associated housekeeping power supplies. The converter controller design was also discussed and an averaged model simulation platform was developed using the actual nonlinear circuit structure, in order to capture the inherent nonlinear plant dynamics.

The Semi-Full Bridge CSEB topology was verified using the hardware converter waveforms, which showed the necessary unidirectional current, bidirectional voltage characteristic.

The proposed capacitor sizing methodology was validated in simulations using the SHOTS controller to mitigate undesirable branch current harmonics, and therefore undesirable capacitor currents. The effect of SHOTS on capacitor current and capacitor losses was demonstrated, and analytical predictions of capacitor rms current was confirmed with simulations. Analytically predicted capacitor current waveforms for a variety of operating points were shown to very closely mimic the simulation waveforms.

Converter operating points were validated for both the scalar model and the dynamic phasor model, which were very well correlated with simulation and experimental results. Furthermore, ac output waveforms of all three platforms were essentially identical.

Finally, the dynamic phasor model was validated against simulation results. An n_s=3 averaged circuit model was developed and transient step response waveforms computed from both simulations and from the state space matrices. For the cases of n_s=1 through 3, the analytical model responses were verified.

Chapter 7 Conclusions and Future Work

This chapter presents a summary of the research work highlighting key results, in particular the work's contributions to the field of solid state power conversion. Those key results are then discussed, and recommendations for future research and investigations are identified.

The overarching goal of this work was to develop and present a generalized framework for analyzing and designing dc-ac bridge of bridge power converters in PWM operation. A battery of development and verification efforts spanning analytical, circuit simulation, and experimental domains was performed, which establishes such a framework. Despite the M2C achieving great traction in the literature since this work began, nothing has yet demonstrated such a comprehensive and generalized view of this one specific BoBC topology, much less extended the principles to the broad family of BoBC converter topologies as is presented in this work.

The BoBC, and especially the M2C, are clearly close relatives to other, more established topologies such as the boost or buck converter. However, the attributes of the BoBC that make it unique also point to the enormous volume of research and resulting literature that are still in their very early stages. As such, this work facilitates these

ongoing and future investigations by establishing a suitable, flexible and common framework across the entire BoBC topological family.

7.1 Contributions of this research

The primary contributions of this work may be identified as:

- Converter topologies in the literature (MMLC, MERS, new family, etc.) that conform to the Bridge of Bridge conversion approach have been brought together into a generalized topological framework and definitively studied using canonical techniques for their analysis and design.
- A novel CSEB topology was proposed that is immune to shoot-through faults, is well-suited for low dc voltage → high ac voltage converter applications, and has a lower parts count than other proposed fault-tolerant topologies. This topology was thoroughly analyzed, simulated and experimentally validated.
- A detailed design-oriented analysis of the CSEB-based converter power circuit has been established using the generalized BoBC topological framework. Sizing of bridge components including switches and capacitors was methodically derived. Voltage and current stresses including average and rms currents have been presented in normalized form. Furthermore, all aspects of this analysis incorporate the effects of series interleaving of bridges within each branch.

- Potentially significant current harmonics were observed with very small values of branch inductance. This behavior was investigated and its source was identified as the converter circuit impedance, which may be excited by very small voltage harmonics at the bridge terminals.
- A control scheme for mitigating undesirable current harmonics in the branches and capacitors has been motivated, presented and analyzed. By integrating a Scalar Higher Order Term Suppression (SHOTS) controller, the branch current is essentially limited to dc and ω_{ac} components, which reduces losses, reduces circulating currents, prevents the injection of unwanted currents into the source, and can reduce converter cost by permitting use of the SFB versus the FB.
- A "per-unit bridge" dynamic phasor model was developed based on the averaged scalar circuit model of the topology. By representing ac quantities in the *dq* synchronous reference frame and the dc quantities as such, steady state time-invariant solutions are provided, which offer significant advantages in design, visualization and regulation.
- Vast improvements in the accuracy of the dynamic phasor model were demonstrated on a SHOTS-enabled simulated converter with very small inductance.
- Waveforms were shown that demonstrate misalignment of the dynamic phasor model when used without a SHOTS controller, highlighting the

importance of modeling additional frequencies in the dynamic phasor model when SHOTS control is not utilized.

- Dynamic behavior resulting from the dynamic phasor model was observed, which extends beyond that captured in the state of the art. The greatest contribution in recent years was [41], which was limited to only modeling the LC resonant frequency, and simplifies the plant by decoupling the ac and dc sides of the converter. The dynamic phasor model proposed in this research overcomes these limitations.
- A small-signal stability analysis framework was proposed and utilized to determine the operating point model eigenvalues, including as a function of SHOTS gain R_a. Eigenvalue migration paths over a range of R_a were also shown.
- The effects of R_a damping on BoBC transfer function behavior were demonstrated to provide utility when designing higher level converter control methodologies. Overall, the information presented allows the system designer to choose a value of R_a to provide a well-damped system.
- The per-unit bridge dynamic phasor model was extended to n_s=2 and n_s=3 branch models, with full nonlinear plant dynamic models, operating point models, and steady-state operating point solutions.

- Scaling laws were identified to connect a converter of arbitrary size to the per-unit dynamic phasor model. These scaling laws naturally preserve the dynamic properties of the per-unit model.
- Eigensystem scaling properties were derived to identify how the system dynamics grow. A method for locating the eigenvalues in higher-scale systems was described.
- Computer simulation and hardware testing platforms were developed for verifying the models and their associated claims. The simulation platform was implemented in MATLAB/Simulink using the PLECS Blockset. The hardware testing platform was a custom-designed suite of circuit boards based on the Microchip dsPIC33FJ64GS606 microcontroller and augmented with communications, PWM synchronization, fault protection, sensing and power bridge components.
- The hardware testing platform achieved a greater level of integration than previously demonstrated in the literature by integrating the housekeeping power from each bridge's power terminals. By eliminating the need for small isolated power supplies to provide power to each bridge's control circuitry, overall system complexity is reduced. This achievement is particularly attractive in large-scale power converters, where additional peripheral equipment represents additional cost and generally reduces reliability.

- A converter controller circuit board was design and implemented, which uses a Texas Instruments F28M35 Concerto dual-core computational platform, to communicate with the bridges over CAN, and interface with a PC over USB.
- A custom CAN-based communications architecture was designed and implemented across the bridges and the converter controller board.
- A bridge-level high-speed PWM synchronization bus was designed and implemented.
- The Semi-Full Bridge CSEB topology was verified as having unidirectional current and bidirectional voltage (UCBV) characteristics.
- Selected design equations were verified using the hardware and computer simulation platforms.
- Analytical models of eigenvalue location and migration behavior were verified using computer simulations.
- Analytical model was verified using the simulation and hardware platforms.

7.2 Discussion of results

The primary goal of this research has been to develop a framework to enable the use of the BoBC in general dc-ac power converter applications. While most publications on the BoBC have shown its utility in specific circumstances and/or applications, this work has instead shown how all dc-ac BoBCs must operate by deriving their fundamental architecture using conservation of energy. Despite most of the presented research herein

focusing on the application of CSEBs to the BoBC, and especially of the SFB to the BoBC, any type of Q-cell may be applied using the same framework proposed in this work.

The BoBC has inherent flexibility, modularity and multilevel behavior. This powerful combination has the potential to establish unforeseen possibilities in power conversion, such as power amplifiers with high power throughput, extremely high ac frequency, and high efficiency. Such a converter is very difficult, if not impossible, to realize using classical converter topologies. The BoBC, however, can utilize strings and arms of Q-cells in appropriate bridge configurations to straightforwardly scale in power throughput while preserving the desirable traits of low- and medium-power switching devices. The contributions of this research provide the necessary framework for enabling these radical changes of power conversion technology.

7.3 Future work

The following branches of research are suggested to further develop the BoBC into an easily used and well-understood topology throughout industry:

- Extension of BoBC component modeling to include inductor sizing, capacitor voltage requirements, capacitor losses, switching losses, and the like.
- Relaxing any assumptions of identical bridge parameters, to encompass realistic variations in capacitance, resistance, etc. Use of statistical methods to

identify effects on steady-state and dynamic model behavior, such as eigenvalue location, can be extremely useful for BoBC modeling and design.

- Determine effects of using staircase modulation, or other switching modulation methods, on the BoBC analytical models presented herein.
- Design and implementation of low-level scalar control methodologies to minimize inter-bridge communications while modulating capacitor voltage, branch current, etc.
- Develop improvements to SHOTS controller design using state estimators, observers, disturbance input decoupling, and the like.
- Design and implementation of higher-level control methodologies to leverage the dynamic phasor model, such as motor drive controls.
- Establishing an appropriate communications control architecture across bridges, branches and converter-level controllers, including distributed and localized Finite State Machines to maintain known states and behavioral synchronicity throughout the distributed system.
- Performing investigations into and establishing criteria for the ideal communications physical layers and protocols to use within the BoBC for sharing data, commands and errors, maintaining switching synchronization, and establishing and maintaining fault tolerance in the presence of EMI.
- Performing subsequent analysis and simulations on the effects of a non-deterministic communications system on the overall converter behavior.

- Investigating the best approaches to achieve tolerance of faults internal to the BoBC, e.g. bypassing faulty bridges, including any limitations resulting from bridge topology choice.
- Investigating the effects of asymmetrical loading on the converter, e.g. phase imbalance.
- Investigating the effects of the bridge-localized housekeeping power supplies on bridge voltage stability.
- Performing an investigation into proper converter startup procedures to minimize peripheral equipment.
- Expanding the BoBC framework to other topologies within the BoBC family, such as direct ac/ac topologies, isolated ac/dc/ac topologies, or dc/ac/dc topologies. Also incorporating other Q-cells such as the ISEB, electromechanical energy storage, or MERS.

This research has shown that the Bridge of Bridge Converter represents an entire field of potential research, which could lead to mass-produced, inexpensive power converter "building blocks," and therefore provide a fundamental shift to how power converters are designed and built.

Chapter 8 Appendices

A RMS Currents for HB CSEB

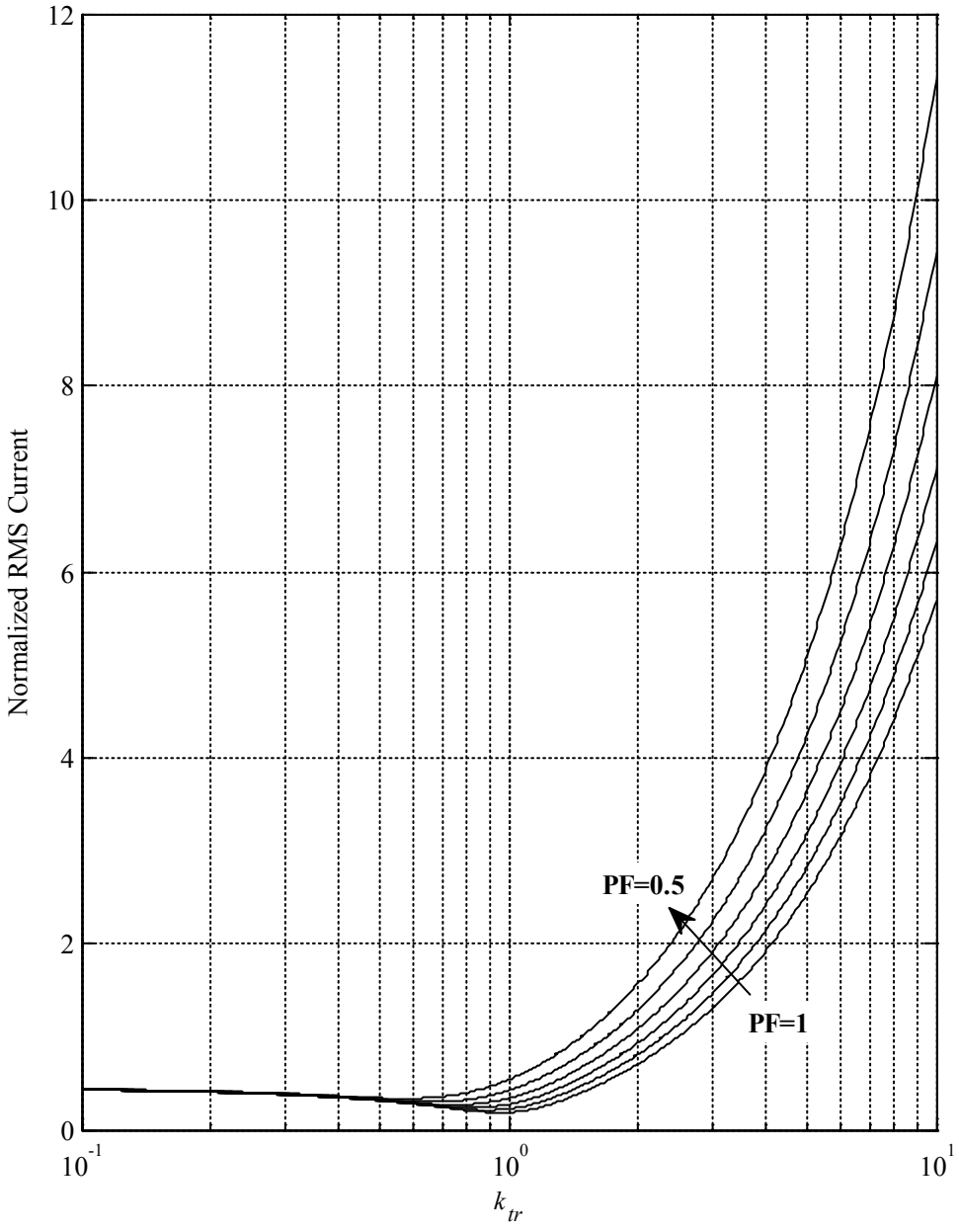


Fig. 8-1. Normalized rms current through S1 for $M = 0.9$ and varying power factor. The minimum value is approximately 0.18 at $k_{tr} = 0.95$ and unity power factor.

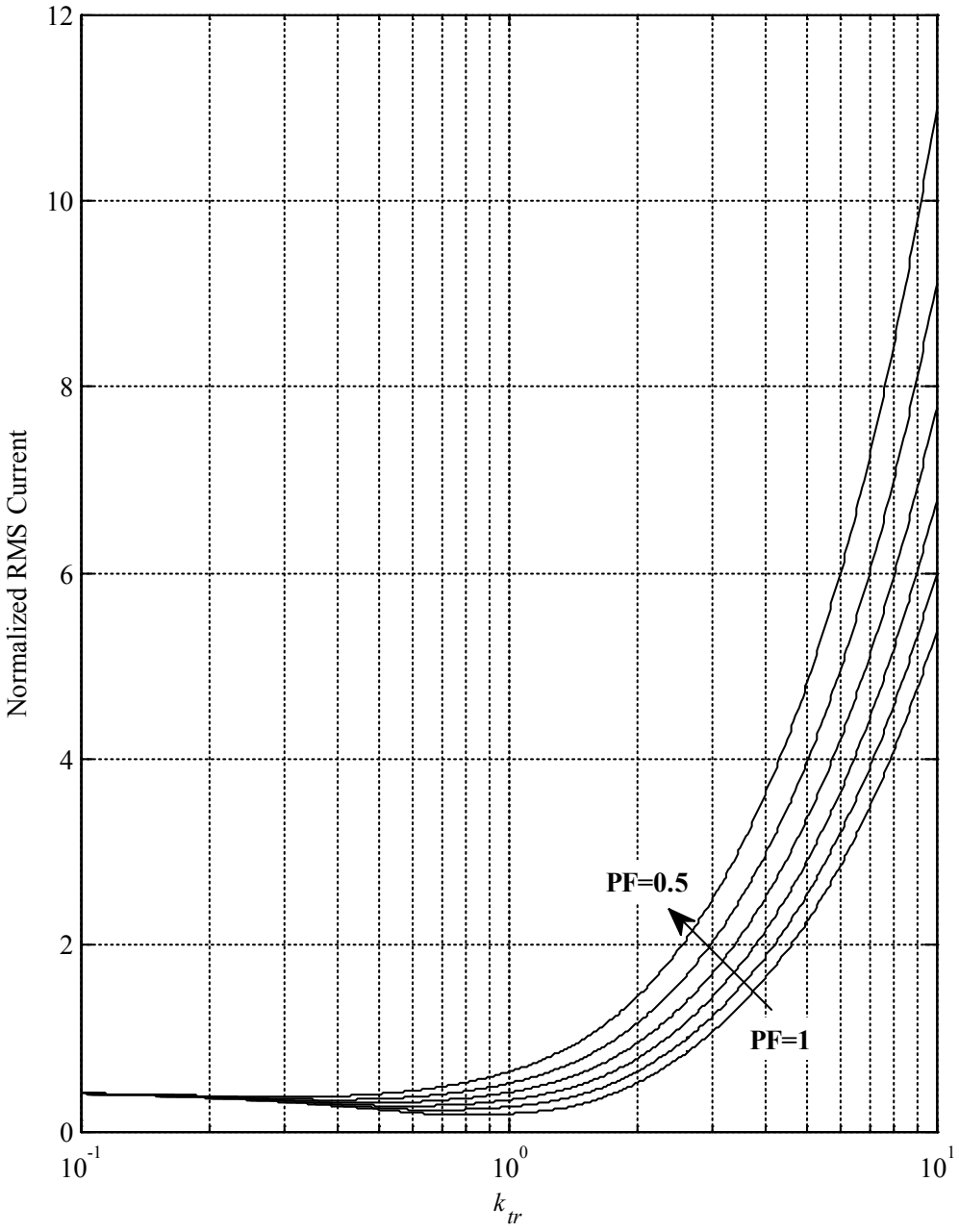


Fig. 8-2. Normalized rms current through D1 for $M = 0.9$ and varying power factor. The minimum value is approximately 0.18 at $k_{tr} = 0.79$ and unity power factor.

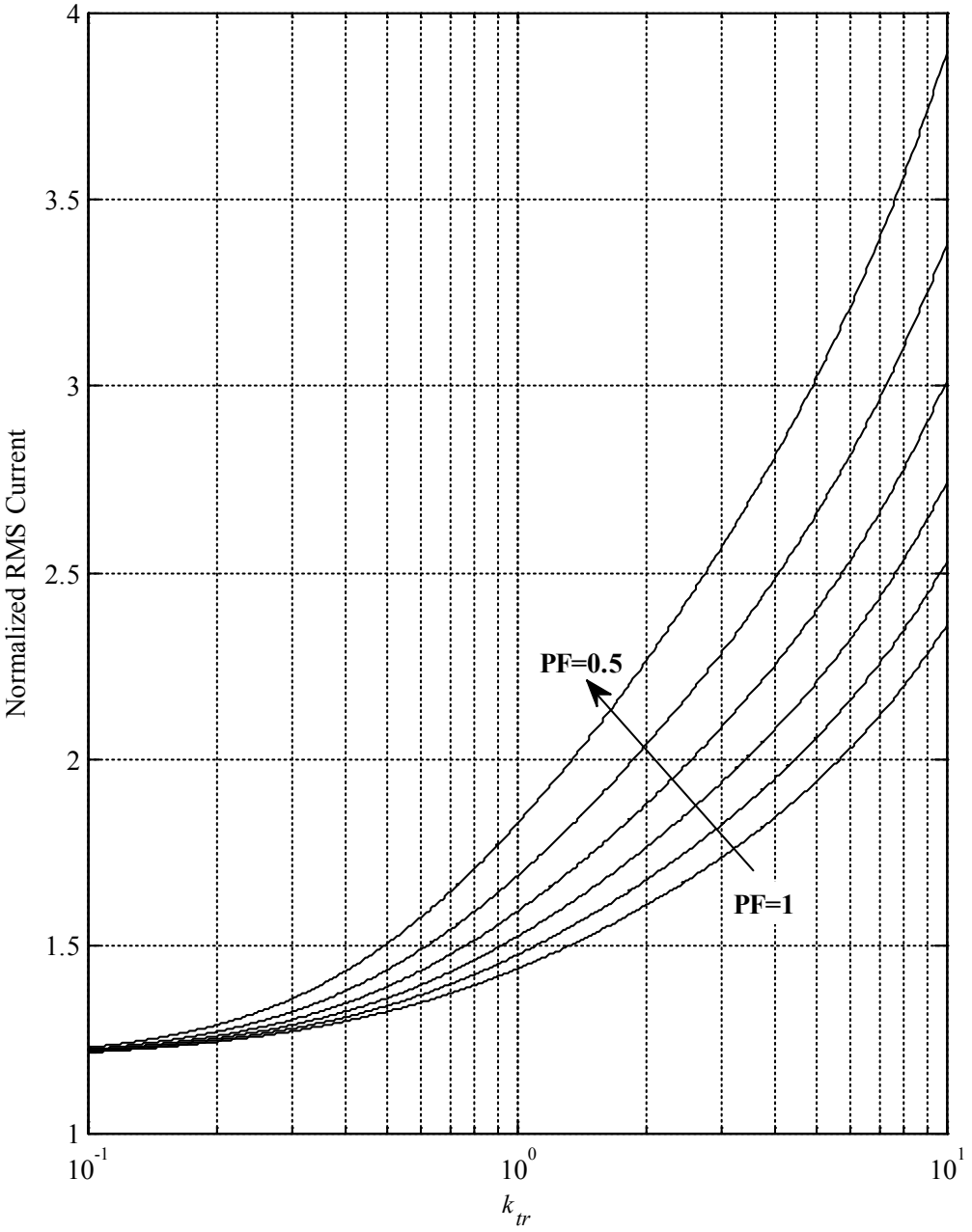


Fig. 8-3. Normalized rms current through S2 for $M = 0.9$ and varying power factor. The minimum value is approximately 1.22 at $k_{tr} = 0.10$ and unity power factor.

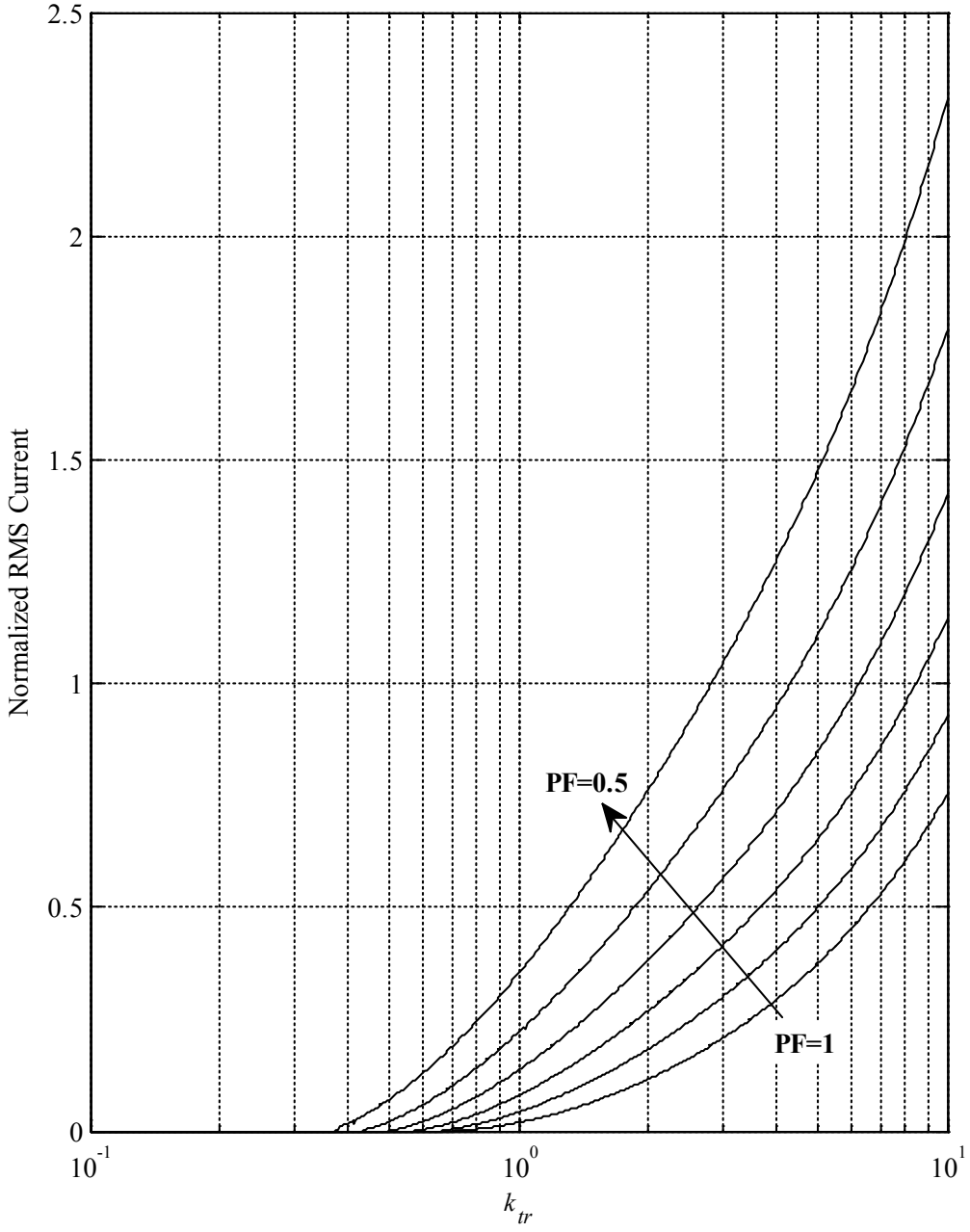


Fig. 8-4. Normalized rms current through D2 for $M = 0.9$ and varying power factor. The minimum value is 0, encountered at $k_{tr} = 0.707$ for unity power factor.

B RMS currents for FB and SFB CSEBs

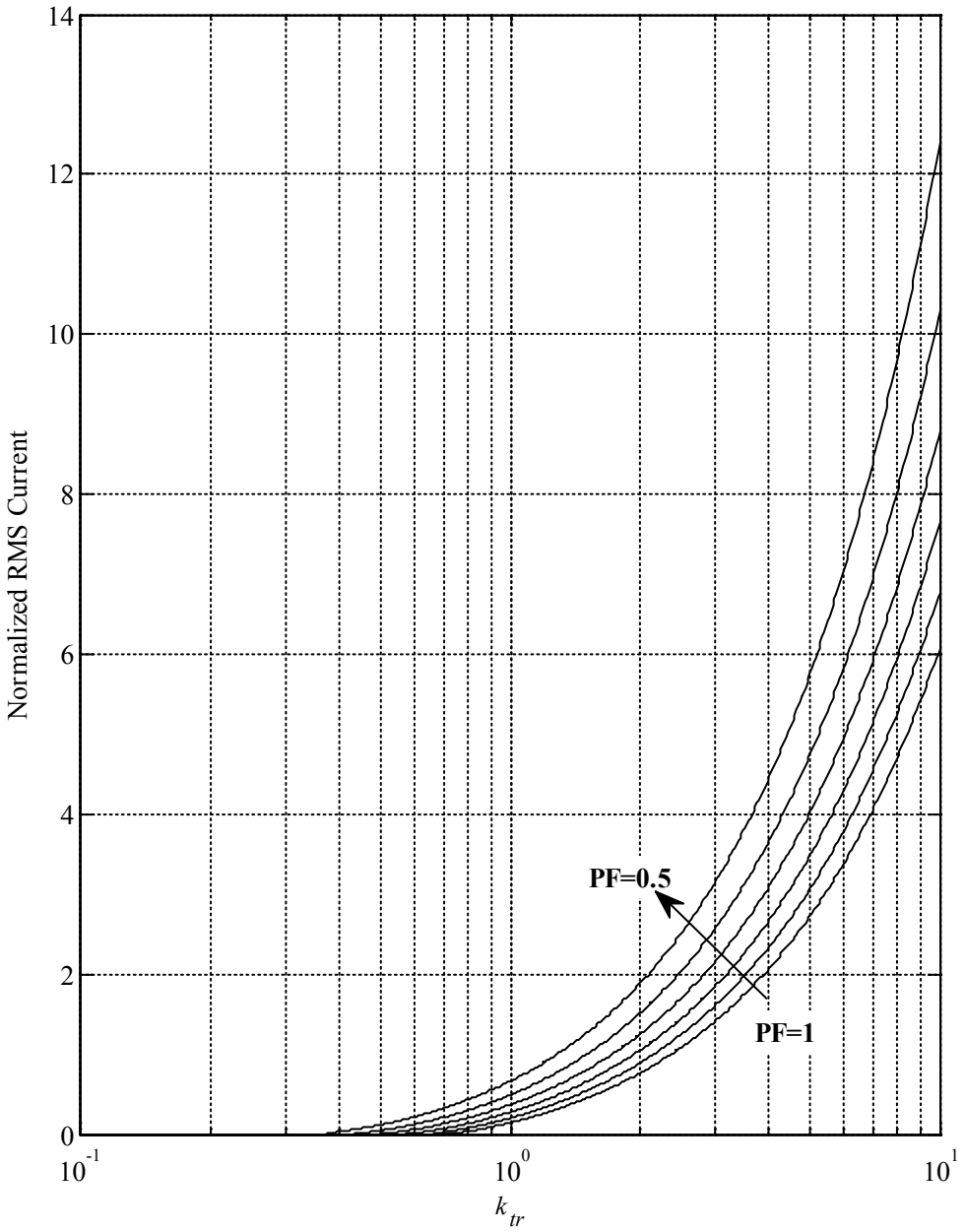


Fig. 8-5. Normalized rms current through S11 or S22 for $M = 0.9$ and varying power factor. The minimum value is 0, encountered at $k_{tr} = 0.707$ for unity power factor.

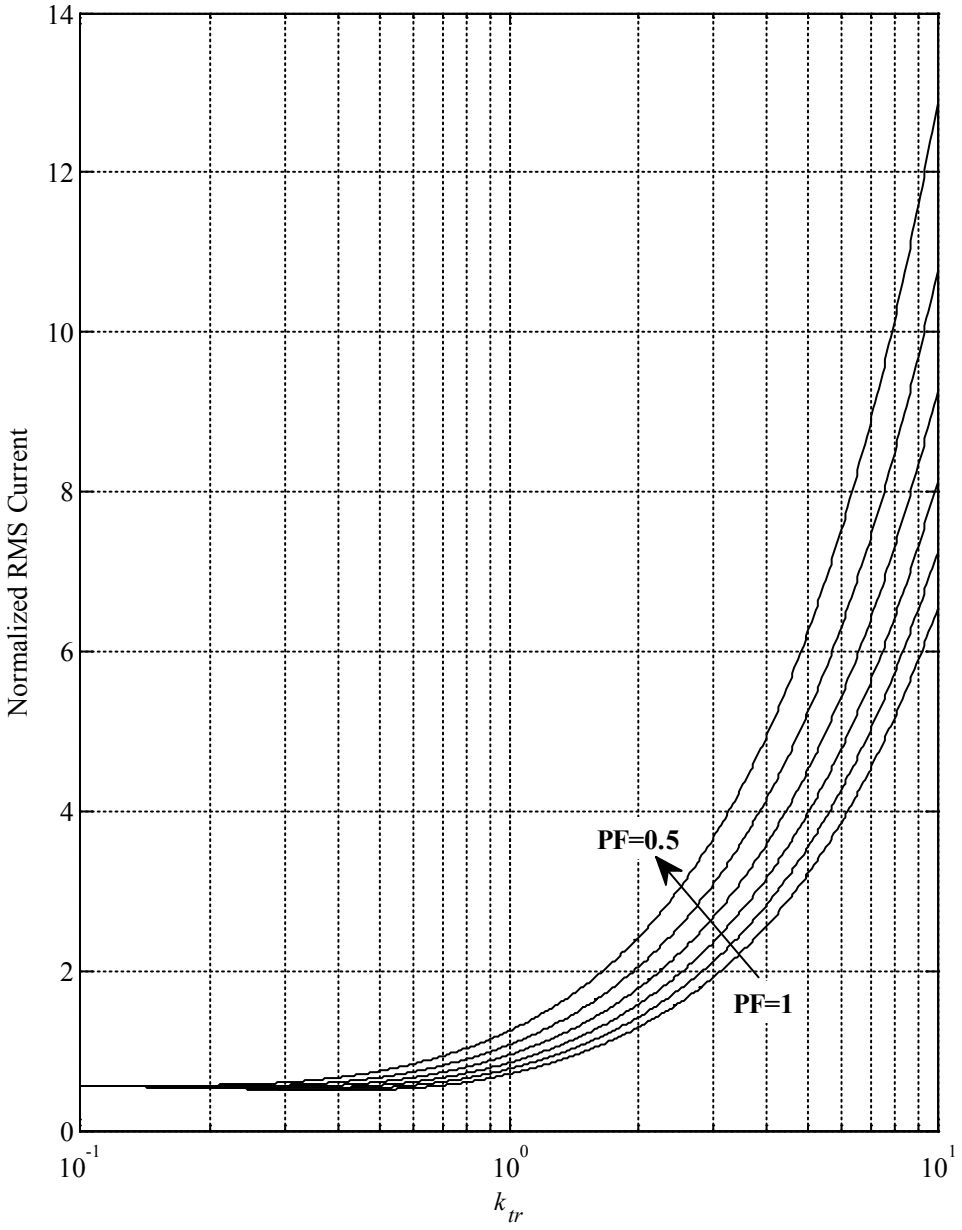


Fig. 8-6. Normalized rms current through D11 or D22 for $M = 0.9$ and varying power factor. The minimum value is 0.51 at $k_{tr} = 0.39$ for unity power factor.

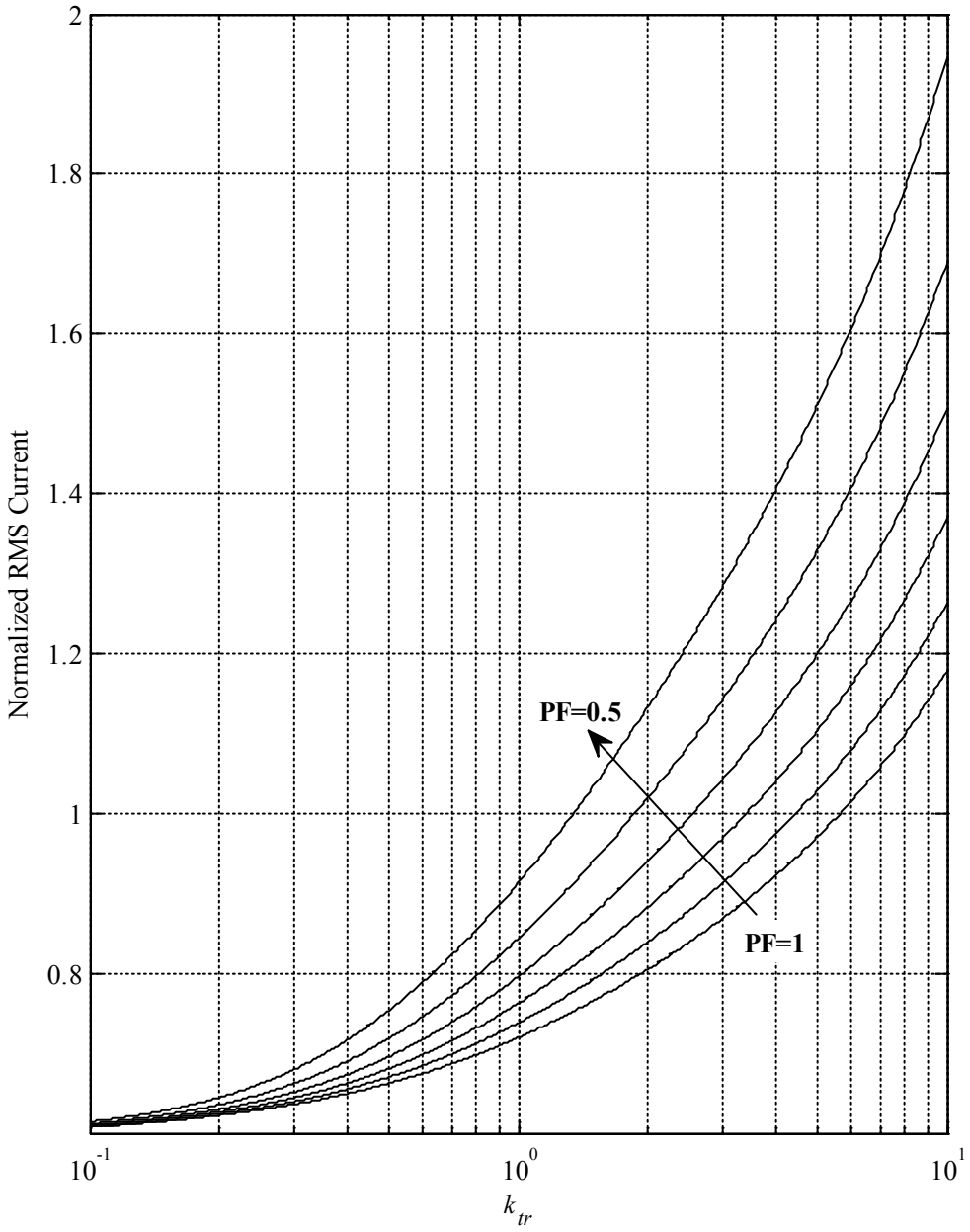


Fig. 8-7. Normalized rms current through S21 or S12 for $M = 0.9$ and varying power factor. The minimum value is 0.61 at $k_{tr} = 0.1$ for unity power factor.

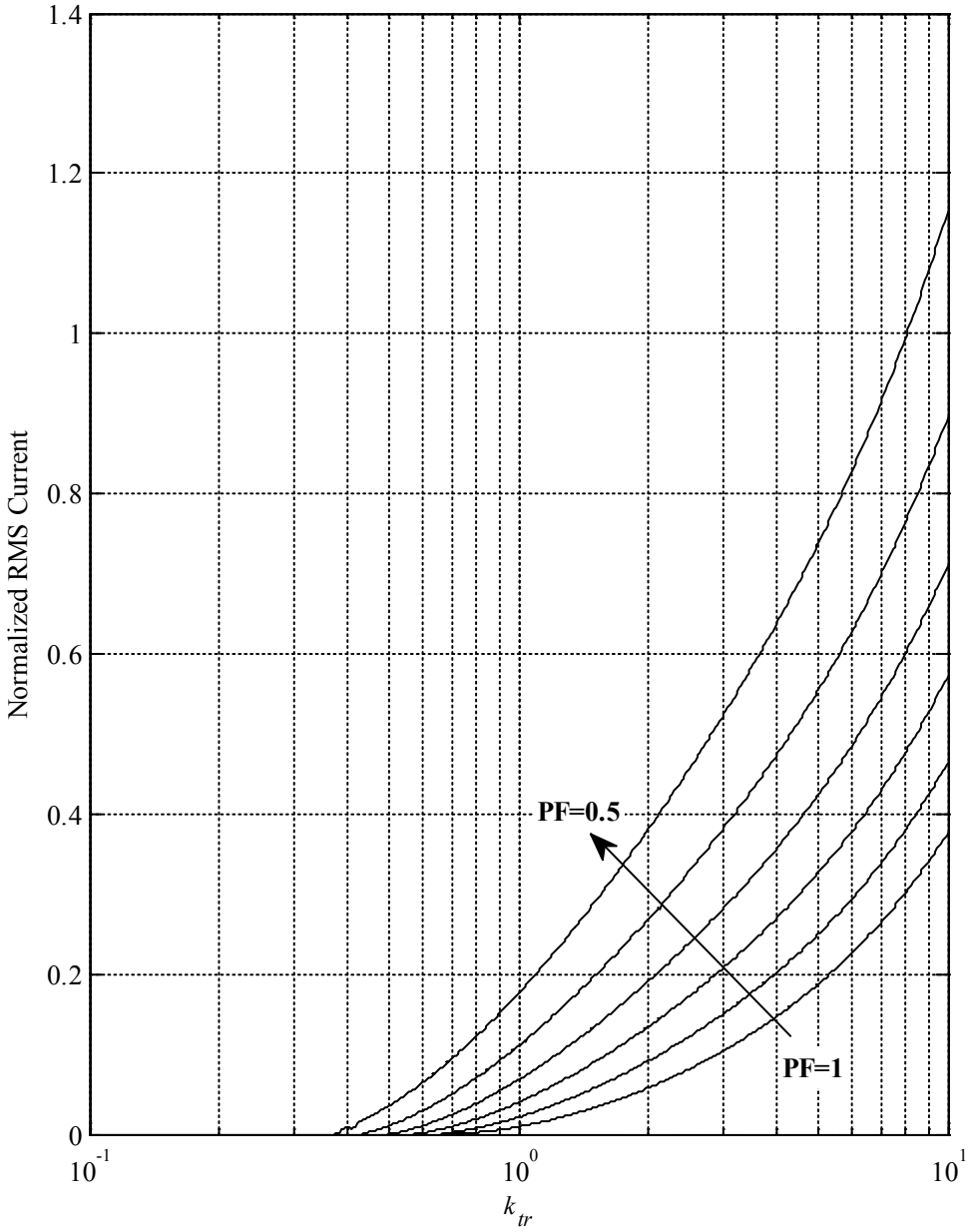


Fig. 8-8. Normalized rms current through D21 or D12 for $M = 0.9$ and varying power factor. The minimum value is 0, encountered at $k_{tr} = 0.707$ for unity power factor.

C Simulation initialization script

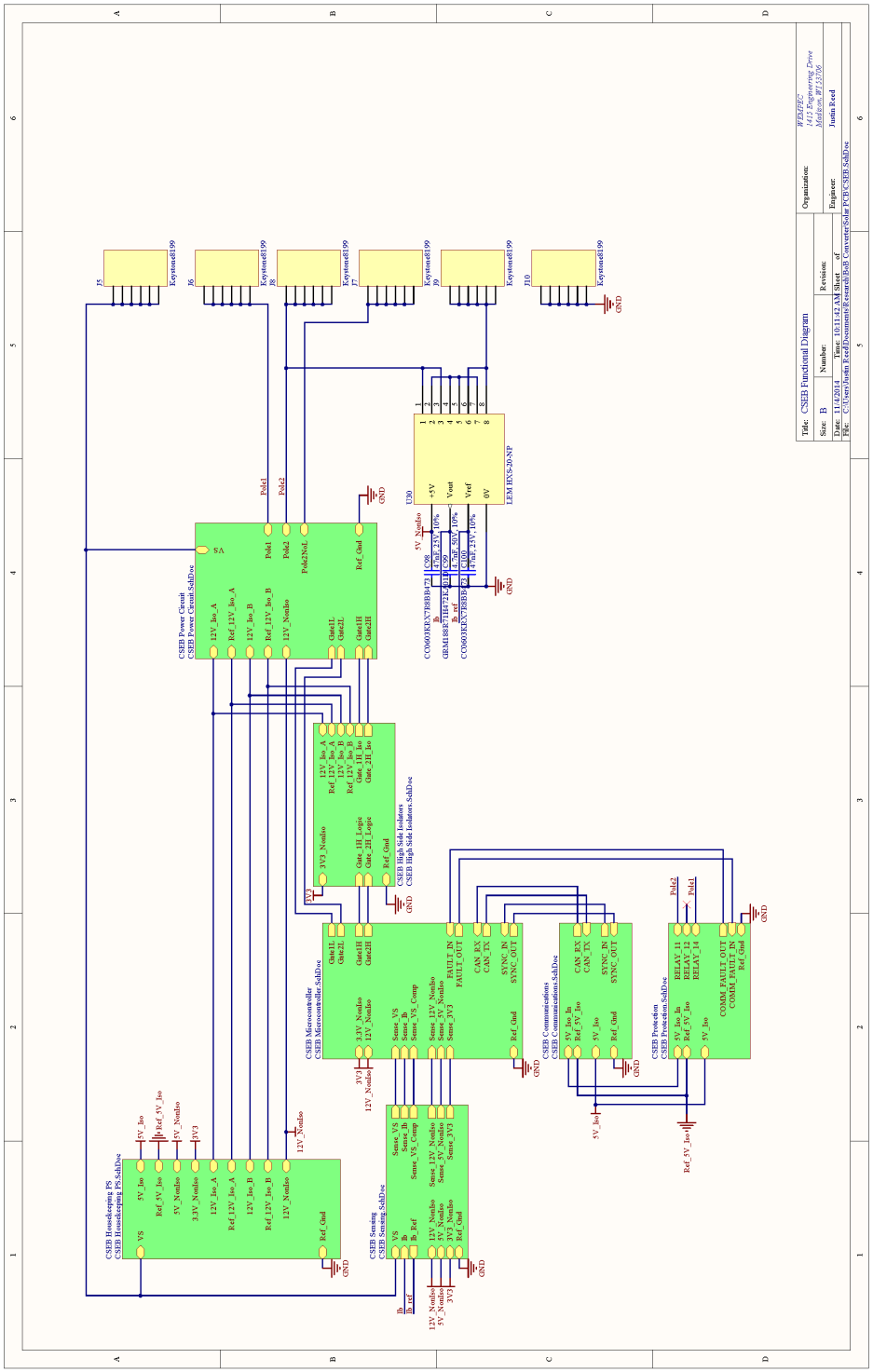
```
% sim_setup.m
% Sets up the simulations in DC_AC_PLECS_HB_CL.mdl
% (single bridge per branch)
% Justin Reed
% November 2014

omega_ac = 2*pi*60;
Rac = 8.2;
Vdc = 30;
ns = 3;
Lb = ns*22e-6;
Rb = ns*0.01;
Rs = ns*750;
Cs = 0.005/ns;
Vs_i = ns*30;     % Initial conditions for capacitor voltages
Ib1_i = 0;        % Initial conditions for branch currents
Ib2_i = 0;
Ib_ac_d = sqrt(2);      % Target ac branch current
Ib_ac_q = 0;
I_base = (Vdc - sqrt(Vdc.^2 - 4*Rb*((Rb+2*Rac)*(Ib_ac_d^2 + Ib_ac_q^2)
+ Vs_i.^2/Rs)))/2/Rb;
dB_dc = (Vdc-Rb*I_base)/Vs_i;
dB_ac_d = (omega_ac*Lb*Ib_ac_q-(Rb+2*Rac)*Ib_ac_d)/Vs_i;
dB_ac_q = (-omega_ac*Lb*Ib_ac_d-(Rb+2*Rac)*Ib_ac_q)/Vs_i;
k_tr = dB_dc/dB_ac;
M = dB_ac*(k_tr + sqrt(2));

Ra = 0;
Db_ac_d_cmd = dB_ac_d;
Db_ac_q_cmd = dB_ac_q;
Db_dc_cmd = dB_dc;

Ib_dc = I_base;
Ib_ac_d_ref = Ib_ac_d;
Ib_ac_q_ref = Ib_ac_q;
Ib_dc_ref = Ib_dc;
```

D CSEB Schematics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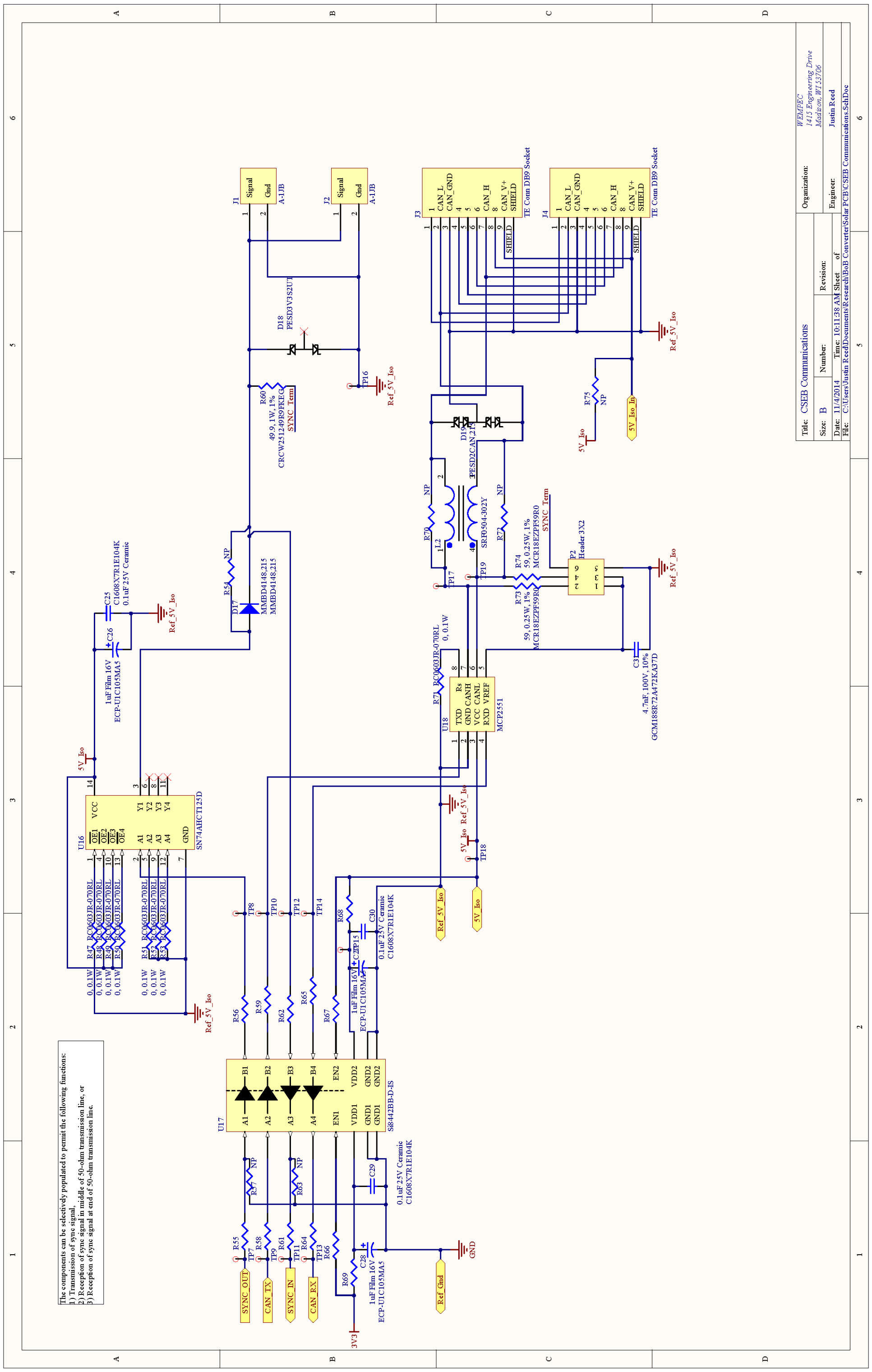
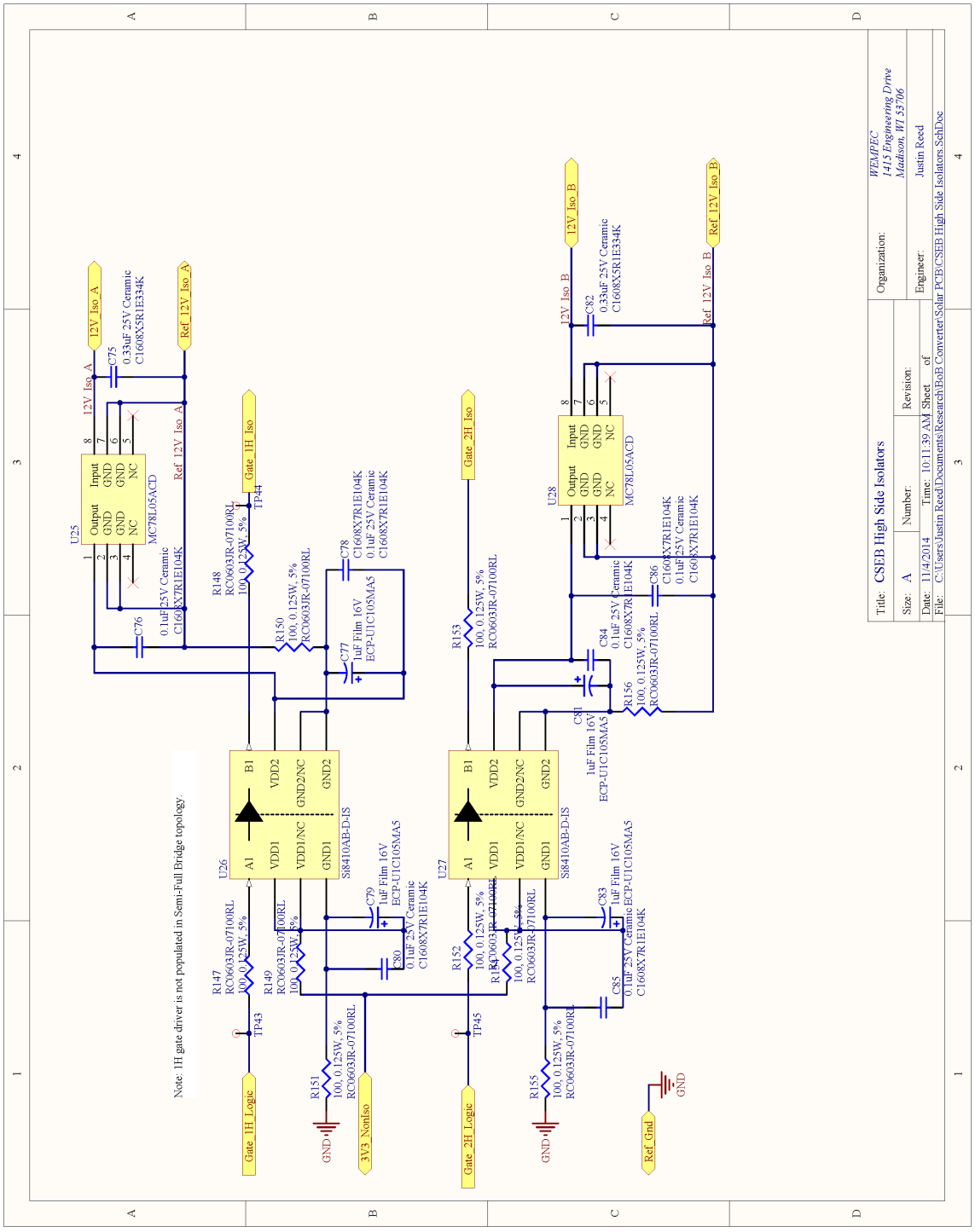
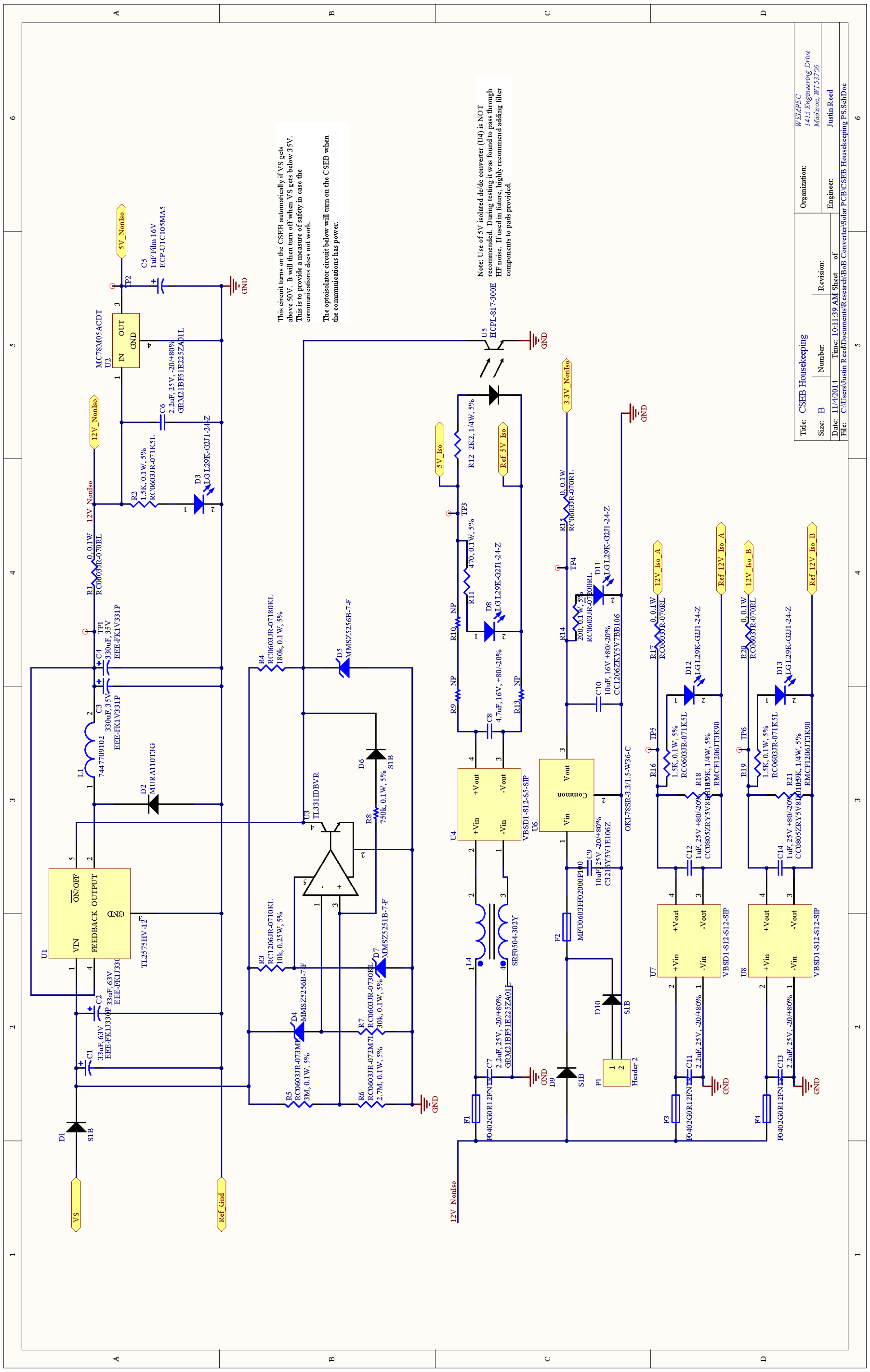
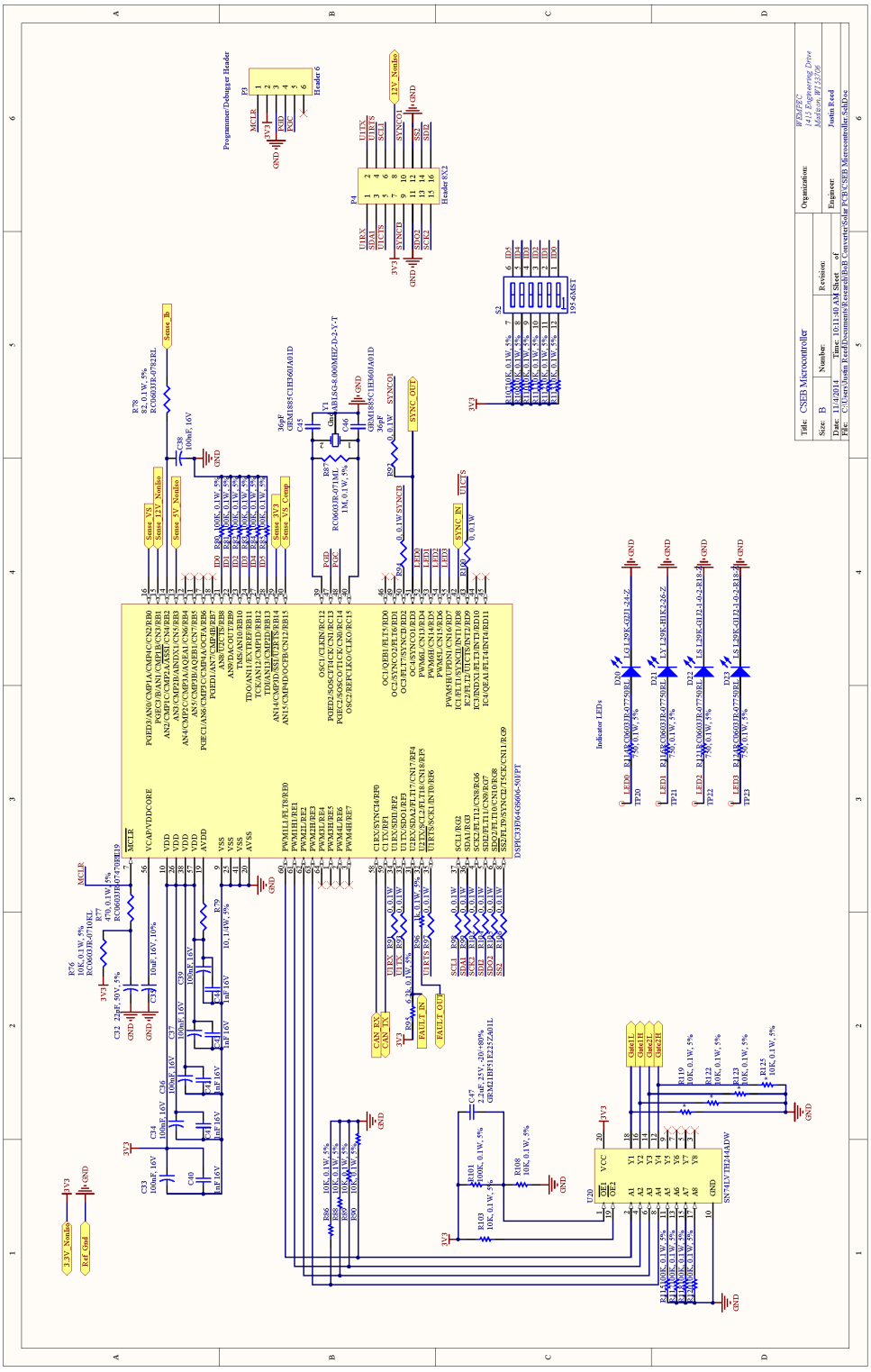
Size: B
Number:
Revision:
Date: 11/4/2014
Time: 10:11:42 AM
Sheet of
File: C:\Users\Justin Reed\Documents\Research\BoB Converter\Solar PCB\CSEB.SchDoc
Organization: FEDEC
Engineer: Justin Reed
CSEB Power Circuit
CSEB Power Circuit.SchDoc
CSEB High Side Isolators
CSEB High Side Isolators.SchDoc
CSEB Microcontroller
CSEB Microcontroller.SchDoc
CSEB Communications
CSEB Communications.SchDoc
CSEB Protection
CSEB Protection.SchDoc
CSEB Sensing
CSEB Sensing.SchDoc
CSEB Housekeeping PS
CSEB Housekeeping PS.SchDoc
LEM HXS-20-NP
GND

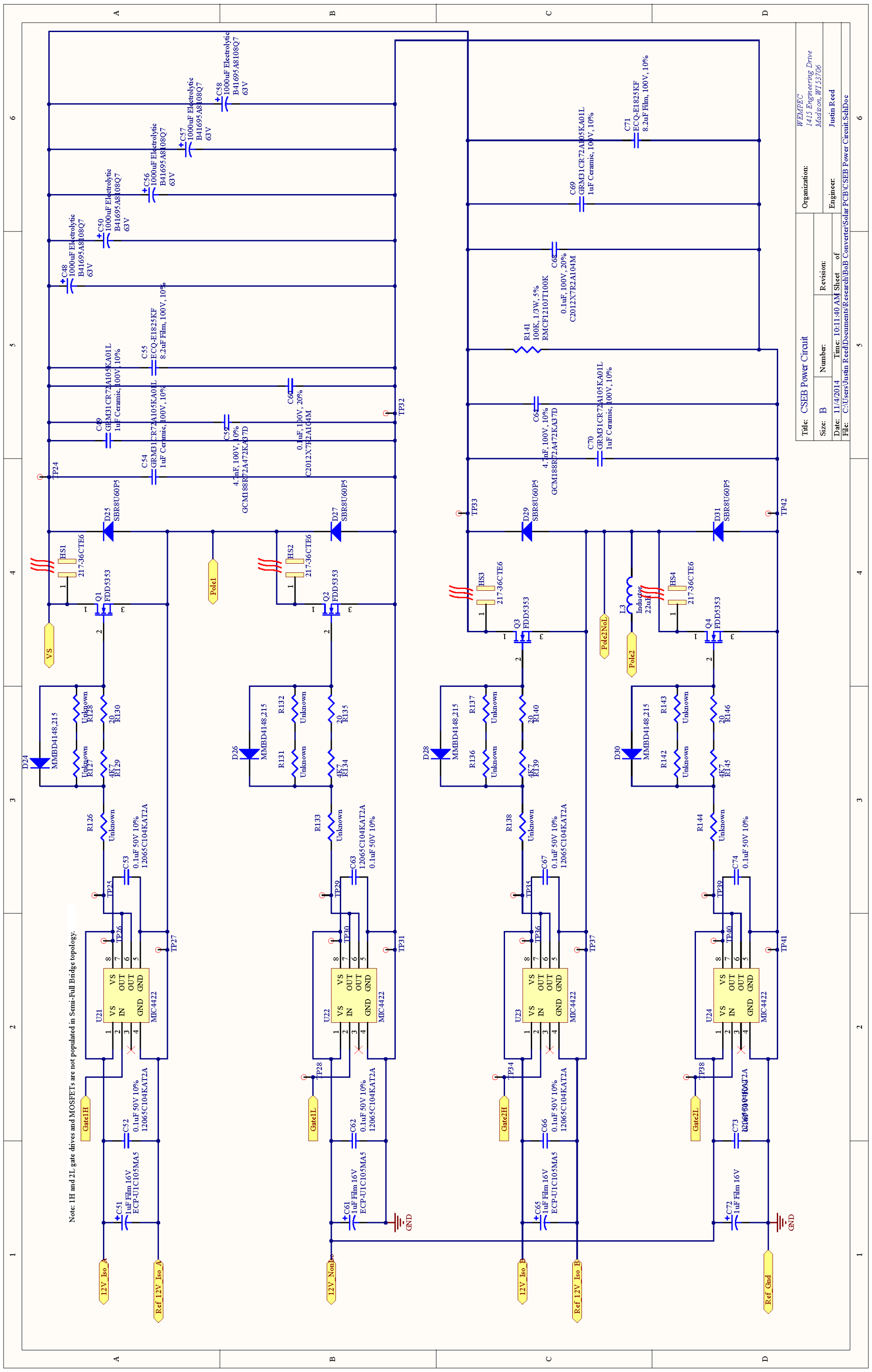


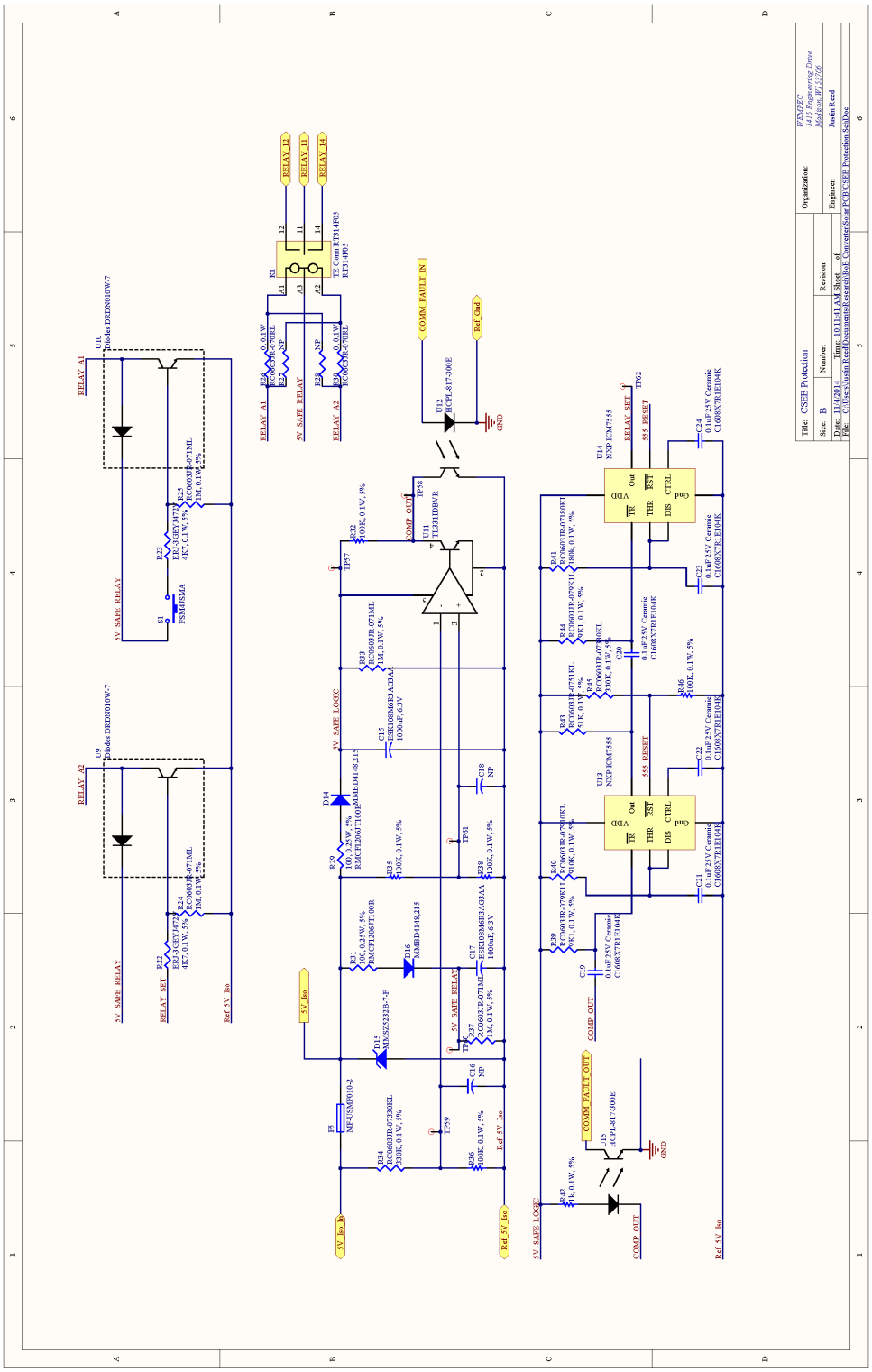
The components can be selectively populated to permit the following functions:
1) Transmission of sync signal.
2) Reception of sync signal in middle of 50-ohm transmission line, or
3) Reception of sync signal at end of 50-ohm transmission line.
Title: CSEB Communications
Size: B
Date: 11/4/2014
Organization: WEMPEC
1415 Engineering Drive
Madison, WI 53706
Engineer: Justin Reed
SN74AHCT125D
MCP2551
TE Conn DB9 Socket
SYNC_OUT
CAN_TX
SYNC_IN
CAN_RX
Ref_Gnd
GND
3V3
5V_Iso
Ref_5V_Iso


Note: 1H gate driver is not populated in Semi-Full Bridge topology.
Title: CSEB High Side Isolators
Organization: WEMPEC
1415 Engineering Drive
Madison, WI 53706
Size: A
Number:
Revision:
Engineer: Justin Reed
Date: 11/4/2014
Time: 10:11:39 AM
Sheet of
File: C:\Users\Justin Reed\Documents\Research\BoB Converter\Solar PCB\CSEB High Side Isolators.SchDoc
U25
U26
U27
U28
Si8410AB-D-IS
MC78L05ACD
12V_Iso_A
Ref_12V_Iso_A
12V_Iso_B
Ref_12V_Iso_B
Gate_1H_Iso
Gate_2H_Iso
Gate_1H_Logic
Gate_2H_Logic
3V3_NonIso
Ref_Gnd
GND


This circuit turns on the CSEB automatically if VS gets above 50V. It will then turn off when VS gets below 35V. This is to provide a measure of safety in case the communications does not work.
The optoisolator circuit below will turn on the CSEB when the communications has power.
Note: Use of 5V isolated dc/dc converter (U4) is NOT recommended. During testing it was found to pass through HF noise. If used in future, highly recommend adding filter components to pads provided.
Title: CSEB Housekeeping
Size: B
Number:
Revision:
Date: 11/4/2014
Time: 10:11:39 AM
Sheet of
File: C:\Users\Justin Reed\Documents\Research\BoB Converter\Solar PCB\CSEB Housekeeping PS.SchDoc
Organization: WEMPEC 1415 Engineering Drive Madison, WI 53706
Engineer: Justin Reed
VS
Ref_Gnd
12V_NonIso
5V_NonIso
3.3V_NonIso
5V_Iso
Ref_5V_Iso
12V_Iso_A
Ref_12V_Iso_A
12V_Iso_B
Ref_12V_Iso_B
GND
TL2575HV-12
MC78M05ACDT
TL331IDBVR
HCPL-817-300E
VBSD1-S12-S5-SIP
VBSD1-S12-S12-SIP
OKI-78SR-3.3/1.5-W36-C
Header 2




Note: 1H and 2L gate drives and MOSFETs are not populated in Semi-Full Bridge topology.
Title: CSEB Power Circuit
Justin Reed


Title: CSEB Protection
Size: B
Number:
Revision:
Date: 11/4/2014
Time: 10:11:41 AM
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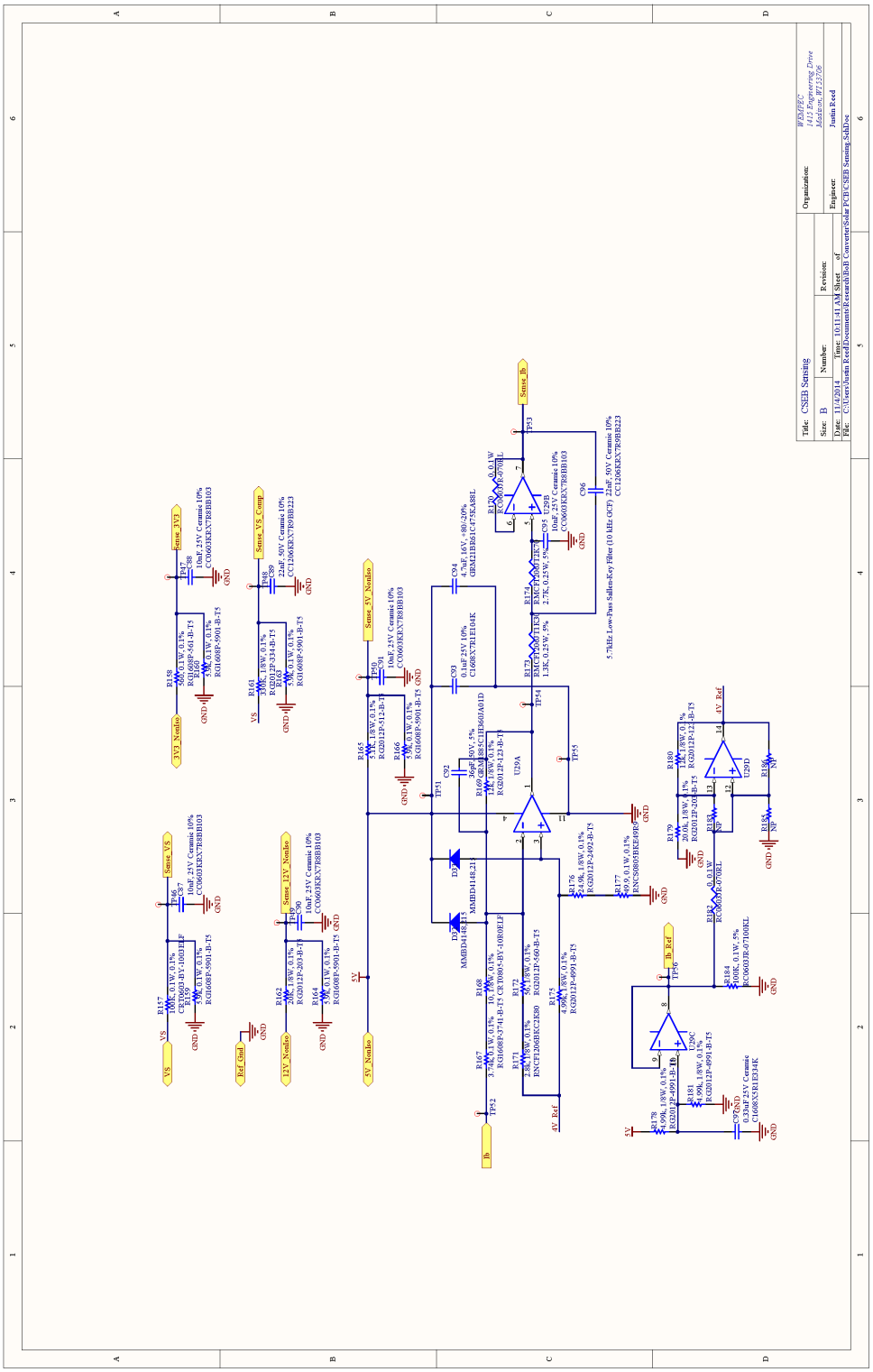
File: C:\Users\Justin Reed\Documents\Research\BoB Converter\Solar PCB\CSEB Protection.SchDoc
Organization: FREDEC
1415 Engineering Drive
Madison, WI 53706
Engineer: Justin Reed
5V_SAFE_RELAY
RELAY_A1
RELAY_A2
RELAY_SET
Ref_5V_Iso
5V_Iso
5V_Iso_In
Ref_5V_Iso_In
5V_SAFE_LOGIC
COMP_OUT
COMM_FAULT_OUT
COMM_FAULT_IN
Ref_Gnd
GND
555_RESET
RELAY_SET
RELAY_12
RELAY_11
RELAY_14
Diodes DRDN01W-7
FSMSSMA
TE Conn RT314F05
NXP ICM7555
HCPL-817-300E
TLV1101IDBVR
MF-USMF010-2
MMBD4148-215
SMAS2323B-7-F


Title: CSED Sensing
Size: B
Number:
Revision:
Date: 11/4/2014
Time: 10:11:41 AM
Sheet of
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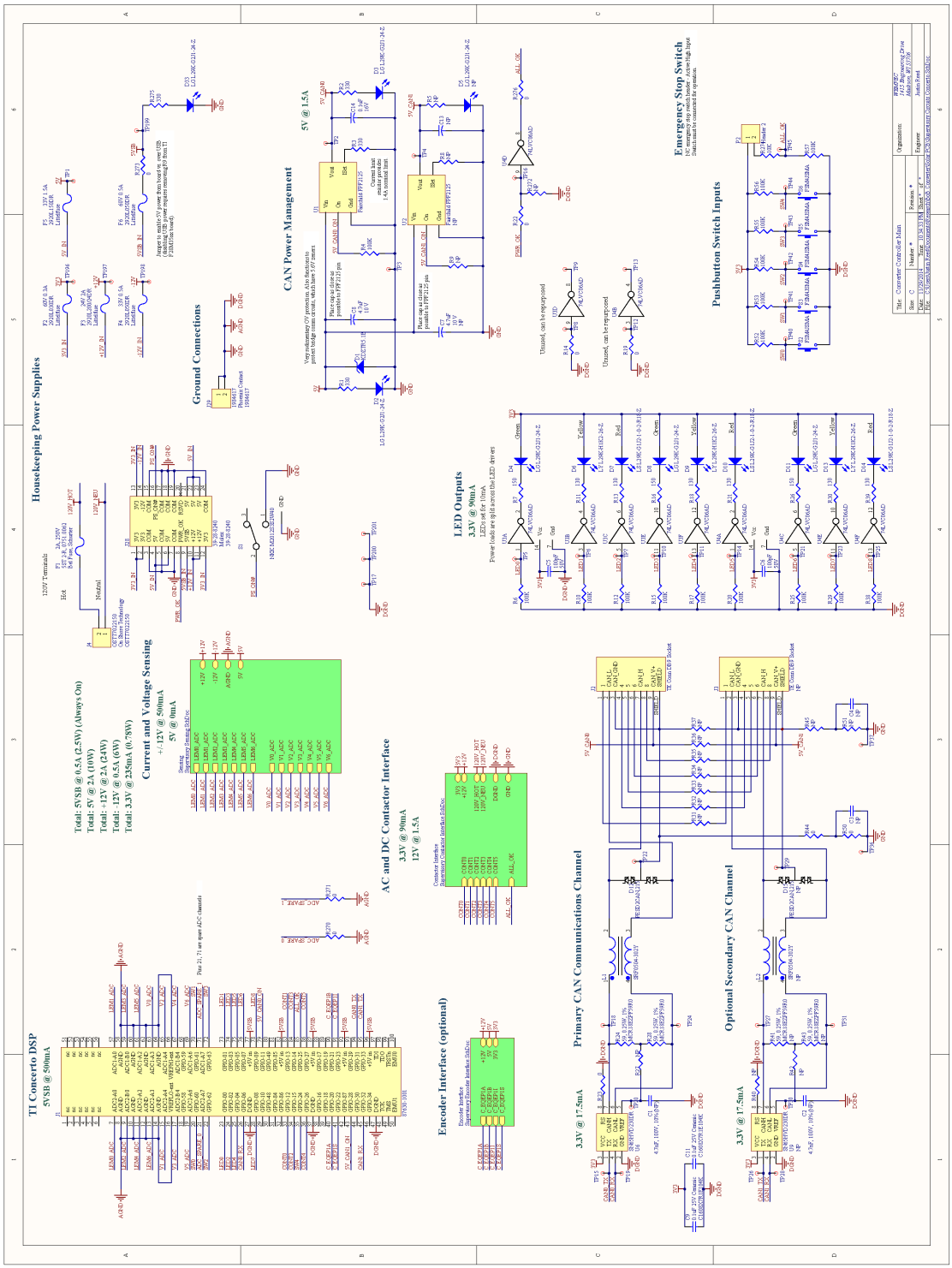
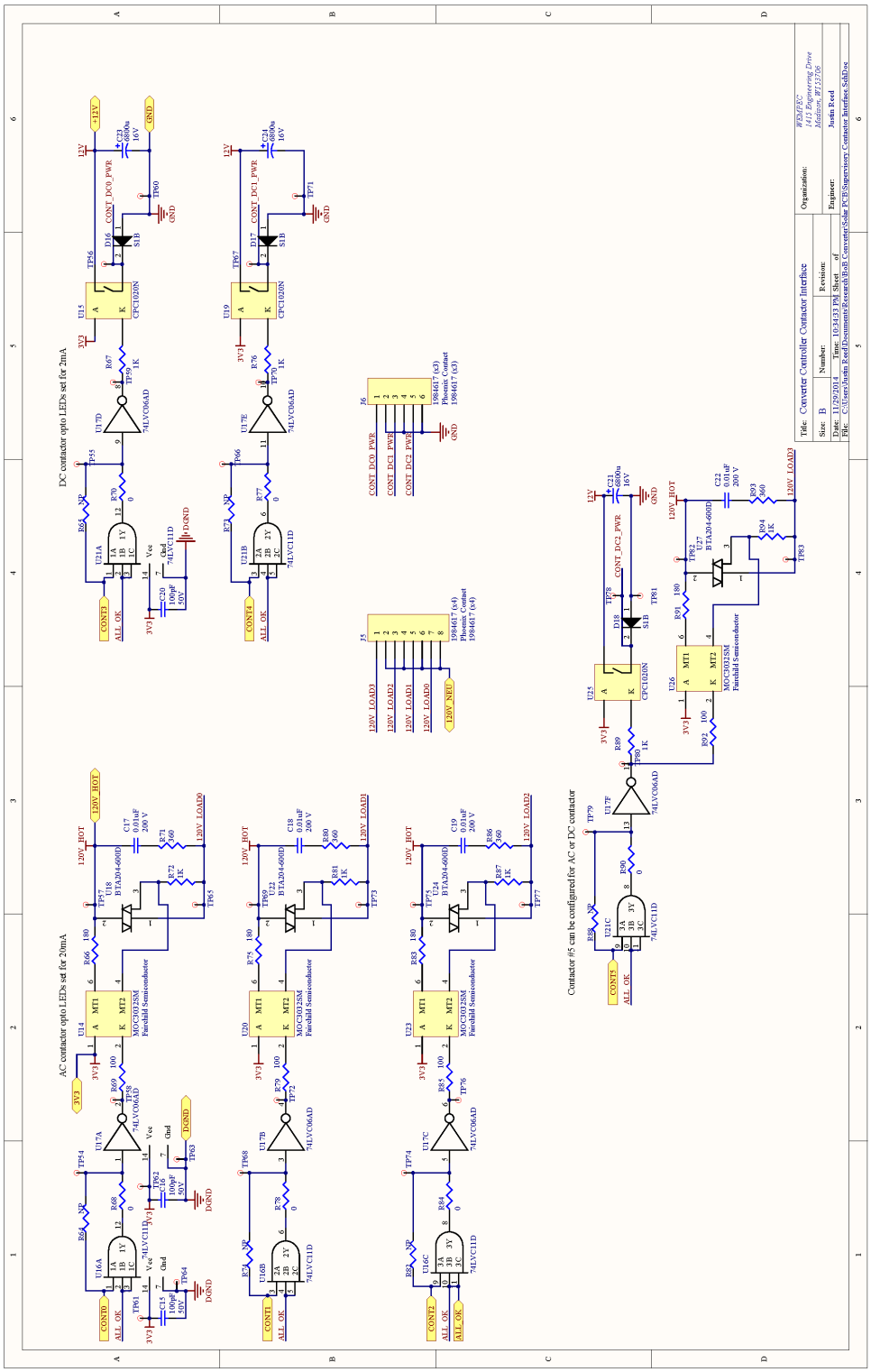
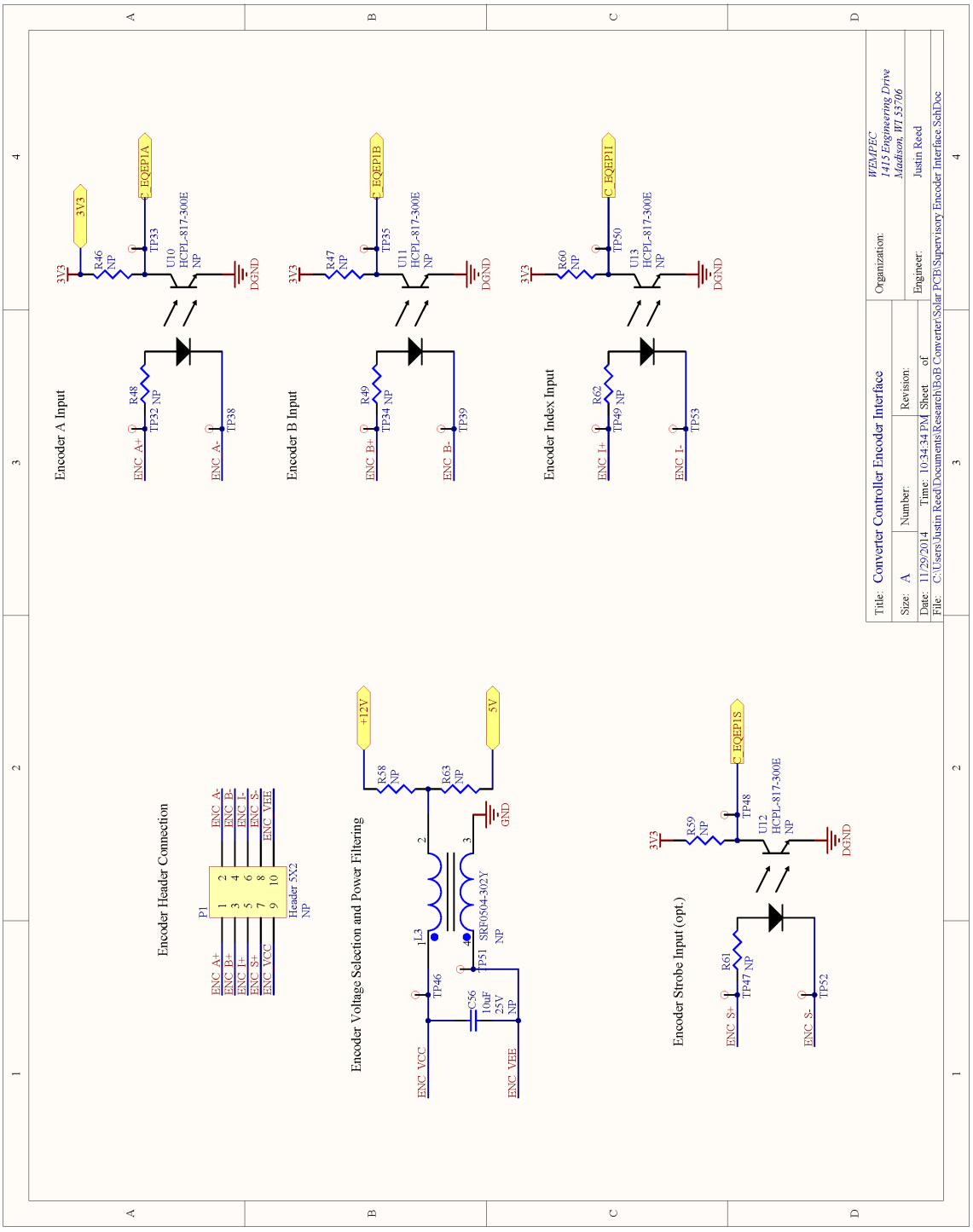
Organization: WESPEC
1415 Engineering Drive
Madison, WI 53706
Engineer: Justin Reed
Sense_VS
Sense_12V_Noniso
Sense_5V_Noniso
Sense_3V3
Sense_VS_Comp
Sense_Ib
Ib
Ib_Ref
4V_Ref
Ref_Gnd
VS
12V_Noniso
5V_Noniso
3V3_Noniso
5V
GND
5.7kHz Low-Pass Sallen-Key Filter (10 kHz -6Cf) 22nF, 50V Ceramic 10% CC1206KRX7R9BB223

E Converter Controller Schematics


TI Concerto DSP
5VSB @ 500mA
Housekeeping Power Supplies
Total: 5VSB @ 0.5A (2.5W) (Always On)
Total: 5V @ 2A (10W)
Total: +12V @ 2A (24W)
Total: -12V @ 0.5A (6W)
Total: 3.3V @ 235mA (0.78W)
Current and Voltage Sensing
+/- 12V @ 500mA
5V @ 0mA
AC and DC Contactor Interface
3.3V @ 90mA
12V @ 1.5A
Encoder Interface (optional)
3.3V @ 17.5mA
Primary CAN Communications Channel
Optional Secondary CAN Channel
Ground Connections
CAN Power Management
5V @ 1.5A
LED Outputs
3.3V @ 90mA
LEDs sink/source
Power loads are split across the LED drivers
Pushbutton Switch Inputs
Emergency Stop Switch
Unused, can be repurposed


AC contactor opto LEDs set for 20mA
DC contactor opto LEDs set for 2mA
Contactor #5 can be configured for AC or DC contactor
Converter Controller Contactor Interface
Justin Reed
Madison, WI 53706
120V_HOT
120V_NEU
120V_LOAD0
120V_LOAD1
120V_LOAD2
120V_LOAD3
120V_LOAD4
120V_LOAD5
CONT_DC0_PWR
CONT_DC1_PWR
CONT_DC2_PWR
MOC3023SM
BTA204-600D
CPC1020N
74LVC06AD
74LVC11D
74LVC1D
1984617 (x4)
1984617 (x3)


Encoder A Input
Encoder B Input
Encoder Index Input
Encoder Header Connection
Encoder Voltage Selection and Power Filtering
Encoder Strobe Input (opt.)
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Organization: WEMPEC 1415 Engineering Drive Madison, WI 53706
Engineer: Justin Reed
Size: A
Number:
Revision:
Date: 11/29/2014
Time: 10:34:34 PM
Sheet of
File: C:\Users\Justin Reed\Documents\Research\BoB Converter\Solar PCB\Supervisory Encoder Interface.SchDoc

Bibliography

[1] M. Cheney, *Tesla : man out of time*, 1st Touchstone ed. New York: Simon & Schuster, 2001.

[2] K. H. Edelmoser and F. A. Himmelstoss, "DC-to-DC solar converter with controlled active clamping system," in *EPE-PEMC 2006: 12th International Power Electronics and Motion Control Conference, August 30, 2006 - September 1, 2006*, Portoroz, Slovenia, 2006, pp. 124-127.

[3] A. Averberg and A. Mertens, "Design considerations of a voltage-fed full bridge DC-DC converter with high voltage gain for fuel cell applications," in *European Conference on Power Electronics and Applications*, Aalborg, Denmark, 2007, pp. 1-11.

[4] C. H. Willis, "Applications of Harmonic Commutation for Thyratron Inverters and Rectifiers," *American Institute of Electrical Engineers, Transactions of the,* vol. 52, pp. 701-707, 1933.

[5] P. C. Krause and T. A. Lipo, "Analysis and Simplified Representations of a Rectifier-Inverter Induction Motor Drive," *Power Apparatus and Systems, IEEE Transactions on,* vol. PAS-88, pp. 588-596, 1969.

[6] P. G. Kamp, M. Wolf, R. Gruber, and R. Schuster, "High power multilevel voltage source converters for the power supply of high speed trains," in *9th European Conference on Power Electronics and Applications*, Graz, Austria, 2001, p. 10.

[7] D. Vinnikov, M. Egorov, and R. Strzelecki, "Evaluative analysis of 2- and 3-level DC/DC converters for high-voltage high-power applications," in *Compatability and Power Electronics (CPE)*, Badajoz, Spain, 2009, pp. 432-7.

[8] D. Ludois and G. Venkataramanan, "An Examination of AC/HVDC Power Circuits for Interconnecting Bulk Wind Generation with the Electric Grid," *Energies,* vol. 3, pp. 1263-1289, 2010.

[9] F. Z. Peng, "Z-source inverter," *Industry Applications, IEEE Transactions on,* vol. 39, pp. 504-510, 2003.

[10] P. C. Loh, D. M. Vilathgamuwa, C. J. Gajanayake, Y. R. Lim, and C. W. Teo, "Transient Modeling and Analysis of Pulse-Width Modulated Z-Source Inverter," *Power Electronics, IEEE Transactions on,* vol. 22, pp. 498-507, 2007.

[11] R. H. Staunton, C. W. Ayers, L. D. Marlino, J. N. Chiasson, and T. A. Burress, "Evaluation of 2004 Toyota Prius Hybrid Electric Drive System," Oak Ridge National Laboratory, Oak Ridge, Tennessee 2006.

[12] D. C. Ludois, J. K. Reed, and G. Venkataramanan, "Hierarchical control of bridge-of-bridge multilevel power converters," *IEEE Transactions on Industrial Electronics,* vol. 57, pp. 2679-2690, 2010.

[13] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," in *IEEE Power Electronics Specialists Conference (PESC)*, Rhodes, Greece, 2008, pp. 174-9.

[14] C. Oates, "A methodology for developing `Chainlink' converters," in *Proc. 13th European Conference on Power Electronics and Applications (EPE)*, Barcelona, Spain, 2009, p. 10.

[15] R. Shimada, "Novel application of electric energy storage using flywheel/SMES," in *Conference Proceedings IPEMC 2004. The 4th International Power Electronics and Motion Control Conference, 14-16 Aug. 2004*, Xi'an, China, 2004, pp. 73-81.

[16] R. Marquardt, "Power Supply With A Direct Converter," US Patent 7269037, 2003.

[17] A. Antonopoulos, L. Angquist, and H. P. Nee, "On dynamics and voltage control of the Modular Multilevel Converter," in *13th European Conference on Power Electronics and Applications (EPE)*, Barcelona, Spain, 2009, pp. 1-10.

[18] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Pulse width modulation scheme for the modular multilevel converter," in *13th European Conference on Power Electronics and Applications (EPE)*, Barcelona, Spain, 2009, pp. 1-10.

[19] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Transactions on Industrial Electronics,* vol. 57, pp. 2633-2642, 2010.

[20] M. Glinka, "Prototype of multiphase modular-multilevel-converter with 2 MW power rating and 17-level-output-voltage," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (PESC)*, Aachen, Germany, 2004, pp. 2572-6.

[21] M. Glinka and R. Marquardt, "A new AC/AC-multilevel converter family applied to a single-phase converter," in *Fifth International Conference on Power Electronics and Drive Systems (PEDS)*, Singapore, 2003, pp. 16-23.

[22] M. Glinka and R. Marquardt, "A new single phase AC/AC-multilevel converter for traction vehicles operating on AC line voltage," *EPE Journal,* vol. 14, pp. 7-12, 2004.

[23] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Transactions on Industrial Electronics,* vol. 52, pp. 662-669, 2005.

[24] J. Hildinger and R. Marquardt, "Erzeugung stabilisierter hilfsspannungen aus dem leistungsteil von U-Umrichtern," in *Bauelemente der Leistungselektronik und ihre Anwendungen, Apr 23 - 24 2002*, Bad Nauheim, Germany, 2002, pp. 91-97.

[25] A. Lesnicar and R. Marquardt, "A new modular voltage source inverter topology," in *Proc. European Conference on Power Electronics (EPE)*, 2003.

[26] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *IEEE Bologna PowerTech, 23-26 June*, Bologna, Italy, 2003, p. 6.

[27] R. Marquardt, "Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-Bus-applications," in *International Power Electronics Conference (IPEC)*, Sapporo, Japan, 2010, pp. 502-507.

[28] R. Marquardt, "Modular Multilevel Converter topologies with DC-Short circuit current limitation," in *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on*, 2011, pp. 1425-1431.

[29] R. Marquardt and A. Lesnicar, "New Concept for High Voltage – Modular Multilevel Converter," in *Proc. German-Korean Symposium*, Aachen, Germany, 2004.

[30] R. Marquardt, A. Lesnicar, and J. Hildinger, "Modulares stromrichterkonzept fur netzkupplungsanwendungen bei hohen spannungen," in *Bauelemente der Leistungselektronik und ihre Anwendungen, Apr 23 - 24 2002*, Bad Nauheim, Germany, 2002, pp. 155-161.

[31] M. Hiller, D. Krug, R. Sommer, and S. Rohner, "A new highly modular medium voltage converter topology for industrial drive applications," in *13th European Conference on Power Electronics and Applications (EPE)*, Barcelona, Spain, 2009, pp. 1-10.

[32] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Analysis and simulation of a 6 kV, 6 MVA modular multilevel converter," in *35th Annual Conference of IEEE Industrial Electronics (IECON)*, Porto, Portugal, 2009, pp. 225-30.

[33] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modelling, Simulation and Analysis of a Modular Multilevel Converter for Medium Voltage Applications," in *IEEE International Conference on Industrial Technology (ICIT)*, Viña del Mar, Chile, 2010, pp. 775-82.

[34] S. Rohner, J. Weber, and S. Bernet, "Continuous model of Modular Multilevel Converter with experimental verification," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 4021-4028.

[35] G. P. Adam, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Modular multilevel converter for medium-voltage applications," in *Electric Machines & Drives Conference (IEMDC), 2011 IEEE International*, 2011, pp. 1013-1018.

[36] G. P. Adam, O. Anaya-Lara, and G. Burt, "Multi-terminal dc transmission system based on modular multilevel converter," in *Proc. 44th International Universities Power Engineering Conference (UPEC)*, Glasgow, UK, 2009.

[37] G. P. Adam, O. Anaya-Lara, G. Burt, and J. McDonald, "Transformerless STATCOM based on a five-level modular multilevel converter," in *Proc. 13th European Conference on Power Electronics and Applications (EPE)*, Barcelona, Spain, 2009.

[38] G. P. Adam, S. J. Finney, K. H. Ahmed, and B. W. Williams, "Modular multilevel converter modeling for power system studies," in *Power Engineering, Energy and Electrical Drives (POWERENG), 2013 Fourth International Conference on*, 2013, pp. 1538-1542.

[39] B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel VSC technologies for power transmission," in *IEEE/PES Transmission and Distribution Conference & Exposition*, Chicago, Illinois, 2008, pp. 993-1008.

[40] H.-J. Knaak, "Modular multilevel converters and HVDC/FACTS: A success story," in *Proceedings of the European Conference on Power Electronics and Applications (EPE)*, Birmingham, UK, 2011, pp. 1-6.

[41] D. C. Ludois, "Wind Farms with DC Collection Networks using Bridge of Bridge Multilevel Converters," PhD Thesis, Electrical and Computer Engineering, University of Wisconsin-Madison, Madison, 2012.

[42] A. Rasic, U. Krebs, H. Leu, and G. Herold, "Optimization of the modular multilevel converters performance using the second harmonic of the module current," in *13th European Conference on Power Electronics and Applications (EPE)*, Barcelona, Spain, 2009, pp. 1-10.

[43] S. P. Teeuwsen, "Simplified dynamic model of a voltage-sourced converter with modular multilevel converter design," in *2009 IEEE/PES Power Systems Conference and Exposition (PSCE 2009)*, Seattle, Washington, 2009, pp. 1-6.

[44] M. Winkelnkemper, A. Korn, and P. Steimer, "A modular direct converter for transformerless rail interties," in *Industrial Electronics (ISIE), 2010 IEEE International Symposium on*, 2010, pp. 562-567.

[45] H. M. Pirouz, M. T. Bina, and K. Kanzi, "A New Approach to the Modulation and DC-Link Balancing Strategy of Modular Multilevel AC/AC Converters," in *Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on*, 2005, pp. 1503-1507.

[46] H. Akagi, "Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)," *Power Electronics, IEEE Transactions on,* vol. 26, pp. 3119-3130, 2011.

[47] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascade PWM STATCOM with star configuration," *IEEE Transactions on Industry Applications,* vol. 43, pp. 1041-1049, Jul/Aug 2007.

[48] M. Hagiwara and H. Akagi, "PWM control and experiment of modular multilevel converters," in *IEEE Power Electronics Specialists Conference (PESC)*, Rhodes, Greece, 2008, pp. 154-61.

[49] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Transactions on Power Electronics,* vol. 24, pp. 1737-46, 2009.

[50] M. Hagiwara, K. Nishimura, and H. Akagi, "A modular multilevel PWM inverter for medium-voltage motor drives," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, 2009, pp. 2557-2564.

[51] T. Yoshii, S. Inoue, and H. Akagi, "Control and Performance of a Medium-Voltage Transformerless Cascade PWM STATCOM with Star-Configuration," in *Conference Record of the 41st IEEE Industry Applications Conference*, 2006, pp. 1716-1723.

[52] A. J. Korn, M. Winkelnkemper, P. Steimer, and J. W. Kolar, "Direct modular multi-level converter for gearless low-speed drives," in *Proceedings of the European Conference on Power Electronics and Applications (EPE)*, Birmingham, UK, 2011, pp. 1-7.

[53] A. J. Korn, M. Winkelnkemper, and P. Steimer, "Low output frequency operation of the Modular Multi-Level Converter," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 3993-3997.

[54] L. Angquist, A. Antonopoulos, S. Norrga, and H. P. Nee, "Arm-current-based control of modular multilevel converters," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-10.

[55] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H. P. Nee, "Inner control of Modular Multilevel Converters - An approach using open-loop estimation of stored energy," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 1579-1585.

[56] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H. P. Nee, "Open-Loop Control of Modular Multilevel Converters Using Estimation of Stored Energy," *Industry Applications, IEEE Transactions on,* vol. 47, pp. 2516-2524, 2011.

[57] A. Antonopoulos, L. Angquist, L. Harnefors, and H. P. Nee, "Optimal selection of the average capacitor voltage for modular multilevel converters," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 3368-3374.

[58] A. Antonopoulos, L. Angquist, S. Norrga, K. Ilves, and H. P. Nee, "Modular multilevel converter ac motor drives with constant torque form zero to nominal speed," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 739-746.

[59] A. Antonopoulos, K. Ilves, L. Angquist, and H. P. Nee, "On interaction between internal converter dynamics and current control of high-performance high-power AC motor drives with modular multilevel converters," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 4293-4298.

[60] L. Harnefors, S. Norrga, A. Antonopoulos, and H.-P. Nee, "Dynamic modeling of modular multilevel converters," in *Proceedings of the European Conference on Power Electronics and Applications (EPE)*, Birmingham, UK, 2011, pp. 1-10.

[61] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, L. Angquist, and H. P. Nee, "Capacitor voltage ripple shaping in modular multilevel converters allowing for operating region extension," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, 2011, pp. 4403-4408.

[62] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, "A New Modulation Method for the Modular Multilevel Converter Allowing Fundamental Switching Frequency," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 3482-3494, 2012.

[63] D. Peftitsis, G. Tolstoy, A. Antonopoulos, J. Rabkowski, L. Jang-Kwon, M. Bakowski, L. Angquist, and H. Nee, "High-Power Modular Multilevel Converters With SiC JFETs," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 28-36, 2012.

[64] D. Siemaszko, A. Antonopoulos, K. Ilves, M. Vasiladiotis, L. Angquist, and H. P. Nee, "Evaluation of control and modulation methods for modular multilevel converters," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 746-753.

[65] F. Kammerer, J. Kolb, and M. Braun, "A novel cascaded vector control scheme for the Modular Multilevel Matrix Converter," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, 2011, pp. 1097-1102.

[66] J. Kolb, F. Kammerer, and M. Braun, "Straight forward vector control of the Modular Multilevel Converter for feeding three-phase machines over their complete frequency range," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, 2011, pp. 1596-1601.

[67] J. Kolb, F. Kammerer, and M. Braun, "Dimensioning and design of a Modular Multilevel Converter for drive applications," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, 2012, pp. LS1a-1.1-1-LS1a-1.1-8.

[68] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded Control System of the Modular Multilevel Converter for Feeding Variable-Speed Drives," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2014.

[69] S. Rajasekar and R. Gupta, "Solar photovoltaic power conversion using modular multilevel converter," in *Engineering and Systems (SCES), 2012 Students Conference on*, 2012, pp. 1-6.

[70] L. Baruschka and A. Mertens, "A new 3-phase direct modular multilevel converter," in *Proceedings of the European Conference on Power Electronics and Applications (EPE)*, Birmingham, UK, 2011, pp. 1-10.

[71] J. Wang, R. Burgos, and D. Boroyevich, "A survey on the modular multilevel converters - Modeling, modulation and controls," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 3984-3991.

[72] M. Guan, Z. Xu, and H. Chen, "Control and modulation strategies for modular multilevel converter based HVDC system," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, 2011, pp. 849-854.

[73] H. Nademi, A. Das, and L. Norum, "An analytical frequency-domain modeling of a Modular Multilevel Converter," in *Power Electronics and Drive Systems Technology (PEDSTC), 2012 3rd*, 2012, pp. 86-91.

[74] S. Huang, R. Teodorescu, and L. Mathe, "Analysis of communication based distributed control of MMC for HVDC," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-10.

[75] J. Wang, E. Farr, R. Burgos, D. Boroyevich, R. Feldman, A. Watson, J. Clare, and P. Wheeler, "State-space switching model of modular multilevel converters," in *Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on*, 2013, pp. 1-10.

[76] J. Reed, G. Venkataramanan, and F. Martínez, "Complex Phasor Modeling and Control of Modular Multilevel Inverters," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Phoenix, AZ, 2011, pp. 4013-4020.

[77] P. Munch, S. Liu, and G. Ebner, "Multivariable current control of Modular Multilevel Converters with disturbance rejection and harmonics compensation," in *Control Applications (CCA), 2010 IEEE International Conference on*, 2010, pp. 196-201.

[78] H. Barnklau, A. Gensior, and S. Bernet, "Submodule capacitor dimensioning for Modular Multilevel Converters," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 4172-4179.

[79] H. Barnklau, A. Gensior, and J. Rudolph, "A Model-Based Control Scheme for Modular Multilevel Converters," *Industrial Electronics, IEEE Transactions on,* vol. 60, pp. 5359-5375, 2013.

[80] A. Hassanpoor, S. Norrga, H.-P. Nee, and L. Angquist, "Evaluation of different carrier-based PWM methods for modular multilevel converters for HVDC application," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 388-393.

[81] K. Ilves, L. Harnefors, S. Norrga, and H. Nee, "Analysis and Operation of Modular Multilevel Converters with Phase-Shifted Carrier PWM," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2014.

[82] Z. Li, P. Wang, H. Zhu, Z. Chu, and Y. Li, "An Improved Pulse Width Modulation Method for Chopper-Cell-Based Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 3472-3481, 2012.

[83] Q. Tu, Z. Xu, and L. Xu, "Reduced Switching-Frequency Modulation and Circulating Current Suppression for Modular Multilevel Converters," *Power Delivery, IEEE Transactions on,* vol. 26, pp. 2009-2017, 2011.

[84] Q. Tu, Z. Xu, and J. Zhang, "Circulating current suppressing controller in modular multilevel converter," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 3198-3202.

[85] A. Hassanpoor, K. Ilves, S. Norrga, L. Angquist, and H. P. Nee, "Tolerance-band modulation methods for modular multilevel converters," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-10.

[86] P. Munch, D. Gorges, M. Izak, and S. Liu, "Integrated current control, energy control and energy balancing of Modular Multilevel Converters," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 150-155.

[87] H. Fehr, A. Gensior, and M. Muller, "Analysis and trajectory tracking control of a modular multilevel converter," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2014.

[88] B. Riar, T. Geyer, and U. Madawala, "Model Predictive Direct Current Control of Modular Multilevel Converters: Modelling, Analysis and Experimental Evaluation," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2014.

[89] B. Riar and U. Madawala, "Decoupled control of Modular Multilevel Converters using Voltage Correcting Modules," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2014.

[90] S. P. Engel and R. W. De Doncker, "Control of the Modular Multi-Level Converter for minimized cell capacitance," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1-10.

[91] M. Saeedifard and R. Iravani, "Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System," *Power Delivery, IEEE Transactions on,* vol. 25, pp. 2903-2912, 2010.

[92] E. K. Amankwah, J. C. Clare, P. W. Wheeler, and A. J. Watson, "Multi carrier PWM of the modular multilevel VSC for medium voltage applications," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, 2012, pp. 2398-2406.

[93] J. Wang, R. Burgos, D. Boroyevich, and W. Bo, "Power-cell Switching-Cycle Capacitor Voltage Control for the Modular Multilevel Converters," in *Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), 2014 International*, 2014, pp. 944-950.

[94] X. Li, W. Liu, Q. Song, H. Rao, and S. Xu, "An enhanced MMC topology with DC fault ride-through capability," in *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, 2013, pp. 6182-6188.

[95] R. Lizana, M. Perez, J. Rodriguez, and W. Bin, "Modular multilevel converter based on current source H-bridge cells implemented with low cost reversing conducting IGCT," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 3363-3367.

[96] J. Reed and G. Venkataramanan, "Fault Tolerant MVDC-HVAC Power Converter for Wind Farm Applications," presented at the CIGRE Colloquium on HVDC and Power Electronic Systems, San Francisco, 2012.

[97] D. C. Ludois and G. Venkataramanan, "Simplified dynamics and control of Modular Multilevel Converter based on a terminal behavioral model," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 3520-3527.

[98] D. C. Ludois and G. Venkataramanan, "Simplified Terminal Behavioral Model for a Modular Multilevel Converter," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 1622-1631, 2014.

[99] G. S. Konstantinou and V. G. Agelidis, "Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques," in *4th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, Xi'an, China, 2009, pp. 3399-404.

[100] S. Angkititrakul and R. W. Erickson, "Control and implementation of a new modular matrix converter," in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, California, 2004, pp. 813-19.

[101] S. Angkititrakul and R. W. Erickson, "Capacitor voltage balancing control for a modular matrix converter," in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Dallas, Texas, 2006, pp. 1-7.

[102] R. W. Erickson and O. A. Al-Naseem, "A new family of matrix converters," in *27th Annual Conference of the IEEE Industrial Electronics Society IECON'2001, November 29, 2001 - December 2, 2001*, Denver, CO, United states, 2001, pp. 1515-1520.

[103] T. Isobe, J. A. Wiik, F. D. Wijaya, K. Inoue, K. Usuki, T. Kitahara, and R. Shimada, "Improved performance of induction motor using magnetic energy recovery switch," in *Power Conversion Conference (PCC)*, Nagoya, Japan, 2007, pp. 919-24.

[104] R. Shimada, J. A. Wiik, T. Isobe, T. Takaku, N. Iwamuro, Y. Uchida, M. Molinas, and T. M. Undeland, "A new AC current switch called MERS with low on-state voltage IGBTs (1.54 V) for renewable energy and power saving applications," in *Proceedings of the 20th International Symposium on Power Semiconductor Devices & ICs (ISPSD)*, Orlando, Florida, 2008, pp. 4-11.

[105] T. Takaku, G. Homma, T. Isober, S. Igarashi, Y. Uchida, and R. Shimada, "Improved wind power conversion system using magnetic energy recovery switch (MERS)," in *Conference Record of the IEEE Industry Applications Conference Fortieth IAS Annual Meeting*, Hong Kong, 2005, pp. 2007-12.

[106] J. A. Wiik, T. Isobe, T. Takaku, F. D. Wijaya, K. Usuki, N. Arai, and R. Shimada, "Feasible series compensation applications using Magnetic Energy Recovery Switch (MERS)," in *2007 European Conference on Power Electronics and Applications, EPE, September 2, 2007 - September 5, 2007*, Aalborg, Denmark, 2007.

[107] J. A. Wiik, A. Kulka, T. Isobe, K. Usuki, M. Molinas, T. Takaku, T. Undeland, and R. Shimada, "Control design and experimental verification of a series

compensated 50 kW permanent magnet wind power generator," in *IEEE Power Electronics Specialists Conference (PESC)*, Rhodes, Greece, 2008, pp. 4525-31.

[108] J. A. Wiik, A. Kulka, T. Isobe, K. Usuki, M. Molinas, T. Takaku, T. Undeland, and R. Shimada, "Loss and rating considerations of a wind energy conversion system with reactive compensation by magnetic energy recovery switch (MERS)," in *EPE Wind Energy Chapter (EPE-WECS)*, Delft, The Netherlands, 2008, pp. 15-20.

[109] J. A. Wiik, T. Takaku, F. D. Wijaya, T. Kitahara, and R. Shimada, "Improvement of synchronous generator charateristics using Bi-directional current phase control switch," in *EPE-PEMC 2006: 12th International Power Electronics and Motion Control Conference, August 30, 2006 - September 1, 2006*, Portoroz, Slovenia, 2006, pp. 1506-1511.

[110] J. A. Wiik, F. D. Widjaya, T. Isobe, T. Kitahara, and R. Shimada, "Series connected power flow control using magnetic energy recovery switch," in *Fourth Power Conversion Conference (PCC)*, Nagoya, Japan, 2007, pp. 983-90.

[111] J. A. Wiik, F. D. Wijaya, and R. Shimada, "Characteristics of the magnetic energy recovery Switch (MERS) as a series facts controller," *IEEE Transactions on Power Delivery,* vol. 24, pp. 828-836, 2009.

[112] F. D. Wijaya, T. Isobe, K. Usuki, J. A. Wiik, and R. Shimada, "A new automatic voltage regulator of self-excited induction generator using SVC magnetic energy recovery switch (MERS)," in *IEEE Power Electronics Specialists Conference (PESC)*, Rhodes, Greece, 2008, pp. 697-703.

[113] T. Isobe, T. Takaku, T. Munakata, H. Tsutsui, S. Tsuji-Iio, T. Matsukawa, and R. Shimada, "Fusion power supplies using magnetic energy recovery switch," in *21st IEEE/NPSS Symposium on Fusion Engineering (SOFE)*, Knoxville, Tennessee, 2005, pp. 1-4.

[114] T. Isobe, T. Takaku, T. Munakata, H. Tsutsui, S. Tsuji-Iio, and R. Shimada, "Voltage rating reduction of magnet power supplies using a magnetic energy recovery switch," 2006, pp. 1646-1649.

[115] T. Isobe, K. Usuki, N. Arai, T. Kitahara, K. Fukutani, and R. Shimada, "Variable frequency induction heating using magnetic energy recovery switch (MERS)," in *IEEE Power Electronics Specialists Conference (PESC)*, Rhodes, Greece, 2008, pp. 2139-45.

[116] R. M. Cuzner, R. D. Lorenz, and D. W. Novotny, "Application of nonlinear observers for rotor position detection on an induction motor using machine voltages and currents," in *Industry Applications Society Annual Meeting, 1990., Conference Record of the 1990 IEEE*, 1990, pp. 416-421 vol.1.

[117] M. J. Ryan, W. E. Brumsickle, and R. D. Lorenz, "Control topology options for single-phase UPS inverters," *Industry Applications, IEEE Transactions on,* vol. 33, pp. 493-501, 1997.

[118] D. W. Novotny and T. A. Lipo, *Vector control and dynamics of AC drives*. New York: Oxford University Press, 1996.

[119] V. A. Caliskan, O. C. Verghese, and A. M. Stankovic, "Multifrequency averaging of DC/DC converters," *Power Electronics, IEEE Transactions on,* vol. 14, pp. 124-133, 1999.

[120] S. R. Sanders, J. M. Noworolski, X. Z. Liu, and G. C. Verghese, "Generalized averaging method for power conversion circuits," *Power Electronics, IEEE Transactions on,* vol. 6, pp. 251-259, 1991.

[121] G. Strang, *Introduction to Linear Algebra*, 4th Edition ed.: Wellesley Cambridge Press, 2009.

[122] C.-T. Chen, *Linear System Theory and Design*, 3rd Edition ed. New York: Oxford University Press, 1999.

[123] P. Kundur, *Power System Stability and Control*: McGraw-Hill Professional, 1994.