# Topologies and Analysis of Capacitor Coupled DC-DC Converters

By

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# Abstract

The ongoing trends of higher utilization of renewable energy, emerging energy storage technology and accelerated adoption of electrical transportation are warranting DC-DC converters at higher power levels. While the field of DC-DC power converters is relatively mature at power levels reaching up to a few kW, converter designs at higher power are just emerging. Modularity, high voltage transfer ratio, high efficiency, bidirectional power transfer capability are important and highly desirable characteristics at these power levels.

DC-DC converter architectures suitable for high power such as resonant , full bridge or the dual active bridge all include magnetic transformer coupling between the input stage and output stage. However transformer design in these converters still remains a challenging problem with several non-linear scaling issues that need to be simultaneously optimized to reduce losses and maintain acceptable performance. The introduction of fast switching semiconductor devices has exacerbated this issue as higher transformer core loss at high switching frequencies make it difficult to appropriately size the transformer while simultaneously increasing power density. Additionally, the inherent mutual coupling effect between adjacent transformer windings makes these topologies less suited to multi-input or multi-output type of applications.

Capacitive coupling has been previously proposed as a method of wireless power transfer at GHz switching frequencies, nanofarads of air capacitance and watts of power. This thesis proposes a novel application of capacitive coupling characteristics operating at kHz-MHz switching frequencies, microfarads of capacitance and kilowatts of power. The traditional magnetic transformer coupling in the DC-DC dual active bridge topology is replaced by

capacitor coupling. There are two variants in the proposed topology -the capacitor coupled single active bridge and dual active bridge converter. These converters share many of the same characteristics of the transformer coupled single and dual active bridge converters. By eliminating the magnetic coupling from input to output capacitive coupled designs are well suited for higher switching frequencies and increased power density.

A review of the current state of the art in DC-DC converter technology leads to a key research objective of replacing magnetic coupling in the dual active bridge topology with capacitive coupling. The capacitor coupled single and dual active bridge converters are introduced and the steady-state and dynamic characteristics of both these topologies are detailed. A comparative evaluation with existing transformer coupled variants is performed to illustrate the strengths and shortcomings of the proposed topologies. The behavior of capacitor coupled converters during various fault scenarios is examined and grounding strategies appropriate for this non-isolated architecture are studied. A high voltage DC-DC converter based on the modular cascade capacitor coupled topology is constructed to verify the analytical model and measure performance characteristics and voltage scaling properties of the proposed topology.

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CHAPTER 1

# Introduction

The panel efficiency of production-scale photovoltaics is steadily improving [1] while global trends show a continuous drop in the projected price of utility scale solar power. This is accompanied by various other trends such as the increase in large-scale computing power represented by cloud computing, falling prices of electrical energy storage and consumer interest in electric vehicles. The net effect is that there is a growing demand for high power DC conversion systems. Modularity, high voltage transfer ratio, high efficiency, bidirectional power transfer capability are some of the desirable characteristics of DC-DC converters for these applications. This chapter provides an overview of the technology of DC-DC converters with particular attention to these features with a goal to identify the major trends and provide a stage for later research efforts.

## 1.1 Overview of step-up converter topologies

High voltage DC-DC converters are an important component in many renewable energy applications where the source usually operates at low voltage, high current while the output load requirement is high voltage, low current. The traditional solution to implement a DC-DC

converter with high voltage transformation ratio typically involves magnetic transformer with a high turns ratio. But with the increasing cost of magnetic transformer components, several transformer-less topologies have been proposed that can achieve high step up ratios with better dynamic performance at lower cost and size. This section provides a review of the state of the art of transformer coupled and transformer-less step-up DC-DC converter topologies. The power handling capability of such converters is directly influenced by the voltage transformation ratio.

Table 1.1: Classification of step-up voltage source DC-DC converter topologies

| Transformer-coupled | Transformer-less |
|---|---|
| Basic | Boost |
| Resonant | Quadratic |
| Dual Active Bridge | Switched capacitor |
| Multiconverter | Multilevel |
| | Multisource |
| | Capacitive wireless power |

## 1.2 Transformer coupled topologies

Transformers provide galvanic isolation between input and output of the converter, which is sometimes necessary due to regulatory concerns. Transformers can extend the voltage transformation ratio, which in turn reduces the loading and losses on the switching components. Transformer primary and secondary windings can be cascaded or paralleled to integrate multiple sources and loads.

### 1.2.1 Basic

The most common transformer coupled topologies are derived from isolated versions of the basic converter types-buck, boost, buck-boost, cúk, SEPIC [2]. Forward converter is based on the buck topology and flyback converter is based on the buck-boost topology. Full-bridge, Half-bridge converters can be both buck and boost derived. The converter types can classified based on the transformer core utilization [3]. Forward and flyback topologies have a net DC

current in the transformer winding which means the flux in the core must be reset at the end of each switching cycle. Full bridge, half bridge and push pull topologies provide bidirectional excitation to the transformer core and the net current in the winding is AC. This means that the flux in the core is reset automatically at the end of each switching cycle.

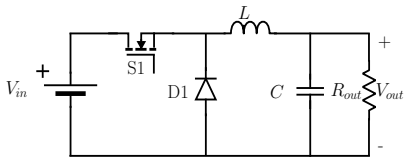


Figure 1.1: Power stage schematic of buck converter

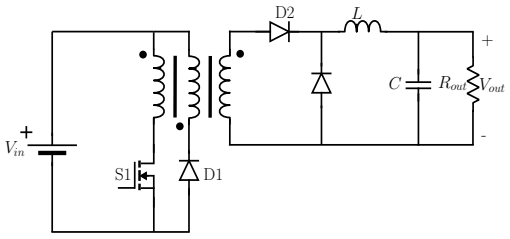


Figure 1.2: Power stage schematic of buck derived forward converter

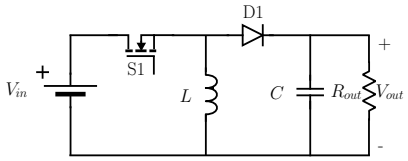


Figure 1.3: Power stage schematic of buck-boost converter

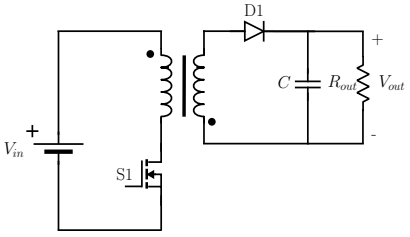


Figure 1.4: Power stage schematic of buck-boost derived flyback converter

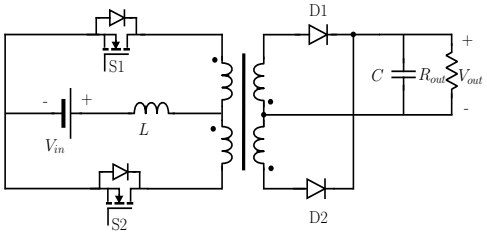


Figure 1.5: Power stage schematic of push pull boost converter

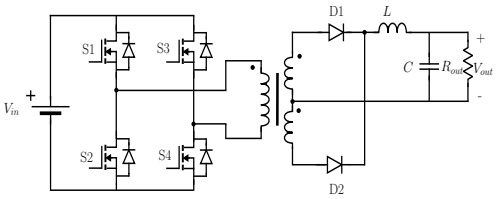


Figure 1.6: Power stage schematic of full bridge buck converter

### 1.2.2 Resonant

The concept of using resonant properties of LC networks for power conversion was proposed as early as [4, 5] when it was realized that the sinusoidal currents and voltages in a resonant

converter allow for higher voltage transformation ratio while simultaneously reducing switching losses because of zero voltage switching (ZVS) and/or zero current switching (ZCS). The basic block diagram of a resonant DC-DC converter is shown in Fig 1.7. The inverter stage is usually a Class D or Class E type inverter. Some of the possible variation of the resonant network are shown in Fig 1.8. The high frequency rectifier stage can be passive (half wave, center-tapped half wave, full wave) or active with switching devices. Some designs eliminate the high frequency transformer and replace it with a parallel capacitor [6].

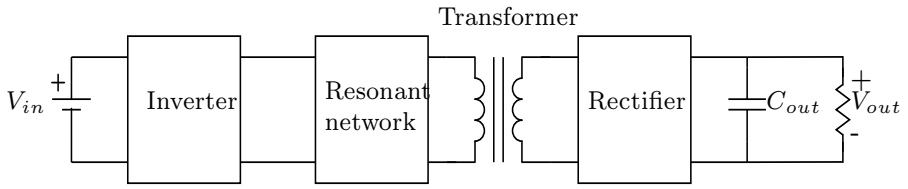


Figure 1.7: Block diagram of the power stage of a resonant DC-DC converter

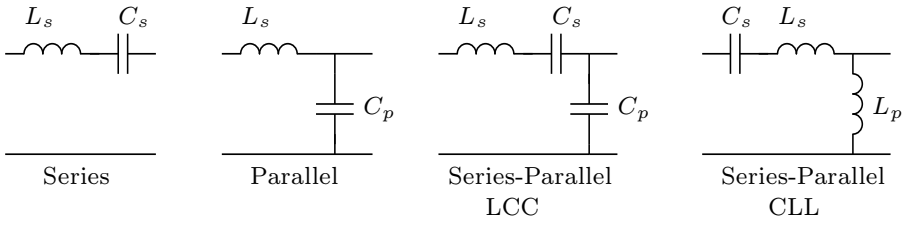


Figure 1.8: Resonant network variations [7]

Resonant converters can be classified based on the order of the resonant network (2nd order, 3rd order etc.) or based on the control algorithm on the inverter stage (frequency control, phase control, optimal trajectory control etc.)[8]. The simplest and most widely used is Frequency control -the power flow of the converter is adjusted by changing the switching frequency closer and away from the resonant frequency of the LC network [9]. The disadvantages of wide frequency operation are well known -EMI issues [10], higher switching loss at low power levels, difficulty in design of magnetic components [11] and circulating currents independent of power level. Phase controlled converters operate at fixed frequencies and adjust the power flow by varying the phase shift between the switching legs of a full-bridge inverter[8, 12].

However, the phase shift will also create assymetric currents at the switching instants between the two legs of a full-bridge inverter. Optimal trajectory control is based on the state-space representation of a resonant converter. The optimal current and voltage trajectories of the converter states are calculated to minimize the energy of the resonant tank network [13, 14]. When compared to frequency control, optimal trajectory control has better startup [15] and dynamic performance since $v$, $i$ trajectories are directly controlled . However the operating frequency will still vary with the load conditions and this method can control the converter only under CCM conditions.

Since the variable frequency operation of resonant converters is a major downside, there have been several attempts to operate resonant converters at fixed frequency by utilizing an additional matching network at the input or output of the resonant network. The effect of these additional networks is to provide an effective impedance that is purely resistive at the resonant frequency [16, 17]. Since resonant converters operate at ZVS or ZCS, conduction losses are the major component of semiconductor loss. Gallium Nitride (GaN) devices have lower output charge $Q_{OSS}$ and lower gate charge $Q_G$ compared to Si devices which further reduces conduction loss compared to Si [18, 19]. There have also been some attempts to operate resonant converters with higher DC bus voltages [20, 21] and higher order resonant networks [22].

### 1.2.3 Dual Active Bridge

Dual Active Bridge (DAB) converters were first introduced by [23, 24] as an alternative to resonant and pseudo-resonant DC-DC topologies for high power applications. DAB converters consist of two voltage-source full-bridge converters connected by a series inductance and isolated by a high frequency(HF) transfomer as shown in Fig 4.16. The high frequency transformer can be either single phase or three phase depending on the application. A three phase DAB has lower current ripple, slightly higher efficiency and better transformer utilization at the cost of more switching devices [25, 26]. The DAB topology eliminated the large output filter inductor present in previous configurations and introduced a smaller inductance in series with

the HF transformer. For high switching frequencies, this series inductance is small enough that it can made part of the leakage inductance of a suitably designed HF transformer thereby reducing the size and component count. The presence of active bridges at both primary and secondary allows for bidirectional power transfer operation with zero voltage switching along the control range defined in [24].

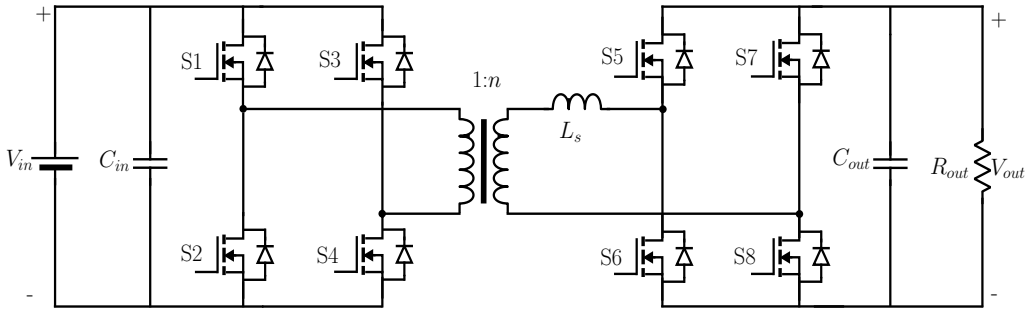


Figure 1.9: Power stage schematic of transformer coupled dual active bridge converter [27]

The basic operating characteristics of DAB were enumerated by [23, 24, 27] and the optimal design constraints with respect to efficiency, power density etc. were explored by [28–32]. DAB converter design was modeled as an optimal design problem with the high frequency transformer turns ratio and the series inductance as the main factors that affected the designed efficiency. The effect of modulation strategy on the converter efficiency was explored by [30, 33–36], where it was shown that the optimal modulation scheme was one with the lowest rms current in the transformer while still maintaining ZVS on the primary and seconary converters.

The most direct approach to increase the power tranfer capability of the DAB converter is to operate at higher primary and secondary voltages [37, 38] with the attendant difficulty in transformer insulation and reduced switching frequency, though the introduction of SiC switching devices has recently allowed for higher switching frequencies. The second approach is a cascaded modular architecture where multiple full bridge converters both on the primary and secondary side can be connected in series or parallel combination to increase the power rating of the converter without increasing the VA rating of the switching devices and passive components[39, 40]. The trade-off here is that control complexity necessitates the use of

distributed controller. But in both cases, the transformer design is not a trivial problem, especially when the voltage conversion ratio is greater than 1:2 or 1:3 [41]. Transformers in bidirectional converters are also susceptible to saturation, which requires passive or active methods for flux balancing [42]. Even for low power application, higher switching frequencies can cause problems in magnetic components.

### 1.2.4 Multiconverter

Modular DC-DC converters with input and output side series/parallel configurations are typically used for conditions where the power processing exceeds the capacity of any one single converter. All of these configurations are supported by transformer windings to reconfigure the input and output sides as required for each application. The input-parallel output-series (IPOS) converter architecture is suitable for photovoltaic applications. The conventional approach to achieve input parallel operation involve use of coupled inductor boost configuration on the input side [43], and transformer-isolated configuration for series connection on the output side [44, 45].

The input-parallel output-parallel (IPOP) architecture improves the light-load efficiency of the converter by phase shedding [46]. Since all the converters operate in parallel, IPOP converters can scale with load conditions and operate at high efficiency over wider range [47, 48]. Input-series output-parallel (ISOP) architecture as shown in Fig 1.10 is most often used to interface high voltage DC to low voltage loads [49, 50]. The most commonly used DC-DC converter topology in all such cases is the single active bridge or dual active bridge converter. The problems with this multiconverter architecture are control-related, ensuring proper power share between the constituent converter modules for wide load conditions.

## 1.3 Transformer-less topologies

Transformer-less switching mode DC-DC converters are an old concept, proposed as early as [51] when it was quickly realized that the basic boost topology has significant disadvantages

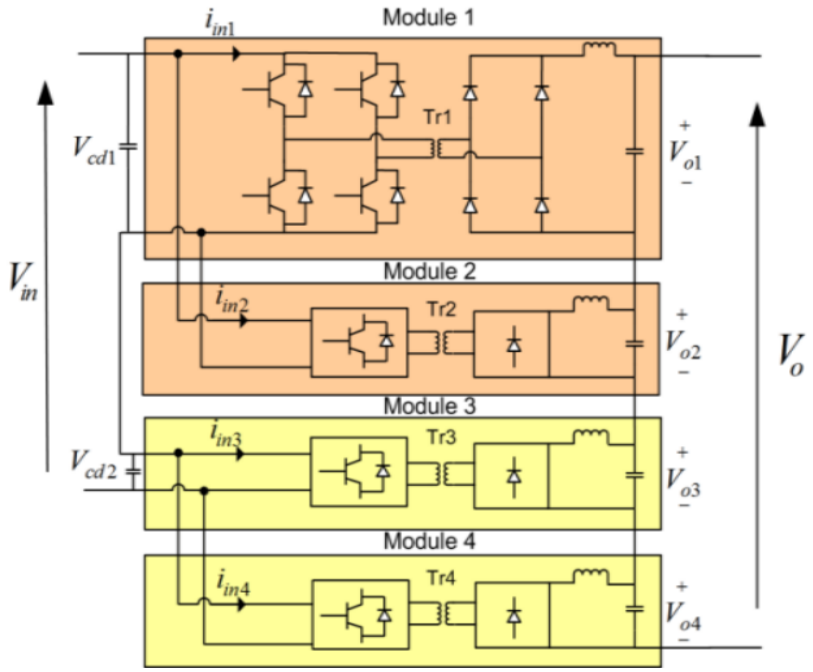


Figure 1.10: An IPOS modular DC-DC converter architecture [45]

when the desired voltage conversion ratio is greater that 1:3 or 1:4. Many transformer-less converter topologies are also modular and can achieve arbitrary conversion ratios by cascading or series-parallel connection of appropriate number of stages. The following subsection provides a brief overview of such topologies.

### 1.3.1 Boost and boost derived

The boost topology is one of the basic non-isolated converter topologies with an ideal voltage conversion ratio [52]

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{1.1}$$

where $D$ is the duty ratio of the active switch. However, the actual conversion ratio is much lower when the effect of inductor equivalent series resistance $R_L$, diode forward voltage drop $V_D$, diode forward resistance $R_d$, switch on-state resistance $R_{on}$ are accounted [2]. The effect of all these non-idealities is that the voltage gain from input to output is rarely more than 1.5

to 2.

$$\frac{V_{out}}{V_{in}} = \left(\frac{1}{1-D}\right)\left(1-\frac{(1-D)V_D}{V_{in}}\right)\left(\frac{1}{1+\frac{R_L+DR_{dson}+(1-D)R_d}{(1-D)^2R}}\right) \tag{1.2}$$

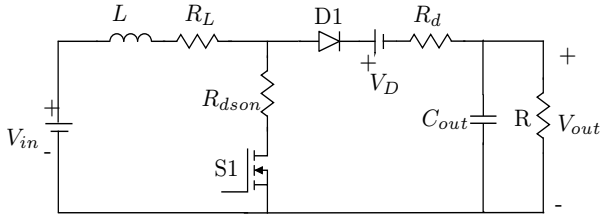


Figure 1.11: Realisitic boost converter non-idealities

Several modifications have been proposed to improve the voltage transformation ratio and power handling capability of the boost converter [53–55]. One way to improve the voltage transformation ratio is to use a tapped inductor with two windings and turns ratio 1:N [56–58]. A significant disadvantage of the boost topology is its single switch topology with input current handling capability constrained by the active switch rating. To improve the current handling capability, interleaving techniques are used to parallel several boost converters at the input [59–61]. The additional inductors can be on different magnetic cores or share the same core. The diode-capacitor combination of a typical ladder-type voltage multiplier cell can be combined with the boost topology to achieve high gain [62]. It is also possible to combine multiple techniques and achieve high gain along with other desirable properties [63–66]. Hybrid topologies that combine switched capacitor and switched inductor structures also exist [67]. [68] gives a good overview of boost modified topologies suitable exclusively for photovoltaic applications.

### 1.3.2 Quadratic

Quadratic converters are DC-DC converters with a voltage conversion ratio that has a quadratic dependence on duty ratio [69]. They are synthesized by cascading two converters in series and then eliminating redundant switches and controllers [70]. From a two stage cascaded boost converter of Fig 1.12, the quadratic boost converter of Fig 1.13 is obtained

by replacing switch S1 with diode D2 to obtain a single switch converter. The ideal voltage conversion ratio of the quadratic boost converter is

$$\frac{V_{out}}{V_{in}} = \frac{D^2}{(1-D)^2} \tag{1.3}$$

The obvious advantage is higher voltage transformation ratio with reduced number of components. The problems of this topology all stem from the cascaded nature of the converter from which it is derived. The combined efficiency is lower than the individual converter stages and the voltage stresses on the boost diode and switch of the final stage are equal to output voltage. Some of these problems can be solved by adding an additional switch to form a three level boost converter [71]. Many other structures can also be integrated with quadratic converters like the capacitor-diode combination of the voltage multiplier [72] or single-phase/three-phase transformer windings [70]. There are other variations like the quadratic boost zeta converter [73], quadratic tapped-boost converter [74], ZVS/ZCS quadratic converters [75] and quadratic converters based on non-cascading structures [76].

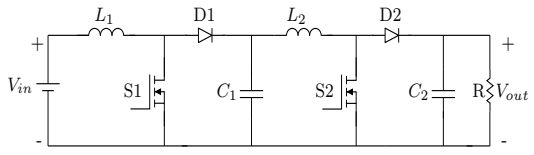


Figure 1.12: Cascaded boost converter with two active switches

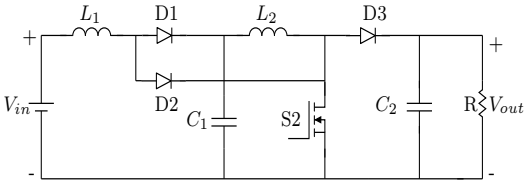


Figure 1.13: Single switch quadratic boost converter

### 1.3.3 Switched capacitor

Swiched capacitor (SC) converters are a class of DC-DC converters where the power stage consists of a network of only capacitors and switches as shown in Fig 1.14-1.17 [77]. The capacitors are charged and discharged in sequence by the input voltage to achieve the required voltage conversion ratio at the output [78]. The biggest advantage is that the absence of inductive storage devices makes this topology very suitable for monolithic integration and high power density as both the switches and capacitors can be fabricated on the same substrate

using standard semiconductor manufacturing processes. The disadvantage is that since the capacitors act as charge pumps, the process of charge transfer results in impulse currents which will increase device stress and EMI issues. Another disadvantage is that the voltage transformation ratio is fixed the efficiency of the converter drops quickly as the conversion ratio moves away from the designed operating mode. An additional complication is that the voltage stress across all the active switches is not equal.

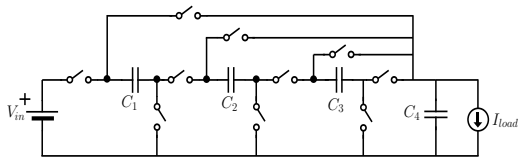


Figure 1.14: Power circuit schematic of series parallel type switched capacitor topology

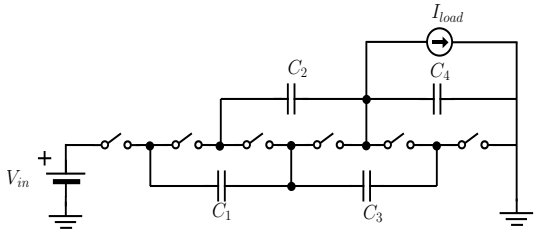


Figure 1.15: Power circuit schematic of ladder type switched capacitor topology

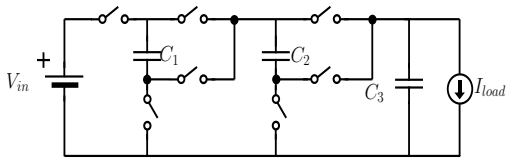


Figure 1.16: Power circuit schematic of fibonacci type switched capacitor topology

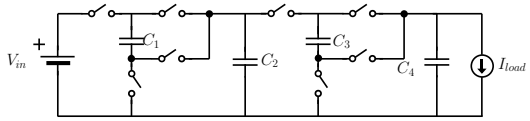


Figure 1.17: Power circuit schematic of doubler type switched capacitor topology

One approach to handle wide operating conditions is to have a two stage converter, with the switched capacitor stage providing a fixed conversion ratio and and an auxiliary low frequency power converter (buck or boost) with wide operating range providing the regulated output [79, 80]. There is always a fixed loss called the charge sharing loss that is independent of the resistance in the charge path and proportional to the voltage difference. By having a high frequency switching auxiliary converter (or a small inductor) in series with the output stage capacitor to act as a current load, this charge loss can be eliminated and also operate the SC at higher voltage ripple without affecting the efficiency. This technique called soft charging is used to eliminate the current transients [77, 81, 82]. A second way to avoid the charge loss is to operate at resonant conditions which can also eliminate the switching loss. However, resonant

conditions require one or more inductors in the charge path [83–86]. Another technique to operate at wide input/output voltage range is to utilize a reconfigurable topology that provides multiple specific conversion ratio and operate the converter at the mode that is closest to the desired output voltage [87, 88]. Modular mulitlevel structures are also applied to switched capacitor designs to produce structures similar to flying capacitor DC-DC converters [89, 90].

### 1.3.4 Multilevel

The chief limitation to achieving higher voltage and power levels is the ratings of the power semiconductor devices do not support very high voltage or power levels at a reasonable cost. Voltage-sourced multilevel converters overcome this limitation by stacking multiple levels of low voltage power semiconductor devices and synthesizing the output high voltage using these discrete low levels. Multilevel topologies offer less harmonic distortion, lower EMI and lower voltage stress on devices when compared with equivalent unilevel topologies since the blocking voltage levels at each stage is lower than the output voltage [91]. Multilevel converter topologies were originally developed for DC-AC inverter applications but they can also be used for DC-DC applications. There are traditionally three types of single source multilevel converter structures - diode-clamped, capacitor-clamped and modular.

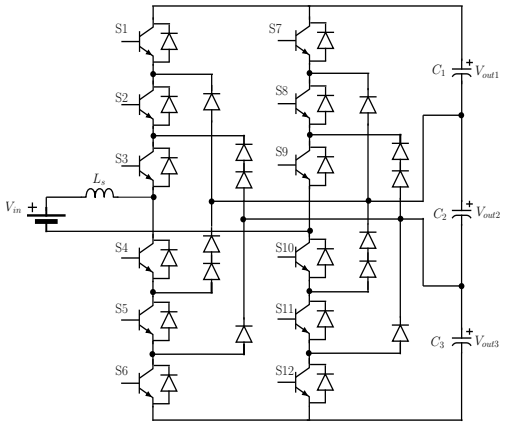


Figure 1.18: Four level diode-clamped DC-DC converter [91]

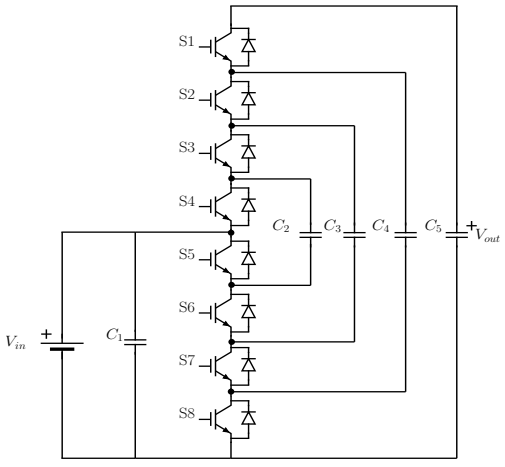


Figure 1.19: Four level capacitor-clamped DC-DC converter with common grounding [92].

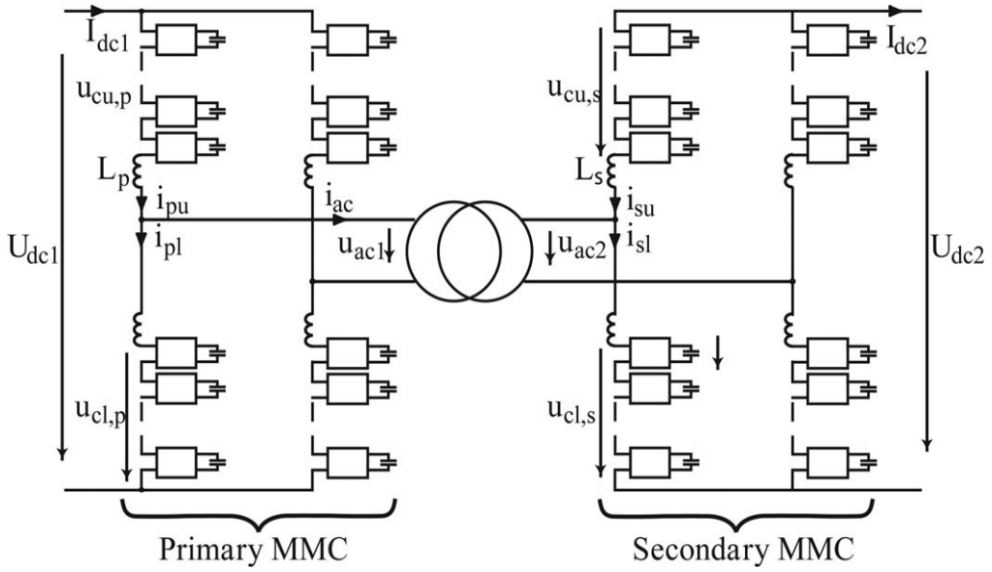


Figure 1.20: Modular multilevel converter architecture [93]

The diode clamped multilevel converter is derived from the neutral-point clamped inverter and is not suitable for DC applications since it difficult to balance the all various voltage levels without AC waveforms [91]. Capacitor-clamped (or flying-capacitor) converter is a variation of the switched capacitor converter and was originally proposed by [94] to reduce the size and weight of a high voltage DC DC converter. Capacitors at different voltage levels are used to transfer energy from the high voltage side to the low voltage side or vice versa as shown in Fig 1.19. For unidirectional operation S1-S4 can be replaced with diodes [95]. The topology has natural voltage balancing property where the excessive voltage unbalance between the capacitor levels is dissipated by switching harmonics [96]. The topology initially eliminated all magnetic components and operated at simple fixed duty ratio with no pulse width modulation, but new variations have proposed better efficiency by introducing coupled inductors and operating the active swithing devices under PWM ZVS conditions [97]. The limitations of the flying capacitor structure are due to the high part count, non-modular structure that cannot be easily extended and a complicated switching scheme as the number of levels is increased [92].

The modular multilevel converter was proposed by [98] specifically as an interface between AC grid and HVDC loads. The modular multilevel converter consists of several identical modules which are connected in series and operated as controllable current sources to modulate power throughput via voltage and current of each module. Each module can behave as a voltage source or current source, with either half-bridge or full bridge configuration along with a series inductor and parallel capacitor [99]. All semiconductor devices are rated for low voltage while the final output voltage is a series-parallel combination of the individual modules. Similar to the case of other multilevel converter, the modular multilevel converter was proposed for AC-DC applications and re-purposed for DC-DC applications [93, 100, 101]. The biggest issue with this architecture is the requirement to balance the energy in every sub module for stable converter behavior. This balance is expressed in terms of capacitor voltage balance within the modules. Another issue is converter modeling and synchronization of the various modules for optimum switching behavior [99].

### 1.3.5 Multisource

Most of the renewable energy sources as well as many energy storage devices operate at low DC voltages while most loads are rated for medium voltage AC. Cascaded H-bridge converters provide a topology to interface numerous DC sources together via series connection of independent H-bridges to synthesize the output waveform as sum of the individual sources[102]. This architecture has found many applications in interfacing distributed photovoltaic solar panels with grid connected applications [103]. The simplest and most widely used modulation scheme is the conventional phase shift modulation method where the power flow is modulated by varing the phase displacement between consecutive H-bridges. The challenge with this topology is that power imbalance between the series connected low-bandwidth DC sources will affect the final output voltage by introducing unwanted harmonics [104]. One method to mitigate such issues is to introduce high bandwidth auxillary sources comprised of capacitors to balance the harmonics [105]. Other techniques involve more sophisticated PWM techniques [106].

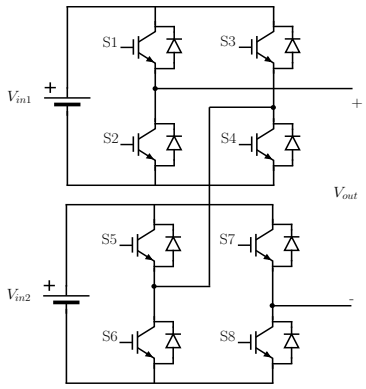


Figure 1.21: Cascaded H-bridge converter with two independent sources

### 1.3.6 Capacitive wireless power transfer

Wireless power transfer using electromagnetic induction principles have been researched since the dawn of the electrical age [107, 108]. Most of the research interest in the previous decade has been centered around magnetic inductive power transfer techniques, which consist of two magnetic coils separated by an air gap with the power being transferred via the induced magnetic field between the primary and secondary coil [109, 110]. More recently, wireless electrostatic induction has emerged as a viable alternative. Here power is transferred via an induced electric field applied between two conductive plates situated close to each other and separated by an air gap or an insulating dielectric. Magnetic induction operates with a larger air gap and at higher power, while electrostatic induction shines at low gap distances and until now at low power [111]. There are specific applications where capacitive power transfer is more suitable than magnetic power transfer - such as low power close range wireless charging [112], power transfer via bearing [113, 114], power transfer via bumpers [115] and chip-level power transfer[116]. Capacitive power DC-DC topologies are based on resonant [117], class E [115] or modified buck-boost [118] type topologies. This allows these converters to operate at switching frequencies in the range of GHz and with very low coupling capacitance in the range of pF.

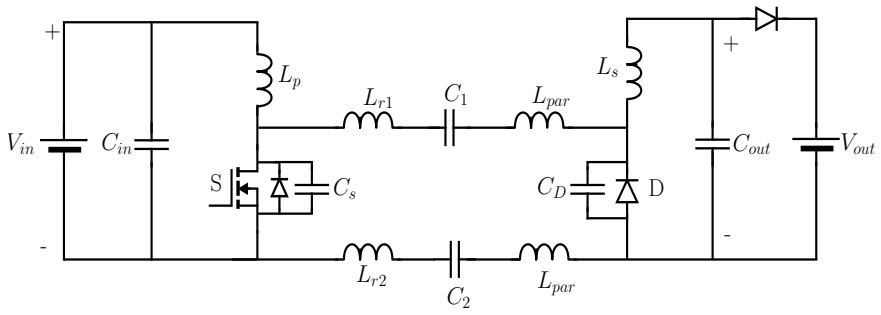


Figure 1.22: Capacitive coupled class $E^2$ type topology [115]

## 1.4 Fault detection and protection

The fault response of DC-DC converters has become a very active research area with the proliferation of HVDC transmission networks and the increase in voltage and power capabilities of such networks . There has been ongoing research in the area of protection specific to the requirements of HVDC systems with most attention focused on DC microgrid coordination and protection [119–122]. The inherent disadvantage of any DC-DC transmission system is that DC fault current interruption is complicated when compared to AC current of same magnitude. This is because AC fault current will naturally become zero instantaneously within a power cycle which helps to quench the arcs when the circuit breaker contacts disengage. Since instantaneous DC fault current amplitude never becomes zero the fault current interrupter must be capable opening with a non-zero fault current and withstand the stored energy in the line and in any passive elements in the fault path. There are basically three types of fault current interrupters or DC circuit breakers classified based on voltage rating and speed of operation [123]

- Mechanical - consist of a low resistance mechanical contacts that touch and conduct current in normal conditions and separate under fault conditions. They can sometimes include LC resonant circuit in parallel to force current to zero [124]. The DC arc current can sometimes be also quenched using explosive fuses [125]. They are typically slow acting with switching times in the range of 30-100ms.

- Solid state - consist of circuit breakers constructed from semiconductor switches (IGBT, IGCT, SCR etc.) that are are turned on during normal conditions and turned off under fault conditions. These switches are typically fast and can switch in a few microseconds [126–128] without any of the arcing issues associated with mechanical switches. However, the series resistance of solid state switches (m$\Omega$) is typically higher than mechanical switches ($\mu\Omega$).

- Hybrid - this is the latest category of DC circuit breakers which consist of a parallel combination of semiconductor switch and mechanical switch [129–131]. The mechanical switch is used for normal operation while the semiconductor switch operates only under fault condition.

Transformers provide galvanic isolation between the input side and output side. The consequence of this isolated coupling is that ground faults occuring on one side of the galvanic boundary have no effect on the circuit on the other side. This can significantly limit the effect of converter faults. Transformer-less topologies do not have this separation and faults need to be managed both at the input and output side.

## 1.5 Summary of review

The previous sections briefly identify the current state of the art in DC-DC converter topology. Although there is a great variety of converter types, with huge variations in operating frequencies, power levels and target application space, it is still useful to classify DC-DC converters into these broad categories of transformer-coupled and transformer-less converters. The discussion in the previous section can be summarized into a few key points.

**DC-DC converters operating at higher power** The present application space of DC-DC converters is mostly confined to low power, high frequency power supplies that are ubiquitous in all modern electronic devices. Most of the application space of power converters is dominated by high power, low frequency variable frequency drives. This is changing

with DC-DC converters appearing as solutions for smart transformer applications in HVDC and MVDC power supplies.

**Increasing popularity of modular converters** Modular converters refer to a category of converters where the total power demand is shared among several stages in a multilevel, multisource or multiconverter configuration. As shown by the preceding section, modular converters have several advantages when compared to a single monolithic converter that handles all the power conversion -they are more robust, reliable, can operate at high efficiency throughout the full load range. They can also be cheaper when its taken into account that monolithic converters require semiconductor devices of much higher power ratings. On the flip side, most modular converters have to balance the local state variables such as capacitor voltage, inductor current etc in addition to the terminal variables of output voltage and current.

**Higher switching frequencies** One of the major advances in power electronics in the last five years is the rise of IV and III-V semiconductor materials like SiC and GaN. These new materials have very low switching loss which means that higher switching frequencies are more easily realized.

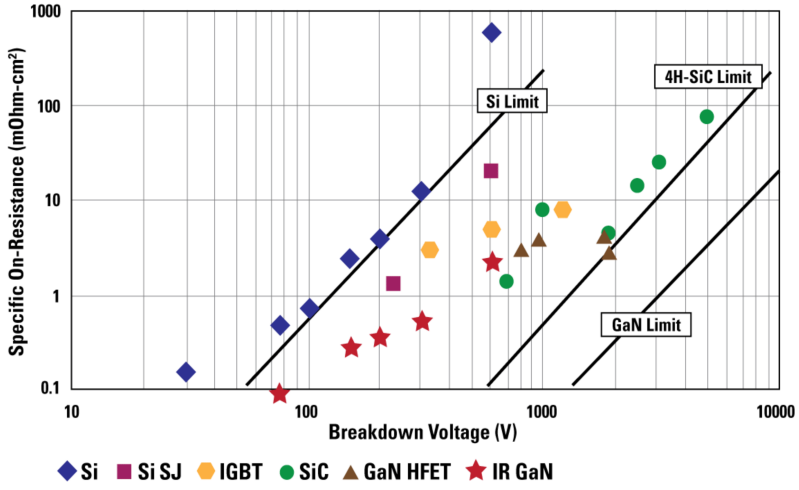


Figure 1.23: Comparion of $R_{dson}$ for Si, SiC and GaN [132]

**Critical role of transformers** The only DC-DC converter topologies that have found popular use at power level over 5kW such as resonant converter, full bridge converter or the dual active bridge converter all include a magnetic transformer coupling in their design. The turns ratio of a high frequency transformer winding provides a simple and effective means to step-up or step-down voltages and currents.

**Challenges in transformer design** At low power [133], medium power [30] or high power [134], transformer design is a hard problem with several non-linearites that need to be optimized simultaneously to reduce losses and maintain acceptable performance. There are also operational difficulties such as flux saturation, DC bias, mutual coupling that also need to be accounted in transformer designs.

**Challenges in multiple inputs and outputs transformer coupled topologies** There are a number of low power distributed DC loads gate drive power supplies, LED power supplies, cooling and housekeeping power supplies. These loads are typically serviced using a flyback, forward, push-pull or full bridge topology with multiple isolated outputs derived from multiple windings of a single transformer [135]. The disadvantage here is that transformer design is complicated and construction with multiple secondary windings is typically bulky. Transformer isolated converters require snubber circuits to mitigate large voltage spikes across the main switches on turn off [136]. Another common issue is cross-regulation, the transformer winding causes mutual coupling between the different isolated outputs which makes precise independent regulation of each DC output very complicated [137, 138]. This is usually mitigated by adding a post regulator stage in the form of a linear regulator or a PWM switching regulator for each output [139, 140] or by complex modulation strategies [141, 142].

**Challenges with high frequency transformer design** As the Fig 1.24 shows, increase in switching frequency is not reflected in the transformer designs. This reason for this discrepancy can be seen in the Fig 1.25 where the core loss per $cm^3$ is plotted for three high frequency magnetic materials. Core loss is an exponential power of frequency for

all soft magnetic materials. Although there are design mitigations that are available for managing the core loss, it is a certain fact that core loss will be a limiting factor for small, power dense designs.

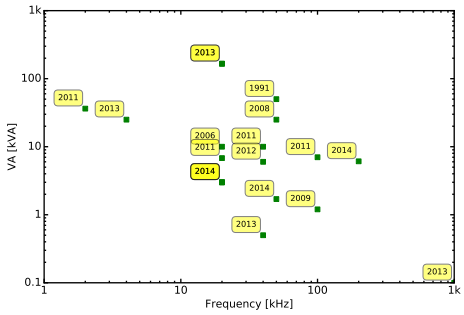


Figure 1.24: Sample survey of transformer designs from past 20 years

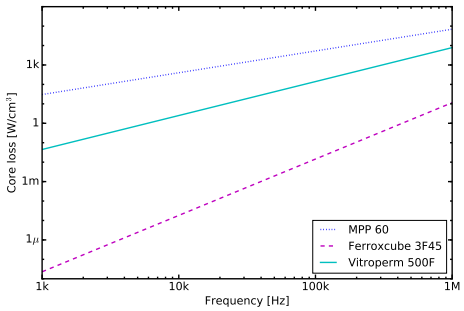


Figure 1.25: Estimated core loss in soft magnetic materials

**Attractiveness of dual active bridge topology** The DAB converter topology is one of the few topologies that can operate at high power and high efficiency along with bidirectional power capability. Another significant advantage of this topology is that compared to other transformer-coupled topologies, the DAB converter is insensitive to transformer and device parasitics. With the increasing adoption of GaN and SiC semiconductor devices, this topology is finding increasing use at both low power and high power applications.

**Fault protection of DC systems** One of the significant challenges to HVDC micogrids is the complexity in fault detection and protection of DC power systems. Both fault detection and fault isolation are complicated because of difficulties in manufacturing DC circuit breakers that can contain and quench the DC fault current arc. Recent research has focused on hybrid relays which combine semiconductor and mechanical switches which can provide fast response along with minimal conduction loss during nominal operation. Even with competent relays and circuit breakers, there are still challenges to isolating some sections of HVDC power system while servicing others.

In contrast there has been comparatively little research in examining the behavior

of HVDC power converters, especially non-isolated converters under fault conditions. This normally comes under Failure Mode Effects Analysis (FMEA) of converter design but there are dynamic conditions which cannot be accurately accounted for by offline analysis. This is another area that needs attention.

## 1.6 Research objectives

In the light of these these findings and status of DC-DC converter topology in the current state of the art, the following key research objectives are identified for the proposed research effort:

1. Propose a new DC-DC converter topology based on the Dual Active Bridge topology with the following characteristics

    a) Modularity

    b) Simple, robust dynamic model

    c) Resistant to component parasitics and non-linearities

    d) Soft switching characteristics for wide operating range

    e) Support for bidirectional power transfer capability

2. Replace magnetic coupling in the proposed converter with capacitor coupling in order to support

    a) Higher switching frequencies

    b) Multiple outputs

3. For the proposed class of DC-DC converter topology perform

    a) Power circuit design

b) Steady-state analysis

c) Dynamic control analysis

d) Comparative evaluation of performance characteristics

e) Verify analytical model through hardware prototype

f) Verify fault behavior during high voltage DC terminal to ground faults

## 1.7 Chapter outline

**Capacitor coupled SAB converter** This chapter introduces the capacitor-coupled single active bridge converter as an cognate of the transformer coupled single active bridge converter. The converter architecture is introduced and the steady state and dynamic properties of the converter are discussed in detail. The discontinuous nature of this converter has a meaningful effect on the state space model and this is also discussed in detail.

**Capacitor coupled DAB converter** This chapter introduces the capacitor-coupled dual active bridge converter which is based on the transformer coupled dual active bridge converter. The topology of this converter is introduced along with steady state operation under phase shift modulation method. The dynamic properties of the dual active bridge converter is studied using the concept of dynamic phasors and suitable controller configurations are proposed.

**Critical evaluation of converter characteristics** The proposed capacitor coupled DC-DC converter topologies have several unique characteristics that are not present in the traditional DC-DC boost topologies. These characteristics are examined to identify the properties and trade-offs associated with this topology. The various wiring configurations of this modular topology are discussed. A comparative evaluation of the capacitor

coupled single active and dual active bridge topology with existing transformer couupled topologies provides a frame of reference to evaluate the benefits of this topology.

**Fault analysis and grounding strategies** This chapter examines the behavior of the non isolated capacitively coupled converters under various fault conditions. This is then followed by grounding configurations that can be used for detecting faults and minimizing the fault leakage current. The equivalent circuit of the capacitor coupled converters under fault conditions is discussed. The various categories of faults are simulated with a prototype 10 stage capacitor coupled DC-DC converter.

**Application case studies** This chapter shares some of the experimental results that validate the analytical models that are developed alongside the proposed topology. The first class of results detail the performance characterisitics of the single phase capacitor coupled single active bridge converter. This is then followed by a high voltage converter built on the three phase cascade capacitor coupled configuration. The converter operation under steady state at different output voltage and power levels is recorded. The converter operation during fault condition is also included to verify the fault model.

**Conclusions and future work** This chapter lists the main contributions of the work and identifies the areas of future contributions.

CHAPTER 2

# Capacitor Coupled Single Active Bridge Converter

This chapter introduces a novel transformer-less unidirectional multilevel DC-DC converter topology. This topology consists of multiple capacitor coupled rectifiers connected in series at the DC output all fed from a single high frequency inverter. The converter architecture is described in Section I. The topology and operation of the converter is presented in Section II. In Section III design considerations of the converter are presented. Section IV examines the averaged equivalent circuit and the state space model of the converter is presented.

## 2.1 Converter architecture

An architectural schematic of the single phase Capacitor Coupled Single Active Bridge (CC-SAB) converter is shown in Fig 2.1. The DC source $V_{in}$ feeds a high frequency full bridge inverter formed by the MOSFETs S1-S4. The AC output $v_i$ of the high frequency inverter is available across output terminals. This voltage is applied across $n$ parallel branches of diode full bridge rectifiers, each in series with an inductance $L_s$ connected at the two AC terminals. The series connection between the diode rectifier and the inductor segments are coupled using series capacitors $C_{sa}$ and $C_{sb}$. The output voltage of each of the full bridge

rectifiers is maintained stiff using a local filter capacitor $C_{out}$.

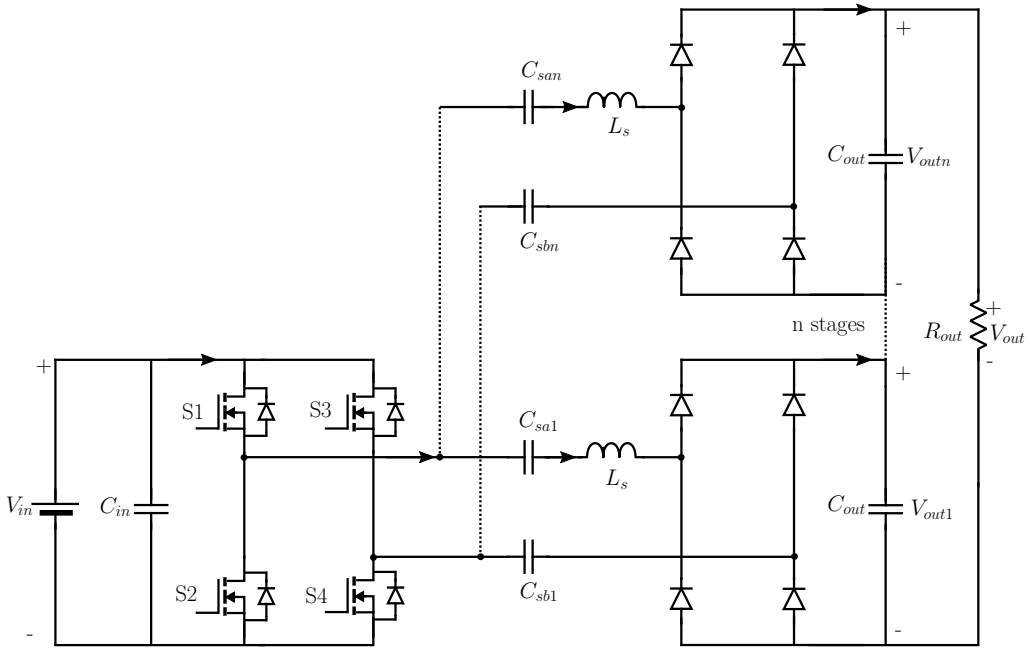


Figure 2.1: Architectural schematic of the single phase Capacitor Coupled Single Active Bridge converter

The rectifier outputs are all connected in series to obtain higher output voltage. This is made possible because of the presence of the coupling capacitors $C_{sa}$ and $C_{sb}$ which are essentially blocking DC voltages and short circuit for the AC voltage at the operating frequency. If output DC voltage of each stage is $V_{out}$, the net output voltage for a n-stage converter is the sum of the output voltage of the individual rectifiers $nV_{out}$.

There are two possible configurations for coupling the input stage to the multiple output stages. In the parallel coupled configuration all the capacitor coupled output stages are connected in parallel the input stage like in Fig 2.2. An alternate configuration, dubbed as cascade coupled connects the coupling capacitors in cascade with the input stage as shown in Fig 2.3.

The same multilevel architecture can be extended to three phases. A high frequency three phase IGBT or MOSFET based inverter feeds multiple three phase rectifiers. The addition of coupling capacitors at the input of every rectifier stage allows us to connect the rectifier

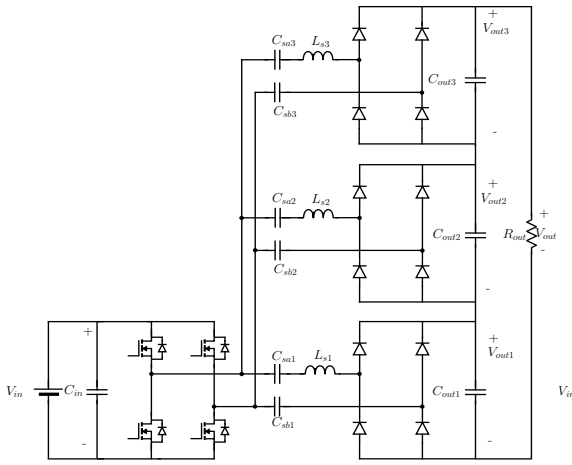


Figure 2.2: Parallel capacitor coupled single phase CCSAB with three output stages

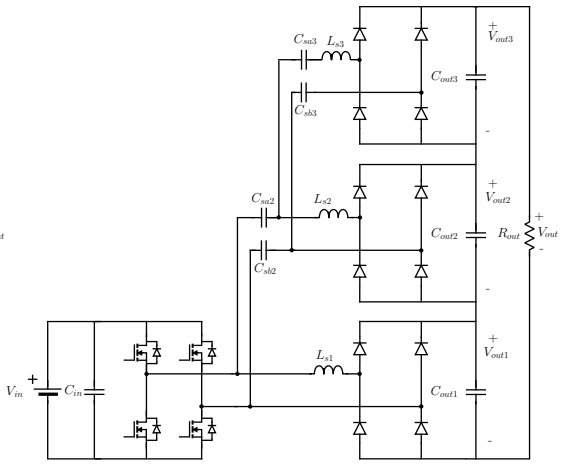


Figure 2.3: Cascade capacitor coupled single phase CCSAB with three output stages

outputs in series. Each three phase rectifier includes a series inductance $L_s$ in each phase and an output filter capacitance $C_{out}$. An architectural schematic of the three phase CCSAB is shown in Fig 2.4.

## 2.2 Steady state analysis

The modular nature of the architecture makes it possible to study the steady state operation with the inverter input stage and a single branch of the rectifier output stage and subsequently extend the analysis to the entire converter with multiple stages. The following simplifying assumptions are made in studying the circuit:

- The AC components of the voltage across the series coupling capacitors $v_{cs}$ are assumed negligible. This assumption is valid if the capacitor is selected to have negligible reactance at the inverter switching frequency, similar to interstage coupling capacitors in multistage audio amplifier circuits. Therefore the coupling capacitors can be replaced by a short circuit at the switching frequency.

- The rectifier output voltage $V_{out}$ ripple in the output filter capacitor $C_{out}$ is assumed to be negligible. This assumption is valid if the capacitor is chosen to be large enough to

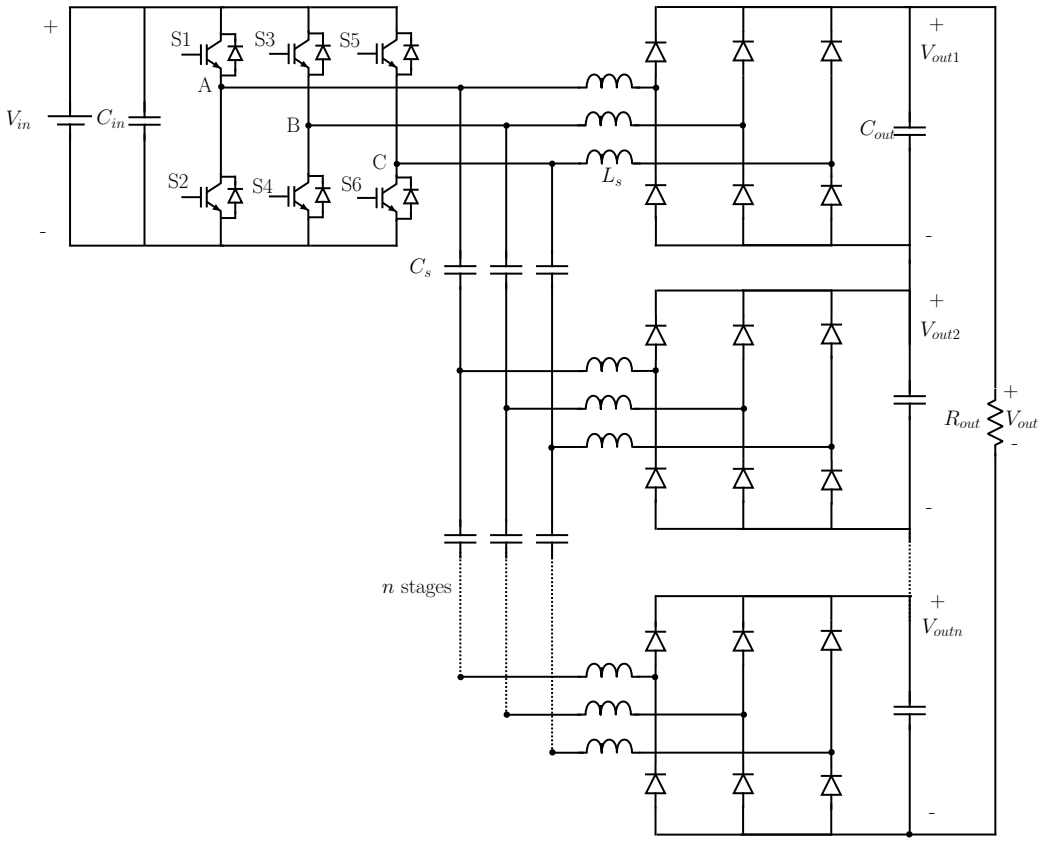


Figure 2.4: Architectural schematic of the three phase cascade coupled Capacitor Coupled Single Active Bridge converter

absorb the AC components of the rectifier current. Similarly the input voltage $V_{in}$ also has zero voltage ripple.

- All semiconductor devices are assumed to be ideal. Device forward voltage drops, on-state resistance, leakage currents, switching transients and reverse recovery currents have negligible effects on circuit operation.

- The power output of an equivalent single stage is $1/n$ times the power output of the full size converter. In other words

$$R_{outn} = \frac{R_{out}}{n} \tag{2.1}$$

$$V_{outn} = \frac{V_{out}}{n} \tag{2.2}$$

### 2.2.1 Single phase operation

Fig 2.5 shows the high frequency inverter along with one of the rectifier pathways illustrated in detail. The MOSFET switches S1-S4 form the high frequency full bridge inverter, operating at a frequency $F_s = 1/T_s$. The MOSFET switches S1 and S4 are turned on during the interval $0.5T_s$ for a time $t < 0.5T_s$. The MOSFET switches S2 and S3 are turned on during the next half cycle to continue the converter operation. Between these two time intervals, a deadtime interval is inserted where all switches are turned off.

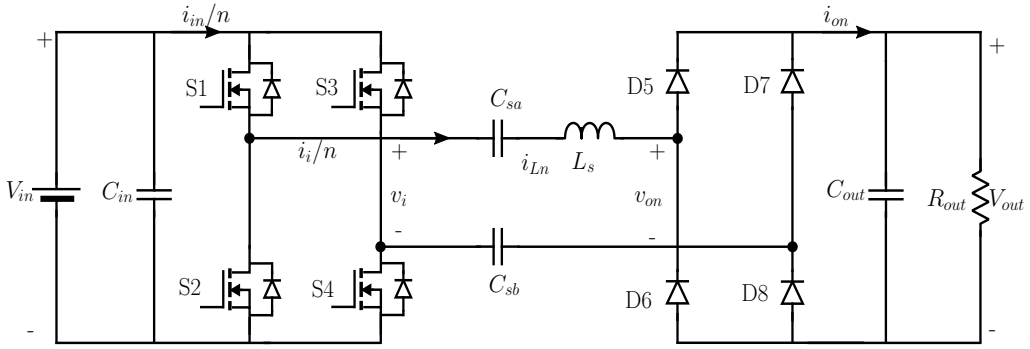


Figure 2.5: Schematic of the single phase inverter feeding a single stage of the capacitor coupled rectifier

Because of half cycle symmetry, the circuit operation of the rectifier may be analyzed over one half cycle and extended further to the other half cycle through appropriate polarity reversals. The typical waveforms of the various electrical quantities over one complete switching cycle are shown in Fig 2.6. It is convenient to divide the period of operation into three separate intervals over each half cycle by behavior of the inductor current which are labeled as charging, discharging and non-conducting intervals. The duty ratios of these intervals normalized to the period of a half cycle ($0.5T_s$) may be defined as charge duty ratio ($d_1$), discharge duty ratio ($d_2$) and non-conducting duty ratio ($d_3$).

Further simplified equivalent circuits of inverter feeding a single rectifier, during the charging, discharging and non-conducing intervals are shown in Fig 2.7(a),(b) and (c) respectively. In these figures, the capacitors $C_s$ are assumed to be short circuits and are not shown; the output side of the rectifier is represented by a constant voltage $V_{out}$. The active paths of

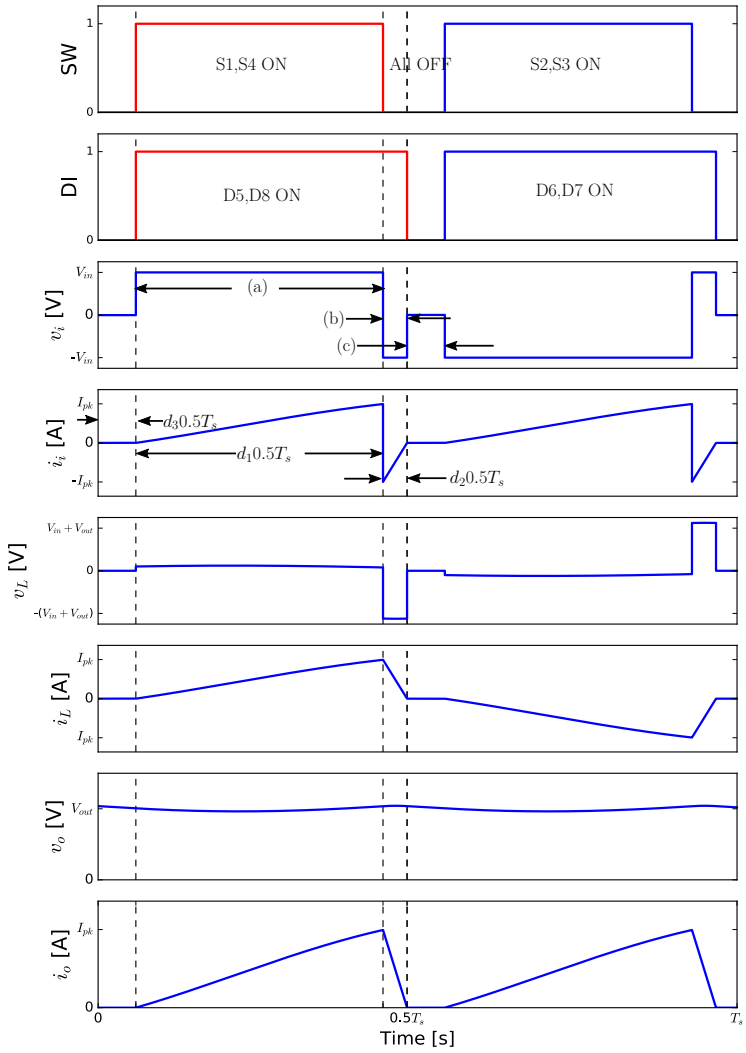


Figure 2.6: Single stage capacitively coupled diode bridge rectifier

current flow are shown in dark, while the paths that do not carry current are shown in grey. The operation of the circuit in each of the intervals are described sequentially.

The inductor charging interval ($d_1 0.5T_s$) begins when the switches S1 and S4 are turned on in the time interval of $0.5T_s$. The voltage across the inductor is equal to the difference between the input voltage $V_{in}$ and the output voltage $V_{out}$. Since this voltage is positive, the inductor current increases linearly and flows through the path indicated in Fig 2.7(a). This interval ends when S1 and S4 are turned off. The circuit operation in this time interval can be

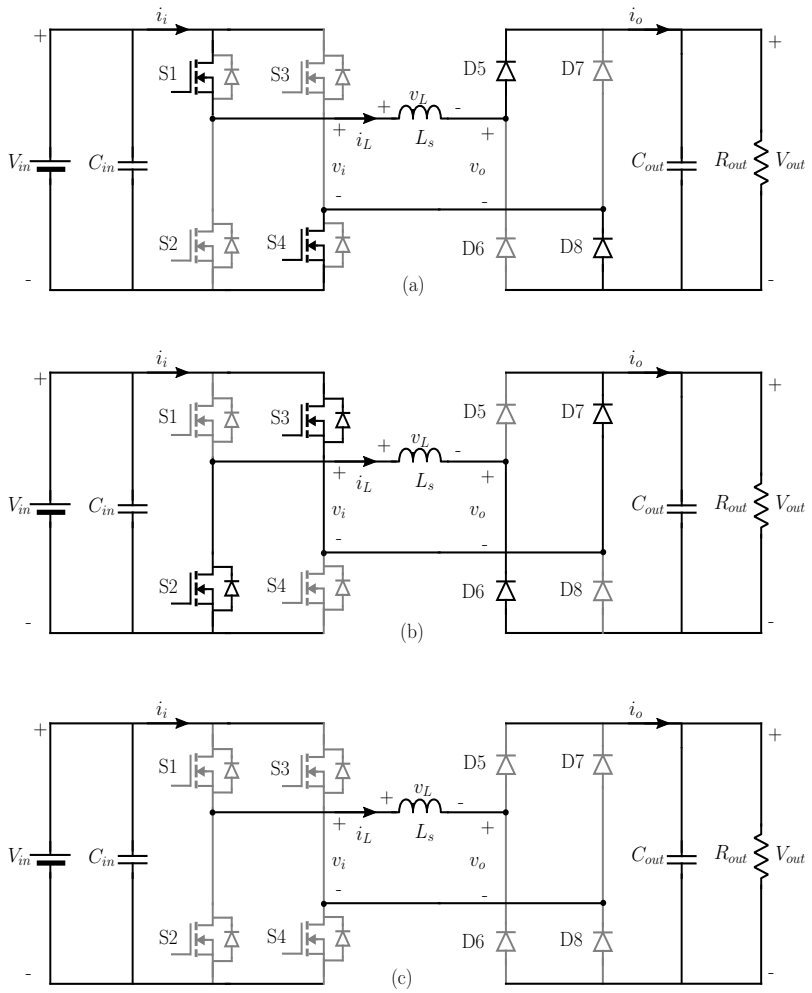


Figure 2.7: Current flow path during charging (top), discharging (middle) and non-conducting (bottom) intervals, represented in a simplified equivalent circuit valid during one half cycle

expressed using the following relationships:

$$\frac{di_L}{dt} = \frac{1}{L_s}(V_{in} - V_{out}) \tag{2.3}$$

$$I_{pk} = \frac{1}{L_s}(V_{in} - V_{out})d_1\frac{T_s}{2} \tag{2.4}$$

$$d_1 = \frac{2L_sI_{pk}}{(V_{in} - V_{out})T_s} \tag{2.5}$$

The inductor discharge interval ($d_20.5T_s$) begins when the switches S1 and S4 are turned off at end of $d_1T_s$. The current freewheels through the anti-parallel body diodes of S2 and S3. This leads to a voltage reversal at the terminals of the inverter as may be observed in Fig 2.6(c).

The net voltage across the inductor is negative, and equal to the sum of the input voltage and the output voltage. Due to the negative voltage, the inductor current decreases linearly and flows through the path indicated in Fig 2.7(b).This interval ends when the inductor current reaches zero. The circuit operation can be expressed using the following relationships:

$$\frac{di_L}{dt} = \frac{1}{L_s}(-V_{in} - V_{out}) \tag{2.6}$$

$$I_{pk} = \frac{1}{L_s}(V_{in} + V_{out})d_2\frac{T_s}{2} \tag{2.7}$$

$$d_2 = \frac{2L_sI_{pk}}{(V_{in} + V_{out})T_s} \tag{2.8}$$

This is then followed by the non-conducting interval where inductor current remains zero and none of the active or passive switches conduct current. At the end of this interval, switches S2 and S3 are turned on, initiating the negative half cycle of conduction. This interval can be calculated as

$$d_3 = 1 - d_1 + d_2 \tag{2.9}$$

The various modes of the single phase CCSAB are summarized in Table 2.1.

Table 2.1: Steady state behavior of single phase CCSAB during different modes.

| | Charging (a) | Discharging (b) | Non-conducting (c) |
|---|---|---|---|
| Interval | $d_1 0.5T_s$ | $d_2 0.5T_s$ | $d_3 0.5T_s$ |
| $v_L$ | $V_{in} + V_{out}$ | $-(V_{in} + V_{out})$ | N/A |
| Initial $i_L$ | 0 | -$I_{pk}$ | 0 |
| Final $i_L$ | $I_{pk}$ | 0 | 0 |

#### 2.2.1.1 Two stage model

Since every output stage has two DC current blocking series capacitors, we can connect the all output stages in series without shorting the source voltage. The evolution of the converter voltage and current with stacked connection can be illustrated using a parallel coupled single phase CCSAB with two ouput stages as shown in Fig 2.8. The final output voltage is now the sum of the rectified voltage of each stage. One effect of this connection is that all the series

coupling capacitors will now have a DC bias voltage. This bias voltage depends on the relative position of each output stage in the connection string. Besides the DC bias voltage across the coupling capacitors, the operation of the two branch converter is identical to that of the single branch converter.

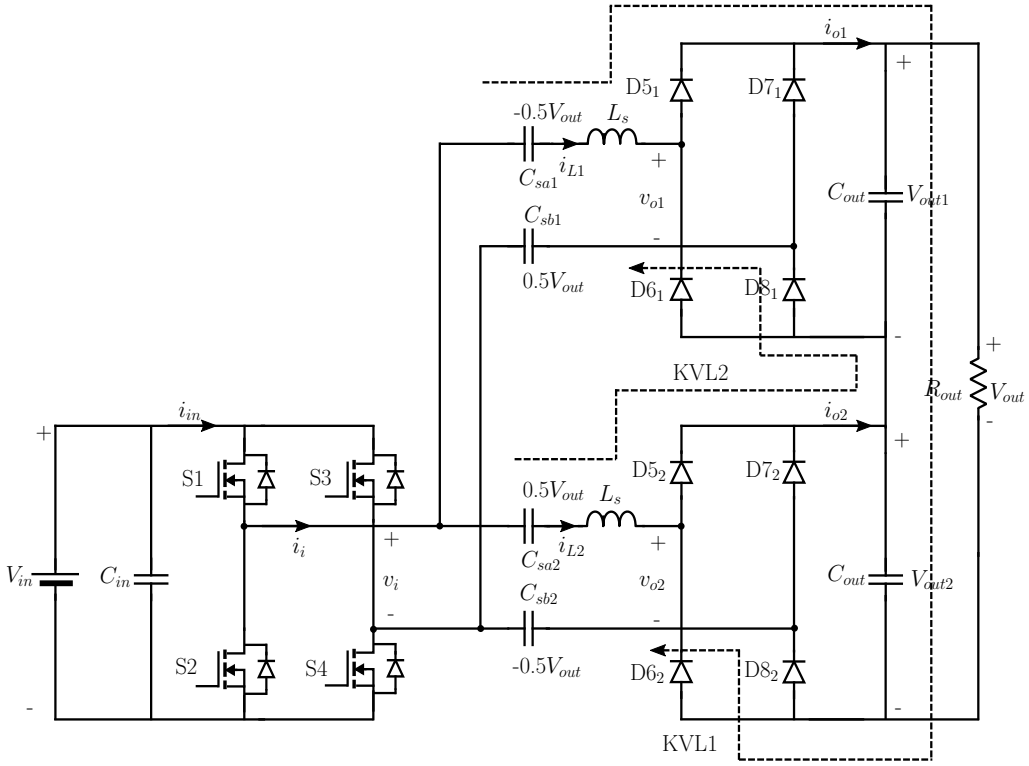


Figure 2.8: Two stage capacitively coupled diode bridge rectifier showing the series capacitor DC bias voltages

The output DC voltage of each stage for a two-stage converter will be

$$V_{out1} = V_{out2} = \frac{V_{out}}{2} \tag{2.10}$$

The average voltage across each series capacitor may be determined by examining the circuit interconnections using Kirchoff's voltage law (KVL). The DC voltage at the output terminals of the inverter ($v_i$) and the DC voltage at the input terminals of the rectifier ($v_{o1}, v_{o2}$) are zero by virtue of waveform symmetry. Therefore any DC voltage across one of the coupling capacitors in a single rectifier branch has to be matched in magnitude with reverse polarity

across the other coupling capacitor in the same rectifier branch. This may be expressed using KVL as

$$\langle v_{csa1} \rangle + \langle v_{csb1} \rangle = 0 \tag{2.11}$$

$$\langle v_{csa2} \rangle + \langle v_{csb2} \rangle = 0 \tag{2.12}$$

where $\langle\rangle$ represents the averaging operator over time period $T_s$. The KVL1 and KVL2 paths illustrated in Fig 2.8 have to be satisfied at all instants of time during the switching cycle. For instance, during the positive half cycle, the following expressions may be used to conform to KVL for the two paths:

$$\langle v_{csa1} \rangle + V_{out1} + V_{out2} + \langle v_{csb2} \rangle = V_{in} \tag{2.13}$$

$$\langle v_{csb1} \rangle + \langle v_{csa2} \rangle = V_{in} \tag{2.14}$$

We can solve (2.11) through (2.14) to arrive at this relationship

$$\langle v_{csa1} \rangle = \langle v_{csb2} \rangle = -\frac{V_{out}}{2} \tag{2.15}$$

$$\langle v_{csb1} \rangle = \langle v_{csa2} \rangle = \frac{V_{out}}{2} \tag{2.16}$$

#### 2.2.1.2 N stage model

This same concept can be generalized and extended to N output stages to realize any high voltage. The analytical process based on application of KVL across different branches illustrated for the 2-branch converter may be extended for the N-branch case as well. In case of the N stage parallel coupled single phase CCSAB, the DC voltage across the series coupling capacitors is a function of the position of the output stage in the parallel connected string. The DC voltage across the coupling capacitor of the $i^{th}$ branch can be derived as

$$\langle v_{csi} \rangle = \pm[-(N-1)\frac{V_{out}}{2} + (i-1)V_{out}] \tag{2.17}$$

where $V_{out}$ is the combined output voltage of N stages. Furthermore, similar to the two stage case, the coupling capacitors in a single branch have voltages of opposite polarity, and the coupling capacitors in the adjacent branches also have opposite polarity. The DC bias voltage

Table 2.2: Coupling capacitor DC bias voltage $\langle v_{csi} \rangle / V_{out}$ for different number of stages $n$

| | $\downarrow n$ i$\rightarrow$ | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|
| $C_{sai}$ | 2 | -1/2 | 1/2 | | | |
| | 3 | -1 | 0 | 1 | | |
| | 4 | -3/2 | -1/2 | 1/2 | 3/2 | |
| | 5 | -2 | -1 | 0 | 1 | 2 |
| $C_{sbi}$ | 5 | 2 | 1 | 0 | -1 | 2 |
| | 4 | 3/2 | 1/2 | -1/2 | -3/2 | |
| | 3 | 1 | 0 | -1 | | |
| | 2 | 1/2 | -1/2 | | | |

across the coupling capacitors follow a particular pattern as the number of stages is increased, as may be discerned from Table 2.2, which shows voltage distribution for cases up to $n = 5$. An equivalent circuit for the N stage parallel coupled single phase CCSAB is shown in Fig 2.9. It can be observed from the equivalent circuit that the topology is essentially an input-parallel output-series configuration with all the output stages sharing equal current from the input stage. Additionally since the output stages are in series, the rectified current is the same in all output stages.

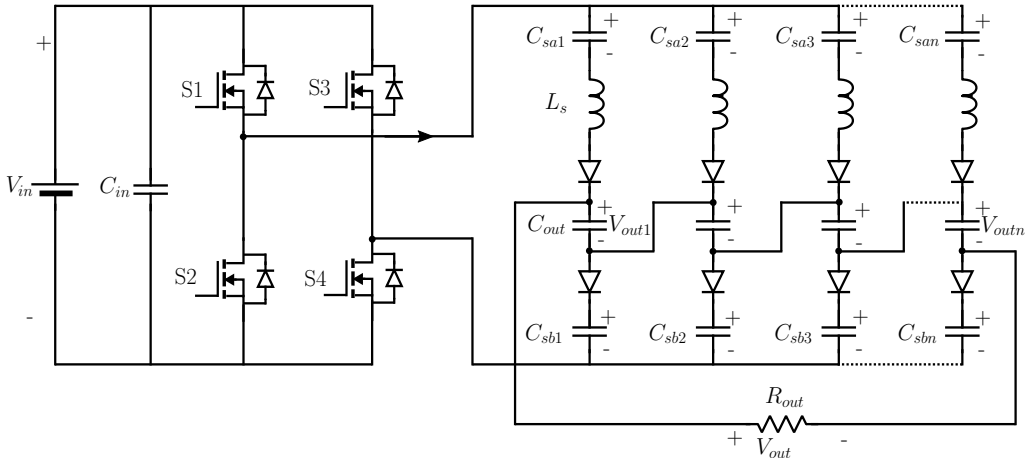


Figure 2.9: Equivalent circuit of the N stage parallel coupled single phase CCSAB

### 2.2.2 Three phase operation

Fig 2.10 shows a three phase inverter feeding a single stage of the three phase CCSAB. The inverter is operating on six-step switching scheme at 50% duty cycle with switching time period set as $T_s$ and deadtime between the switches in the same phase $T_d$ set to $0.02T_s$. The three phase switches of the inverter and rectifier are labeled as incoming phase $S_i$,$D_i$, outgoing phase $S_o$,$D_o$ and transitioning phase $S_t$,$D_t$. The complementary switches and diodes of each phase are labeled using the prime symbol $S_i'$,$D_i'$ etc. As mentioned earlier, the series coupling capacitors $C_s$ will not take part in the dynamic behavior of the converter at the switching frequency.

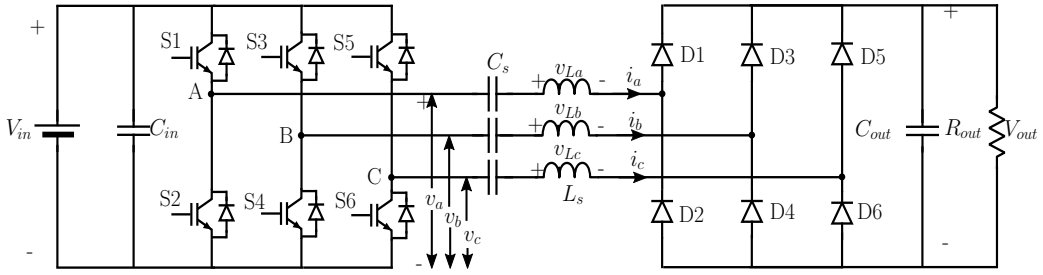


Figure 2.10: Schematic of three phase inverter feeding a three phase capacitor coupled rectifier

The time required for the inductor current in any phase to extinguish to zero is defined as the commutation interval $t_c$. The inductor current behavior depends on the relationship between the commutation time and the deadtime interval. There are two operating conditions of this converter based on this relationship. In light load condition or with low input and output voltage, the commutation time interval is longer than the dead time interval. In this condition, the switch on the transitioning phase will turn on under zero voltage conditions since the reverse connected diode of the switch is still conducting current. In heavy load condition or when the input and output voltage are close to nominal rating, the commutation time interval is shorter than the dead time interval. In this condition, the inductor phase current is turned off before the transitioning phase switch is turned on, which means the incoming phase is briefly non-conducting till the end of dead time interval.

#### 2.2.2.1 Operating condition: $t_c > T_d$

In this operating condition, the inductor current in the transitioning phase is essentially continuous with current transitioning from positive to negative with no non-conduction period in the dead time interval. The converter operation can be subdivided into two modes -power transfer mode and transition mode as shown in Fig 2.11. In the interval prior to $t = 0$ (Fig 2.11a), the circuit is operating in power transfer mode, with the rectified DC output current $i_{out}$ equal to the current in the outgoing phase $i_o$. At time $t = 0$, switch $S_t'$ is turned off but $S_t$ is not immediately turned on because of the deadtime delay between $S_t$ and $S_t'$. Since $i_t \neq 0$, the anti-parallel diode of $S_t$ turns on and conducts till $i_t = 0$(Fig 2.11b). This mode is called the transition mode since $i_t$ current direction is transitioning from negative to positive. The current commutation interval $t_c$ depends on the instantaneous current at the beginning of this mode $I_c$ and the input and output voltages. At time $t = T_d$, switch $S_t$ is turned on (Fig 2.11c) but since the current direction has not changed, the anti-parallel diode of $S_t$ continues to conduct. Since $t_c > T_d$, there is no change in the circuit behavior (Fig 2.11b,c) till $i_t = 0$. Then at time $t = T_s/6 - t_c$, $i_t$ reverses direction and starts a new power transfer mode (Fig 2.11d).

The relevant voltages and currents during the various modes are shown in Fig 2.12. The three inverter pole voltages with respect to the DC bus reference are shown in the first three plots to illustrate the switching sequence. The next three plots show the inductor currents for the incoming phase ($i_b$), transitioning phase ($i_a$) and outgoing phase ($i_c$). The final plot in Fig 2.12 shows the rectified DC current $i_{out}$. Since $t_c > T_d$, the transitioning phase current is continuous with current reversing direction from negative to positive only after $t_c$ and not after $T_d$. At every time instant, the currents are balanced such that $i_a + i_b + i_c = 0$. The state of the circuit in each mode are summarized in Table 2.3. The first row shows the inductor voltage across each of the three phases, the subsequent rows describe the instantaneous currents in each phase at the beginning and end of each mode. $I_c$ is defined as the instantaneous current in the transitioning phase at the beginning of the transition interval, $I_p$ is defined as the instantaneous current in the transitioning phase at end of the power transfer interval. $I_{max}$

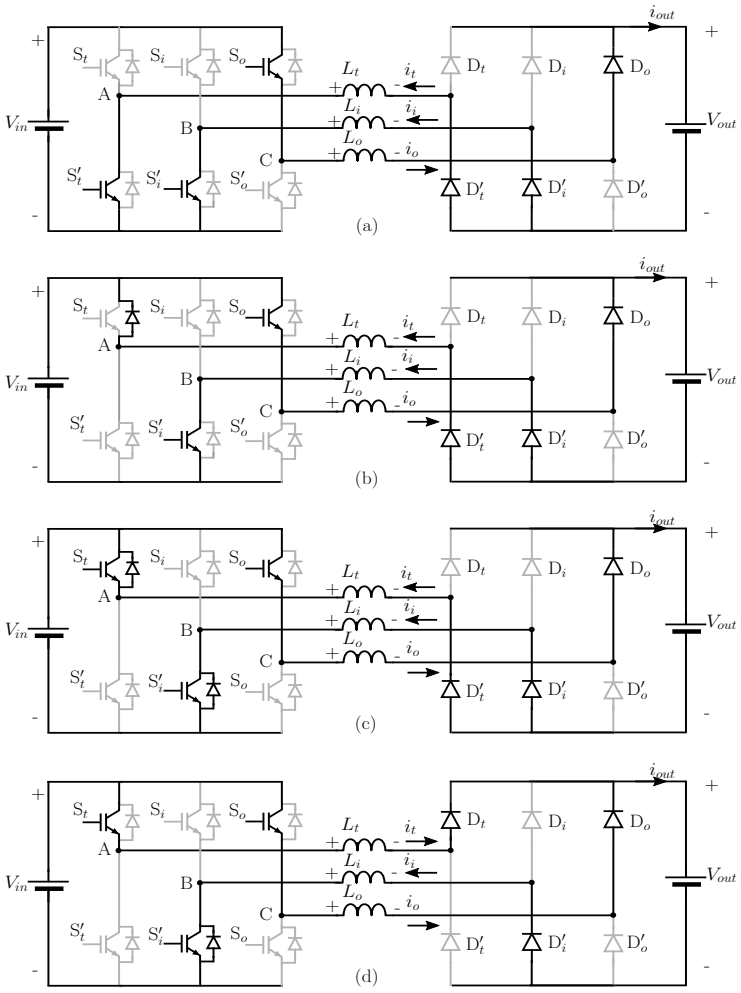


Figure 2.11: Circuit schematic showing the operating modes of the three phase CCSAB converter when $t_c > T_d$.

and $I_{min}$ are the maximum and minimum instanteous currents respectively of the rectified output current $i_{out}$.

#### 2.2.2.2 Operating condition: $t_c < T_d$

In this operating condition, a brief interval exists within the dead time interval where the transitioning phase has zero inductor current. As in the previous analysis, the circuit is operating in power transfer mode before time $t = 0$ (Fig 2.13a). In this mode the rectified output DC current $i_{out}$ is equal to the current in the outgoing phase $i_o$. At time $t = 0$, switch

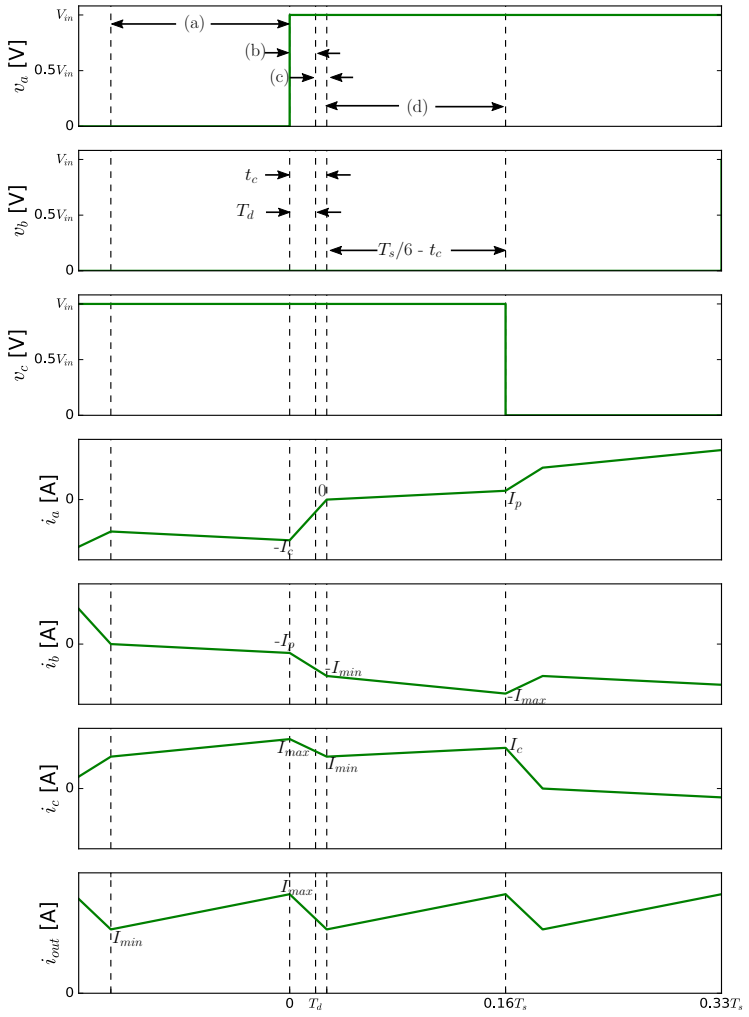


Figure 2.12: Simulation waveforms of line-to-DC bus-ground voltage ($v_a, v_b, v_c$), line current ($i_a, i_b, i_c$) and rectified output current $i_{out}$ when $t_c > T_d$.

$S_t'$ is turned off but $S_t$ turn on is delayed because of the dead time delay between $S_t$ and $S_t'$. Since $i_t \neq 0$, the anti-parallel diode of $S_t$ turns on and conducts till $i_t = 0$ (Fig 2.13b). This current commutation interval $t_c$ depends on the instantaneous current at the beginning of this mode $I_c$, the phase inductance $L_s$ and the input $V_{in}$ and output voltages $V_{out}$. At the beginning of the interval in Fig 2.13c $i_t = 0$ but since $S_t$ is not turned on, the current in the transitioning phase will remain zero. At time $t = T_s/6 - T_d$, $S_t$ is turned on (Fig 2.13d) and a new power transfer mode is started with the rectified output DC current $i_{out}$ equal to the current in the incoming phase $i_i$.

Table 2.3: Steady state behavior of three phase CCSAB in different modes when $t_c > T_d$.

| | Power transfer (a) | Transition (b) | Power transfer (c) |
|---|---|---|---|
| Interval | $T_s$/6 - $t_c$ | $t_c$ | $T_s$/6 - $t_c$ |
| $v_{Lt}$ | $-\frac{1}{3}(V_{in}-V_{out})$ | $\frac{1}{3}(V_{in}+V_{out})$ | $\frac{1}{3}(V_{in}-V_{out})$ |
| $v_{Li}$ | $-\frac{1}{3}(V_{in}-V_{out})$ | $\frac{1}{3}(V_{out}-2V_{in})$ | $-\frac{2}{3}(V_{in}-V_{out})$ |
| $v_{Lo}$ | $\frac{2}{3}(V_{in}-V_{out})$ | $\frac{1}{3}(V_{in}-2V_{out})$ | $\frac{1}{3}(V_{in}-V_{out})$ |
| Initial $i_{Lt}$ | $-I_{min}$ | $-I_c$ | 0 |
| Final $i_{Lt}$ | $-I_c$ | 0 | $I_p$ |
| Initial $i_{Li}$ | 0 | $-I_p$ | $-I_{min}$ |
| Final $i_{Li}$ | $-I_p$ | $-I_{min}$ | $-I_{max}$ |
| Initial $i_{Lo}$ | $I_{min}$ | $I_{max}$ | $I_{min}$ |
| Final $i_{Lo}$ | $I_{max}$ | $I_{min}$ | $I_c$ |

The relevant voltages and currents during the various modes are shown in Fig 2.12. The three inverter pole voltages with respect to the DC bus reference are shown in the first three plots to illustrate the switching sequence. The next three plots show the inductor currents for the incoming phase ($i_b$), transitioning phase ($i_a$) and outgoing phase ($i_c$). The final plot in Fig 2.12 shows the rectified DC current $i_{out}$. Since $t_c < T_d$, the transitioning phase current has a discontiuity in the interval $T_d$ as it is transitioning from negative to positive. Similar to the previous case, at every time instant, the currents are balanced such that $i_a + i_b + i_c = 0$. The state of the circuit in each mode are summarized in Table 2.4. The first row shows the inductor voltage across each of the three phases, the subsequent rows describe the instantaneous currents in each phase at the beginning and end of each mode. As in the previous operating condition, $I_c$ is defined as the instantaneous current in the transitioning phase at the beginning of the transition interval. $I_{p1}$ is defined as the instantaneous current in the incoming and outgoing phase at end of the dead time interval. $I_{p2}$ is defined as the current in the transitioning phase at the end of the power transfer interval such that $|I_{p1}| > |I_{p2}|$. $I_{max}$ and $I_{min}$ are the maximum and minimum instantaneous currents respectively of the rectified output current $i_{out}$.

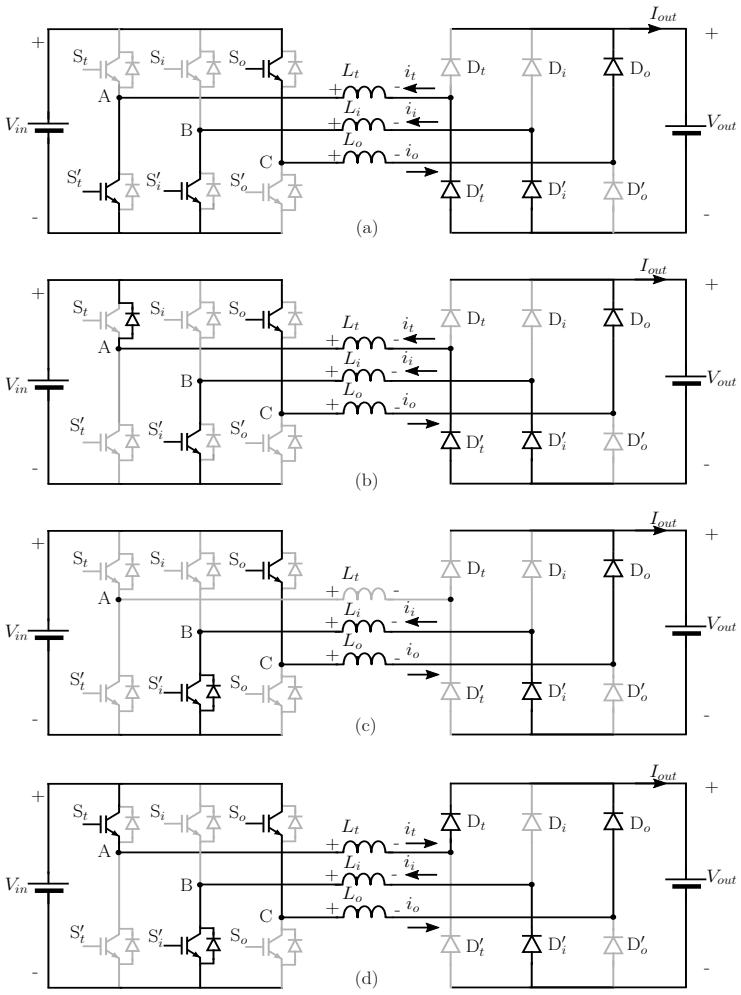


Figure 2.13: Circuit schematic showing the operating modes of the three phase CCSAB converter when $t_c < T_d$.

#### 2.2.2.3 N stage model

We can extend the steady state analysis to N stages of capacitor coupled three phase rectifier stages with series connected DC output voltages. The single phase equivalent circuit of a three phase cascade coupled CCSAB is shown in Fig 2.15 to illustrate the evolution of the DC voltage across the coupling capacitors in each output stage. We can observe from the cascade arrangement that the DC voltage across each coupling capacitor will not exceed the rectified output voltage of any stage. A notable difference from the single phase equivalent circuit is that each output stage branch now has two series inductors. Another feature shown here

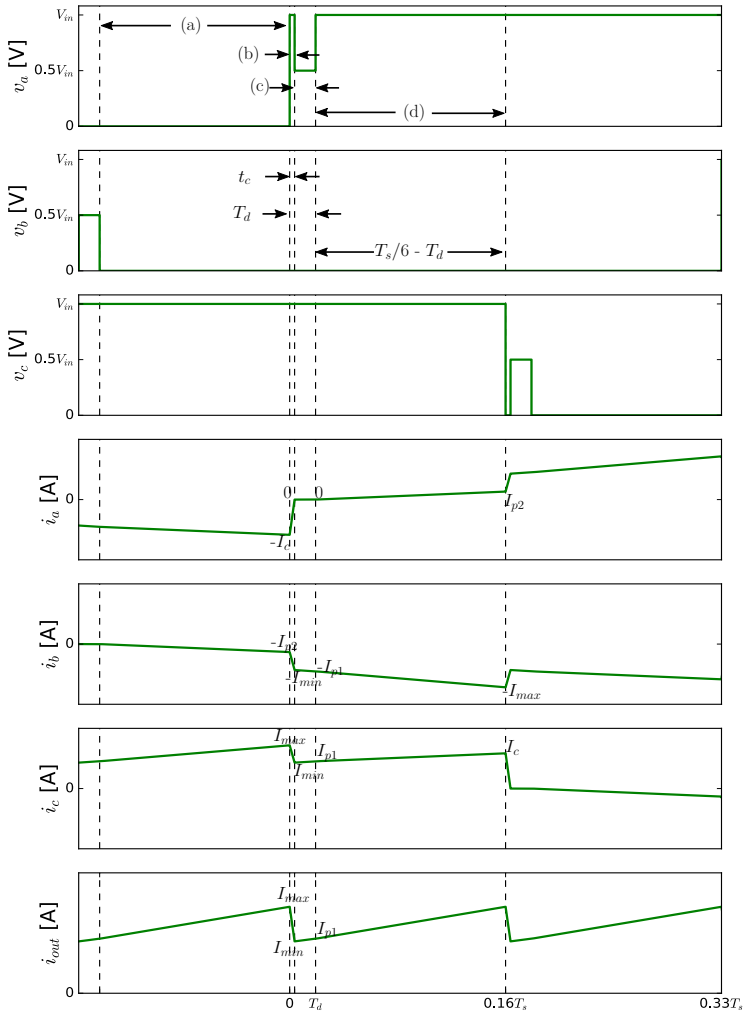


Figure 2.14: Simulation waveforms of line-to-DC bus-ground voltage ($v_a, v_b, v_c$), line current ($i_a, i_b, i_c$) and rectified output current $i_{out}$ when $t_c < T_d$.

that is not present in the single phase CCSAB is the presence of reverse blocking diodes $D_{rb}$ which are inserted between the series connection of the rectified output voltage. The function of these reverse blocking diodes is to decouple the AC current of each output stage from its neighboring stage. This ensures that each output stage behaviour is dependent only on the input stage which means that the overall converter behavior is truly modular.

Table 2.4: Steady state behavior of three phase CCSAB in different modes when $t_c < T_d$.

| | Power transfer (a) | Transition (b) | Discontinuous (c) | Power transfer (d) |
|---|---|---|---|---|
| Interval | $T_s/6$ - $T_d$ | $T_c$ | $T_d - T_c$ | $T_s/6$ - $T_d$ |
| $v_{Lt}$ | $-\frac{1}{3}(V_{in} - V_{out})$ | $\frac{1}{3}(V_{in} + V_{out})$ | N/A | $\frac{1}{3}(V_{in} - V_{out})$ |
| $v_{Li}$ | $-\frac{1}{3}(V_{in} - V_{out})$ | $\frac{1}{3}(V_{out} - 2V_{in})$ | $-\frac{1}{2}(V_{in} - V_{out})$ | $-\frac{2}{3}(V_{in} - V_{out})$ |
| $v_{Lo}$ | $\frac{2}{3}(V_{in} - V_{out})$ | $\frac{1}{3}(V_{in} - 2V_{out})$ | $\frac{1}{2}(V_{in} - V_{out})$ | $\frac{1}{3}(V_{in} - V_{out})$ |
| Initial $i_{Lt}$ | $-I_{p1}$ | $-I_c$ | 0 | 0 |
| Final $i_{Lt}$ | $-I_c$ | 0 | 0 | $I_{p2}$ |
| Initial $i_{Li}$ | 0 | $-I_{p2}$ | $-I_{min}$ | $-I_{p1}$ |
| Final $i_{Li}$ | $-I_{p2}$ | $-I_{min}$ | $-I_{p1}$ | $-I_{max}$ |
| Initial $i_{Lo}$ | $I_{p1}$ | $I_{max}$ | $I_{min}$ | $I_{p1}$ |
| Final $i_{Lo}$ | $I_{max}$ | $I_{min}$ | $I_{p1}$ | $I_c$ |

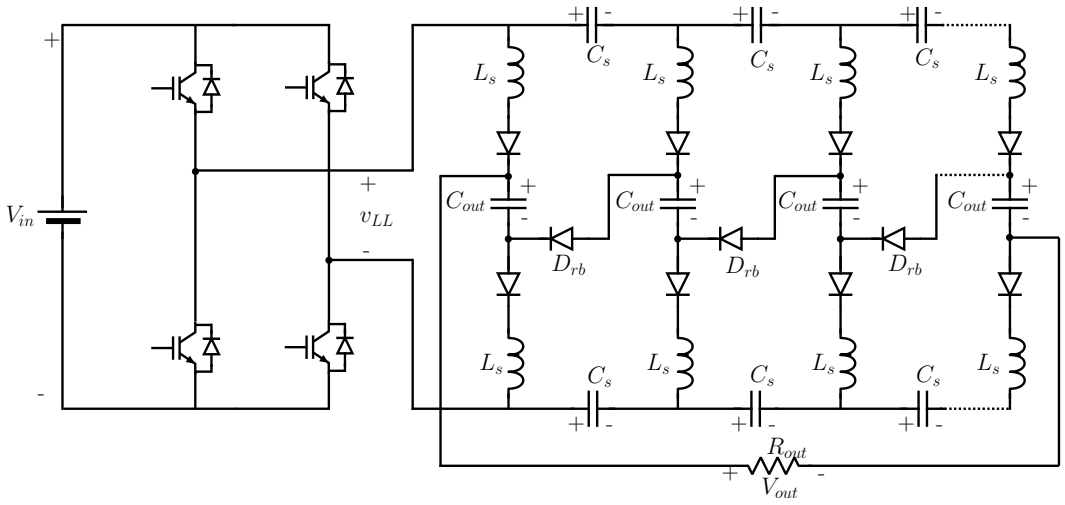


Figure 2.15: Equivalent circuit of three phase cascade coupled CCSAB.

## 2.3 Design considerations

### 2.3.1 Single phase CCSAB

#### 2.3.1.1 Voltage transfer ratio

The concept of inductor volt-second balance over the inductor charge and discharge intervals can be used to derive the output voltage conversion ratio for a single stage.

$$(V_{in} - V_{out})\,d_1 + (-V_{in} - V_{out})\,d_2 = 0 \tag{2.18}$$

$$V_{out} = V_{in}\frac{d_1 - d_2}{d_1 + d_2} \tag{2.19}$$

The average output current can be calculated from the inductor current waveform.

$$I_{out}(t) = |i_L(t)| \tag{2.20}$$

$$\langle I_{out}\rangle = \frac{I_{pk}}{2}(d_1 + d_2) \tag{2.21}$$

$$\langle I_{out}\rangle = \frac{V_{out}}{R_{out}} \tag{2.22}$$

Equating (2.21) and (2.22), the relationship between the input and output voltage for different duty ratio and load conditions can be derived. Eliminating $d_2$, the solution for the voltage conversion ratio $M$ is

$$M(d_1, K) = \frac{V_{out}}{V_{in}} \tag{2.23}$$

$$M(d_1, K) = \frac{1 + d_1^2 K}{2}\left[\sqrt{1 + \frac{4d_1^2 K}{\left(1 + d_1^2 K\right)^2}} - 1\right] \tag{2.24}$$

$$K = \frac{T_s R_{out}}{2L_s} \tag{2.25}$$

$$\tau_L = \frac{L_s}{R_{out}} \tag{2.26}$$

$K$ is the ratio of the switching period and the equivalent LR time constant of one stage of the converter. Fig 2.16 shows the modulation range of the converter for various $K$ values for a single stage. Higher $K$ ensures that $V_{out} \approx V_{in}$, but there is limited control on the output voltage. Lower values of $K$ allow for variation in output voltage based on $d_1$ but this also means that $V_{out}$ would be much smaller than $V_{in}$.

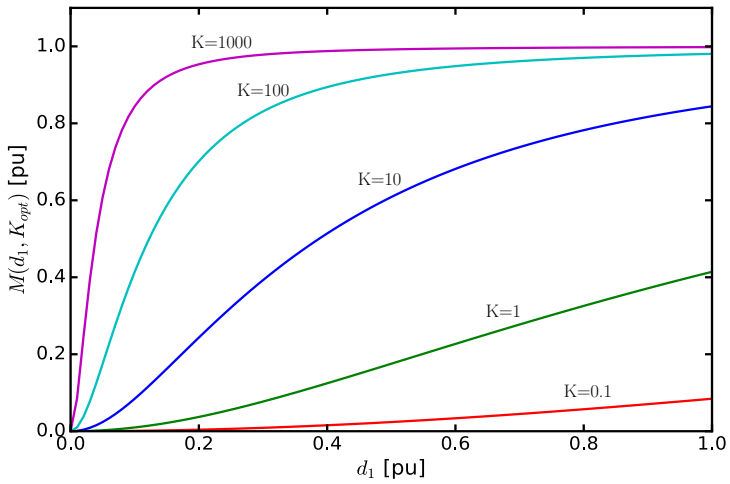


Figure 2.16: A plot of the voltage conversion ratio, $M(d_1,K)$ for one stage of the power converter

#### 2.3.1.2 Output voltage regulation

It is clear from the expression of the voltage transfer ratio that the output voltage of the power converter is strongly affected by the interaction between the output current and the AC voltage drop across the inductor. The output voltage expressed explicitly in terms of the output current to be

$$V_{out} = V_{in} \frac{1 - \dfrac{2L_s F_s I_{out}}{{d_1}^2 V_{in}}}{1 + \dfrac{2L_s F_s I_{out}}{{d_1}^2 V_{in}}} \tag{2.27}$$

Here, the output voltage is expressed as a bilinear fraction that depends on the normalized voltage drop across the series inductor at the switching frequency. The voltage drop term is $2L_s F_s I_{out}$, and it is normalized by the voltage term ${d_1}^2 V_{in}$. It is clear that when output current is zero, the bilinear terms vanish, and the output voltage is equal to $V_{in}$, as there is no voltage drop across the series inductor $L_s$. Typically, when the choice of K is close to the optimum value of 10, the normalized voltage drop across the series inductor would be close to about 1/10, for value of $d_1$ close to unity. Under these conditions, the output voltage may be approximated as

$$V_{out} = V_{in}[1 - \frac{4L_s F_s I_{out}}{{d_1}^2 V_{in}}] \tag{2.28}$$

A plot of the load regulation of the converter is illustrated in Fig 2.17, for different value of $d_1$, for the choice of $K = 10$. The horizontal axis is normalized to the nominal average output current of the output stage. The vertical axis is normalized to the input voltage $V_{in}$. The effect of the inductive voltage drop is clear from the regulation characteristics. In order to maintain appropriate output voltage regulation with realistic inductor value, it would be necessary to build a closed loop regulator by appropriately controlling $d_1$.

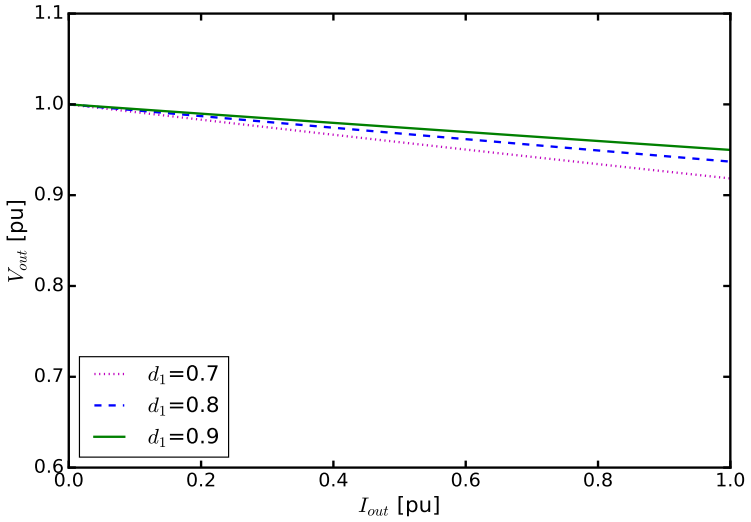


Figure 2.17: A plot of load regulation of the power converter for selected values of $d_1$

#### 2.3.1.3 Series inductor

From Fig 2.16, the optimum range of K to ensure good control range with adequate output voltage is about 10. Thus, if $K_{opt}$ and the operating frequency is known, inductor $L_s$ can be sized appropriately.

$$L_s = \frac{T_s}{2} \frac{R_{outn}}{K_{opt}} \tag{2.29}$$

The RMS inductor current can be calculated from

#### 2.3.1.4 Series coupling capacitor

Since the inductor current waveform is now known, the peak-to-peak capacitor voltage ripple can be derived using the current waveform

$$\Delta v_{cs} = \frac{I_{out}}{4F_s C_s} \tag{2.30}$$

$$C_s = \frac{2K_{opt} T_s}{R_{outn}} \tag{2.31}$$

The RMS value of the coupling capacitor current is also equal to the RMS value of the inductor current.

#### 2.3.1.5 Output filter capacitor

The filter capacitor voltage and current are illustrated in Fig 2.18. The worst-case voltage ripple in the filter capacitor can be calculated under the condition $d_1 + d_2 = 1$. This is the border between discontinuous and continuous conduction mode of the series inductor current. In this condition

$$I_{pk} = 2I_{out} \tag{2.32}$$

$$C_{out} = \frac{I_{out} T_s}{8\Delta v_{out}} \tag{2.33}$$

The output filter capacitor can be sized based on the choice of $\Delta v_{out}$. The worst case RMS value of the filter capacitor current will be to be equal to the RMS value of the inductor current under the same conditions.

#### 2.3.1.6 Input switches

The reverse blocking voltage rating of the input switches and diodes is same as input voltage $V_{in}$. The RMS current of the input side switch $n$ times the RMS current of the series inductor.

$$I_{swirms} = nI_{pk}\sqrt{\frac{d_1 + d_2}{3}} \tag{2.34}$$

The switch anti-parallel diode current is given as

$$I_{dirms} = nI_{pk}\sqrt{\frac{d_2}{3}} \tag{2.35}$$

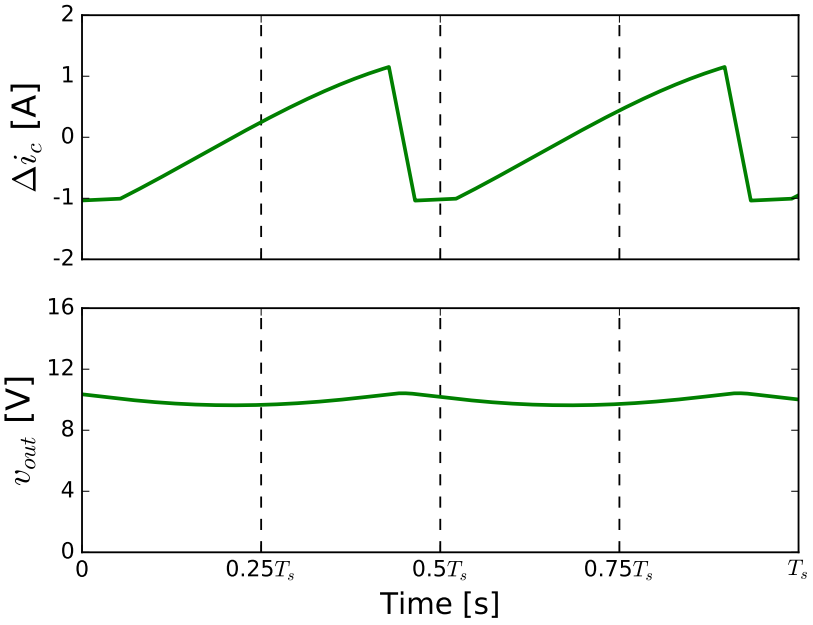


Figure 2.18: Typical waveforms of output voltage and capacitor ripple current

#### 2.3.1.7 Output switches

Since the CCSAB topology is input-parallel and output-series, the reverse blocking voltage rating of the output diodes is equal to the input voltage $V_{in}$ not the final output voltage $V_{out}$. The RMS current of each output diode is given as

$$I_{dorms} = I_{pk}\sqrt{\frac{d_1 + d_2}{3}} \tag{2.36}$$

### 2.3.2 Three phase CCSAB

#### 2.3.2.1 Voltage transfer ratio

The concept of inductor volt-second balance cannot be used to derive the input to output voltage transfer ratio since the inductor current is purely AC within a single switching cycle and the volt-seconds do not reset to the value in the beginning of an interval even within a half cycle. However, the concept of a duty ratio is still applicable in this case to distinguish between the modes where power is transferred from the input to the output and the modes where power is recirculated within the passive components.

Let us consider the condition where $t_c > T_d$. In this case, there are two states of the converter -power transfer mode and transition mode which repeat every $T_s/6$ in a switching period. The time interval in power transfer mode can be described using the duty ratio $d$ which is a function of the commutation interval $t_c$. So we can define the power transfer and transition interval duty ratio as

$$d\frac{T_s}{6} = \frac{T_s}{6} - t_c \tag{2.37}$$

$$(1-d)\frac{T_s}{6} = t_c \tag{2.38}$$

$$d = 1 - \frac{t_c}{T_s/6} \tag{2.39}$$

From Table 2.3, for the transition time interval we can derive the series inductor voltages as

$$v_{Lt} = L_s\frac{(0-(-I_c))}{t_c} = \frac{V_{in}+V_{out}}{3} \tag{2.40}$$

$$v_{Li} = L_s\frac{I_p-(-I_{min})}{t_c} = \frac{V_{out}-2V_{in}}{3} \tag{2.41}$$

$$v_{Lo} = L_s\frac{I_{min}-(-I_{max})}{t_c} = \frac{V_{in}-2V_{out}}{3} \tag{2.42}$$

Similarly we can derive the voltage across the series inductor for the power transfer interval

$$v_{Lt} = L_s\frac{I_p-0}{\frac{T_s}{6}-t_c} = \frac{V_{in}+V_{out}}{3} \tag{2.43}$$

$$v_{Li} = L_s\frac{-I_{max}-(-I_{min})}{\frac{T_s}{6}-t_c} = -2\left(\frac{V_{in}-V_{out}}{3}\right) \tag{2.44}$$

$$v_{Lo} = L_s\frac{I_c-I_{min}}{\frac{T_s}{6}-t_c} = \frac{V_{in}-V_{out}}{3} \tag{2.45}$$

Equating Eq. 2.42 and 2.44 and replacing $t_c$ with $d$ from Eq. 2.39, we get

$$M(d) = \frac{V_{out}}{V_{in}} = \frac{1+d}{2} \tag{2.46}$$

For the condition where $t_c < T_d$, we can see that

$$t_c \ll T_s \tag{2.47}$$

$$d \simeq 1 \tag{2.48}$$

$$M(d) \simeq 1 \tag{2.49}$$

$$V_{out} \simeq V_{in} \tag{2.50}$$

Fig 2.19 shows a plot of the voltage conversion ratio as a function of the duty ratio. From the plot, $d = 1$ refers to the condition where current commutation is instantaneous and in that condition the output voltage would be ideally equal to the input voltage. At the other extreme, $d = 0$ refers to the condition where the current commutation interval is equal to $T_s/6$ in which case the output voltage would be half the input voltage.

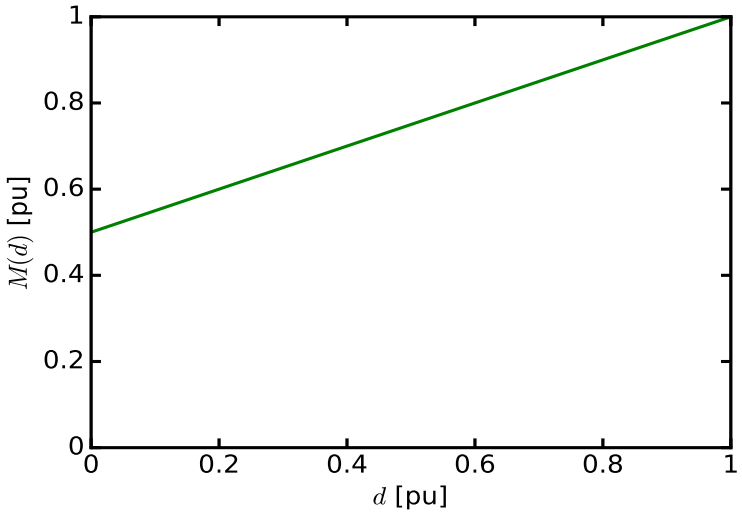


Figure 2.19: Plot of voltage conversion ratio $M(d)$ for a single output stage

#### 2.3.2.2 Output voltage regulation

The output voltage regulation of the three phase CCSAB can be derived from Eq.2.40 by substituting $V_{out}$ by $V_{in}$ and $t_c$.

$$3L_sI_c = V_{in}t_c + V_{out}t_c \tag{2.51}$$

$$3L_sI_c = V_{in}t_c + V_{in}\left(\frac{\frac{T_s}{2} - \frac{t_c}{2}}{T_s/6}\right)t_c \tag{2.52}$$

Simplifying the above expression, we derive a quadratic equation for $t_c$

$$V_{in}\frac{t_c^2}{2} - 2V_{in}t_c\frac{T_s}{6} + 3L_sI_c\frac{T_s}{6} = 0 \tag{2.53}$$

There are two solutions to this quadratic equation,

$$t_c = \frac{T_s}{3} \pm \frac{T_s}{3}\sqrt{1 - \frac{9I_cL_s}{T_sV_{in}}} \tag{2.54}$$

The appropriate root is

$$t_c = \frac{T_s}{3} - \frac{T_s}{3}\sqrt{1 - \frac{9I_cL_s}{T_sV_{in}}} \tag{2.55}$$

Using this solution and substituting in Eq. 2.46, we get

$$V_{out} = V_{in}\sqrt{1 - \frac{9I_cL_s}{T_sV_{in}}} \tag{2.56}$$

From the Taylor series expansion

$$\sqrt{1-\epsilon} = 1 - \frac{\epsilon}{2} - \frac{\epsilon^2}{8}\cdots \tag{2.57}$$

$$\sqrt{1-\epsilon} \simeq 1 - \frac{\epsilon}{2} \quad \text{if} \quad \epsilon \ll 1 \tag{2.58}$$

$$V_{out} \simeq V_{in}\left(1 - \frac{9I_cL_s}{2T_sV_{in}}\right) \quad \text{since} \quad \frac{9I_cL_s}{2T_sV_{in}} \ll 1 \tag{2.59}$$

Fig 2.20 shows a plot of the per-unit output rectified voltage as a function of the per-unit output DC current. The load regulation plot is linear even though the relationship in Eq. 2.56 is non-linear.

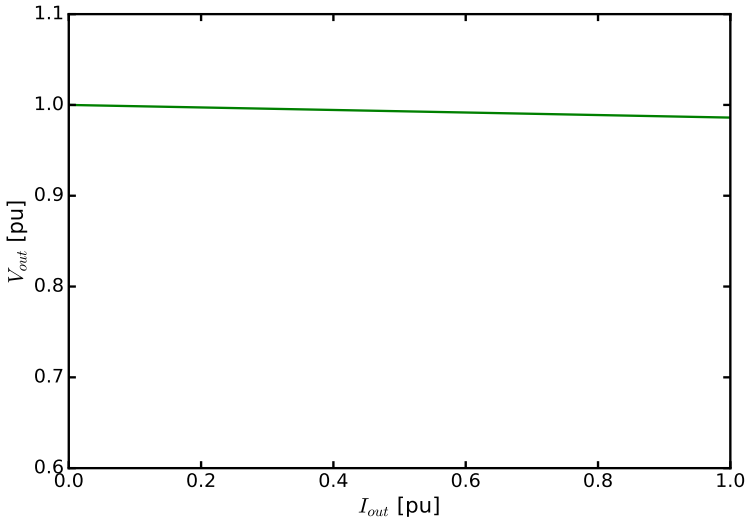


Figure 2.20: A plot of load regulation of the three phase CCSAB

#### 2.3.2.3 Series inductor

The series inductor $L_s$ can be sized from the input voltage, output voltage, commutation interval and assuming commutation current $I_c \simeq I_{out}$.

$$L_s = \frac{V_{in} + V_{out}}{3} \frac{t_c}{I_c} \tag{2.60}$$

#### 2.3.2.4 Output filter capacitor

The filter capacitor voltage and current for the operating condition $t_c > T_d$ are shown in Fig 2.12. The current ripple is defined as

$$2\Delta i_{out} = I_{max} - I_{min} \tag{2.61}$$

$$C_{out} = \frac{2\Delta i_{out} t_c}{\Delta v_{out}} \tag{2.62}$$

where $\Delta v_{out}$ is the output voltage ripple. The output filter capacitor can be sized based on the choice of $\Delta v_{out}$.

#### 2.3.2.5 Series coupling capacitor

The three phase coupling capacitors are designed with the same principles as the single phase - to minimize the AC impedance at the operating frequency.

$$X_{cs} = \frac{1}{2\pi F_s C_s} \tag{2.63}$$

#### 2.3.2.6 Effect of coupling capacitor ESR

It can be observed from the equivalent circuit of three phase cascade coupled CCSAB in Fig 2.15 that the coupling capacitors $C_s$ closer to the input stage will conduct more AC current than the coupling capacitors further away from the input stage. This unequal distribution of AC current in the coupling capacitors means that equivalent series resistance (ESR) will play a significant role in the rectified voltage of output stages connected close to the input stage. If $I_{rmsN}$ is the RMS value of the per phase coupling capacitor current in the Nth stage, then

current in the coupling capacitance of the (N-1)th stage will be

$$I_{rms(N-1)} = 2I_{rmsN} \tag{2.64}$$

At the other end, the RMS current in the coupling capacitor nearest to the input stage will be (the first stage does not include any coupling capacitors)

$$I_{rms2} = (N-1)I_{rmsn} \tag{2.65}$$

We can generalize this as

$$I_{rmsn} = (N-(n-1))I_{rmsN} \quad 1 \le n \le N \tag{2.66}$$

The AC voltage drop due to coupling capacitor ESR at every stage can be estimated as

$$V_{esrn} = I_{rmsn}R_{cs} \quad 2 \le n \le N \tag{2.67}$$

This voltage drop due to capacitor ESR will reduce the AC voltage applied to every output stage depending on the RMS phase current of each output stage coupling capacitors. If $V_{iLNn}$ is the line-to-neutral AC voltage applied to the nth stage,

$$V_{iLN1} = \frac{1}{\sqrt{3}}V_{in}\sqrt{\frac{2}{3}} \tag{2.68}$$

$$V_{iLNn} = V_{iLN(n-1)} - V_{esrn} \quad 2 \le n \le N \tag{2.69}$$

$$V_{in-n} = V_{iLNn}\sqrt{3}\sqrt{\frac{3}{2}} \quad 2 \le n \le N \tag{2.70}$$

The nth AC voltage $V_{in-n}$ can be used to estimate the rectified output voltage of the nth output stage $V_{outn}$ using Eq. 2.52 and Eq. 2.46. Fig 2.21 shows the analytical estimated DC voltage distribution among the output stages. As can be observed from from the figure, the output voltage per stage drops as we move away from the input stage . However after about 15 stages, since the coupling capacitor current amplitute is reduced, the effect of the ESR voltage drop is not noticeable.

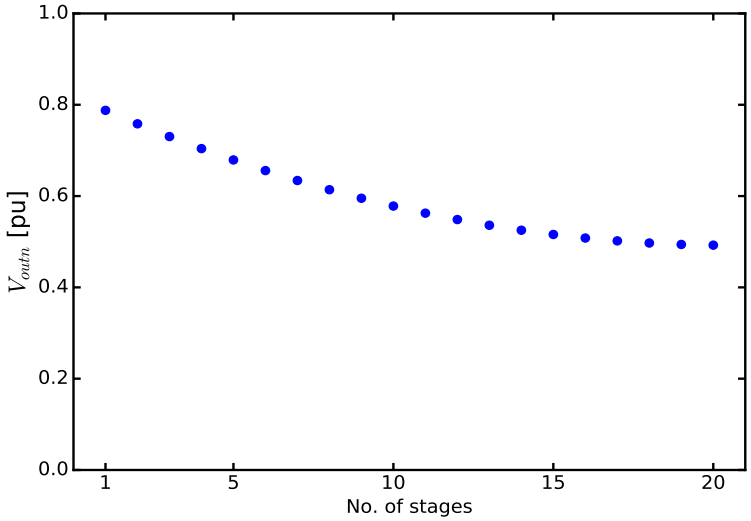


Figure 2.21: Effect of coupling capacitor ESR on output voltage across different stages compared in pu basis normalized to input voltage $V_{in}$. $R_c$=47mΩ, Output stages=20.

#### 2.3.2.7 Effect of on-state voltage of semiconductor switches

The discussion so far has assumed that the active switching devices on the input stage and the passive diodes on the output stage are ideal with no forward voltage drop and instantaneous switching characteristics. Consider the situation where an input stage is followed by a single

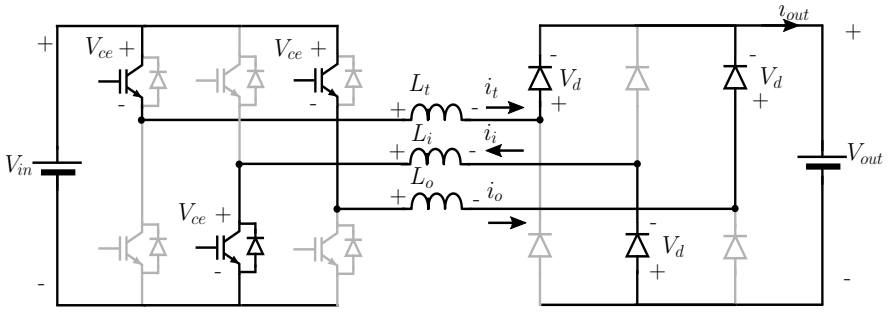


Figure 2.22: Effect of on-state voltage drop in semiconductor switches

output stage. For the input voltage of $V_{in}$, if $V_{out-ideal}$ is the rectified output voltage under ideal switching device conditions, then we can account for the on-state voltage drop of the input stage $V_{ce}$ and forward voltage drop of the output stage $V_d$ as

$$V_{out} = V_{out-ideal} - 2V_{ce} - 2V_d \tag{2.71}$$

## 2.4 Dynamic modeling

This section focuses on the dynamic modeling and control methods of the single phase CCSAB. There is no difference in the dynamic behavior of cascade coupled and parallel coupled converters. There is however, a notable difference in control methods of the single phase when compared to the three phase CCSAB. The switching scheme of choice of the three phase CCSAB in this chapter is the six step sequence. In this technique, the duty ratio is decided by the circuit parameters and switching frequency and not actively managed by a modulation sequence. Since it is not possible to affect the output voltage using duty ratio in case of the three phase CCSAB, the remainder of this chapter will focus on the modeling and control issues with the single phase CCSAB. The dynamic model for the CCSAB is based on simplified averaged equivalent circuit of the PWM switch, which is a convenient methodology to model these converters [143, 144]. The state equivalent circuit is subsequently obtained by linearizing the averaged model around a steady state operating point.

### 2.4.1 Averaged equivalent circuit

The converter dynamic behavior can be expressed using an averaged equivalent circuit model illustrated in Fig 2.23. The averaged equivalent circuit represents the relationship between the steady state DC quantities of the inductor current $I_L$ the filter capacitor voltage $V_{out}$ and input voltage $V_{in}$. The dependent sources $d_E V_{dc}$ and $d_E I_L$ represent the average characteristics of the PWM switch and diode for one half of the switching cycle. Each of the capacitors $C_s$ is replaced by a short circuit, since the capacitor is assumed to have negligible reactance at the inverter operating frequency. $N$ refers to the number of branches that are coupled in series at the output. $d_E$ represents the equivalent duty ratio for discontinuous mode of operation, $d_1$ is the actual duty ratio applied to the switches($0 < d_1 < 1$) and $f_{sw}$ is the switching frequency.

Using the governing equations for the circuit during its conduction and idle states, the averaged equivalent duty cycle for the discontinuous mode of operation for a single stage can

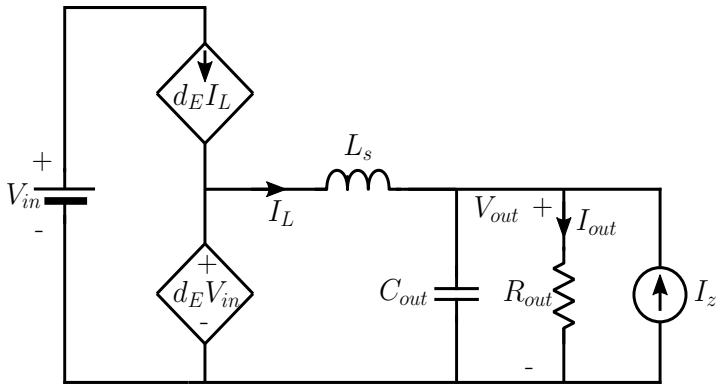


Figure 2.23: Averaged equivalent circuit for one half switching cycle

be represented as

$$d_E = \frac{V_{outn}}{V_{in}} = \frac{1 - \dfrac{2L_s F_s I_{out}}{{d_1}^2 V_{in}}}{1 + \dfrac{2L_s F_s I_{out}}{{d_1}^2 V_{in}}} \tag{2.72}$$

For typical design parameters and operation under normal conditions, the load dependent terms of the duty ratio are rather small compared to unity, i.e.

$$\frac{2L_s f_{sw} I_{out}}{{d_1}^2 V_{in}} \ll 1 \tag{2.73}$$

In such cases, Eq. 2.72 can be simplified as as

$$d_E \simeq 1 - \frac{4L_s F_s I_{out}}{{d_1}^2 V_{in}} \tag{2.74}$$

### 2.4.2 Small signal equivalent circuit

Since the model described by Fig 2.23 and (2.72) are nonlinear, in order to develop a closed loop regulator to maintain adequate control of output voltage it is necessary to develop small signal transfer functions that describe the localized dynamic behavior of the power converter at its steady state operating point. From Fig 2.23, the averaged behavior of the PWM switch can be represented by dependent sources $d_E V_{dc}$ and $d_E I_L$, where $V_{in}$ is the applied switch voltage blocking voltage and $I_L$ is the switch conduction current. Each of these variables- $I_L$, $V_{in}$ and $d_E$ can independently determine the behavior of the converter. Therefore, the variations of

the dependent sources with respect to each of these independent factors evaluated at a steady state operating point will provide the small signal equivalent circuit.

Let the steady state quantities be denoted by $(D_1, I_L, V_{in})$ and the small signal perturbations be denoted by $(\tilde{d}_1, \tilde{i}_L, \tilde{v}_{in})$. The small signal averaged equivalent circuit model may be illustrated as shown in Fig 2.24, which also includes a perturbation source for the output load current $\tilde{i}_z$. The coefficients of the small signal dependent current sources and voltage sources in the equivalent circuit may be determined as partial derivatives of the corresponding nonlinear relationships with respect to the appropriate independent variables to be

$$D_T = \frac{\partial(d_E I_L)}{\partial I_L} \tag{2.75}$$

$$G_T = \frac{\partial(d_E I_L)}{\partial V_{in}} \tag{2.76}$$

$$I_T = \frac{\partial(d_E I_L)}{\partial d_1} \tag{2.77}$$

$$R_P = \frac{\partial(d_E V_{in})}{\partial I_L} \tag{2.78}$$

$$D_P = \frac{\partial(d_E V_{in})}{\partial V_{in}} \tag{2.79}$$

$$V_P = \frac{\partial(d_E V_{in})}{\partial d_1} \tag{2.80}$$

Using the simplified expression of $d_E$, the coefficients of the dependent sources are defined as

$$D_T = 1 - \frac{8L_s I_L}{D_1^2 V_{in} T_s} \tag{2.81}$$

$$G_T = \frac{4L_s I_L^2}{D_1^2 V_{in}^2 T_s} \tag{2.82}$$

$$I_T = \frac{8L_s I_L^2}{D_1^3 V_{in} T_s} \tag{2.83}$$

$$R_P = -\frac{8L_s I_L}{D_1^2 T_s} \tag{2.84}$$

$$D_P = 1 \tag{2.85}$$

$$V_P = \frac{8L_s I_L}{D_1^3 T_s} \tag{2.86}$$

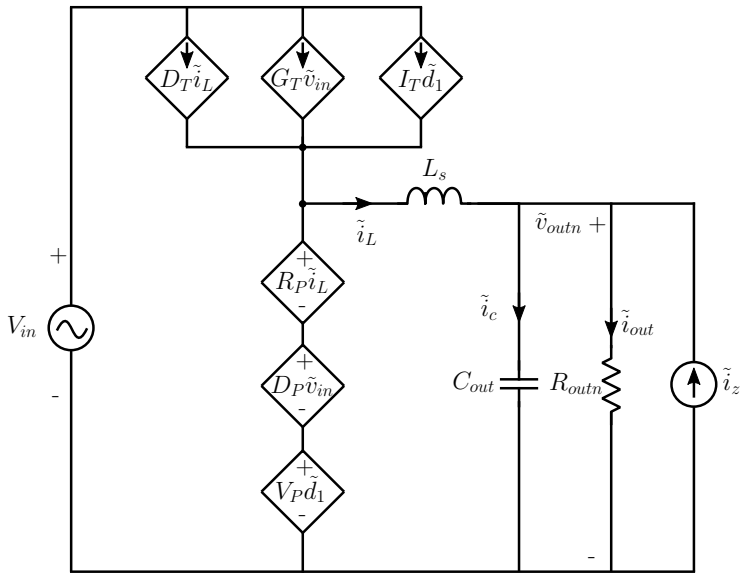


Figure 2.24: Linearized averaged equivalent circuit

### 2.4.3 Small signal state space model

In order to obtain the small signal state space model, ee can write the KVL and KCL equations for the equivalent circuit in Fig 2.24.

$$L_s\frac{d\tilde{i}_L}{dt} = R_P\tilde{i}_L + D_P\tilde{v}_{in} + V_P\tilde{d}_1 - \tilde{v}_{outn} \tag{2.87}$$

$$C_f\frac{d\tilde{v}_{out}}{dt} = \tilde{i}_L - \frac{\tilde{v}_{outn}}{R_{outn}} + \tilde{i}_z \tag{2.88}$$

These relationships may be recast as a matrix representation to form the state space dynamic model valid for small perturbations near the operating point.

$$\begin{bmatrix} \frac{d\tilde{i}_L}{dt} \\ \frac{d\tilde{v}_{outn}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{R_P}{L_s} & -\frac{1}{L_s} \\ \frac{1}{C_{out}} & -\frac{1}{C_{out}R_{outn}} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_{outn} \end{bmatrix} + \begin{bmatrix} \frac{V_P}{L_s} \\ 0 \end{bmatrix} \tilde{d}_1 + \begin{bmatrix} \frac{D_P}{L_s} \\ 0 \end{bmatrix} \tilde{v}_{in} + \begin{bmatrix} 0 \\ \frac{1}{C_{out}} \end{bmatrix} \tilde{i}_z \tag{2.89}$$

$$\tilde{v}_{outn} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_{outn} \end{bmatrix} \tag{2.90}$$

$$\tilde{i}_L = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_{outn} \end{bmatrix} \tag{2.91}$$

The state space equations are in the canonical form

$$\dot{\tilde{x}} = A\tilde{x} + B_1\tilde{d}_1 + B_2\tilde{v}_{in} + B_3\tilde{i}_z \tag{2.92}$$

$$\tilde{v}_{out} = C\tilde{x} \tag{2.93}$$

$$\tilde{i}_L = D\tilde{x} \tag{2.94}$$

where the $A$, $B$, $C$ and $B_i$ matrices are appropriately defined.

## 2.5 Converter transfer functions

### 2.5.1 Control voltage gain

Using the state space model described in (2.92) and (2.93), the open loop control-to-output transfer function may be determined as ($\tilde{v}_{in}, \tilde{i}_z = 0$)

$$G_{vd}(s) = \frac{\tilde{v}_{outn}(s)}{\tilde{d}_1(s)} = C[sI - A]^{-1}B_1 \tag{2.95}$$

$$G_{vd}(s) = \frac{V_P}{1 + \frac{1}{Q_p}\frac{s}{\omega_p} + \frac{s^2}{\omega_p^2}} \tag{2.96}$$

where

$$\omega_p = \sqrt{\frac{1}{L_s C_{out}}} \tag{2.97}$$

$$Q_p = \frac{\sqrt{L_s C_{out}\left(1 - \frac{R_P}{R_{outn}}\right)}}{L_s C_{out}\left(\frac{1}{C_f R_{outn}} - \frac{R_P}{L_s}\right)} \approx \frac{\sqrt{\frac{L_s}{C_{out}}}}{-R_P} \tag{2.98}$$

for the condition where

$$\frac{-R_P}{R_{outn}} \ll 1 \tag{2.99}$$

$$\frac{1}{C_f R_{outn}} \ll \frac{R_P}{L_s} \tag{2.100}$$

For low values of $Q_p$, the transfer function can be further approximated as

$$G_{vd}(s) \approx \frac{V_P}{(1 + \frac{s}{\omega_p Q_p})(1 + \frac{s}{\omega_p / Q_p})} \approx \frac{V_P}{1 + \frac{s}{\omega_o}} \tag{2.101}$$

where

$$\omega_o = Q_P \omega_p = \frac{D_1^2 t_{sw}}{8 L_s C_f I_L} \tag{2.102}$$

and the high frequency pole $\omega_p/Q_p$ has been neglected in the low frequency band.

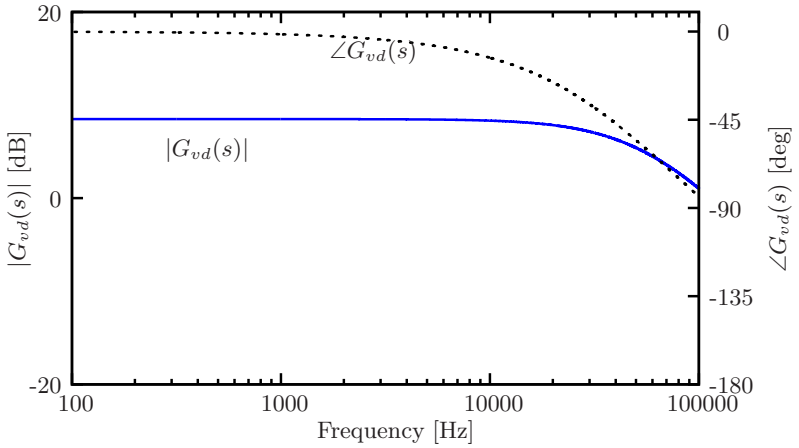


Figure 2.25: Control voltage gain transfer function

### 2.5.2 Audio susceptibility

The input-to-output voltage transfer function is defined as ($\tilde{d}_1, \tilde{i}_z = 0$)

$$G_{vv}(s) = \frac{\tilde{v}_{outn}(s)}{\tilde{v}_{in}(s)} = C[sI - A]^{-1} B_2 \tag{2.103}$$

$$G_{vv}(s) = \frac{D_P}{1 + \frac{1}{Q_p}\frac{s}{\omega_p} + \frac{s^2}{\omega_p^2}} \tag{2.104}$$

### 2.5.3 Output impedance

The output current to output voltage transfer function is defined as ($\tilde{d}_1, \tilde{v}_{dc} = 0$)

$$G_{vi}(s) = \frac{\tilde{v}_{outn}(s)}{\tilde{i}_z(s)} = C[sI - A]^{-1} B_3 \tag{2.105}$$

$$G_{vi}(s) = \frac{-R_P\left(1 + \frac{s}{\omega_{rz}}\right)}{1 + \frac{1}{Q_p}\frac{s}{\omega_p} + \frac{s^2}{\omega_p^2}} \tag{2.106}$$

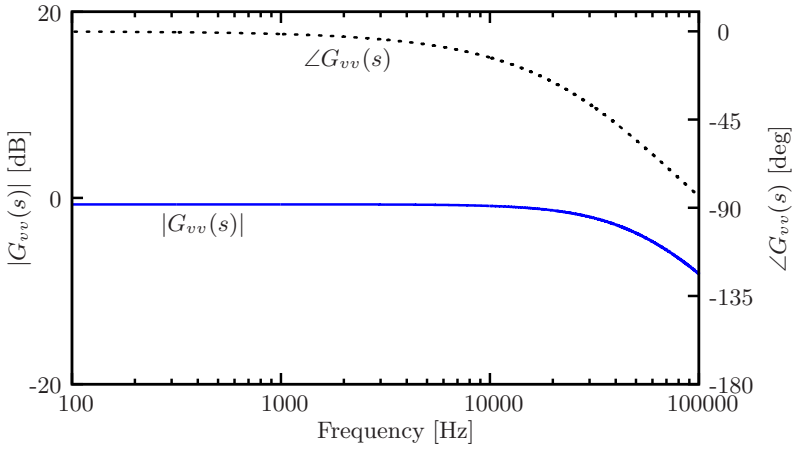


Figure 2.26: Audio susceptibility transfer function

where

$$\omega_{rz} = \frac{-R_P}{L_s} \tag{2.107}$$

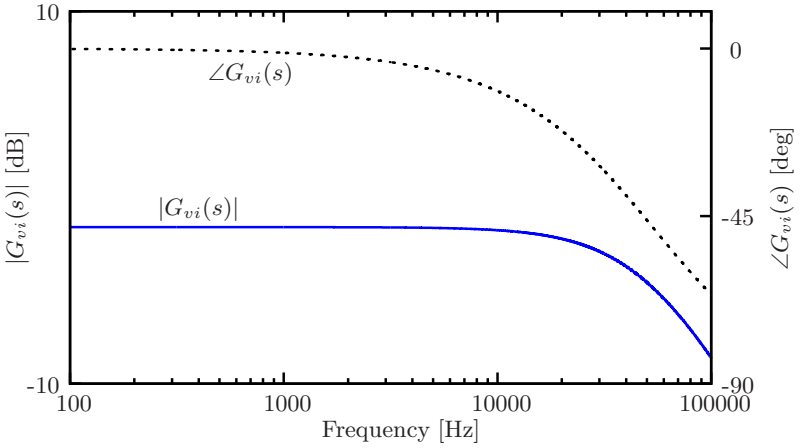


Figure 2.27: Output impedance transfer function

## 2.6 Regulator design

### 2.6.1 PI regulator

A block diagram of the proposed closed loop regulator is shown in Fig 2.28. Since the small signal transfer function of the converter is dominated by a first order pole in the low frequency

band is convenient to design a proportional-integral (PI) regulator, whose inverted zero is placed at the low frequency pole of the converter. The desired gain-crossover-frequency ($GCF_d$) is a design parameter compared with the actual gain-crossover-frequency ($GCF_a$) of the plant.

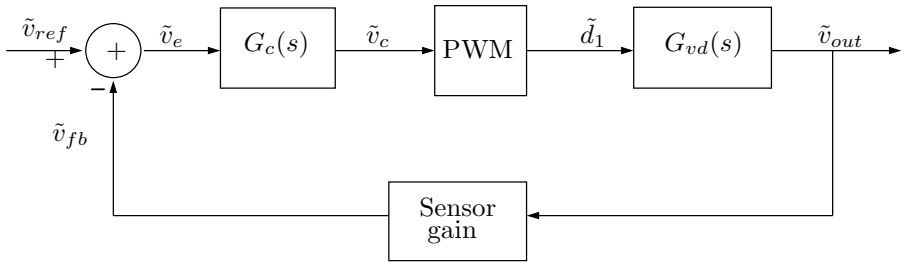


Figure 2.28: Block diagram of closed loop regulator

The PI regulator transfer function may be represented as

$$G_c(s) = K_p\left(1 + \frac{\omega_c}{s}\right) \tag{2.108}$$

where, tthe regulator gain $K_p$ is defined as

$$K_p = \frac{GCF_d}{GCF_a} \tag{2.109}$$

The regulator compensating zero $\omega_c$ is located at the -3dB frequency of the dominant lower frequency pole of $G_{vd}(s)$, $\omega_o$.

### 2.6.2 Loop gain of the regulator

The dc gain of regulator gain is adjusted for a bandwidth of 1kHz. The loop gain is defined as

$$G_{lg}(s) = G_c(s)G_{vd}(s) \tag{2.110}$$

Bode plots of the converter transfer function ($G_{vd}$), regulator transfer function ($G_c$), and the loop gain transfer function ($G_{lg}$) are illustrated in Fig 2.29.

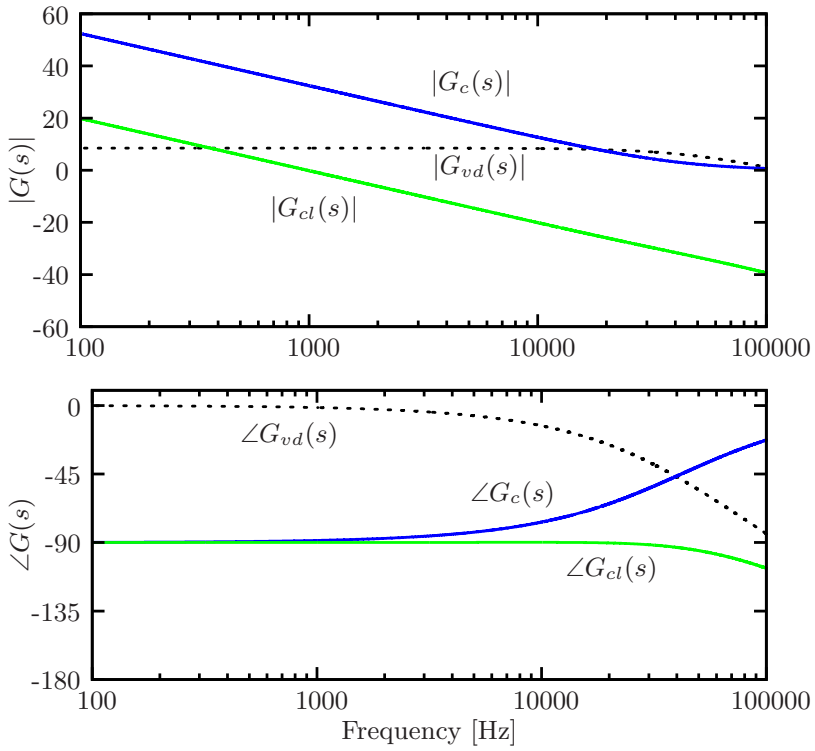


Figure 2.29: Effect of PI controller on control voltage gain

### 2.6.3 Effect of regulator on audio susceptibility

The audio susceptibility of the converter in the presence of the PI regulator may be determined as ($\tilde{d}_1 = -G_c(s)\tilde{v}_{outn}, \tilde{i}_z = 0$).

$$G_{vvc}(s) = \frac{\tilde{v}_{outn}(s)}{\tilde{v}_{dc}(s)} = \frac{G_{vv}(s)}{1+G_{lg}(s)} \tag{2.111}$$

The Bode plots of the audio susceptibility of the open loop converter (dotted lines) and the closed loop converter (solid line) are illustrated in Fig 2.30. The performance improvement at low frequencies below the bandwidth of the regulator is readily evident.

### 2.6.4 Effect of regulator on output impedance

The output impedance of the converter in the presence of the PI regulator may be determined as ($\tilde{d}_1 = -G_c(s)\tilde{v}_{outn}, \tilde{v}_{dc} = 0$).

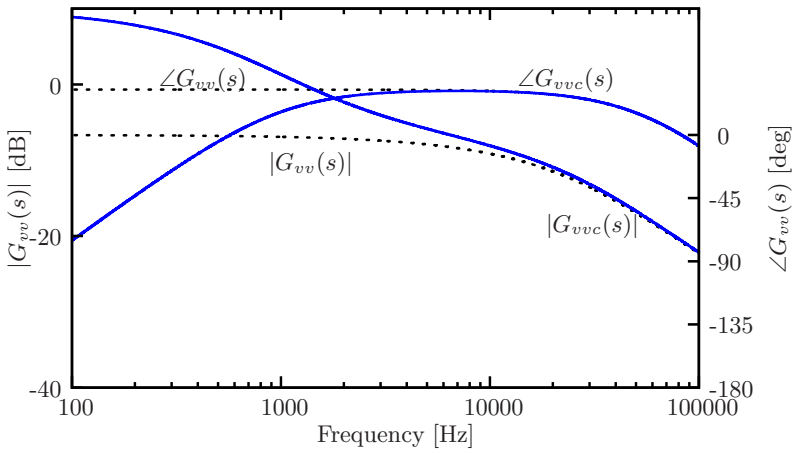


Figure 2.30: Effect of PI controller on audio susceptibility

$$G_{vic}(s) = \frac{\tilde{v}_{outn}(s)}{\tilde{i}_z(s)} = \frac{G_{vi}(s)}{1 + G_{lg}(s)} \tag{2.112}$$

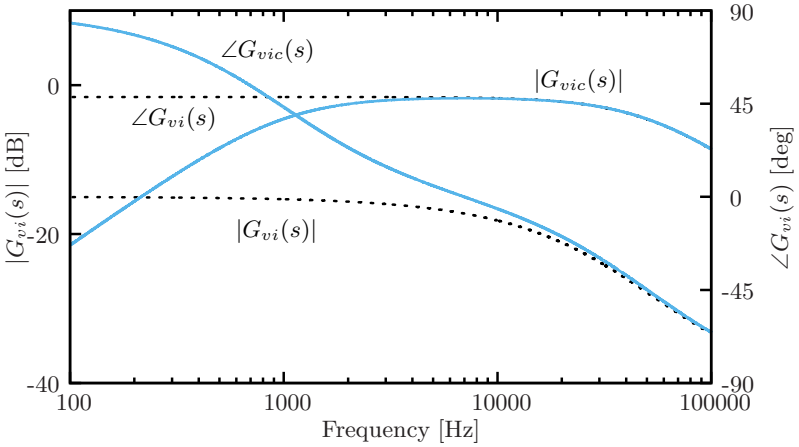


Figure 2.31: Effect of PI controller on output impedance

The Bode plots of the output impedance of the open loop converter (dotted lines) and the closed loop converter (solid line) are illustrated in Fig 2.31. The performance improvement at low frequencies below the bandwidth of the regulator is readily evident.

### 2.6.5 PI controller response in time domain

The operation of the converter has been verified via simulation in PLECS in the time domain. In Fig 2.32, a step change in source voltage was applied at 15 ms. Traces of AC link voltage, AC link current and output voltage are illustrated in the figure, illustrating the excellent response of the converter. In Fig 2.33, a step change in load current was applied at 15 ms. As can be observed, the PI regulator quickly adjusts for step changes and output voltage is well regulated under both conditions.

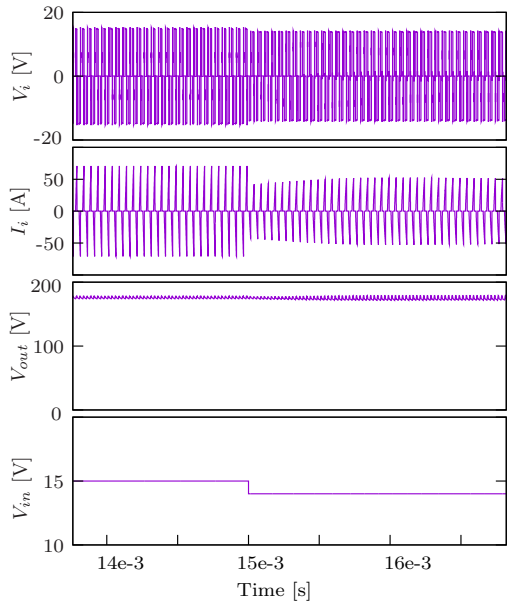


Figure 2.32: PI controller action during step change during source voltage dip from $V_{in}$ = 15V to 14V. $V_{out} = 176V$.

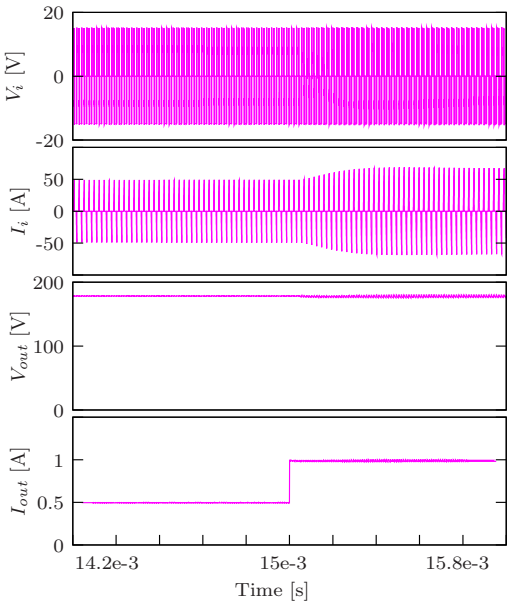


Figure 2.33: PI controller action during step change in load current from $I_{out}$ = 0.5A to 1A. $V_{out} = 176V$.

## 2.7 Summary

This chapter has introduced a novel multilevel DC-DC unidirectional boost topology. The coupling from the input stage inverter to the output stage rectifier is provided by series coupling capacitors. The voltage magnification is achieved by multiple output stages in input-parallel output-series architecture. The topology and steady state operation of the converter

in both single phase and three phase variants is discussed. The design considerations of this topology are also discussed in some detail. The averaged equivalent circuit model of the single phase CCSAB topology is presented. The small signal dynamic model of the converter is then derived from the averaged model using the concept of effective duty ratio. The state space matrix is used to derive the control-to-output transfer function. A continuous time PI regulator is designed for the desired bandwidth with excellent dynamic properties.

CHAPTER 3

# Capacitor Coupled Dual Active Bridge Converter

This chapter introduces a novel transformer-less bidirectional multilevel DC-DC converter topology. This topology is derived from the transformer coupled dual active bridge topology with the magnetic transformer coupling replaced by capacitive coupling. The converter architecture is described in Section I. The topology and operation of the converter under steady state conditions with fixed frequency phase shift modulation is presented in Section II. The design considerations for this new architecture is described in Section III. Section IV examines the small signal dynamics of the proposed converter using the concept of dynamic phasors.

## 3.1 Converter architecture

An architectural schematic of the single phase Capacitor Coupled Dual Active Bridge (CCDAB) converter is shown in Fig 3.1. The dc source $V_{in}$ feeds a high frequency full bridge inverter formed by the MOSFETs S1-S4. The AC output $v_i$ of the high frequency inverter is available across output terminals. This voltage is applied across multiple parallel branches of H-bridge controlled rectifiers. Each output stage consists of the H-bridge rectifier and a series inductor $L_s$. The multiple output H-bridge rectifiers are coupled to the input H-bridge using series

coupling capacitors $C_{sa}$ and $C_{sb}$. Finally, the output voltage of each of the H-bridge rectifiers is maintained stiff using a local filter capacitor $C_{out}$.

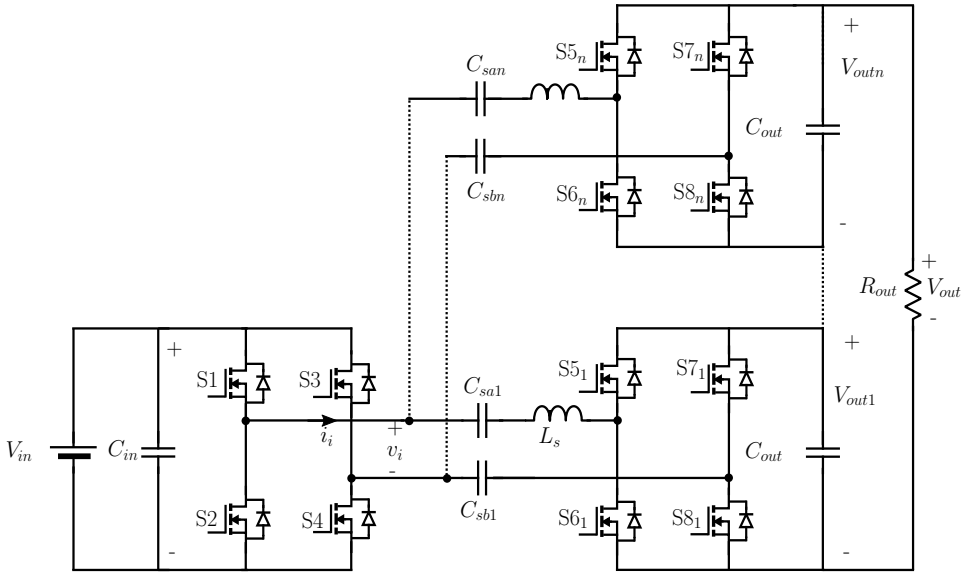


Figure 3.1: Architectural schematic of single phase capacitor coupled dual active bridge converter

The single phase CCDAB can be compared to the single phase CCSAB introduced in the previous chapter. As in the the case of the CCSAB, the DC output of each H-bridge rectifier in the output stage are connected in series. But different from the single phase CCSAB a feature of this topology is that the output voltage of each stage can be individually controlled by modulating the switching states of the output H-bridge of that stage. There are again two possible configurations for coupling the input stage to the multiple output stages- parallel-coupled configuration as shown in Fig 3.2 and cascade-coupled configuration as shown in Fig 3.3.

The same multilevel architecture can be once again extended to three phases. A high frequency two-level three phase IGBT or MOSFET based inverter feeds multiple three phase active rectifiers. The addition of coupling capacitors at the input of every rectifier stage allows us to connect the rectifier outputs in series. Each three phase rectifier includes series inductance $L_s$ in each phase and an output filter capacitance $C_{out}$. An architectural schematic

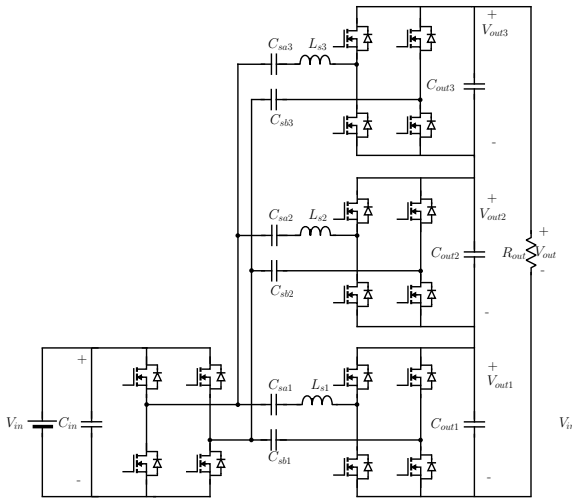


Figure 3.2: Parallel capacitor coupled CCDAB with three output stages

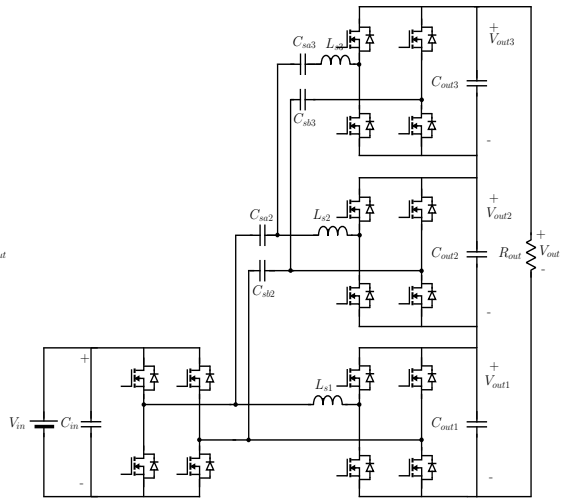


Figure 3.3: Cascade capacitor coupled CCDAB with three output stages

of the three phase CCSAB is shown in Fig 3.4.

## 3.2 Steady state analysis

This section and the following sections of this chapter will focus on the characteristics of the single phase CCDAB. The following simplifying assumptions are made in studying the circuit:

- The converter operation during various PWM intervals is assumed to be linear, ie ZVS interval in inductor current is excluded.
- Phase shift modulation is the preferred modulation scheme.
- The effect of modulation strategy is only to regulate the power flow between fixed voltage sources at the input and output.
- Second order effects like ESR of series inductor are ignored.

### 3.2.1 Single stage equivalent circuit

Fig 4.17 shows the single stage equivalent circuit of the $n$-stage single phase CCDAB. The series coupling capacitors of CCDAB are assumed to be of negligible reactance at the switching

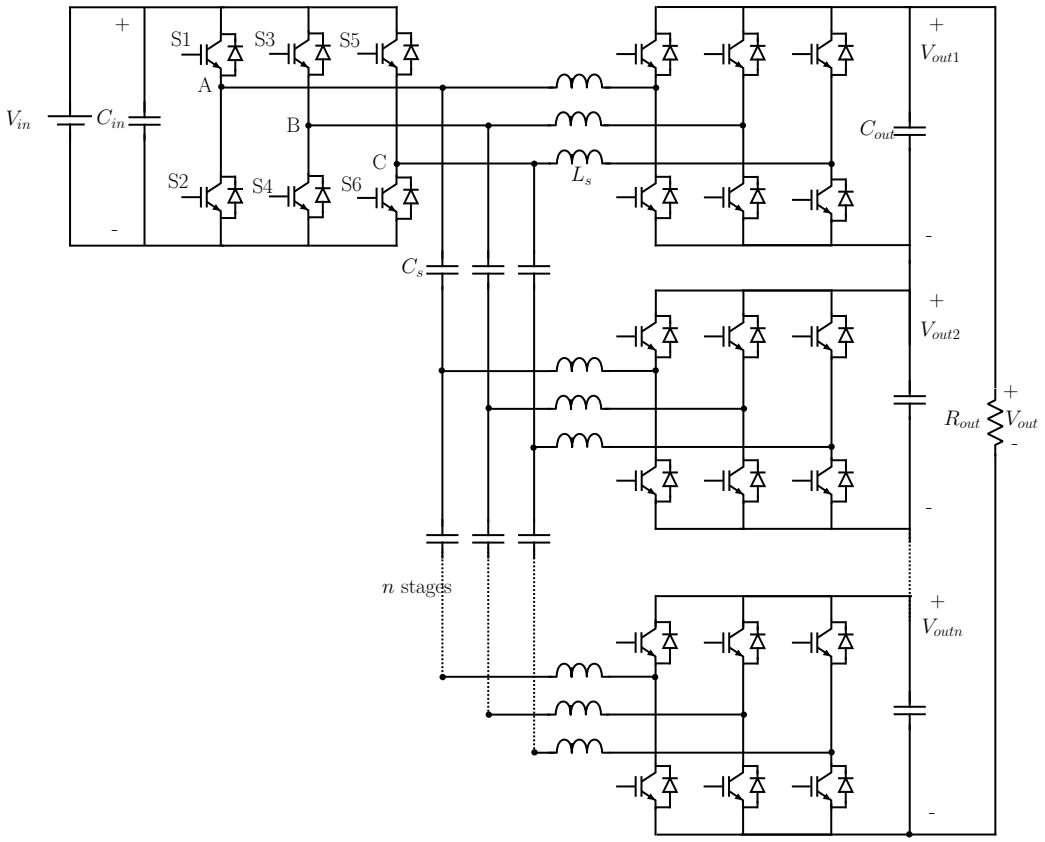


Figure 3.4: Architectural schematic of the three phase capacitor coupled dual active bridge converter

frequency and have been replaced by a short circuit. The single stage equivalent circuit has $1/n$ output power of the full CCDAB. There is no change in input voltage, but the input current is reduced by $1/n$. On the output side, the output voltage is $V_{outn}$ while the inductor current is $i_{Ln}$. The results from the analysis of the single stage circuit can be readily 'unwound' to extend the results to the n-stage converter as required. T The typical waveforms of the various electrical quantities over one complete switching cycle are shown in Fig 3.6. The power flow by adjusting the phase difference between the input and output voltage stages. The phase of the input voltage bridge is $\theta_i$ and the phase of the output voltage bridge is $\theta_{on}$. The phase shift between the the input and output bridges is $\phi$ . $T_\phi$ is the phase shift expressed in units of time. $t_D$ is the time interval where the output voltage of the input or output bridge is positive while the current direction is negative. This is the diode conduction interval. For the remainder of

this analysis, $\theta_i = 0$ rad.

$$\phi_n = \theta_i - \theta_{on} \tag{3.1}$$

$$T_{\phi n} = \frac{\phi_n}{2\pi F_s} \tag{3.2}$$

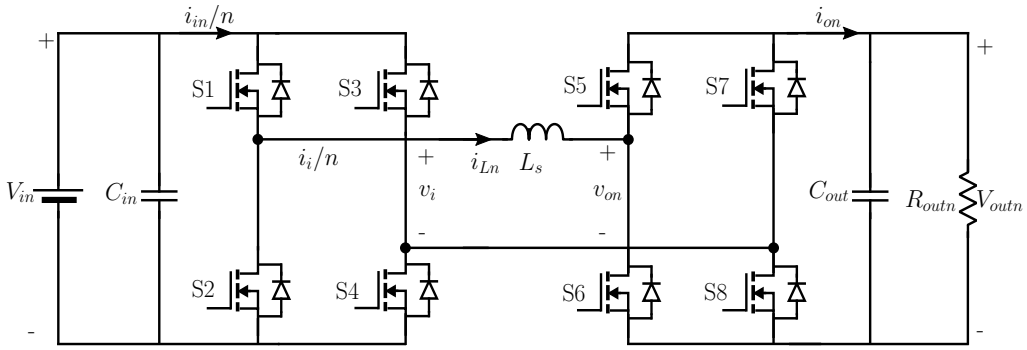


Figure 3.5: Simplified single stage equivalent circuit for CCDAB

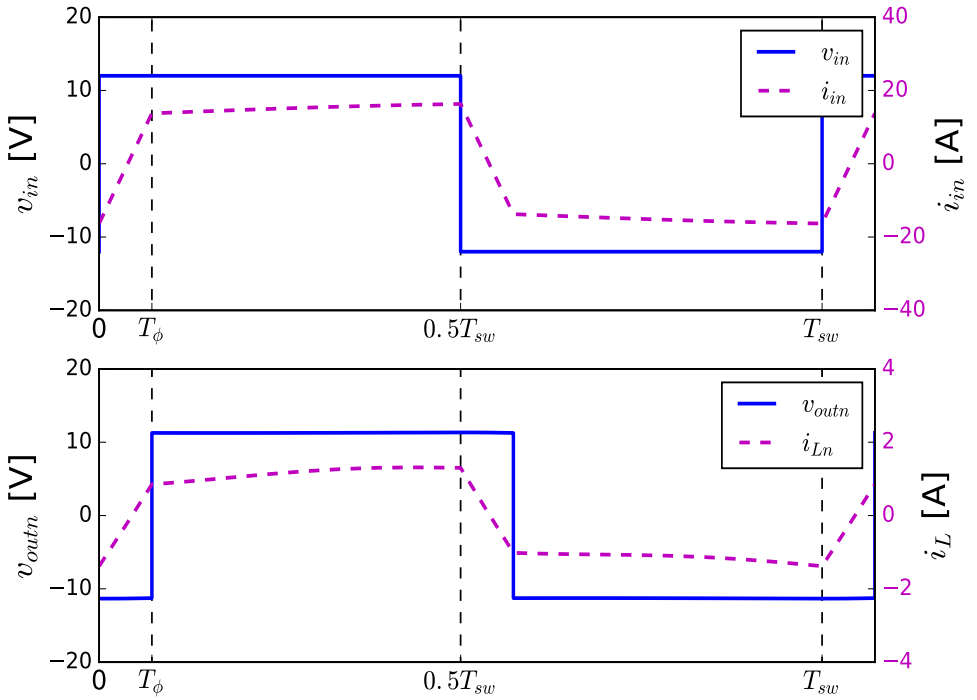


Figure 3.6: Typical voltage and current waveforms of input and output stages of CCDAB with phase-shift modulation

#### 3.2.1.1 Input and output voltage

The AC side voltages across the two ends of the inductor may be expressed as

$$v_i(t) = \begin{cases} +V_{in} & \text{if S1,S4 ON} \\ 0 & \text{if S1,S3 ON; or S2,S4 ON} \\ -V_{in} & \text{if S2,S3 ON} \end{cases} \tag{3.3}$$

$$v_{on}(t) = \begin{cases} +V_{outn} & \text{if S5,S8 ON} \\ 0 & \text{if S5,S7 ON; or S6,S8 ON} \\ -V_{outn} & \text{if S6,S7 ON} \end{cases} \tag{3.4}$$

The actual DC output will be

$$V_{out} = nV_{outn} \tag{3.5}$$

#### 3.2.1.2 Input and output current

The steady state inductor current waveform during the various intervals may be expressed as a piecewise linear function as

$$i_L(t) = \begin{cases} I_{L0} + \dfrac{V_{in} + V_{outn}}{L_s} t & t \le T_\phi \\ I_{L1} + \dfrac{V_{in} - V_{outn}}{L_s} t & T_\phi \le t \le 0.5T_s \\ -I_{L0} - \dfrac{V_{in} + V_{outn}}{L_s} t & 0.5T_s \le t \le 0.5T_s + T_\phi \\ -I_{L1} - \dfrac{V_{in} - V_{outn}}{L_s} t & 0.5T_s + T_\phi \le t \le T_s \end{cases} \tag{3.6}$$

where $I_{L0}$ is the current at the beginning of the switching half-cycle, $I_{L1}$ is the current at time $t = T_\phi$ that can be determined as

$$I_{L0} = \frac{\pi(V_{outn} - V_{in}) - 2|\theta_{on}|V_{outn}}{4\pi F_s L_s} \tag{3.7}$$

$$I_{L1} = \frac{\pi(V_{outn} - V_{in}) + 2|\theta_{on}|V_{in}}{4\pi F_s L_s} \tag{3.8}$$

by relating the boundary conditions and through symmetry. Furthermore, the diode conduction interval may be determined to be

$$t_D = \frac{|I_{L0}|L_s}{V_{in} + V_{outn}} \tag{3.9}$$

From the solution to the inductor current waveform, its RMS value and peak value may be readily determined. Furthermore, assuming all the output stages operate at the same phase $\theta_{on}$ the AC current at the input stage may be determined using

$$i_i = n i_{Ln} \tag{3.10}$$

#### 3.2.1.3 Input and output power

Using the relationships for voltage and current, the average power throughput may be determined to be

$$P_o = \frac{V_{in} V_{outn} \phi (\pi - |\phi|)}{2\pi^2 F_s L_s} \approx \frac{V_{in} V_{outn}}{2\pi F_s L_s} \phi [\text{for small } \phi] \tag{3.11}$$

Furthermore, the apparent power or kVA throughput of the converter can be defined as

$$S = V_{in} I_{Lrms} \tag{3.12}$$

From $S$ and $P$, reactive power transfer is defined as

$$Q = \sqrt{S^2 - P_o^2} \tag{3.13}$$

### 3.2.2 N stage model

Similar to the CCSAB, the CCDAB equivalent circuit can be extended to n series connected output stages to realize any output voltage from 0 to $nV_{outn}$. For the series connected coupling capacitors, the DC voltage distribution will be similar to table 2.2.

## 3.3 Design considerations

### 3.3.1 Effect of transfer ratio

The voltage transfer ratio of the equivalent single stage converter is defined as $v = V_{outn}/V_{in}$. This is different from the transformer voltage transformation ratio $n$. The transfer ratio is a design factor that has a direct effect on the reactive power transfer of the DAB converter.

Fig 3.7 shows a plot of per-unit real power $P$, reactive power $Q$ and apparent power $S$ as a function of $v$. The real power plot is scaled such that 1 pu of real power is transferred at $v = 1$. As shown in Fig 3.7, the real power transfer is directly proportional to the voltage transfer ratio. However, as $v > 1$, the reactive power pu increases much faster than the real power. This effect can also be observed when the $v < 1$. The effect of this reactive power is conduction loss in switches, conduction loss in transformer and higher ripple current in input and output capacitors. The minimum reactive power transfer in a DAB converter occurs only when $v = 1$. This means that the DAB converter topology must be operated at this operating point and is is unsuitable for voltage transfer ratios that are very high or very low. It is prudent to use the turns ratio of the transformer in the case of TCDAB or number of stages in the case of CCDAB to realize the voltage transformation.

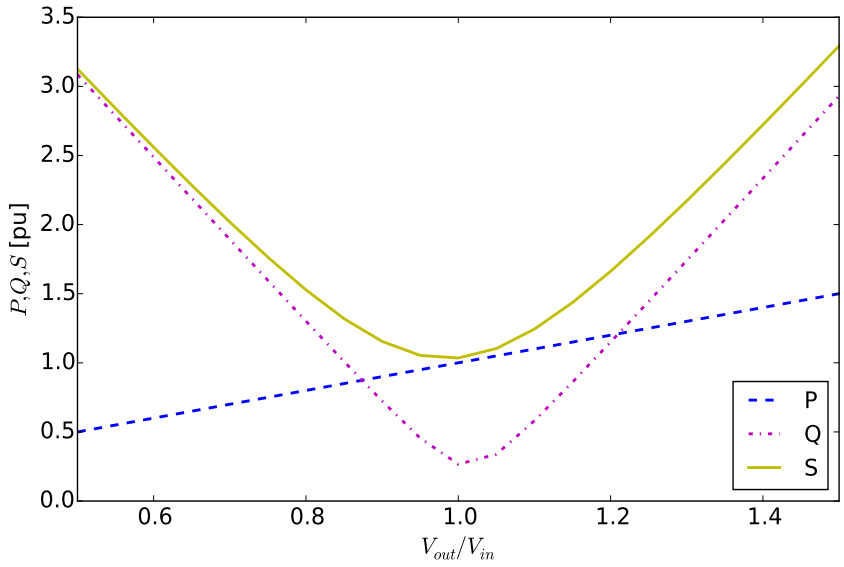


Figure 3.7: Effect of transfer ratio $V_{out}/V_{in}$ on real power pu $P$, reactive power pu $Q$ and apparent power pu $S$. $V_{in} = 12$V, $P_{out} = 150$W, $n = 1$, $\phi = 0.05\pi$ rad.

### 3.3.2 Effect of $\Phi$

As shown in (3.11), the output power of a DAB converter can be expressed as a function of the displacement phase difference between the input ac voltage $v_i(t)$ and output ac voltage $v_o(t)$.

Fig 3.8 shows the effect of this phase difference $\phi$ on the per-unit real, reactive and apparent power. The figure is per-unitized to the real power transferred at $\phi/\pi = 0.05$. For small angles of $\phi$, it can be observed that $P$ vs $\phi$ is linear, and the amount reactive power throughput is less than 1 pu, and is reasonably flat . But if the phase difference is increased more than this small angle $\phi/\pi > 0.15$, the per-unit reactive power $Q$ is more than 1 pu. This figure illustrates that the DAB converter would have reasonable performance when the the operating phase shift cannot be much greater than $0.1\pi$ rad. In reality, this leads to a limit in the dynamic range that is available for providing output regulation in the presence of load changes.

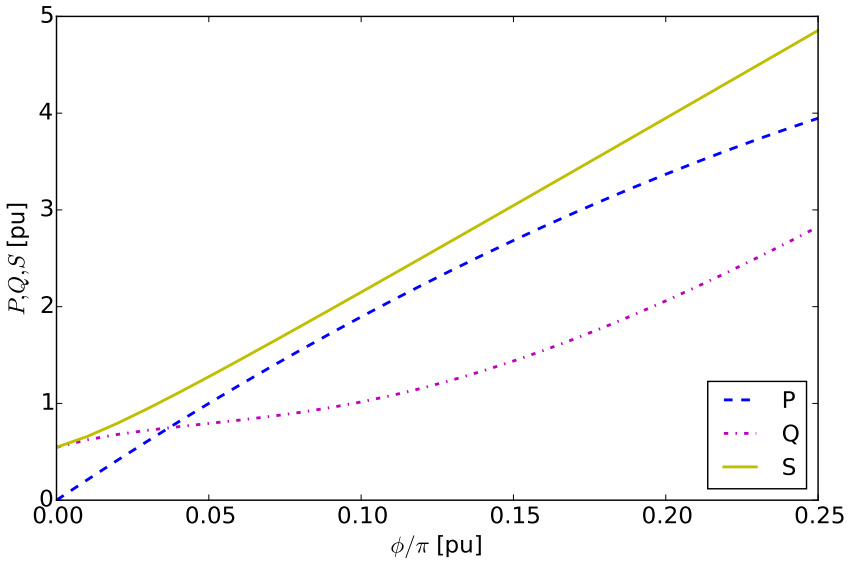


Figure 3.8: Effect of phase shift $\phi$ on real power $P$, reactive power $Q$ and apparent power $S$. $V_{out} = 150$V, $V_{in} = 12$V, $P_{out} = 150$W, $n = 14$.

The result of the preceding discussion is that there are two obvious design elements that lead to optimal realizations of DAB converters. The first feature is that $V_{in} \simeq V_{outn}$, or $nV_{in} \simeq V_{out}$, and the second feature is that $\phi \ll 0.5\pi$, or $\phi \approx 0$. The consequence of these optimal design features is that they may be applied as simplifying approximations in that the analysis of the converter, leading to simple design expressions.

### 3.3.3 Series inductor

There is one series inductor is present in the series path of each of the stages whose value may be determined to be

$$L_s \leq \frac{V_{in} V_{outn}}{32 F_s P_{outn}} \tag{3.14}$$

The power loss in this component can be derived from the series equivalent resistance ESR $R_L$.

$$P_{Ls} = I_{Lrms}^2 R_L \tag{3.15}$$

### 3.3.4 Series coupling capacitor

Capacitors in other dc-dc converters are primarily used for energy storage and accordingly operate with steady dc voltage and small ac ripple voltage. The series capacitor in capacitor-coupled DAB converter operates with large ac currents. The dc voltage across each series capacitor is a function of its position along the string and the output voltage. The capacitance is selected such that the capacitive impedance at switching frequency is negligible. This translates into a design rule,

$$C_s > \frac{50}{R_{outn} F_s}. \tag{3.16}$$

The maximum voltage rating of the capacitors are maintained at $0.5V_{out}$, while the RMS current ratings are identical to $I_{Lrms}$. The power loss in a capacitor depends on the equivalent series resistance of the capacitor. ESR is expressed in terms of the dissipation factor ($\tan\delta$) of the capacitor.

$$X_c = \frac{1}{2\pi F_s C_s} \tag{3.17}$$

$$R_{cs} = X_c \tan\delta \tag{3.18}$$

$$P_{cs} = I_{Lrms}^2 R_{cs} \tag{3.19}$$

### 3.3.5 Output filter capacitor

The filter capacitor voltage and current are illustrated in Fig 3.9. The worst-case voltage ripple in the filter capacitor can be calculated assuming $0.5T_s >> T_\phi$. In this condition

$$C_{out} = \frac{\Delta i_c T_s}{8 \Delta v_{outn}} \tag{3.20}$$

$$\Delta i_c = |I_{L0} - I_{L1}| \tag{3.21}$$

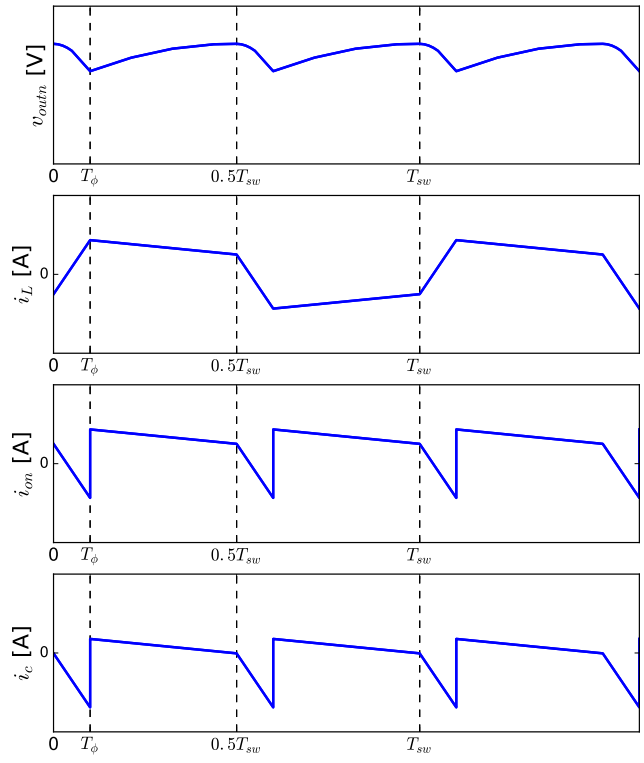


Figure 3.9: (a) Output DC voltage $v_{outn}$;(b) Inductor current $i_{Ln}$; (c) Rectified output stage current $i_{on}$; (d) Filter capacitor current $i_c$.

### 3.3.6 Input switches

The rms current of the switches on the input side can be approximated as

$$I_{swirms} = n\sqrt{\frac{I_{L0}^2 + |I_{L0}||I_{L1}| + I_{L1}^2}{3}\frac{(0.5T_s - T_\phi)}{T_s}} \tag{3.22}$$

where $I_L$ is the inductor current per stage. The average switch current can be similarly defined as

$$I_{swiavg} = n\frac{1}{4T_s}\left[|I_{L0}|(T_s - 2t_D) + |I_{L1}|(T_s - 2T_\phi))\right] \tag{3.23}$$

The diode current on the input side is given as

$$I_{dirms} = n\sqrt{\frac{I_{L0}^2}{3}\frac{t_D}{T_s}} \tag{3.24}$$

$$I_{diavg} = n\frac{I_{L0}}{2}\frac{t_D}{T_s} \tag{3.25}$$

The voltage ratings of the input switches and diodes are maintained at $V_{in}$. Both the input and output switches are operated under ZVS conditions which implies that switching loss is negligible. The only loss in the switches is during conduction. If $R_{dsoni}$ is the drain to source on-state resistance of the switching devices and $V_{fi}$ is the anode to cathode forward voltage drop of the antiparallel diode, the average loss at the input switch for both CCDAB and TCDAB is given by

$$P_{swi} = I_{swirms}^2 R_{dsoni} + I_{diavg} V_{fi} \tag{3.26}$$

### 3.3.7 Output switches

Similar to the input side, the output switch currents will also be derived.

$$I_{sworms} = \sqrt{\frac{I_{L0}^2 + |I_{L0}||I_{L1}| + I_{L1}^2}{3}\frac{(0.5T_s - T_\phi)}{T_s}} \tag{3.27}$$

$$I_{swoavg} = \frac{1}{4T_s}\left[|I_{L0}|T_s + |I_{L1}|(T_s + 2t_D - 2T_\phi))\right] \tag{3.28}$$

The one difference is in the maximum reverse blocking voltage on the output side switches in case of CCDAB will be lower than TCDAB. The diode current on the output side is given as

$$I_{dirms} = \sqrt{\frac{I_{L1}^2}{3}\frac{T_\phi - t_D}{T_s}} \tag{3.29}$$

$$I_{diavg} = \frac{I_{L1}}{2}\frac{T_\phi - t_D}{T_s} \tag{3.30}$$

$R_{dson}$ is the drain to source on-state resistance of the switching devices and $V_{fo}$ is the anode to cathode forward voltage drop of the antiparallel diode on the output side of CCDAB. The average switch loss is

$$P_{swo} = I_{sworms}^2 R_{dson} + I_{doavg} V_{fo} \tag{3.31}$$

## 3.4 Dynamic modeling

The CCDAB is structurally similar to the conventional transformer coupled dual active bridge converter. Hence an examination of the small signal modeling efforts on the dual active bridge converter will be useful to set the stage for modeling the CCDAB. The state space averaging method introduced by [145] for most DC-DC converters is not applicable in case of the dual active bridge converter since the inductor current $i_L$ has zero DC with large AC ripple. The consequence of high AC ripple is that the net volt-seconds across the series inductor does not average to zero for any time interval equal to one switching period. The averaged model is also only valid upto half the switching frequency and will give erroneous results as the bandwidth approaches the switching frquency [146]. For this reason, all linear time-invariant canonical circuit model derived from the state space averaging methods [147–149] do not accurately describe the converter small signal model.

The first small signal model of the dual active bridge converter was proposed by [27]. In this work, the square wave input and output voltage functions were modeled by the fundamental component of the fourier series of the square waves. To derive the small signal model, small signal disturbances were introduced in the phase difference between the input and output

voltage to obtain the following control-to-output transfer function [27].

$$\frac{\Delta V_o(s)}{\Delta \psi(s)} = \frac{2k(1-\psi)R_{out}}{1+sC_{out}R_{out}} \tag{3.32}$$

$$k = \frac{V_i}{8F_s L_s n} \tag{3.33}$$

$$\psi = \frac{\phi}{0.5\pi} \tag{3.34}$$

where $\phi$ is the phase difference between the input and output square waveforms and $n$ is the turns ratio of the transformer secondary/primary. Although this model verifies the expected first order response of the converter, it does not identify all the poles and zeros of the system that can impact the small signal response. The discussion in this thesis is partially derived from and extends the work done by [27]. More recently, accurate discrete time model based on the sampled data modeling method [146, 150, 151] was proposed by [30, 133]. This method has the advantage that the small signal model is not dependent upon small inductor current AC ripple and is valid upto the switching frequency of the converter.

### 3.4.1 Dynamic phasors

Dynamic phasors were developed as a one-phasor approximation of non-linear systems, also known as “harmonic linearization" [152]. Any arbitrary periodic waveform can be represented by a unique dynamic phasor, the only condition being both the magnitude and phase components need to be bandwidth limited time domain function. In [153, 154], the dynamic phasors are selected as the output voltage $v_{out}$ and real and imaginary components of the inductor current $\Re(i_L), \Im(i_L)$. In this study, the selected dynamic phasors are output voltage $v_{out}$ and magnitude and phase angle of inductor current $i_L^a, i_L^\theta$. The phasors represent the magnitude and phase angle of the first order harmonic of the fourier series of the inductor current and the output voltage.

### 3.4.2 Dynamic phasor equivalent circuit

Fig 3.11 shows the simplified equivalent circuit of a DAB converter [27] with one input stage and a single output stage. All the inductive losses (core loss, copper loss, proximity loss etc.)

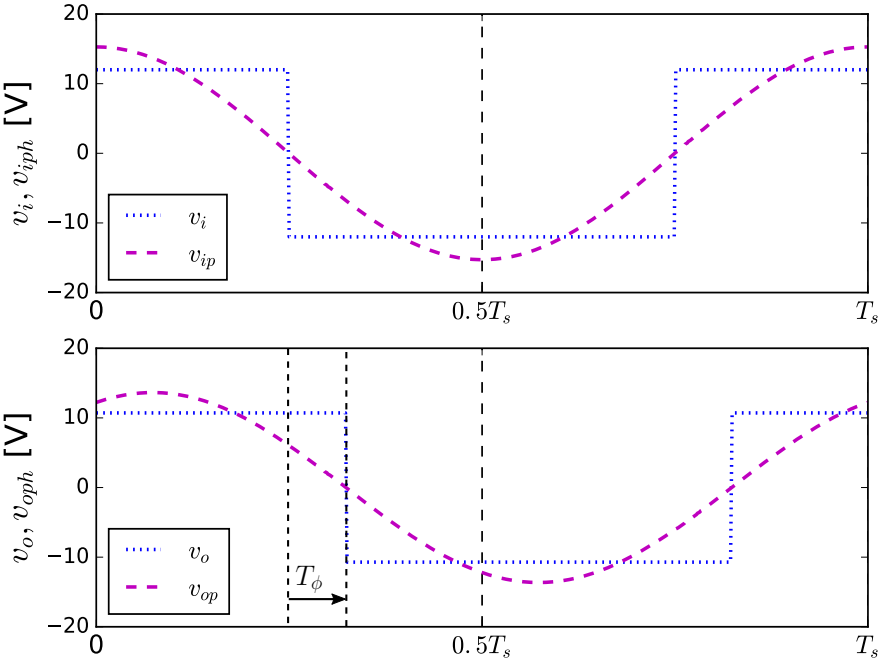


Figure 3.10: $v_i, v_o$: Input and output time domain square waveforms. $v_{iph}, v_{oph}$: Fundamental component of fourier series of input and output waveforms.

are represented by a series resistance $R_L$. The input and output full-bridges are represented by square wave time domain functions $v_i(t)$ and $v_o(t)$.

$$v_i(t) = \begin{cases} +V_{in} & \text{if S1,S4 ON} \\ 0 & \text{if S1,S3 ON; or S2,S4 ON} \\ -V_{in} & \text{if S2,S3 ON} \end{cases} \tag{3.35}$$

$$v_{on}(t) = \begin{cases} +V_{outn} & \text{if S5,S8 ON} \\ 0 & \text{if S5,S7 ON; or S6,S8 ON} \\ -V_{outn} & \text{if S6,S7 ON} \end{cases} \tag{3.36}$$

The periodic time domain functions in Eq. 3.35-3.36 are approximated by the fundamental component of the fourier series.

$$v_i(t) = V_{in} M_i^a \cos(\omega_s t + \theta_i) = \Re\left[V_{in} \overline{M}_i e^{j\omega_s t}\right] \tag{3.37}$$

$$v_{on}(t) = V_{outn} M_{on}^a \cos(\omega_s t + \theta_o) = \Re\left[V_{outn} \overline{M}_{on} e^{j\omega_s t}\right] \tag{3.38}$$

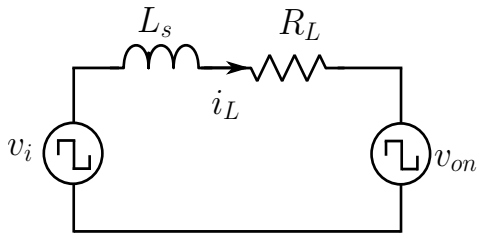


Figure 3.11: Simplified equivalent circuit of DAB converter [27].

The phasors are typically described using an overbar symbol and the magnitude of the phasors usually represent RMS quantities.

$$\overline{V}_i = V_{in}\overline{M}_i \tag{3.39}$$

$$\overline{V}_{on} = V_{outn}\overline{M}_{on} \tag{3.40}$$

Since the input and output voltages are represented by phasors, the inductor current can now

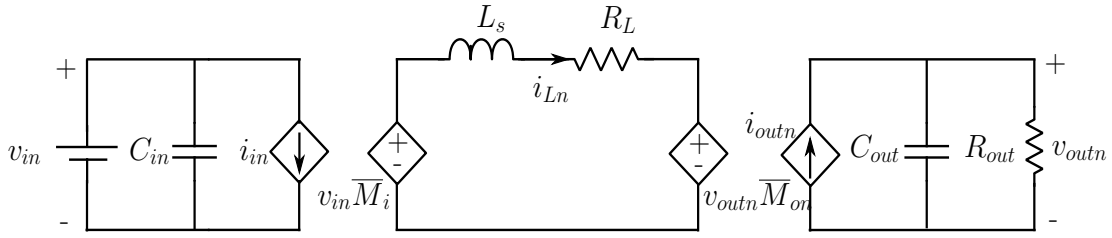


Figure 3.12: Input and output voltages with the fundamental component phasors

be derived as a phasor as shown by (3.41).

$$\overline{I}_{Ln} = \frac{\overline{V}_i - \overline{V}_{on}}{j\omega_s L_s + R_L} \tag{3.41}$$

$$\overline{I}_{Ln} = I^a_{Ln}\angle\theta_{Ln} \tag{3.42}$$

$$i^a_{Ln} = |i_L| \tag{3.43}$$

$$i^\theta_{Ln} = \angle i_L \tag{3.44}$$

$\overline{M}_i$ and $\overline{M}_{on}$ are unit modulation phasors that have the same phase relationship as the time domain $v_i$ and $v_{on}$.

$$\overline{M}_i = \frac{1}{\sqrt{2}}\frac{4}{\pi}e^{j\theta_i} \tag{3.45}$$

$$M_i^a = |\overline{M}_i| \tag{3.46}$$

$$M_i^\theta = \angle\overline{M}_i = \theta_i = 0 \tag{3.47}$$

$$\overline{M}_{on} = \frac{1}{\sqrt{2}}\frac{4}{\pi}e^{j\theta_{on}} \tag{3.48}$$

$$M_{on}^a = |\overline{M}_{on}| \tag{3.49}$$

$$M_{on}^\theta = \angle\overline{M}_{on} = \theta_{on} \tag{3.50}$$

The input and output side DC currents are now derived from the scalar product of the inductor current phasor and input or output modulation phasor.

$$i_{in} = \overline{M}_i \bullet \overline{i}_{Ln} \tag{3.51}$$

$$i_{outn} = \overline{M}_o \bullet \overline{i}_{Ln} \tag{3.52}$$

The transient dynamic equations are derived as

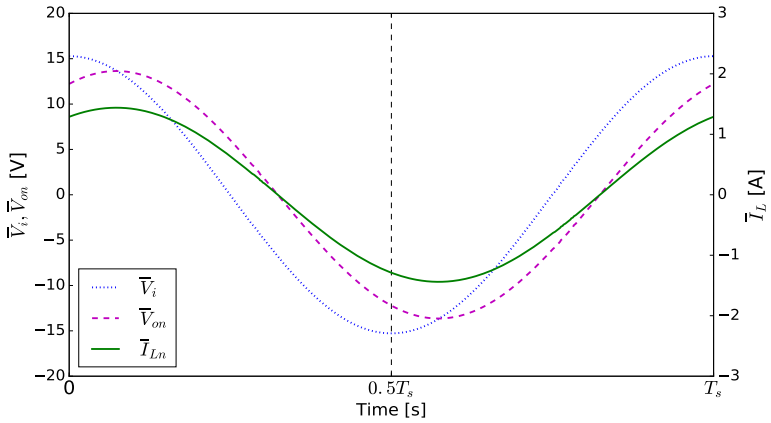


Figure 3.13: $\overline{V}_i$:Input voltage phasor; $\overline{V}_{on}$:Output voltage phasor of stage $n$; $\overline{I}_{Ln}$:Inductor current phasor of stage $n$.

$$L_s \frac{\bar{i}_{Ln}(t)}{dt} = v_{in}\overline{M}_i - v_{outn}\overline{M}_{on} - R_L\bar{i}_{Ln} \tag{3.53}$$

$$C_{out}\frac{dv_{out}}{dt} = M^a_{on} i^a_{Ln}\cos(\theta_{on}-\theta_{Ln}) - \frac{v_{outn}}{R_{outn}} \tag{3.54}$$

This can be expanded as

$$\frac{di^a_{Ln}}{dt} = \frac{1}{L_s}\left[V_{in}M^a_i\cos(\theta_i-\theta_{Ln}) - V_{out}M^a_{on}\cos(\theta_{on}-\theta_{Ln}) - i^a_{Ln}R_L\right] \tag{3.55}$$

$$\frac{dv_{outn}}{dt} = \frac{1}{C_{out}}\left[M^a_{on}i^a_{Ln}\cos(\theta_{on}-\theta_{Ln}) - \frac{v_{outn}}{R_{outn}}\right] \tag{3.56}$$

$$\frac{d\theta_{Ln}}{dt} = \frac{V_{in}M^a_i\sin(\theta_i-\theta_{Ln}) - V_{outn}M^a_{on}\sin(\theta_{on}-\theta_{Ln})}{i^a_{Ln}L_s} - \omega_s \tag{3.57}$$

To obtain the steady state solutions from the state space model, set the left hand side quantities to be zero.

$$V_{in}M^a_i\cos(\theta_i-\theta_{Ln}) = V_{out}M^a_{on}cos(\theta_{on}-\theta_{Ln}) \tag{3.58}$$

$$\frac{V_{outn}}{R_{outn}} = M^a_o I^a_{Ln}\cos(\theta_{on}-\theta_{Ln}) \tag{3.59}$$

$$I^a_{Ln}L_s\omega_s = V_{in}M^a_i\sin(\theta_i-\theta_{Ln}) - V_{outn}M^a_{on}\sin(\theta_{on}-\theta_{Ln}) \tag{3.60}$$

These three relationships provide real power balance at the ac terminals, power balance at the output dc terminals, and the reactive power balance at the ac terminals respectively. The phase angle of each of the output bridges are the control variable that affects the power throughput through that bridge.

### 3.4.3 Phasor domain output voltage regulation

A plot of the load regulation of the capacitor coupled DAB converter in the phasor domain is shown in Fig 3.14 for different output phase angles. This verifies that the output characteristics derived by the phasor model is similar to the output characteristics derived from the time domain model of [27]. The y-axis of this plot is per-unitized to the input voltage $V_{in}$ and the x-axis is per-unitized to the RMS current for 1 PU power.

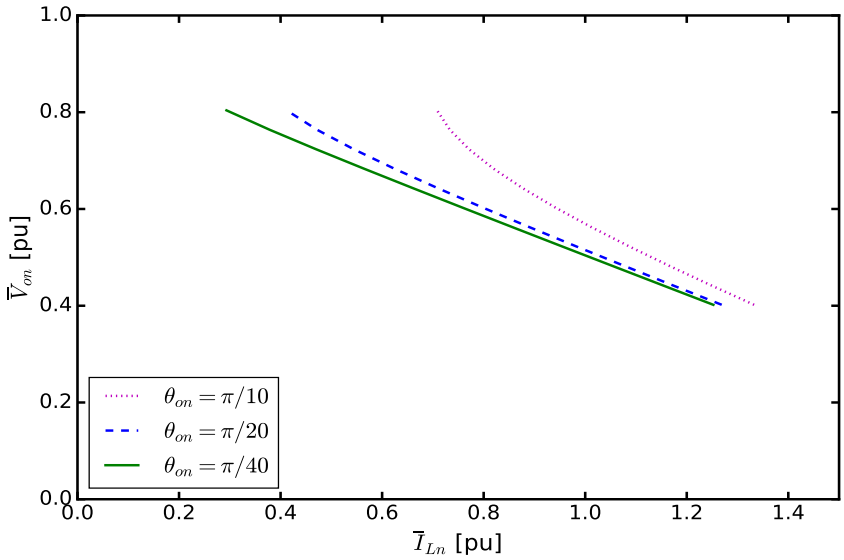


Figure 3.14: A plot of load regulation of the converter using the phasor model for different output phase angles $\theta_{on}$.

### 3.4.4 Phasor domain real and reactive power

The power flow equation for the capacitor coupled DAB converter has been described by Eq.3.11. This can be compared with the power flow equations derived from the phasor domain equivalent circuit. In the phasor domain the input and output power are defined as

$$\overline{P}_i + j\overline{Q}_i = \Re\left[\overline{V}_i \overline{I}^*_{Ln}\right] + j\Im\left[\overline{V}_i \overline{I}^*_{Ln}\right] \tag{3.61}$$

$$\overline{P}_{on} + j\overline{Q}_{on} = \Re\left[\overline{V}_{on} \overline{I}^*_{Ln}\right] + j\Im\left[\overline{V}_{on} \overline{I}^*_{Ln}\right] \tag{3.62}$$

### 3.4.5 Small signal model

The circuit shown in Fig3.12 can be now linearized at a steady state operating point to derive the averaged linearized phasor dynamic model. For the dynamic phasor equivalent circuit shown in Fig 3.12, the state variables are the inductor current and output capacitor voltage. Since the state variables are expressed as phasors, the phasor model state variables will be inductor current magnitude ($i^a_{Ln}$), inductor current phase ($i^\theta_{Ln} = \theta_{Ln}$) and output capacitor

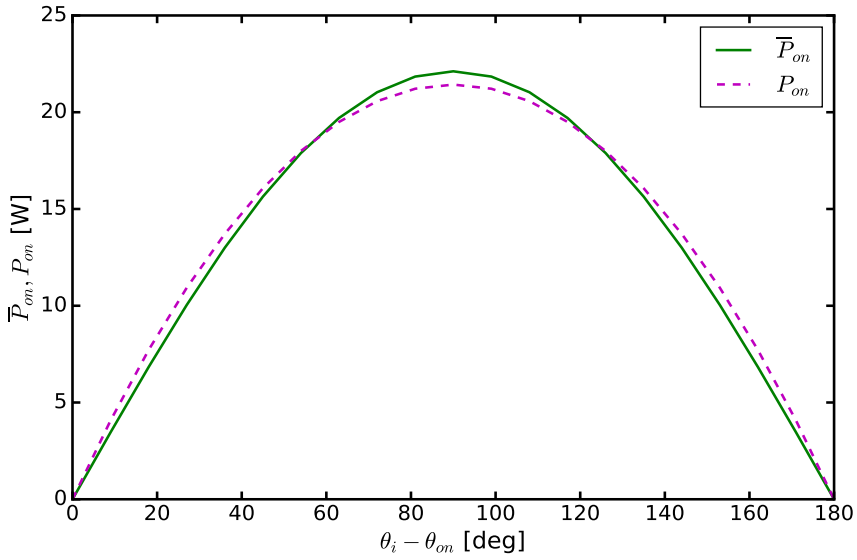


Figure 3.15: Comparing output power of stage $n$ derived from time domain model $P_{on}$ and phasor domain model $\overline{P}_{on}$

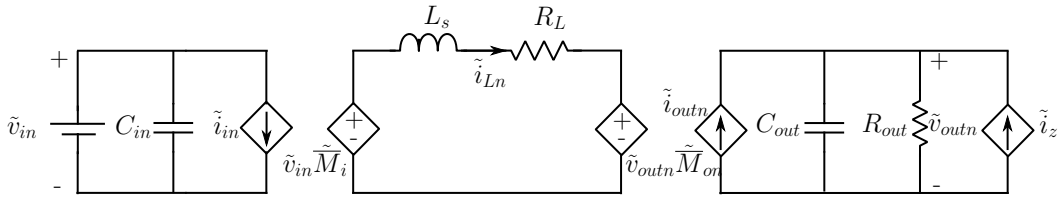


Figure 3.16: Linearized averaged equivalent circuit

voltage $v_{outn}$. The phasor dynamic state space equations in the polar coordinate system for the $n^{th}$ stage are

$$\frac{di^a_{Ln}}{dt} = f_1(V_{in}, \overline{M}_i, \overline{M}_{on}, \bar{i}_{Ln}, v_{outn}, i_z) \tag{3.63}$$

$$\frac{dv_{outn}}{dt} = f_2(V_{in}, \overline{M}_i, \overline{M}_{on}, \bar{i}_{Ln}, v_{outn}, i_z) \tag{3.64}$$

$$\frac{d\theta_{Ln}}{dt} = f_3(V_{in}, \overline{M}_i, \overline{M}_{on}, \bar{i}_{Ln}, v_{outn}, i_z) \tag{3.65}$$

The most general form of the state variables, input variables and output variables for the $n^{th}$ stage are

$$\tilde{x}_n = \begin{bmatrix} \tilde{i}^a_{Ln} & \tilde{v}_{outn} & \tilde{i}^\theta_{Ln} \end{bmatrix}^T \tag{3.66}$$

$$u_{pn} = \begin{bmatrix} \tilde{v}_{in} & \tilde{M}_i^a & \tilde{\theta}_i & \tilde{M}_{on}^a & \tilde{\theta}_{on} & \tilde{i}_z \end{bmatrix}^T \tag{3.67}$$

$$\tilde{y}_n = \tilde{v}_{outn} \tag{3.68}$$

$$\begin{bmatrix} \frac{d\tilde{i}_{Ln}^a}{dt} \\ \frac{d\tilde{v}_{outn}}{dt} \\ \frac{d\tilde{i}_{Ln}^\theta}{dt} \end{bmatrix} = \begin{bmatrix} \frac{\partial f_1}{\partial i_{Ln}^a} & \frac{\partial f_1}{\partial v_{outn}} & \frac{\partial f_1}{\partial i_{Ln}^\theta} \\ \frac{\partial f_2}{\partial i_{Ln}^a} & \frac{\partial f_2}{\partial v_{outn}} & \frac{\partial f_2}{\partial i_{Ln}^\theta} \\ \frac{\partial f_3}{\partial i_{Ln}^a} & \frac{\partial f_3}{\partial v_{outn}} & \frac{\partial f_3}{\partial i_{Ln}^\theta} \end{bmatrix} \begin{bmatrix} \tilde{i}_{Ln}^a \\ \tilde{v}_{outn} \\ \tilde{i}_{Ln}^\theta \end{bmatrix} + \begin{bmatrix} \frac{\partial f_1}{\partial u_{1n}} & \frac{\partial f_1}{\partial u_{2n}} & \frac{\partial f_1}{\partial u_{3n}} & \frac{\partial f_1}{\partial u_{4n}} & \frac{\partial f_1}{\partial u_{5n}} & \frac{\partial f_1}{\partial u_{6n}} \\ \frac{\partial f_2}{\partial u_{1n}} & \frac{\partial f_2}{\partial u_{2n}} & \frac{\partial f_2}{\partial u_{3n}} & \frac{\partial f_2}{\partial u_{4n}} & \frac{\partial f_2}{\partial u_{5n}} & \frac{\partial f_2}{\partial u_{6n}} \\ \frac{\partial f_3}{\partial u_{1n}} & \frac{\partial f_3}{\partial u_{2n}} & \frac{\partial f_3}{\partial u_{3n}} & \frac{\partial f_3}{\partial u_{4n}} & \frac{\partial f_3}{\partial u_{5n}} & \frac{\partial f_3}{\partial u_{6n}} \end{bmatrix} \begin{bmatrix} \tilde{v}_{in} \\ \tilde{M}_i^a \\ \tilde{\theta}_i \\ \tilde{M}_{on}^a \\ \tilde{\theta}_{on} \\ \tilde{i}_z \end{bmatrix} \tag{3.69}$$

The state space equations are in the canonical form,

$$\dot{\tilde{x}}_n = A_n \tilde{x}_n + B_0 \tilde{v}_{in} + B_1 \tilde{M}_i^a + B_2 \tilde{\theta}_i + B_{3n} \tilde{M}_{on}^a + B_{4n} \tilde{\theta}_{on} + B_{5n} \tilde{i}_z \tag{3.70}$$

$$\tilde{y}_n = C_n \tilde{x}_n \tag{3.71}$$

In the most general form, the $A_n$ matrix can be expanded as

$$A_n = \begin{bmatrix} -\frac{R_L}{L_s} & -\frac{M_{on}^a \cos(\theta_{Ln} - \theta_{on})}{L_s} & \frac{M_i^a V_{in} \sin(\theta_i - \theta_{Ln}) + M_{on}^a v_{outn} \sin(\theta_{Ln} - \theta_{on})}{L_s} \\ \frac{M_{on}^a \cos(\theta_{Ln} - \theta_{on})}{C_{out}} & -\frac{1}{C_{out} R_{out}} & -\frac{i_{Ln}^a M_{on}^a \sin(\theta_{Ln} - \theta_{on})}{C_{out}} \\ -\frac{M_i^a V_{in} \sin(\theta_i - \theta_{Ln}) + M_{on}^a v_{outn} \sin(\theta_{Ln} - \theta_{on})}{i_{Ln}^{a2} L_s} & \frac{M_o^a \sin(\theta_{Ln} - \theta_{on})}{i_{Ln}^a L_s} & \frac{-M_i^a V_{in} \cos(\theta_i - \theta_{Ln}) + M_{on}^a v_{outn} \cos(\theta_{Ln} - \theta_{on})}{i_{Ln}^a L_s} \end{bmatrix} \tag{3.72}$$

The above state space model can be further simplified by making the following assumptions.

- The input voltage phase angle is the reference phase $\theta_i = 0$.
- The input voltage phasor magnitude is fixed at $M_i^a$.
- The output voltage phasor magnitude is also fixed at $M_{on}^a$.

Now the state space model becomes

$$\dot{\tilde{x}}_n = A_n \tilde{x}_n + B_0 V_{in} + B_{4n} \theta_{on} + B_{5n} \tilde{i}_z \tag{3.73}$$

$$\tilde{y}_n = C_n \tilde{x}_n \tag{3.74}$$

where the $B_0$,$B_4$ are expanded as

$$B_0 = \begin{bmatrix} \frac{M_i^a \cos(\theta_{Ln})}{Ls} \\ 0 \\ -\frac{M_i^a \sin(\theta_{Ln})}{i_{Ln}^a L_s} \end{bmatrix} \tag{3.75}$$

$$B_{4n} = \begin{bmatrix} -\frac{M_{on}^a v_{outn} \sin(\theta_{Ln} - \theta_{on})}{L_s} \\ \frac{i_{Ln} M_{on}^a \sin(\theta_{Ln} - \theta_{on})}{C_{out}} \\ -\frac{M_{on}^a v_{outn} \cos(\theta_{Ln} - \theta_{on})}{i_{Ln}^a L_s} \end{bmatrix} \tag{3.76}$$

$$B_{5n} = \begin{bmatrix} 0 \\ \frac{1}{C_{out}} \\ 0 \end{bmatrix} \tag{3.77}$$

### 3.4.6 Extending state space model to n-stages

One of the advantages of the CCDAB over the traditional transformer-coupled DAB converter is that there is no mutual coupling between the output stages. Each output stage can be independently controlled without affecting the output of any other stage. Additionally, the coupling capacitors are DC blocking, low impedance for AC and do not affect the small signal response of the converter. This modular structure also means that there can be multiple independent floating outputs each regulated at different voltages as shown in Fig 3.17.

So for an $n$ stage circuit,

$$\begin{bmatrix} \dot{\tilde{x}}_1 \\ \vdots \\ \dot{\tilde{x}}_n \end{bmatrix} = \begin{bmatrix} [A_1] & 0 & \dots & 0 & 0 \\ 0 & [A_2] & \dots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \dots & 0 & [A_n] \end{bmatrix} \begin{bmatrix} \tilde{x}_1 \\ \vdots \\ \tilde{x}_n \end{bmatrix} + \begin{bmatrix} B_0 \\ \vdots \\ B_0 \end{bmatrix} \tilde{v}_{in} + \begin{bmatrix} B_{41} \\ 0 \\ \vdots \\ 0 \end{bmatrix} \tilde{\theta}_{o1} + \dots \begin{bmatrix} 0 \\ 0 \\ \vdots \\ B_{4n} \end{bmatrix} \tilde{\theta}_{on} \tag{3.78}$$

It may be observed that the A-matrix for the full converter is a block diagonal matrix, where all the off-diagonal entries are null matrices. This also proves that the output stages are decoupled.

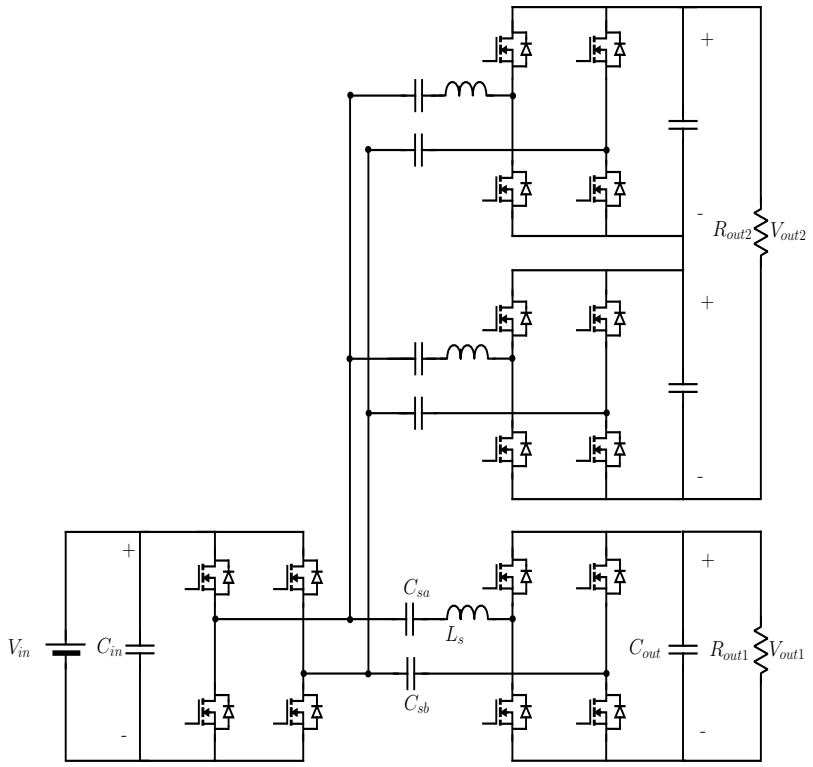


Figure 3.17: Schematic of single phase CCDAB showing two independent floating outputs

## 3.5 Converter transfer functions

### 3.5.1 Control voltage gain

Using the simplified state space model shown in Eq 3.73-3.74, the open-loop control-to-output transfer function can be determined as ($\tilde{v}_{in}, \tilde{i}_z = 0$).

$$G_{v\theta}(s) = \frac{\tilde{v}_{out}(s)}{\tilde{\theta}_{on}(s)} = \frac{K_1\left[\frac{R_L^2}{L_s^2} + \omega_s^2 - \frac{M_{on}^a v_{out}\omega_s}{i_{Ln}^a L_s \sin(\theta_{Ln}-\theta_{on})} + 2\frac{R_L}{L_s}s + s^2\right]}{K_2\left[\frac{1}{C_{out}R_{out}} + s\right]\left[\frac{{M_{on}^a}^2 R_{out}R_L}{L_s^2} + \frac{R_L^2}{L_s^2} + \omega_s^2 + 2\frac{R_L}{L_s}s + s^2\right]} \tag{3.79}$$

This can be expressed in the characteristic equation form as

$$G_{v\theta}(s) = \frac{K_3\left[1 + \frac{1}{Q_{z1}}\frac{s}{\omega_{z1}} + \frac{s^2}{\omega_{z1}^2}\right]}{K_4\left[1 + \frac{s}{\omega_{p1}}\right]\left[1 + \frac{1}{Q_{p2}}\frac{s}{\omega_{p2}} + \frac{s^2}{\omega_{p2}^2}\right]} \tag{3.80}$$

where $K_1, K_2, K_3, K_4$ are constants and

$$Q_{z1} = \frac{\sqrt{\frac{R_L^2}{L_s^2} + \omega_s^2 - \frac{M_{on}^a v_{out} \omega_s}{i_{Ln}^a L_s \sin(\theta_{Ln} - \theta_{on})}}}{2\frac{R_L}{L_s}} \tag{3.81}$$

$$\omega_{z1} = \sqrt{\frac{R_L^2}{L_s^2} + \omega_s^2 - \frac{M_{on}^a v_{out} \omega_s}{i_{Ln}^a L_s \sin(\theta_{Ln} - \theta_{on})}} \tag{3.82}$$

$$\omega_{p1} = \frac{1}{C_{out} R_{out}} \tag{3.83}$$

$$Q_{p2} = \frac{\sqrt{\frac{{M_{on}^a}^2 R_{out} R_L}{L_s^2} + \frac{R_L^2}{L_s^2} + \omega_s^2}}{2\frac{R_L}{L_s}} \tag{3.84}$$

$$\omega_{p2} = \sqrt{\frac{{M_{on}^a}^2 R_{out} R_L}{L_s^2} + \frac{R_L^2}{L_s^2} + \omega_s^2} \tag{3.85}$$

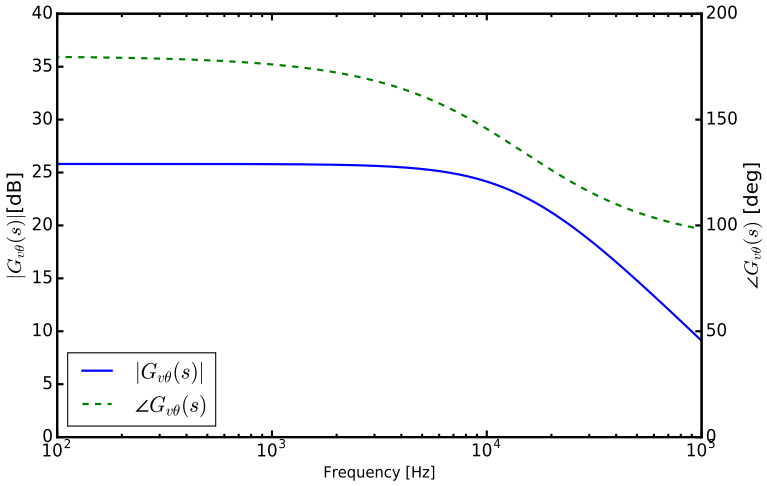


Figure 3.18: Control voltage gain transfer function

### 3.5.2 Audio susceptibility

The input-to-output voltage transfer function is defined as ($\tilde{i}_z, \tilde{\theta}_{on} = 0$).

$$G_{vv}(s) = \frac{\tilde{v}_{out}(s)}{\tilde{v}_{in}(s)} = \frac{K_5\left[\frac{R_L}{L_s} - \omega_s \tan\theta_{on} + s\right]}{K_6\left[\frac{1}{C_{out}R_{out}} + s\right]\left[\frac{M_{on}^{a\ 2}R_{out}R_L}{L_s^2} + \frac{R_L^2}{L_s^2} + \omega_s^2 + 2\frac{R_L}{L_s}s + s^2\right]} \tag{3.86}$$

This can be expressed in the characteristic equation form as

$$G_{vv}(s) = \frac{K_7\left[1 + \frac{s}{\omega_{z2}}\right]}{K_8\left[1 + \frac{s}{\omega_{p1}}\right]\left[1 + \frac{1}{Q_{p2}}\frac{s}{\omega_{p2}} + \frac{s^2}{\omega_{p2}^2}\right]} \tag{3.87}$$

where $K_5, K_6, K_7, K_8$ are constants and

$$\omega_{z2} = \frac{R_L}{L_s} - \omega_s \tan\theta_{on} \tag{3.88}$$

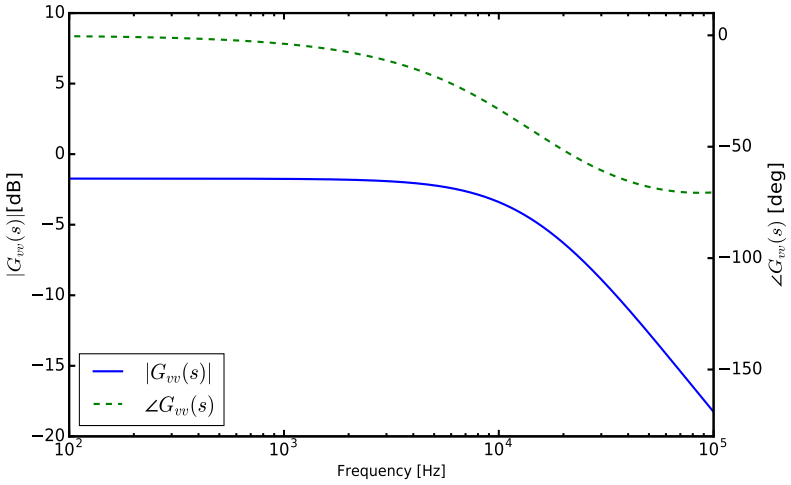


Figure 3.19: Audio susceptibility transfer function

### 3.5.3 Output impedance

The output current to output voltage transfer function is defined as ($\tilde{v}_{in}, \tilde{\theta}_{on} = 0$)

$$G_{vi}(s) = \frac{\tilde{v}_{out}(s)}{\tilde{v}_{in}(s)} = \frac{K_9 \left[ \frac{R_L^2}{L_s^2} + \omega_s^2 + 2\frac{R_L}{L_s}s + s^2 \right]}{K_{10} \left[ \frac{1}{C_{out}R_{out}} + s \right] \left[ \frac{{M_{on}^a}^2 R_{out} R_L}{L_s^2} + \frac{R_L^2}{L_s^2} + \omega_s^2 + 2\frac{R_L}{L_s}s + s^2 \right]} \tag{3.89}$$

This can be expressed in the characteristic equation form as

$$G_{vi}(s) = \frac{K_{11} \left[ 1 + \frac{1}{Q_{z3}} \frac{s}{\omega_{z3}} + \frac{s^2}{\omega_{z3}^2} \right]}{K_{12} \left[ 1 + \frac{s}{\omega_{p1}} \right] \left[ 1 + \frac{1}{Q_{p2}} \frac{s}{\omega_{p2}} + \frac{s^2}{\omega_{p2}^2} \right]} \tag{3.90}$$

where $K_9, K_{10}, K_{11}, K_{12}$ are constants and

$$Q_{z3} = \frac{\sqrt{\frac{R_L^2}{L_s^2} + \omega_s^2}}{2\frac{R_L}{L_s}} \tag{3.91}$$

$$\omega_{z3} = \sqrt{\frac{R_L^2}{L_s^2} + \omega_s^2} \tag{3.92}$$

$$\tag{3.93}$$

## 3.6 Regulator design

As discussed before the small signal linear model is applicable only upto a frequency of about $0.1\omega_s$. From Eq. 3.82-3.85,

$$\omega_s^2 \gg \frac{R_L^2}{L_s^2} - \frac{M_{on}^a v_{out} \omega_s}{i_{Ln}^a L_s \sin(\theta_{Ln} - \theta_{on})} \tag{3.94}$$

$$\omega_s^2 \gg \frac{{M_{on}^a}^2 R_{out} R_L}{L_s^2} + \frac{R_L^2}{L_s^2} \tag{3.95}$$

which means $\omega_{z1} \approx \omega_{p2}$. The second order zero and the second order pole essentially cancel each other do not affect the system response over the control bandwidth. Hence the system behaves as a first order pole at low frequencies, which is a function of the output capacitance

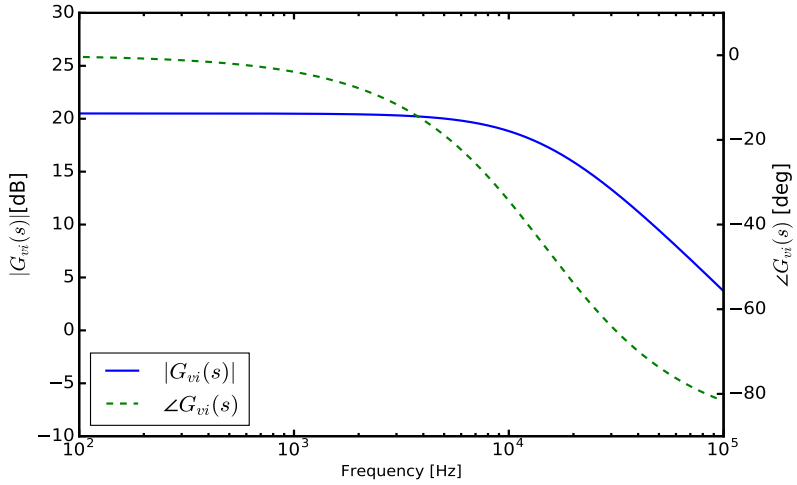


Figure 3.20: Output impedance transfer function

and load resistance of each stage. This also verifies the first order response derived by Eq. 3.32. The control to output transfer function will therefore be

$$G_{v\theta}(s) \simeq \frac{K_3}{K_4\left[1+\frac{s}{\omega_{p1}}\right]} \tag{3.96}$$

### 3.6.1 PI regulator

The regulator is designed to compensate this first order pole using a simple PI controller. The controller transfer function is defined as $G_c(s)$. The controller is designed for a desired closed loop bandwidth ($GCF_d$) of 1 kHz. The actual gain-crossover-frequency of the system is given by $GCF_a$. The loop gain is defined as $G_{lg}(s)$.

$$G_c(s) = K_p\left(1+\frac{\omega_c}{s}\right) \tag{3.97}$$

$$K_p = \frac{GCF_d}{GCF_a} \tag{3.98}$$

$$G_{lg}(s) = G_c(s)G_{v\theta}(s) \tag{3.99}$$

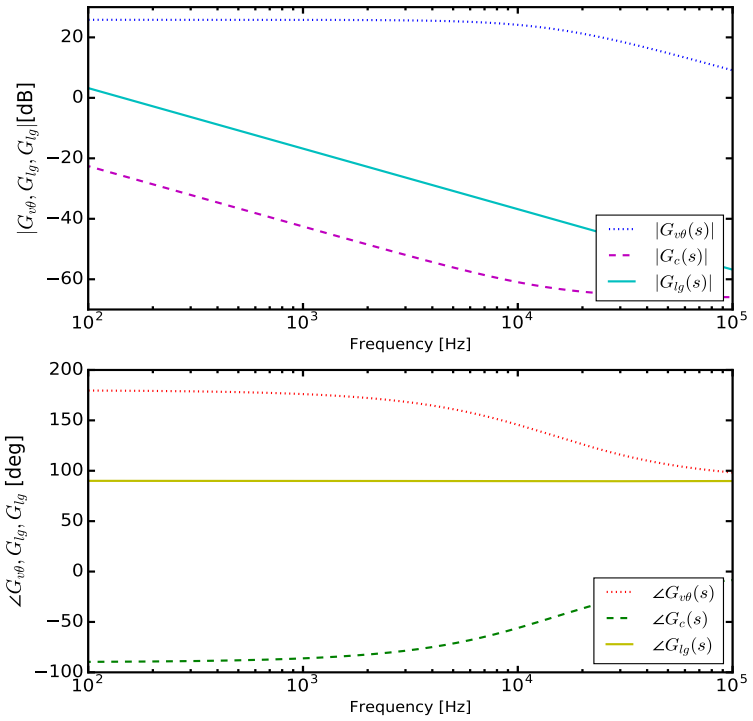


Figure 3.21: Effect of PI regulator on control voltage gain

### 3.6.2 PI controller response in time domain

A dual output prototype of the single phase CCDAB was simulated in PLECS™to verify steady-state operation and closed-loop dynamics. The input voltage is set at 12V and one of the outputs with a single rectifier stage is regulated at 10V and the second output is regulated at 15V. Fig 3.23 shows the startup and response to step change in load for two outputs. At $t = 3$ms, a step change in load in applied to $V_{out1}$ and similarly, a step change in load is applied to $V_{out2}$ at $t = 7$ms. As verified by the simulation, the disturbance in any output has no effect on the other outputs.

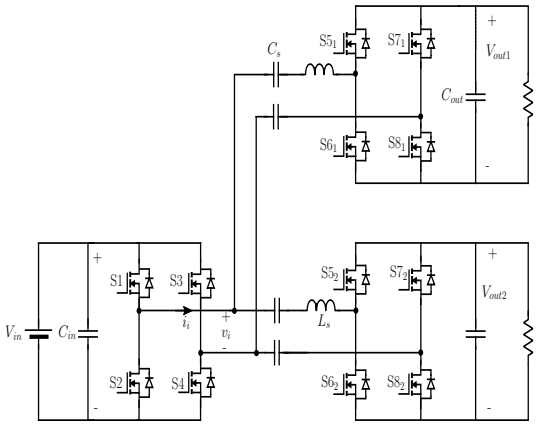


Figure 3.22: Power stage schematic of single phase parallel coupled CCDAB showing two independent floating outputs

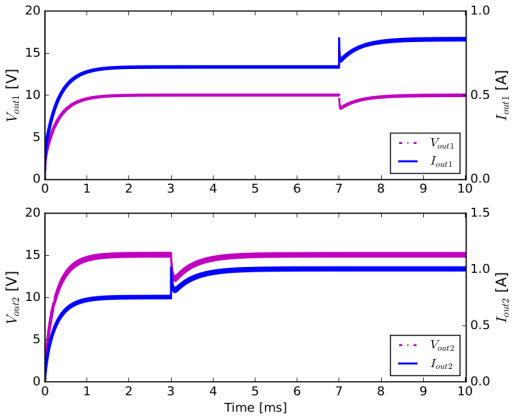


Figure 3.23: Simulation of multiple DC outputs, showing $V_{out1} = 10$V, $V_{out2} = 15$V, $R_{out1} = 15\Omega, R_{out2} = 20\Omega$

## 3.7 Summary

This chapter has introduced the capacitor coupled bidirectional dual active bridge converter. The coupling from the input stage full-bridge to the output stage full-bridge rectifier is provided by coupling capacitors. The steady state operation of the converter topology is analyzed for phase shift modulation between the input and output stages and the design considerations discussed in detail. The concept of dynamic phasors is used to develop a dynamic model of the converter and this concept is further extended to derive the state space model for an n-stage converter. The state space matrix is used to derive the control-to-output transfer function. A continuous time PI regulator is designed for the desired bandwidth with excellent dynamic properties.

CHAPTER 4

# Critical Evaluation of Converter Characteristics

The proposed capacitor coupled DC-DC converter topologies have several unique characteristics that are not present in the traditional DC-DC boost topologies. We can examine these characteristics to identify the properties and trade-offs associated with this topology. Such an examination will also help to quantify the effect of the various trade-offs that emerge as a consequence of this topology. There are topological variations within capacitor coupled topologies that have a significant effect on the component selection without affecting the power capabilities. These variations are also discussed in some detail in this chapter. This chapter also introduces a comparative evaluation of the CCSAB and CCDAB topology with existing transformer coupled single and dual active bridge topologies to evaluate the design benefits of this new topology.

## 4.1 Coupling capacitors

A capacitor is a device that stores energy in the form of an electric field. This electric field is applied between two conducting electrodes (cathode (-) and anode (+)) that are separated by an insulating material called the dielectric. An effect of this applied electric field is that positive

and negative charges appear on either side of the dielectric on the surface of the electrodes. Starting with this basic struture 250 years ago [155, 156], capacitor technology has rapidly advanced hand in hand with advances in material science. The capacitance $C_{AK}$ is a physical property defined as

$$C_{AK} = \epsilon_0 \epsilon_r \frac{S}{d} \tag{4.1}$$

where $\epsilon_0$ is the absolute permittivity of free space ($8.854 \times 10^{-12}$ F/m), $\epsilon_r$ is the relative permittivity of the dielectric insulator, $S$ is the surface are of the electrodes ($m^2$) and $d$ is the thickness of the dielectric (or distance between electrodes in $m$). From Eq 4.1 the size and rating of a capacitor are affected by surface area of the conducting electrodes, the separation between the electrodes and the dielectric constant of the insulating material between the electrodes. If $V_{AK}$ is the voltage applied across the capacitor electrodes, then the stored energy in the electric field $E_c$ is given as

$$E_c = \frac{1}{2} C_{AK} V_{AK}^2 \tag{4.2}$$

### 4.1.1 Types of capacitors

The commonly used capacitor types for general purpose power applications are classified on the basis of the dielectric material as shown in Fig 4.1. Polarized capacitors can hold charge only when a positive voltage is applied from the anode to cathode. The dielectric material in polarized capacitors consists of a thin layer of oxide of the anode metal. This dielectric layer is maintained by the applied voltage polarity. If the polarity is reversed, this dielectric layer on the anode is destroyed via electrochemical reduction and thus the capacitor will short circuit [156]. In non-polarized capacitors the dielectric material is independent of the anode or cathode and hence these capacitors can hold charge when polarized in either direction.

### 4.1.2 Dielectric properties

The earliest recorded capacitor was the Leyden jar which was a ceramic capacitor invented by the german Ewald Georg von Kleist in 1745 [155]. Capacitors became very important for power

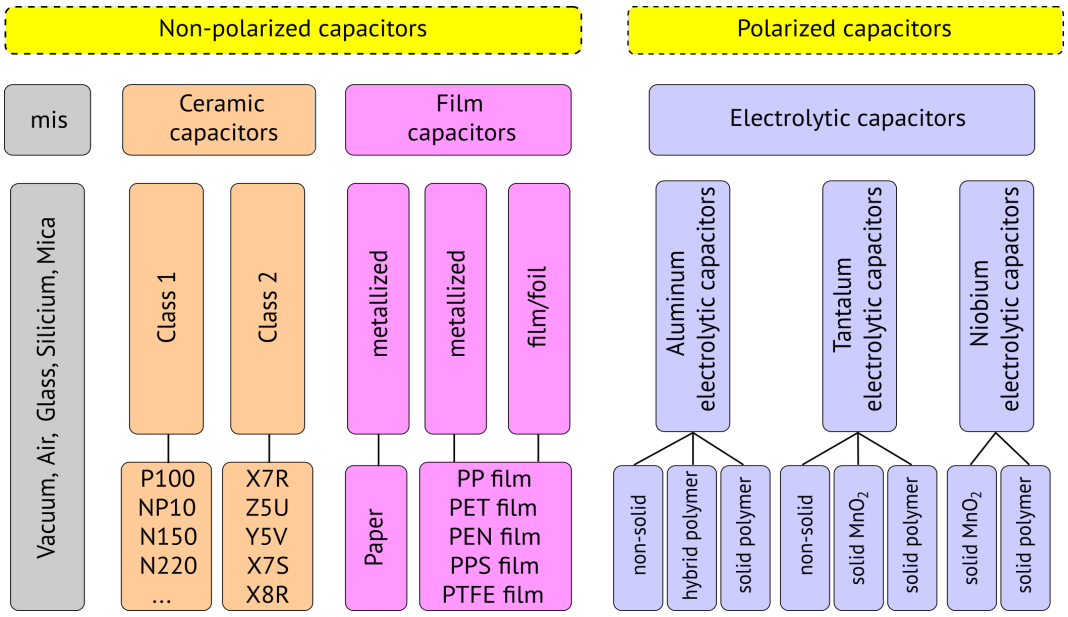


Figure 4.1: Classification of commonly-used capacitor types [157]

supply filtering with the invention of radio receivers in the 1920s. The dielectric material used in these early capacitors was wax-impregnated paper or mica. Mica capacitors were invented by William Dubilier in 1909 who later formed Cornell-Dubilier Electric company after merging with Cornell Radio in 1933. Around the 1930s electrolytic capacitors with significantly higher capacitance began to replace both wax impregnated capacitors and large filter chokes [156]. These were mainly “dry" type electrolytic capacitor made radio receivers affordable and popular. In the 1950s, ceramic capacitor technology got a major boost by to the discovery of barium titante which had a dielectric constant x1000 any other material at that time. New manufacturing techniques like multilayer ceramic capacitor (MLCC) fabrication expanded the capacitance and range of possible applications of ceramic capacitors. Metalized self-clearing paper capacitors reached maturity during World war II, but they perfected after by Bell labs around 1954 and found wide use in telecom power supplies [158]. Plastic dielectrics like polyethylene terephthalate, olyethylene, polystyrene, polytetrafluoroethylene, PET, polycarbonate and polypropylene were invented by multiple groups including Dupont Inc in the 1950s-1980s.

Table 4.1: Dielectric constant, dielectric strength and voltage rating of commonly used capacitor types [159–162]

| Capacitor type | Dielectric | $\epsilon_r$ | Strength [V/$\mu$m] | Voltage rating |
|---|---|---|---|---|
| Glass, Mica | Glass | 4.8 - 9.9 | 10 - 40 | $10^2$ - $10^3$ |
| | Mica | 5.4 - 8.7 | 60 - 180 | $10^2$ - $10^4$ |
| Ceramic | Class 1 | 12-40 | 20 - 40 | 10 - $10^4$ |
| | Class 2 | 200-14,000 | | |
| Film | Plastic | 2.1 - 6 | 60 - 450 | 10 - $10^4$ |
| | Paper | 2 - 6 | 30 - 60 | $10^2$ - $10^5$ |
| Electrolytic | Aluminium oxide $Al_2O_3$ | 8 - 10 | 700 - 1000 | 10 - 500 |
| | Tantalum oxide $Ta_2O_5$ | 10 - 27 | 625 | 10 - 500 |
| | Niobium oxide $Nb_2O_5$ | 41 | 400 | 10 - 20 |

### 4.1.3 Voltage rating

An important physical factor that affects the capacitance but does not appear in Eq.4.1 is dielectric strength [159]. Dielectric strength (V/$\mu$m) is the maximum electric field that the insulator can withstand without experiencing failure of its insulating properties [163]. Dielectric strength directly affects the thickness of the dielectric and thereby the voltage rating and size of the capacitor.

### 4.1.4 Current rating

The current rating of capacitors is essentially limited by the loss characteristics of the capacitor. The losses in a capacitor can be divided into two categories: AC loss and DC loss.

DC loss is also known as leakage current loss occurs because a small DC current can “leak" through the dielectric and cause the capacitor to lose its charge over time. This loss depends on the insulation resistance of the dielectric. Fig 4.3 shows the DC loss characteristics of various dielectric materials. Although very important, DC loss or the static loss is not an important factor for capacitor coupled DC DC converter applications.

AC loss is also known as equivalent series resistance (ESR) which is caused by resistance of dielectric plus resistance of electrodes. This resistance is expressed in terms of material-specific frequency-dependent factor called the dissipation factor (DF) or loss angle ($\tan\delta$).

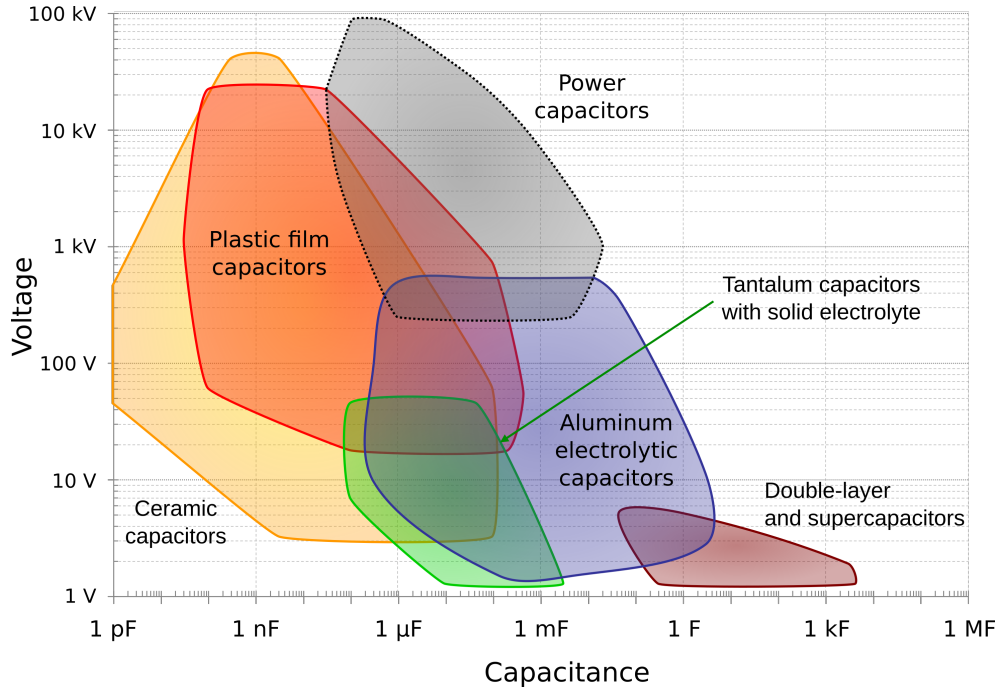


Figure 4.2: Capacitance vs voltage range [164]

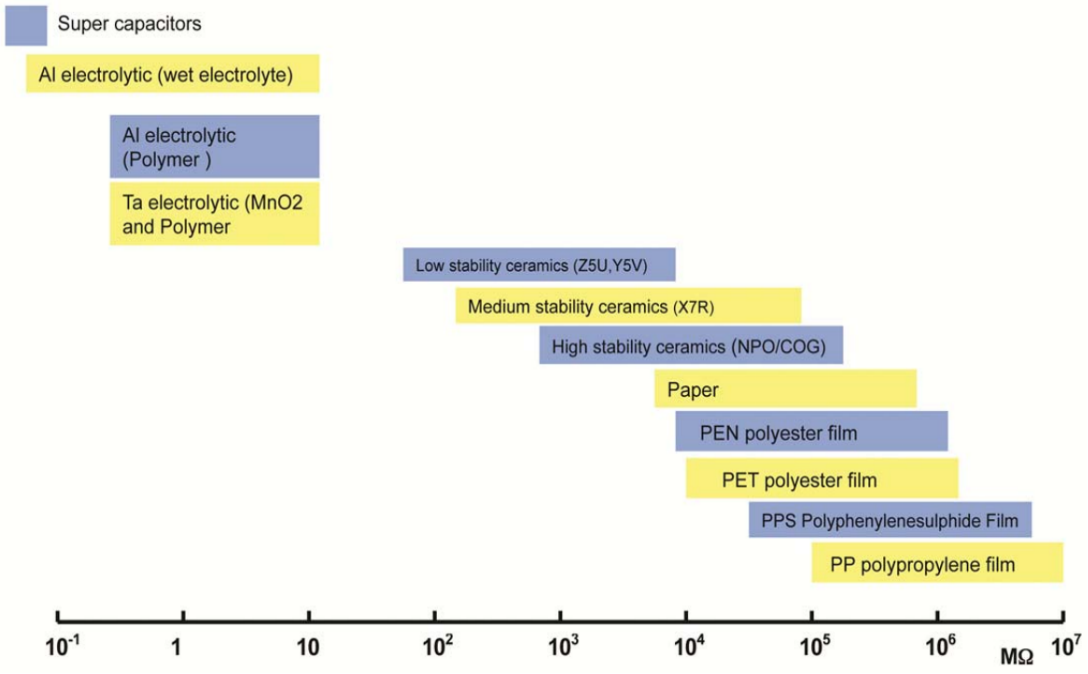


Figure 4.3: Insulation resistance for various dielectric materials [165]

The electrode resistance is frequency independent, while the dielectric resistance is high at low frequencies and decreases with increasing frequency. If $X_c$ is the total reactance of the capacitor at frequency $f_s$

$$\tan\delta(f_s) = \frac{ESR(f_s)}{X_c(f_s)} \tag{4.3}$$

As can be seen from the figure, ceramic and polymer capacitors have the lowest DF while

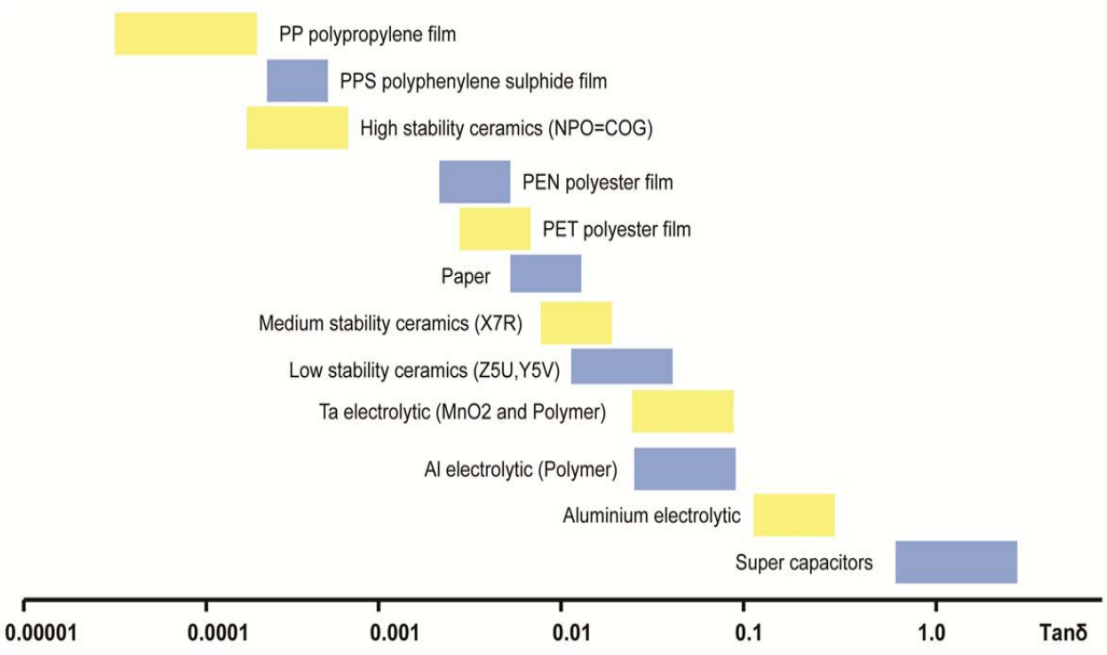


Figure 4.4: Combined DF for various dielectric materials [165]

aluminum electrolytic capacitors have the highest DF.

### 4.1.5 Ceramic capacitors

Ceramic capacitors are mainly classified into two categories based on IEC standards: Class 1 [166] or Class 2[167]. Class 1 capacitors are suitable for resonant circuit applications and offer high stability and low losses. Class 2 are suitable for smoothing, by-pass, coupling and decoupling applications and offer high volumetric efficiency [168]. The important distinction between them is that Class 1 capacitors have high accuracy and high temperature stability.

They are far more stable under variable environmental conditions. Class 2 capacitors are notorious for having widely varying characteristics and the capacitance can vary depending on the applied voltage and temperature [169, 170]. The multilayer ceramic capacitor consist of a monolithic ceramic block with comb-like sintered electrodes [171]. The chief differences between the ceramic capacitor types is listed in the table below.

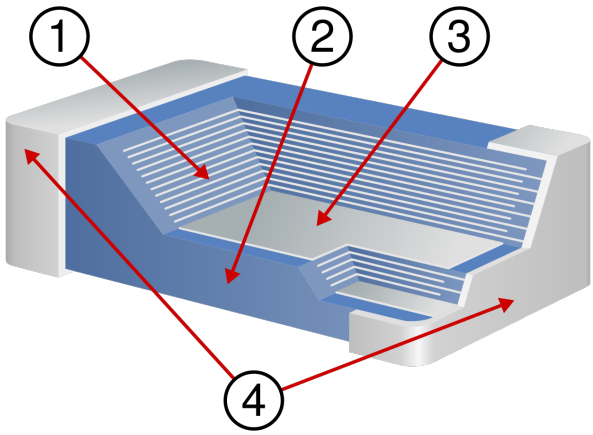


Figure 4.5: Internal structure of a MLCC capacitor: 1.Dielectric ceramic, 2.Outer ceramic layer, 3.Electrode 4.Contact surface [172]

Table 4.2: Chief differences of Class 1 and Class 2 ceramic capacitor types [168, 173, 174].

| Property | Class 1 | Class 2 |
|---|---|---|
| Dielectric | Paraelectric: $TiO_2$+additives | Ferroelectric: $BaTiO_3$+additives |
| Temperature coeff. | Defined, linear | Non-linear |
| Dissipation factor | $1.5x10^{-3}$ | $25x10^{-3}$ |
| $\epsilon_r$ | 21-40 | 200-14000 |
| EIA codes | M7G, C0G, H2G, L2G, P2H etc | X8R, X7R, X5R, Y5V, Z5U etc |

### 4.1.6 Film capacitors

Film capacitors consist of thin films of paper or plastic as dielectric material which are then metallized by aluminum or zinc to form the electrodes. The electrodes can also be inserted separately as metal foils. The entire assembly is layered or wound into cylindrical shapes. Metallized film capacitors have self-healing capability, unique among all the capacitor

technologies. If a short-circuit occurs in the capacitor due to manufacturing or other physical defects, the resulting arc vaporizes the metallized electrodes at the surface of the dielectric. This arc then clears the local fault and the mechanical defect without interrupting the normal operation of the capacitor. The basic structure of the film capacitor also provides flexibility to increase voltage rating and surge current rating by orienting the metallization in particular patterns[175].

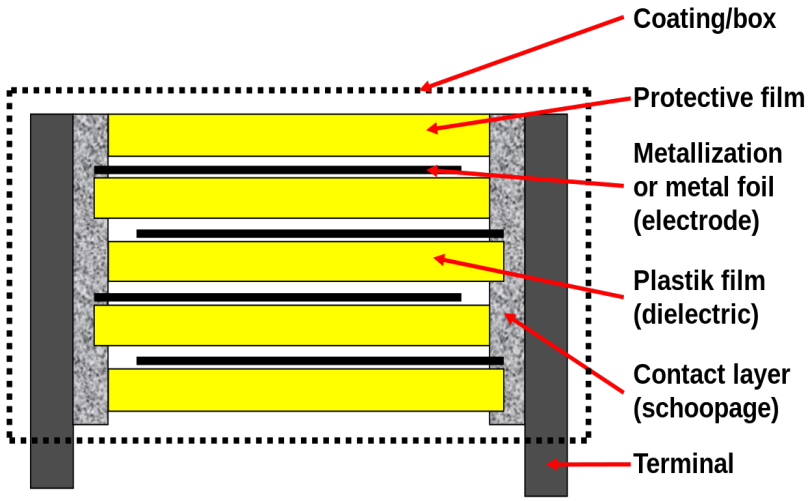


Figure 4.6: Cross-section of a plastic film capacitor [175]

Metallized film capacitors reached maturity during World War 2 with Bosch manufacturing paper film capacitors. However, the capacitors are very sensitive to impurities during construction [176, 177] and it is only starting from the 1970s these manufacturing tolerances for reliable operation have been achieved. The broad categories of film capacitors is shown in table below with the important characteristics.

Table 4.3: Characteristics of plastic film materials for film capacitors [159–162, 175].

| Characteristics | PET | PEN | PPS | PP |
|---|---|---|---|---|
| $\epsilon_r$ at 1kHz | 3.3 | 3.0 | 3.0 | 2.2 |
| Dielectric strength (V/$\mu$m) | 580 | 500 | 470 | 650 |
| DC voltage range (V) | 50-1000 | 16-250 | 16-100 | 40-2000 |
| Capacitance range (F) | 100p-22$\mu$ | 100p-1$\mu$ | 100p-0.47$\mu$ | 100p-10$\mu$ |
| Disspation factor at 100kHz | 170-300 | 120-300 | 12-60 | 2-25 |

### 4.1.7 Electrolytic capacitors

Electrolytic capacitors are polarized capacitors where the dielectric consists of an oxide of the anode electrode. This dielectric can be either aluminum oxide (aluminum anode), tantalum oxide (tantalum anode) or niobium oxide (niobium anode). This dielectric layer is further maintained by applying an anode voltage higher than cathode at all times. Reversing the polarity destroys the the dielectric oxide layer. The cathode consists of a non-solid or solid electrolyte that covers the surface of the oxide layer. Since the dielectric oxide layer is very thin and has a large surface area, electrolytic capacitors have the highest capacitance compared to film or ceramic capacitors [178].

Samuel Ruben patented the aluminum electrolytic capacitor in 1925. The structure of an aluminum capacitor consists of metal electrodes formed of aluminum foil separated by plastic or paper dielectric. The entire assembly is wound togeather to increase capacitance per unit volume. Chemical etching of the anode surface was introduced to further increase the electrode surface are. The first market for aluminum capacitors was for filtering of line-rectified voltage in early radio receivers in the 1930s. With the introduction of PCB technology in the 1960s, the structure of the capacitor was modified to fit within the low clearance tighter margins of PCBs. Contamination of the aluminum electrode with water or chlorine can destroy the dielectric and shorten lifespan. The improvements in purity and stability of modern manufacturing processes have allowed for massive increase in capacitor lifespans [179, 180].

The development of tantalum capacitors began in the post war period with the invention of the semiconductor transistor. Tantalum was powdered and then sintered to increase the surface area available for the electrodes. $MnO_2$ was developed as the solid electrode for the cathode. These innovations allowed for large scale use of tantalum capacitors for SMD applications. The discovery of conductive polymers greatly influenced the development of the modern electrolytic capacitors. Materials like TCNQ-TTF, PPy and PEDOT have lower ESR characteristics than $MnO_2$. The shortage of Tantalum in 2000 led to the useage of Niobium as an alternate material in the supply chain. Niobium capacitors have similar characteristics but are less expensive. They are also less likely to catch on fire upon failure unlike tantalum

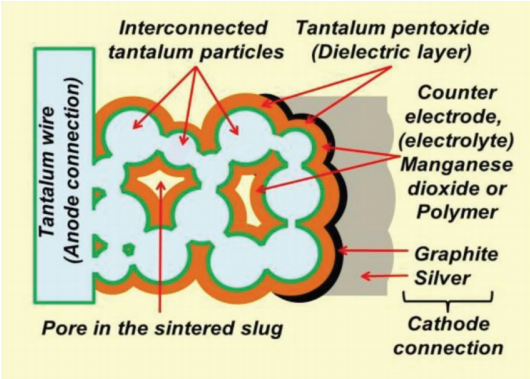


Figure 4.7: Cross-section of a sintered, oxidized tantalum pellet with a solid semiconductor as counter electrode [179].

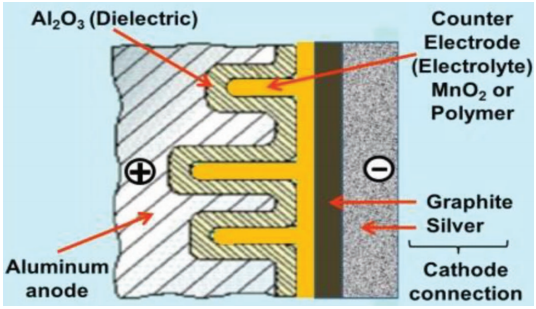


Figure 4.8: Cross-section of a solid aluminum electrolytic capacitor with a solid MnO2 or polymer electrolyte [179].

capacitors [179, 180].

## 4.2 Topological variations

### 4.2.1 Parallel coupling and cascade coupling

There are two possible configurations for coupling the input stage to the multiple output stages. The first type is termed as parallel coupled configuration with all the capacitor coupled output stages connected in parallel the input stage. In this configuration, the RMS currrent in the coupling capacitors of all output stages will be shared equally. In effect, this is an input-parallel output-series arrangement with the output stage DC load current identical in stages. As previously discussed in chapter 2, a side effect of this configuration is that the DC voltage across the coupling capacitors will vary depending on the position of the output stage with respect to the input stage. The coupling capacitors farthest away from the input stage can have a DC voltage as high as $0.5V_{out}$ while the capacitors in the middle stages can have zero average voltage. For this configuration, capacitors with high voltage rating and low current rating are most suited as coupling capacitors.

An second configuration is dubbed as cascade coupled configuration where the coupling capacitors of later output stages are cascaded with the capacitors of earlier output stages as

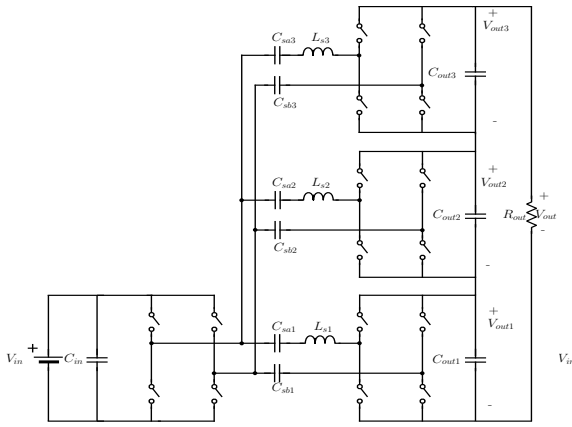


Figure 4.9: Parallel capacitor coupled single phase DC-DC converter with three output stages

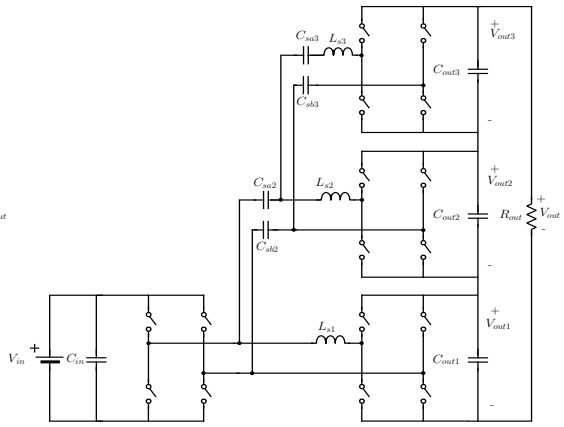


Figure 4.10: Cascade capacitor coupled single phase DC-DC converter with three output stages

shown in Fig 4.10. The consequence of this connection is that the coupling capacitor RMS current of each stage will be different with capacitors closer to the input stage conducting more current than others further away. But the coupling capacitor average DC voltages for all stages will now be equal. Additionally, the net DC voltage across all the current loops that include the input stage and the first output stage are always zero, which means that coupling capacitors that balance the DC loop voltage are not required for coupling the input stage and first output stage. The ESR of the coupling capacitor of the previous stage will have an impact on the rectified output voltage of all subsequent stages. For this configuration, coupling capacitors with low voltage rating and high current rating are most suitable. The properties of the different configuration are summarized in Table 4.4.

Table 4.4: Comparing parallel coupled and cascade coupled characteristics.

| Parameter | Parallel coupling | Cascade coupling |
|---|---|---|
| Capacitor currents (AC rms) | $i_{cs} = i_{cs} = \cdots$ | $i_{cs} \neq i_{cs} \neq \cdots$ |
| Capacitor voltages (DC avg) | $\langle v_{cs1} \rangle \neq \langle v_{cs2} \rangle \neq \cdots$ | $\langle v_{cs1} \rangle = \langle v_{cs2} \rangle = \cdots$ |
| Capacitor quantity ($n$-stages) | $2n$ | $2(n-1)$ |
| Output voltage per stage | $V_{out1} = V_{out2} = \cdots$ | $V_{out1} > V_{out2} > \cdots$ |

### 4.2.2 Unipolar and bipolar outputs

The discussion so far has focused on the multilevel capacitor coupled topologies with a single DC output. However, there are several applications that require bipolar output voltage with a ground reference. Both CCSAB and CCDAB topologies are capable of bipolar outputs with ground reference on the output. Fig 4.11-4.12 shows three phase cascade coupled converters with four output stages supporting both unipolar and bipolar DC outputs. The bipolar configuration provides a convenient terminal to ground the high voltage converter at the DC output.

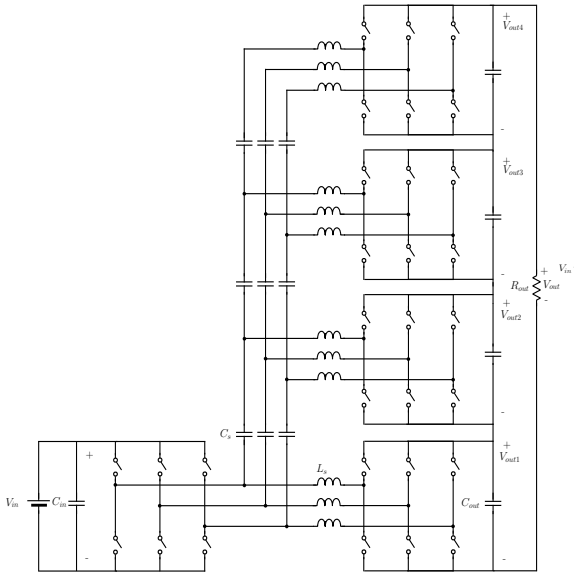


Figure 4.11: Cascade capacitor coupled three phase unipolar DC-DC converter with four output stages.

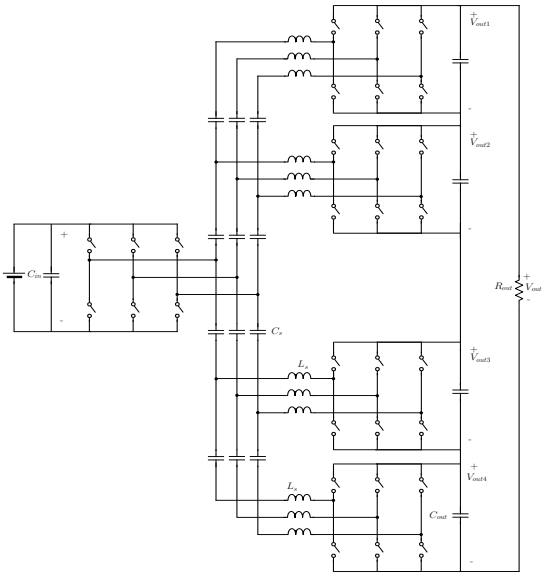


Figure 4.12: Cascade capacitor coupled three phase bipolar DC-DC converter with four output stages, two stages for each polarity

The equivalent circuit of the single phase cascade coupled CCSAB topology with bipolar output is shown in Fig 4.13.

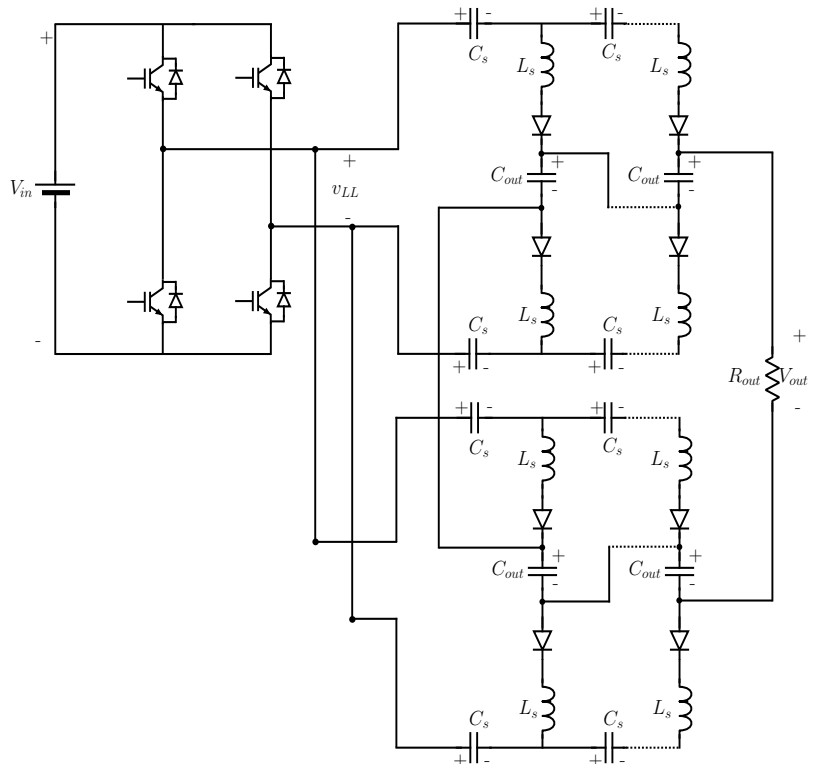


Figure 4.13: Equivalent circuit of three phase cascade coupled CCSAB topology with bipolar output.

## 4.3 Comparative evaluation of single phase CCSAB

The transformer coupled single active bridge converter (TCSAB) was first proposed by [27] as an alternative to the buck derived full bridge converter (FBC) [2]. The disadvantages of the FBC topology stem from the hard-switched PWM nature of the input side, which cause EMI issues. This effect is worsened by the presence of transformer parasitics which become more significant at higher switching frequencies. The usual solution is to incorporate snubber circuits to mitigate the rate of rise/fall of the current/voltage in the input switches. FBC topology also requires a large filter inductor at the output which acts as a current source and when coupled with the transformer causes large voltage spikes. In the TCSAB, this inductor is transferred to the AC side of the circuit which significantly modifies the operating characteristics as shown by [27]. When compared to FBC, TCSAB operates in soft-switching mode in a resonable load range which means that TCSAB is more efficient than FBC for the

same switching frequency.

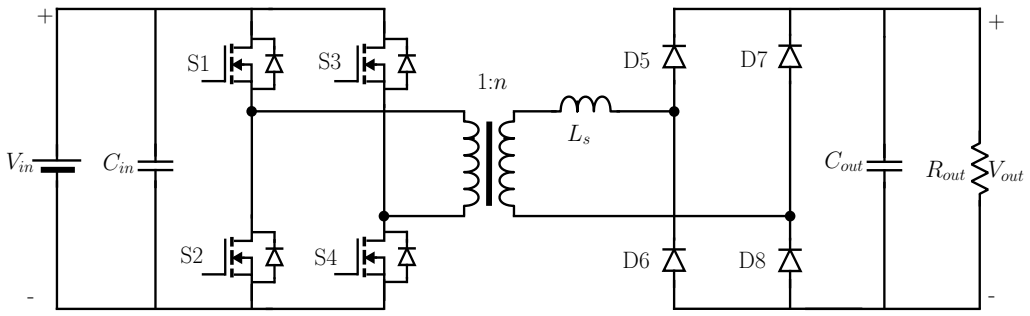


Figure 4.14: Transformer coupled single active bridge converter [27]

The capacitor coupled single active bridge converter (CCSAB) as described in this thesis is inspired by the TCSAB. Apart from the obvious difference of using capacitor coupling with multiple output stages, there are certain operational differences between CCSAB and TCSAB. The TCSAB operates in continuous inductor current mode, while CCSAB operates in discontinuous inductor current mode. The TCSAB requires phase shift modulation on the input stage to control the output voltage. The CCSAB can operate with a much simpler PWM modulation and achieve the same control characteristics. To maintain ZVS characteristics on diode turn off, the TCSAB requires snubber capacitors on the output stage. CCSAB operates in discontinuous mode where the diode turn off energy is recirculated back to the source.

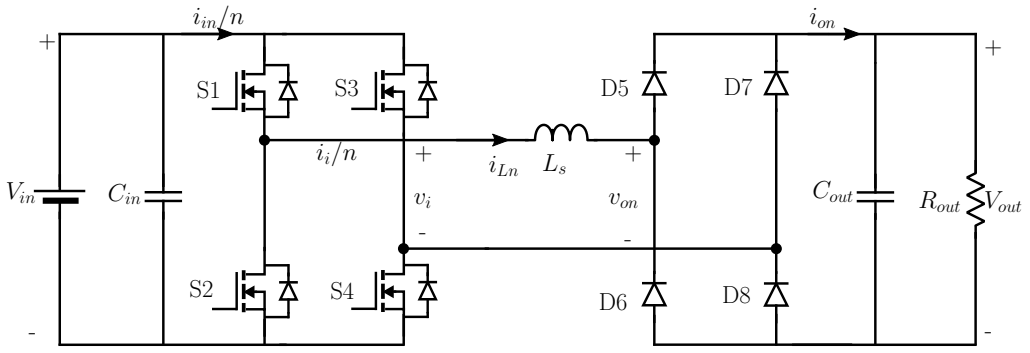


Figure 4.15: Simplified single stage equivalent circuit for both TCSAB and CCSAB

It is convenient to use an equivalent single stage unity turns-ratio converter to represent both CCSAB and TCSAB so that the analysis can be developed in a unified manner. Fig

4.15 shows the single stage equivalent circuit that is suitable for analysis of both TCSAB as well as CCSAB. The transformer of the TCSAB is modeled simply by its leakage inductance, lumped together with the series inductance of the coupling circuit, while the magnetizing inductance has been assumed to be infinite. The capacitor of CCSAB is assumed to be of negligible reactance, and has been replaced by a short circuit and the number of stages has been reduced to one. The single stage equivalent circuit has $1/n$ output power of the full TCDAB or CCDAB. There is no change in input voltage, but the input current is reduced by $1/n$. On the output side, the output voltage is $V_{outn}$ while the inductor current is $i_{Ln}$. The results from the analysis of the single stage circuit can be readily extended to the $n$-turn or $n$-stage converter as required.

### 4.3.1 Design example

For a qualitative comparison of both converter topologies, a prototype transformer-coupled and capacitor-coupled SAB converter is designed for the specifications listed in Table 4.5. Both converters are operated in simple PWM modulation scheme with discontinuous inductor current. These specifications are derived from a typical dc-dc converter application for datacenter loads [181].

Table 4.5: Single active bridge converter ratings

| $V_{in}$ | $I_{in}$ | $V_{out}$ | $I_{out}$ | $P_{out}$ | $f_s$ |
|---|---|---|---|---|---|
| V | A | V | A | W | MHz |
| 12 | 12.5 | 150 | 1 | 150 | 1 |

### 4.3.2 Design equations

#### 4.3.2.1 Input switches

The input switch current is same in case of both TCSAB and CCSAB if the transformer turns ratio of TCSAB is same as the number of stages of CCSAB. The RMS and average current of

the switches on the input side can be approximated as

$$I_{swirms} = nI_{pk}\sqrt{\frac{d_1}{3}} \tag{4.4}$$

$$I_{swiavg} = n\frac{1}{2}I_{pk}d_1 \tag{4.5}$$

where $I_{pk}$ is the peak inductor current on the secondary side in case of TCSAB and inductor current per stage in case of CCSAB. The RMS and average diode current on the input side is given as

$$I_{dirms} = nI_{pk}\sqrt{\frac{d_2}{3}} \tag{4.6}$$

$$I_{diavg} = n\frac{1}{2}I_{pk}d_2 \tag{4.7}$$

The voltage ratings of the input switches and diodes are maintained at $V_{in}$.

The only loss in the switches is during conduction. If $R_{dsoni}$ is the drain to source on-state resistance of the switching devices and $V_{fi}$ is the anode to cathode forward voltage drop of the antiparallel diode, the average loss at the input switch for both CCDAB and TCDAB is given by

$$P_{swi} = I_{swirms}^2 R_{dsoni} + I_{diavg}V_{fi} \tag{4.8}$$

#### 4.3.2.2 Output switches

Similar to the input side, the output diode currents for both TCSAB and CCSAB can be expressed as

$$I_{dorms} = I_{pk}\sqrt{\frac{d_1 + d_2}{3}} \tag{4.9}$$

$$I_{doavg} = \frac{1}{2}I_{pk}(d_1 + d_2) \tag{4.10}$$

The one difference is in the maximum reverse blocking voltage on the output side switches in case of CCSAB will be $V_{out}/n$, lower than TCSAB maintained at $V_{out}$.

Since the reverse blocking voltage in case of CCSAB is lower than TCSAB, the output side diodes will be different for the two realizations. $V_{foc}$ is the anode to cathode forward voltage

drop of the diodes on the output side of CCSAB. $V_{fot}$ is the anode to cathode forward voltage drop of the diodes on the output side of TCSAB. The average switch loss in case of CCSAB is

$$P_{swoc} = I_{doavg} V_{foc} \tag{4.11}$$

The average switch loss in case of TCSAB is

$$P_{swot} = I_{doavg} V_{fot} \tag{4.12}$$

Since the forward voltage drop of even the most efficient Schottky barrier diodes is around 0.38V, it is not possible to design a CCSAB with pure diodes on the output stages for low output voltages (100-500V) with acceptable diode conduction loss. Hence this design assumes a synchronous rectification arrangement on the output stages with the losses now limited by the $R_{dson}$ of GaN switches instead of diode forward voltage drop [182]. $R_{dson}$ can be as low as 1.3mΩ for a GaN blocking voltage of 30V.

$$P_{swoc} = I_{sworms}^2 R_{dsono} \tag{4.13}$$

#### 4.3.2.3 Transformer

The converter operating point for both TCSAB and CCSAB is selected such that the inductor current is discontinuous mode. Discontinuous conduction mode also means that the peak current will be as high as 2x the RMS current. Hence the transformer needs to be designed such that the core will not saturate for the entire operating range. The area product can be defined in terms of the sum of KVA on the primary and secondary winding.

$$\sum VA = V_{in} n I_{Lrms} + V_{out} I_{Lrms} \tag{4.14}$$

$$A_p = \frac{\sum VA}{B_{max} F_s J_{max} K_f K_a} \tag{4.15}$$

where $K_f$ is the waveform coefficient (8 for discontinuous triangle wave), $B_{max}$ is the designed maximum flux density in the core, $J_{max}$ is the maximum designed current density in the copper winding, $F_s$ is the switching frequency and $K_u$ is the window utilization factor.

The sources of loss in the transformer are core loss in the magnetic core and copper loss in the winding. If the winding is designed to have diameter less than the skin depth of copper at the switching frequency, the copper loss can be modeled in terms of DC resistance. The core loss is derived from the datasheet of the ferrite material for the core. If $V_e$ is the volume of core, $B_{max}$ is the maximum flux density in the core, $K_c$, $\alpha$ and $\beta$ are constants derived from the datasheet, the core loss is derived as

$$P_{core} = V_e K_c F_s^{\alpha} B_{max}^{\beta} \tag{4.16}$$

The copper loss is derived as

$$P_{cupri} = (nI_{Lrms})^2 R_{dcpri} \tag{4.17}$$

$$P_{cusec} = I_{Lrms}^2 R_{dcsec} \tag{4.18}$$

where $R_{dcpri}$ and $R_{dcsec}$ are the primary and secondary copper winding resistance at DC.

#### 4.3.2.4 Series coupling capacitor

The capacitance is selected such that the capacitive impedance at switching frequency is negligible.

$$C_s = \frac{2K_{opt}T_s}{R_{outn}} \tag{4.19}$$

The maximum voltage rating of the capacitors are maintained at $V_{out}/2$, while the RMS current ratings are identical to $I_{Lrms}$.

#### 4.3.2.5 Series inductor

The series inductor is assumed to be on the secondary side of the transformer for TCSAB, since it leads to smaller currents. Since both TCSAB and CCSAB have the same discontinuous inductor current PWM strategy, the same series inductor can be selected for both topologies.

$$L_s = \frac{T_s}{2}\frac{R_{outn}}{K_{opt}} \tag{4.20}$$

### 4.3.3 Efficiency

The inductor is designed such that the inductor current for both CCSAB and TCSAB is discontinuous. This results in peak currents that in turn lead to additional core loss in the transformer. As can be seen from Table 4.6, the biggest loss component in case of TCSAB is the high frequency transformer. The transformer as designed for this application represents a realistic design and not the most optimized design specifically in terms of core loss or copper loss. An additional factor to consider is that the converters are designed to dissipate semiconductor power loss via air convection and copper trace conduction cooling. This means that the estimated volume of the converter is also quite realistic.

### 4.3.4 Volume

Table 4.6 illustrates the volume of major power circuit components for both TCSAB and CCSAB. The volume of each component is calculated using the exact mechanical specifications in the datasheets and does not account for the volumetric clearance needed for creepage clearance and layout. From the table, CCSAB is 4x better than TCSAB in terms of volumetric power density. The semiconductor switch volume does not include any gate drive circuits on the input stage. Such aspects related to the physical realization will affect the final 'box' volume of the power converters and are the subject of continuing investigations.

Table 4.6: Volume and loss comparison of single phase TCSAB and CCSAB

| Component | **TCSAB** | | **CCSAB** | |
|---|---|---|---|---|
| | Vol. [$mm^3$] | Loss [W] | Vol. [$mm^3$] | Loss [W] |
| Series inductor | 17.6 | 0.05 | 246.4 | 0.69 |
| Transformer | 15600 | 1.11 | N/A | |
| Series capacitor | N/A | | 2234 | 0.57 |
| Input switch | 38 | 2 | 38 | 2 |
| Output switch | 4 | 4.5 | 533 | 8.31 |
| Total volume | **15700** | | **3052** | |
| Total Loss | | 7.78 | | 11.65 |
| Efficiency | | **94%** | | **92%** |

Table 4.7: Design details of switching elements for a 12V-150V, 150W TCSAB and CCSAB converter operating at 1MHz

| | | **Input SW S1-S4** | | **Output SW S5-S8** | |
|---|---|---|---|---|---|
| | Units | TCSAB | CCSAB | TCSAB | CCSAB |
| Quantity | | 4 | 4 | 4 | 56 |
| max($v_{sw}$) | V | 12 | 12 | 150 | 12 |
| rms($i_{sw}$) | A | 19.98 | 19.98 | 1.428 | 1.428 |
| max($i_{sw}$) | A | 40.73 | 40.73 | 2.909 | 2.909 |

Table 4.8: Design details of passive elements for a 12V-150V, 150W TCSAB and CCSAB converter operating at 1MHz

| **Transformer** | | | **Series Capacitor** | | |
|---|---|---|---|---|---|
| Core: Ferroxcube 3F45 EQ-30 | | | Dielectric: Ceramic | | |
| Copper: Foil (pri), Litz (sec) | | | | | |
| | Units | TCSAB | | Units | CCSAB |
| Quantity | | 1 | Quantity | | 28 |
| Turns | | 2:28 | $C_s$ | $\mu$F | 7 |
| max(rms($i_p$)) | A | 19.98 | ESR | $\Omega$ | 0.01 |
| max(rms($i_s$)) | A | 1.42 | max($i_c$) | A | 2.90 |
| max($v_p$) | V | 12 | rms($i_c$) | A | 1.42 |
| max($v_s$) | V | 150 | max($v_c$) | V | 75 |

Table 4.9: Design details of passive elements for a 12V-150V, 150W TCSAB and CCSAB converter operating at 1MHz

| | | **Output capacitor** | | | | **Series inductor** | |
|---|---|---|---|---|---|---|---|
| | Units | TCSAB | CCSAB | | Units | TCSAB | CCSAB |
| Quantity | | 1 | 14 | Quantity | | 1 | 14 |
| $C_{out}$ | $\mu$F | 0.1 | 1 | $L_s$ | nH | 90 | 90 |
| max($v_{out}$) | V | 150 | 12 | ESR | m$\Omega$ | 24 | 24 |
| | | | | max($i_L$) | A | 2.909 | 2.909 |
| | | | | rms($i_L$) | A | 1.428 | 1.428 |
| | | | | max($v_L$) | V | 162 | 24 |

## 4.4 Comparative evaluation of single phase CCDAB

The transformer coupled (TCDAB) and capacitor coupled (CCDAB) converters have the same full bridge structure at the input terminals of the ac side. In case of TCDAB, the voltage gain from input to output is achieved via the transformer turns ratio defined as $n \geq \frac{V_{out}}{V_{in}}$. There is a single series inductor $L_s$ which is referred to the output side acts as the intermediary current stiff component to interface between two fixed voltage stiff components $C_{in}$ and $C_{out}$. In case of CCDAB, the output voltage is realized through the series connection of several

output states at the dc terminals. Each output stage consists of two series capacitors $C_{sa}$ and $C_{sb}$, series inductor $L_s$, converter full-bridge S5-S8 and an output filter capacitor $C_{out}$. The voltage transformation in case of a CCDAB is similarly defined as $n \geq \frac{V_{out}}{V_{in}}$. Both the converters control the output voltage via phase shift modulation between the input and output stages.

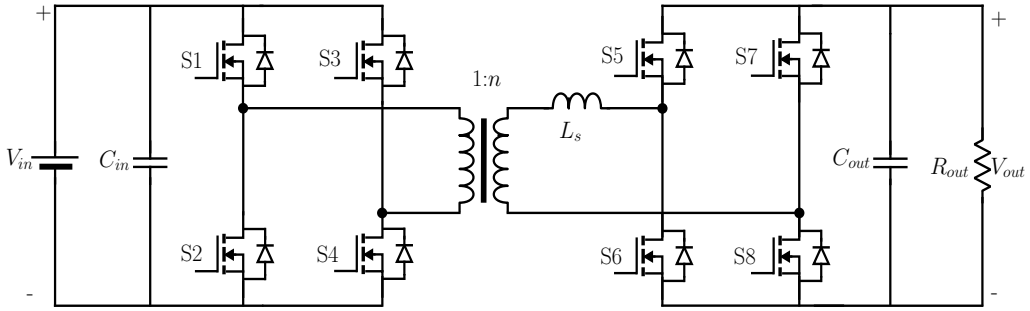


Figure 4.16: Transformer coupled dual active bridge converter [27]

It is convenient to use an equivalent single stage unity turns-ratio converter to represent both CCDAB and TCDAB so that the analysis can be developed in a unified manner. Fig 4.17 shows the single stage equivalent circuit that is suitable for analysis of both TCDAB as well as CCDAB. The transformer of the TCDAB is modeled simply by its leakage inductance, lumped together with the series inductance of the coupling circuit, while the magnetizing inductance has been assumed to be infinite. The capacitor of CCDAB is assumed to be of negligible reactance, and has been replaced by a short circuit and the number of stages has been reduced to one. The single stage equivalent circuit has $1/n$ output power of the full TCDAB or CCDAB. There is no change in input voltage, but the input current is reduced by $1/n$. On the output side, the output voltage is $V_{outn}$ while the inductor current is $i_{Ln}$. The results from the analysis of the single stage circuit can be readily extended to the $n$-turn or $n$-stage converter as required.

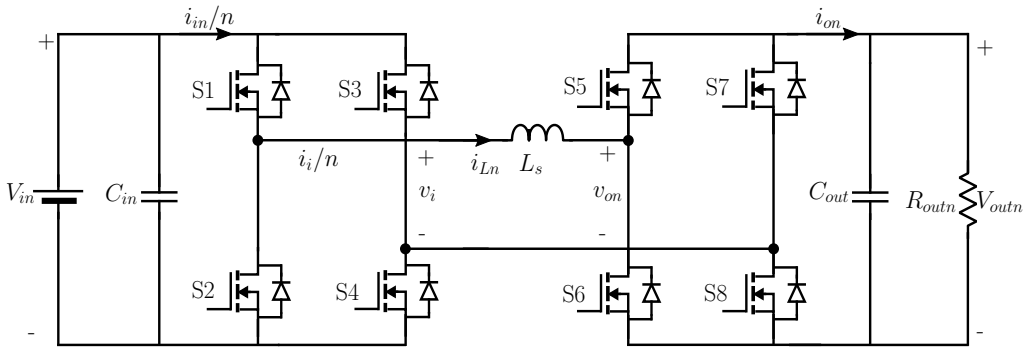


Figure 4.17: Simplified single stage equivalent circuit for both TCDAB and CCDAB

### 4.4.1 Design example

For a qualitative comparison of both converter topologies, a prototype transformer-coupled and capacitor-coupled DAB converter is designed for the specifications listed in Table 4.10. These specifications are derived from a typical dc-dc converter application for datacenter loads [181].

Table 4.10: Dual Active Bridge converter ratings

| $V_{in}$ | $I_{in}$ | $V_{out}$ | $I_{out}$ | $P_{out}$ | $f_s$ |
|---|---|---|---|---|---|
| V | A | V | A | W | MHz |
| 12 | 12.5 | 150 | 1 | 150 | 1 |

### 4.4.2 Design equations

#### 4.4.2.1 Input switches

The input switch current is same in case of both TCDAB and CCDAB if the transformer turns ratio of TCDAB is same as the number of stages of CCDAB. The rms current of the switches on the input side can be approximated as

$$I_{swirms} = n\sqrt{\frac{I_{L0}^2 + |I_{L0}||I_{L1}| + I_{L1}^2}{3}\frac{(0.5T_s - T_\phi)}{T_s}} \tag{4.21}$$

where $I_L$ is the inductor current on the secondary side in case of TCDAB and inductor current per stage in case of CCDAB. The average switch current can be similarly defined as

$$I_{swiavg} = n\frac{1}{4T_s}\left[|I_{L0}|(T_s - 2t_D) + |I_{L1}|(T_s - 2T_\phi))\right] \tag{4.22}$$

The diode current on the input side is given as

$$I_{dirms} = n\sqrt{\frac{I_{L0}^2}{3}\frac{t_D}{T_s}} \tag{4.23}$$

$$I_{diavg} = n\frac{I_{L0}}{2}\frac{t_D}{T_s} \tag{4.24}$$

The voltage ratings of the input switches and diodes are maintained at $V_{in}$.

Both the input and output switches are operated under ZVS conditions which implies that switching loss is negligible. The only loss in the switches is during conduction. If $R_{dsoni}$ is the drain to source on-state resistance of the switching devices and $V_{fi}$ is the anode to cathode forward voltage drop of the antiparallel diode, the average loss at the input switch for both CCDAB and TCDAB is given by

$$P_{swi} = I_{swirms}^2 R_{dsoni} + I_{diavg} V_{fi} \tag{4.25}$$

#### 4.4.2.2 Output switches

Similar to the input side, the output switch currents will also be derived.

$$I_{sworms} = \sqrt{\frac{I_{L0}^2 + |I_{L0}||I_{L1}| + I_{L1}^2}{3}\frac{(0.5T_s - T_\phi)}{T_s}} \tag{4.26}$$

$$I_{swoavg} = \frac{1}{4T_s}\left[|I_{L0}|T_s + |I_{L1}|(T_s + 2t_D - 2T_\phi))\right] \tag{4.27}$$

The one difference is in the maximum reverse blocking voltage on the output side switches in case of CCDAB will be lower than TCDAB. The diode current on the output side is given as

$$I_{dirms} = \sqrt{\frac{I_{L1}^2}{3}\frac{T_\phi - t_D}{T_s}} \tag{4.28}$$

$$I_{diavg} = \frac{I_{L1}}{2}\frac{T_\phi - t_D}{T_s} \tag{4.29}$$

The voltage ratings of the output switches and diodes are maintained at $V_{out}$ in the case of TCDAB, and $V_{out}/n$ in the case of CCDAB.

Since the reverse blocking voltage in case of CCDAB is lower than TCDAB, the output side switches will be different for the two realizations. $R_{dsonc}$ is the drain to source on-state resistance of the switching devices and $V_{foc}$ is the anode to cathode forward voltage drop of the antiparallel diode on the output side of CCDAB. $R_{dsont}$ is the drain to source on-state resistance of the switching devices and $V_{fot}$ is the anode to cathode forward voltage drop of the antiparallel diode on the output side of TCDAB. The average switch loss in case of CCDAB is

$$P_{swoc} = I_{sworms}^2 R_{dsonc} + I_{doavg} V_{foc} \tag{4.30}$$

The average switch loss in case of TCDAB is

$$P_{swot} = I_{sworms}^2 R_{dsont} + I_{doavg} V_{fot} \tag{4.31}$$

#### 4.4.2.3 Transformer

The RMS current of the transformer winding on the input side will be approximately same as the switch current on the input side, if the phase difference is assumed negligible. Similarly, the RMS current of the transformer winding on the output side will be same as the switch current on the output side. The RMS voltage of the primary winding is $V_{in}$ and on the secondary winding is $V_{out}$. The area product is a measure of the power handling capability of the transformer. The area product in terms of the sum of KVA on the primary and secondary winding is

$$\sum VA = V_{in} n I_{Lrms} + V_{out} I_{Lrms} \tag{4.32}$$

$$A_p = \frac{\sum VA}{B_{max} F_s J_{max} K_f K_a} \tag{4.33}$$

where $K_f$ is the waveform coefficient (4.0 for square wave), $B_{max}$ is the designed maximum flux density in the core, $J_{max}$ is the maximum designed current density in the copper winding, $F_s$ is the switching frequency and $K_u$ is the window utilization factor.

The sources of loss in the transformer are core loss in the magnetic core and copper loss in the winding. If the winding is designed to have diameter less than the skin depth of copper at the switching frequency, the copper loss can be modeled in terms of DC resistance. The core loss is derived from the datasheet of the ferrite material for the core. If $V_e$ is the volume of core, $B_{max}$ is the maximum flux density in the core, $K_c$, $\alpha$ and $\beta$ are constants derived from the datasheet, the core loss is derived as

$$P_{core} = V_e K_c F_s^{\alpha} B_{max}^{\beta} \tag{4.34}$$

The copper loss is derived as

$$P_{cupri} = (nI_{Lrms})^2 R_{dcpri} \tag{4.35}$$

$$P_{cusec} = I_{Lrms}^2 R_{dcsec} \tag{4.36}$$

where $R_{dcpri}$ and $R_{dcsec}$ are the primary and secondary copper winding resistance at DC.

#### 4.4.2.4 Series coupling capacitor

The capacitance is selected such that the capacitive impedance at switching frequency is negligible.

$$C_s > \frac{50}{R_{outn} F_s} \tag{4.37}$$

The maximum voltage rating of the capacitors are maintained at $V_{out}/2$, while the RMS current ratings are identical to $I_{Lrms}$.

The power loss in a capacitor depends on the equivalent series resistance of the capacitor. ESR is expressed in terms of the dissipation factor ($\tan\delta$) of the capacitor.

$$X_c = \frac{1}{2\pi F_s C_s} \tag{4.38}$$

$$R_{cs} = X_c \tan\delta \tag{4.39}$$

$$P_{cs} = I_{Lrms}^2 R_{cs} \tag{4.40}$$

#### 4.4.2.5 Series inductor

The series inductor is assumed to be on the secondary side of the transformer for TCDAB, since it leads to smaller currents. The design value for the inductance for rated power transfer in case of TCDAB can be derived from the power equation with approximation for small $\phi = \pi/16$, to be

$$L_s \leq \frac{nV_{in}V_{out}}{32F_sP_{out}} \tag{4.41}$$

In the case of CCDAB, one series inductor is present in the series path of each of the stages whose value may be determined to be

$$L_s \leq \frac{V_{in}V_{outn}}{32F_sP_{outn}} \tag{4.42}$$

The series inductance can be designed as part of the transformer leakage inductance. If the series inductance is designed as an individual component using off-the-shelf parts, the power loss can be derived from the series equivalent resistance ESR $R_{Ls}$.

$$P_{Ls} = I_{Lrms}^2 R_{Ls} \tag{4.43}$$

### 4.4.3 Volume

Table 4.11 illustrates the volume of major power circuit components for both TCDAB and CCDAB. The volume of each component is calculated using the exact mechanical specifications in the datasheets and does not account for the volumetric clearance needed for creepage clearance and layout. From the table, CCDAB is 4x better than TCDAB in terms of volumetric power density. The semiconductor switch volume does not include any gate drive circuits. Such aspects related to the physical realization will affect the final 'box' volume of the power converters and are the subject of continuing investigations.

### 4.4.4 Efficiency

The transformer as designed for this application represents a realistic design and not the most optimized design specifically in terms of core loss or copper loss. When comparing active

semiconductor devices, it can be observed from the previous section the maximum blocking voltage on the output and input stage depend on the output and input voltage respectively in case of TCDAB. In case of CCDAB, due to the output-parallel topology, all the active semiconductor devices are rated for the same input voltage. Under rated operating conditions, both the input and output bridges operate under ZVS, and hence have no switching losses. This, combined with negligible conduction loss means that the total semiconductor power loss can be dissipated via air convection and copper trace conduction cooling.

Table 4.11: Volume and loss comparison of TCDAB and CCDAB

| Component | **TCDAB** | | **CCDAB** | |
|---|---|---|---|---|
| | Vol. [mm$^3$] | Loss [W] | Vol. [mm$^3$] | Loss [W] |
| Series inductor | 48 | 0.1 | 1022 | 0.5 |
| Transformer | 15600 | 0.65 | N/A | |
| Series capacitor | N/A | | 2230 | 0.2 |
| Input switch | 38 | 0.92 | 38 | 1.22 |
| Output switch | 4 | 1.96 | 533 | 4.89 |
| Total volume | **15700** | | **3800** | |
| Total Loss | | 3.64 | | 6.79 |
| Efficiency | | **97%** | | **95%** |

Table 4.12: Design details of switching elements for a 12V-150V, 150W TCDAB and CCDAB converter operating at 1MHz

| | | **Input SW S1-S4** | | **Output SW S5-S8** | |
|---|---|---|---|---|---|
| | Units | TCDAB | CCDAB | TCDAB | CCDAB |
| Quantity | | 4 | 4 | 4 | 56 |
| max($v_{sw}$) | V | 12 | 12 | 150 | 12 |
| rms($i_{sw}$) | A | 10.65 | 10.65 | 0.782 | 0.761 |
| max($i_{sw}$) | A | 25.39 | 25.39 | 1.814 | 1.814 |
| max($R_{dson}$) | mΩ | 1.3 | 1.3 | 100 | 1.3 |

## 4.5 Comparative evaluation of three phase CCSAB

A popular method to generate high voltages from a three phase grid frequency power supply is by using a high voltage transformer to first boost low voltage AC to high voltage AC and then subsequently rectify the high voltage AC using three phase diode bridge rectifiers as shown in Fig 4.18. This is essentially a version of the three phase transformer coupled single

Table 4.13: Design details of passive elements for a 12V-150V, 150W TCDAB and CCDAB converter operating at 1MHz

| **Transformer** Core: Ferroxcube 3F45 EQ-30 Copper: Foil (pri), Litz (sec) | | | **Series Capacitor** Dielectric: Ceramic | | |
|---|---|---|---|---|---|
| | Units | TCDAB | | Units | CCDAB |
| Quantity | | 1 | Quantity | | 28 |
| Turns | | 3:42 | $C_s$ | $\mu$F | 7 |
| max(rms($i_p$)) | A | 14.12 | ESR | $\Omega$ | 0.01 |
| max(rms($i_s$)) | A | 1.07 | max($i_c$) | A | 1.81 |
| max($v_p$) | V | 12 | rms($i_c$) | A | 1.07 |
| max($v_s$) | V | 150 | max($v_c$) | V | 75 |

Table 4.14: Design details of passive elements for a 12V-150V, 150W TCDAB and CCDAB converter operating at 1MHz

| | **Output capacitor** | | | | **Series inductor** | | |
|---|---|---|---|---|---|---|---|
| | Units | TCDAB | CCDAB | | Units | TCDAB | CCDAB |
| Quantity | | 1 | 14 | Quantity | | 1 | 14 |
| $C_{out}$ | $\mu$F | 0.1 | 1 | $L_s$ | $\mu$H | 5.25 | 0.375 |
| max($v_{out}$) | V | 150 | 12 | ESR | m$\Omega$ | 90 | 30 |
| | | | | max($i_L$) | A | 1.81 | 1.81 |
| | | | | rms($i_L$) | A | 1.07 | 1.07 |
| | | | | max($v_L$) | V | 306 | 24 |

active bridge converter (TCSAB). All the components on the secondary side of the transformer must be rated for the output voltage including the three phase diode bridge rectifier and the output filter capacitor. The isolation transformer itself must be rated for a Basic Impulse Level of atleast two to three times the output voltage. In comparison, the three phase cascade

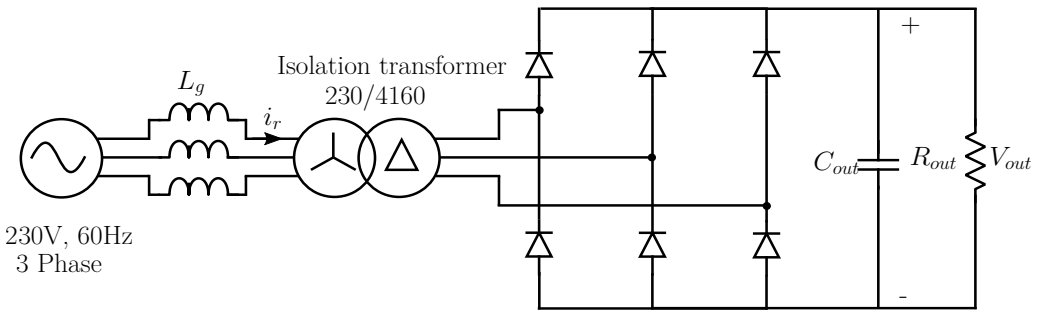


Figure 4.18: Three phase 60 Hz diode bridge rectifier with high voltage transformer.

coupled CCSAB topology provides an alternative configuration to achieve high voltage DC using the low voltage rated modular multilevel configuration described in earlier chapters.

The topology is well suited for delivering high output voltages at low currents which is the typical requirement of load application at high voltage DC.

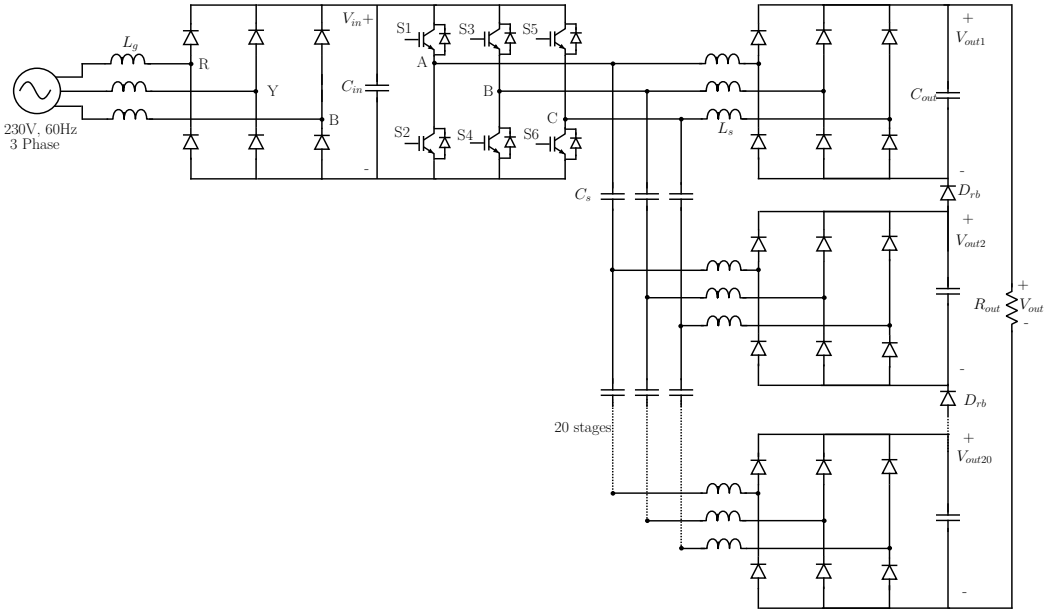


Figure 4.19: Three phase cascade coupled CCSAB topology with 60 Hz diode bridge rectifier front-end.

### 4.5.1 Design example

For a qualitative comparison of both converter topologies, a prototype three phase transformer coupled and capacitor coupled SAB converter is designed for the specifications listed in Table 4.15. These specifications are derived from a 6kV, 6kW DC output required for an electrostatic machine.

Table 4.15: Three phase rectified DC power supply

| $V_{in}$ | $I_{in}$ | $V_{out}$ | $I_{out}$ | $P_{out}$ |
|---|---|---|---|---|
| V | A | kV | A | kW |
| 230 | 16 | 6 | 1 | 6 |

### 4.5.2 Design equations

#### 4.5.2.1 Input source

The input souce for both three phase TCSAB and CCSAB is the standard three phase 230V 60Hz grid that is common in North America. The grid inductance per phase $L_g$ in both cases is assumed to be 0.2mH. The grid current per phase can be calculated from the output power $P_{out}$ and the line-to-line grid voltage $V_{ry}$ as

$$I_r = \frac{P_{out}}{\sqrt{3}V_{ry}} \tag{4.44}$$

The input side of the three phase TCSAB converter is directly coupled to the grid. In case of the three phase CCSAB, a 60Hz diode front end feeds a DC voltage which acts as the source to the three phase IGBT based inverter.

#### 4.5.2.2 Transformer

A standard NEMA rated medium voltage three phase star delta 230/4160 isolation transformer is selected as the step-up transformer for this application [183]. The transformer specifications are shown in Table 4.16.

Table 4.16: Three phase 230/4160 transformer ratings

| Parameter | Unit | Value |
|---|---|---|
| Input voltage | V-LL-RMS | 230 |
| Output voltage | V-LL-RMS | 4160 |
| Frequency | Hz | 60 |
| VA | kVA | 15 |
| Winding type | N/A | Copper |
| Insulation class | °C | 220 |
| Enclosure rating | N/A | NEMA 3R |
| Impedance | pu % | 3 |
| BIL | kV | 20 |
| Efficiency | % | 97.5 |

#### 4.5.2.3 Input switches

As mentioned before, the three phase TCSAB is directly coupled to the grid on the input side which means that there is no input switches to modulate the power flow on the input stage of the transformer. The input switches in the three phase CCSAB consists of a three phase two level IGBT inverter. The inverter is operating on six-step modulation scheme at 50% duty cycle with switching time period set as $T_s$ and deadtime between the switches in the same phase $T_d$ set to $0.02T_s$. The RMS current per phase on the input side for one half switching cycle can be derived from the steady state behavior of the three phase CCSAB as shown in chapter 2. The AC current in a single stage $i_{an}$ can be derived in terms of the DC bus voltage $V_{in}$, rectified output voltage per stage $V_{outn}$ and series inductance $L_s$. For the condition where the commutation time $t_c$ is greater than the deadtime,

$$i_{an}(t) = \begin{cases} -I_c + \frac{1}{L_s}\frac{V_{in}+V_{outn}}{3} & 0 < t < t_c \\ 0 + \frac{1}{L_s}\frac{V_{in}-V_{outn}}{3} & t_c < t < \frac{T_s}{6} \\ I_p - \frac{1}{L_s}\frac{V_{outn}-2V_{in}}{3} & \frac{T_s}{6} < t < \frac{T_s}{6} + t_c \\ I_{min} + \frac{2}{L_s}\frac{V_{in}+V_{outn}}{3} & \frac{T_s}{6} + t_c < t < \frac{2T_s}{6} \\ I_{max} + \frac{1}{L_s}\frac{V_{in}-2V_{out}}{3} & \frac{2T_s}{6} < t < \frac{2T_s}{6} + t_c \\ I_{min} + \frac{1}{L_s}\frac{V_{in}-V_{outn}}{3} & \frac{2T_s}{6} + t_c < t < \frac{3T_s}{6} \end{cases} \tag{4.45}$$

where $I_c, I_p, I_{min}, I_{max}$ are defined in Chapter 2. From the AC current per phase, the AC current in the input stage can be derived as

$$I_a = N i_{an} \tag{4.46}$$

where $N$ refers to the number of output stages and $i_{an}$ refers to AC current per stage. The voltage ratings of the input switches and diodes are maintained at $V_{in}$. The RMS current rating of the input switches can be calculated as

$$I_{swirms} = \sqrt{\frac{1}{T_s}\int_0^{T_s} I_a^2 \; dt} \tag{4.47}$$

#### 4.5.2.4 Output switches

The output stage in case of the TCSAB consists of six diodes in the configuration of a three phase diode bridge rectifier. There are twenty output stages in the CCSAB configuration with each stage having a single diode bridge rectifier module in a TO247 package.

#### 4.5.2.5 Series coupling capacitors

All the output stages are coupled to the input stage via cascade coupling using three phase capacitors. In cascade coupling all coupling capacitors have approximately the same DC bias voltage while the AC RMS current through the individual stages is different in each output stage. The capacitor voltage rating depends on the maximum rectified voltage of any output stage. The current rating of any individual coupling capacitor depends on its position with respect to the input stage. The maximum AC current in the series coupling capacitors can be estimated as

$$I_{csrms} = (N-1)i_{an} \tag{4.48}$$

#### 4.5.2.6 Series inductor

The series inductor current is same in all output stages and can be estimated using Eq 4.45.

$$I_{lrms} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{an}^2 \; dt} \tag{4.49}$$

The peak inductor current in any output stage will be equal to $I_{max}$ as shown in Chapter 2.

### 4.5.3 Volume

Table 4.17 illustrates the volume of major power circuit components for both TCSAB and CCSAB. The volume of each component is calculated using the exact mechanical specifications in the datasheets and does not account for the volumetric clearance needed for creepage clearance and layout. The overall system volume of CCSAB is estimated from the cabinet size that includes all components. From the table, a three phase cascade coupled CCSAB topology

is smaller than TCDAB for the same power rating. The TCSAB estimated volume does not include bus bars, relays, switches and other protection equipment that would be required for such converter configuration.

### 4.5.4 Efficiency

The transformer selected for the three phase TCSAB design is a general purpose medium voltage 15kVA transformer that is NEMA rated for 97.5% efficiency at full load conditions. This can give an estimate of the projected loss when operating under nominal conditions as part of the TCSAB. The losses in the CCSAB calculated using the analytical equations described in Chapter 2. The losses on the three phase TCSAB do not include the effect of input 60 Hz current harmonics on the efficiency characteristics of the transformer and other miscellaneous losses due to bleeder resistors on the DC bus capacitors.

Table 4.17: Volume and loss comparison of three phase TCSAB and CCSAB

| Component | **TCSAB** | | **CCSAB** | |
|---|---|---|---|---|
| | Vol. [L] | Loss [W] | Vol. [L] | Loss [W] |
| Series inductor | N/A | | 0.11 | 2.93 |
| Transformer | 281.5 | 196.23 | N/A | |
| Series capacitor | N/A | | 70.51 | 155.52 |
| Input switch | N/A | | 0.93 | 71.52 |
| Output switch | 0.48 | 13.8 | 0.04 | 17.88 |
| Filter capacitor | 109.82 | 1.52 | 6.19 | 0.03 |
| 60 Hz diodes | N/A | | 0.38 | 82.44 |
| Total volume | **391.8** | | **78.16** | |
| Total Loss | | 211.37 | | 900 |
| Efficiency | | **96.46%** | | **93.38%** |

Table 4.18: Design details of switching elements for a 6kV, 6kW three phase TCSAB and CCSAB converter

| | | **Input SW S1-S4** | | **Output SW S5-S8** | |
|---|---|---|---|---|---|
| | Units | TCSAB | CCSAB | TCSAB | CCSAB |
| Quantity | | N/A | 6 | 6 | 120 |
| max($v_{sw}$) | V | N/A | 320 | 6000 | 320 |
| rms($i_{sw}$) | A | N/A | 14.72 | 0.776 | 0.756 |
| max($i_{sw}$) | A | N/A | 23.59 | 2.133 | 1.244 |

Table 4.19: Design details of passive elements for a 6kV, 6kW three phase TCSAB and CCSAB converter

| **Transformer** | | | **Series Capacitor** | | |
|---|---|---|---|---|---|
| Core: CRGO Silicon steel | | | Dielectric: Electrolyte | | |
| Copper: Wire (pri, Y), Wire (sec, $\Delta$) | | | Conn: Two parallel per phase | | |
| | Units | TCSAB | | Units | CCSAB |
| Quantity | | 1 | Quantity | | 114 |
| Turns | | 1:32 | $C_s$ | $\mu$F | 1500 |
| max(rms($i_p$)) | A | 19.76 | ESR | m$\Omega$ | 100 |
| max(rms($i_s$)) | A | 1.06 | max($i_c$) | A | 11.79 |
| max($v_p$) | V | 325 | rms($i_c$) | A | 7 |
| max($v_s$) | V | 6000 | max($v_c$) | V | 320 |

Table 4.20: Design details of passive elements for a 6kV, 6kW three phase TCSAB and CCSAB converter

| | | **Output capacitor** | | | | **Series inductor** | |
|---|---|---|---|---|---|---|---|
| | Units | TCSAB | CCSAB | | Units | TCSAB | CCSAB |
| Quantity | | 3 | 20 | Quantity | | N/A | 60 |
| $C_{out}$ | $\mu$F | 330 | 1500 | $L_s$ | $\mu$H | | 100 |
| max($v_{out}$) | V | 3000 | 320 | ESR | m$\Omega$ | | 90 |
| | | | | max($i_L$) | A | | 1.244 |
| | | | | rms($i_L$) | A | | 0.776 |
| | | | | max($v_L$) | V | | 211 |

## 4.6 Summary

The critical characteristics of capacitor coupled converters are examined in this chapter. The main component of both CCSAB and CCDAB is the coupling capacitor. The capacitor current and voltage characteristics can be very different depending on the topological variation. It can be seen that series coupled designs are limited by the capacitor voltage rating while cascade coupled designs are limited by capacitor current ratings. Also in order to understand the utility of the proposed topology, a comparative evaluation of CCSAB and CCDAB with existing TCSAB and TCDAB is performed. The evaluation shows that capacitor coupled designs are quite suitable to replace the corresponding transformer coupled designs.

CHAPTER 5

# Fault Analysis and Grounding Strategies

Capacitively coupled converters do not provide galvanic isolation between the input and output stage which means that their behavior under fault conditions will be is substantially different from transformer coupled converters. The lack of galvanic isolation also affects the location and type of grounding that is suitable for these converters. Section I provides an overview of the various types of faults that can occur in such high voltage converters. The typical grounding configurations that can be used for detecting faults and minimizing the fault leakage current are presented in Section II. Section III analyzes the converter behavior during faults to estimate the magnitude and possible paths of fault current. Section IV-VI discuss a simulation study to model the behavior of the cascade capacitor coupled converter in bipolar configuration for terminal to ground faults.

## 5.1 Type of faults

All of the various capacitor coupled converters introduced in this work have a similar structure consisting of strings of capacitors forming a single phase or three phase AC distribution network. These coupling capacitors conduct AC current while simultaneously charged with

varying amplitude of DC bias voltage depending on their position in the AC network. This AC capacitor network is then connected to an equal number of single phase or three phase output stage rectifiers. Each output stage rectifier also includes a filter capacitor at the DC output. All these filter capacitors are connected in series which then forms a DC output network of capacitors with the same DC bias voltage across each capacitor. The rectifier network can consist of unidirectional diodes (CCSAB) or bidirectional switches (CCDAB). In this work we are chiefly concerned with faults that result in any voltage terminal of the converter being shorted to ground. The analysis on the remainder of this chapter will focus on this category of terminal to ground faults. Based on their location in this AC+DC network, we can categorize terminal faults as

**DC output array fault** This type of fault occurs when a terminal of one of the DC filter capacitor terminals is shorted to ground as shown in Fig 5.2.

**AC distribution array fault** This type of fault occurs on the coupling capacitors. This can be further classified as

- capacitor terminal to ground fault: one of the coupling capacitor terminals is shorted to ground as shown in Fig 5.1
- capacitor terminal to terminal fault: coupling capacitor terminal of one phase is shorted to capacitor terminal of a second phase

Electrical shock or injury is a physiological reaction to electric current passing through the human body [187, 188]. As shown in Table 5.1, relatively low amplitudes of current can have major effects on the body. The actual amount of current that can flow during an electric shock depends on the voltage, frequency, skin resistance and the point of entry and exit of current. With the AC current as specified by Table 5.1, the sensation of electric shock persists as long as the current is conducting. In contrast, with DC current the feeling of shock is felt only when the conduction path is made or broken [187]. From Table 5.1, it can observed that 5mA is the threshold that is most commonly used to indicate the presence of fault.

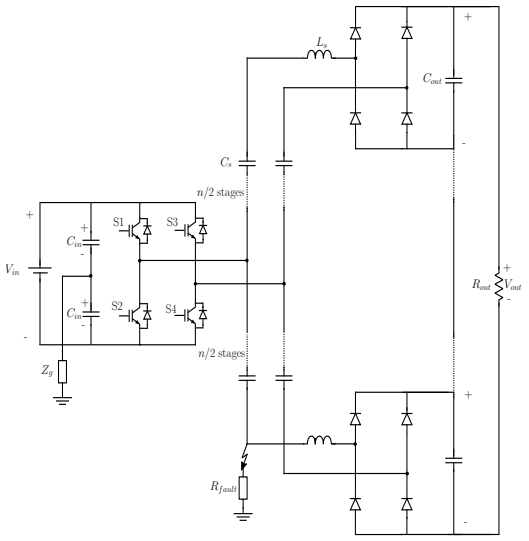


Figure 5.1: AC fault on single phase cascade coupled CCSAB with bipolar output configuration and input side midpoint grounding

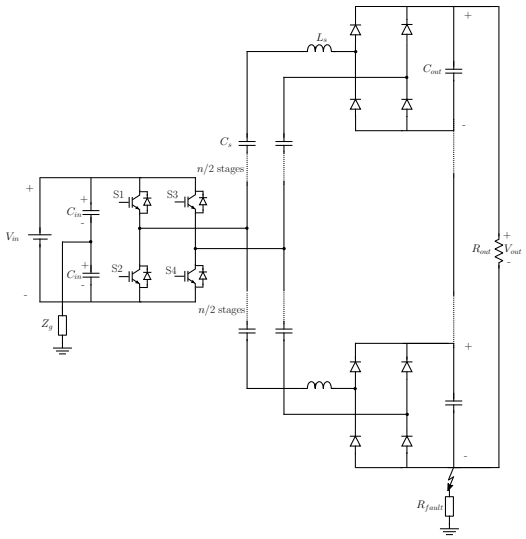


Figure 5.2: DC fault on single phase cascade coupled CCSAB with bipolar output configuration and input side midpoint grounding

Table 5.1: Estimated effect of 60Hz AC current [187, 189]

| Amplitude [mA] | Effect |
|---|---|
| 1 | Threshold of sensation |
| 5 | Ground Fault Current Interrupter trip level |
| 16 | Maximum current an average man can grasp and ‚Äúlet go‚Äù |
| 20 | Paralysis of respiratory muscles |
| 100 | Ventricular fibrillation threshold |
| 2000 | Cardiac standstill and internal organ damage |

## 5.2 Grounding configurations

Terminal or chassis grounding has three important functions - safety of the system operator, detecting fault condition and minimizing fault leakage current. In the commercial space standards like [184, 185] specify grounding and protection standards for low voltage (<1kV) electrical wiring in large installations like buildings. For example, the USA National Electric Code (NEC) [184] specifies that for two-wire dc systems operating between 50-300V one of the conductors must be grounded. For DC systems operating at higher voltages, a three-wire system must be used and the neutral conductor must be grounded. The IEEE 142 standard

[186] also provides a comprehensive overview of the recommended practices and grounding structures for electronic equipment. It should be noted that all of these standards are specified for AC systems and do not account for pure DC systems with no galvanic isolation.

In case of both single phase and three phase capacitively coupled converters the midpoint of the input voltage $V_{in}$ is selected as the grounding terminal. The output side is ungrounded even thought the output voltage has a natural midpoint in the bipolar configuration. By restricting the grounding connection to a single terminal on the converter input side, the fault can be detected on the low side and fault current minimized by appropriately sizing the ground impedance. There are four types of grounding that are usually recommended [186], solid grounding, resistance grounding, reactance grounding and impedance grounding.

In case of hybrid AC+DC systems such as the CCSAB and CCDAB, solid grounding is not suitable since the voltage before fault can often be purely DC. This means that in practice, the fault current will be limited solely by the resistance to ground at the point of fault. Pure reactance grounding can limit the instantaneous fault current however if the fault persists for longer than a few switching cycles, the current will once again be limited by the fault resistance only. Pure resistive grounding is compatible with this hybrid toplogy to limit both the instantaneous and steady state amplitude of fault current at the same time. But this type of grounding is not compatible with response characteristics of the ground fault detection and protection relays which depend on instantaneous current detection followed by delayed action of protection relays. Therefore, the most suitable grounding configuration for the CCSAB and CCDAB topology is the impedance type of grounding. In this case, the instantaneous current is limited by the inductive element while the fault current after a few switching cycles is limited by the resistive element.

Fig 5.3 shows the effect of changing the characteristics of the grounding impedance $Z_g$ on the fault current. As predicted, with solid grounding and inductance grounding the instantaneous fault current is limited only by the fault resistance $R_{fault}$. Resistance and impedance grounding show that fault current is now limited by the $R_g$. The difference between resistance and impedance grounding is the time delay in reaching the maximum fault current.

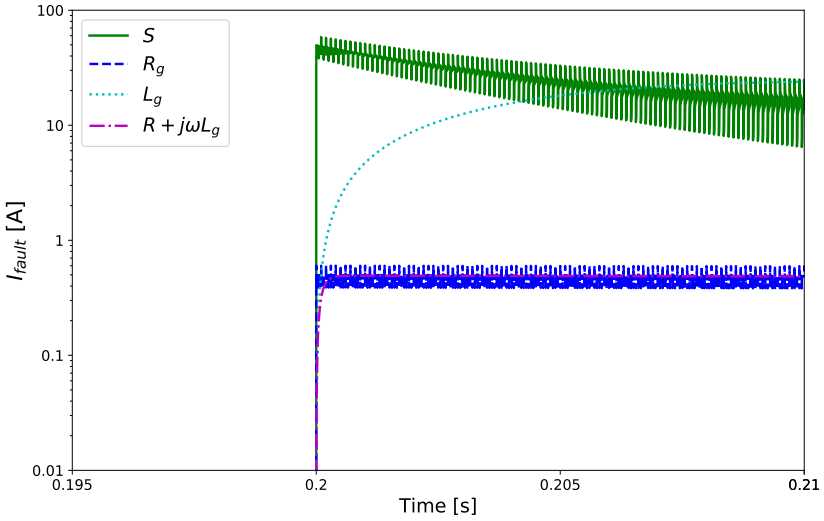


Figure 5.3: Current to ground at faulted terminal of a 10 stage cascaded CCSAB with bipolar configuration and input side midpoint grounding. Voltage before fault = 500V, fault resistance $R_{fault}$=10Ω. $R_g$=1kΩ, $L_g$=100mH

Table 5.2: Comparison of grounding configurations

| | Solid | Resistive R | Inductive L | Impedance RL |
|---|---|---|---|---|
| $Z_g$ | 0 | $R_g$ | $j\omega L_g$ | $R_g + j\omega L_g$ |
| max($I_{fault}$) limited by | $R_{fault}$ | $R_g$ | $R_{fault}$ | $R_g$ |
| rate of rise($I_{fault}$) limited by | undefined | undefined | $L_g$ | $L_g$ |

## 5.3 Equivalent circuit during fault

The capacitor coupled converter topology does not include galvanic isolation between the input stage and the numerous output stages. The net effect is that during fault conditions a continuous conduction path exists from the DC source to the fault terminal. A single output stage equivalent circuit of the single phase cascade coupled CCSAB topology is shown in Fig 5.4.

The DC current that conducts during fault can be estimated from the ground referenced equivalent circuit as shown in Fig 5.5. From the figure, the DC component of the fault current

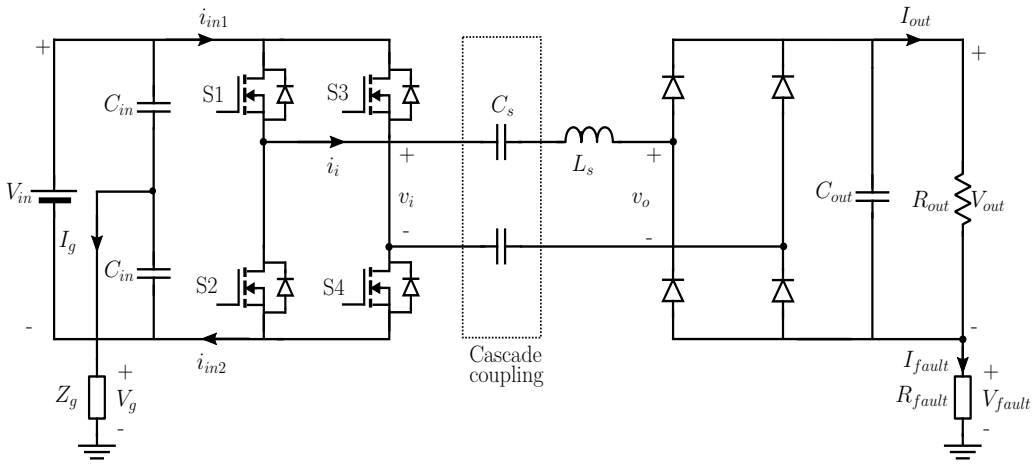


Figure 5.4: Equivalent circuit of cascade coupled CCSAB showing output stage with fault on DC output terminal

$i_{fault}$ is termed as $I_{fdc}$ and can be estimated as

$$V_{fdc} = \frac{V_{in} + nV_{outn}}{2} \tag{5.1}$$

$$I_{fdc} = \frac{V_{fdc}}{(R_g + R_{fault})} \tag{5.2}$$

$$I_{fdc} \simeq \frac{nV_{out}}{2(R_g + R_{fault})} \quad V_{out} \gg V_{in} \tag{5.3}$$

where $n$ refers to the number of stages between the fault and the input stage. The The $n$ refers

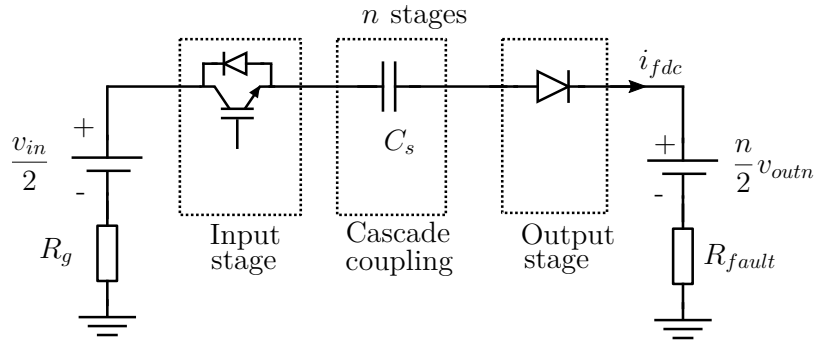


Figure 5.5: Ground referenced fault equivalent circuit for bipolar output configuration with midpoint grounding on the input DC bus.

to the number of output stages between the input stage and the fault terminal at the output.

This equivalent circuit is valid for bipolar output configuration with midpoint grounding on

the input side. In case of unipolar output configuration with grounding on the source return, $0.5nV_{outn}$ is replaced by $nV_{outn}$ and $0.5V_{in}$ by $V_{in}$.

In fault conditions, the converter is supplying power to the fault $R_g + R_{fault}$ in addition to the nominal load $R_{load}$. This additional power is reflected in the increased RMS current in the input stage inverter AC current as well as an imbalance in the net AVG current in the source. The additional power can be estimated from the fault power balance equivalent circuit as shown in Fig 5.6. From the figure, the electrical terms on the source side and fault side

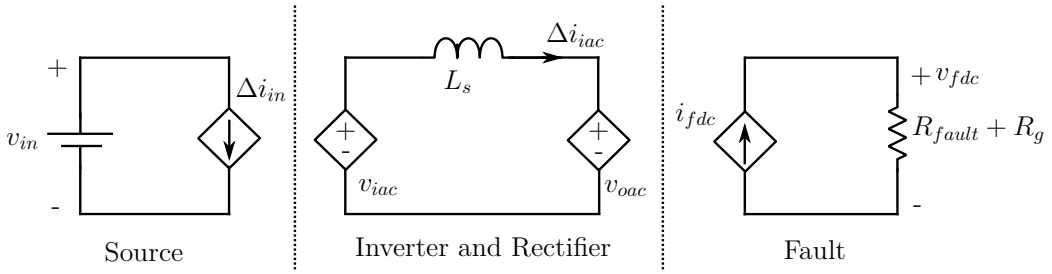


Figure 5.6: Fault power balance equivalent circuit

are AVG (pure DC) quantities while the quantities on the inverter and rectifier side are RMS (pure AC) quantities. The source current $\Delta i_{in}$ refers to the imbalance in the current sourcing and sinking into the DC source because of the ground fault. $i_{in1}$ is the current sourcing from the DC input source $v_{in}$ and $i_{in2}$ is the current sinking into the DC input source as shown in Fig 5.4. In nominal conditions $i_{in1} = i_{in2}$ (pre-fault). However, during fault conditions with mid-point grounding on the input side, these currents will be unequal (post-fault), the quantum of inequality dependent on the location and polarity of fault terminal with respect to the ground.

$$\Delta i_{in} = \max(i_{in1}, i_{in2})|_{post} - \max(i_{in1}, i_{in2})|_{pre} \tag{5.4}$$

$i_{iac}$ is the RMS of AC component of the inverter output current $i_i$ and $\Delta i_{iac}$ refers to the increase in RMS current due to fault power. The power balance equations are

$$P_{fault} = i_{fdc}^2 (R_{fault} + R_g) \tag{5.5}$$

This excess fault power is balanced on the single phase inverter side by

$$P_{fault} = v_{iac}\Delta i_{iac} \tag{5.6}$$

and in the case of the three phase inverter by

$$P_{fault} = \sqrt{3}v_{iLLac}\Delta i_{iac} \tag{5.7}$$

This is then reflected on the source side as

$$P_{fault} = v_{in}\Delta i_{in} \tag{5.8}$$

## 5.4 Converter specifications for fault analysis

The effect of the terminal to ground faults is studied with the help of a prototype 1kV, 1kW capacitive DC-DC converter. The input stage configuration of this converter can be either single phase full bridge converter switching at frequency $F_s$ or a three phase two level inverter operating on six-step modulation at 50% duty cycle at the same frequency. The output stage configuration also can be either single phase or three phase. The coupling capacitors are arranged in cascade configuration to the input stage. The chief benefit of cascade configuration is in the lower voltage rating on the coupling capacitors which will reduce component cost and improve reliability of the overall converter. The output stages are arranged in bipolar configuration which will reduce the maximum terminal to ground voltage of the converter to $V_{out}$/2 while still supplying $V_{out}$ to the load. The converter specifications are detailed in Table 5.3.

## 5.5 DC output array faults

As the capacitor coupled toplogy is a modular structure with voltages added by successive stages, the magnitude of fault current depends on the location of the fault. In this section, the fault location is assumed to be in the output stage with the most negative output terminal with respect to ground. The behavior of the DC-DC converter for single phase and three phase

Table 5.3: Table of parameters

| Parameter | Unit | Value |
|---|---|---|
| $V_{in}$ | V (AVG) | 110 |
| $V_{out}$ | kV AVG) | 1 |
| $R_{out}$ | kΩ | 1 |
| $P_{out}$ | kW | 1 |
| $F_s$ | kHz | 10 |
| $C_{in}$ | $\mu$F | 1000 |
| $C_s$ | $\mu$F | 1000 |
| $L_s$ | $\mu$H | 100 |
| $C_{out}$ | $\mu$F | 1000 |
| $R_g$ | kΩ | 1 |
| $L_g$ | mH | 1 |

variants are studied in this section. In order to exaggerate the effect of the fault condition, the grounding impedance is set so that the DC component of the fault current $I_{fdc}$ is about 0.5 A.

### 5.5.1 Single phase CCSAB

A single phase cascade CCSAB converter with 10 output stages in bipolar configuration is shown in Fig 5.7 with a terminal fault on the negative terminal (with respect to ground) of the output voltage $V_{out}$. The DC bus of the input stage $V_{in}$ is split and the midpoint is grounded with impedance $Z_g$=$R_g + j\omega_s L_g$

As shown in Fig 5.8, the DC fault on the output stage fault does not have an instantaneous effect on the input stage inverter current or the overall DC output voltage. In Fig 5.9 it can be observed that the average fault current is approximately 0.5 A for DC fault terminal voltage of 500 V. Since the converter is grounded at a single point on the input side, the grounding impedance current is same as fault current.

In Fig 5.10 the effect of the sustained fault on the DC bias voltages of the coupling capacitors and the output stages can be observed. The coupling capacitors $C_{s5}$ and $C_{s6}$ are directly coupled to the input stage and consequently have half the DC bias voltage as the remaining stages. After fault, these coupling capacitor voltages diverge as one of the capacitors is charged while the other is discharged. At every instant, $V_{cs5} + V_{cs6} = V_{in}$. There is no effect of the fault on the individual filter capacitor voltage of every stage. In Fig 5.11, the DC and AC

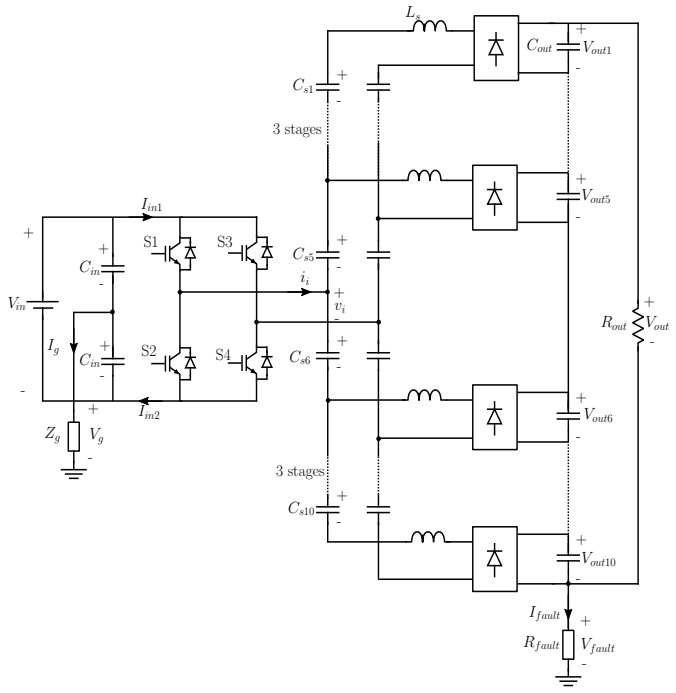


Figure 5.7: Single phase cascade coupled CCSAB converter with fault on DC output terminal.

components of the inverter current $i_i$ is shown to illustrate the effect of fault. The DC current on the input stage $i_{in}$ is split as $i_{in1}$ and $i_{in2}$ which are normally equal and opposite in sign to each other. But during fault condition, $i_{in1} - i_{in2} = i_{fdc}$. The difference in these currents can be accounted by the DC component of fault current.

### 5.5.2 Single phase CCDAB

A single phase cascade CCDAB converter with 10 output stages in bipolar configuration is shown in Fig 5.12. The converter is operated with phase shift control between the input stage the output stages. All the output stages are slaved to a single controller to achieve a regulated output of 1 kV at 1 kΩ. A terminal fault on the negative terminal (with respect to ground) of the output voltage is created at $t$=3.2s. The DC bus of the input stage $V_{in}$ is split and the midpoint is grounded with impedance $Z_g$=$R_g + j\omega_s L_g$.

The inverter current $i_i$ is continuous with the amplitude determined by the phase shift between the input stage and all the output stages as shown in Fig5.13. Similar to the case

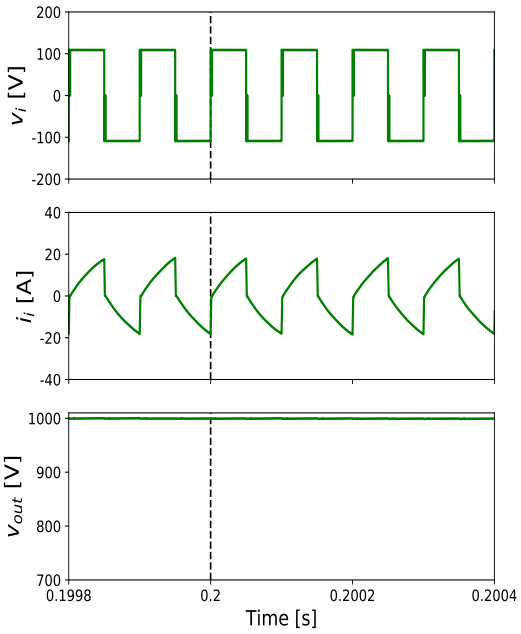


Figure 5.8: Single phase CCSAB DC fault configuration.Top: Input stage AC voltage $v_i$, Middle: Input stage AC current $i_i$, Bottom: Output voltage $V_{out}$.

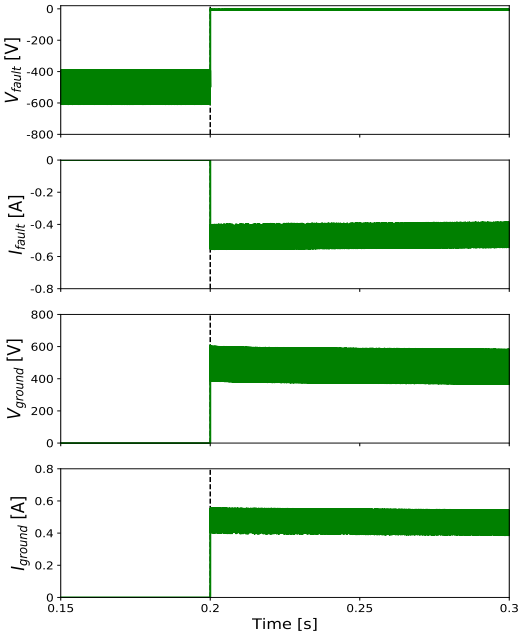


Figure 5.9: Single phase CCSAB DC fault configuration. First: Voltage to ground at fault terminal, Second: Current to ground at fault terminal. Third: Voltage to ground at grounding impedance, Fourth: Current to ground at grounding impedance.

of the single phase CCSAB, there is no intantaneous effect of the DC terminal fault on the inverter output waveforms. The fault resistance $R_{fault}$ and the grounding impedance are adjusted such that the fault current is limited to 0.5 A on a 1 kV output voltage.

As shown in Fig 5.15, even with closed loop control, the effect of a DC terminal fault is to reduce the output voltage. The coupling capacitor DC bias voltages $V_{cs5}$ and $V_{cs6}$ once again diverge from the nominal ratings. The converter behavior on the input side is also very similar to the CCSAB case where $i_{in1} \neq i_{in2}$ and the net power increase due to fault current is distributed in the DC and AC component of inverter current. The DC component of the fault current $i_{fdc}$ is once again limited by the resistance $R_g$ in the fault current path.

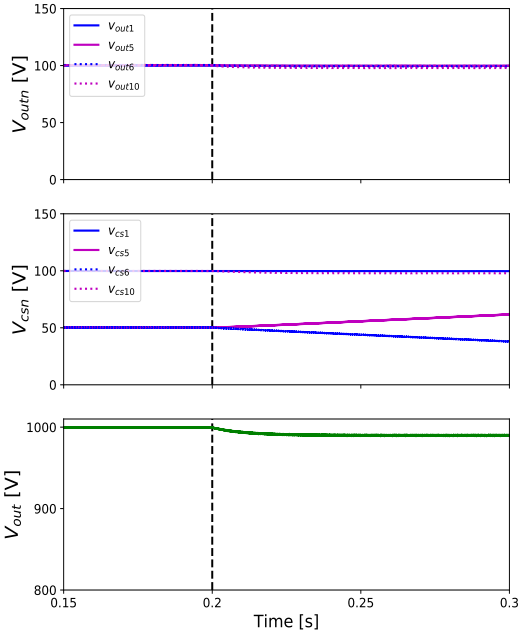


Figure 5.10: Single phase CCSAB DC fault configuration. Top: Voltage across filter capacitors (stages 1,5,6,10), Middle: Voltage across coupling capacitors (stages 1,5,6,10), Bottom: Output voltage $V_{out}$

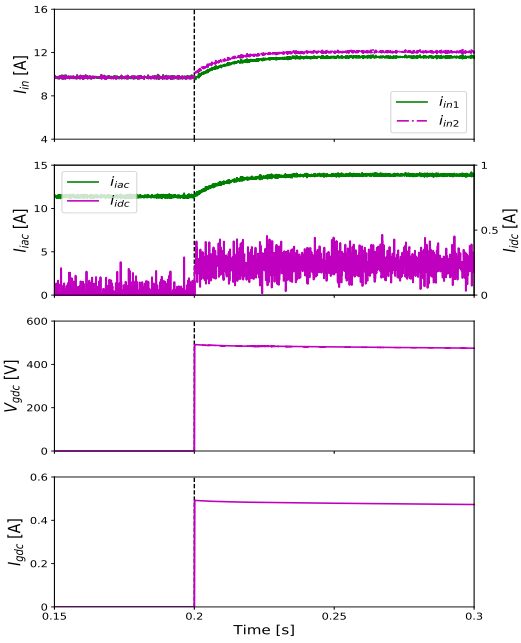


Figure 5.11: Single phase CCSAB DC fault configuration. First: Current in input side DC bus $I_{in1}, I_{in2}$, Second: Fundamental component and DC component of input stage AC current $i_i$, Third: DC component of voltage to ground at grounding impedance $V_{gdc}$, Fourth: DC component of current to ground at grounding impedance $I_{gdc}$

### 5.5.3 Three phase CCSAB

A three phase cascade CCSAB converter with 10 output stages in bipolar configuration is shown in Fig 5.17 with a terminal fault on the negative terminal (with respect to ground) of the output voltage $V_{out}$. As before, the three phase two level inverter is operating in open loop six step switching sequence. The DC bus of the input stage $V_{in}$ is split and the midpoint is grounded with impedance $Z_g$=$R_g + j\omega_s L_g$

As before, the DC fault on the output terminal does not affect the instantaneous line-to-line AC voltage or AC line current of the three phase inverter as shown by Fig 5.18. In Fig 5.19, it can be observed that the AC component of the fault current is reduced by about 50% compared

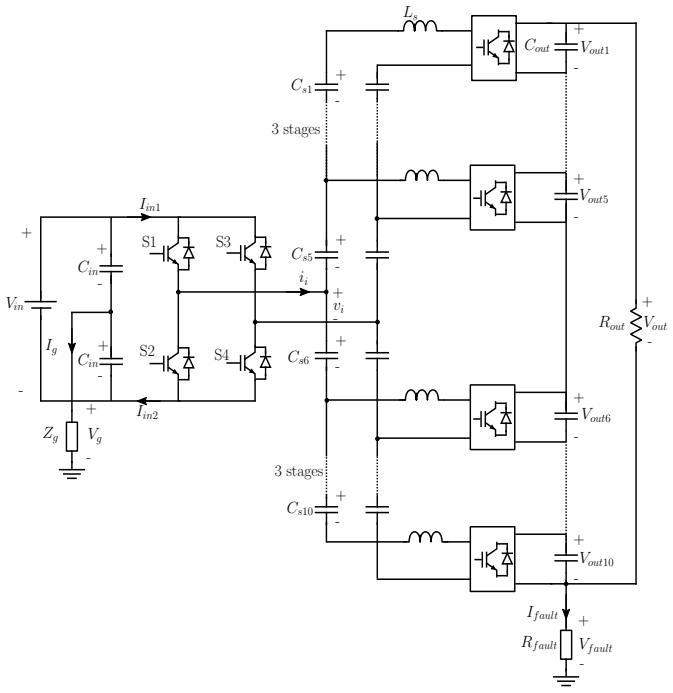


Figure 5.12: Single phase cascade coupled CCDAB converter operating in closed loop with fault on DC output terminal.

to the single phase CCSAB.

The effect of the DC output terminal fault on the series coupling capacitor voltages is similar to earlier cases as shown by Fig 5.20. As in earlier cases, the extra fault current shows up as additional DC and AC component current in the three phase inverter as well as a current imbalance on the DC input side.

## 5.6 AC distribution array faults

In this section, the fault location is assumed to be in the series cascade capacitor terminal of the 9th stage with respect to ground. The behavior of the DC-DC converter for single phase and three phase variants are studied in this section. In order to exaggerate the effect of the fault condition, the grounding impedance is set so that the DC component of the fault current $I_{fdc}$ is about 0.5 A.

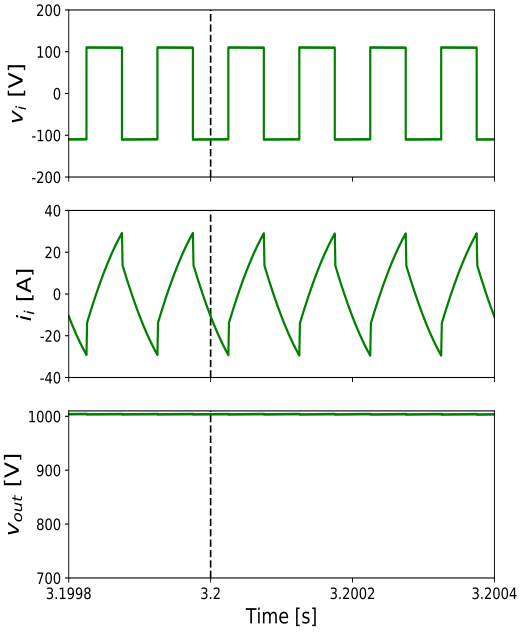


Figure 5.13: Single phase CCDAB DC fault configuration. Top: Input stage AC voltage $v_i$, Middle: Input stage AC current $i_i$, Bottom: Output voltage $V_{out}$.

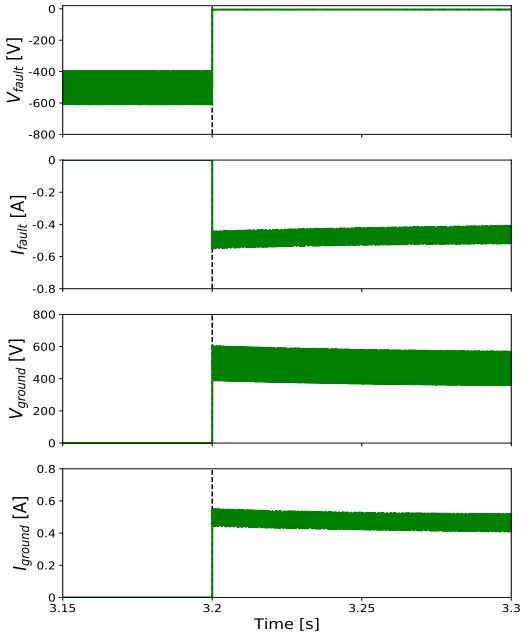


Figure 5.14: Single phase CCDAB DC fault configuration. First: Voltage to ground at fault terminal, Second: Current to ground at fault terminal. Third: Voltage to ground at grounding impedance, Fourth: Current to ground at grounding impedance

### 5.6.1 Single phase CCSAB

A single phase cascade CCSAB converter with 10 output stages in bipolar configuration is shown in Fig 5.22 with a terminal fault in a cascade coupling capacitor terminal to ground. In terms of fault behavior AC cascade terminal to ground faults are very similar to DC filter capacitor terminal to ground faults. The maximum fault current at any AC terminal will depend on the position of the output stage relative to input stage just as in the case of the DC fault.

The coupling capacitor voltage is at the fault terminal less than $0.5V_{out}$. This in turn affects the magnitude of fault current as can be seen from Fig 5.24.

The effect of the AC cascade terminal fault on the series coupling capacitor voltages is similar to earlier cases as shown by Fig 5.10.

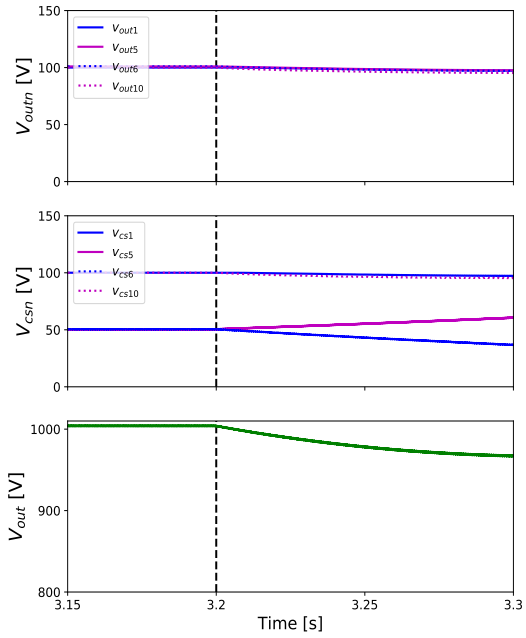


Figure 5.15: Single phase CCDAB DC fault configuration. Top: Voltage across filter capacitors (stages 1,5,6,10), Middle: Voltage across coupling capacitors (stages 1,5,6,10), Bottom: Output voltage $V_{out}$

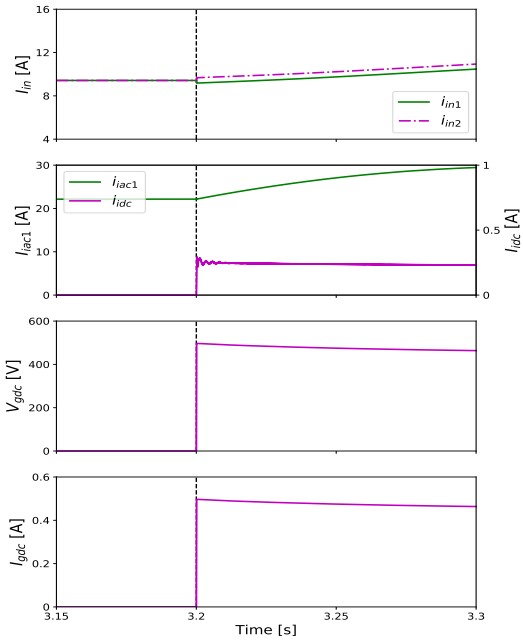


Figure 5.16: Single phase CCDAB DC fault configuration. First: Current in input side DC bus $I_{in1}$,$I_{in2}$, Second: Fundamental component and DC component of input stage AC current $i_i$, Third: DC component of voltage to ground at grounding impedance $V_{gdc}$, Fourth: DC component of current to ground at grounding impedance $I_{gdc}$

### 5.6.2 Three phase CCSAB

A three phase cascade CCSAB converter with 10 output stages in bipolar configuration is shown in Fig 5.17 with a terminal fault the A-phase cascade coupling capacitor terminal to ground. As before the maximum fault current at any AC terminal will depend on the position of the output stage relative to input stage.

Since the coupling capacitor is closer to the input stage, the voltage to ground at the coupling capacitor terminal is less than $0.5V_{out}$. This in turn affects the magnitude of fault current as can be seen from Fig 5.29.

The effect of the AC cascade terminal fault on the series coupling capacitor voltages is

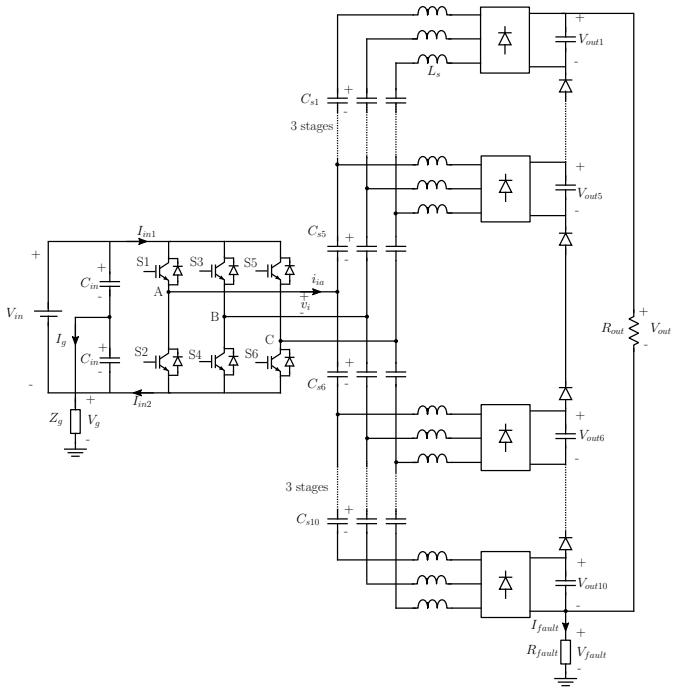


Figure 5.17: Three phase cascade coupled CCSAB converter with fault on DC output terminal.

similar to earlier cases as shown by Fig 5.20. However, as before the magnitude of fault current affects the deviation of coupling capacitor voltages from the nominal condition. If the DC current can be restricted to less than 5 mA, there is very little effect on the coupling capacitor voltages or output voltage.

## 5.7 Summary

The main objective of this chapter is to model the behavior of the non-isolated capacitor coupled converter topology during high voltage terminal to ground faults. High voltage terminal to ground short are the type of faults that are studied in details. The capacitor coupled topology is a modular and non-isolated topology where the fault current path dependent on the location of the fault terminal from the input stage. An equivalent circuit that models the behavior of the converter during fault conditions is proposed. A simulation study of the various fault configurations confirms the analytical fault model.

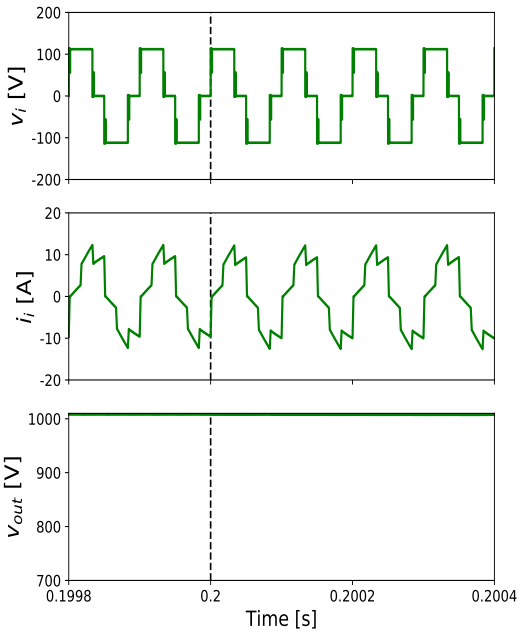


Figure 5.18: Three phase CCSAB DC fault configuration. Top: Input stage line-to-line AC voltage $v_{iab}$, Middle: Input stage AC line current $i_{ia}$, Bottom: Output voltage $V_{out}$.

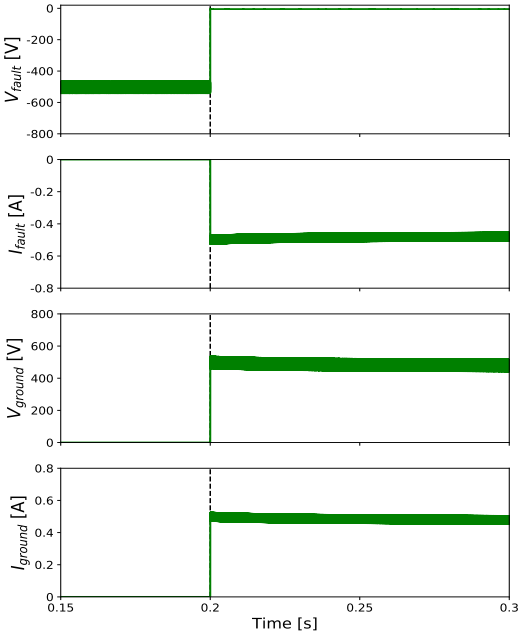


Figure 5.19: Three phase CCSAB DC fault configuration. First: Voltage to ground at fault terminal, Second: Current to ground at fault terminal. Third: Voltage to ground at grounding impedance, Fourth: Current to ground at grounding impedance

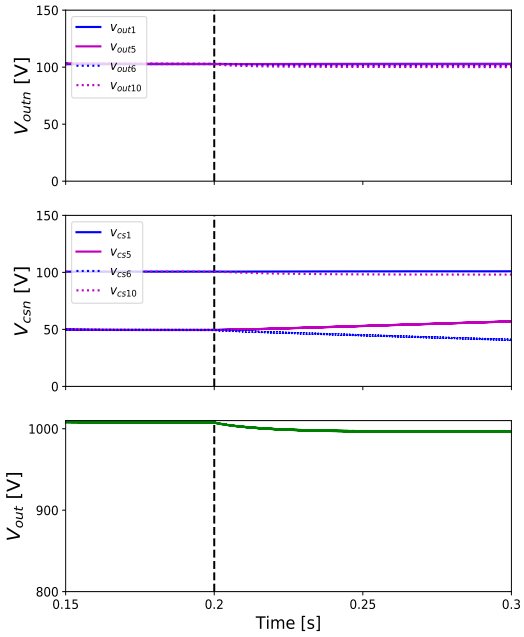


Figure 5.20: Three phase CCSAB DC fault configuration. Top: Voltage across filter capacitors (stages 1,5,6,10), Middle: Voltage across coupling capacitors (stages 1,5,6,10), Bottom: Output voltage $V_{out}$

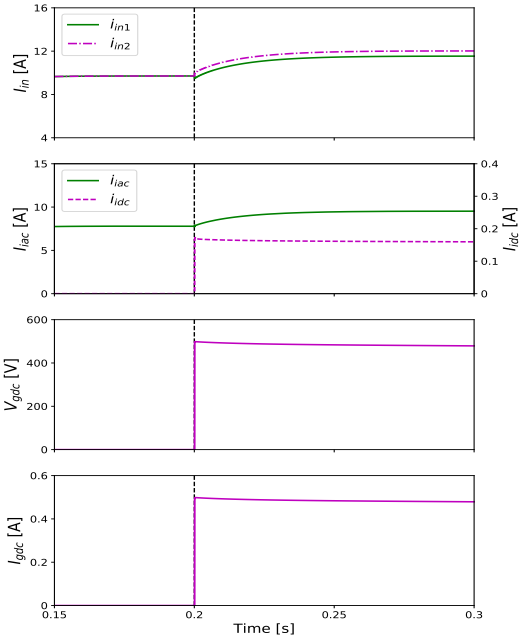


Figure 5.21: Three phase CCSAB DC fault configuration. First: Current in input side DC bus $I_{in1}, I_{in2}$, Second: Fundamental component and DC component of input stage AC current $i_i$, Third: DC component of voltage to ground at grounding impedance $V_{gdc}$, Fourth: DC component of current to ground at grounding impedance $I_{gdc}$

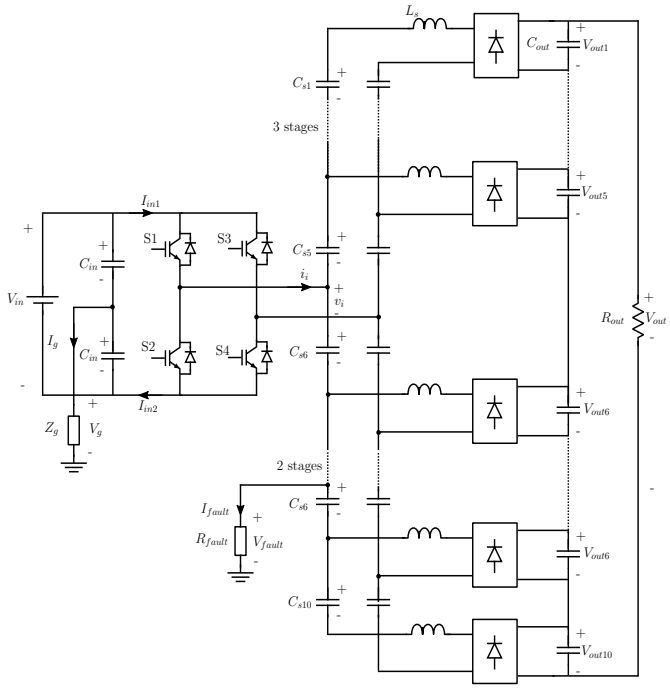


Figure 5.22: Single phase cascade coupled CCSAB converter with fault on AC output terminal.

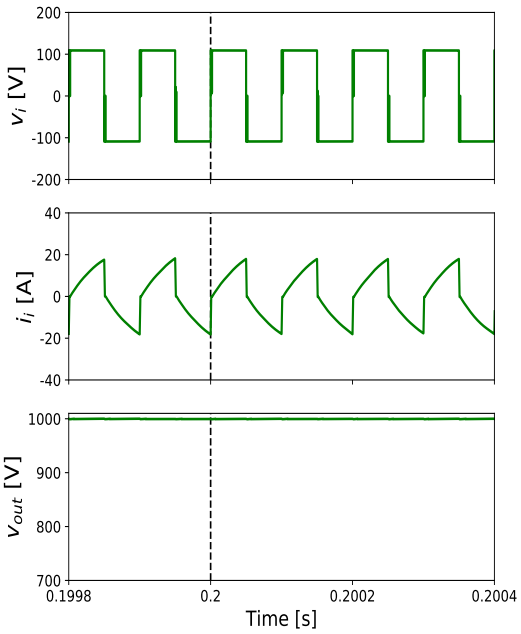


Figure 5.23: Single phase CCSAB AC fault configuration. Top: Input stage AC voltage $v_i$, Middle: Input stage AC current $i_i$, Bottom: Output voltage $V_{out}$.

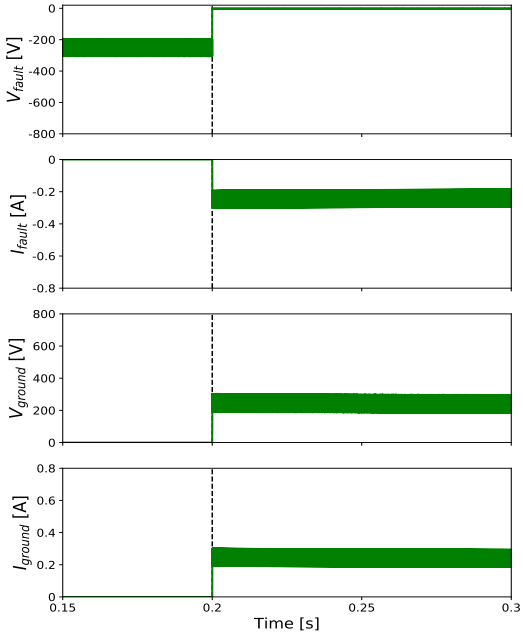


Figure 5.24: Single phase CCSAB AC fault configuration. First: Voltage to ground at fault terminal, Second: Current to ground at fault terminal. Third: Voltage to ground at grounding impedance, Fourth: Current to ground at grounding impedance

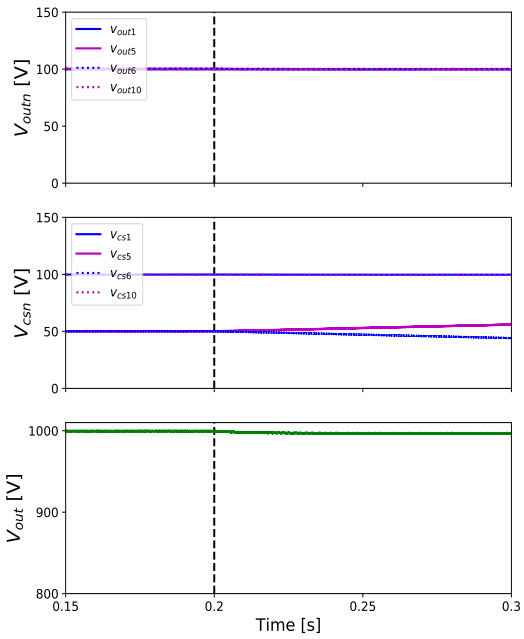


Figure 5.25: Single phase CCSAB AC fault configuration. Top: Voltage across filter capacitors (stages 1,5,6,10), Middle: Voltage across coupling capacitors (stages 1,5,6,10), Bottom: Output voltage $V_{out}$

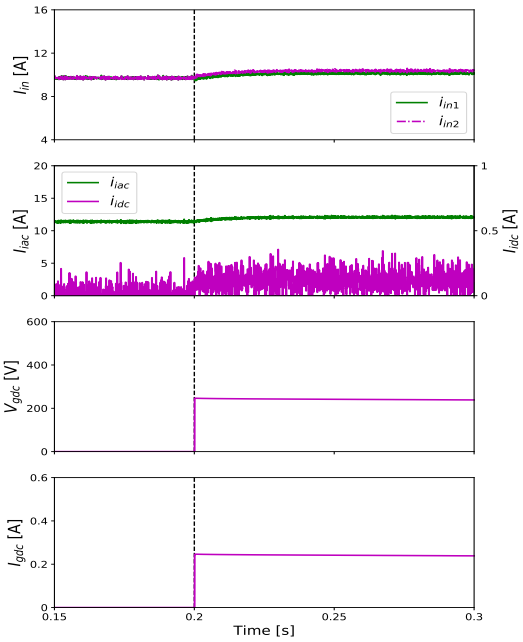


Figure 5.26: Single phase CCSAB AC fault configuration. First: Current in input side DC bus $I_{in1}, I_{in2}$, Second: Fundamental component and DC component of input stage AC current $i_i$, Third: DC component of voltage to ground at grounding impedance $V_{gdc}$, Fourth: DC component of current to ground at grounding impedance $I_{gdc}$

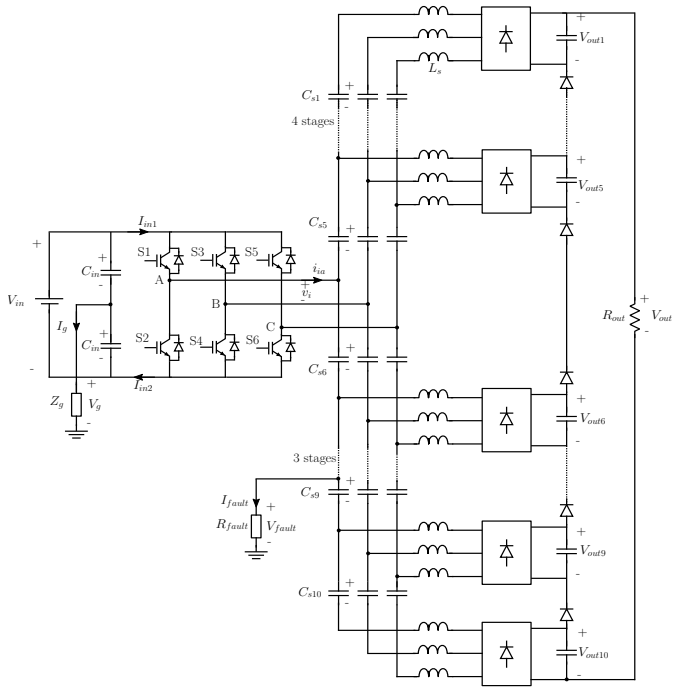


Figure 5.27: Three phase cascade coupled CCSAB converter with fault on AC cascade terminal.

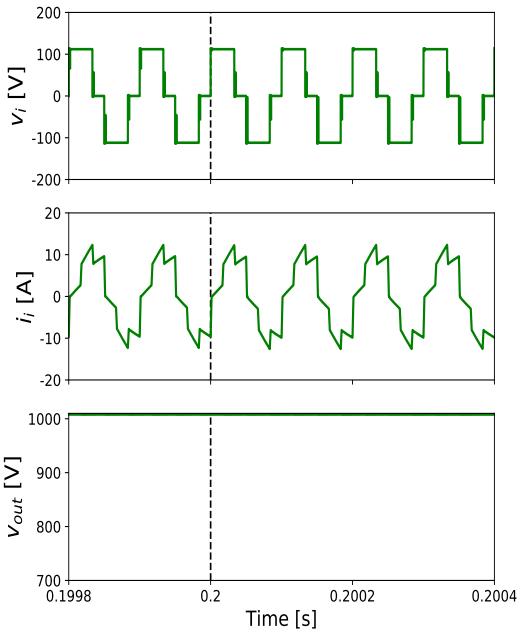


Figure 5.28: Three phase CCSAB AC fault configuration. Top: Input stage line-to-line AC voltage $v_{iab}$, Middle: Input stage AC line current $i_{ia}$, Bottom: Output voltage $V_{out}$.

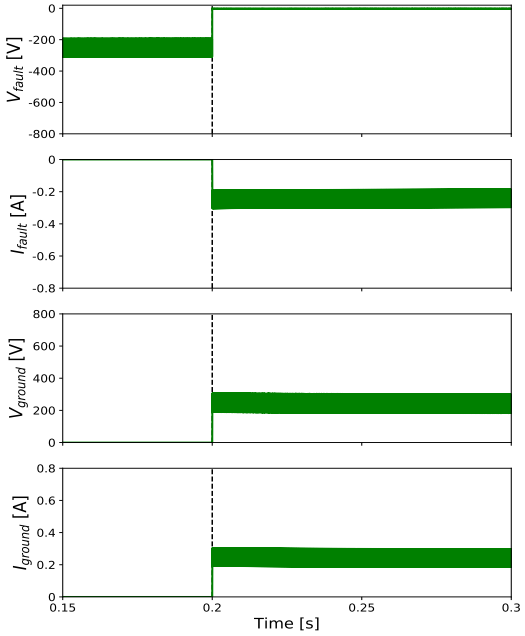


Figure 5.29: Three phase CCSAB AC fault configuration. First: Voltage to ground at fault terminal, Second: Current to ground at fault terminal. Third: Voltage to ground at grounding impedance, Fourth: Current to ground at grounding impedance

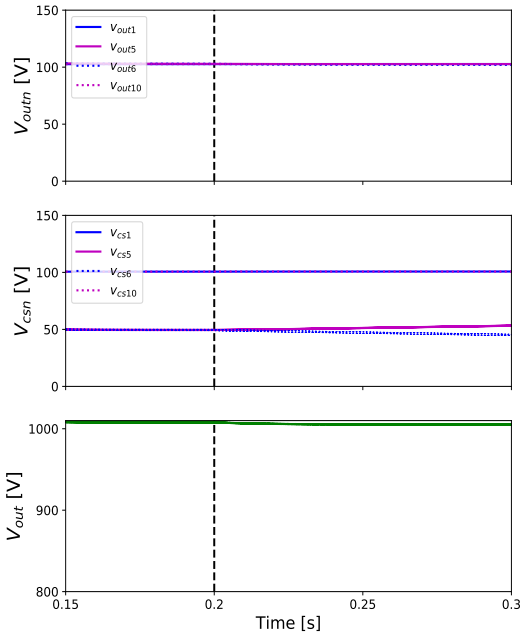


Figure 5.30: Three phase CCSAB AC fault configuration. Top: Voltage across filter capacitors (stages 1,5,6,10), Middle: Voltage across coupling capacitors (stages 1,5,6,10), Bottom: Output voltage $V_{out}$

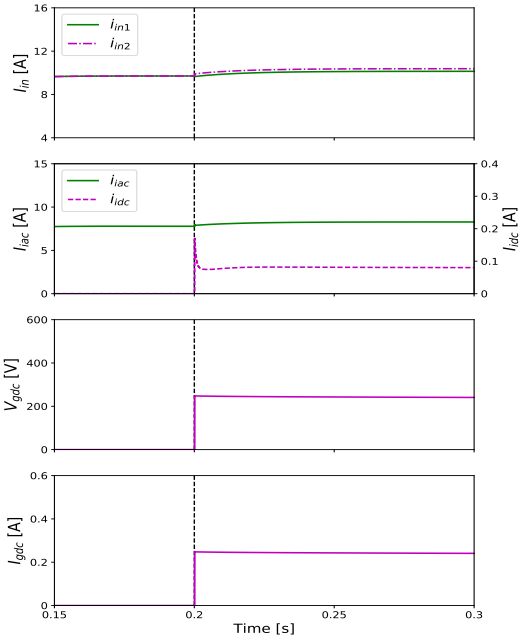


Figure 5.31: Three phase CCSAB AC fault configuration. First: Current in input side DC bus $I_{in1}, I_{in2}$, Second: Fundamental component and DC component of input stage AC current $i_i$, Third: DC component of voltage to ground at grounding impedance $V_{gdc}$, Fourth: DC component of current to ground at grounding impedance $I_{gdc}$

CHAPTER 6

# Application Case Studies

The previous chapters introduced the capacitor coupled DC-DC converter topology and discussed the analytical model and design aspects of this new topology. This chapter verifies the analytical and simulation model introduced in earlier chapters and records the experimental performance measures of this topology. The first prototype to be introduced is a single phase CCSAB design which mainly serves to verify the initial analytical approach. This is then followed by a three phase CCSAB design that verifes the operation of at higher voltage and higher power. The converter design process is introduced along with detailed hardware specifications and designed parameters.

## 6.1 Single phase CCSAB converter

A laboratory scale prototype power converter was constructed to verify the design equations of the proposed CCSAB topology. The parameters of the prototype power converter are presented in Table 6.1. Extensive and detailed circuit simulations and hardware testing have been completed on the prototype power converter.

### 6.1.1 Converter architecture

The converter architecture is is based on the parallel coupled single phase CCSAB. The DC source $V_{in}$ feeds a high frequency full bridge inverter formed by the MOSFETs S1-S4. The ac output $v_i$ of the high frequency MOSFET based inverter is applied to two parallel stages of of high frequency schottky diode full bridge rectifiers, each with a series inductance $L_s$. Low voltage rated metal film capacitors are used as the series coupling capacitors$C_s$. The output voltage of each of the full bridge rectifiers is maintained stiff using an electrolytic capacitor $C_{out}$. The output load $R_{out}$ is applied across the series connection of $V_{out1} + V_{out2}$.

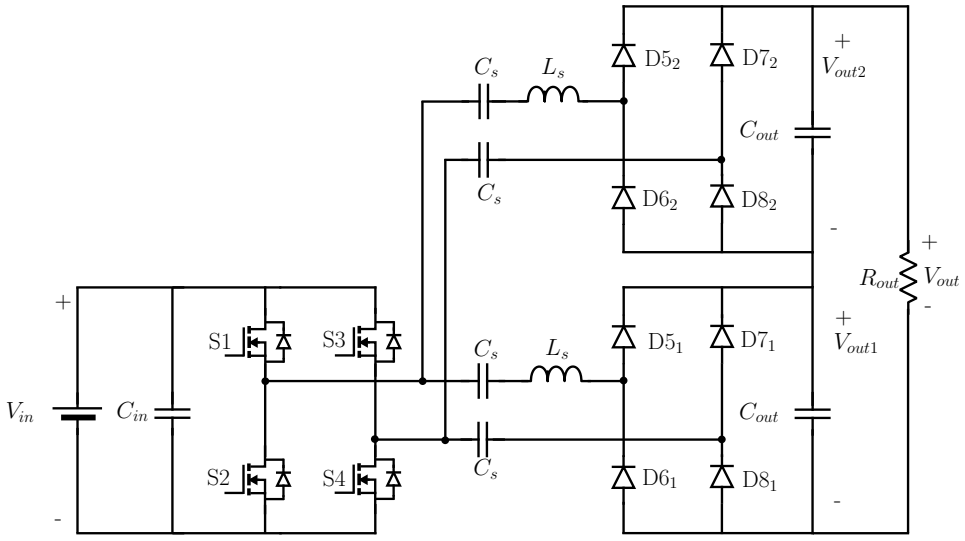


Figure 6.1: Power circuit schematic of series coupled single phase 2 stage capacitor coupled DC-DC converter

### 6.1.2 Hardware specifications

The high level specifications of the prototype power supply are shown in Table 6.1. The designed component values of the prototype power supply are shown in Table 6.2.

### 6.1.3 Simulation and experimental results

The prototype converter was built using discrete components mounted on printed circuit board assemblies. Selected experimental waveforms from the converter operation at no-load,

Table 6.1: Hardware specifications for single phase parallel coupled CCSAB converter

| Parameter | Units | Input | Output |
|---|---|---|---|
| Voltage | V | 12 | 22 |
| Current | A | 1.25 | 0.68 |
| Power | W | 15 | |
| Number of stages | $n$ | 1 | 2 |
| Voltage per stage | V-AVG | - | 11 |
| Current per stage | A-AVG | - | 0.68 |
| Power per stage | W | - | 7.5 |
| Switching freq | kHz | 125 | |

Table 6.2: Component details of the 2-stage prototype power converter

| Component | Unit | Value | Description | Qty/$n$ | Total |
|---|---|---|---|---|---|
| **Input stage** | | | | | |
| $C_{in}$ | $\mu$F | 100 | CAP ALUM 100UF 20% 35V SMD | 1 | 1 |
| MOSFET | S1-S4 | FDP8860 | MOSFET N-CH 30V 80A TO-220AB | 4 | 4 |
| **Output stage** | | | | | |
| $C_s$ | $\mu$F | 30 | CAP CER 33UF 35V C0G SMD | 2 | 4 |
| $L_s$ | $\mu$H | 2 | FIXED IND 2UH 1.1A 95 MOHM SMD | 1 | 2 |
| $C_{out}$ | $\mu$F | 1 | CAP CER 1UF 35V C0G 2012 | 1 | 2 |
| DIODE | D5-D8 | UF5404 | DIODE GEN PURP 400V 3A DO201AD | 4 | 8 |

part-load and full-load are presented in Fig 6.2 through Fig 6.4. The load regulation of the output voltage is shown in Fig 6.5. The experimental results indicate excellent conformance to the operational principles of the proposed converter.


Figure 6.2: Waveforms from the experimental two stage capacitively coupled converter $V_{out} = 23.96$ V, $I_{out} = 0$ A

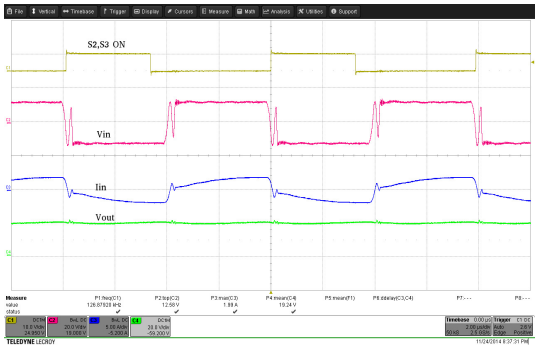


Figure 6.3: Waveforms from the experimental two stage capacitively coupled converter $V_{out} = 18.79$ V, $I_{out} = 0.5$ A

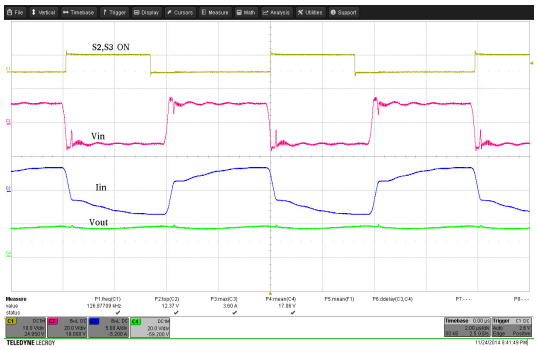


Figure 6.4: Waveforms from the experimental two stage capacitively coupled converter $V_{out}$ = 16.61 V, $I_{out}$ = 1 A

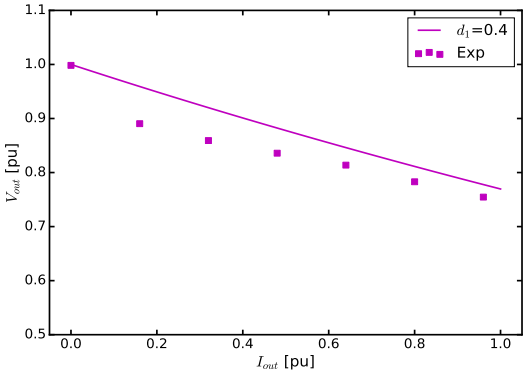


Figure 6.5: A plot of load regulation of the experimental prototype converter at constant duty cycle vs analytical estimation

## 6.2 Three phase CCSAB converter

High voltage DC power supplies up to several kW have been traditionally used in a variety of niche applications- insulation testing, plasma research, particle accelerators, electrostatic dust precipitators and microwave radar. A popular approach to produce HVDC is to rectify line-frequency AC voltage and simultaneously boost the resulting DC voltage by using the capacitor diode combination of Cockcroft Walton (CW) ladder type voltage multiplier [191]. This is a simple rugged structure design with no costly magnetic transformer coupling for voltage gain. However the series structure of the voltage multiplier limits the bandwidth for sensitive load applications [192]. The line regulation is also quite poor since the impedance of the capacitors in the input stages affect the final output voltage. There have been some improvements to this basic structure like [193] which showed that output load regulation was substantially improved by adding additional coupling capacitors in each stage the CW ladder network.

There is renewed interest lately in multi-kW HVDC driven by a new category of electric machines called the electrostatic machine [190]. In an electrostatic machine torque is produced by applying a high voltage between the stator and rotor surfaces. This application requires a new class of high voltage DC DC converters. The modular three phase capacitor coupled

high voltage converter topology introduced in an earlier chapter can provide a modular robust architecture for these loads. A high voltage DC power supply is designed for an electrostatic machine. The machine requirements are an output voltage of 6 kV at an average current of 1A. The converter is designed to be powered from a 230 V 60 Hz AC supply.

### 6.2.1 Converter architecture

The converter architecture is shown in Fig 6.6. The three phase 230V 60Hz AC utility supply is connected to a standard low frequency three phase diode bridge rectifier. A three phase autotransformer is used to adjust the amplitude of the line-to-line voltage applied to bridge rectifier, therby giving control over the final rectified DC bus voltage $V_{in}$. The 60Hz rectified voltage is filtered using line capacitance $C_{in}$. This DC bus voltage acts as the source for a high frequency two level IGBT based three phase inverter (HFI). The HFI is the input stage of the subsequent three phase cascade coupled CCSAB converter.

The output of the inverter feeds a string of 20 series connected three phase capacitor banks with per phase capacitance $C_s$, each of which provide a set of floating three phase voltages. The coupling capacitors are selected to have negligible reactance at the operating frequency of the inverter. Each of floating three phase voltages are connected to independent passive high frequency three phase rectifier bridges (CCR). Each rectifier bridge has a line inductance $L_s$ at each phase input. The DC output voltage of each of the rectifiers are floating from each other, and hence can be connected in series to develop a higher net voltage DC output. Series decoupling diodes $D_{rb}$ are used to connect the DC voltages is series to ensure that the conduction paths of each of the rectifiers do not interfere with each other. The function of this linking diode is to decouple the steady-state behavior of the output stages so that all output stage capacitors $C_{out1}, C_{out2}$... etc. charge and discharge depending only on the input voltage and independent from the neighboring output stages.

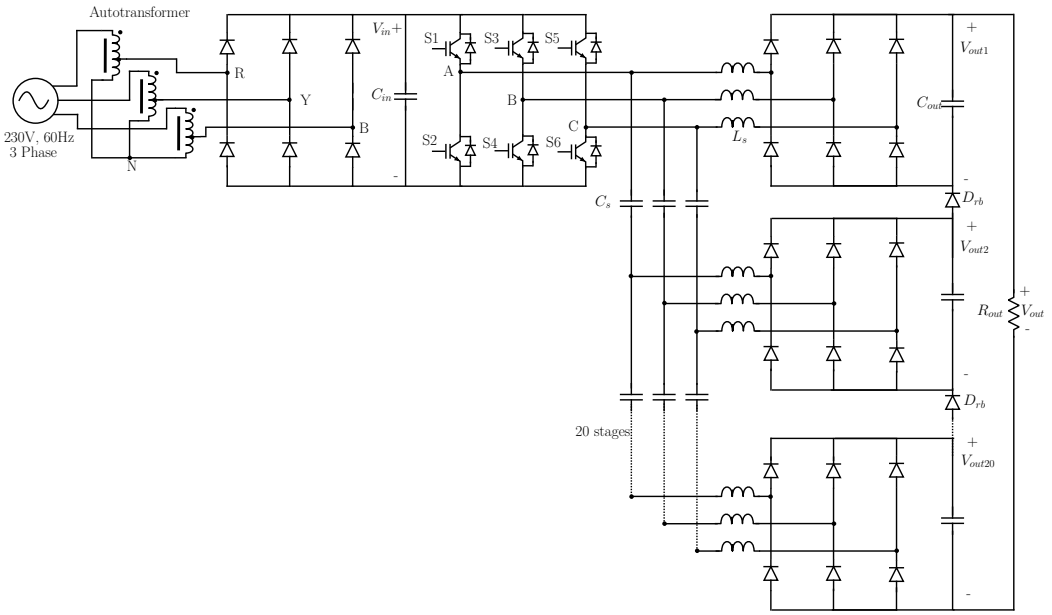


Figure 6.6: Power circuit schematic of cascade capacitor coupled three phase 20 stage HVDC power supply

### 6.2.2 Design considerations

#### 6.2.2.1 Power source

The converter is designed to operate from a 230 V, 60 Hz 3 phase AC source. This makes the converter compatible with a majority of power outlets common in North America. The peak line to line voltage of 230 V AC source is 325 V. The maximum rectified DC bus voltage ($V_{in}$) of the 60 Hz rectifier will be 325 V. This voltage also influences the rating of the passive and switching components of the converter. All the components in the converter that need to withstand this voltage like series coupling capacitors, three phase inverter and three phase rectifier are rated for a maximum voltage of 400-600 V.

#### 6.2.2.2 Switching frequency

The switching frequency of operation affects the sizing of passive components and the selection of semiconductor switches. The switching frequency is selected to be in the range of 5kHz-20kHz. This is the typical frequency range of high performance motor drives in the power

range of few kW-100kW. This gives the flexibility us to use a wide variety of standard three phase motor drives from manufacturers like Rockwell Automation, Siemens etc. as the input stage.

#### 6.2.2.3 Input stage

The switching frequency range (5kHz-20kHz), the maximum blocking voltage (600V) and the maximum current (15A) provide the constraints for the selection of the input stage switches. The input stage is selected as a IGBT based two level three phase power driver module with integrated gate drive for the high side switches. The part ratings are: power driver module, 600V, 30A.

#### 6.2.2.4 Series coupling capacitors

There are two factors that affect the actual component selection of the series coupling capacitor.

- Voltage rating: The maximum voltage rating of any coupling capacitor is 400V.
- Current rating: In cascade coupling, the coupling capacitors nearest to the input stage conduct maximum current. That can be estimated analytically by calculating the RMS current of one stage and multiplying it by the number of stages as shown in Chapter 4 Eq 4.45-4.47. The maximum RMS current through the coupling capacitors is 14.75A.

These design constraints lead us to the following selection of the coupling capacitance: aluminum electrolytic capacitor,1500 $\mu$F 400V, 8A ripple current. Since the current rating is not satisfied with a single capacitor, two are connected in parallel for a total coupling capacitance of 3000 $\mu$F. The series impedance of the selection is negligible at the frequency of operation.

$$X_{cs} = \frac{1}{2\pi F_s C_s} \tag{6.1}$$

$$X_{cs} = \frac{1}{2\pi \times 10 \cdot 10^3 \times 3000 \cdot 10^{-6}} = 0.053\Omega \tag{6.2}$$

#### 6.2.2.5 Series inductance

The series inductance is selected to balance the requirement of acceptable harmonics on the line current of the HFI with the voltage drop across the inductance. The series inductance is selected as: wire wound ferrite core inductor, 100 $\mu$H 2.6A 90m$\Omega$.

#### 6.2.2.6 Output stage rectifiers

The output stage rectifier operates the switching frequency of 5-20kHz, with a maximum reverse blocking voltage of 600V and an average output current of 1A. The actual part is selected as a three phase diode bridge module with fast recovery diodes, with maximum reverse blocking voltage of 1.2kV and forward current rating of 30A and reverse recovery time of 40ns.

#### 6.2.2.7 Reverse blocking diodes

The reverse blocking diodes are essential in case of the three phase CCSAB converter to decouple the AC current of each output stage from its neighboring stage. The maximum current rating of this diode will be 1A and the maximum blocking voltage will be 600V. Since the current in this conduction path is DC, slow recovery diodes are selected with rating of: 6A, 1kV.

#### 6.2.2.8 Output stage filter capacitor

The same capacitor used as series coupling capacitor is also used as the filter capacitor on every output stage. The capacitor ratings are: 1500 $\mu$F 400 V, 8 A ripple current.

### 6.2.3 Hardware specifications

The high level specifications of the HVDC power supply are shown in Table 6.3. The HVDC power supply is designed to supply 6kV at 1A for a nominal operating rating of 6kW. The grid connected autotransformer is rated at 10kVA at 230V. The low frequency 60Hz diode bridge is designed for a maximum current rating of 30A per phase.

Table 6.3: Hardware specifications for cascade coupled three phase CCSAB converter

| Parameter | Units | Input | Output |
|---|---|---|---|
| **60 Hz grid interface** | | | |
| Line voltage | LL-RMS | 230 | NA |
| Line current | L-RMS | 17.5 | NA |
| **High frequency inverter interface** | | | |
| Bus voltage | V-AVG | 320 | 6000 |
| Bus current | A-AVG | 18.75 | 1 |
| Number of stages | $n$ | 1 | 20 |
| Voltage per stage | V-AVG | - | 300 |
| Current per stage | A-AVG | - | 1 |
| Total power | kW | 6 | |
| Switching freq | kHz | 10 | |

Table 6.4: Component details of the 20-stage HVDC power supply

| Component | Unit | Value | Description | Qty/$n$ | Total |
|---|---|---|---|---|---|
| **Input stage** | | | | | |
| AutoTX | kVA | 10 | 230V 60 HZ 3 PH AUTOTX. | 1 | 1 |
| DIODE-SLOW | D1-D6 | DSP25-12A | DIODE ARRAY GP 1200V 28A TO247AD | 3 | 3 |
| $C_{in}$ | $\mu$F | 1500 | CAP ALUM 1500UF 20% 400V SNAP | 2 | 2 |
| IGBT | S1-S6 | FSBB30CH60DF | POWER MODULE IGBT 3$\phi$ 600V 30A | 1 | 1 |
| **Output stage** | | | | | |
| $C_s$ | $\mu$F | 1500 | CAP ALUM 1500UF 20% 400V SNAP | 6 | 120 |
| $L_s$ | $\mu$H | 100 | FIXED IND 100UH 3A 40 MOHM TH | 3 | 60 |
| $C_{out}$ | $\mu$F | 1500 | CAP ALUM 1500UF 20% 400V SNAP | 1 | 20 |
| DIODE-FAST | D1-D6 | FUE30-12N1 | RECT BRIDGE FAST 3PHASE I4-PAC-5 | 1 | 20 |
| DIODE | $D_{rb}$ | 6A10DICT | DIODE GEN PURP 1KV 6A R6 | 1 | 20 |

### 6.2.4 Safety features

**Input relay and fuse protection on AC source** The three phase 60 Hz 230V AC source is both fuse and relay protected. The fuse is rated for 30A and the relay is rated for 60A.

**Emergency switch** The emergency switch (ESW) is wired in series to the input relay coil to turn off three phase 230V power to the converter. The ESW is a normally closed push button located on the front panel of the converter.

**Control return and Power return separated** The PWR RTN for the DC bus generated by the 60Hz rectifier ($V_{in}$) is used to power the gate drive. The front panel, controller

logic and sensors are powered by an isolated +15V, 0, -15V power supply with a separate return RTN.

**RELAY ON and PWM ON control signals** The front panel controls include two toggle switches that control the inverter logic relay and gate signal outputs. RELAY ON turns on the 60 Hz input relay and PWM ON turns on the gate signal output to the gate drivers of the three phase inverter input stage. The logic is coded such that the inverter can be turned ON only in this sequence.

**Inverter control logic FAULT trip** The three phase IGBT power module is protected from overcurrent by an internal short circuit sense logic present on the low side of all the three phase legs. If the current exceeds the short circuit current limit, all the gate signals on the low side are turned off and the $V_{FO}$ fault signal is pulled low. This is sensed by the inverter controller in a high priority interrupt and inverter enters FAULT state. In this state, all the IGBT gate signals are turned off, and the input AC relay is disconnected.

**Fuse protection in every output stage** All the output stages are fuse protected via slow acting printed circuit board (PCB) mounted fuses rated for 6A at 300V AC.

**Quick bleed resistors at every capacitor terminal** All the high voltage capacitors in the converter like the series coupling capacitors, output filter capacitors and the input DC bus capacitors are parallel connected with bleeder resistors that can quickly discharge the voltage across each capacitor. Additionally, each capacitor also includes an LED that indicates the charge status of the capacitor. The LED series resistance is designed to limit the LED current and turn off the LED when the capacitor voltage is less than 50 V.

**Board to board high voltage wiring** The DC output of all the output stage rectifiers are connected in series using HV rated wiring - 10kV insulation rating, 22 AWG.

**HV rated wiring for DC output** The high voltage DC output of the converter is connected to an external load via Bayonet Neill-Concelman (BNC) terminated wiring rated for 5kV

AC voltage. The outer shielding of the high voltage wiring is grounded to earth.

### 6.2.5 Inverter control software logic

The control software logic manages the sequential power up of the high voltage converter, varying the switching frequency of the input stage, managing the modulation sequence of the three phase inverter in the input stage, sensing the fault condition and sequential power off of the converter. The control logic is embedded in a hardware microcontroller SAMD21G18A which is a component in the Arduino M0 development board. The control platform is written in C and compiled using the open source compiler AVR-GCC provided by Arduino. The control state logic runs at a constant frequency of 10kH. The switching frequency of the inverter can be varied via push buttons on the front panel. By default the switching frequency is set to 10kHz and can be varied in steps in the range of range of 6-20 kHz. The six step state logic runs at a corresponding frequency range of 36-120 kHz.

The control state logic flow chart is shown in Fig 6.7. The control state starts in POWER state on system turn on, with AC relay, gate signals to inverter and the six step state machine clock all turned off. When the RELAYON rocker switch is turned on in the front panel, the logic transitions to RELAY state, where AC relay is turned on and the six step state machine clock is turned on. The gate signal are not turned on in this state. When the PWMON rocker switch is turned on in the front panel, the state transitions to RUN state where the gate signals are enabled to the inverter. The input stage inverter now feeds the three phase line to line AC voltage to all the cascaded output stages. The state logic transitions to FAULT state if the instantaneous over current protection limit is exceeded on the inverter power module.

### 6.2.6 Simulation and experimental results

#### 6.2.6.1 Nominal operation

Fig 6.8 shows the effect of cascade coupling capacitor ESR on the DC voltage distribution across all output stages. The analytical estimated voltage distribution derived in of Chapter 2 is compared with simulation of the 20 stage converter in PLECS and measured voltages in the

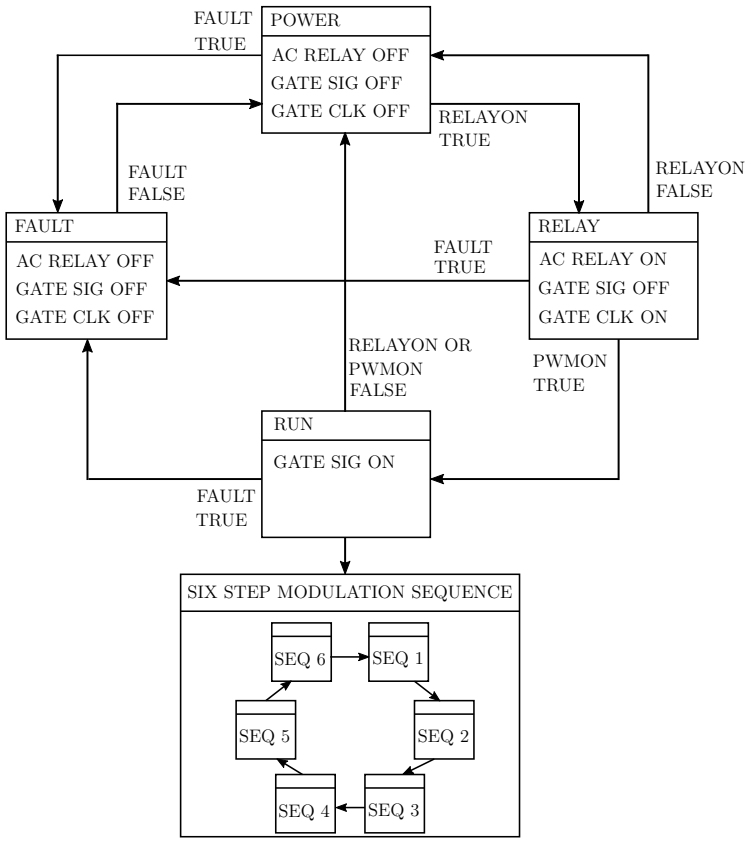


Figure 6.7: Flow chart showing control logic state machine

hardware setup of the three phase CCSAB converter. In all the cases, the output voltage $V_{out}$ is set at 600 V, and the load resistance $R_{out}$ is set at 600 Ω. The figure shows good agreement between the analytical model, simulation and experimental data.

Fig 6.9 shows the AC current per phase in different output stages of the converter. Since all the output stages are connected in series, the rectified DC output current will be identical in all stages. This in turn ensures that the AC line current in all output stages is also identical. This illustrates the modular nature of the converter behavior with power shared equally across all stages without need for power sharing control logic. The series inductor current in stages 4, 10 and 16 $i_{L4}, i_{L10}, i_{L16}$ is measured from the hardware setup of the three phase CCSAB and compared to a simulation of the 20 stage converter in PLECS. There is good agreement between simulation and experimental waveforms.

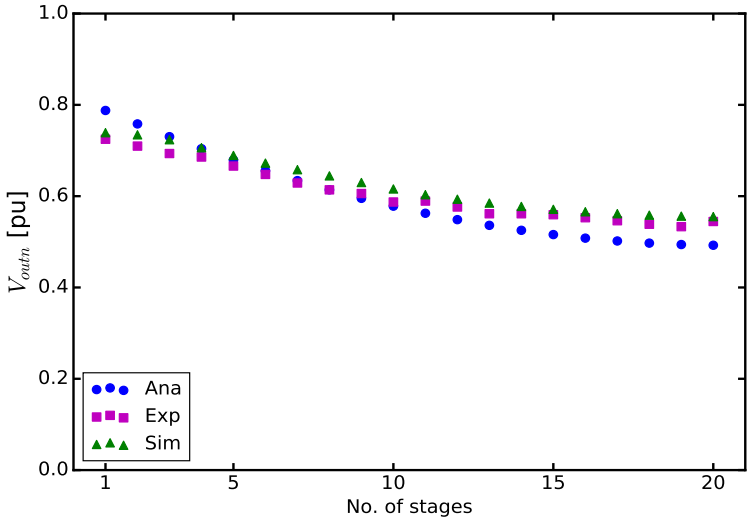


Figure 6.8: Effect of coupling capacitor ESR on output voltage across different stages. Per unit comparison of analytical calculation, experimental measurement and simulation of per stage output voltage. $C_s$=3000$\mu$F, $R_{cs}$=47m$\Omega$, Output stages=20, $V_{in}$=50V,$V_{out}$=600V.

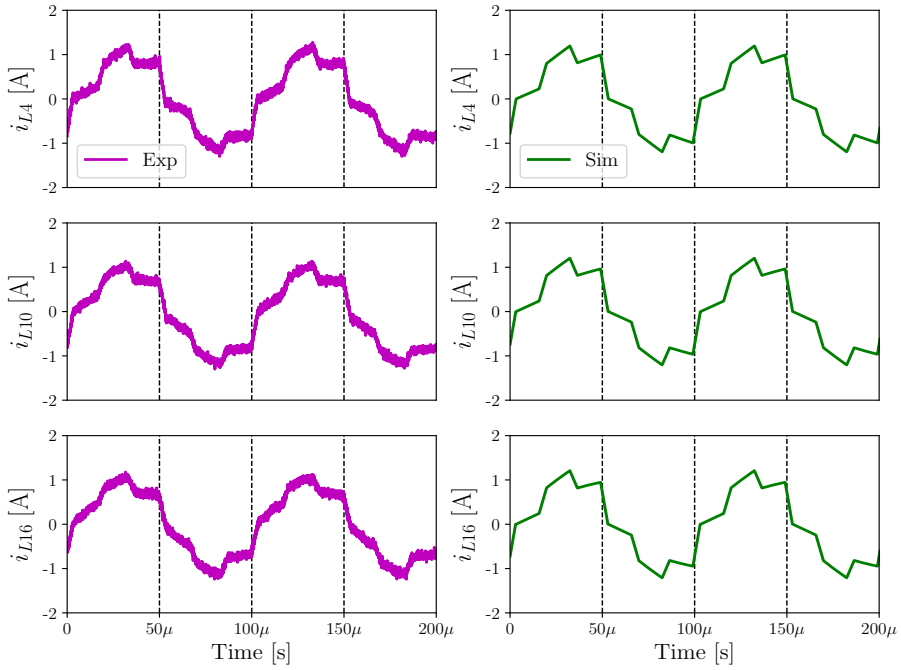


Figure 6.9: Series inductor line current in stages 4,10,16. $L_s$=100 $\mu$H, $R_{ls}$=90 m$\Omega$, Output stages=20, $V_{in}$=50V, $V_{out}$=600V, $F_s$=10 kHz.

Fig 6.12 -6.13 shows the simulated and experimental results for AC current and AC line-to-line voltage generated by the three phase inverter when $V_{out}$=3.3 kΩ, $P_{out}$ = 3.3 kW giving a output DC current of $I_{out}$=1 A. This is condition where the converter is operating at full output current but reduced output voltage. Fig 6.10 -6.11 shows the AC line-to-line voltage and current drawn from the 60 Hz, 230 V AC source under this condition. Under these conditions rectified DC bus voltage $V_{in}$ is at 185 V while the AC source power is at 4.2 kW.

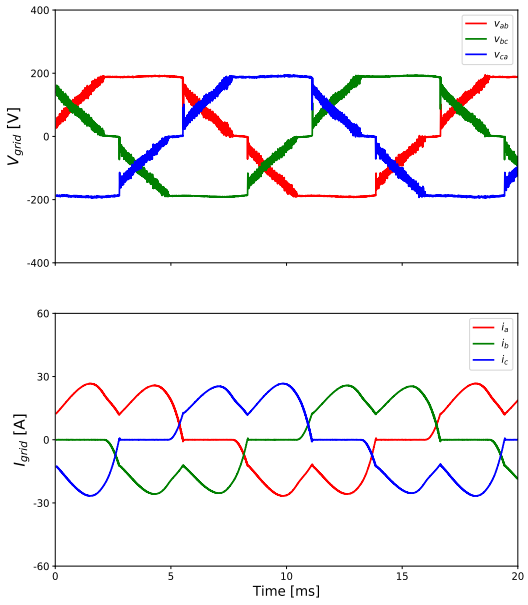


Figure 6.10: Experimental data. Top: Three phase line-to-line 60 Hz AC supply voltage. Bottom: Three phase line-to-line 60 Hz AC supply current. $V_{gridll}$=143.37 V, $I_{grid}$=16.77 A, $V_{in}$=185 V, $P_{in}$=4.2 kW.

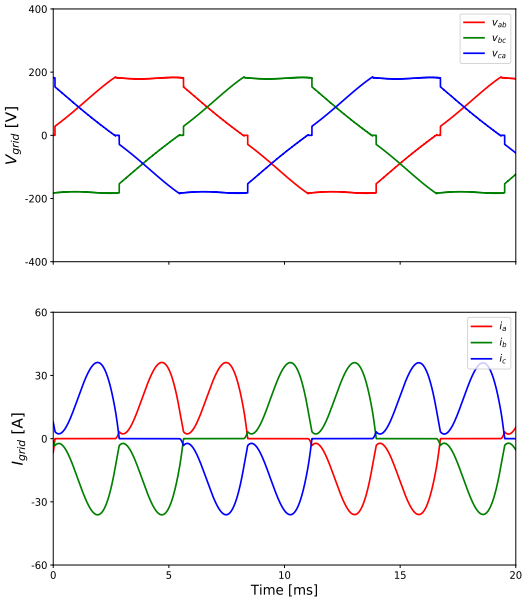


Figure 6.11: Simulation data. Top: Three phase line-to-line 60 Hz AC supply voltage. Bottom: Three phase line-to-line 60 Hz AC supply current. $V_{gridll}$=135 V, $I_{grid}$=19.18 A, $V_{in}$=179 V, $P_{in}$=3.6 kW.

Fig 6.16 -6.17 shows the simulated and experimental results for AC current and AC line-to-line voltage of the three phase inverter when $V_{out}$= 5 kV. The output DC load is kept constant at 3.3 kΩ which means that the converter is operating at DC output current of 1.5 A. This shows the capability of the converter operating under overcurrent conditions. The output power also exceeds the nominal output power rating of 6 kW to reach 7.48 kW, an overload of 24%. The AC power on the 60 Hz grid side under these conditions is 9.1 kW. The VA measured at the autotransformer output is 10 kVA which is the maximum VA rating of the transformer.

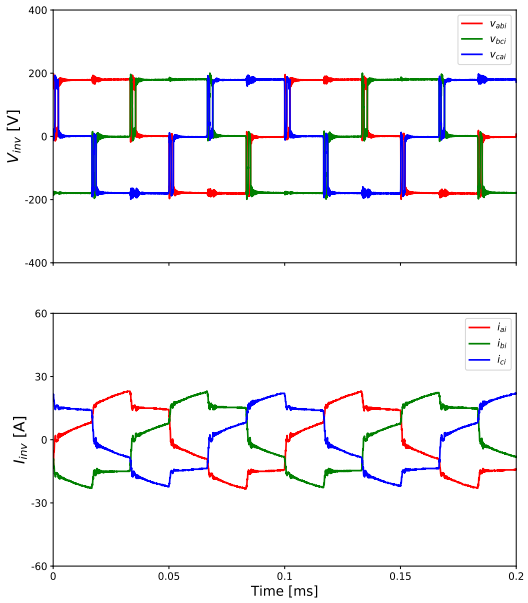


Figure 6.12: Experimental data. Top: Three phase AC line-to-line output voltage of inverter. Bottom: Three phase AC output current of inverter. $V_{iab}$=146 V, $I_{ia}$=14.82 A, $V_{out}$=3.3 kV, $P_{out}$=3.3 kW.

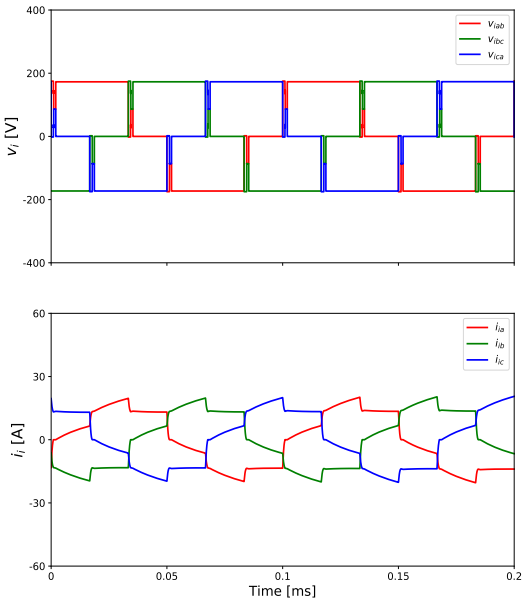


Figure 6.13: Simulation data. Top: Three phase AC line-to-line output voltage of inverter. Bottom: Three phase AC output current of inverter. $V_{iab}$=138.6 V, $I_{ia}$=11.53 A, $V_{out}$=3.3 kV, $P_{out}$=3.3 kW.

The converter is operated at different output voltages under constant load conditions and constant switching frequency. The converter is loaded using a high voltage load bank wired at $R_{load}$=3.33 kΩ and rated for peak power dissipation capability of 10 kW. The switching frequency is fixed at the nominal value of 10 kHz. The converter operation is verified over the entire power range and overall system efficiency of the entire converter system is recorded upto 5 kV. The measured efficiency is compared with the analytical estimated efficiency at a similar operating point which shows good agreement with analytical loss model vs the physical losses in the system.

#### 6.2.6.2 Fault operation

The behavior of the DC-DC cascade capacitor coupled converter in bipolar configuration with input side midpoint grounding during fault conditions has been covered in some detail in Chapter 5. The purpose of this subsection is to analyze the behavior of the three phase AC-

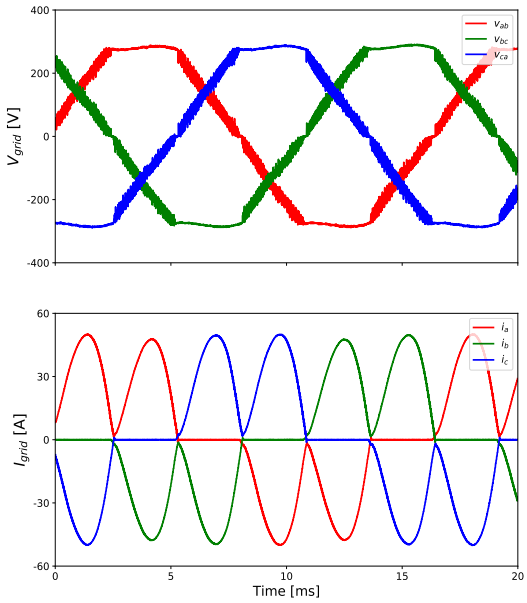


Figure 6.14: Experimental data. Top: Three phase line-to-line 60 Hz AC supply voltage. Bottom: Three phase line-to-line 60 Hz AC supply current. $V_{gridll}$=209.11 V, $I_{grid}$=27.84 A, $V_{in}$=275 V, $P_{in}$=9.1 kW.

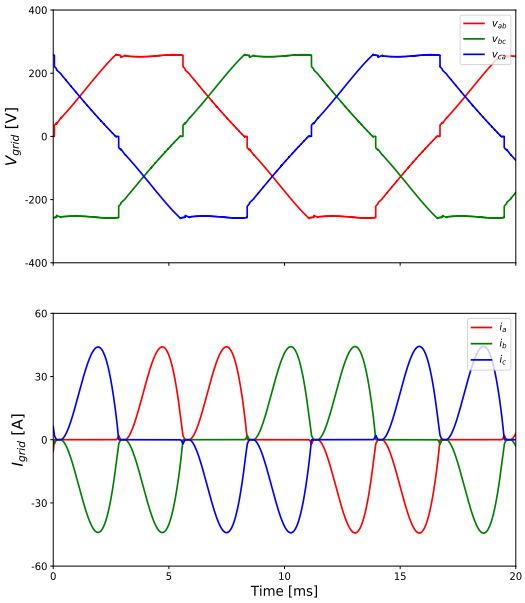


Figure 6.15: Simulation data. Top: Three phase line-to-line 60 Hz AC supply voltage. Bottom: Three phase line-to-line 60 Hz AC supply current. $V_{gridll}$=189.72 V, $I_{grid}$=23.05 A, $V_{in}$=275.1 V, $P_{in}$=5.8 kW.

DC capacitor coupled converter configuration. As shown in Fig 6.28, the entire converter is grounded on the 60 Hz AC source side by neutral to ground impedance $Z_g = R_g + j\omega L_g$. The ground referenced equivalent circuit of the converter with the 230 V, 60 Hz AC source is shown in Fig 6.20. Since the source is neutral grounded and the DC component of the neutral to ground voltage is approximately zero, the magnitude of the DC component of the fault current is entirely dependent on the DC output voltage between the fault terminal and ground. The fault current can be estimated as

$$I_{fdc} = \frac{nV_{outn}}{(R_g + R_{fault})} \tag{6.3}$$

(6.4)

where $R_{fault}$ refers to the resistance to ground at the fault terminal. As before, a fault on the DC output or AC coupling capacitor terminals appears as additional power that is reflected in the 60 Hz three phase AC source power. The additional power can be estimated from

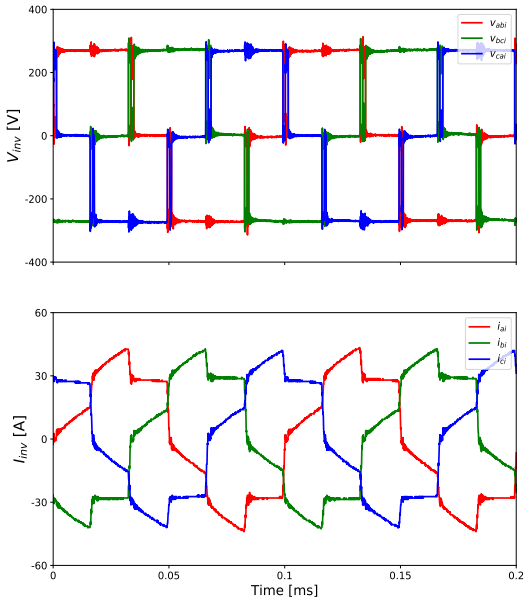


Figure 6.16: Experimental data. Top: Three phase AC line-to-line output voltage of inverter. Bottom: Three phase AC output current of inverter. $V_{iab}$=219.4 V, $I_{ia}$=27.76 A, $V_{out}$=5 kV, $P_{out}$=7.5 kW.

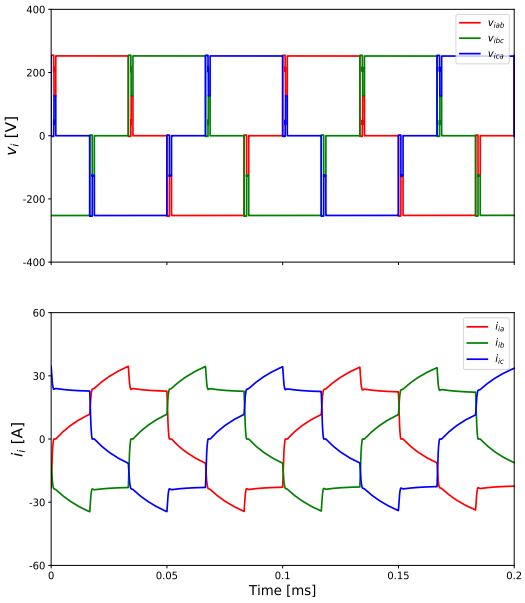


Figure 6.17: Simulation data. Top: Three phase AC line-to-line output voltage of inverter. Bottom: Three phase AC output current of inverter. $V_{iab}$=198.36 V, $I_{ia}$=17.8 A, $V_{out}$=4.6 kV, $P_{out}$=6.4 kW.

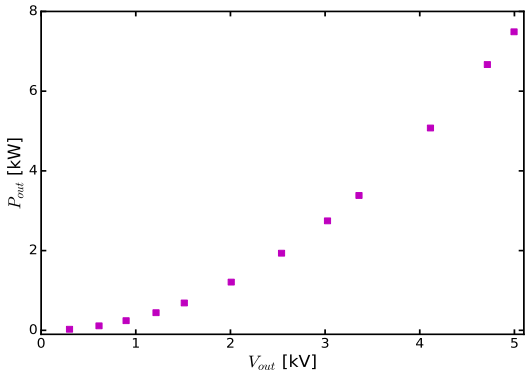


Figure 6.18: A plot of output power vs DC output voltage. $R_{load}$ = 3.3 kΩ.

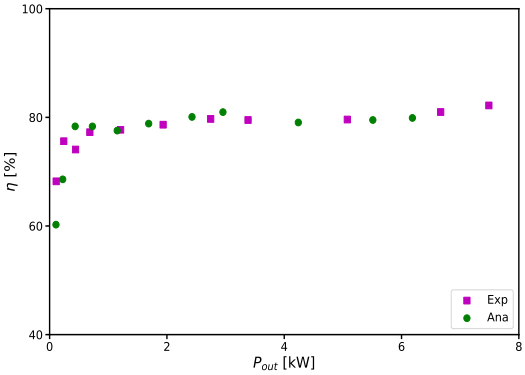


Figure 6.19: A plot comparing analytical and experimental overall system efficiency at constant switching frequency. $F_s$ = 10 kHz.

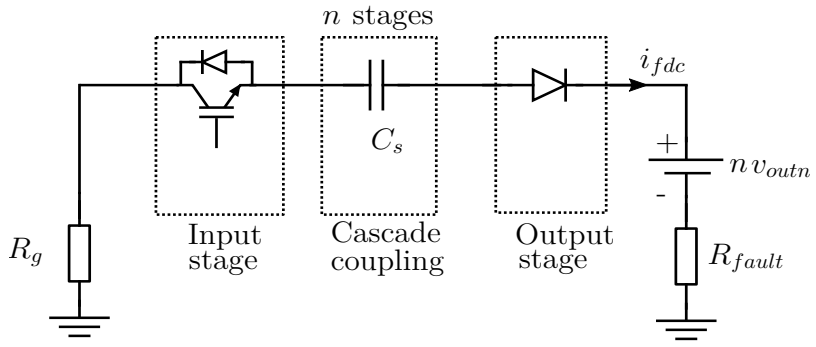


Figure 6.20: Ground referenced fault equivalent circuit for unipolar output configuration with neutral point grounding on the 60 Hz, three phase 230 V AC source

the differential mode fault power balance equivalent circuit as shown in Fig 6.21. From the

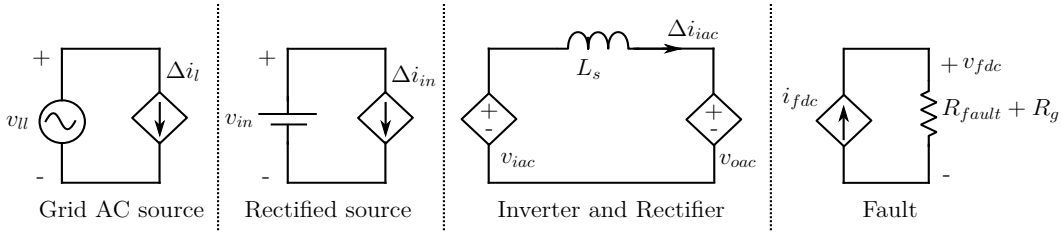


Figure 6.21: Fault power balance equivalent circuit

figure, the electrical terms on the fault side and rectified source side are AVG (pure DC) quantities while the quantities on the grid side and inverter and rectifier side are RMS (pure AC) quantities. The source current $\Delta i_l$ refers to the additional RMS line current at the 60 Hz AC source to balance the power loss in the fault. Similarly $\Delta i_{in}$ is the additional AVG current drawn at the rectified DC source generated by the 60 Hz diode front end. $i_{iac}$ is the RMS of AC component of the inverter output current $i_i$ and $\Delta i_{iac}$ refers to the increase in RMS current due to fault power. $v_{iac}$ refers to the line-to-line voltage at the output of the three phase high frequency inverter. The power balance equations are

$$P_{fault} = i_{fdc}^2 (R_{fault} + R_g) \tag{6.5}$$

This excess fault power is balanced on the three phase high frequency inverter (input stage) side by

$$P_{fault} = \sqrt{3} v_{iac} \Delta i_{iac} \tag{6.6}$$

This is then reflected on the rectified source side as

$$P_{fault} = v_{in} \Delta i_{in} \tag{6.7}$$

and on the grid side as

$$P_{fault} = \sqrt{3} v_{ll} \Delta i_{l} \tag{6.8}$$

The converter fault behavior is studied at full rated output voltage using a PLECS simulation model with all simulation parameters modeled after the measured quantities. The grounding impedance is constructed with a resistance $R_g$=600 Ω and reactance $L_g$=5.4 H. A fault resistance is set to $R_{fault}$=10 Ω. A DC output array fault to ground is initiated on the output terminal at $t$=33.33ms. The three phase inverter continues to operate through the fault and it can be observed in Fig 6.23 that the inverter line current envelope is increasing similar to Fig 6.30. As we can observe from Fig 6.22, the effect of a DC fault to ground in the converter is to add a DC bias in the AC current supplied by the 60 Hz source.

From Fig 6.24 we can see the effect of the fault on the coupling capacitor and filter capacitor voltages. $V_{out20}$ is the filter capacitor with the shorted terminal which accounts for the steep voltage drop after fault. The entire output voltage of the converter appears across the grouding impedancea as can be seen from Fig 6.24. The fault current is DC with a steady state value determined by the grounding resistance $R_g$ and the output voltage $V_{out}$. In this case the steady state fault current will be equal to 10A.

The three phase CCSAB converter is designed to float the output high voltage with respect to the ground. The converter is grounded at a single point at the 230V AC input via a grounding impedance from neutral of the AC source to ground. This experiment is conducted to determine the nature and magnitude of this grounding impedance. The three phase 230V 60 Hz three wire AC source is connected to a star connected auto transformer. The open circuit neutral to

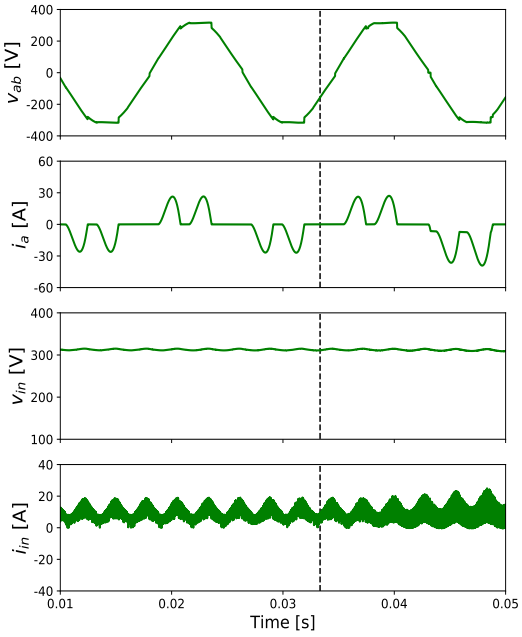


Figure 6.22: Top: Envelope of phase AB line-to-line voltage $v_i$ of three phase inverter. Bottom: Envelope of phase A line current $i_i$

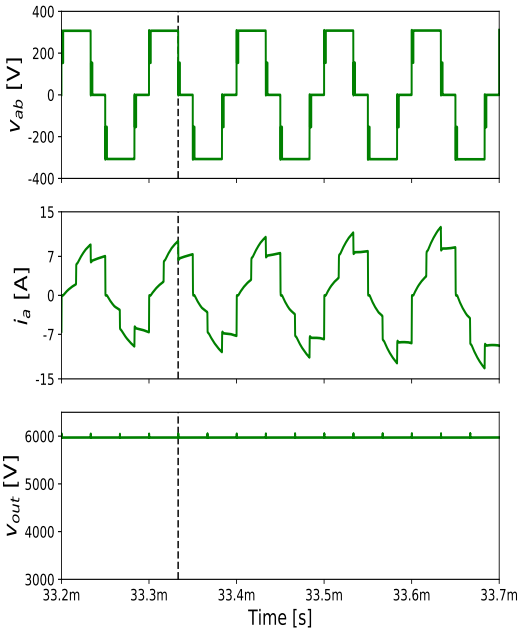


Figure 6.23: First: Line-to-line high frequency inverter output $v_{iab}$, Second: Inverter output line current $i_{ia}$, Third: 20 stage output DC voltage $v_{out}$.

ground voltage of the auto transformer $v_{ngoc}$ is measured as shown in Fig 6.25(a). Then a test resistance $R_{test}$ of known value is connected from the neutral point to ground and the neutral to ground voltage $v_{ngl}$ and current $i_{test}$ through the test resistance is measured as shown in Fig 6.25(b). The neutral to ground impedance at different frequencies can be estimated using Fourier analysis.

$$\overline{Z}_g^f = R_{test}\left(\frac{\overline{V}_{ngoc}^f}{\overline{V}_{ngl}^f} - 1\right) \tag{6.9}$$

where $\overline{Z}_g^f$ represents the complex neutral to ground impedance at frequency $f$, $\overline{V}_{ngoc}^f$ and $\overline{V}_{ngl}^f$ represent the Fourier harmonic at frequency $f$ of the neutral to ground voltage at open circuit and load conditions respectively. Fig 6.26 shows the time domain and frequency domain (magnitude and phase) of $v_{ngoc}$ and $v_{ngl}$. Fig 6.27 shows a frequency plot of $Z_g$ at upto 5th harmonic. This is then used to estimate the ground resistance and reactance at fundamental

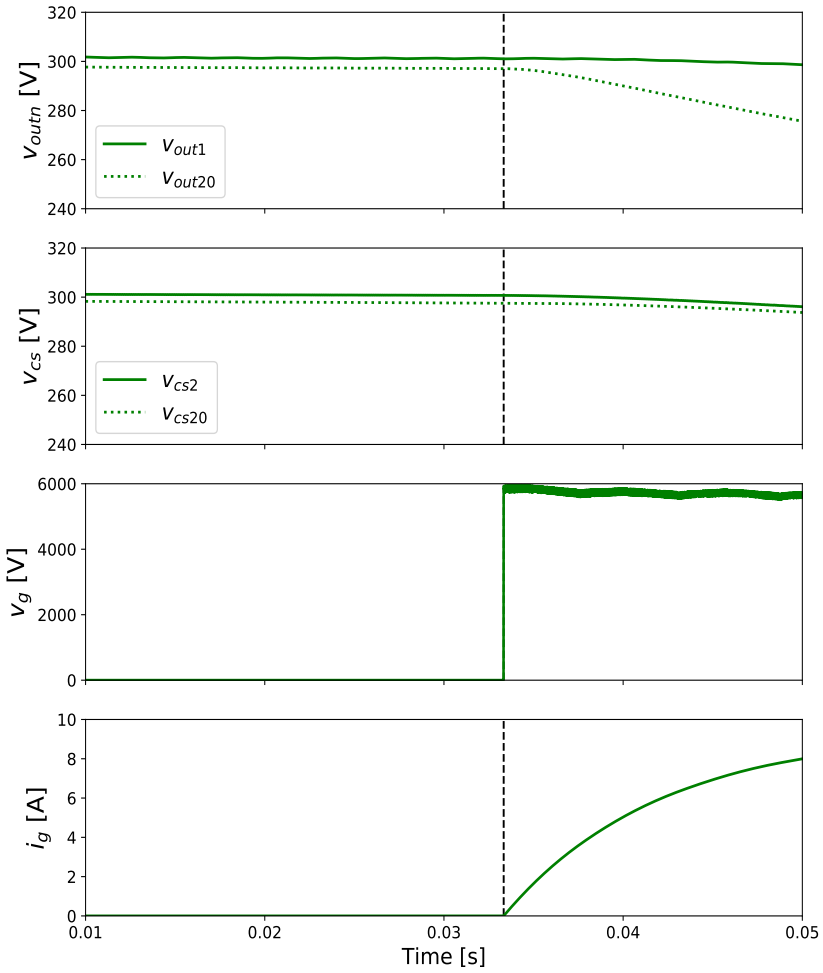


Figure 6.24: First: Rectified output voltage of stage 1 and 20 , Second: Coupling capacitor DC bias voltage stage 2 and 20, Third: Fault voltage across grounding impedance, Fourth: Fault current in grounding impedance

frequency.

$$\overline{Z}_g = R_g + j\omega L_g \tag{6.10}$$

From 6.27, $R_g$ at fundamental frequency is approximately 600 Ω and $L_g$ is approximately 5.4 H.

A DC output array fault is created on the high voltage side of the converter in order to study the effect of high voltage DC terminal to ground faults on the converter operation. A manually operated knife switch rated for high current is connected at the highest voltage

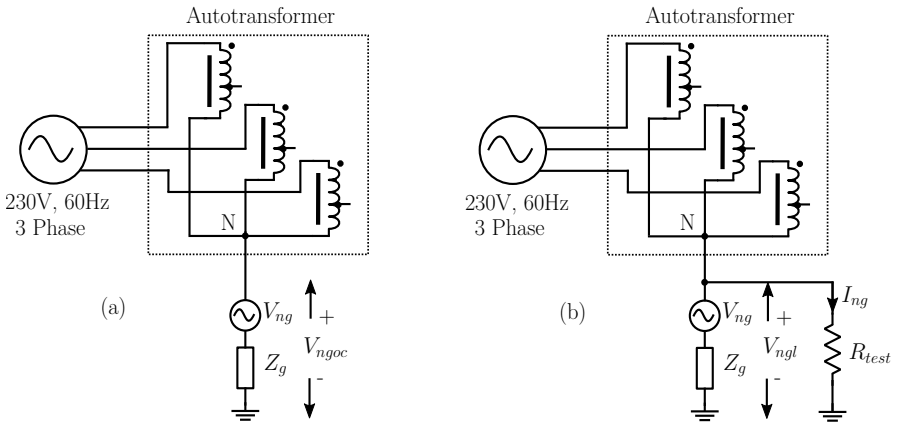


Figure 6.25: Schematic of experiment to determine grounding impedance $Z_g$ at the facility AC input

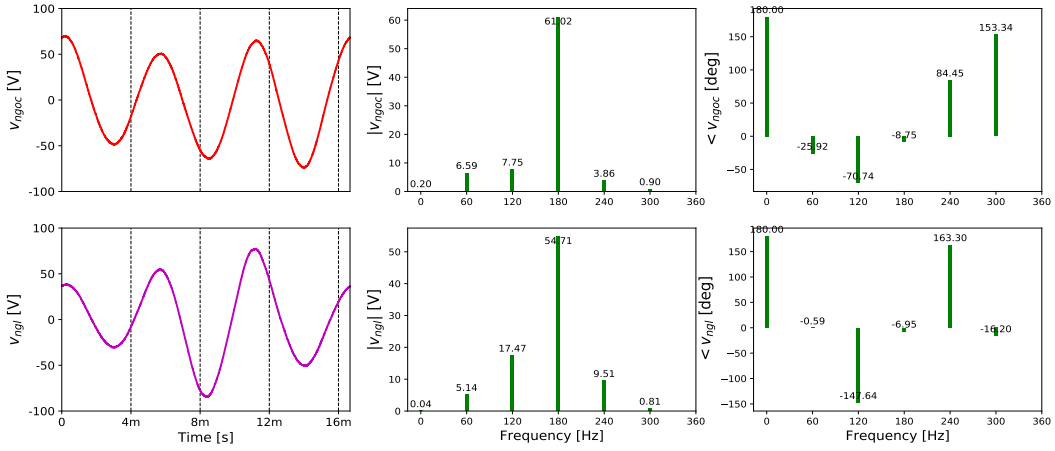


Figure 6.26: Harmonic spectrum of $v_{ngoc}$ and $v_{ngl}$

DC terminal as shown in Fig 6.28. In order to limit the fault current, a fault resistance of 900 Ω is connected in series with the knife switch. The other terminal of the fault resistance is grounded. A high voltage differential probe is connected across this fault resistance and a current probe is connected in series to measure the fault current. The other quantities of interest are the input side DC bus voltage $v_{in}$, the line-to-line AC output voltage of the inverter $v_{iab}$, line current of the inverter $i_{ia}$ and the overall output voltage $v_{out}$. The converter output voltage is set at 600 V and the output DC load is set at 3.3 kΩ. A DC output to ground fault is created after the converter has reached steady state operating conditions.

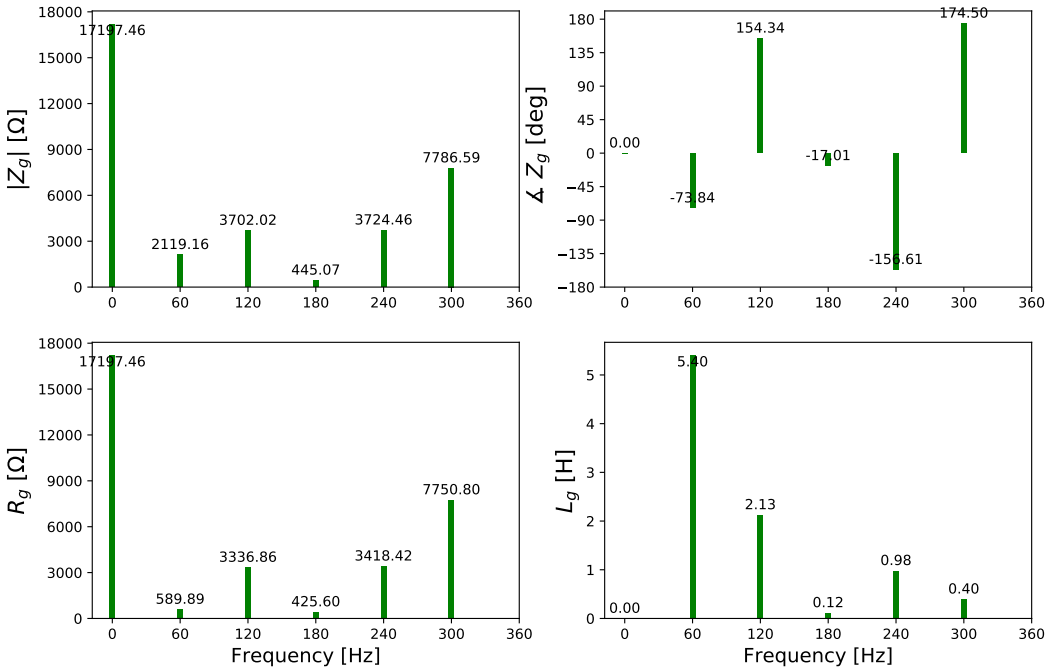


Figure 6.27: Harmonic spectrum of $Z_g$,$R_g$ and $L_g$

From Fig 6.30 the fault occurs at $t$=0.04s, and we can observer that the inverter current remains steady at the instant of the fault. However if the inverter continues to operate under this fault condition the inverter current will increase. The rate of increase of current is determined by the all the reactances in the fault path such as grounding reactance, autotransformer leakage reactance, source reactance etc. Fig 6.29 shows the current and voltage envelope of the three phase inverter confirming that inverter current is rising while the inverter voltage is slowly reducing.

Fig 6.31 shows the effect of the fault on output voltage and DC bus voltage. Before fault, the DC bus $v_{in}$ is approximately 35 V and $v_{out}$ is approximately 600 V. After the fault both the bus voltages are reducing. Before fault the fault terminal to ground voltage has a third harmonic AC voltage at 180 Hz on top of the expected DC voltage. Both AC and DC component of fault terminal voltage drop instantaneously after fault but persist at a different voltage level. The fault current also has an AC and DC component which remains steady after fault.

Fig 6.32-6.34 show the fault condition where the three phase inverter is turned off when a

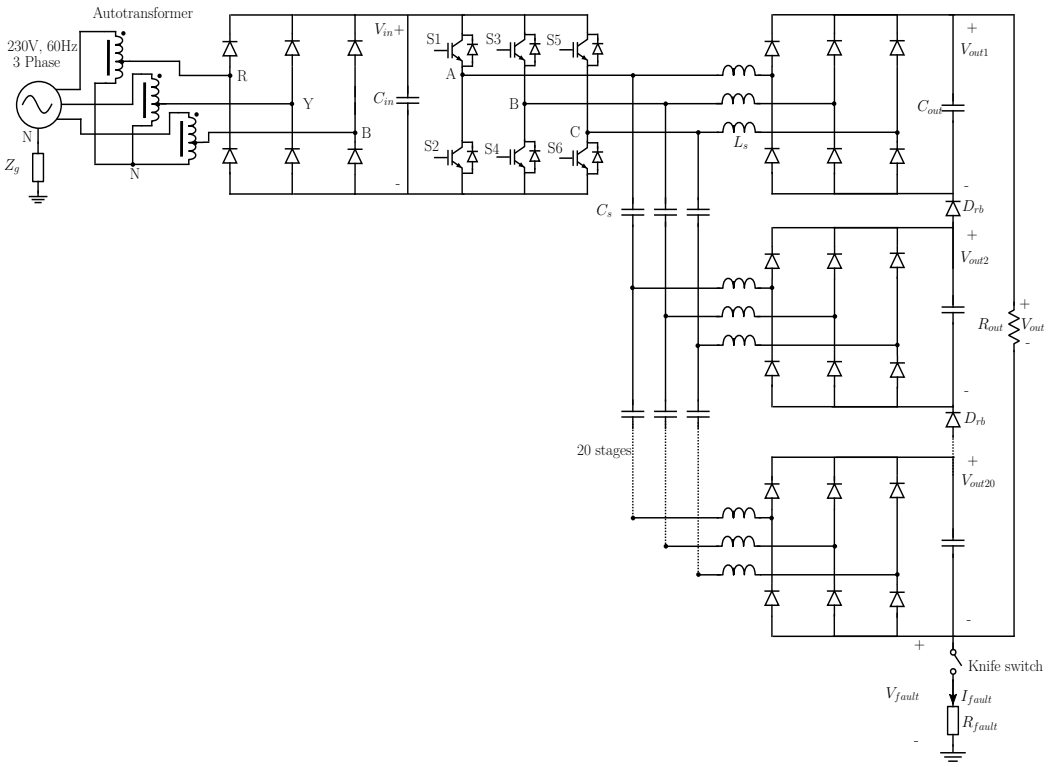


Figure 6.28: Power circuit schematic of the three phase cascade coupled CCSAB converter with 60 Hz neutral grounded AC source showing DC terminal to ground location.

fault condition is detected. The converter is operating under nominal condition before $t$=0.04s. At $t$=0.04s a DC output terminal to ground fault is created by closing the knife switch. The inverter is turned off after fault and it can be observed from both Fig 6.32 and Fig 6.33 that inverter line to line output voltage is not switching. However, the inverter line current will now be equal to the DC component of the fault current.

Since capacitively coupled converter do not include galvanic isolation, a DC fault on the output side will still present a conduction path through the reverse conduction diodes of the IGBT switches in the inverter. Hence turning off the IGBT switches will not break the path of the fault current. This can be seen in Fig 6.34 where the fault current $i_{fault} \neq 0$ even though the inverter is no longer switching. The fault current will sustain until the output voltage $v_{out}$ discharges to zero. Additionaly since there is no load on the input side DC bus, the voltage $v_{in}$ will now charge to the peak of the line-to-line 230 V 60 Hz AC source.

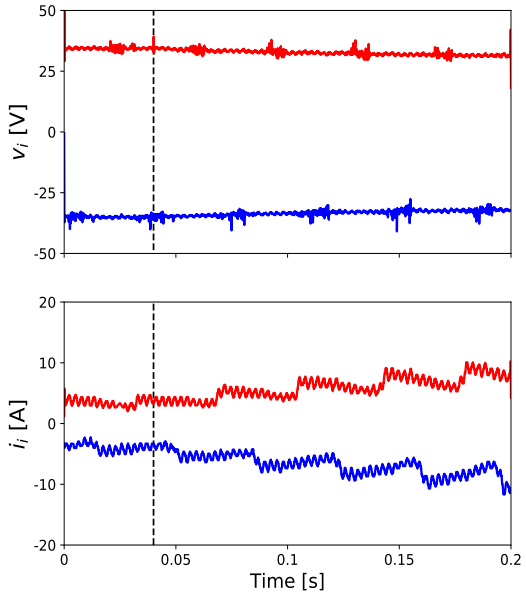


Figure 6.29: Top: Envelope of phase AB line-to-line voltage $v_i$ of three phase inverter. Bottom: Envelope of phase A line current $i_i$

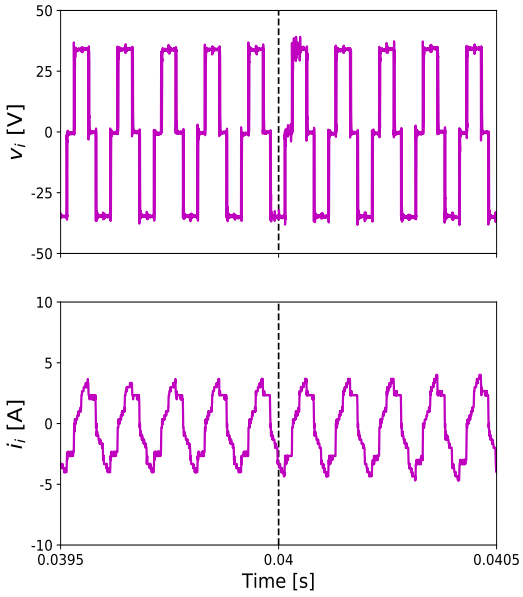


Figure 6.30: Top: Zoom view of phase AB line-to-line voltage $v_i$ of three phase inverter. Bottom: Zoom view of phase A line current $i_i$

## 6.3 Summary

The application examples utilize the unique properties of the capacitor coupled converters and provide good performance within the designed parameters. Two different capacitor coupled converter prototypes are built to explore the design capabilities of this topology. The low power high frequency single phase CCSAB converter is used to verify the steady state and dynamic model of the single phase topology. The high power low frequency three phase CCSAB converter is built to verify that the modular capacitor coupled topology can easily scale to kV of voltage and kW of power. The performance of the three phase converter under various load conditions is studied and the steady state model under six step modulation switching scheme is verified. A short circuit test on the high voltage DC output of the three phase converter is performed to verify the dynamic model under fault conditions.

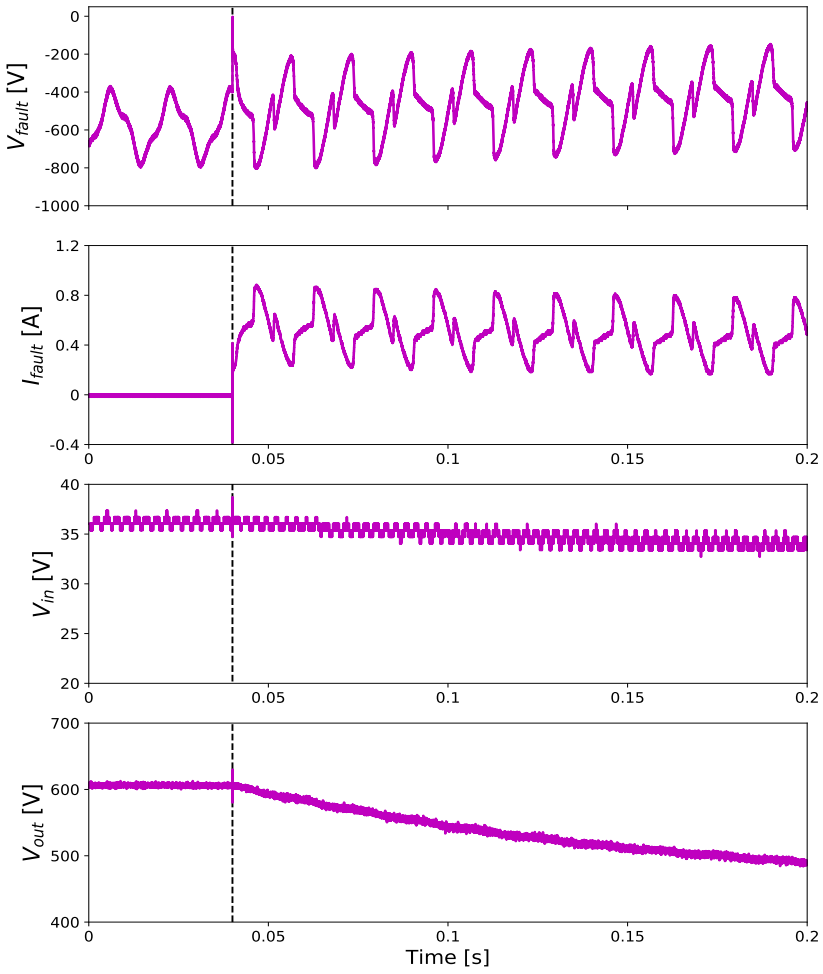


Figure 6.31: First: Voltage to ground at fault terminal $V_{fault}$, Second: Current to ground at fault terminal $I_{fault}$. Third: Input DC bus voltage $V_{in}$, Fourth: DC output voltage $V_{out}$. $R_{load}$=3.33 kΩ, $R_{fault}$=900 Ω.

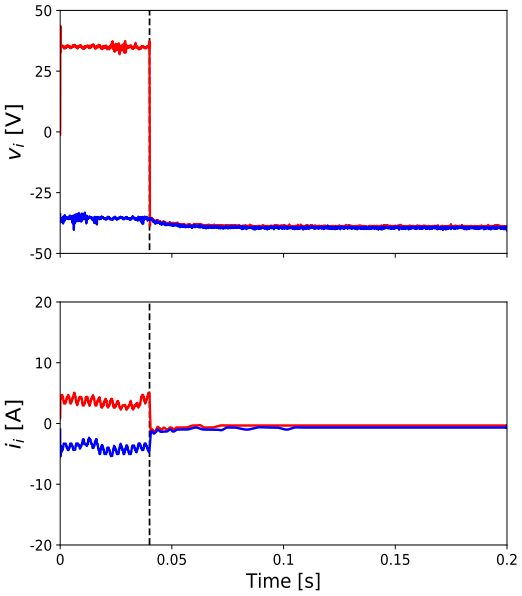


Figure 6.32: Top: Envelope of phase AB line-to-line voltage $v_i$ of three phase inverter. Bottom: Envelope of phase A line current $i_i$

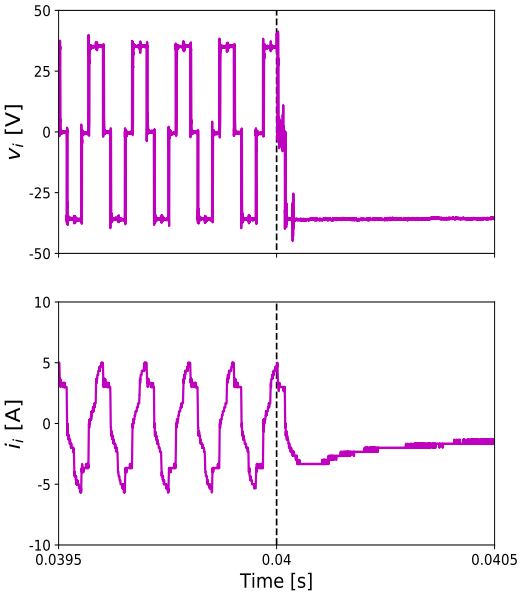


Figure 6.33: Top: Zoom view of phase AB line-to-line voltage $v_i$ of three phase inverter. Bottom: Zoom view of phase A line current $i_i$

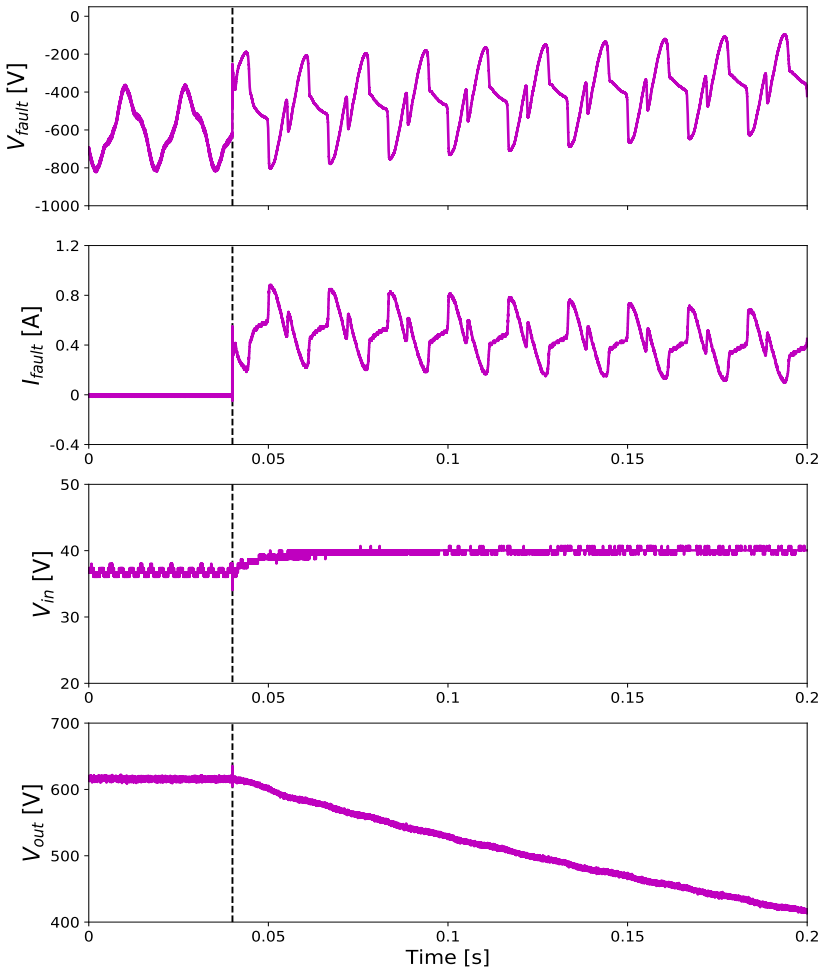


Figure 6.34: First: Voltage to ground at fault terminal $V_{fault}$, Second: Current to ground at fault terminal $I_{fault}$. Third: Input DC bus voltage $V_{in}$, Fourth: DC output voltage $V_{out}$. $R_{load}$=3.33 kΩ, $R_{fault}$=900 Ω.

CHAPTER 7

# Conclusions and Future Work

This research effort has focused on a systematic study of capacitor coupled power conversion as a critical step in the evolution of high power DC-DC systems. The major contributions of this study and remaining work are discussed further in the chapter.

## 7.1 Main contributions

**Comprehensive overview of DC-DC converters** A survey of the current state-of-the-art has been conducted by identifying the current role of DC-DC converters and classifying, comparing and contrasting the major categories of DC-DC boost topologies. The topologies are broadly classified into transformer coupled and transformer less topologies. An in depth review shows the current strengths, disadvantages and future trends of each class of converter. The role of transformers in increasing the power transfer capability of DC-DC converters is noted. The current requirements and future trends can be crystallized into a set of significant characteristics -modularity, distributed control, bidirectionality, suitability for system-on-a-chip realization.

**Selection of dual active bridge converter topology** The dual active bridge converter topol-

ogy has several advantages -fixed frequency operation, zero voltage switching characteristics over wide operating range, voltage source operation, simple control architecture, bidirectional power capability, impervious to parasitics. This topology also has its downsides, most of them stemming from the use of a magnetic transformer coupling between the input and output stages.

**Proposing novel capacitor coupled SAB topology** The unidirectional capacitor coupled single active bridge topology is proposed as an analogue to the transformer coupled single active bridge topology.

**Comprehensive steady state and dynamic modeling of CCSAB** The steady state model of the CCSAB is derived. It is shown that the CCSAB naturally operates in discontinuous inductor current mode. An averaged equivalent circuit model is developed and used to determine the small signal model of the converter. It is shown that the CCSAB operates with a single pole in the control range of interest leading to a simple control model.

**Analysis of design considerations of CCSAB** The design considerations of this novel topology are discussed in detail showing the important parameters that affect the sizing of passive components as well as the effect of sizing components on the steady state behavior of the circuit.

**Proposing novel capacitor coupled DAB topology** The transformer coupling in the dual active bridge converter has been replaced with capacitive coupling. The proposed topology shown to be analogous to the dual active bridge converter topology with similar steady state and dynamic characteristics.

**Comprehensive steady state and dynamic modeling of CCDAB** The steady state model resembles the transformer coupled dual active bridge converter. The topology and steady state operation of the converter has been analyzed for phase shift modulation between the input and output stages. The concept of dynamic phasors is used to develop a dy-

namic model, and this concept is further extended to derive the state space model for an n-stage converter.

**Analysis of design considerations of CCDAB** The design considerations of this novel topology are discussed in detail showing the important parameters that affect the sizing of passive components as well as the effect of sizing components on the behavior of the circuit.

**Critical evaluation of converter characteristics** The proposed capacitor coupled DC-DC converter topologies have a number of characteristics that are subtly different from existing converter topologies. Hence an examination of these characteristics will prove to be instructive to appreciate and quantify the effect of the design trade-offs that emerge as a consequence of this topology.

**Comparative evaluation with transformer coupled topologies** The comparative evaluation of this novel topology with existing transformer coupled single and dual active bridge converter is important to understand the real-world benefits and trade offs associated with the proposed topologies.

**Application case studies** Two different capacitor coupled converter prototypes are built to explore the design capabilities of this topology. The low power high frequency single phase CCSAB converter is used to verify the steady state and dynamic model of the single phase topology. The high power low frequency three phase CCSAB converter is built to verify that the modular capacitor coupled topology can easily scale to kV of voltage and kW of power. The converter architecture for all these designs is detailed along with the hardware specifications and designed parameters. The analytical model is verified using computer simulation during nominal and fault operation.

**Design, construction and validation of high voltage power supply** A 6kV, 6kW high voltage DC power supply operating on three phase 230V, 60 Hz AC input is built based on the three phase cascade coupled CCSAB topology. The performance of the three phase

converter under various load conditions is studied and the steady state model under six step modulation switching scheme is verified.

**Fault analysis and grounding strategies** The capacitor coupled topology is a modular and non-isolated topology where the fault current path dependent on the location of the fault terminal from the input stage. An equivalent circuit that models the behavior of the converter during fault conditions is proposed. A simulation study of the various fault configurations confirms the analytical fault model. A short circuit test on the high voltage DC output of the three phase converter is performed to verify the analytical fault model.

## 7.2 Future work

**Design, construction and validation of high efficiency power converter** The parallel capacitor coupled CCDAB topology is well suited to operate at high switching frequencies. A high efficient compact DC-DC converter based on this architecture would be ideal for applications that require high performance in a small volume and size.

**Distributed synchronous control of CCDAB** The control architecture of the CCDAB as detailed in this thesis needs high accuracy synchronization between the PWM generated by the input stage and the output stages. One way to achieve synchronization is by sampling the voltage waveform at every output stage. A controller logic at every stage can then modulate the switching times of its own switches to achieve the desired output voltage per stage. Multiple controllers working in sync can then control the overall output voltage in a distributed manner. More work is need to validate this approach and achieve distributed synchronous control.

**EMI filtering strategies** The absence of galvanic isolation also has implications on conducted common mode electromagnetic interference (EMI) which can now propagate from

the input stage to all output stages. The effect of this EMI needs to be characterized and mitigated.

**Parametric analysis of component sizing** The passive components $L_s$,$C_s$ are linked to the implicit variables of the system $R_{out}$, $F_s$. A better understanding of sizing of the capacitor coupled converters can be had by parameterizing this relationship between the passive components as a function of per unit power. This will also guide future designers to size the various components depending on the switching frequency and operating power level.

**Applications using wide bandgap devices** Silicon carbide and gallium nitride devices are well suited for high switching frequencies. The power density and operating voltage of capacitor coupled converters can be further increased by incorporating these wide bandgap devices in capacitively coupled topologies.

**Resonant operation** The capacitor coupled converters discussed in this work all size the coupling capacitance such that the capacitive impedance is negligible at operating frequency. However, the series inductor and coupling capacitor in each output stage form a potential resonant network. By varying the switching frequency to and away from this resonant frequency, it is possible to control both output voltage and output power and simultaneously reduce the the switching power loss. This is another active research area that can provide some interesting benefits in terms of reducing the size of coupling capacitors.

**Reliability analysis** The three phase CCSAB application design discussed in this work uses aluminum electrolytic capacitors extensively. The lifetime of these capacitors is very sensitive to operating temperature. A reliability study of capacitor coupled converters will be useful in quantifying not only the bill of material cost but also the lifetime reliability cost of using electrolytic capacitors vs film or ceramic capacitors.

## 7.3 Summary

The work presented in this thesis is expected to open up new research possibilities in areas such as

- Miniaturization and integrated circuit realization
- Multiterminal MVDC and HVDC systems
- Wireless transfer applications
- Resonant topologies
- Battery equalization systems
- Multilevel output integration with inverters

At the conclusion, it is expected that this work will firmly establish the field of capacitor coupled DC-DC power conversion as a competitive approach for realizing high power DC systems.

# Bibliography

[1] N. C. for Photovoltaics, "Best research-cell efficiency," 2016.
[Online; accessed 05-Dec-2016].

[2] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*.
Springer Science & Business Media, 2007.

[3] N. Mohan and T. M. Undeland, *Power electronics: converters, applications, and design*.
John Wiley & Sons, 2007.

[4] F. C. Schwarz, "An improved method of resonant current pulse modulation for power converters," *Industrial Electronics and Control Instrumentation, IEEE Transactions on*, no. 2, pp. 133–141, 1976.

[5] S. Johnson, A. Witulski, and R. Erickson, "A comparison of resonant topologies in high voltage dc applications," in *Applied Power Electronics Conference and Exposition, 1987 IEEE*, pp. 145–156, IEEE, 1987.

[6] M. Hajian, J. Robinson, D. Jovcic, and B. Wu, "30 kw, 200 v/900 v, thyristor lcl dc/dc converter laboratory prototype design and testing," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 1094–1102, March 2014.

[7] M. K. Kazimierczuk and D. Czarkowski, *Resonant power converters*.
John Wiley & Sons, 2012.

[8] M. Youssef and P. Jain, "A review and performance evaluation of control techniques in resonant converters," in *Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of IEEE*, vol. 1, pp. 215–221 Vol. 1, Nov 2004.

[9] R. Steigerwald, "High-frequency resonant transistor dc-dc converters," *Industrial Electronics, IEEE Transactions on*, vol. IE-31, pp. 181–191, May 1984.

[10] D. Fu, S. Wang, P. Kong, F. Lee, and D. Huang, "Novel techniques to suppress the common-mode emi noise caused by transformer parasitic capacitances in dc dc

converters," *Industrial Electronics, IEEE Transactions on*, vol. 60, pp. 4968–4977, Nov 2013.

[11] Q. Wang, X. Zhang, R. Burgos, D. Boroyevich, A. White, and M. Kheraluwala, "Design considerations for a high efficiency 3 kw llc resonant dc/dc transformer," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, pp. 5454–5461, Sept 2015.

[12] J.-P. Vandelac and P. Ziogas, "A dc to dc pwm series resonant converter operated at resonant frequency," *Industrial Electronics, IEEE Transactions on*, vol. 35, pp. 451–460, Aug 1988.

[13] R. Oruganti, J. J. Yang, and F. C. Lee, "Implementation of optimal trajectory control of series resonant converter," in *Power Electronics Specialists Conference, 1987 IEEE*, pp. 451–459, June 1987.

[14] H. Chen, E. Sng, and K.-J. Tseng, "Generalized optimal trajectory control for closed loop control of series-parallel resonant converter," *Power Electronics, IEEE Transactions on*, vol. 21, pp. 1347–1355, Sept 2006.

[15] W. Feng and F. Lee, "Optimal trajectory control of llc resonant converters for soft start-up," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 1461–1468, March 2014.

[16] W. Inam, K. Afridi, and D. Perreault, "High efficiency resonant dc/dc converter utilizing a resistance compression network," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 4126–4135, Aug 2014.

[17] J. Lu, D. Perreault, and K. Afridi, "Impedance control network resonant dc-dc converter for wide-range high-efficiency operation," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, pp. 1440–1447, March 2015.

[18] D. Reusch and J. Strydom, "Evaluation of gallium nitride transistors in high frequency resonant and soft-switching dc-dc converters," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, pp. 464–470, March 2014.

[19] A. Sepahvand, L. Scandolat, Y. Zhang, and D. Maksimovic, "Voltage regulation and efficiency optimization in a 100 mhz series resonant dc-dc converter," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, pp. 2097–2103, March 2015.

[20] S. Fan, T. Lint, H. Zhang, S. Finney, and B. Williams, "Design and control of wind energy conversion system based on resonant dc/dc converter," in *Renewable Power Generation (RPG 2011), IET Conference on*, pp. 1–6, Sept 2011.

[21] D. Dujic, G. Steinke, E. Bianda, S. Lewdeni-Schmid, C. Zhao, and J. Steinke, "Characterization of a 6.5kv igbt for medium-voltage high-power resonant dc-dc converter," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, pp. 1438–1444, March 2013.

[22] N. Shafiei, M. Pahlevaninezhad, H. Farzanehfard, A. Bakhshai, and P. Jain, "Analysis of a fifth-order resonant converter for high-voltage dc power supplies," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 85–100, Jan 2013.

[23] R. W. a. a. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Transactions on Industry Applications*, vol. 27, no. 1 pt 1, pp. 63–73, 1991.

[24] M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," *IEEE Transactions on Industry Applications*, vol. 28, no. 6, pp. 1294–1301, 1992.

[25] H. van Hoek, M. Neubert, A. Kroeber, and R. W. De Doncker, "Comparison of a single-phase and a three-phase dual active bridge with low-voltage, high-current output," *International Conference on Renewable Energy Research and Applications (ICRERA)*, pp. 1–6, 2012.

[26] D. Segaran, D. Holmes, and B. McGrath, "Comparative analysis of single and three-phase dual active bridge bidirectional DC-DC converters," *2008 Australasian Universities Power Engineering Conference*, vol. 1, pp. 1–6, 2008.

[27] M. H. Kheraluwala, *High-power high-frequency dc-to-tc converters*.
PhD thesis, University of Wisconsin-Madison, 1991.

[28] F. Krismer, S. Round, and J. W. Kolar, "Performance optimization of a high current dual active bridge with a wide operating voltage range," *PESC Record - IEEE Annual Power Electronics Specialists Conference*, 2006.

[29] F. Krismer and J. Kolar, "Accurate Power Loss Model Derivation of a High-Current Dual Active Bridge Converter for an Automotive Application," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 3, pp. 881–891, 2010.

[30] F. Krismer, *Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies*.
PhD thesis, Eidgenssische Technische Hochschule ETH Zrich, 2010.

[31] N. M. L. Tan, T. Abe, and H. Akagi, "Optimal design of a high-efficiency bidirectional isolated dc-dc converter across a wide range of power transfer," in *Power and Energy (PECon), 2012 IEEE International Conference on*, pp. 22–27, IEEE, 2012.

[32] L. Xue, M. Mu, D. Boroyevich, V. Tech, P. Mattavelli, and a. G. M.-c. M. Introduction, "The Optimal Design of GaN-based Dual Active Bridge for Bi-Directional Plug-in Hybrid Electric Vehicle ( PHEV ) Charger," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 602–608, 2015.

[33] H. Zhou and a. M. Khambadkone, "Hybrid Modulation for Dual-Active-Bridge Bidirectional Converter With Extended Power Range for Ultracapacitor Application," *Industry Applications, IEEE Transactions on*, vol. 45, no. 4, pp. 1434–1442, 2009.

[34] A. Jain and R. Ayyanar, "PWM control of dual active bridge: comprehensive analysis and experimental verification," *2008 34th Annual Conference of IEEE Industrial Electronics*, vol. 26, no. 4, pp. 1215–1227, 2008.

[35] H. Bai and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge dc-dc converters using novel dual-phase-shift control," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2905–2914, 2008.

[36] K. Myoungho, M. Rosekeit, S. Seung-Ki, and R. W. a. a. De Doncker, "A dual-phase-shift control strategy for dual-active-bridge DC-DC converter in wide voltage range," *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on*, pp. 364–371, 2011.

[37] A. Kadavelugu, S. Baek, S. Dutta, S. Bhattacharya, M. Das, A. Agarwal, and J. Scofield, "High-frequency design considerations of dual active bridge 1200 V SiC MOSFET DC-DC converter," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 314–320, 2011.

[38] N. H. Baars, H. Huisman, and J. L. Duarte, "A 80 kW Isolated DC-DC Converter for Railway Applications," in *16th European Conference on Power Electronics and Applications (EPE'14-ECCE Europe)*, pp. 26–28, 2014.

[39] H. Akagi and R. Kitada, "Control and design of a modular multilevel cascade BTB system using bidirectional isolated dc/dc converters," *IEEE Transactions on Power Electronics*, vol. 26, no. 9, pp. 2457–2464, 2011.

[40] P. Zumel, L. Ortega, A. Lazaro, C. Fernandez, A. Barrado, A. Rodriguez, and M. M. Hernando, "Modular dual active bridge converter architecture," *IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, no. 1, pp. 1081–1087, 2014.

[41] K. Mainali, A. Tripathi, D. C. Patel, S. Bhattacharya, and T. Challita, "Design, measurement and equivalent circuit synthesis of high power HF transformer for three-phase composite dual active bridge topology," *IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, pp. 342–349, 2014.

[42] Y. Panov, M. M. Jovanovi, and B. T. Irving, "Novel Transformer-Flux-Balancing Control of Dual-Active- Bridge Bidirectional Converters," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 42–49, 2015.

[43] X. Hu and C. Gong, "A High Gain Input-Parallel Output-Series DC/DC Converter with Dual Coupled-Inductors," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1306–1317, 2015.

[44] C.-m. Young, S.-j. Cheng, J.-w. Siao, and W.-s. Yeh, "An Input-Parallel and Output-Series-Parallel Phase-Shift Full-Bridge Converter with Maximum Power Point Tracking for Wind Turbine," in *International Conference on Renewable Energy Research and Applications (ICRERA)*, pp. 20–23, October 2013.

[45] Y. Lian, G. Adam, D. Holliday, and S. Finney, "Active power sharing in input-series-input-parallel output-series connected dc/dc converters," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 2790–2797, IEEE, 2015.

[46] P. Bartal, J. Hamar, and I. Nagy, "Efficiency improvement in modular dc/dc converters using unequal current sharing," in *Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2012 International Symposium on*, pp. 275–280, IEEE, 2012.

[47] Y. Ting, S. De Haan, and B. Ferreira, "Modular single-active bridge dc-dc converters: Efficiency optimization over a wide load range," *IEEE Industry Applications Magazine*, vol. 22, no. 5, pp. 43–52, 2016.

[48] S. Waffler and J. Kolar, "Efficiency optimization of an automotive multi-phase bidirectional dc-dc converter," in *Power Electronics and Motion Control Conference, 2009. IPEMC'09. IEEE 6th International*, pp. 566–572, IEEE, 2009.

[49] X. She, A. Q. Huang, and X. Ni, "Current sensorless power balance strategy for dc/dc converters in a cascaded multilevel converter based solid state transformer," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 17–22, 2014.

[50] W. Li, Q. Jiang, Y. Mei, C. Li, Y. Deng, and X. He, "Modular multilevel dc/dc converters with phase-shift control scheme for high-voltage dc-based systems," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 99–107, 2015.

[51] R. Middlebrook, "Transformerless dc-to-dc converters with large conversion ratios," *Power Electronics, IEEE Transactions on*, vol. 3, no. 4, pp. 484–488, 1988.

[52] S.Cuk, "Basics of switched-mode power conversion: Topologies, magnetics and control," *Advances in Switched-Mode Power Conversion*, vol. 2, pp. 279–310, 1981.

[53] F. Lessa Tofoli, D. De Castro Pereira, W. Josias de Paula, and D. De Sousa Oliveira JuÃÅnior, "Survey on non-isolated high-voltage step-up dc dc topologies based on the boost converter," *Power Electronics, IET*, vol. 8, no. 10, pp. 2044–2057, 2015.

[54] A. Tomaszuk and A. Krupa, "High efficiency high step-up dc/dc converters-a review," *Bulletin of the Polish Academy of Sciences: Technical Sciences*, vol. 59, no. 4, pp. 475–483, 2011.

[55] W. Li and X. He, "Review of nonisolated high-step-up dc/dc converters in photovoltaic grid-connected applications," *Industrial Electronics, IEEE Transactions on*, vol. 58, pp. 1239–1250, April 2011.

[56] R. Middlebrook, "A continuous model for the tapped-inductor boost converter," in *Power Electronics Specialists Conference, 1975 IEEE*, pp. 63–79, IEEE, 1975.

[57] Q. Zhao and F. C. Lee, "High-efficiency, high step-up dc-dc converters," *Power Electronics, IEEE Transactions on*, vol. 18, no. 1, pp. 65–73, 2003.

[58] F. S. Silva, A. A. Freitas, S. Daher, S. C. Ximenes, S. K. Sousa, M. Edilson Jr, F. L. Antunes, and C. M. Cruz, "High gain dc-dc boost converter with a coupling inductor," in *Power Electronics Conference, 2009. COBEP'09. Brazilian*, pp. 486–492, IEEE, 2009.

[59] D. R. Garth, W. Muldoon, G. Benson, and E. Costague, "Multi-phase, 2-kilowatt, high-voltage, regulated power supply," in *Power Electronics Specialists Conference, 1971 IEEE*, pp. 110–116, IEEE, 1971.

[60] R. Gules, L. L. Pfitscher, and L. C. Franco, "An interleaved boost dc-dc converter with large conversion ratio," in *Industrial Electronics, 2003. ISIE'03. 2003 IEEE International Symposium on*, vol. 1, pp. 411–416, IEEE, 2003.

[61] S. Dwari and L. Parsa, "An efficient high-step-up interleaved dc–dc converter with a common active clamp," *Power Electronics, IEEE Transactions on*, vol. 26, no. 1, pp. 66–78, 2011.

[62] Y. Deng, Q. Rong, W. Li, Y. Zhao, J. Shi, and X. He, "Single-switch high step-up converters with built-in transformer voltage multiplier cell," *Power Electronics, IEEE Transactions on*, vol. 27, no. 8, pp. 3557–3567, 2012.

[63] R.-J. Wai and R.-Y. Duan, "High step-up converter with coupled-inductor," *Power Electronics, IEEE Transactions on*, vol. 20, no. 5, pp. 1025–1035, 2005.

[64] W. Li, Y. Zhao, Y. Deng, and X. He, "Interleaved converter with voltage multiplier cell for high step-up and high-efficiency conversion," *Power Electronics, IEEE Transactions on*, vol. 25, no. 9, pp. 2397–2408, 2010.

[65] G. A. Henn, R. Silva, P. P. Praça, L. H. Barreto, and D. S. Oliveira Jr, "Interleaved-boost converter with high voltage gain," *Power Electronics, IEEE Transactions on*, vol. 25, no. 11, pp. 2753–2761, 2010.

[66] T.-J. Liang, S.-M. Chen, L.-S. Yang, J.-F. Chen, and A. Ioinovici, "Ultra-large gain step-up switched-capacitor dc-dc converter with coupled inductor for alternative sources of energy," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 59, no. 4, pp. 864–874, 2012.

[67] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC-DC PWM converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 2, pp. 687–696, 2008.

[68] D. Meneses, F. Blaabjerg, O. Garcia, and J. A. Cobos, "Review and comparison of step-up transformerless topologies for photovoltaic ac-module application," *Power Electronics, IEEE Transactions on*, vol. 28, no. 6, pp. 2649–2663, 2013.

[69] D. Maksimović and S. Ćuk, "Switching converters with wide dc conversion range," *Power Electronics, IEEE Transactions on*, vol. 6, no. 1, pp. 151–157, 1991.

[70] D. S. Wijeratne and G. Moschopoulos, "Quadratic power conversion for power electronics: principles and circuits," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 59, no. 2, pp. 426–438, 2012.

[71] Y. De Novaes, A. Rufer, and I. Barbi, "A new quadratic, three-level, dc/dc converter suitable for fuel cell applications," in *Power Conversion Conference-Nagoya, 2007. PCC'07*, pp. 601–607, IEEE, 2007.

[72] P. Yang, J. Xu, G. Zhou, and S. Zhang, "A new quadratic boost converter with high voltage step-up ratio and reduced voltage stress," in *Power Electronics and Motion Control Conference (IPEMC), 2012 7th International*, vol. 2, pp. 1164–1168, IEEE, 2012.

[73] A. M. Andrade, R. C. Beltrame, L. Schuch, M. da S, and L. MaÃÅrio, "Integrated quadratic-boost-zeta converter for high voltage gain applications," in *Industry Applications (INDUSCON), 2014 11th IEEE/IAS International Conference on*, pp. 1–8, IEEE, 2014.

[74] K. Patidar and A. C. Umarikar, "High step-up converters based on quadratic boost converter for micro-inverter," *Electric Power Systems Research*, vol. 119, pp. 168–177, 2015.

[75] M. A. Al-Saffar, E. H. Ismail, and A. J. Sabzali, "Family of zc-zvs converters with wide voltage range for renewable energy systems," *Renewable energy*, vol. 56, pp. 32–43, 2013.

[76] R. Loera-Palomo and J. A. Morales-Saldaña, "Family of quadratic step-up dc–dc converters based on non-cascading structures," *Power Electronics, IET*, vol. 8, no. 5, pp. 793–801, 2015.

[77] Y. Lei and R. C. N. Pilawa-Podgurski, "Analysis of switched-capacitor dc-dc converters in soft-charging operation," in *Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on*, pp. 1–7, IEEE, 2013.

[78] D. Ma and R. Bondade, "Reconfigurable switched-capacitor power converters," in *Reconfigurable Switched-Capacitor Power Converters*, pp. 71–110, Springer, 2013.

[79] O. Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, "Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 50, no. 8, pp. 1098–1102, 2003.

[80] J. Sun, M. Xu, Y. Ying, and F. C. Lee, "High power density, high efficiency system two-stage power architecture for laptop computers," in *Power Electronics Specialists Conference, 2006. PESC'06. 37th IEEE*, pp. 1–7, IEEE, 2006.

[81] R. C. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converterarchitecture with softcharging switched-capacitor energy transfer," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, pp. 4008–4015, IEEE, 2008.

[82] Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-phase control: Achieving complete soft-charging operation of a dickson switched-capacitor converter," *Power Electronics, IEEE Transactions on*, vol. 31, no. 1, pp. 770–782, 2016.

[83] Y.-S. Lee, Y.-Y. Chiu, and M.-W. Cheng, "Zcs switched-capacitor bi-directional quasi-resonant converters," in *Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on*, vol. 2, pp. 866–871, IEEE, 2005.

[84] M. Shen, F. Z. Peng, and L. M. Tolbert, "Multilevel dc–dc power conversion system with multiple dc sources," *Power Electronics, IEEE Transactions on*, vol. 23, no. 1, pp. 420–426, 2008.

[85] D. Cao and F. Z. Peng, "Zero-current-switching multilevel modular switched-capacitor dc–dc converter," *Industry Applications, IEEE Transactions on*, vol. 46, no. 6, pp. 2536–2544, 2010.

[86] B. B. Macy, Y. Lei, and R. C. Pilawa-Podgurski, "A 1.2 mhz, 25 v to 100 v gan-based resonant dickson switched-capacitor converter with 1011 w/in3 (61.7 kw/l) power density," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, pp. 1472–1478, IEEE, 2015.

[87] J. Kwong, Y. K. Ramadass, N. Verma, and A. P. Chandrakasan, "A 65 nm sub-microcontroller with integrated sram and switched capacitor dc-dc converter," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 1, pp. 115–126, 2009.

[88] E. Bayer, "Optimized control of the" flying"-capacitor operating voltage in" gear-box"-charge-pumps-the key factor for a smooth operation," in *Power Electronics Specialist Conference, 2003. PESC'03. 2003 IEEE 34th Annual*, vol. 2, pp. 610–615, IEEE, 2003.

[89] W. Qian, D. Cao, J. G. Cintrón-Rivera, M. Gebben, D. Wey, and F. Z. Peng, "A switched-capacitor dc–dc converter with high voltage gain and reduced component rating and count," *Industry Applications, IEEE Transactions on*, vol. 48, no. 4, pp. 1397–1406, 2012.

[90] Y. Lei, W.-C. Liu, and R. C. Pilawa-Podgurski, "An analytical method to evaluate flying capacitor multilevel converters and hybrid switched-capacitor converters for large

voltage conversion ratios," in *Control and Modeling for Power Electronics (COMPEL), 2015 IEEE 16th Workshop on*, pp. 1–7, IEEE, 2015.

[91] F. Zhang, F. Z. Peng, and Z. Qian, "Study of the multilevel converters in dc-dc applications," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, vol. 2, pp. 1702–1706, IEEE, 2004.

[92] F. H. Khan and L. M. Tolbert, "A multilevel modular capacitor-clamped dc–dc converter," *IEEE Transactions on Industry Applications*, vol. 43, no. 6, pp. 1628–1638, 2007.

[93] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. De Novaes, "Isolated dc/dc structure based on modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 89–98, 2015.

[94] F. Z. Peng and F. Zhang, "A novel compact dc/dc converter for 42 v systems," in *Power Electronics in Transportation, 2002*, pp. 143–148, IEEE, 2002.

[95] A. Parastar, A. Gandomkar, and J.-K. Seok, "High-efficiency multilevel flying-capacitor dc/dc converter for distributed renewable energy systems," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7620–7630, 2015.

[96] B. Reznikov and A. Ruderman, "Six-level single-leg flying capacitor converter voltage balancing dynamics analysis," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2010 14th International*, pp. T2–7, IEEE, 2010.

[97] E. Deschamps and I. Barbi, "A flying-capacitor zvs pwm 1.5 kw dc-to-dc converter with half of the input voltage across the switches," *IEEE Transactions on Power Electronics*, vol. 15, no. 5, pp. 855–860, 2000.

[98] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, vol. 3, pp. 6–pp, IEEE, 2003.

[99] J. K. Reed, *Topology, modeling and analysis of bridge of bridge DC-AC and AC-DC power converters*.
PhD thesis, University of Wisconsin-Madison, 2014.

[100] J. A. Ferreira, "The multilevel modular dc converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4460–4465, 2013.

[101] Y. Li, X. Lyu, and D. Cao, "A high voltage gain modular multilevel dc-dc converter," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 3535–3541, IEEE, 2015.

[102] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded h-bridge multilevel pv inverter with distributed mppt for grid-connected applications," *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1722–1731, 2015.

[103] W. Zhao, H. Choi, G. Konstantinou, M. Ciobotaru, and V. G. Agelidis, "Cascaded h-bridge multilevel converter for large-scale pv grid-integration with isolated dc-dc stage," in *2012 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 849–856, IEEE, 2012.

[104] H. Choi, M. Ciobotaru, and V. G. Agelidis, "Cascaded h-bridge converter with multiphase isolated dc/dc converter for large-scale pv system," in *Industrial Technology (ICIT), 2014 IEEE International Conference on*, pp. 455–461, IEEE, 2014.

[105] H. Sepahvand, J. Liao, M. Ferdowsi, and K. A. Corzine, "Capacitor voltage regulation in single-dc-source cascaded h-bridge multilevel converters using phase-shift modulation," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 9, pp. 3619–3626, 2013.

[106] J. Napoles, A. J. Watson, J. J. Padilla, J. I. Leon, L. G. Franquelo, P. W. Wheeler, and M. A. Aguirre, "Selective harmonic mitigation technique for cascaded h-bridge converters with nonequal dc link voltages," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 1963–1971, 2013.

[107] N. Tesla, "Experiments with alternate currents of very high frequency and their application to methods of artificial illumination," *Trans. Am. Soc. Agric. Eng*, vol. 8, no. 1, pp. 267–319, 1891.

[108] T. C. Martin, *The inventions, researches and writings of Nikola Tesla*. Ripol Classic, 1894.

[109] R. Bosshard and J. W. Kolar, "All-sic 9.5 kw/dm 3 on-board power electronics for 50 kw/85 khz automotive ipt system," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 419–431, 2017.

[110] S. Y. R. Hui, W. Zhong, and C. K. Lee, "A critical review of recent progress in mid-range wireless power transfer," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4500–4511, 2014.

[111] J. Dai and D. C. Ludois, "A survey of wireless power transfer and a critical comparison of inductive and capacitive coupling for small gap applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6017–6029, 2015.

[112] M. Kline, I. Izyumin, B. Boser, and S. Sanders, "Capacitive power transfer for contactless charging," in *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, pp. 1398–1404, IEEE, 2011.

[113] D. C. Ludois, J. K. Reed, and K. Hanson, "Capacitive power transfer for rotor field current in synchronous machines," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4638–4645, 2012.

[114] J. Dai, S. S. Hagen, and D. C. Ludois, "Linear motion system cable elimination via multiphase capacitive power transfer through sliding journal bearings," in *Applied Power Electronics Conference and Exposition (APEC), 2017 IEEE*, pp. 2157–2164, IEEE, 2017.

[115] J. Dai and D. C. Ludois, "Capacitive power transfer through a conformal bumper for electric vehicle charging," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 1015–1025, 2016.

[116] K. Ichikawa and H. Bondar, "Power transfer system and noncontact charging device," Dec. 2016.
US Patent 9,300,135.

[117] C. Liu, *Fundamental study on capacitively coupled contactless power transfer technology*. PhD thesis, ResearchSpace@ Auckland, 2011.

[118] J. Dai and D. C. Ludois, "Single active switch power electronics for kilowatt scale capacitive power transfer," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 1, pp. 315–323, 2015.

[119] D. Salomonsson, L. Soder, and A. Sannino, "Protection of low-voltage dc microgrids," *IEEE Transactions on Power Delivery*, vol. 24, no. 3, pp. 1045–1053, 2009.

[120] J.-D. Park and J. Candelaria, "Fault detection and isolation in low-voltage dc-bus microgrid system," *IEEE transactions on power delivery*, vol. 28, no. 2, pp. 779–787, 2013.

[121] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "Dc microgrids‚Äîpart ii: A review of power architectures, applications, and standardization issues," *IEEE transactions on power electronics*, vol. 31, no. 5, pp. 3528–3549, 2016.

[122] S. A. Gopalan, V. Sreeram, and H. H. Iu, "A review of coordination strategies and protection schemes for microgrids," *Renewable and Sustainable Energy Reviews*, vol. 32, pp. 222–228, 2014.

[123] A. Qawasmi, N. Soltau, R. W. De Doncker, M. Heidemann, G. Nikolic, and A. Schnettler, "A comparison of circuit breaker technologies for medium voltage direct current distribution networks," in *Transmission & Distribution Conference and Exposition-Latin America (PES T&D-LA), 2016 IEEE PES*, pp. 1–6, IEEE, 2016.

[124] B. Pauli, G. Mauthe, E. Ruoss, G. Ecklin, J. Porter, and J. Vithayathil, "Development of a high current hvdc circuit breaker with fast fault clearing capability," *IEEE Transactions on Power Delivery*, vol. 3, no. 4, pp. 2072–2080, 1988.

[125] T. Mönnich and T. Rummel, "Protection system for the superconducting coils in wendelstein 7-x," *Fusion engineering and design*, vol. 66, pp. 1041–1044, 2003.

[126] Z. J. Shen, Z. Miao, and A. M. Roshandeh, "Solid state circuit breakers for dc micrgrids: Current status and future trends," in *DC Microgrids (ICDCM), 2015 IEEE First International Conference on*, pp. 228–233, IEEE, 2015.

[127] A. Abramovitz, M. Smedley, *et al.*, "Survey of solid-state fault current limiters," *IEEE Transactions on power electronics*, vol. 27, no. 6, pp. 2770–2782, 2012.

[128] K. Sano and M. Takasaki, "A surgeless solid-state dc circuit breaker for voltage-source-converter-based hvdc systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 4, pp. 2690–2699, 2014.

[129] C. M. Franck, "Hvdc circuit breakers: A review identifying future research needs," *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 998–1007, 2011.

[130] A. Shukla and G. D. Demetriades, "A survey on hybrid circuit-breaker topologies," *IEEE Transactions on Power Delivery*, vol. 30, no. 2, pp. 627–641, 2015.

[131] W. Zhou, X. Wei, S. Zhang, G. Tang, Z. He, J. Zheng, Y. Dan, and C. Gao, "Development and test of a 200kv full-bridge based hybrid hvdc breaker," in *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*, pp. 1–7, IEEE, 2015.

[132] M. A. Briere, "Gan based power devices: Cost-effective revolutionary performance," *Power Electronics Europe*, no. 7, pp. 29–31, 2008.

[133] D. J. Costinett, *Analysis and Design of High Efficiency , High Conversion Ratio , DC-DC Power Converters*.
PhD thesis, University of Colorado, 2013.

[134] M. A. Bahmani, *Design and Optimization Considerations of Medium-Frequency Power Transformers in High-Power DC-DC Applications*.
PhD thesis, Chalmers University of Technology, 2016.

[135] R. M. Zwicker, "Generation of multiple isolated bias rails for igbt inverters using flyback/sepic/cuk combination," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, pp. 1–8, VDE, 2014.

[136] C. Vartak, A. Abramovitz, and K. M. Smedley, "Analysis and design of energy regenerative snubber for transformer isolated converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 6030–6040, 2014.

[137] S. Falcones, R. Ayyanar, and X. Mao, "A dc–dc multiport-converter-based solid-state transformer integrating distributed generation and storage," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2192–2203, 2013.

[138] R. W. Erickson and D. Maksimovic, "A multiple-winding magnetics model having directly measurable parameters," in *Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE*, vol. 2, pp. 1472–1478, IEEE, 1998.

[139] G. Xiao-ying, L. Wei, C. Tai-qiang, L. Jia-hui, and L. Qian, "Independent regulation of multiple output flyback converter with pulse-train control," *International Journal of Control and Automation*, vol. 9, no. 1, pp. 55–62, 2016.

[140] Y. Xi and P. K. Jain, "A forward converter topology with independently and precisely regulated multiple outputs," *IEEE Transactions on Power Electronics*, vol. 18, no. 2, pp. 648–658, 2003.

[141] Y. Chen and Y. Kang, "A fully regulated dual-output dc–dc converter with special-connected two transformers (sctts) cell and complementary pulsewidth modulation–pfm (cpwm-pfm)," *IEEE Transactions on Power Electronics*, vol. 25, no. 5, pp. 1296–1309, 2010.

[142] S.-H. Cho, C.-S. Kim, and S.-K. Han, "High-efficiency and low-cost tightly regulated dual-output resonant converter," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2982–2991, 2012.

[143] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch - II: Discontinuous conduction mode," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 26, no. 3, pp. 497–505, 1990.

[144] J. Sun, D. M. Mitchell, M. M. E. Greuel, P. T. Krein, and R. M. Bass, "Modeling of PWM converters in discontinuous conduction mode. A reexamination," *PESC Record - IEEE Annual Power Electronics Specialists Conference*, vol. 1, no. 4, pp. 615–622, 1998.

[145] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *Power Electronics Specialists Conference, 1976 IEEE*, pp. 18–34, IEEE, 1976.

[146] I. Batarseh and K. Siri, "Generalized approach to the small signal modelling of dc-to-dc resonant converters," *IEEE transactions on aerospace and electronic systems*, vol. 29, no. 3, pp. 894–909, 1993.

[147] G. D. Demetriades, *On small-signal analysis and control of the single-and the dual-active bridge topologies*.
PhD thesis, KTH Royal Institute of Technology, 2005.

[148] H. Bai, C. Mi, C. Wang, and S. Gargies, "The dynamic model and hybrid phase-shift control of a dual-active-bridge converter," in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, pp. 2840–2845, IEEE, 2008.

[149] A. R. Alonso, J. Sebastian, D. G. Lamar, M. M. Hernando, and A. Vazquez, "An overall study of a dual active bridge for bidirectional dc/dc conversion," in *2010 IEEE Energy Conversion Congress and Exposition*, pp. 1129–1135, IEEE, 2010.

[150] D. J. Packard, *Discrete modeling and analysis of switching regulators*.
PhD thesis, California Institute of Technology, 1976.

[151] A. R. Brown, "Sampled-data modeling of switching regulators," in *Power Electronics Specialists Conference, 1981 IEEE*, pp. 349–369, IEEE, 1981.

[152] P. A. Mendoza-Arraya, *Impedance matching based stability criteria for AC microgrids*.
PhD thesis, University of Wisconsin-Madison, 2014.

[153] H. Qin and J. W. Kimball, "Generalized average modeling of dual active bridge DC-DC converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 2078–2084, 2012.

[154] H. Qin and J. W. Kimball, "Closed-loop control of dc–dc dual-active-bridge converters driving single-phase inverters," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 1006–1017, 2014.

[155] J. Ho, R. Jow, and S. Boggs, "Historical introduction to capacitor technology," *IEEE Electrical Insulation Magazine*, vol. 1, no. 26, pp. 20–25, 2010.

[156] J. Both, "Electrolytic capacitors, 1890 to 1925: early history and basic principle," *IEEE Electrical Insulation Magazine*, vol. 31, no. 1, pp. 22–29, 2015.

[157] J. B. Elcap, "Overview over the most commonly used fixed capacitors in electronic equipment," 2014.
[Online; accessed 05-Dec-2016].

[158] D. McLean and H. Wehe, "Miniature lacquer film capacitors," *Proceedings of the IRE*, vol. 42, no. 12, pp. 1799–1805, 1954.

[159] P. Venet, "Electrolytic capacitors," *Dielectric Materials for Electrical Engineering*, pp. 403–434.

[160] Wima, "Characteristics of metallized film capacitors in comparison with other dielectrics," 2016.
[Online; accessed 22-Dec-2016].

[161] H. stone capacitors, "Capacitor dielectric comparison," 2016.
[Online; accessed 22-Dec-2016].

[162] AVX, "Dielectric comparison chart," 2016.
[Online; accessed 22-Dec-2016].

[163] J. B. Elcap, "Dielectric strength," 2016.
[Online; accessed 21-October-2016].

[164] J. B. Elcap, "Capacitance vs voltage range," 2016.
[Online; accessed 21-October-2016].

[165] Kemet, "Introduction to capacitor technologies," 2013.
[Online; accessed 21-Dec-2016].

[166] "Fixed capacitors for use in electronic equipment - Part 8: Sectional specification: Fixed capacitors of ceramic dielectric, Class 1," standard, International Electrotechnical Commission, Geneva, CH, 2015.

[167] "Fixed capacitors for use in electronic equipment - Part 9: Sectional specification: Fixed capacitors of ceramic dielectric, Class 2," standard, International Electrotechnical Commission, Geneva, CH, 2015.

[168] W. contributors, “Ceramic capacitor — wikipedia, the free encyclopedia,” 2016. [Online; accessed 16-December-2016].

[169] M. Fortunato, “Temperature and voltage variation of ceramic capacitors, or why your 4.7uf capacitor becomes a 0.33uf capacitor,” 2016. [Online; accessed 23-Dec-2016].

[170] F. Janssen, “How to measure capacity versus bias voltage on mlccs,” 2016. [Online; accessed 23-Dec-2016].

[171] S. M. Components, “Ceramic capacitors,” 2016. [Online; accessed 21-Dec-2016].

[172] J. B. Elcap, “Ceramic capacitor — wikipedia, the free encyclopedia,” 2016. [Online; accessed 16-December-2016].

[173] Kemet, “Ceramic capacitors,” 2016. [Online; accessed 21-Dec-2016].

[174] V. Draloric, “Ceramic capacitors,” 2016. [Online; accessed 21-Dec-2016].

[175] W. contributors, “Film capacitor — wikipedia, the free encyclopedia,” 2016. [Online; accessed 26-December-2016].

[176] R. W. Brown, “Linking corrosion and catastrophic failure in low-power metallized polypropylene capacitors,” *IEEE Transactions on Device and Materials Reliability*, vol. 6, no. 2, pp. 326–333, 2006.

[177] M. El-Husseini, P. Venet, A. Al-Majid, M. Fathallah, G. Rojat, and J. Ferreira, “Manufacturing technology effect on current pulse handling performance of metallized polypropylene film capacitors,” *Journal of Physics D: Applied Physics*, vol. 36, no. 18, p. 2295, 2003.

[178] W. contributors, “Electrolytic capacitor — wikipedia, the free encyclopedia,” 2016. [Online; accessed 26-December-2016].

[179] J. Both, “Electrolytic capacitors from the postwar period to the present,” *IEEE Electrical Insulation Magazine*, vol. 32, no. 2, pp. 8–26, 2016.

[180] J. Both, “The modern era of aluminum electrolytic capacitors,” *IEEE Electrical Insulation Magazine*, vol. 31, no. 4, pp. 24–34, 2015.

[181] D. Costinett, H. Nguyen, R. Zane, and D. Maksimovic, "GaN-FET based dual active bridge DC-DC converter," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 1425–1432, 2011.

[182] O. Djekic and M. Brkovic, "Synchronous rectifiers vs. schottky diodes in a buck topology for low voltage applications," in *Power Electronics Specialists Conference, 1997. PESC'97 Record., 28th Annual IEEE*, vol. 2, pp. 1374–1380, IEEE, 1997.

[183] H. P. S. Inc., "Transformer product catalog," 2017.
[Online; accessed 10-Apr-2018].

[184] N. F. P. Association, "National electrical code grounding and bonding," standard, 2016.

[185] "Electrical installations for buildings," standard, International Electrotechnical Commission, Geneva, CH, 2005.

[186] IEEE, "Ieee recommended practice for grounding of industrial and commercial power systems," standard, 2007.

[187] R. M. Fish and L. A. Geddes, "Conduction of electrical current to and through the human body: a review," *Eplasty*, vol. 9, 2009.

[188] W. contributors, "Electrical injury — wikipedia, the free encyclopedia," 2018.
[Online; accessed 22-Apr-2018].

[189] I. A. of Electrical Inspectors, *Soares Book on Grounding and Bonding*.
International Association of Electrical Inspectors, 2017.

[190] B. Ge, A. N. Ghule, and D. C. Ludois, "Three-dimensional printed fluid-filled electrostatic rotating machine designed with conformal mapping methods," *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4348–4359, 2017.

[191] I. C. Kobougias and E. C. Tatakis, "Optimal design of a half-wave cockcroft–walton voltage multiplier with minimum total capacitance," *IEEE transactions on Power Electronics*, vol. 25, no. 9, pp. 2460–2468, 2010.

[192] A. Lamantia, P. G. Maranesi, and L. Radrizzani, "Small-signal model of the cockcroft-walton voltage multiplier," *IEEE transactions on power electronics*, vol. 9, no. 1, pp. 18–25, 1994.

[193] S. Iqbal, "A hybrid symmetrical voltage multiplier," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 6–12, 2014.