Study of Nanofabrication, High Power, and Biodegradable Flexible Electronics

By

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To My Family

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Abstract

In this thesis, the approaches of nanofabrication schematics, fast flexible electronics, and biodegradable flexible electronics have been explored. The current challenges has been identified and addressed, and practical solutions have been proposed and demonstrated with supporting measurement results.

The first part of the thesis will cover challenges generated from the ambition to pursue better and faster electronics. The projection characteristic dimension (CD) of the next generation electronics from the well-known Moore's Law now locates at sub-10 nm features. The cost and the complexity to setup reliable lithography exposure process have grown exponentially as the manufacture techniques are facing the most fundamental physical limits. The alternative bottom-up approach, directed assembly based on block copolymer assembly, has emerged to compete with the next generation top-down approaches, i.e. extreme ultraviolet lithography (EUV) and multiple e-beam system. DSAs features many advantages, for example, potential extendable to 1-3nm application, compatible with top-down approach, quick assembly process, self-healing, but also face issues in further extending its fabrication into sub-10 nm. As the feature size becomes smaller, the unavoidable thickness of the chemical template becomes compatible with the molecular size of the block copolymer and begins to increase the defects of the assembly pattern. Here, we introduce novel 2D material, graphene, which is the thinnest material identified to replace the polymer based chemical pattern used in DSAs. The smooth topology of the graphene surface replace the traditional PS based chemical pattern without interrupting the assemble behavior. DSA on graphene chemical based pattern shows almost every aspect in terms

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Besides the evolution of electronics into smaller feature sizes, a new research field, flexible electronics, quickly finds its unique role in the community. From the simply passive radio frequency identification (RFID) tags used in billing, locating, and wrists access to those more complicated skin tag monitor system, brain implant sensor, and artificial human skin, flexible electronics are rapidly penetrating into everyday life because of their convenient functions. However, current existing flexible electronics are usually based on passive elements or those materials that have only moderate to poor electronic properties. Lacking of high performance elements, for example power amplifier, HEMTs, HBTs, greatly limit the application of the flexible electronics. For III-V materials characterized as high performance materials, a reliable way to embed the materials into flexible electronics is still under investigating. In addition, active elements, such as AlGaN/GaN HEMTs, usually generate a lot of heat during operation and quickly dissipate on the rigid substrate. On the flexible substrate, due to the limited thermal budget, these high power electronics would either be forced to operate at high temperature or burned together with low-heat-tolerant flexible substrates. The second part of the thesis introduces the technique of releasing a large area and high transparent GaN membrane to a flexible substrate. The thin film of highly transparent GaN membranes not only enables the highest transparent heat dissipation layer on the flexible substrate, but the AlGaN/GaN fabricated on top of it also exhibits comparable performance with respect to its rigid form. To our surprise,

the radio frequency characteristic of the HEMTs after being transferred to the flexible substrate is further improved. A follow-up simulation explains the process of removing bottom substrate minoring the loss of the device and the well heat control preventing degradation of the device performance.

With the capability of incorporating high performance electronics into flexible substrate, I will step backwards in this chapter to reexamine the impact of the constantly remodeled electronics to our environment. Annually, millions of tons of personal electronics are discarded and the majority of them will end up in incinerators and landfills. The e-waste occupies millions of cubic meters of the volume, with a large fraction of it comprised of packaging materials. Due to the petroleum product nature, e-waste takes an extremely long time to degrade and enter the natural carbon cycle. The cost of processing the e-waste is rapidly climbing and demand valuable landfill to accomplish. Here, the Carbon Nano cellulose (CNF) substrate, a product from renewable resources such as wood, as the source of flexible substrate is adapted and demonstrate the feasibility of high performance flexible electronics with disposability. CNF film can be made transparent as the strong light interference from the cellulose of the wood dissociates into the nanometer range. Electronics behave functionally on the CNF film can be easily discarded by biodegradation. The brown fungi, abundant in wild life, can digest and consume the packaging of the CNF film and recycle all the materials. 99.8% of the flexible electronics can be recycled and the small non-biodegradable fraction left over has minimum environmental impact. Next generation green electronics are highly promising in its performance and post usage recyclability.

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Chapter 1 Introduction

For the past decade, the goal of pursuing electronics with better performance has changed sharply. Instead of simply reducing the feature size of the electronics for better performance, the development of electronics have quickly spread into different fields, including renewable electronics, flexible electronics, and hybrid electronics. The emergence of 2D materials greatly deviates from the predictions of next generation electronics. The marvelous properties of 2D materials have immediately made breakthroughs in energy storage capacity, display, and even portable electronics. The breakthrough of fabricating large area and single crystal 2D materials has quickly eliminated any existing doubt about implanting 'so called' next generation techniques. 2D materials, as its name suggests, are compatible to be quickly adapted into the state of the art industry. Several wafer scale commercial products have been demonstrated by IBM, the world leading company, without transition issues. So far, attention is turned on using 2D materials as either an active or passive element of the final products. However, the potential of using 2D materials in improving the manufacturing process has still been lacking of attention.

Meanwhile, electronics waste has become a problem endangering both the environment and humans. At this very moment, waste the size of an island is still moving and growing somewhere in the Pacific Ocean. Current electronic products are made of more than 90% of packaging materials and only 10% of the volume is the actual computing elements. The petroleum based packaging materials can remain undegraded in the soil for thousands of years and cause the buildup of landfill. To minimize waste from devices, the goals of next generation electronics have been to make it flexible without excessive packaging and easy to dispose.

It has been long foreseen that traditional electronics will face the fundamental physical limits of photolithography tools as the feature size goes down to sub-10nm. The price of fabricating reliable source of excimer lasers and relative photoresists has dominated the production cost of the semiconductor manufacturers; the condition becomes even worse when the feature size of the chip step into the sub 10nm scale. Many new approaches have been addressed to replace the traditional lithography tools, for example, directed assembly of block copolymer over the lithography generated template, DSA. Many promising results have been published and industry have announced the production line based on DSA. Nevertheless, the polymer based chemical pattern face the same unsolvable fundamental issues, like spinning thickness and uniformity, and resistance to the permeability as the molecular weight of polymer becomes smaller.

In this dissertation, I will first talk about how the integration of 2D materials with its robust structures, atomically thin layer, and inert chemical properties will benefit next generation lithography techniques. And shows the promising assemble results of large area assembly with a lower requirement for lithography tools to reduce the fabrication cost and feasibility in generating sub-10nm feature. In the follow up session, a step in the breakthrough of non-performance sacrificing high power flexible electronics is demonstrated by the skills of transferring high quality single crystal membranes onto flexible electronics. By replacing the traditional polycrystalline or organic materials as the heat dissipating techniques with crystalline GaN membranes, the heat conducting problems are solved. With a similar thermal conductivity as the metal, totally transparent and the highly flexibility AlGaN/GaN HEMTs with improved RF performance on the flexible substrate has been first demonstrated.

In the last session, carbon cellulose fiber (CNF) substrate has been adapted to replace the petroleum based flexible substrate, PET. A 99.8% degradability has been demonstrated by the

integration of two important fabrication aspects: (1) replacing the most volume occupying packing materials with renewable CNF film from wood, and (2) the new transfer printing techniques in separation materials from handling substrate. The amount of toxic materials has been reduced to an environmentally safe value. The whole device is later degraded by the abundant fungi in nature as shown in a simulated buried disposal condition.

1.1 Basic properties of graphene

The non-existence of thermally stable 2D materials has been long discussed many of years ago[1]. The argument is later backed up by the observation of the melting point of the thinned down 3D materials[2]. It is generally recognized that due to the abrupt decrease in thermal stability, 2D materials will not exist unless it is integrated with 3D structures as its base[2]. Not until 2004 with the help of daily used scotch tape, a single layer of graphite, named graphene, was first peel off mechanically from its bulk 3D structures and remained stable after being printed on SiO_2 substrate[3]. The research in 2D materials rapidly spread out to numerous fields and more than 40 new family members in 2D materials have been discovered [4].

Graphene, the first member in 2D materials, consists of carbon atoms that are tightly packed in honeycomb-like lattice structures[5], where adjacent carbon atoms share a strong sigma bond (s-bond) in the planar direction and a weakly coupled π-bond in the z direction[6]. The latter electron is believed to contribute to the unique charge carriers in graphene and the charge carriers in graphene with mobility estimated up to 2×10^5 cm^2 V^{-1} s^{-1} and higher conductivity compares to copper[7]. This could be understood through its tight bonding simulation as shown in Figure 1.1[8, 9]. The conduction band and valence band touch at the so-called Dirac points where

the Fermi level crosses the touch point. This makes the graphene a zero bandgap material. Except for the zero bandgap property, the dispersion in graphene is linear at the direct point, which makes the calculation of the effective electron mass become zero after second order derivation, which is massless Dirac fermions[6]. The zero bandgap feature makes graphene become a metal-like material, the fermi level in graphene and band diagram of graphene is still adjustable[3, 5, 10]. In this way, graphene is generally considered a semi-metal-like material[11].

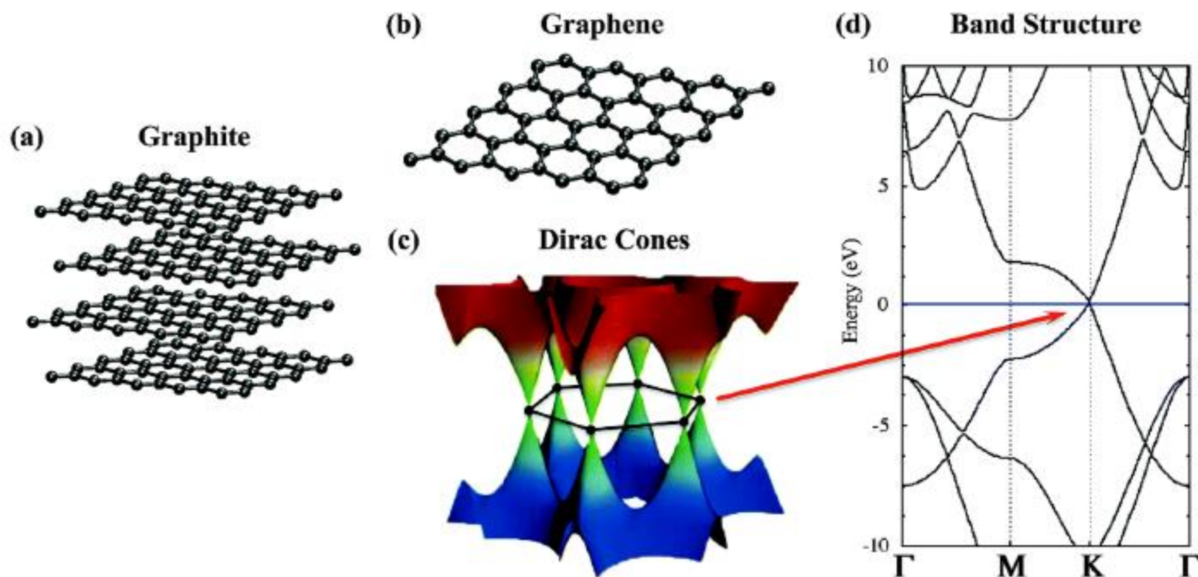

Figure 1.1 *Graphene, the prototype 2D material. (a) Graphite structure. (b) Graphene structure. (c) Dirac cones in graphene (d) Graphene band structure (G–M–K–G). Fermi level has been shifted to 0 eV and depicted with a blue horizontal line[9, 12].*

Other properties of graphene, including transparency[13], high thermal conductivity[14], and mechanical durability[15], have enabled graphene to be a great candidate material for utilization in flexible electronics. Recently, large area fabrication of graphene from chemical vapor deposition (CVD)[16] and solution-based graphene demonstrated the possibility of replacing rare indium tion

oxide (ITO)[17], a material used in display and flexible devices, with cheap and ambient carbon sources in which the favorable electrical properties of graphene could speed up the development of high performance flexible electronics.

Among most of the graphene applications, some applications that utilize the unique properties of graphene. For example, due to the nature of sp^2 carbon bonding in graphene, the electrons are strongly coupled in the planar direction, leaving π electron resonance between carbon atoms in the out-of-plane direction. This is the reason why layers in graphene are weakly coupled. By exploiting this feature, single crystal graphene grown on Ge wafer can be peeled off easily and the precious Ge can be reused[18]. Similar results extend to the growth and transfer of III-V materials[19]. No absurd physics is integrated into the fabrication process but greatly reduce the production cost of wafer scale single crystal graphene. In addition, the graphene has demonstrated in the application of high quality diodes with almost perfect schottky diode[20].

The uniqueness of 2D materials has enabled novel designs of next generation electronics that could improve or even generate distinct designs in both the fabrication process and electronic performance. Many genius approaches remain to be uncovered.

1.2 Nano-fabrication: From Top-Down to bottom up renovation

Different from the 2D materials that are still remaining on the research based applications, the semiconductor industry has been struggling to meet consumer needs for personal electronics with faster speed and larger storage space. The needs and expecatations in the consumer markets, Moore's Law that doubles the transistors every 18 months, has gradually exceeded the physical

limit of the methodology of devices by traditional photolithography. It is reported that state-of-the-art fabrication facilities cost as high as several billions of dollars and next generation extreme ultraviolet prototype tools cost at least $125 million. Top-Down approaches nowadays has run into fundamental bottlenecks with no easy solution. Alternative approaches that feature high resolutions, batch process capabilities, and low cost have been drawing significant attention over the last 10 years.

Among all the bottom-up approaches in making electronics, block copolymers (BCPs) feature facile assemble capabilities that assemble into a variety of morphologies including hexagonal cylinders, lamellae, sphere, etc. BCPs, as its name suggests, contain blocks of polymer with distinct polymer-to-polymer interaction parameters (χ)[21]. As demonstrated in Figure 1.2, raising the temperature or dissolving in solvent so that BCPs have more freedom of movement will rearrange BCPs and the polymer blocks will rearrange with polymers or surfaces that has similar interaction parameters and move away from those blocks that have opposite χ.

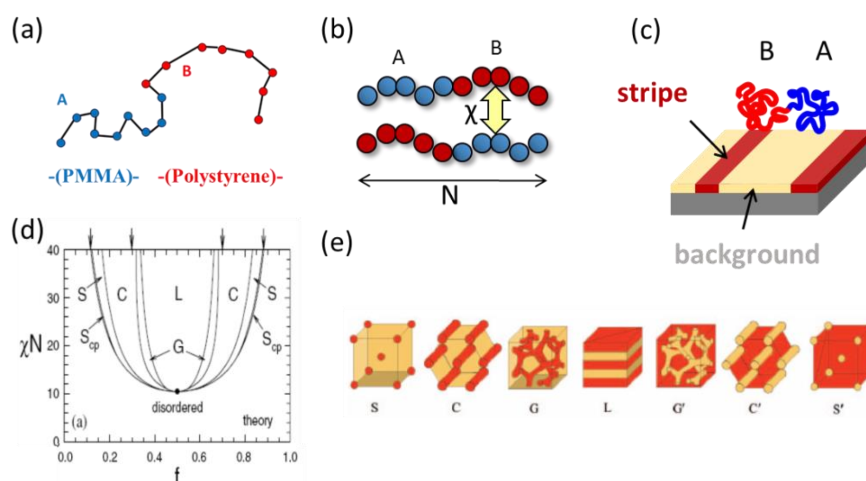

Figure 1.2 *Introduction of the block copolymer assembly (a) schematic of PS-b-PMMA di-block copolymer based on the polystyrene block and PMMA block (b) interaction factor χ and*

polymerization number N (c) interaction of each block to the grounding surface will prefer to stay at its lowest energy condition (d) assembly morphology chart and (e) corresponding assembly morphology result.[22, 23]

The size of the feature (usually called polymerization number N) can range from several nm to several hundred nm. Over the past few decades, the self-assembly of (BCP) thin films has attracted enormous research interest and many bottom-up electronics built from BCPs have been developed. For example, in Figure 1.3a, a 20-inch wafer scale 29nm-pitch side silicon with compatible performance has been demonstrated.

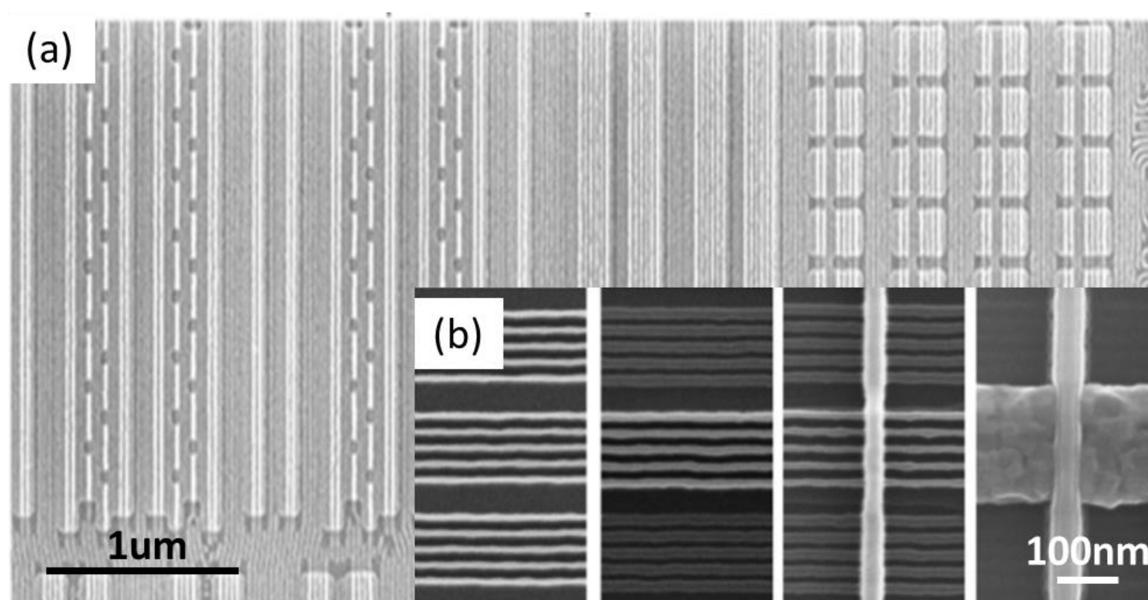

Figure 1.3 *BCP enables electronics 20 inches wafer scale 29nm-pitch size Si FinFET (2014). (a) sem image of wafer scale 29nm Si nano-Fin structure from DSA (b) fabrication process of the Si FinFET*[24]*.*

One of the most appealing characteristics of the BCPS is the capability of forming a directed self-assembly pattern, a connection of the bottom-up technique to top-down technique. In this method, the assembly of the pattern can be guided with the pre-processing that makes the originally random assembly process controllable. Directed self-assembly of block copolymer films is possible when the films are assembled over pre-processed handling substrates that are covered with geographical structures[25], and lithography defined chemical patterns[22, 23, 26]. With the underlying patterns on the substrates, not only can large area ordered patterns be achieved, but also improve the line edge roughness[27], multiplied sparse patterns[22, 28], and self-healing of defeat-patterns[29]. Here, we will focus on the directed assembly of BCP over the pre-patterned chemical pattern. Figure 1.4 shows the standard (LiNe) schematic of the directed assembly of BCP over the pre-patterned chemical pattern. The most commonly used PS-b-PMMA based BCPs are referred to below.

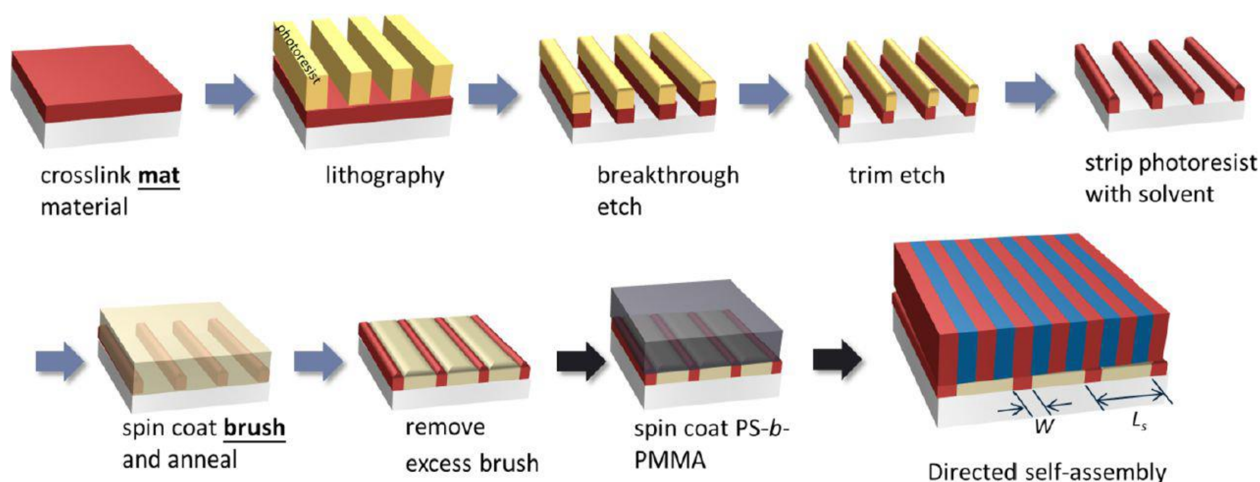

Figure 1.4 *Schematic of the (LiNe) fabrication process of the chemically patterned substrates and the directed assembly of PS-b-PMMA with density multiplication.*[30].

In the directed assembly of BCP, the chemical contrast surface is prepared before assembly. To prepare the chemical pattern, the first layer of polystyrene (PS) (with interaction parameters similar to the PS block) with cross-linkable agent is cast on the substrate surface. The cross-linkable agent is activated through thermal annealing. After the crosslinking process, the chemical resistance and stability of the PS chemical pattern are enhanced and become invulnerable to the latter fabrication process. In order to generate the regulated pattern, a lithographic process is required on the PS enhanced substrate to define the PS strips into regular pattern, called guiding strips, for example, lamellae shape PS guiding strips (Figure 1.4). The advantage of BCP assembly is their ability to assemble over the sparse chemical pattern. As long as the surface in between the PS strips remain neutral to both the blocks of the BCPS, the BCPs can still form a regular pattern over sparsely defined chemical patterns.

1.3 High Performance Fast Flexible Electronics

Flexible electronics, contrary to its rigid form, have changed the way that humans are living quickly and abruptly over the past decade[31]. Imagine in less than 10 years, instead of having a heavy and awkward sensor that is constantly dropped from the front window of a car, drivers can apply a thin and transparent RFID tag in order to access the toll way. The thickness, flexibility, and transparent nature of the tag make installation user-friendly and the drivers will not sense the mounted tag while driving. Although flexible electronics can be incorporated into many applications, for example flexible solar cell, flexible organic LED, or the identification tag, the need for high performance flexible electronics remain the main driving force in the research of

the flexible electronics. Departing from traditional flexible electronics that either used amorphous Si, polycrystalline Si, or organic materials[32], the need for integrating high quality monocrystalline nanomembranes (NMs) into flexible electronics have emerged[33].

Single crystal NMs exhibit far better electronic properties than non-crystalline materials, even though the thickness is less than a few micrometers. It is usually grown or prepared on a rigid substrate and requires additional processes to separate and release it. The most well-known process is the PDMS releasing and printing process[34]. In general, single crystal NMs are embedded on top of the bulk wafer with the sacrificial layer in between. The sacrificial layer can be oxide, or III-V epi-layer that is vulnerable to certain chemicals but not the NM itself. For example, silicon on insulators (SOIs from SmartCut@ techniques[35]) have constantly been used to as a source wafer to release and print Si NMs. Single crystal NMs can become suspended and released when the sacrificial layer is removed through wet etching methods. Once the NMs are released, PDMS stamps are appliedto the NMs to pick up the NMs for the later process.

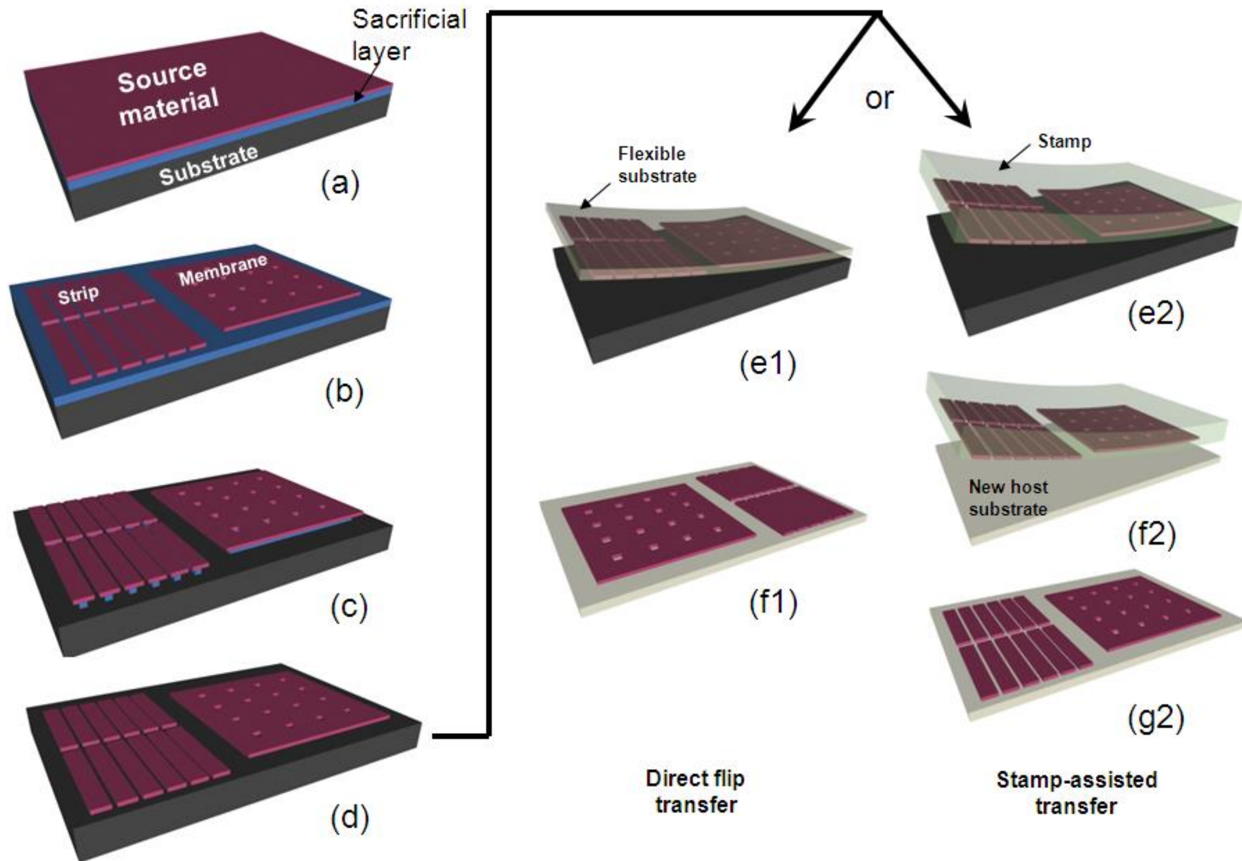

Figure 1.5 *General process illustration for crystalline semiconductor membrane release, transfer and stacking. (a) Begin with source material (e.g., SOI, GeOI, III-V multi layers with a sacrificial layer). Metallization can be applied here, if needed. (b) Pattern top layer into membrane (or strip forms) down to the sacrificial layer. (c) Release membrane by undercutting the sacrificial layer. (d) Fully released membrane settles down on the handling substrate via van der Waals force ("in-place bonding"). Direct flip transfer: (e1). Apply glue on host (e.g., flexible) substrate and attach it to the handling substrate. (f1) Lift-up the host substrate and flip to complete the transfer. Glue can be dissolved if needed. Stamp-assisted transfer: (e2) Bring a stamp (e.g., Polydimethylsiloxane, or PDMS) toward the handling substrate, press and lift-up. (f2) Apply the stamp with membrane attached to a new host substrate (which can be coated with glue, but not necessary). (g2) Slowly peel off the stamp or remove the stamp with shear force,*

leaving the membrane to stay on the new host substrate. Multiple layers can be applied by repeating (a)-(f1) or (a)-(g2)[36].

Besides the sacrificial based releasing transfer methods that usually use expensive SOI wafers, some alternative approaches have been discussed to lower the production cost and enable large batch fabrication, including anisotropic wet etching methods[37] and XeF2 gas based wafer scale releasing methods[38]. These approaches feature the capability of reusing the source handling wafer to reduce the production cost. Both are also compatible with the PDMS transfer printing technique.

Based on transfer printed NMs on flexible substrates, fast flexible electronics with record speed RF performances are achieved yearly. This is owing to the high electron mobility in single crystalline semiconductors. Though the first steps of single crystal NM- based flexible electronics start much later than the traditional flexible electronics, the substantial performance process has been announced yearly. The timeline of the development of the high performance Si flexible electronics is shown in Figure 1.6. The performance of fast flexible transistors quickly advanced to 12 GHz maximum oscillation frequency (*fmax*) by integrating 1μm channel alignment for the Si-NMs on a soft plastic substrate, and further increased to 15GHz by strain engineering based on strained Si/SiGe/Si-NMs[39].

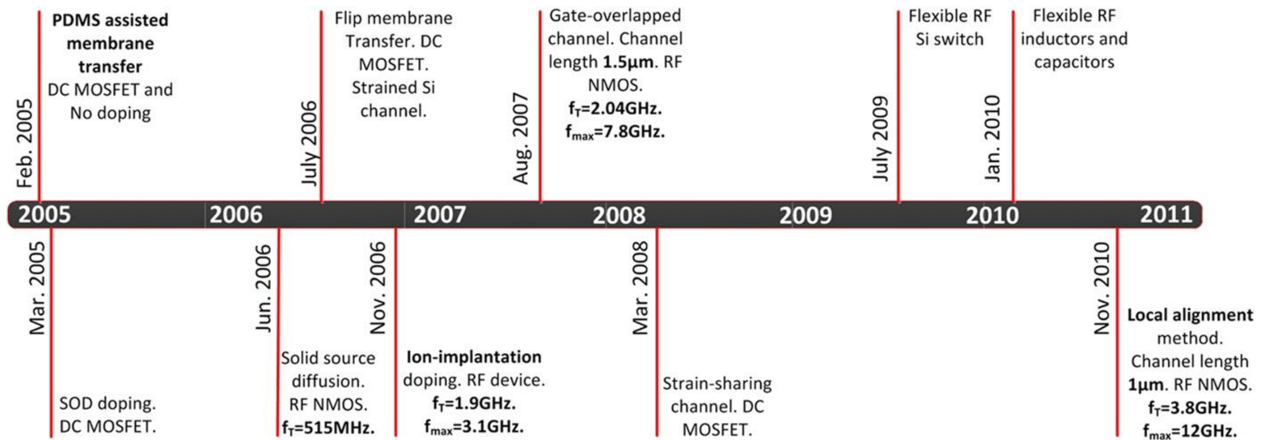

Figure 1.6 *A short development history of flexible RF active devices (and related passive devices) on plastic substrates using transferrable Si NMs*[33].

So far, the development of fast flexible electronics is based on Si and Ge (IV group) field effect transistors, which amplify the small signal. Instead of a small signal, many applications require the device to load higher current, as inwireless transmission, signal amplification, single processing, and multifunction electronics. For example, the signal extracted from flexible brain sensor would usually be several mV, which cannot be detected unless further amplified. In order to extract and harvest useful signals, power element devices that are generally used to amplify the small signal to analyzable levels are needed. However, these power devices, the heart in driving the application of flexible electronics, usually require carrying large current, as in bipolar junction transistors (BJTs), heterojunction transistors (HBTs), and high electron mobility transistors (HEMTS). With the PDMS printing transfer techniques, many of them have been demonstrated already. However, with large amounts of current flowing inside the device channels, the heat generated in flexible substrate cannot be easily removed as they are in the rigid substrates and a significant amount of performance degradation has been reported[40].

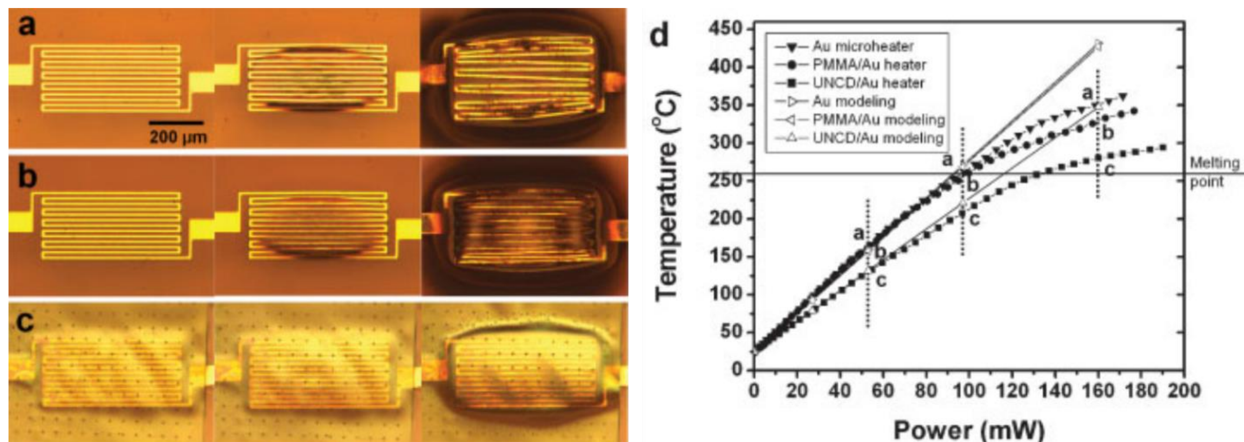

Figure 1.7 *Optical microscopy images of serpentine microheaters on plastic substrates collected at applied powers of 53 mW, 97 mW, and 160 mW, for the case of heaters a) exposed to air, b) coated with a thin (600 nm) spin-cast layer of PMMA, and c) covered with a printed thin (400 nm) platelet of diamond. d) Average heater temperatures from experiment and from finite element modeling as a function of applied power for these three different samples*[41].

In Figure 1.7, heat dissipation over the plastic has been discussed. From the experiment, even by adapting ultra nano crystalline diamond (UNCDs), temperature of the flexible substrate still quickly rises over the melting point at 260°C of the flexible substrate. Though, the UNCDS partially spread out the heat and the robust melting point of diamonds, preventing the devices from directly melting with the bottom substrate. 160mW power tolerance is still far from the generally required power of 1W. Moreover, due to the limit of heat control, reliable and repeatable power electronics have not yet be reported without sacrificing the performance on the flexible substrate. Hence, the research and design of solving the heal management issues on the flexible electronics have been identified as the requirement to realize the high performance flexible electronics.

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Chapter 2 Improve Block Copolymer Based Nanofabrication with 2D Materials

The feature size of the semiconductor electronics has formally entered sub-10nm. Photolithography based exposure tools have faced physical limit because of the inevitable light interference effect. Directed self-assembly of block copolymers is a scalable method to fabricate defect-free and well-ordered patterns with sub-10 nm feature size over the wafer scale. In chemoepitaxy, lithographically-defined patterns with varying chemical contrast are used to rationally guide assembly. However, the non-negligible surface topography of conventional chemical patterns and the relatively limited conditions under which they can be processed pose challenges to directed self-assembly.

In this chapter, we demonstrate that an atomically-thin layer of graphene on germanium can direct the assembly of polystyrene-block-poly(methyl methacrylate). Faster assembly dynamics are observed on graphene guiding stripes than on conventional polystyrene based chemical patterns. The block copolymer compresses to 15% and stretches to 13% to match the periodicity of the pattern and 90° bends are fabricated. We also demonstrate density multiplication by a factor of 10, enhancing the pattern resolution compared to the periodicity of the guiding stripes, and lamellae with half-pitch of 12.5 nm are achieved. This implies 10 times in reduction the exposure time in the sub-10nm fabrication. The minimal topography and broad processing window provided by this robust graphene chemical pattern will improve the fidelity and reproducibility of high-resolution patterns for industrial nanoscale manufacturing.

2.1 Introduction

The phase separation of block copolymers can yield patterns with various morphologies and feature sizes ranging from 5 to 100 nm[1]. In order to take advantage of phase separation for lithographic nanopatterning, block copolymer assembly can be rationally guided using pre-defined templates. For example, defect-free and well-registered block copolymer domains can be created using patterned topographic features, known as graphoepitaxy[2], or using patterned regions of varying chemical contrast[3-7], known as chemoepitaxy. Directed self-assembly can also improve the line-edge roughness of the lithographically-defined template[8], correct defects in the underlying template via a self-healing mechanism[9], and enhance the pattern resolution compared to the periodicity of the template via density multiplication[7, 10].

The Liu-Nealey (LiNe) flow is a paradigm of chemoepitaxy, as it seamlessly integrates with state-of-the-art 193 nm immersion lithography[11]. Cross-linkable polystyrene (X-PS) based chemical patterns are commonly used in the LiNe flow because the X-PS preferentially wets the polystyrene (PS) domains in the widely studied polystyrene-block-poly(methyl methacrylate) (PS-*b*-PMMA) system[12]. After the X-PS mat (6-8 nm in thickness) is patterned to form line-space arrays, the guiding stripes are typically trimmed with a plasma etch and then a random copolymer brush with hydroxyl groups is grafted into the void spaces between the guiding lines. This process, known as backfilling, renders the void area neutral to both polymer domains in PS-*b*-PMMA and reduces the step height of the chemical pattern[12].

However, these processing steps can increase the difficulty of performing directed self-assembly on organic chemical patterns. For example, during plasma trimming, the sidewalls of the X-PS stripes can become oxidized, which makes them reactive toward the brush, and

subsequently changes the wetting behavior and alters the geometry of the guiding lines[13]. As the size of the block copolymer domains decreases, the physical dimension of the guiding line become especially critical to ensure defect-free assembly. Even with backfilling, the step height between the X-PS stripes and neutral brush region is still > 3 nm[12]. The topology of prepared surface is shown in Figure 2.1.

This non-negligible topography disrupts block copolymer assembly, leading to the formation of trapped defects in the lamellae patterns[14]. Moreover, the grafted brush layer can cause interdigitation of the polymer chains with the random copolymer brush, decreasing their diffusivity and resulting in slowed assembly dynamics and impeded formation of well-ordered patterns during nucleation of the block copolymer domains[15].

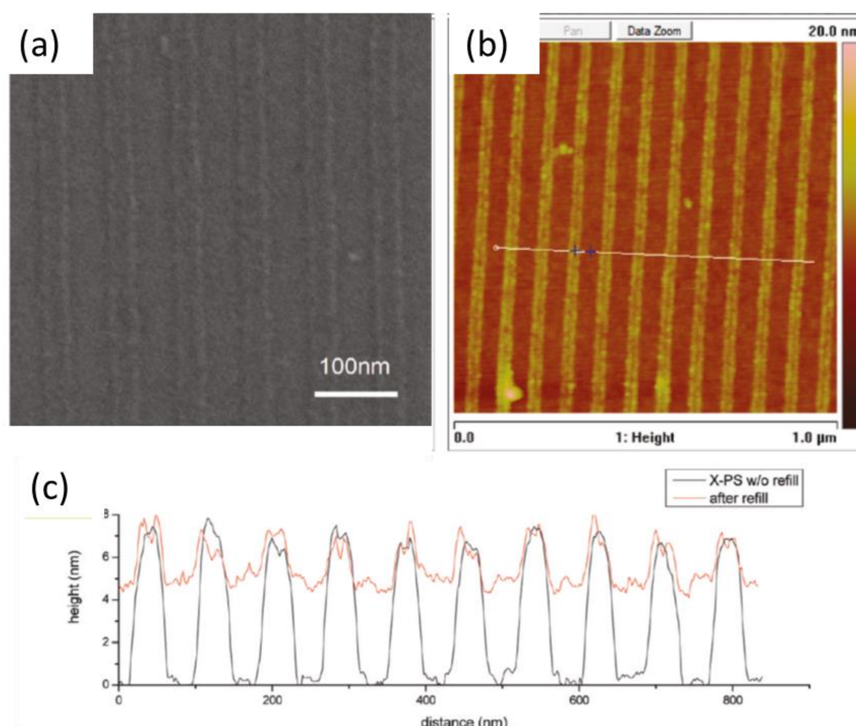

Figure 2.1 *SEM and AFM analysis of LiNe based chemical pattern after grafting P(S-r-MMA)-OH. (a) SEM image after grafting P(S-r-MMA)-OH. (b) AFM images of X-PS after grafting. (c) Cross-sectional profile along the lines shown in (b)* [12].

Alternatively, the atomically-thin graphene layer is an appealing template on which to perform directed self-assembly. Graphene has similar wetting behavior as an X-PS mat[16], but is a single atom in thickness, forming nearly no topography and providing a smooth and flat surface for the assembly of block copolymers. Unlike traditional X-PS based chemical patterns, the graphene surface interacts weakly with block copolymers, which can enhance the mobility of the polymer chains during segregation and result in more rapid assembly dynamics. Due to its sp^2 bonded lattice with carbon-carbon bond distance of 1.42 Å, graphene also has high mechanical strength[17], thermal stability[18], chemical inertness, and impermeability[19], making it a robust template that is compatible with a broad range of manufacturing conditions. Continuous graphene deposited over the wafer scale via chemical vapor deposition (CVD)[20, 21] ensures uniform monolayer thickness and surface chemistry over large areas, and the graphene can also be transferred onto arbitrary substrates.

In this work, we use atomically-thin graphene stripe arrays as chemical templates to direct the block copolymer assembly to form defect-free and well registered lamellae patterns with complex architectures. The directed self-assembly on graphene/germanium chemical patterns can accommodate strain, as the block copolymer can stretch to 13% and compress to 15% to adapt to incommensurate chemical patterns. In addition, density multiplication by a factor of 10 is demonstrated, which means that the domain size of the assembled block copolymer is one-tenth of the periodicity of the chemical pattern. These results indicate that graphene chemical patterns may enable more robust, reproducible block copolymer directed self-assembly, advancing the capabilities of such lithographic techniques for nanoscale patterning of complex designs with high resolution and fidelity.

2.2 Preparing Block Copolymer Assembly With 2D Materials As Its Chemical Template

First, we demonstrate that chemical patterns consisting of graphene guiding stripes on germanium can direct the self-assembly of block copolymers into straight, parallel lamellae structures. In this process, which is shown schematically in Figure 2.2a-e, continuous monolayer graphene films are grown directly on germanium wafers via CVD (Fig. 2.2a,b). Ge(111) substrates (Semiconductor Wafer, Inc, resistivity > 30 Ω-cm,) are used to catalyze graphene growth, as described previously[22]. The Ge(111) samples are sonicated in acetone and isopropyl alcohol for 15 min to clean their surfaces and then etched in deionized water at 90 ℃ for 15 min. The Ge(111) substrates are placed into a horizontal tube furnace with a quartz tube inner diameter of 34 mm and the system is evacuated to ~10^{-5} torr. The chamber is filled to atmospheric pressure with a flow of 200 sccm of Ar (99.999%) and 100 sccm of H_2 (99.999%). The samples are annealed for 30 min at 910 ℃ before introducing 4.6 sccm of CH_4 (99.99%), which serves as the carbon precursor, to start the graphene synthesis. The growth occurs for 12 h to ensure complete graphene coverage on the Ge(111) surface. The samples are rapidly cooled by sliding the furnace away from the growth region, which also terminates growth.

Scanning electron microscopy (SEM) and atomic force microscopy (AFM) show that the graphene surface is uniform with low roughness of < 1 nm over 10×10 μm^2. The underlying germanium surface consists of steps and terraces that are induced during synthesis and the graphene film contains sparse wrinkles 1-5 nm in height that are formed during post-growth cooling. Raman spectroscopy (Figure 2.2i, top blue spectrum) confirms that the graphene is predominately a single layer in thickness, as indicated by the integrated 2D:G ratio of ~4 and the

Raman 2D full-width-at-half-maximum of ~26 cm^{-1}. The negligible Raman D band intensity indicates that the graphene is of high quality, with a relatively low defect density.

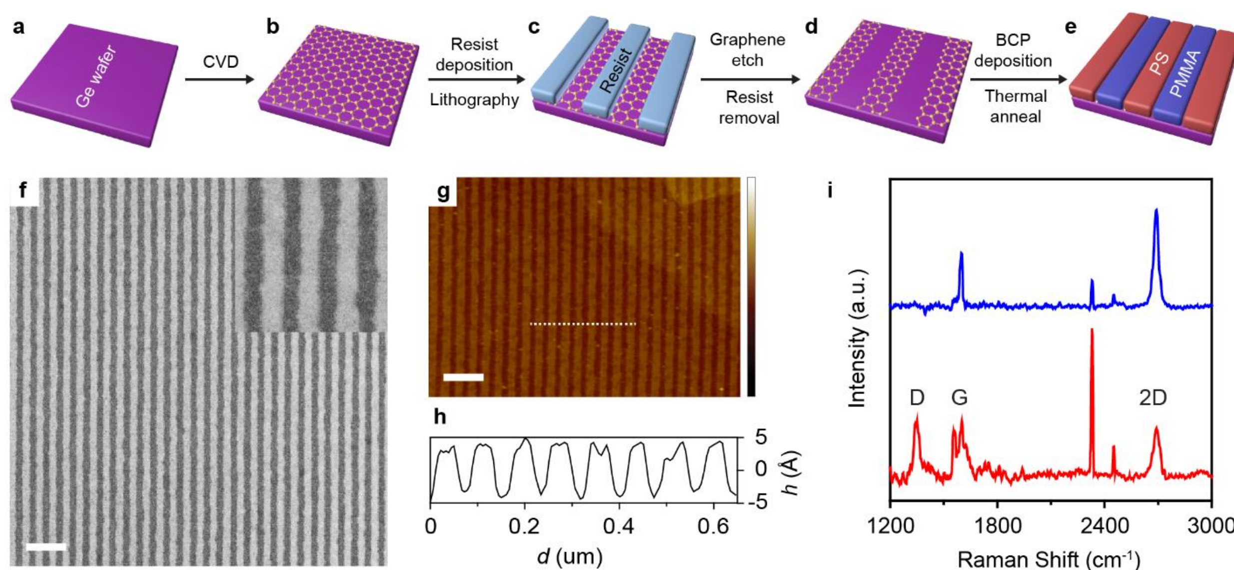

Figure 2.2 *Characterization of the graphene chemical pattern. a-e, Process flow of the block copolymer directed self-assembly on graphene chemical patterns on germanium. Graphene is grown directly on germanium via CVD (a,b). Electron-beam resist is spin-coated onto the graphene and patterned into stripe arrays (c). The exposed graphene is etched using a reactive ion plasma and the resist is removed in solvents and via thermal annealing, resulting in a graphene/germanium stripe array (d). The block copolymer is spin-coated on the chemical pattern and thermally annealed to induce directed self-assembly (e). f, SEM image of a graphene stripe array (bright lines) on germanium (dark lines). Inset shows a magnified image highlighting the edges of the graphene stripes. g,h, AFM topographic map (g) and height, h, profile plotted against surface distance, d, (h) along the dashed line in g. Scale bars in f,g are 250 nm. Height scale bar in g is 8 nm. i, Raman spectrum of an as-synthesized monolayer graphene film on germanium (top blue spectrum) and a graphene stripe array on germanium*

(bottom red spectrum). The sharp peaks at ~ 1555 and ~ 2330 cm^{-1} correspond to ambient oxygen and nitrogen, respectively.

Line arrays are patterned into a poly(methyl methacrylate) (PMMA) mask over the continuous graphene monolayer films using electron-beam lithography (Figure 2.2c). The exposed graphene regions are subsequently etched with reactive oxygen ion plasma, resulting in the formation of isolated graphene guiding stripes (Figure 2.2d,f,g,h). Mild etching conditions are used (10 sccm O_2, 50 W, 10 mtorr, 1-2 s) to ensure that the germanium surface is not etched and that the single-atom step height of the graphene stripes is preserved (Figure 2.1g,h). The samples are sonicated and rinsed in chlorobenzene and toluene and then annealed at 350-400 °C at ~10^{-5} torr to remove residue and contamination introduced during patterning. This cleaning ensures a pristine, atomically-thin chemical pattern, which increases the fidelity and reproducibility of the directed block copolymer self-assembly. The height profile along the graphene stripe array (Figure 2.2g,h) indicates that the average step height of the chemical pattern is ~ 5 Å, consistent with a single layer of graphene. After etching, the Raman D:G ratio increases to ~1 (Figure 2.2i, bottom red spectrum), consistent with increased graphene edge density due to ribbon formation.

Finally, PS-*b*-PMMA is segregated on the graphene chemical patterns via thermal annealing (Figure 2.2e). PS-*b*-PMMA is chosen for the directed self-assembly studies because it is among the most commonly studied and well understood systems used for block copolymer lithography[3, 12, 23]. The molecular weight of the PS-*b*-PMMA is 85k-*b*-91k, corresponding to a natural lamellar period (L_0) of 78 nm. The graphene ribbon arrays are spin-coated with 60 nm of PS-*b*-PMMA and the sample is annealed at 250 °C for 5-10 min in an inert nitrogen environment (O_2 < 1 ppm and H_2O < 1 ppm) to induce segregation.

2.3 Directed Self-Assembly on Graphene Chemical Patterns

Figure 2.3b-d shows that the PS-*b*-PMMA self-assembles into lamellae that closely follow the underlying graphene chemical pattern. The PS block selectively aligns with the graphene stripes, whereas the PMMA block selectively aligns with the exposed germanium surface. In Fig. 2.3, the period of the patterned graphene stripes, L_s, is chosen to be equivalent to L_0 = 78 nm to ensure that the PS-*b*-PMMA self-assembles under optimum conditions in which it is under neither tension nor compression.

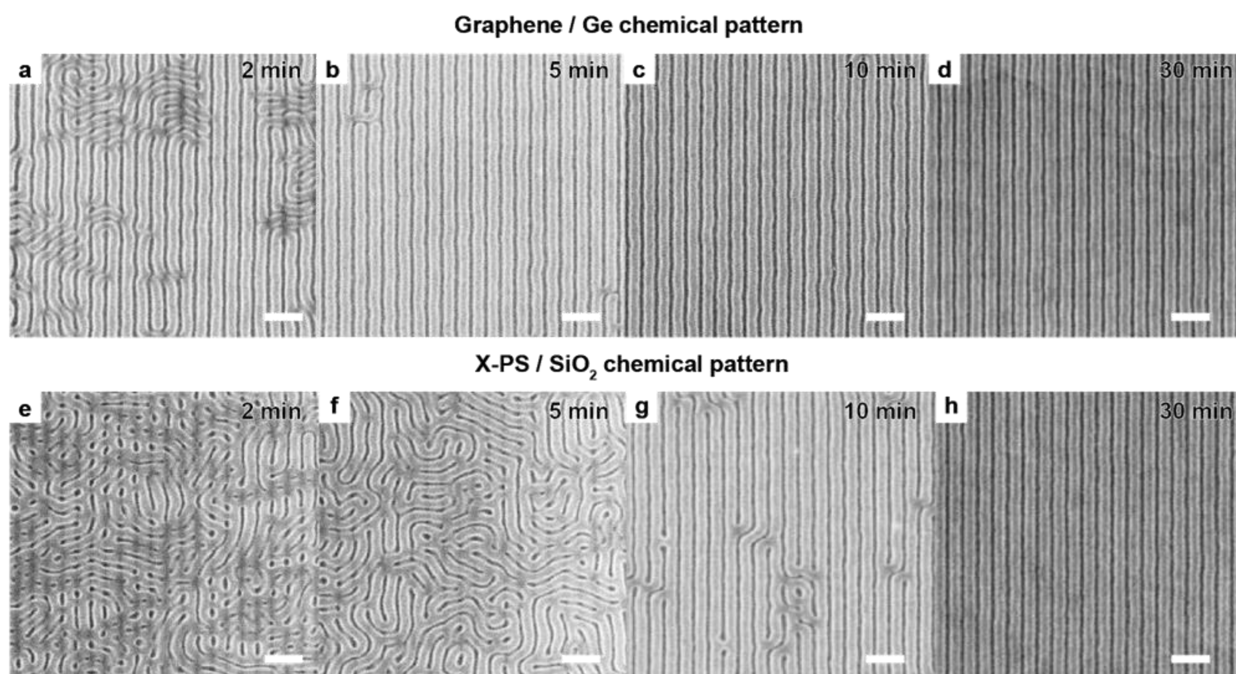

Figure 2.3 *Assembly dynamics on graphene chemical patterns. a-h, Dynamics of directed self-assembly of PS-b-PMMA after annealing at 250 °C on graphene chemical patterns (a-d) and X-PS chemical patterns (e-h) after 2 min (a,e), 5 min (b,f), 10 min (c,g), and 30 min (d,h). Ls is 78 nm. Scale bars are 200 nm.*

We compare the self-assembly dynamics of PS-*b*-PMMA on graphene templates and conventional X-PS chemical patterns (Fig 2.3). The latter control sample consists of a patterned X-PS mat on a SiO_2 substrate. The graphene and X-PS samples are patterned into similar line-space arrays with $L_s = L_0$. The samples are spin-coated with PS-*b*-PMMA and annealed at 250 ℃ for 2-30 min to reach equilibrium. We find that directed self-assembly occurs more rapidly on the graphene chemical pattern than on the X-PS based chemical pattern. Within 2 min, the block copolymer is largely ordered, following the underlying graphene chemical pattern on > 65% of the surface area (Fig. 2a); while the directed self-assembly remains local and is limited to short segments on the X-PS based chemical pattern (Figure 2.3e). The block copolymer is well-assembled with improved line-edge roughness on > 95% of the graphene chemical pattern after 5 min (Figure 2.3b) and becomes completely ordered over the entire surface at 10 min (Figure 2.3c). On the other hand, it takes 30 min to achieve the same degree of order on the X-PS based chemical pattern (Figure 2.3d). These results may indicate that the smooth, crystalline surface of graphene enables the polymers to diffuse more efficiently, resulting in faster assembly dynamics with fewer defects[15].

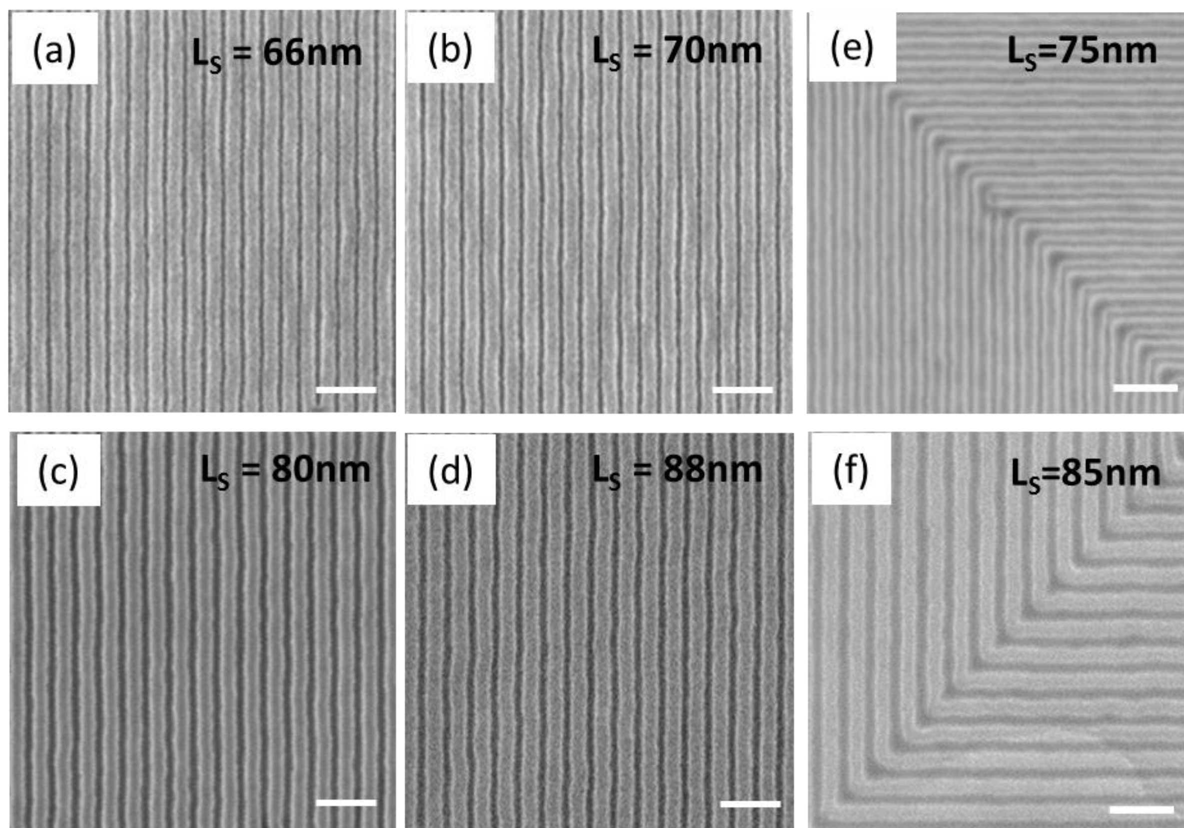

Figure 2.4 *Directed self-assembly on mismatched graphene chemical templates. a-d, Directed self-assembly of PS-b-PMMA on graphene chemical patterns with L_s of 66 nm (a), 70 nm (b), 80 nm (c), and 88 nm (d) corresponding to L_s/L_0 = 0.846 (compression), L_s/L_0 = 0.897 (compression), L_s/L_0 = 1.03 (tension), and L_s/L_0 = 1.13 (tension), respectively. Scale bars are 200 nm. e,f, Directed self-assembly of PS-b-PMMA on graphene chemical templates patterned into 90° bends with L_s of 85 nm (e) and 75 nm (f). Scale bars are 200 nm.*

The ability of the block copolymer to stretch and compress relative to L_0 to conform to the underlying chemical pattern during self-assembly is critical to ensure robust, reproducible patterning of uniform feature sizes over defective or irregular templates. PS-*b*-PMMA is self-assembled on graphene line arrays with L_s varying between 65 and 88 nm (Figure 2.4a-d). The PS-*b*-PMMA is able to compress up to L_s/L_0 = 0.846 (Fig. 2.4a,b) and stretch up to L_s/L_0 = 1.13

(Fig. 2.4c,d) to adapt to the period of the graphene guiding stripes, which is a broader commensurability window compared to that of standard X-PS chemical patterns (6.3% compression and 9.3% elongation).

We further demonstrate directed self-assembly of the PS-*b*-PMMA over graphene chemical patterns with complex architectures (Figure 2.4 e,f). Bends with 90° angles, in which the line-to-line distance at the corner is 41% longer than L_0, are patterned. Despite this large degree of stretchability, the assembled PS-*b*-PMMA follows the graphene chemical pattern with 90° turns, as shown in Fig. 3e,f. Self-assembly on 90° bends with L_s of 85 nm shows less edge roughness than that on 90° bends with L_s of 75 nm. In order to achieve such abrupt features using other types of chemical patterns, extra monomer is typically required to fill the gaps near the areas where the block copolymer domains bend[4, 24].

We also assess the assembly of block copolymers on sparse graphene chemical pattern via density multiplication (Figure 2.5). The graphene is patterned into stripe arrays with L_s that are integer multiples, n, of L_0 (where n = 1, 4, 5, 6, 8, 9, and 10). The line width of the graphene guiding stripes is chosen to be $1.5L_0$ to clearly identify the underlying graphene stripes with scanning electron microscopy after directed self-assembly. The PS-*b*-PMMA is spin-coated onto the graphene ribbon array and the sample is annealed at 250 ℃ for 5-10 min to induce self-assembly. Despite the lack of guiding stripes for n periods of L_0, the block copolymer segregates into regular domains between the graphene ribbons. On the wide graphene stripes, the PS and PMMA domains assemble into lamellae with the bottom partly parallel to the surface, creating a U-shaped cross-section; this likely occurs because the PS preferentially wets the graphene surface when the width of a stripe is greater than L_0, as previously reported on X-PS based chemical patterns. Density multiplication by a factor of 10 is achieved using the graphene

chemical pattern (Figure 2.5f), which is greater than the largest factor of 6 achieved using X-PS based chemical templates [25].

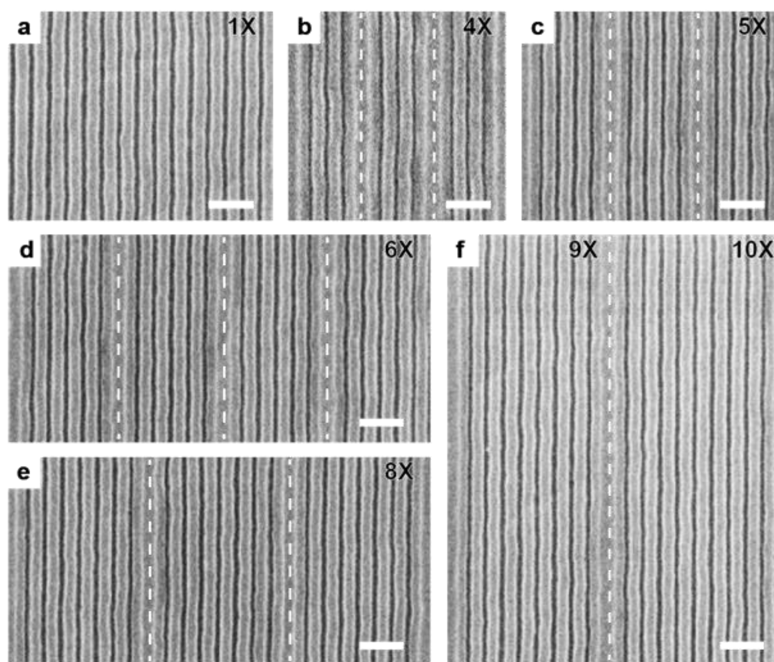

Figure 2.5 *Density multiplication on graphene chemical patterns. a-f, Directed self-assembly of PS-b-PMMA on graphene chemical patterns with density multiplication by a factor of 1 (a), 4 (b), 5 (c), 6 (d), 8 (e), and 9 and 10 (f). In f, the regions to the left and right of the dashed line are patterned with 9X and 10X density multiplication, respectively. Scale bars are 200 nm.*

We also demonstrate density multiplication using PS-b-PMMA with smaller molecular weight (22k-*b*-22k, corresponding to L_0 of 25 nm) to achieve pattern resolution of 12.5 nm (Figure 2.6). In this scheme, arrays consisting of graphene guiding stripes that are 75 nm wide and germanium stripes that are 25 nm wide are patterned. Interestingly, unlike the above situation, in which density multiplication is achieved on the germanium area, density multiplication is achieved on the graphene guiding stripe between the bare germanium regions. The mechanism of this density

multiplication is still under investigation. Nevertheless, the achievement of features with 12.5 nm domain size demonstrates the promise of atomically-thin graphene chemical patterns to enable high-resolution nanopatterning.

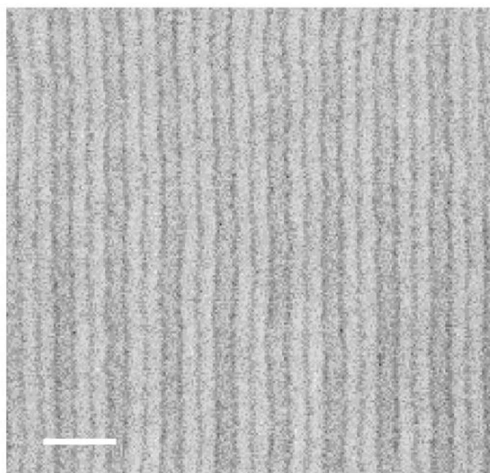

Figure 2.6 *Density multiplication with 22k-b-22k PS-b-PMMA (L_0 = 25 nm) on a graphene/germanium chemical pattern. The graphene and germanium stripes are 75 and 25 nm wide, respectively. Density multiplication by a factor of 3 is achieved to obtain a feature size of 12.5 nm. Scale bar is 100 nm.*

2.4 EUV Enhanced Large Scale Block Copolymer Assembly

The above results were obtained using graphene guiding stripes that are grown directly on germanium. The direct synthesis of the graphene chemical pattern on a target substrate is desirable for wafer-scale assembly of block copolymers for multiple reasons. For example, CVD is an inherently scalable process, yielding uniform continuous graphene films over large areas that are only limited in extent by the size of the substrate or the size of the reaction chamber[26]. Furthermore, the direct growth yields relatively unperturbed, pristine graphene films[22], providing a clean, highly reproducible template on which to conduct directed self-assembly.

However, we also show that graphene guiding stripes can be used for directed self-assembly on alternate surfaces. Continuous graphene films that are grown on copper substrates are transferred to SiO_2 with a sacrificial polymer support[20]. The continuous films are subsequently patterned into guiding stripes using electron-beam lithography and reactive ion etching, as described above. The PS-*b*-PMMA is able to assemble epitaxially into lamellae on these graphene guiding stripes on SiO_2 wafers with L_s of 78 nm. Thus, the transfer of graphene enables self-assembly on arbitrary surfaces, provided that the target substrate has sufficient interfacial energetics to direct assembly.

Finally, we demonstrate that the directed self-assembly of PS-*b*-PMMA using graphene chemical patterns can be achieved over large areas. Graphene guiding stripes are patterned on SiO_2 over areas of 100×75 μm^2 using extreme ultraviolet (EUV) lithography and the block copolymer films are self-assembled (Fig. 2.7). The block copolymer is well-ordered over the entire patterned area, demonstrating that our approach is compatible with conventional planar lithographic patterning.

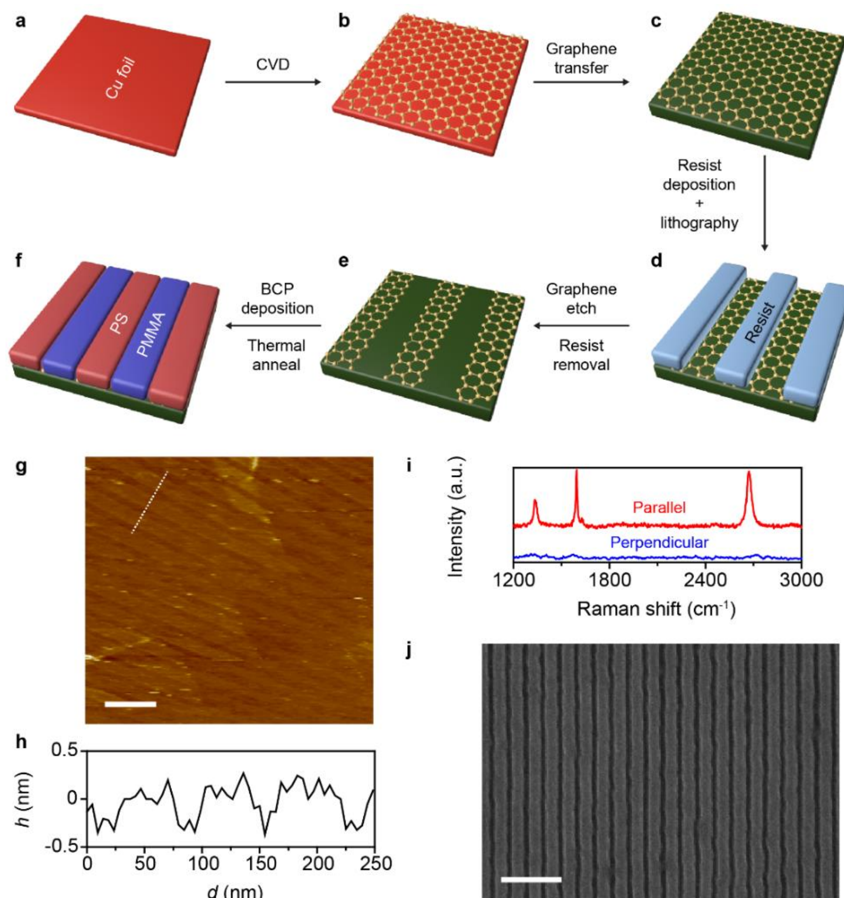

Figure 2.7 *a-f, Process flow of the block copolymer directed self-assembly on graphene chemical patterns on* SiO_2*. Graphene is grown on copper foil via CVD (a,b). The graphene is then transferred on to* SiO_2 *(c). PMMA is used as a mechanical support and the copper is etched with* $FeCl_3$*. The graphene is then transferred onto* SiO_2 *and the PMMA support is removed in acetone. Next, electron-beam resist is spin-coated onto the graphene and patterned into stripe arrays with electron-beam lithography of extreme ultraviolet lithography (d). The exposed graphene is etched using a reactive ion plasma and the resist is removed in solvents and via thermal annealing, resulting in a graphene/*SiO_2 *stripe array (e). The block copolymer is spin-coated on the chemical pattern and thermally annealed to induce directed self-assembly (f). g, AFM topographic image of patterned graphene stripes on germanium with* L_s *of 78 nm. Scale bar is 200 nm. h, Height (h) profile along the white line shown in g shows that the chemical*

pattern step height is ~0.5 nm. i, Raman spectra polarized parallel (vertical) and perpendicular (horizontal) to the long-axis of the graphene stripes. j, SEM image of the lamellae forming 85k-b-91k block copolymer assembled on the graphene chemical pattern with L_s of 78 nm. Scale bar is 250 nm.

Chemical pattern	Assemble Time	Minimum CD	Density Multiplication	Monomer for 90º R	Commersurability
Graphene	5min	7nm	10 times	No	15% / 13%
Polystyrene	30nm	25nm	4 times	Needed	< 10%

Table 2.1 *The difference between 85k-b-91k PS-PMMA di-block copolymer assemble over PS based and graphene based chemical pattern is summarized.*

The compare between the PS based chemical pattern and graphene based chemical pattern is summarized in Table 2.1.

Water contact angle measurements are conducted to gain insight into the mechanism governing the directed self-assembly (Figure 2.8). With its atomic layer thickness, the graphene is not likely sufficiently thick to serve as a boundary for the topographically-guided graphoepitaxy. We compare the water contact angle on graphene, germanium, PS, PMMA, and a random PS-PMMA (PS-*r*-PMMA) film. The water contact angle on a continuous monolayer graphene film (81°) is similar to that of the PS film (91°). Furthermore, the contact angle on a bare germanium surface after plasma treatment (72°) is similar to that of the PMMA film (68°). Therefore, the difference in surface energy between the graphene and the germanium likely provides the chemical contrast needed for directed self-assembly; the PS preferentially wets the graphene guiding stripes and the PMMA preferentially wets the exposed germanium areas.

Figure 2.8 *a-e, Water contact angles measurements of a graphene surface after solvent rinsing in chlorobenzene and toluene and annealing at 350 °C at ~10^{-5} torr for 2 h to remove residues and contamination introduced during processing (a), Ge(111) surface after O_2 (10 sccm) plasma etching at 50 W and 10 mtorr for 1-2 s (b), PS film (c), PMMA film (d), and PS-r-PMMA random brush neutral film consisting of 57% PS by weight composition (e).*

The large degree of commensurability that is provided by the graphene guiding stripes may also be attributed to this strong chemical contrast, which is due to the difference in interfacial energy between the guiding stripe and the open area. This chemical contrast can allow compensation of the energetic penalty when the block copolymers assemble on guiding stripes with L_S that deviates from L_0[5]. The chemical affinity of X-PS is modified by processing steps, such as plasma trimming and brush backfilling[13]. In contrast, the interfacial energy of graphene should be relatively unchanged during processing due to its high chemically inertness. Moreover, the atomic thickness of the graphene chemical pattern (~ 3.5 Å) minimizes sidewall effects, which may contribute to directed assembly, especially compared to the much larger thickness of X-PS patterns (> 30 Å)[5].

Surprisingly, we find that the water contact angle of the bare germanium surface after the weak plasma treatment (72°) is approximately the same as the neutral surface of the block

copolymer (72°), making it neutral towards PS-*b*-PMMA. This neutral surface likely provides a favorable template on which to achieve density multiplication because it is neither preferential towards the PS nor the PMMA domains. Typically, the bare regions between guiding stripes of the chemical pattern are made neutral with a brush backfilling step to achieve such density multiplication.

2.5 Sub 10nm Block Copolymer Assembly Over Graphene Chemical Pattern

So far, we have discussed advantages of DSA based on PS-*b*-PMMA di-block copolymer, currently most reliable and reproducible BCPs and PS-*b*-PMMA with feature size 28nm has been demonstrated with 193i photolithography on 300mm production. [27] The feasibility of the PS-*b*-PMMA based system face fundamental challenging when shrinking the feature size to below 20nm because the low interaction factor (χ) of PS-*b*-PMMA. In the regime with smaller feature size polymerization, it requires higher χ to enable the phase separation in the assembly results. Figure 2.9 plots the block copolymer with different factor χ.

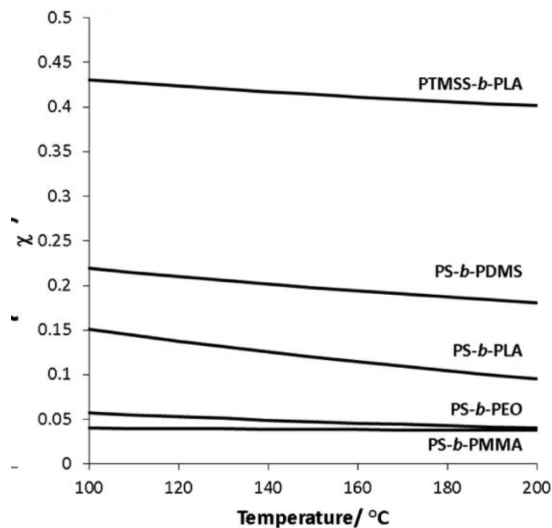

Figure 2.9 *Temperature dependence of χ in the form χ = A/T + B for PTMSS-b-PLA (this work) (A = 51.3 K, B = 0.29, measured by absolute intensity SAXS), PS-b-PDMS (A = 68 K, B = 0.037, using a reference volume of 118 Å3),41 PS-b-PLA (A = 98.1 K, B = −0.11, using a reference volume of 185 Å3),30 PS-b-PEO (A = 29.8 K, B = −0.023, using a reference volume of 118 Å3),41 and PS-b-PMMA (A = 4.46 K, B = 0.028, measured by absolute intensity SAXS)[28].*

Different from the typical PS-*b*-PMMA system that uses thermal annealing for the polymerization, other BCP chemistries that has higher χ usually require alternative annealing strategies, such as solvent vapor annealing[29] or the use of top coat layers[30]. Here, we will adapt ABA (P2VP-b-PS-b-P2VP, 8k-16k-8k) type triblock terpolymer that has feature size 16nm and solvent annealing process to demonstrate the feasibility of DSA based on our graphene chemical system. We first test the assembly result of P2VP-*b*-PS-*b*-P2VP on PS chemical pattern and graphene chemical pattern with pitch size 100nm and 10nm oxide exposure gap as the process we used in the previous PS-*b*-PMMA assemble process. The assemble result is shown in Figure 2.10.

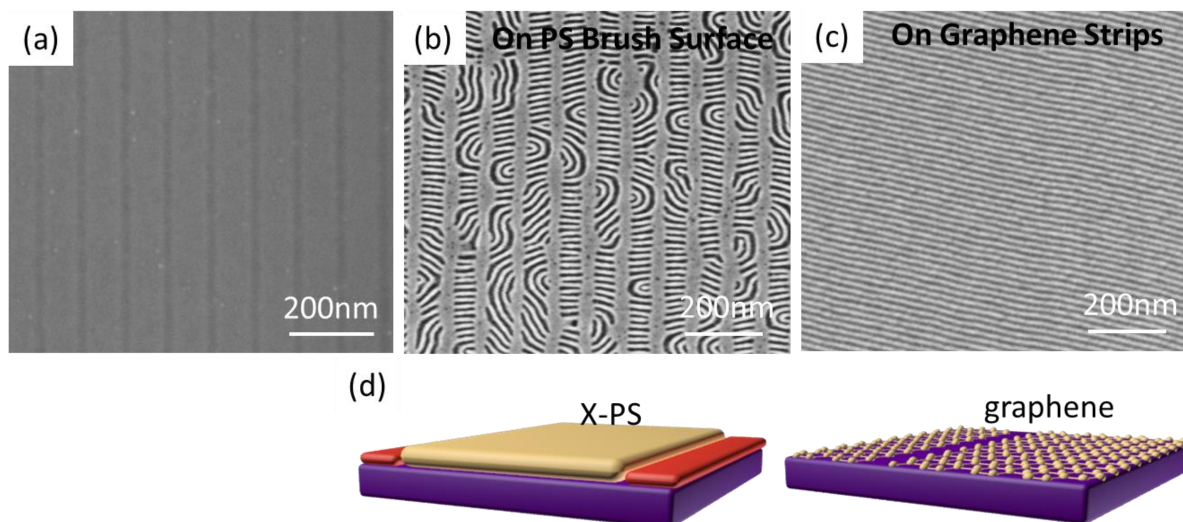

Figure 2.10 *Solvent annealing of ABA (P2VP-b-PS-b-P2VP, 8k-16k-8k) type triblock terpolymer with SIS Process (a) SEM image of Graphene strips on oxide wafer with 100nm strip width and 10nm oxide exposed region. Assembly results of PS-P2VP triblock on (b) PS strips (c) graphene strips (d) schematic of PS brush pattern and graphene chemical pattern with 100nm pitch size and 10nm oxide exposure gap.*

Not surprisingly, in the figure 2.10, triblock copolymer P2VP-*b*-PS-*b*-P2VP assemble on the PS chemical pattern shows parallel morphology whenever it is on the 10nm oxide surface (Fig. 2.10 b). On the PS chemical pattern surface, the assembly morphology is the same as the assembly over the graphene surface (Figure 2.10c). Contrary to the results on the classical PS chemical pattern, with atomic layer topology over the graphene based pattern, P2VP-*b*-PS-*b*-P2VP easy meander across the 10nm oxide exposed area. To our surprise, the assembly pattern of P2VP-*b*-PS-*b*-P2VP with feature size 16nm form regular lamellae pattern with very low defect over the periodic structure graphene/oxide 100nm/10nm. The assembled large area lamellae pattern has a constant degree deviation from the bottom guiding strips. This acts as a

proof of the semi-guiding behavior of the bottom guiding oxide strips. Since the complexity of the lithography required to exposure the pattern with 100nm separation is way much lower compared to those lithography required for the sub-10nm techniques (including the DSA of block copolymer), the result shows the potential schematic of using low level exposure tool to achieve the sub 10nm features with much cheaper prices. To further study the cause of the semi-regulated pattern, we regulate the oxide strips width ranging from 10nm, 30nm, 100nm as shown in Figure 2.11.

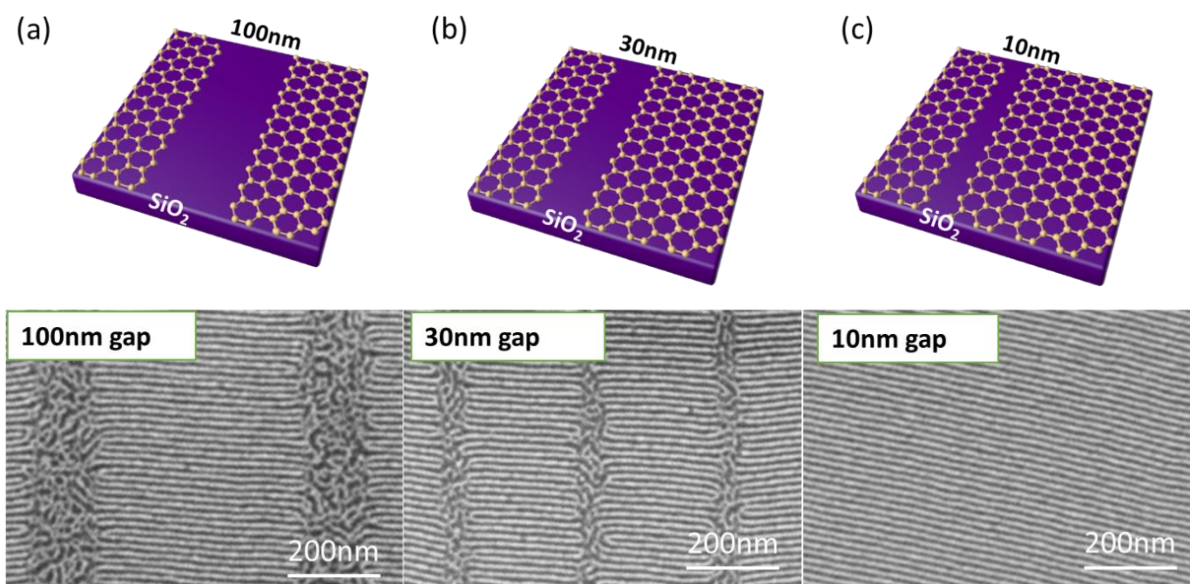

Figure 2.11 *Solvent annealing of ABA (P2VP-b-PS-b-P2VP, 8k-16k-8k) type triblock terpolymer with SIS Process on graphene strips with different gap in demonstration of boundary effect (a) 100nm (b) 30nm (c) 10nm.*

P2VP-*b*-PS-*b*-P2VP with characteristic distance 16nm seem to be greatly affected by the oxide strips width. As the width of oxide strips reaching 30nm, almost twice the L_0 of P2VP-*b*-PS-*b*-P2VP, the perpendicular lamellae morphology graduate gradually transit to the parallel one.

Since we already know that P2VP-*b*-PS-*b*-P2VP only form perpendicular lamellae pattern on the graphene area, we expect to see even clear parallel condition in 100nm gap, which is confirm in Figure 2.11a. In addition to the confirmation of the ridge guiding behavior, we observe an increase boundary control results on top of the graphene area. The perpendicular lamellae with 100nm shows stronger and more oriented straight assemble results as the two surrounding oxide ridges are wider. Some lamellae perpetrates into 30nm oxide strips area because the confinement is smaller on 30nm condition. The assembly results is double confirmed with the simulation results based on Coarse Grain model, demonstrated in Figure 2.12.

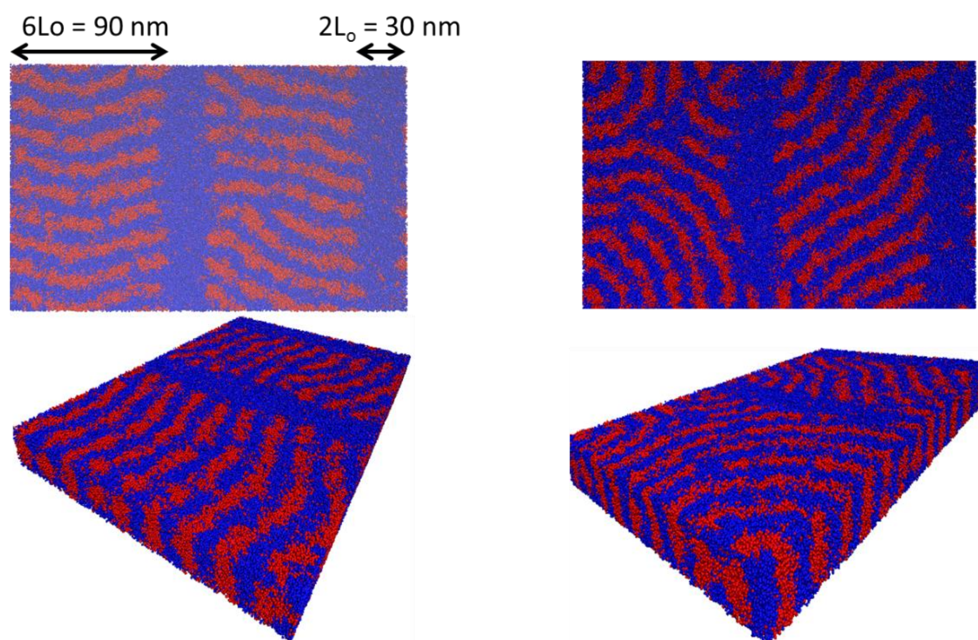

Figure 2.12 *Exploratory results of ABA triblock copolymer films in the presence of "chemically patterned surfaces" with period of* $L_s = 8L_o$ *and the stripes have a width of W = 6Lo, representing PS-preferential regions. The background is preferential for P2VP. Film thickness is* $L_z=1.5L_o$*, red represent PS and blue P2VP. We present top and lateral view of 3D configuration of two different values of pattern interactions.*

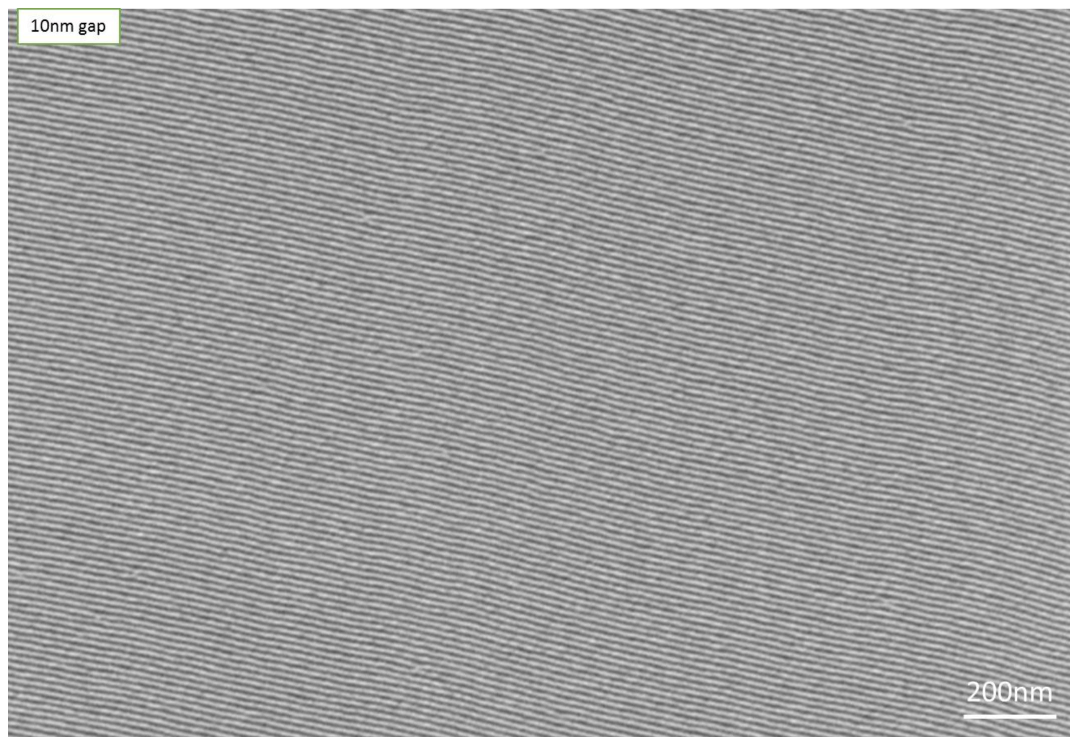

Figure 2.13 *Assembly results of P2VP-b-PS-b-P2VP on top of 100nm/10nm graphene/gap surface. Solvent annealing with swelling ratio 0.5. The assembled perpendicular lamellae follows the bottom guiding stripes and can meander several um.*

Finally we test limit of the mismatch assemble results and shows it in Figure 2.13. It shows that the angle deviated lamellae pattern can always be continuous and as long as the underline mismatch 100nm/10nm guiding pattern exist. It can last to several millimeters. Due to the limit of the e-beam we used to pattern the graphene chemical, we only shows up to 3um.

2.6 Summary

In conclusion, the directed self-assembly of block copolymer films using traditional X-PS based chemical patterns has invoked recent discussions on the exact guiding scheme with a

trapezoidal shape, as the chemical contrast evolves per processing step[13]. Here, we demonstrate that monolayer graphene can instead be used as an atomically-thin, ideal chemical pattern to direct the self-assembly of PS-*b*-PMMA, which will become more relevant as the pattern resolution increases. With similar wetting behavior as traditional X-PS chemical patterns but with the contribution of nearly zero topography, graphene based chemical patterns offer several unique advantages. Specifically, graphene chemical patterns (1) reduce the assembly time, (2) enable the block copolymer to compress to $L_s/L_0 = 0.846$ and stretch to $L_s/L_0 = 1.13$ to assemble over incommensurate patterns, (3) allow the block copolymer to conform to irregular and complex templates, and (4) provide density multiplication by a factor of 10. In addition to etching the graphene into stripes, future studies will be conducted to pattern chemical contrast by exposing the sample to chemical or plasma treatment, by forming a self-assembled monolayer, or by depositing a second two-dimensional atomic layer (e.g. by van der Waals epitaxy or stacking). The assembly is further extended to BCP with feature side 16nm, which implies the capability of forming 8nm electronics. We demonstrate that with the help of graphene chemical pattern, we can form large and order perpendicular lamellae morphology of 16nm BCP assemble results with sparse pattern. This technique enable the adaption of lower cost lithography tool in sub-10nm fabrication line.

These graphene based chemical patterns may enable the directed self-assembly of ultra-narrow block copolymer domains for future industrial-scale manufacturing of nanoscale features with sub-10 nm resolution, such as transistors and interconnects in integrated circuits and magnetic components in data storage media.

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Chapter 3 High Power Fast Flexible Electronics: Transparent RF AlGaN/GaN HEMTs on CNF substrate

3.1 Introduction

As wireless network prevails, the demand for the high power microwave flexible electronics is increasing dramatically. For conventional applications, need for wide bandwidth, higher frequency, and high power amplifiers, as well as energy-efficient power converters, have enabled the rapid development of GaN HEMTs. With excellent electron mobility (~2000 cm^2/Vs) of heterojunction[1] and high breakdown field (3 MV/cm), GaN based HEMT devices have demonstrated high breakdown voltage to ON-resistance ratio[2] and ultra-high frequency[3]. However, incorporation of GaN HEMT into flexible electronics faces major challenges. First, to make flexible devices, GaN films should be released from the rigid epitaxial substrates. Current Si and III-V flexible electronics are based on hydro fluoride (HF) or HCl wet etching of sacrificial layers (SiO_2 or AlGaAs) or AlInP [4], which is usually impossible for GaN. There are efforts to transfer GaN from the growth substrates through laser ablation[5], mechanical releasing[6], and chemical releasing[7, 8]. But these methods are either time consuming, leaving rough surfaces, or incompatible with flexible electronics due to thickness limitation. Second and more importantly, thermal management is a critical issue for flexible electronics[9]. On rigid substrates, heat generation from the GaN HEMTs can be dissipated through heat sinks[10], which is neither flexible nor light-weight. For flexible devices, heat dissipation only happens through in-plane conduction and air cooling. So the most effective way is to use the material that is flexible and has high thermal conductivity. Heat can then be evenly spread out over a large area

for the air to remove it. But, thermal conductivity of the soft materials is usually low, which makes high power electronics still a missing piece in the flexible applications. Recently, some materials has been employed to improve the thermal management of flexible electronics: adapting thin film glass[11], ultra-nano-crystalline diamond (UNCD)[9], mixtures[12, 13], and 2D materials[14, 15]. The UNCD thin film varies from 0.3~551W/mK, heavily depending on the grain side[16]. UNCD with large grain size usually has thicknesses that are over microns, resulting in poor flexibility. By mixing the high conductivity particles, the thermal conductivity of flexible materials that usually has thermal conductivity of 0.01~0.2 Wm/K and can be increased [12, 17], but still far from the requirement of high power electronics. A mixture of 2D materials BN or graphene film and soft materials can greatly increase the thermal conductivity[14]. However the dielectric loss, opacity, low temperature tolerance, and availability of thin thickness of this film remain unsolved. On the contrary, we noticed many single crystal films are highly thermal conductive and can serve as a flexible heat dissipation layer once their thickness is reduced. By introducing the enhanced thermal conductivity crystal membrane as the heat spreading layer, locally generated heat could be managed.

Here a unique heat management method is introduced. It is implemented by transferring AlGaN/GaN HEMT devices onto flexible substrate and in-situ using the large-area single crystal GaN buffered layer to spread out the heat. Using this method, high power RF GaN HEMT on PET film will be demonstrated. Our approach is based on the GaN-on-Si technology which provides an alternative method of transferring large area GaN on the flexible substrate[8]. Instead of using the wet releasing method, the transfer is further improved by introducing gas phase XeF_2 etching on PDMS handling substrate[18]. With the PDMS stamp holding the large area

suspended GaN released from the silicon substrate, the freestanding large scale GaN film can be further printed on PET.

3.2 Limited Thermal Budget For The High Performance Flexible Electronics

Unlike in conventional electronic systems, fans, metal dissipater, or liquid-circulation system cannot be installed on the flexible substrates. Heat is dissipated through in-plane conduction and air cooling. Usually the flexible substrate is a thermal insulator, and it degrades at elevated temperatures. Therefore, we suggest utilizing both a heat conduction layer to spread the heat and a heat insulation layer to keep heat from the substrate, as shown in Figure 3.1. In such a configuration, the heat generated from the active device can quickly flow laterally without vertical penetration and eventually dissipate into the air.

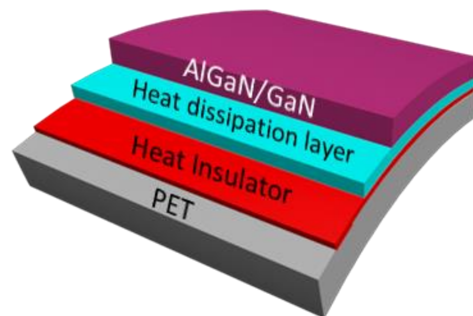
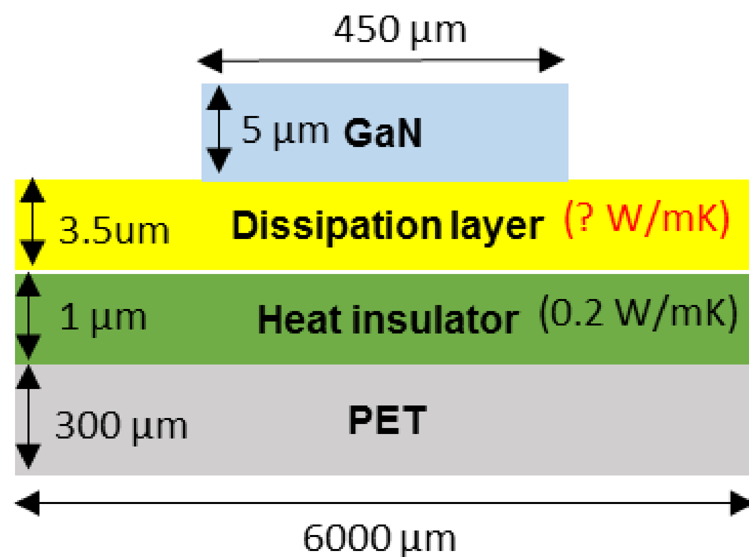


Figure 3.1 *Schematic of three layers heat management structures for the high performance high power flexible electronics. The active AlGaN/GaN HEMTs is mounting on the heat dissipation/heat insulation layer on top of the PET substrate.*

To investigate its viability, a numerical simulation is carried out with COMSOL at total power input of 0.5W, the most basic requirement for the function of wireless transmission elements.

The ambient condition is defined as windless, and experiencing natural convection due to temperature caused expansion and gravity gradient, based on the assumption of the most general use of flexible electronics. The thermal insulation layer places a key role to protect the flexible substrate from overheating. Ideally, it should confine heat conduction within the thermal conductive layer. We will use SU-8 as the heat insulation layer. Figure 3.2b shows the temperature distribution within the structure shown in Figure 3.2a. It is clear that maximum temperature declines rapidly as the thermal conductivity coefficient increased.



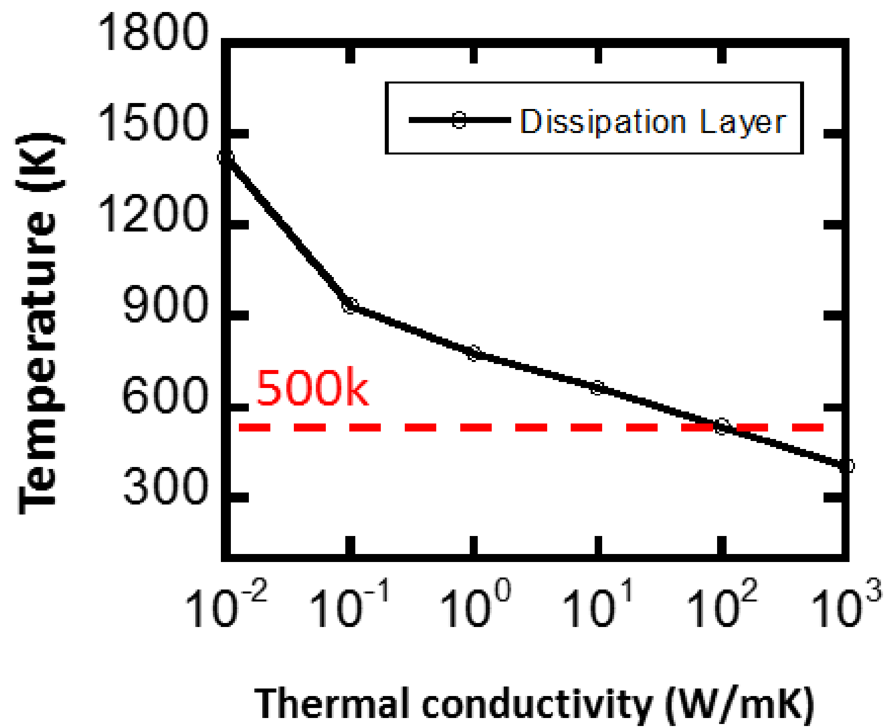


Figure 3.2 *Thermal Simulation of heat source on flexible substrate (a) simulation parameter (b) temperature distribution versus dissipation layer with different thermal conductivity. The thermal conductivity of the Heat Insulator is set to 0.2W/mK similar to the properties of the SU-8.*

When the dissipation coefficient of the dissipation layer is close to that of flexible materials, a controlled condition similar to those without dissipation mechanism, the temperature could easily go beyond 1000 ºC. This is the reason why previous thermal management quickly failed[19]. According to the simulation, the requirement of thermal conductivity coefficient over 100Wm/K

is needed to reduce the maximum temperature of the device to below 200°C, the safety operation temperature of the flexible electronics. The required thermal conductivity for dissipating 0.5W input power is higher than the current available choices in flexible materials. Different candidate materials are listed with relevant properties in Table 3.1.

UNCD film is brittle while the other materials are not favored in terms of thermal conductivity. In comparison, GaN film is mechanically softer than UNCD and has a thermal conductivity coefficient up to 260 Wm/K, which make it a promising candidate for heat dissipation. Hence, the thought of using GaN film as a heat dissipation layer has been tested.

	Soft Material	BSG Glass*3	CNF /BN*	UNCD	GaN
Thermal conductivity (W/mK)	0.15~ 0.3	1.4	20~ 100	1~ 410	130
Young's modulous (GPa)	2	63	-------	1220	180
Dielectric Constant					
Transparency	High	High	Low	High	High

Table 3.1 *Brief summary of the current used materials for the flexible electronics.*

3.3 Transfer Printing of Transparent Single Crystalline AlGaN/GaN HEMTs to PET

Figure 3.3 *Process Flow of fabricating flexible GaN HEMT. The AlGaN/GaN thin film is transferred through PDMS stamp transferring and XeF2 selective etching*

Before attaching to PDMS stamp, 1um Microchem. S1813 photoresist with thickness around 1um was coated on the substrate. The unevenly coated photoresist at the edge was exposed and removed to ensure better contact to the PDMS stamp. The sample was then attached to 1:6 cured PMDS stamp with the device side attached, and baked at 100˚C for 10 minutes. The whole structure was held on the glass lid for handling. The device was then placed in the SPTS Xetch e1 XeF_2 etcher to remove the Si substrate and release the GaN membrane. The short 30 second XeF_2 gas flow with pressure 4.0 Torr is applied with a nitrogen purge session in between. Once the transparent GaN membrane is exposed, SU-8 2000.5 coated 3 mils PET film is attached to the GaN membrane held on the PDMS stamp. The SU-8 is posed exposed and baked to

strengthen the contact. The whole device is then placed in acetone to release the AlGaN/GaN HEMTs on PET from the PDMS stamp.

The 3 um Fe doped high-resistive AlGaN/GaN epi layers is grown on Si by MOCVD method. After the growth, AlGaN/GaN film is transferred onto PET, with the procedures shown in Figure 1. To begin with, the finished GaN HEMTs is covered with photoresist which acts as the planarization and protection layer during XeF_2 etching. Once the photoresist is hard baked, the wafer is flipped and attached to a PDMS stamp, which is able to hold the AlGaN/GaN side without any air bubbles. Good contact is important to prevent the undercut XeF2 from etching into photoresist protecting layer.

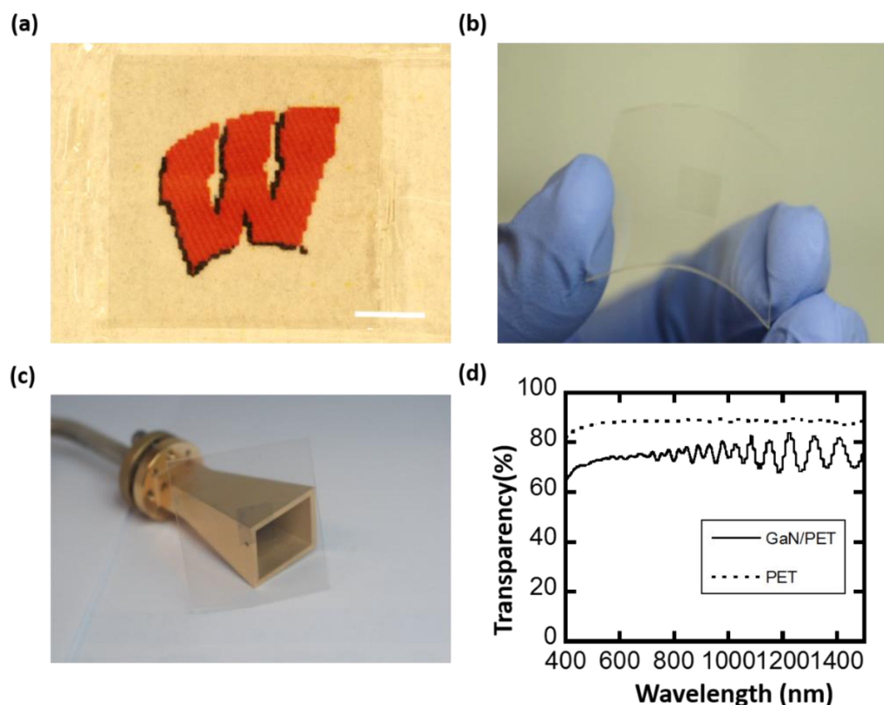


Figure 3.4 *(a) Thin GaN membrane printed on PET film, with scale bar of 2mm (b) Bending of the GaN/PET film (c) GaN/PET next to a horn-antenna d) Optical transparency measured on the bare PET film and the GaN/PET.*

The sample is then placed in XeF_2 chamber upside down for 3 hours to remove the Si bottom substrate. The XeF_2 pressure is set to 4.0mTorr with 30 second etching cycles. Due to the high selectivity between the Si and PDMS/photoresist, the sample will remain undamaged through the etching process. The images during the etching are shown in Figure 3.5.

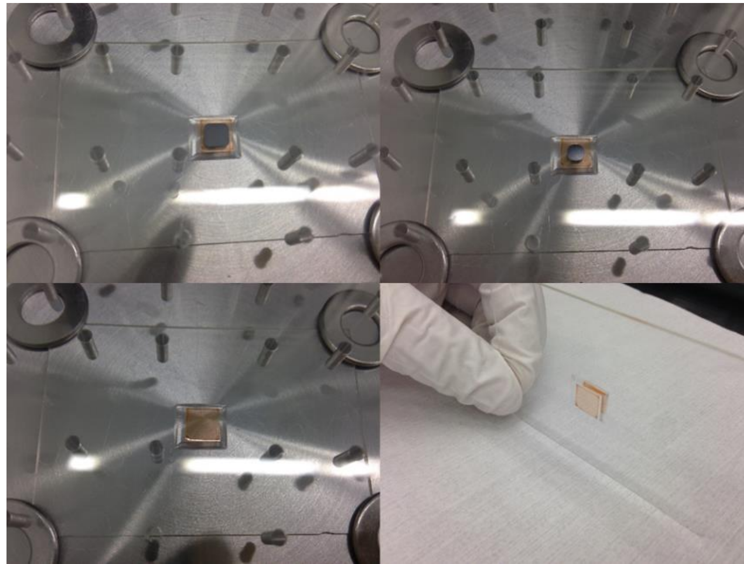


Figure 3.5 *PDMS assist GaN on Si transfer process. XeF2 etching in process (a) early stage (b) middle (c) end (d) a release GaN membrane on PDMS holding on glass substrate. Ready to be printed on flexible substrate.*

After Si is totally removed, the smooth GaN membrane surface is exposed. The released GaN thin film remained attached to the PMDS handling substrate without curving up due to the internal stress. Before transferring the GaN membrane, the target PET film is coated with SU-8 as the adhesion layer. PDMS stamp is then pressed onto the SU-8/PET film by gently applying pressure to drive out the bubbles in the contact. After curing and hard baking of SU-8, the

PDMS/PR/GaN/SU-8/PET is immersed in acetone to remove the photoresist between the GaN and PDMS. Then the GaN is transferred onto PET film. Figure 3.4a to 3.4c show the transferred GaN on PET. In Figure 3.4a, the transferred GaN film is placed on the printed "W" showing the ultra-high transparency nature of the high bandgap GaN film. In Figure 3.4b and 3.4c, hand held bending of 5mm radius GaN/PET film and placement on a horn-antenna are demonstrated, respectively. The transparency of the GaN/SU-8/PET is shown in Figure 3.4d. Averaging 70% of transparency of the structure in the visible light range compared to 90% PET film. The oscillation at long wavelength is the interference pattern within the GaN/SU-8/PET structure due to the refraction index stacking. Currently, it is the most thermal conductive film that is flexible and but still maintain optical transparent properties. The GaN film has similar thermal conductivity as the UNCD thin film and is more flexible at the same thickness. After transfer, thermal conduction is crucial in flexible electronics.

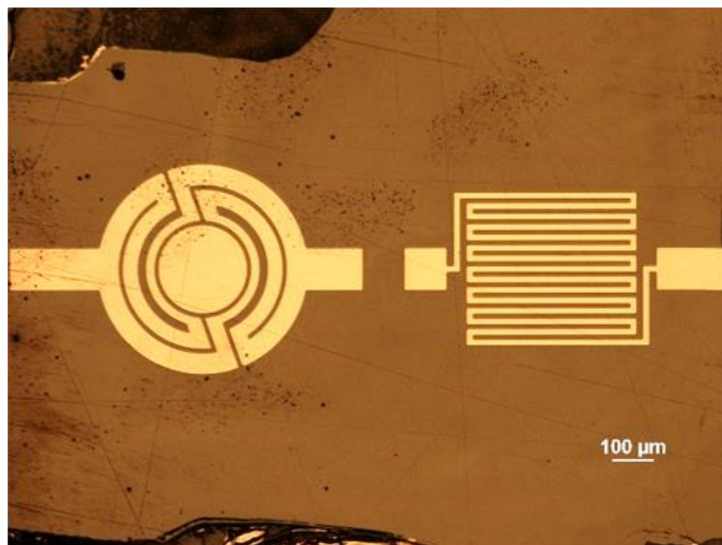
3.4 Heat dissipation Using GaN as Heat Dissipation Layer

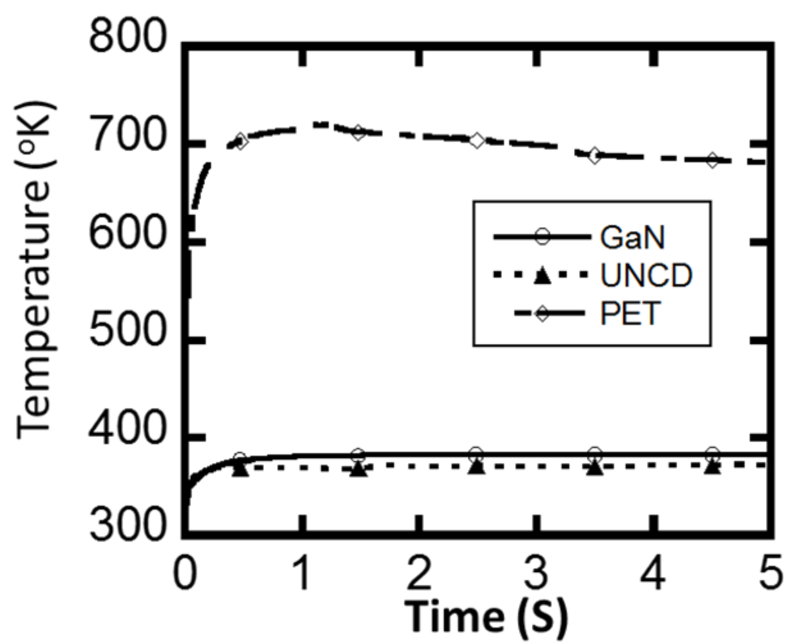
We experimentally compared the thermal dissipation of three samples, specifically, PET film, 3.5 um GaN/SU-8/PET, and 3 um UNCD/SU-8/PET. The GaN film is released byXeF_2 etching Si of GaN-on-Si sample. Current GaN-on-Si grown by MOCVD can precisely control the thickness of GaN epilayer, and the XeF_2 release - PDMS transfer methods demonstrated can make it flexible (Figure 3.5).

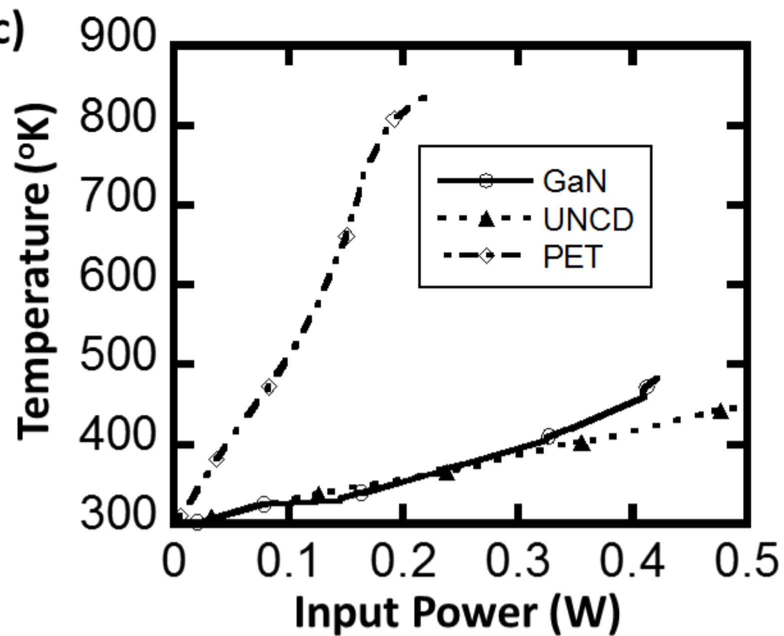
As shown in Figure 3.6a, Ti/Au micro-heater and sensor are fabricated on the surfaces of samples. The temperature is measured according to the variation of thermal resistance. To begin

with, the micro-heater are powered by a DC source while the time-dependent temperature is measure according to its thermal resistance. In Figure 3.6b, the transient temperature of different samples are plotted with 0.35 W heating power starting at 0 s. The bare PET film is immediately overheated as the temperature rise to its boiling point (around 350°C). For GaN/SU-8/PET and UNCD/SU-8/PET, heat is transferred faster and the temperature reaches a plateau within 1 second. In Figure 3.6c, temperature measured under different heating power is compared. It suggests that with limited thermal budget for the flexible electronics on PET, the temperature rises rapidly as power increases. Single crystal GaN films can conduct heat at the same level as the diamond films. The configuration is well maintained below the melting temperature of the PET with power up to 0.5 W. The thermal conductivity of GaN and UNCD is also measured using temperature different between the heater and the sensor. The value is plotted in Figure 4.4 (d), a little overestimated due to the ignorance of the air convection in the system.

(a)




(b)
800
700
600
500
400
300
Temperature (oK)
0
1
2
3
4
5
Time (S)
GaN
UNCD
PET


(c)
900
800
700
600
500
400
300
Temperature (oK)
0
0.1
0.2
0.3
0.4
0.5
Input Power (W)
GaN
UNCD
PET

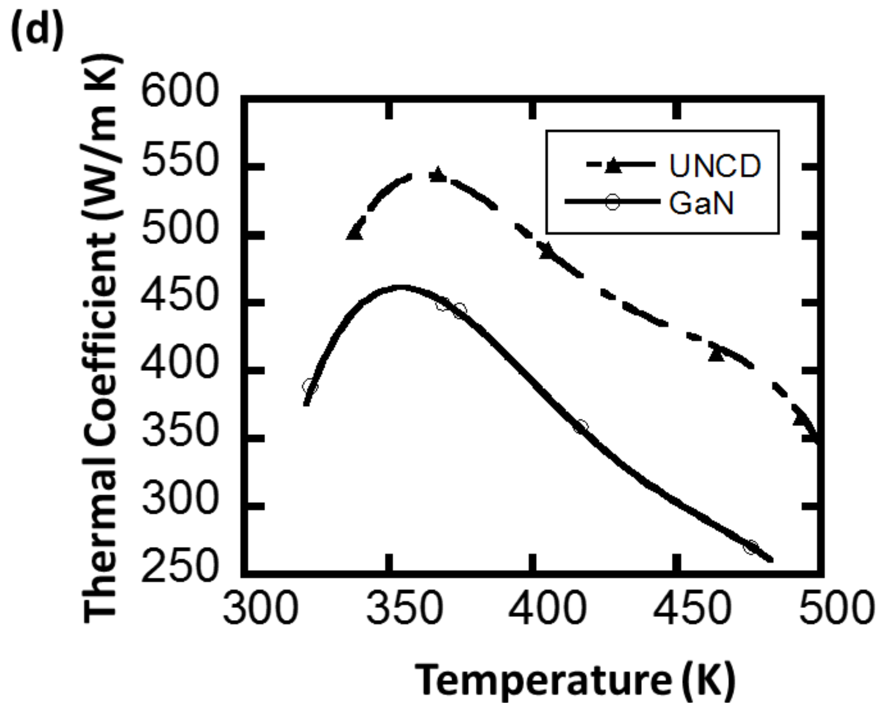


Figure 3.6 Thermal resistors fabricated on the flexible PET film (b) Transient Temperature of thermal resistor of PET with GaN, UNCD, and bare PET at input power 0.35W (c) Temperature of GaN,UNCD, PET at different input power (d) Calculated thermal conduction coefficient of GaN and UNCD at different temperature.

3.5 Transparent AlGaN/GaN HEMTs on PET Substrate

AlGaN/GaN heterojunction structures was grown with 3um GaN layer as the growth buffered layer on top of 800um thick Si substrate. Ti/Al/Ni/Au 20nm/120nm/50nm/50nm was deposited for the ohmic contact layer and was rapid thermal annealed at 850ºC for 30 seconds. The channel is defined through inductive coupled plasma etching with Cl_2/Ar gas flow. Self-aligned Ni/Au 20/250nm T-gate was evaporated through 3 layer (PMMA/LOR300A/PMMA) e-beam

lithography. The channel was then passivated with 10nm ALD Al2O3 and the probing pad Ni/Au 10/300nm was evaporated after opening Al_2O_3 with standard photography steps. The AlGaN/GaN heterostructure is grown on [111] Si substrate by MOCVD, with a 2 um Fe doped high-resistive GaN layer. The as grown sample show a Hall mobility of 2150 cm^2/VS with a carrier concentration of $6.2*10^{12}$ /cm^3. The active region is defined by Cl_2/BCl_3 based ICP etching. Ti/Al/Ni/Au are deposit for ohmic contact by e-beam evaporation, followed by rapid annealed in 850°C with nitrogen for 30s. T-shape gates are formed through standard 3-layer (PMMA/LOR 300A/PMMA) e-beam lithography and Ni/Au metal evaporation. Double finger gate geometry is selected for the compact heat structures. Then the surface is passivated with atomic layer deposited aluminum oxide (ALD Al_2O_3). Ni/Au Source-Ground-Source pad is evaporated at last. After the device is fabricated, the whole GaN film is transferred onto PET film. The finished device is shown in Figure 3.7. In Figure 3.7a, the HEMT/PET sample is placed on the fabric tissue and the fiber from the tissue can be easily seeneen through the sample. An SEM image of double finger microwave GaN HEMT with gate length (Lg) of 400 nm is demonstrated in Figure 3.7b.

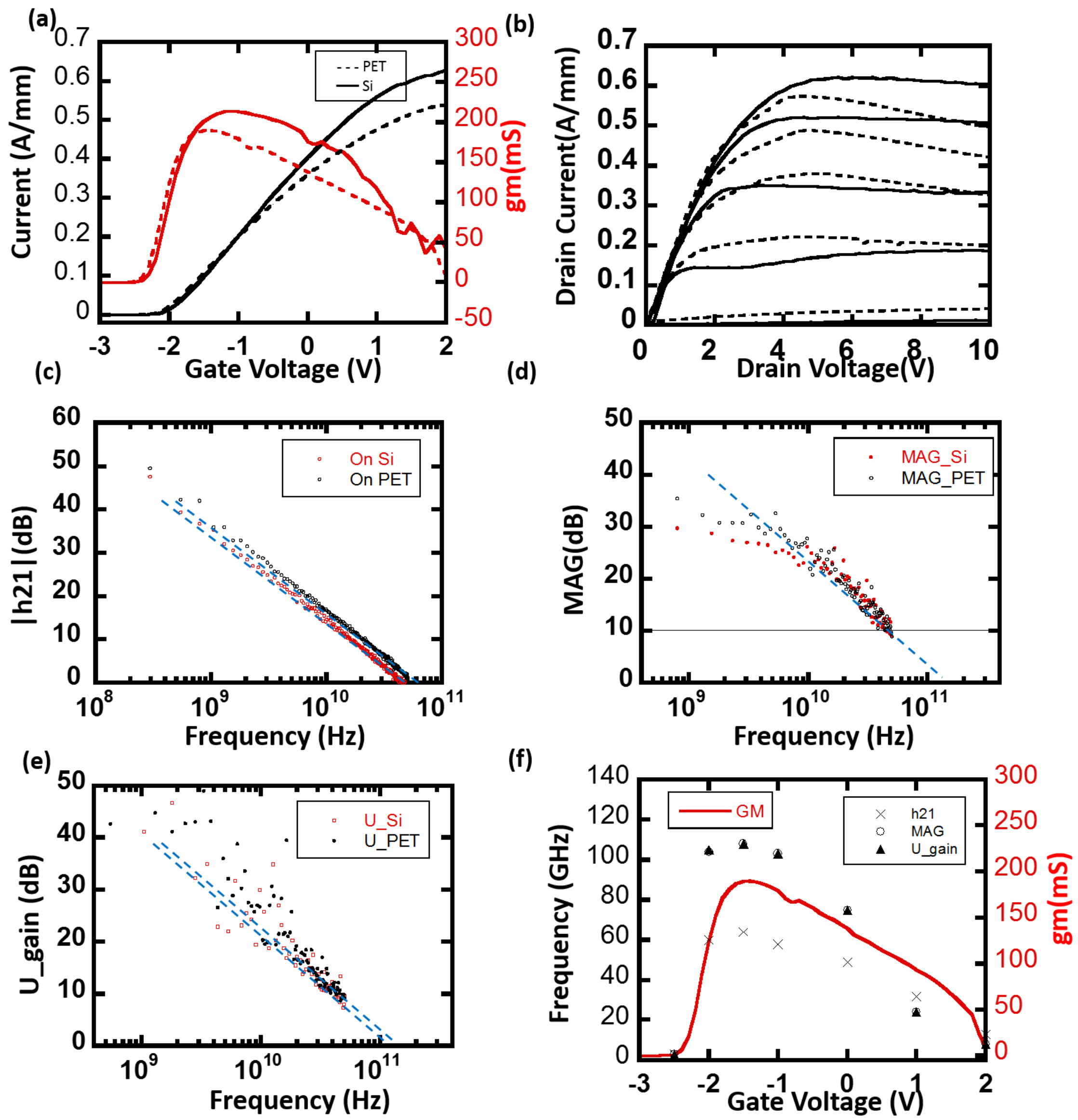
Figure 3.7*(a) optical image of flexible AlGaN/GaN HEMT on PET film wrapped on a cylinder with radius 1.5cm (b) optical image of the device on papers, scale bar=400um (c) SEM image of GaN HEMT with Lg=400nm, scale bar=10um.*

DC measurement and RF measurement is presented in Figure 3.8. In Figure 3.8a, Id-Vg measured on one side of the double finger structure is shown. The ON-resistance of the device is 6.5 Ω mm. The device before transfer shows maximum current of 0.6A/mm, transconductance of 220mS/mm, and threshold voltage of -2V. After being transferred onto PET, the current shows an overall slight reduction, which can be understood by the thermal effect of the flexible AlGaN/GaN shown in Figure 3.8b. Compared to the result before transfer, the saturation current of the AlGaN/GaN HEMT degraded as the voltage bias increased. The saturation current has relatively 10 percent degradation at drain voltage 5 V, and 20 percent when the drain voltage becomes 10 V where the power input is 0.35 W and 0.5W respectively. Thanks to the buffered GaN layer beneath the AlGaN/GaN hetero-junction which serves as the high thermal conductive layer, high power AlGaN/GaN flexible HEMTs are achieved. Considering the low thermal budget of the flexible electronics, the power is large enough to drive the personal wireless communication on wearable electronics.

RF performance of the GaN HEMTs was measured in the range of 0.45 to 50.1 GHz using a network analyzer. For the measurement, the AC signal power is set to -17 dB. The system was calibrated with a short-open-load-through method. On-wafer cold open and short patterns were used to de-embed parasitic capacitances and inductances from the environment. Figure 3.8c,d show the current gain |h21|, maximum available gain (MAG), and unilateral gain (U) against

frequency at Vds = 5 V and Vgs = −1.5 V. Surprisingly, even though the dc performance is lower compared to the results on rigid Si substrate, the cut-off frequency is 60 GHz on PET film increased from 50 GHz on Si substrate. The improvement came from substituting the high RF loss 800 um Si substrate with the lower tangent loss 125 um PET substrate. The small RF signal is then transferred more efficiently without leaking into the substrate. The same results can be observed in the maximum oscillation frequency (MAG) and unilateral gain U. The U gain in Figure 3.8e shows a −20 dB/dec frequency dependence, consistent with the f_{MAX} *extrapolated from MAG, is as high as 115 GHz on PET substrate, compared to 105 GHz before transfer. The frequency response follows the trends of the transconductance measured as shown in Figure 4.8f. In order to study the RF response of the released AlGaN/GaN, small signal approximation is released through ADS simulation. The S-parameter measured on different substrate is plotted in Figure 3.8g.*

The results show that capacitance in the equivalent circuit is significantly reduced after transferring.



(g) **Simulated HEMT parameters**

Parameter	Before	Transferred	Parameter	Before	Transferred
Rg	42.4 ohm	45.9 ohm	Cgs	26.3 fF	38fF
Rd	47.8 ohm	49.2 ohm	Cgd	9.6 fF	5.6fF
Rs	21.7 ohm	23 ohm	Cds	4.6 fF	2.6fF
Lg	98.8 pH	109 pH	Ri	3.2 ohm	3.3 ohm
Ld	35.3 pH	25.9 pH	gm	32 mS	25.8mS
Ls	10.6 pH	9.1 pH	Tau	0.52 ps	0.1ps
Cpg	50 fF	29fF	Rds	960 ohm	930 ohm
Cpd	22.3 fF	13fF			

.

Figure 3.8 *Measurement of the single finger Lg=400nm, Lw=50um, Lc=5um flexible AlGaN/ GaN HEMT devices. (a) Id-Vgs at Vd=5V (b) Id-Vds curve with Vg range from -3 to +2V with step 1V (c) Cutoff frequency |h21|measured under Vd=5V, Vg=-1.5V (d) MAG and (e)unilateral gain U of the Lg=400nm flexible AlGaN/ GaN HEMT devices. (f) Frequency response versus gate voltage (g) s-parameter of before and after transfer and simulated device parameters.*

This can be explained by the lower dielectric constant of PET (3.4) compared with that of Si (11.7). By replacing thick Si with the thinner flexible PET substrate, lower dielectric constant of the structures will result in lower capacitance between electrodes. With good thermal management of the transferred structures, the device performance did not degrade significantly. Hence, the maintained performance with lower parasitic capacitance finally increase f_T and f_{MAX}.

3.6 Summary

We solved the thermal management problem by incorporating single crystal GaN film as the heat dissipation layer. The GaN film transferred onto PET shows heat dissipation capabilities without compromising flexibility and transparency. We demonstrated the availability of high power GaN HEMT on the flexible substrate by transferring the 0.4 um T-gate AlGaN/GaN HEMT on Si through XeF_2 selective etching and PDMS stamp transferring. With the heat dissipation through 3um GaN single crystal film, the flexible HEMT device works under 0.5 W with current density as high as 0.6A/mm and f_{MAX} up to 115GHz. The operation temperature is controlled under the maximum available temperature of the flexible materials. By using the

single crystal membrane as the heat dissipation layer, we opened a path to high power flexible electronics.

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Chapter 4 High Performance Biodegradable Flexible Electronics Based on Cellulose Nanofibril Substrate (CNF)

4.1 Introduction

As the innovation of the consumer electronics, such as cell phones and portable electronics, are being upgraded and renewed every year. The renew of the next generation products has become the driving force in pushing consumers to replace theirs personal electronics based on the trends of the development of the electronics. Due to the reduced lifetime of the electronics, it has been reported, American trashed more than 150’000’000 cell phones in a year[1] and purchased another 120’000’000 smartphones in 2013 [2]. Among all the trashed 150 million cell phones, only less than 10% of the phones are recycled[1]. An 18-month cellphone replacing period generates a lot of waste and non-recycles precious metals used in the products are buried and burned. Whatever remains in the two disposing processes even demands a great potion of landfill to compensate whatever left over. These issues usually cause several serious environment issues.

If we looks into deeper the design of personal electronics, for example a cell phone, the major 90% volume of the component is actually packaging materials: including plastic case, electronics board for carrying the chips, and even the chip packaging plastics. Actually semiconductor chips of the electronics plays only a tiny portion of the volume devise and the electronics circuits inside the chip is even more ignorable. All of these packaging materials occupy most of the volume in a phone and also becomes the majority waste when consumers replaced the phone yearly with the updated model. Even worst, the source of these materials that usually comes from petroleum products that are limited to only to oil producing country. The current approaches to

trash these petroleum products includes underground bury or burning process. Because of the non-biodegradable nature and air-polluting results, a repelling force raise among the resident community have driven the research of adapting renewable, recyclable and even degradable resources. For example, silk, resins, papers, and woods have long been applied to your daily lives and these materials can be degraded naturally in nature and usually result in minimum environment impacts.

In this reason, new materials that are non-toxic and biodegradable in nature, such as paper[3], silk[4] and a number of synthetic polymers[5], have been explored as electronic substrates[6-8]. Many groups have reported electronics on paper by depositing organic semiconductors, but while the concept is very interesting in that it is flexible and degradable, the performance of such electronics falls behind the requirements of state-of-the-art electronics[9]. Another promising approach developed by Hwang *et al*. was to use biodegradable silk combined with high performance inorganic semiconductors[8, 10]. Despite their excellent degradation capability, biocompatibility and performance, silk based electronics is highly vulnerable to water and solvents. Cellulose nanofibril (CNF) is an ecofriendly material as it is completely derived from wood.[11, 12] With its high transparency[13], flexibility[14] and electrical properties[15], CNF is an ideal candidate as an alternative ecofriendly substrate for electronics. Figure 4.1 shows the schematic of directly harvesting the cellulose nano fibril from woods. By gradually exploits the cellulose fiber into smaller fibril, a whole wood bulk can be dissociate into tons of fiber with diameter less than 10nm. The refined fibril have totally different mechanical and optical properties from the woods but is still biological similar to wood in turn of the cellulose composition. In this way, the granted CNF film can be biodegraded by the similar mechanism as the woods, for example fungi degradation. Brown rot fungi is an abundant fungi that naturally

exists in the woods and soil can easily digest cellulose fiber. Hence, by replacing the original non degradable packaging materials with the degradable CNF film, the procedure to discard the electronics could be greatly simplified and caused minimum environment impact.

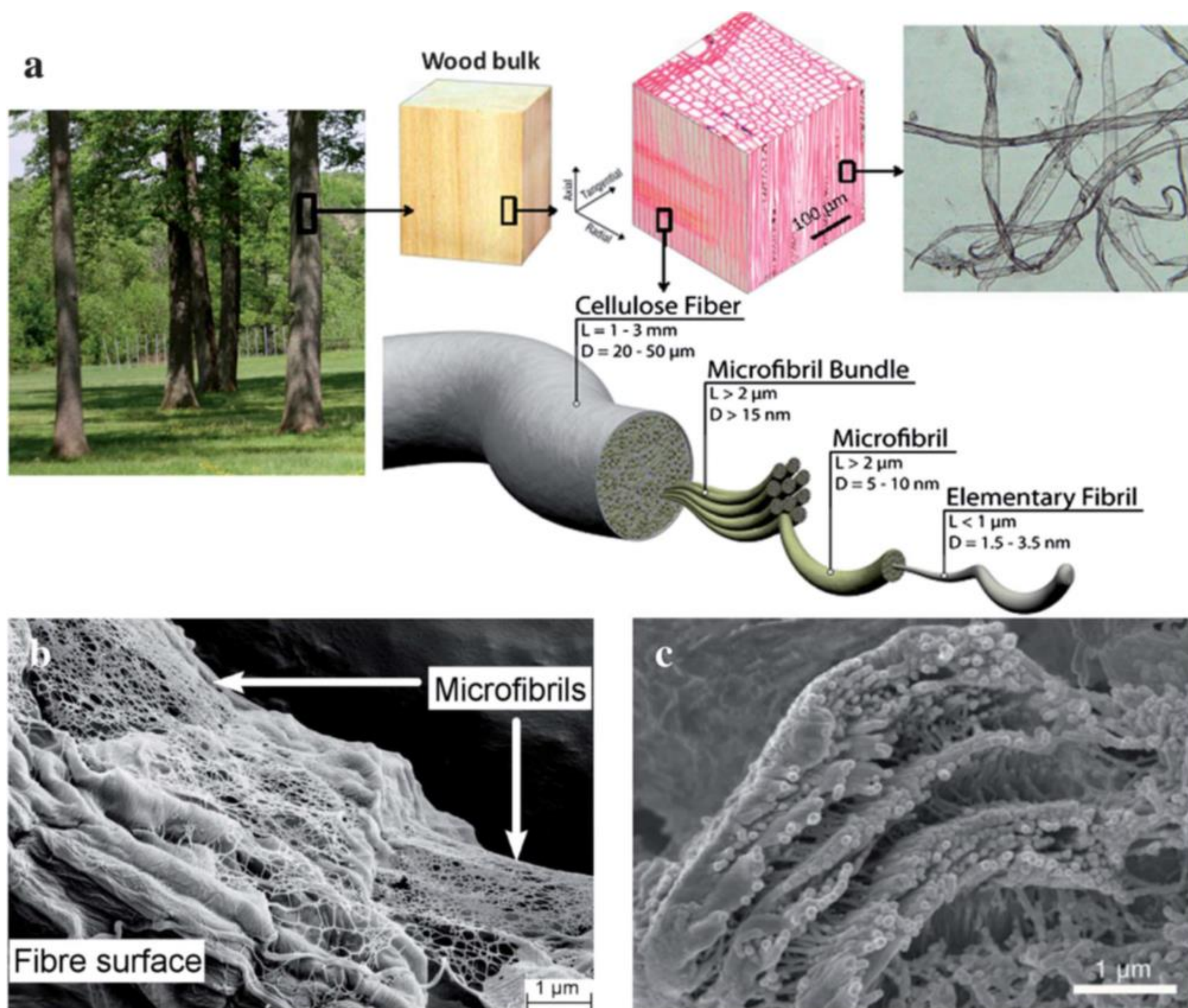


Figure 4.1 *(a) Schematic to show the hierarchical structure of wood fibers. (b) SEM image of the network of microfibrils covering the outer wall layer of the fiber. (c) SEM image of the cross section of spruce fiber to show the micro fibrils with a diameter of 20 nm*[12, 16].

The remaining concern will be the inevitable non-degraded materials that enable functions the electronics. The problems could be easily solved if we take a glance at the structures of the semiconductor chips: a skin-depth circuit that is usually built up on top of a silicon wafer. The actually functional circuits that usually have carrier channels less than an um but are mounted on the rigid semiconductors that are usually several hundred um in thickness. Thus, due to the processing handling issues, those thickness of the handling substrate becomes necessarily to prevent mechanical failure during process. What even worse, the precious Si substrate with several hundred um are usually grinding down at the last step for packaging. Not only the non-necessarily purified Si handling substrate is waste, but the final thin down process generate huge amount of poisonous waste water. In this way, a genius way to minimize the materials used in fabrication, recycle and reuse the precious substrate is necessarily. In this chapter, we will introduce the novel design that first adapting CNF substrate as the final device packaging materials and then a delicate fabrication process that minimize the toxic materials used in the chips by PDMS printing transfer methods. The active materials used in the electronics device are separately prepared and integrated together through release and printing methods onto the handling substrate. Once the device is well fabricated, it is further printing away and the handling substrate can be re-polished and recycled.

4.2 Preparation of CNF Substrate and Characterization Methods

To prepare the CNF film, the tetramethylpiperidine-1-oxy (TEMPO) oxidized CNFs are refined in a Microfluidizer processor (Microfluidics, Newton, MA), followed by filtering (Millipore Corporation, USA) under an air pressure (0.55 MPa) with polytetrafluoroethylene

(PTFE) membranes that have 0.1 μm pore sizes[17]. Subsequently, the filter cake is separated from the membrane and sandwiched between layers of waxy coated paper, filter paper, and caul plates at room temperature for drying, followed by further drying in an oven at 60 ℃ for several hours. The dried CNF film is then coated with bisphenol A based epoxy resin (Dow Chemical Company, 56:24:24 mixture of low viscosity epoxy resin, flexible epoxy resin and amine-based curing agent) and pressed at 130 ℃ for ten minutes under 100 psi pressures. The well fabricated CNF film is shown in Figure 4.2.

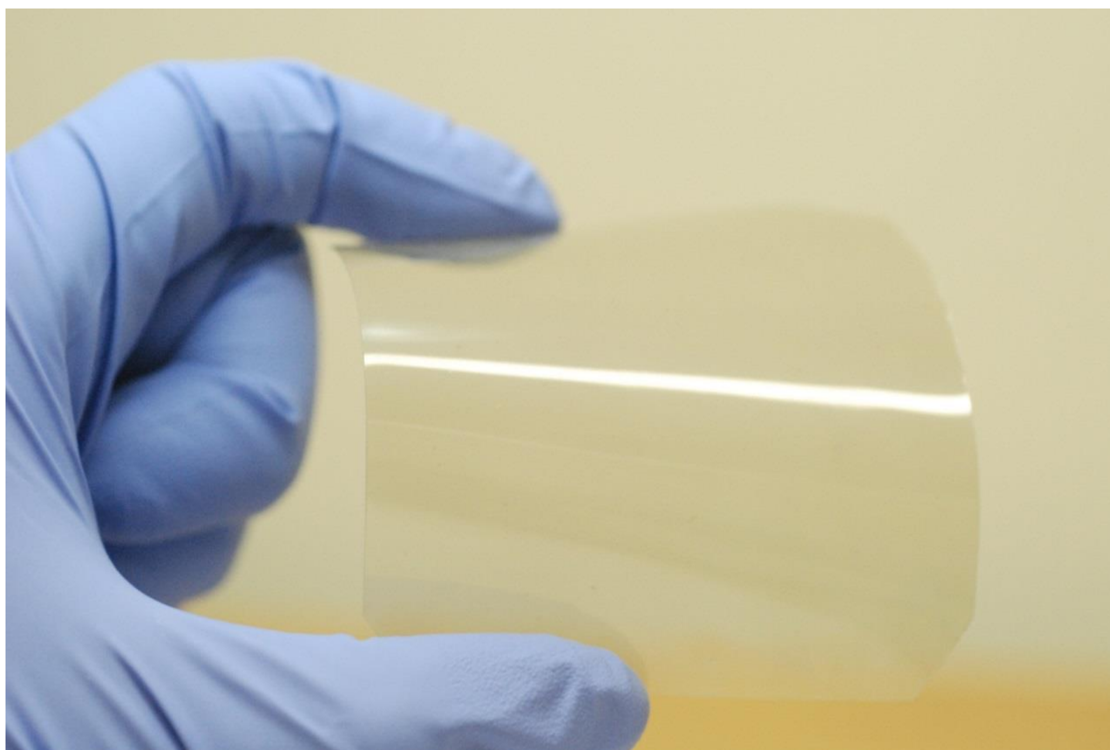


Figure 4.2 *Thin film 80um CNF film with highly transparency and flexibility is demonstrated.*

4.3 Physical and Biodegradable Properties of CNF Substrate

To measure transmittance, CNF film with a thicknesses of either 80 μm or 200 μm was loaded into a FTIR chamber. System was set to a transmission mode and the transmittance was recorded every 1 nm through spectrum from 200 nm to 1200 nm. The thermal stability of the epoxy coated CNF films were characterized via thermogravimetric analysis (TGA) using a TGA/Q50 thermal analyzer (TA Instruments, DE USA). Approximately 10 mg of the CNF films were heated from 30 to 600 ℃ at a heating rate of 10 ℃/min in an N_2 atmosphere. UV-vis absorbance was measured using a Varian Cary 5000 Bio UV-visible spectrophotometer. Differential scanning calorimetry (DSC) was performed in an N2 atmosphere using a Q20 DSC thermal analyzer (TA Instruments, DE USA) from 0 to 160 ℃ at a heating rate of 5 ℃/min and a N_2 flow rate of 20 mL/min. The DSC sample (about 8.0 mg) was stored in a sealed aluminum pan. To measure the electrical breakdown characteristics, metal (Ti/Au, 10/200 nm) was evaporated on both sides of a 200 μm thick CNF film via a shadow mask, with a pad of 300 μm in diameter. High voltage was applied using a Keithley's 2410 voltage source through standard DC probing while the current was monitored. To measure the dielectric constant and loss tangent, the microstrip transmission line-approximation-method is used. A square CNF film with an area of 17.64 cm^2 was attached with a copper film as the ground on the back side, and a 6 mm wide copper tape on the center of the top side. S-parameters were collected through the SMA connectors as RF signal is transmitted through the microstrip transmission line. Dielectric constant and loss tangent of the CNF film were then extracted according to the ADS small signal circuit approximation.

Pure CNF paper is vulnerable to bioorganic germs and fungi, and permeable and swellable to water and various solvents[32]. To address this issue, pure CNF paper was coated with bisphenol, a based epoxy resin, which made the resulting CNF film highly resistant to bioorganic

and solvents while providing further improvement in its mechanical properties. This treatment allows for easier handling of the CNF substrate and offers better manufacturing capabilities.

Paper is made of cellulose nanofibril with fiber diameter around 20um, covering all the rage of the visible wavelength. With the fiber size large like this, the surface of the paper is rather rough. This aggregate the incident light to transmit through the paper and cause the paper to become non transparent. In order to general film with much better optical properties, carbon cellulose fiber is usually dissociated into smaller diameter to improve the optical properties[7]. In this way, CNF film becomes gradually transparent through light scattering as its fiber component has diameter to several nm meters. As shown in Figure 4.3, the CNF paper is transparent and highly bendable that is different from a regular paper, making it ideal for certain applications. The transmittance is over 80 % for an 80 μm thick CNF film and 60 % for a 220 μm *thick CNF film* over the visible spectrum.

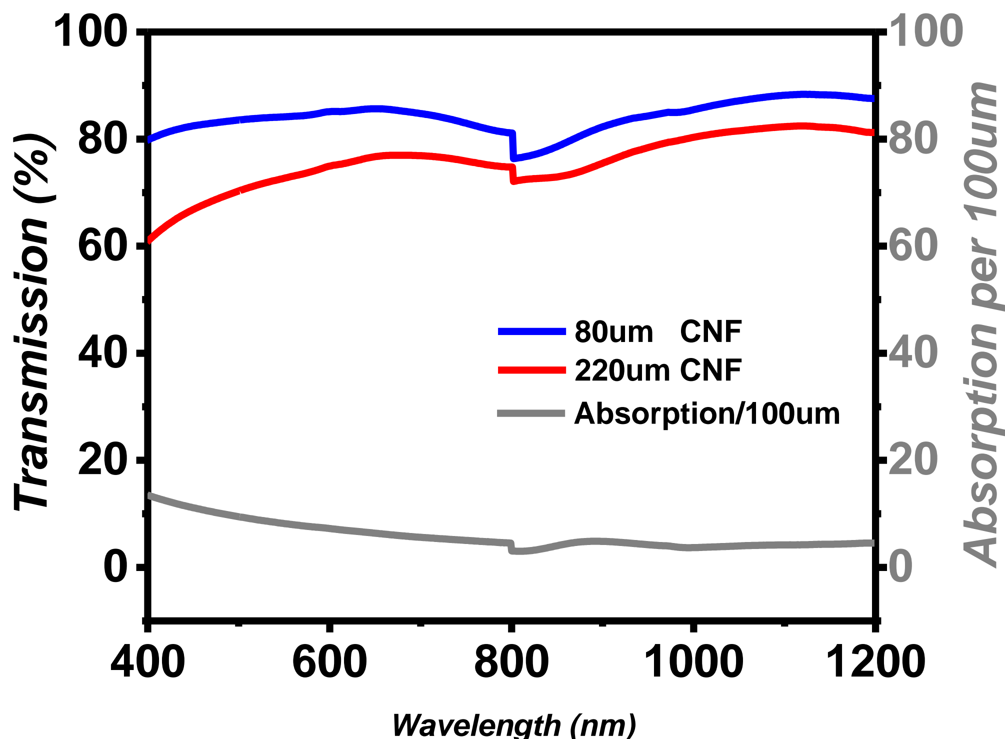


Figure 4.3 *Optical properties of CNF substrate with thickness 80um and 220um.*

The overall broadband absorption percentage per 100um average lower than 10% and slightly increased to 12% around the UV light range. The optical properties of the generated CNF film is more than 4 times the transparency of the reported data[17, 18]*. Surprising, the dense packed CNF film, after hot embossing to drain the containing water, is totally transparent and does not have the scattering effect as those reported CNF film with fiber diameter equals or above several nanometers*[18]*. This could be inferred by the even smaller dimension of our cellulose fiber. We believed the increased optical properties is achieved through more uniform dispersing* cellulose nanofibril *uniformly and the firmly embossing post processing step at higher temperature.*

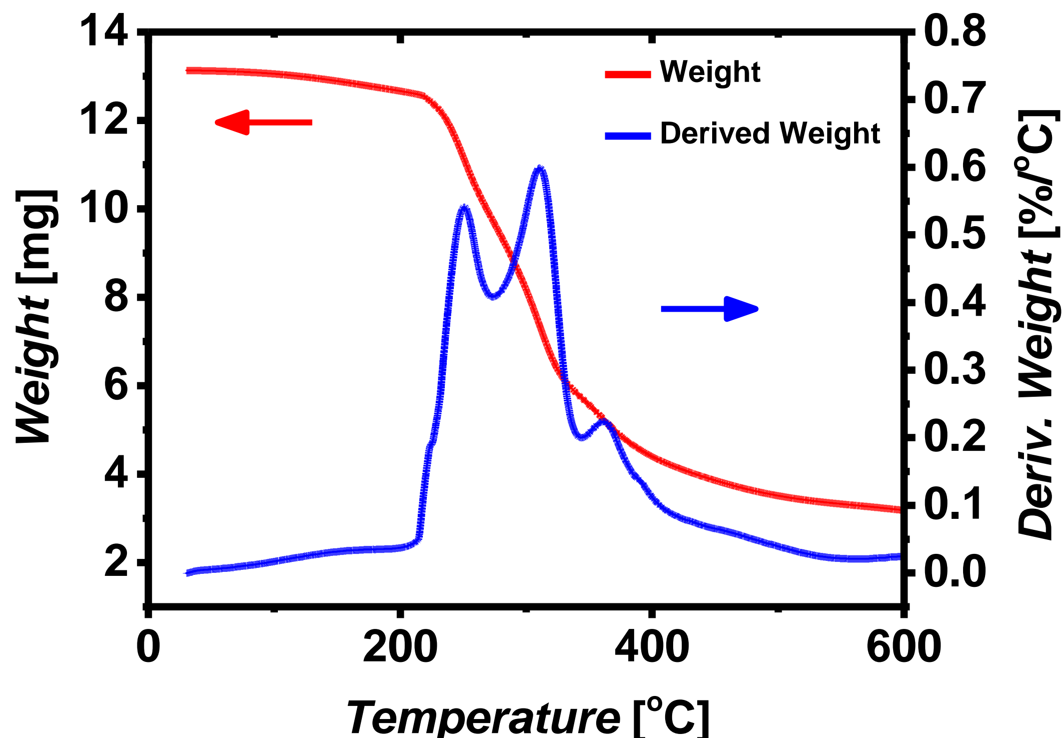


Figure 4.4 TGA and DTG of the fabricated CNF substrate. Dissociated temperature of three component located at 220ºC, 310ºC, and 340º corresponding to the degradation of CNF, epoxy, and carbonization of CNFs, relatively.

Figure 4.4 presents a thermogravimetric analysis (TGA) data showing the weight loss of the epoxy coated CNF film as a function of temperature. In TGA data, the CNF film remain semi-stable and show constantly dehydration starting from 60ºC to 200ºC. At this stage, the moisture residues and moisture components that naturally happened in the cellulose fiber are gradually evaporated into the ambient. First noticeable sharp change in weight percentage can be found at 220℃. From TGA curves, as well as the first derivative (DTG). As shown in the DTG curve, the CNF/epoxy film showed three weight loss processes, with the first degradation taking place at a temperature of 213 ℃~220℃, which was attributed to the decomposition of CNFs in the

CNF/epoxy film[17]. The decomposition of epoxy started at 270 ℃ and peak at 310oC. The last peak at 340ºC corresponds to carbonization of the CNF and epoxy and the collapse of the cellulose structures. Glass transition temperature (T_g) of the film was measured to be 72.77 ℃ (Figure 4.5), which is slightly similar to that of polyethylene terephthalate (PET).

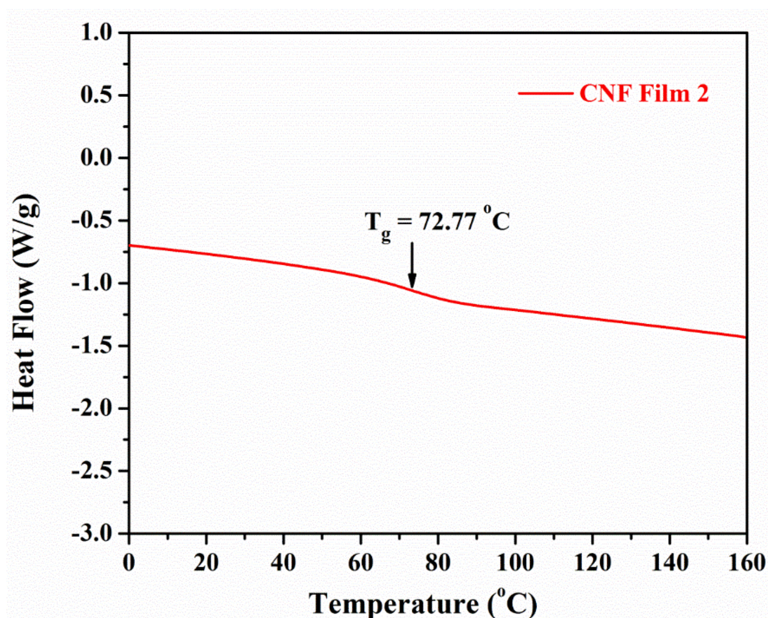
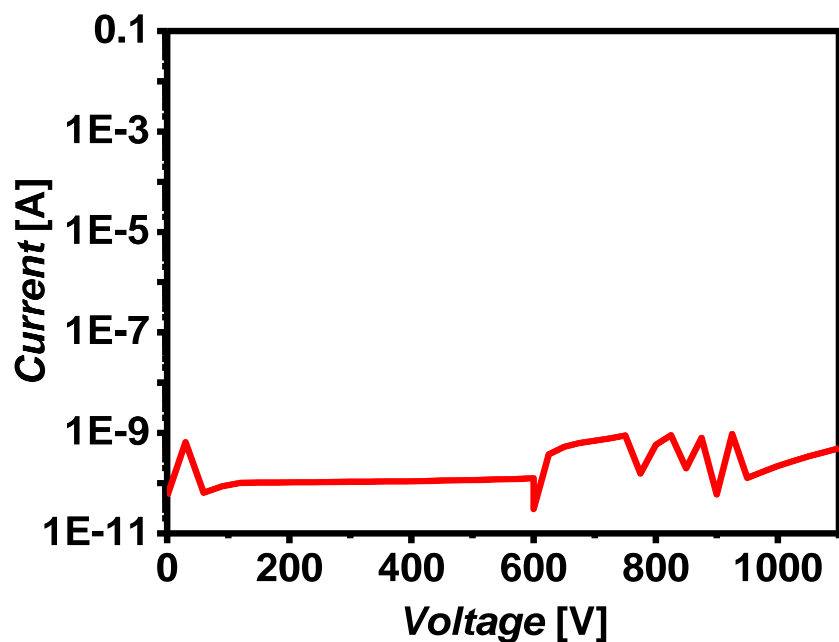


Figure 4.5 *The differential scanning calorimetry (DSC) curve of the epoxy coated CNF film obtained during the second heating cycle.*

The electrical properties of the CNF film is also an important factors to be used for the high performance electronics. Here, we test the breakdown voltage, dielectric constant, and the RF loss properties of the CNF film. To test the breakdown voltage, Ti/Au 10nm/100nm was e-beam evaporated on both side of the 100um CNF film with a pre-fabricated Si shadow mask to form 200um by 200um squares patterns. As presented in Figure 4.6, the CNF film does not undergo an electrical breakdown even at very high voltages (e.g., 1100 V), which is far beyond the requirement for consumer electronics. Furthermore, because the dielectric properties of the substrate are a major aspect to be considered in designing for high performance electronic circuit,

for example the radio frequency (RF) loss and dielectric constant were extracted using a microstrip waveguide and analyzed at high frequencies. To analyze the results, In the frequency range from 0 to 10 GHz, the dielectric constant ranged from 2.58 to 2.69 and the loss tangent ranged from 0.0302 to 0.0415, as presented in Figure 6.7c. These values are comparable to those of PET film, which is commonly used as substrates for flexible electronics.



(b)

(c)

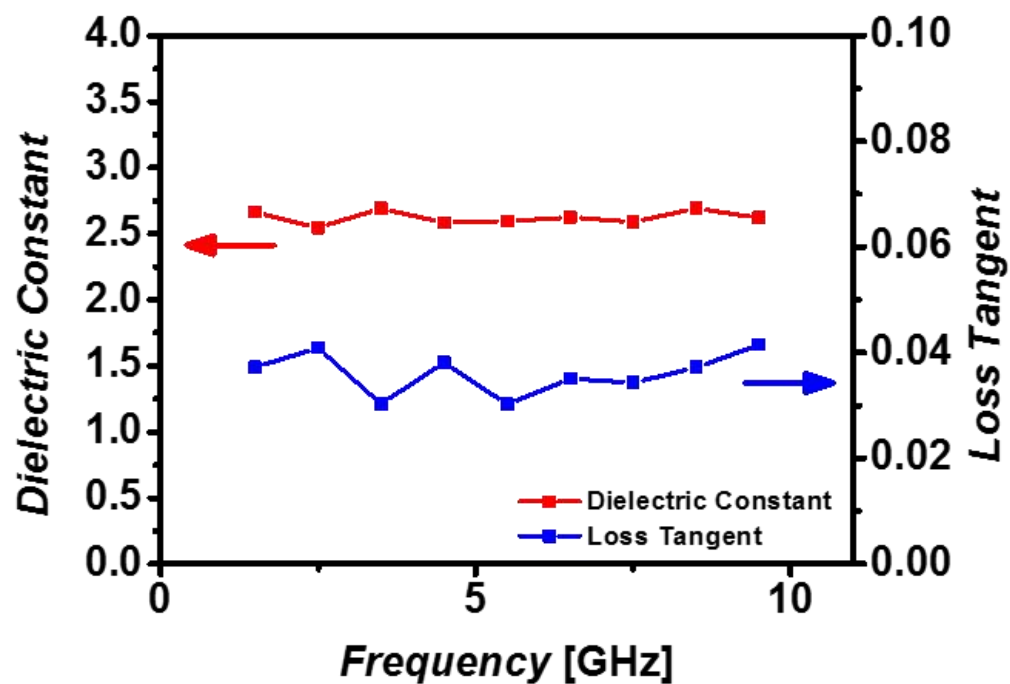


Figure 4.6 *Electrical properties of CNF substrate (a) Breakdown measurement at film thickness 100um (b) optical image of microstrips waveguide used in simulation (c) dielectric constant and tangent loss from frequency 1~10 GHz.*

Prior to integrating the CNF substrate into our applications, the degradability of the film is tested with different fungi and epoxy coating. The goal is to maintain the biodegradability and acceptable resistivity to moisture/solvent during usage/fabrication process. In order to generate a reliable and repeatable fungi biodegradability experiment, the degradation control follows the American Wood Preservers' Association (AWPA) E-10-06 Standard, where the degradation environment is sealed and maintain moisture constant in moisture and light control incubation room. Figure 4.7a shows the typical wood degradation test with fungi sealed bottles. Here, instead of using woods chuck and soil, we simplify the controlled environment to transparent sealed petridish, for better monitoring, single fungi environment, instead of soil, with background agar to support the eco system. First, two different types of decay fungus, postia placenta and phanerochaete chrysosporium, were considered and tested on the pure CNF substrate and on the epoxy coated CNF substrate. The reasons of choosing these two fungi are because they are the most common brown rot fungi and white rot fungi exist in nature and could most represent the nature environment. To prepare for a fungal degradation test, the decay fungus was maintained on 2% malt agar. Inoculum was incubated at 27 ℃ in a 70% relative humidity room for 2 weeks to obtain confluent growth on petridish. Meanwhile, the CNF substrate went through a 24 hours cleaning process in a propylene gas chamber to remove any germ and spore contamination. The cleaned CNF substrate was then laid inside of the petridishes with the fungus and incubated and observed. The degradation process in shown in Figure 4.7b and Figure 4.7c.

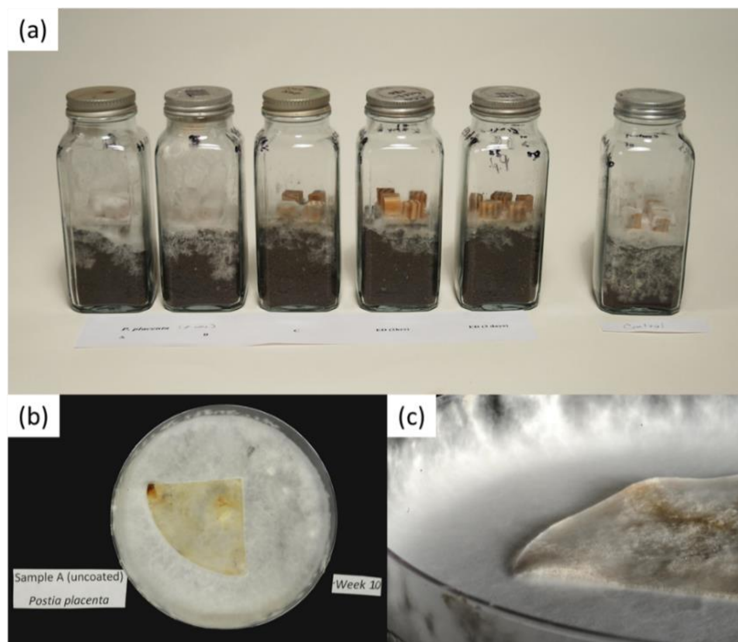


Figure 4.7 *Examples of Standard Wood Degradation E-10-06 Standard. (a) The samples are sealed in control environment and stored in humidity control incubation room. (b) Modified fungi degradation experiment for CNF film (c) a closer view of degradation of CNF under 10 weeks.*

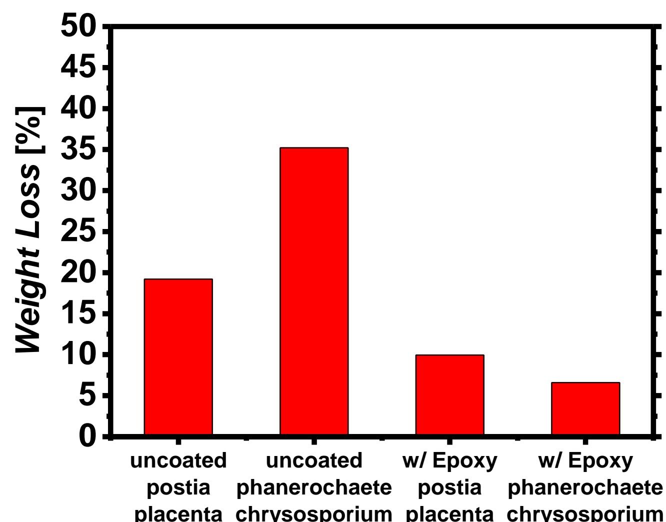


Figure 4.8 *CNF film weight loss calculation with controlled degradation test for 8 weeks. Different control condition with/out epoxy and degradation with different fungi is compared.*

Figure 4.8 presents the average weight loss percentages of the CNF films after 2 months. Pure CNF samples showed a larger weight loss (postia placenta: 19.2%, phanerochaete chrysosporium: 35.2%) compared to the epoxy coated samples. While postia placenta induced a slower degradation rate for pure CNF film, it caused a faster degradation for the epoxy coated CNF film (postia placenta: 9.96%, phanerochaete chrysosporium: 6.6%) in comparison with phanerochaete chrysosporium. The ability of brown rot fungi, posita placenta, to penetrate through epoxy to degrade the CNF film is stronger. Therefore, postia placenta was chosen as the decaying agent for our CNF electronics, which consisted of the epoxy coated CNF film. The amount of epoxy in the epoxy coated CNF film was 9.6% by weight.

4.4 Fabrication Process of Releasable Digital Adder with Minimum Active materials

Before going to the details of the fabrication, it should be noted that the amount of semiconductor materials that actually participate in functioning the electronics is only within the skin depth of the total semiconductor wafer. An apple and its peel would perfectly describe scenario. Not just the depth of the channel in actually semiconductor are shallow, the actually planar area is not utilized efficiently. The proposed fabrication schematic show in Figure 4.9 could explain the idea easily. In the proposed process, the active membrane that will be used in the full devices are individually prepared on it source substrate, where SOI substrate is prepared for the easy release-and-printing procedure. Here, we intentional separate PMOS and NMOS membrane in two SOI source wafers to demonstrate the ability of printing active membrane with different purpose to unite together for the final device, a 2 bit full adder in this dissertation.

In the process, n-type and p-type active region for CMOS are prepared separately on the p-type (4×10^{15} cm^{-3}) and n-type (5×10^{14} cm^{-3}) SOI wafers. Before ion implantations, 20 nm of thermal oxides (Tystar Oxidation Furnace) are grown on both n- and p-type SOIs for screen oxides. A uniform ion implantation is followed to slightly raise the doping concentration of the active region to minimize channel resistances and adjust the threshold voltage of the MOSFET. The detail of the ion implantation is list in Table 5.1.

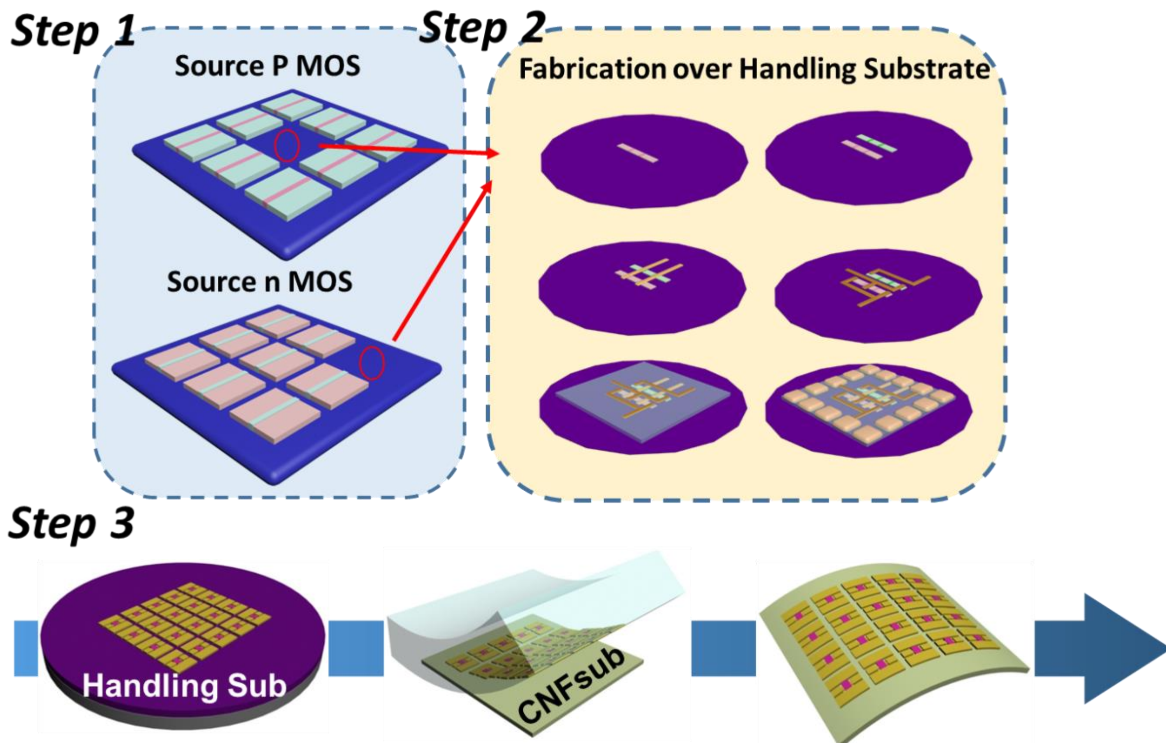


Figure 4.9 *Schematic of proposed fabrication process that use minimum active membrane and recyclable handling substrate. Step 1: the active membranes for both PMOS and NMOS are separately ion implanted in separate SOI wafer and later printing to the handling substrate to assemble a complete CMOS structure. STEP 2: after the fabrication on the handling substrate; Step 3: the device is printed again to the CNF substrate with adhesive. The handling substrate is re-polished and printed again with next batch of membrane.*

Target	**Initial substrate** [Type/Si thickness/BOx thickness]	**Implantation condition** [Dopant/Dose/Energy/Tilt angle]	**Screen oxide thickness**	**Anneal condition** [Temperature/Gas/ Time]
NMOS Channel	p-type/ 205 nm/ 400 nm	Boron (P)/ 4×10^{12} cm^{-1}/ 20 keV/ 7 °	20 nm	950 °C / N_2, O_2 / 30 min
NMOS Contact	p-type/ 205 nm/ 400 nm	Phosphorus (N++)/ 5×10^{15} cm^{-1}/ 20 keV/ 7 °	20 nm	950 °C / N_2, O_2 / 10 min
PMOS Channel	n-type/ 260 nm/ 600 nm	Phosphorus (N)/ 4×10^{12} cm^{-1}/ 20 keV/ 7 °	20 nm	950 °C / N_2 / 5 min
PMOS Contact	n-type/ 260 nm/ 600 nm	Boron (P++)/ 1×10^{15} cm^{-1}/ 10 keV/ 7 °	20 nm	950 °C / N_2 / 5 min

Table 4.1 *The specs of SOI wafer and ion implantation process for 2 bit full adder is listed. Both PMOS and NMOS have two steps ion implantations for channels doping level and Ohmic contact purpose.*

A short thermal annealing in a furnace is applied to recover the defects generated from the implantation and activate the dopants. A heavy ion implantation is applied on the photolithography pre-defined Source and Drain region. After second thermal annealing in the furnace, active regions on the SOI wafers were isolated using reactive plasma etching (Unaxis 790). The SOI wafers are then placed in diluted HF (1:10) solution to etch the sacrificial buried oxide layer and release the membrane. Polyimide (~1 *μm)* is spin casted and cured on a 60 nm thick PMMA coated Si wafer. Soft bake of 1 minute at 100 ℃ dries out the solvent while maintaining adhesive surface. Individually released membranes from each type of the SOIs are aligned and transferred separately onto the polyimide using a PDMS stamp mounted on a modified mask aligner (Karl Suss MJB3), followed by hard bake at 300 ℃ for 1 hour in a vacuum oven. A standard source/drain metal pad, dielectric layer, via hole openings, and gate process for CMOS fabrication are processed on the temporary substrate. A second PI layer is

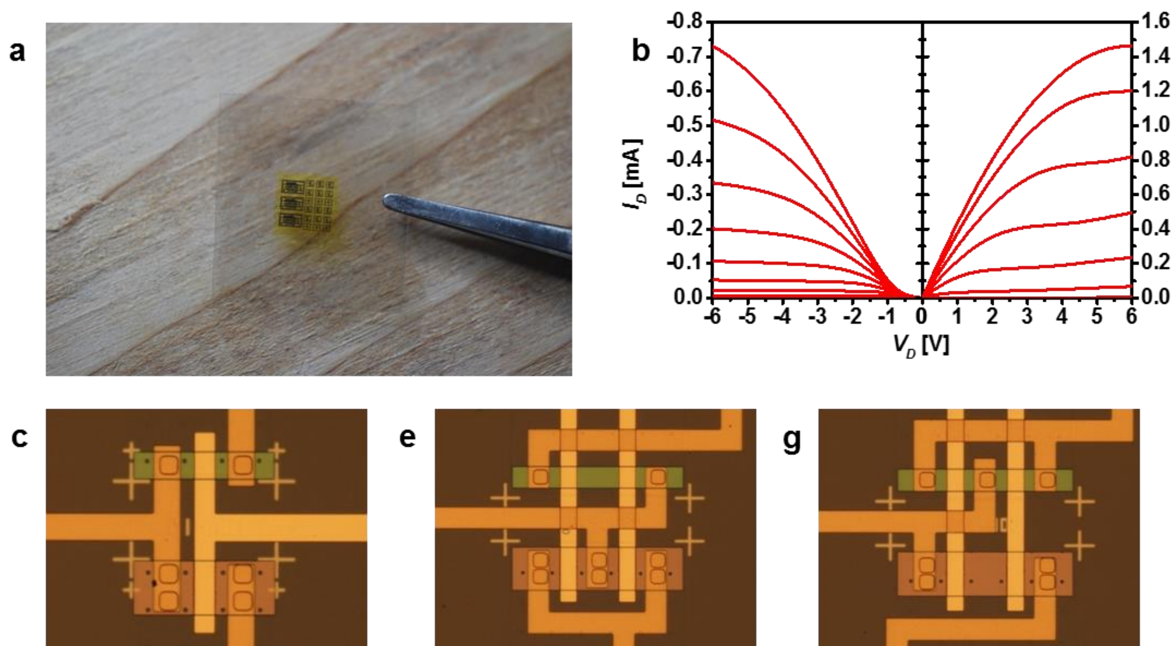
coated on the surface for passivation and protection followed by via hole etching for measurement pads.

After the full devices are fabricated, the handling Si substrate is immerse in boiling acetone at 200 ℃ removed the underlying PMMA sacrificial layer for the electronics (HBT, Schottky diode, inductor & capacitor, digital electronics) fabricated on a temporary substrate. A large PDMS elastomer stamp was used to transfer print the finalized device onto a CNF substrate with a thin layer of polymer (SU8 2000.5, Microchem, 500 nm) as adhesive.

4.5 Performance of Biodegradable Electronics on CNF Substrate

DC measurements were performed using an HP 4155B Semiconductor Parameter Analyzer, and a cyclic voltage generator is used for sending the control signal to the input of the digital devices. Figure 10 summarizes a set of digital electronic circuitries on a CNF substrate using silicon based complementary metal-oxide-semiconductor (CMOS) devices. The Si membrane with p-type and n type transistors, where the I-V curves are shown in Figure 10b, separately transfer printed onto the CNF substrate from different silicon-on-insulator (SOI) wafers and finished with metallization to form a circuit. Figure 5a shows the completed digital circuit on a CNF substrate, which includes ‘universal’ logic gates (Inverter, NOR gate, and NAND gate) and a full adder. Due to the different type of doping level and thickness of the Si membrane, we can clear distinguish the channel membrane of PMOS (red) and NMOS (blue). Figure 10c shows an optical image of the CMOS inverter. As presented in Figure 5d, the inverter exhibits a good input and output relationship. A further modelling of these CMOS transistors established NOR and

NAND logic gates, which are optically shown in Figure 10e and 10g, respectively. The input and output relationships of NOR and NAND gates are shown in Figure 10f and 10h, respectively, where the inputs and outputs can be seen as well-defined “0” and “1”. All of these components can be used together to yield a simple integrated circuit on a CNF substrate. As an example, a full adder, which is highly scalable and useful in many cascaded circuits, is designed and fabricated on a CNF substrate, as optically shown in Figure 5i. Here, the full adder is a mirror full adder, which consists of 28 transistors with 4 of them used for inverter construction. As presented in Figure 10j, the two single bit outputs (SUM and Carry Out) has a 0.2ms switching delay when responding to the three single bit inputs (Input A, Input B, and Carry In). This makes the 2-bit full adder working at frequency up to 5kHz.



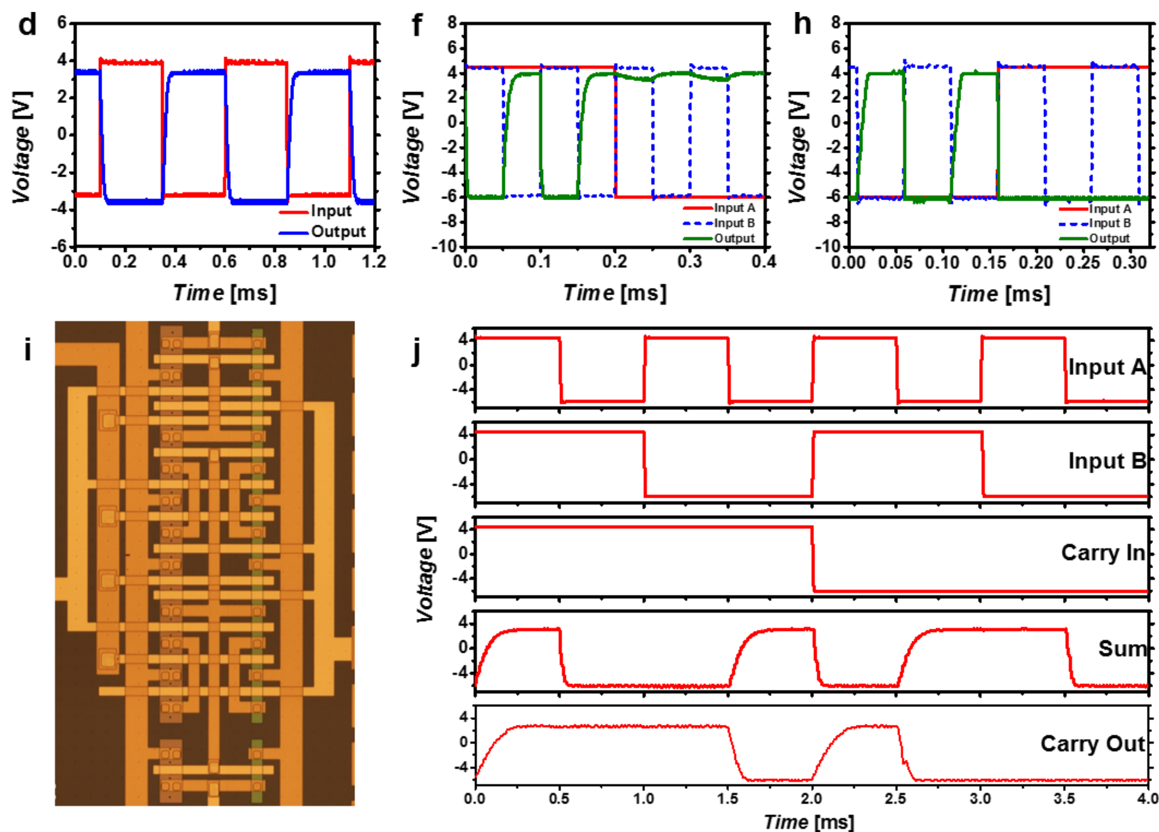


Figure 4.10 *Digital electronics on CNF paper. (a) A photograph of a CNF paper with digital electronics. (b) ID vs. VD plot of a p-type MOSFET (left) and an n-type MOSFET (right) with VG steps of 1 V. (c) An optical microscopy image of an inverter. (d) Input-output characteristics of the inverter. (e) An optical microscopy image of a NAND gate. (f) Input-output characteristics of the NAND gate. (g) An optical microscopy image of a NOR gate. (h) Input-output characteristics of the NOR gate. (i) An optical microscopy image of a full adder. The adder consists of 28 transistors. (j) Characteristics of the full adder, Input A, Input B, Carry in, Sum, and Carry out are shown in the descending order.*

4.6 Degradation of CNF Film with Digital Device

Figure 4.11 shows the images of the decaying process of a CNF substrate with digital electronics. Photos were taken after 6 hours, 10 days, 18 days and 2 months. The brown rot fungus started to partially cover the sample after 10 days and fully covered the sample after 2 months. Figure 4.12 summarize the results of four different sets of decaying test for digital electronics on CNF substrates using postia placenta. Weight losses were obtained by measuring the mass after 2 months of the decaying process. On average, the weight loss percentage after 2 months was 12.25 %, suggesting that the CNF film may fully degrade after an extended period. Once degraded, the left over electronics portion which is encapsulated in biocompatible polyimide can be collected to be decomposed and recycled.

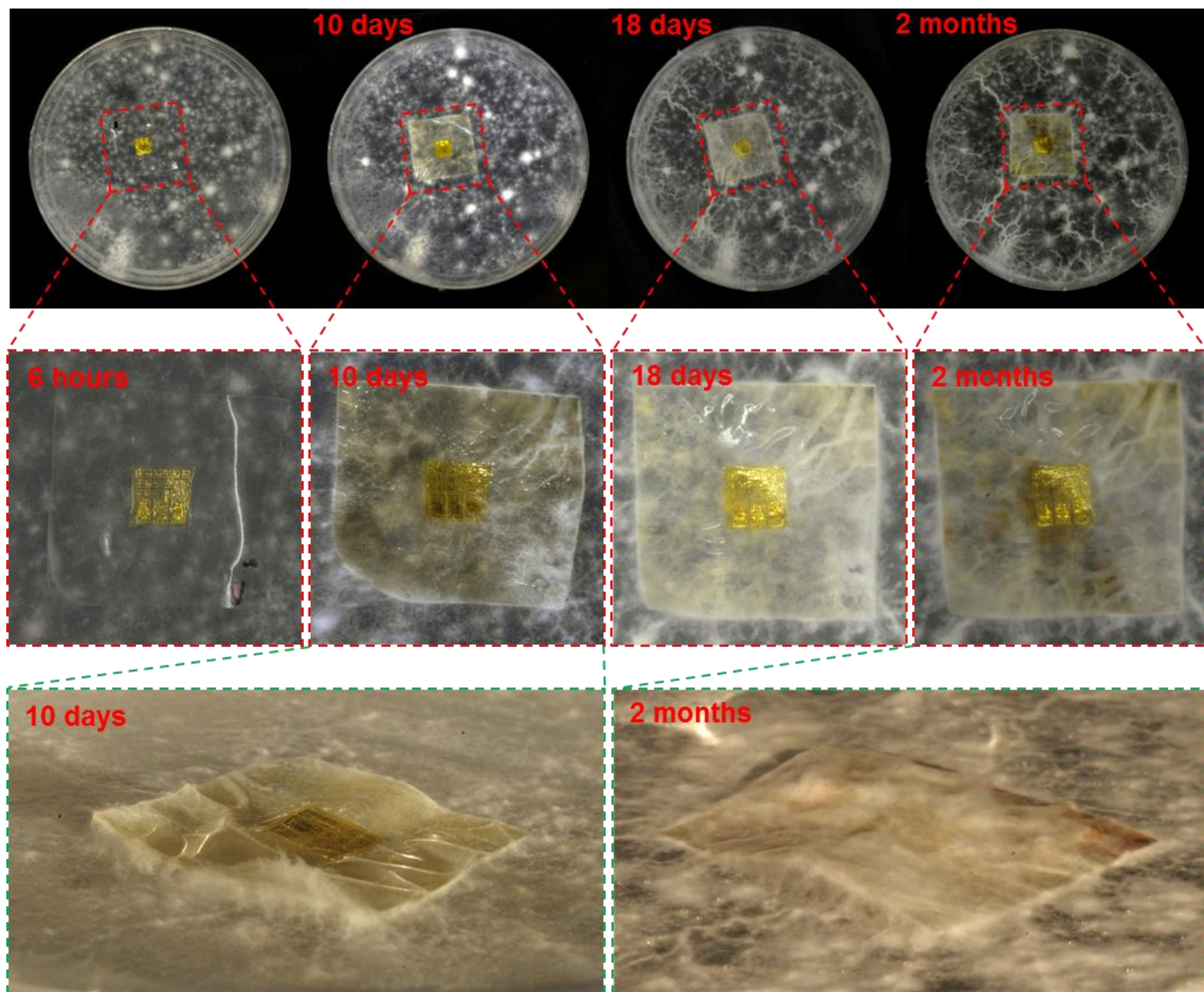


Figure 4.11 *A series of photographs taken at 6 hours, 10 days, 18 days, and 2 months after starting the degradation process. (d) A series of magnified photographs of the CNF electronics during degradation process. (e) Tilted view photograph of the CNF electronics after 10 days and 2 months of degradation. The fungus fully covers the film after 2 months.*

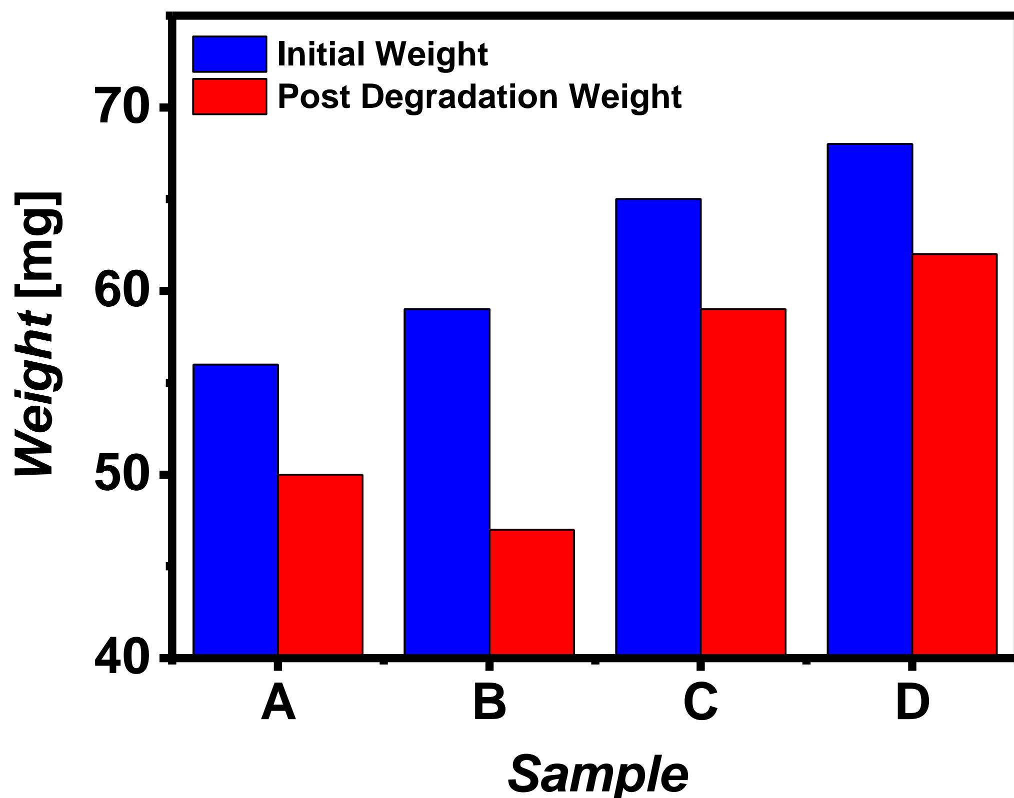


Figure 4.12 *Biodegradation of four of the digital devices mounted CNF film in the posita placenta environment. The average weight loss of the CNF film for 2 months equals to 12.25%. The degradation results matches the previous degradation test with the average loss of 9.96%.*

4.7 Summary

In summary, we demonstrate the capability of fabricating environment friendly electronics with the following features together: ability of assembling CMOS from separate PMOS and NMOS wafer, minimum use of the environmental toxic materials, recyclability of the semiconductor handling wafer, disposability and degradability with minimum landfill

requirement. Without flaming the e-waste and generate air pollutant, the precious materials in the e-waste could be recycled after naturally degradation in soils.

4.8 Reference

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Chapter 5 Conclusion and Future Work

5.1 Conclusion

In this dissertation, we investigated the application of 2D materials in nanofabrication, power management on the flexible substrate, and wood-enabled renewable flexible electronics by examining large area BCP assembly with assistance of atomic thin layer chemical pattern, high power fast flexible electronics with transparent AlGaN/GaN HEMTs on plastic substrate, and biodegradable flexible electronics with renewable cellulose nanofibril substrate.

Photolithography based on spin coating chemicals and optical exposure have faced substantial challenges in the feature size below 10nm. Directed DSA of BCPs have been proposed to replace the exposure techniques in the sub-10nm fabrication but still facing similar problems of preparing spin coating polymer based chemical pattern. We propose replacing the traditional spin-coated-polymer chemical pattern with the uniform chemical vapor deposited 2D materials and demonstrate that the new technique not only maintains the original advantage of DSA but outperforms the polymer based chemical pattern in commensurability, thermal dynamics, mismatch tolerance, and density multiplication. Compressibility and stretchability of 15% and 13%, 90 degree of mismatch pattern, 10x density multiplication, and several times faster in thermal dynamics assembly have been demonstrated. The DSA assembly of LS=25nm PS-*b*-PMMA based on thermal annealing and LS=16m P2VP-b-PS-b-P2VP based on solvent annealing have been demonstrated. After pattern transferring the DSA pattern to the SOI wafer, the fabrication of 8nm Si FINFET has been demonstrated.

In the follow-up session, the challenge of adding power electronics elements into flexible electronics has been identified: reliable approaches to thermal management on flexible

electronics and reproducible way of transferring high power materials to flexible substrate. The need of a highly efficient thermal dissipating layer has been simulated at the input power 0.5W through COMSOL simulation tool. The simulation results imply the need of a thermal dissipation layer with thermal conductivity over 100W/mK to accommodate the poor thermal properties of flexible substrate and soft materials. The materials with these kinds of thermal conductivity are generally categorized as metal or crystalline materials with good phonon scattering. Hence, we combine the XeF_2 with the standard PDMS printing transfer process to present a large scale GaN membrane transfer process. An 8*8mm transparent GaN film printed on the flexible substrate shows good thermal conduction and the AlGaN/GaN HEMTs embedded on top of the GaN membrane show improved RF characteristic after it is released and printing on the flexible substrate. The speed of f_{MAX} = 115GHz and f_T = 60GHz have been demonstrated without any thermal degradation during functioning, which leads to the potential to realize amplifiers on flexible substrates.

Finally, the life cycle and environment impact of frequently renewing flexible electronics have been discussed. In order to generate disposable flexible electronics, the amount of toxic materials used in the device and fabrication process should be minimized to above the underground contamination. Additionally, volume occupied packing materials should be degradable once the electronics are discarded. The idea is finally carried out by introducing the CNF as packaging materials from renewable wood source to replace the non-degradable petroleum product. With the delicate fabrication process that separates the source materials from the handling substrate, the digital devices with minimum active materials have been embedded on CNF substrate. The 2 bit full adder and universal logic elements based on CMOS have been test and measured from separated PMOS and NMOS and whole device shows high degradability by the nature enriched

brown-rot fungi. Flexible electronics with minimum landfill disposal requirement and high recyclability have been demonstrated.

5.2 Future Work

We have investigated the advantage of integration 2D materials into the BCP self-assembly and how it favors the wafer scale mass production of next generation sub-10nm electronics in chapter 2. In the demonstration, wafer scale single crystal graphene grown on Ge wafer is chosen to compare to the general spin coated PS based chemical pattern. The requirement of minimum concentration of solution used the spin coated on wafer with large diameters has been facing scaling problems. However, the growth mechanism of 2D materials also have some issues to be resolved. The current technique of the growth temperature of highly ordered graphene demonstrated is close to 900°C on Ge, which is higher than most of the III-V materials and close to the dopant diffusion temperature of the Si and Ge based semiconductors. The techniques of growing wafer scale graphene on Si has also not yet been mature. Other than graphene, many other 2D materials have been exploited and the growth mechanism can be much lower on different substrates. It is expected that feasibility of 2D materials enhanced BCP assembly will be demonstrated on other 2D materials like BN, MoS_2, phosphorene, etc. in the short future. And with the reported high quality Si-Graphene Schottky diodes, the application of the hybrid of complicated graphene-semiconductors in complicated sub-10nm nanoscale features would be expected to bloom all kinds of fields including photonic electronics, and medical equipment soon.

We also cover the successful incorporation of transparent high power and AlGaN/GaN HEMTs into flexible electronics in Chapter 3. The capability of printing well-fabricated AlGaN/GaN HEMTs to arbitrary substrate without sacrificing the performance could be used as the foundation to build flexible electronics without losing performance compared to their rigid counterpart. It can be imagined that in a short time, flexible power amplifiers will be presented and driven by the flexible higher power elements. Once equipped with the capability of a power amplifier, the application of flexible electronic devices could quickly migrate from simple functions and passive elements to complicated multi-function electronics system.

Furthermore, with the assistance of the disposable and renewable green electronics mention in Chapter 4, complicated and disposable flexible electronics could be massively fabricated with a cheap and renewable fabrication process. The next generation complicate flexible electronics can infiltrate our lives like disposable contact lenses. Bulky and heavy personal electronics will be replaced with elegant, cheap, and disposable electronics.