

Development of an Asymmetric Two-Phase Variable-Speed Electric Drive for  
Permanent-Split Capacitor Motors in HVAC Applications

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TABLE OF CONTENTS

|                                                                          |           |
|--------------------------------------------------------------------------|-----------|
|                                                                          | Page      |
| LIST OF TABLES . . . . .                                                 | vii       |
| LIST OF FIGURES . . . . .                                                | ix        |
| NOMENCLATURE . . . . .                                                   | xvi       |
| ABSTRACT . . . . .                                                       | xxii■     |
| <b>1 Introduction . . . . .</b>                                          | <b>1</b>  |
| 1.1 Research Motivation . . . . .                                        | 4         |
| 1.2 Research Objectives . . . . .                                        | 10        |
| 1.3 Outline of this Dissertation . . . . .                               | 11        |
| <b>2 Review of the State of the Art PSC Motors and Control . . . . .</b> | <b>12</b> |
| 2.1 PSC Motor Modeling . . . . .                                         | 12        |
| 2.2 Multispeed Operation . . . . .                                       | 14        |
| 2.3 Efficiency Improvement . . . . .                                     | 15        |
| 2.4 Winding Stress . . . . .                                             | 17        |
| 2.5 Balanced Capacitance . . . . .                                       | 18        |
| 2.6 Inverter Topologies . . . . .                                        | 20        |
| 2.6.1 Topology Comparison Metrics . . . . .                              | 21        |
| 2.6.2 AC TRIAC Variable-Voltage Controller (CHP-TRIAC) . . . . .         | 22        |
| 2.6.3 AC PWM Variable-Voltage Controller (CHP-PWM) . . . . .             | 22        |
| 2.6.4 Two-Leg Inverters (1X-2LEG and 2X-2LEG) . . . . .                  | 23        |

|                                                                                                              | Page      |
|--------------------------------------------------------------------------------------------------------------|-----------|
| 2.6.5 Three-Leg Inverters (1X-3LEG and 2X-3LEG) . . . . .                                                    | 26        |
| 2.7 Comparison of Existing Topologies . . . . .                                                              | 28        |
| 2.8 Selection of a Topology for Improvement . . . . .                                                        | 29        |
| <b>3 Proposed Inverter Topology for PSC Motors . . . . .</b>                                                 | <b>31</b> |
| 3.1 Summary of PSC Motor Parameter Trends . . . . .                                                          | 31        |
| 3.2 Proposed Inverter Topology . . . . .                                                                     | 32        |
| 3.3 Topology Model . . . . .                                                                                 | 34        |
| 3.4 Limits of Capacitor Voltage Regulation . . . . .                                                         | 41        |
| 3.5 Motor Efficiency and V/I Trajectories . . . . .                                                          | 43        |
| 3.5.1 Motor Model . . . . .                                                                                  | 44        |
| 3.5.2 Line Operated PSC Motors and Circulating Currents Under Variable<br>Frequency Operation . . . . .      | 45        |
| 3.5.3 Loss Distribution and the Effect of Magnetizing Flux . . . . .                                         | 47        |
| 3.5.4 Effect of MMF Ratio on Efficiency . . . . .                                                            | 48        |
| 3.6 Boost Leg Control . . . . .                                                                              | 49        |
| 3.6.1 Boost Duty Cycle Generation and Decoupling $v_{p2}^*$ from Capacitor Volt-<br>age Regulation . . . . . | 50        |
| 3.7 Summary . . . . .                                                                                        | 52        |
| <b>4 Comparative Evaluation . . . . .</b>                                                                    | <b>53</b> |
| 4.1 Topology Comparison and Selection . . . . .                                                              | 53        |
| 4.1.1 VA Rating Definitions . . . . .                                                                        | 54        |
| 4.1.2 Per-Unit System . . . . .                                                                              | 54        |
| 4.1.3 Comparison of Topologies 2X-2LEG with 1X-3LEG . . . . .                                                | 56        |
| 4.1.4 Comparison of Topologies and Remarks . . . . .                                                         | 59        |
| 4.2 Summary . . . . .                                                                                        | 60        |

## Appendix

|                                                                               | Page      |
|-------------------------------------------------------------------------------|-----------|
| <b>5 Modulation Strategy for the Three-Leg Inverter . . . . .</b>             | <b>61</b> |
| 5.1 Buck-Boost Inverter Leg Modulation . . . . .                              | 61        |
| 5.1.1 Boost Modulation Polarity Example . . . . .                             | 61        |
| 5.1.2 Boost Modulation . . . . .                                              | 63        |
| 5.2 Three-Leg Modulation . . . . .                                            | 65        |
| 5.2.1 Trapezoidal Modulation . . . . .                                        | 67        |
| 5.2.2 Harmonic Distortion of Neutral-Voltage Trapezoidal Modulation . . .     | 70        |
| 5.3 Consequences of Modulation Strategy on Capacitor Voltage Regulation . . . | 73        |
| 5.4 Summary . . . . .                                                         | 74        |
| <b>6 Dynamic Modeling and Control for the Three-Leg Inverter . . . . .</b>    | <b>75</b> |
| 6.1 Operating Point Model of the Converter . . . . .                          | 75        |
| 6.1.1 Capacitor Voltage Regulation . . . . .                                  | 80        |
| 6.2 HVAC Dynamics and Motor Control . . . . .                                 | 83        |
| 6.2.1 Proposed Approach to Control Stator Current . . . . .                   | 84        |
| 6.2.2 Optimal Efficiency Control . . . . .                                    | 87        |
| 6.3 Utility Connection and Utility-VFD Dynamics . . . . .                     | 89        |
| 6.4 Summary . . . . .                                                         | 91        |
| <b>7 Simulation of the Proposed PSC Motor Drive . . . . .</b>                 | <b>93</b> |
| 7.1 Simulation Models . . . . .                                               | 93        |
| 7.1.1 dq- and qd- Models . . . . .                                            | 94        |
| 7.1.2 Expression of State-Space Models in Steady State . . . . .              | 95        |
| 7.1.3 Nonlinear Programming and Identification of Key Efficiency Variables    | 96        |
| 7.1.4 Prediction of Efficiency Benefits . . . . .                             | 99        |
| 7.1.5 Power Loss Predictions . . . . .                                        | 100       |
| 7.2 System Simulation . . . . .                                               | 101       |

## Appendix

|                                                                                                      | Page       |
|------------------------------------------------------------------------------------------------------|------------|
| 7.2.1 Efficiency vs. MMF Ratio . . . . .                                                             | 103        |
| 7.2.2 Voltage Generation of the Buck-Boost Inverter Leg . . . . .                                    | 103        |
| 7.3 Response to Change in Frequency . . . . .                                                        | 105        |
| 7.4 Simulation Summary . . . . .                                                                     | 107        |
| <b>8 Experimental Prototype 1.2X-3LEG PSC Motor Drive . . . . .</b>                                  | <b>108</b> |
| 8.1 Line Operation of the PSC Motor . . . . .                                                        | 109        |
| 8.1.1 Efficiency as Capacitance is Varied . . . . .                                                  | 109        |
| 8.1.2 Efficiency as a Function of Input Voltage and Flux Selection . . . . .                         | 110        |
| 8.2 PSC Motor using 1X-3LEG Inverter . . . . .                                                       | 111        |
| 8.3 Efficiency and MMF Ratio . . . . .                                                               | 113        |
| 8.4 Trapezoidal Modulation . . . . .                                                                 | 115        |
| 8.5 Boost Voltage Generation . . . . .                                                               | 116        |
| 8.6 Efficiency Comparison . . . . .                                                                  | 118        |
| 8.7 Response to Change in Frequency . . . . .                                                        | 119        |
| 8.8 Summary . . . . .                                                                                | 120        |
| <b>9 Conclusions and Future Work . . . . .</b>                                                       | <b>122</b> |
| 9.1 Contributions . . . . .                                                                          | 122        |
| 9.1.1 Development of Design and Evaluation Criteria for PSC Motor drive<br>for HVAC System . . . . . | 122        |
| 9.1.2 Development of the 1.2X-3Leg Inverter Topology . . . . .                                       | 123        |
| 9.1.3 Development of a Model for the Proposed Inverter . . . . .                                     | 123        |
| 9.1.4 Comparative Evaluation of the 1.2X-3Leg Inverter Topology . . . . .                            | 123        |
| 9.1.5 Development of Modulation Strategies for the Proposed Inverter . . . . .                       | 124        |
| 9.1.6 Development of Control Approach for the Proposed Inverter . . . . .                            | 124        |
| 9.1.7 Simulation of the Proposed Inverter . . . . .                                                  | 125        |
| 9.1.8 Experimental Prototype Development of the Proposed Inverter . . . . .                          | 125        |

## Appendix

|                                                                           | Page       |
|---------------------------------------------------------------------------|------------|
| 9.2 Future Work . . . . .                                                 | 126        |
| 9.2.1 Asymmetric Current Regulators for use with the Asymmetric PSC Motor | 126        |
| 9.2.2 Development of Rotor Speed Estimation . . . . .                     | 126        |
| 9.2.3 Development of Efficiency Optimizing Search Controller . . . . .    | 127        |
| 9.2.4 Space-Vector Modulation and Optimal Modulation . . . . .            | 127        |
| 9.2.5 A Unified Control Law for Buck-Boost Inverter Leg . . . . .         | 127        |
| 9.2.6 System Implementation Issues . . . . .                              | 128        |
| 9.2.7 Field Commissioning . . . . .                                       | 128        |
| 9.3 Summary . . . . .                                                     | 128        |
| <b>LIST OF REFERENCES . . . . .</b>                                       | <b>130</b> |
| <b>APPENDIX Simulation and Experimental Parameters . . . . .</b>          | <b>134</b> |

## LIST OF TABLES

| Table                                                                                                                                                                                                                                                                                                                                                                                                      | Page |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 1.1 Quantities used in simple payback calculation . . . . .                                                                                                                                                                                                                                                                                                                                                | 6    |
| 1.2 Assumptions for payback sample points in analysis . . . . .                                                                                                                                                                                                                                                                                                                                            | 8    |
| 2.1 Definition of switching vectors for 1X-2LEG and 2X-2LEG topologies . . . . .                                                                                                                                                                                                                                                                                                                           | 24   |
| 2.2 Definition of switching vectors for 1X-3LEG and 2X-3LEG topologies . . . . .                                                                                                                                                                                                                                                                                                                           | 26   |
| 2.3 Comparison of PSC motor drive topologies present in the state of the art. The motor efficiency capability is an absolute efficiency improvement for a 120V, 3/4 hp motor. The voltage stress is a normalized metric compared to the peak voltage applied by the utility line connection. The required capacitance is used to compare the voltage-doubling rectifiers to the normal rectifiers. . . . . | 29   |
| 3.1 Assignment of switch states to switching functions . . . . .                                                                                                                                                                                                                                                                                                                                           | 34   |
| 3.2 Switching states for the switched-capacitor leg . . . . .                                                                                                                                                                                                                                                                                                                                              | 35   |
| 3.3 Summary of switching states when switches are operated in pairs . . . . .                                                                                                                                                                                                                                                                                                                              | 36   |
| 4.1 Per-Unit Scaling of a 1/6 hp PSC Induction Motor . . . . .                                                                                                                                                                                                                                                                                                                                             | 55   |
| 4.2 List of symbols used in efficiency calculation . . . . .                                                                                                                                                                                                                                                                                                                                               | 58   |
| 4.3 VA study comparison of 2X-2LEG and 1X-3LEG topologies . . . . .                                                                                                                                                                                                                                                                                                                                        | 59   |
| 5.1 Summary of simulation parameters . . . . .                                                                                                                                                                                                                                                                                                                                                             | 71   |
| 6.1 Limits on winding and pole voltage commands . . . . .                                                                                                                                                                                                                                                                                                                                                  | 86   |

| Table                                          | Page |
|------------------------------------------------|------|
| A.1 Simulated motor parameters . . . . .       | 135  |
| A.2 Simulation inverter parameters . . . . .   | 136  |
| A.3 Experimental motor parameters . . . . .    | 136  |
| A.4 Experimental inverter parameters . . . . . | 137  |

## LIST OF FIGURES

| Figure                                                                                                                                                                                                                                                                                                                                                                      | Page |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 1.1 Schematic illustration of the basic HVAC cycle and usage of PSC motors. In residential HVAC systems, the condenser usually rejects heat to the air. In commercial HVAC systems, the condenser can reject heat to the air or to a water connection. In either case, the condenser may or may not be located in close proximity to the compressor and controller. . . . . | 3    |
| 1.2 Graphical illustration of market penetration as a function of payback [1] for LED lighting . . . . .                                                                                                                                                                                                                                                                    | 5    |
| 1.3 Application of the variable speed drive into the existing HVAC application: a) the existing PSC motor application, b) the upgraded application with the power converter installed, and c) the alternative upgrade approach using a PM motor                                                                                                                             | 7    |
| 1.4 Illustration of example cost structure of an electronic power converter as a function of output power. Numerical thresholds and acceptance criteria would be driven by market studies and material cost. . . . .                                                                                                                                                        | 9    |
| 2.1 Multispeed PSC motor connected to a HVAC controller. The electromechanical switching elements are represented by mechanical switches. . . . .                                                                                                                                                                                                                           | 15   |
| 2.2 Torque-speed curve for a multispeed PSC motor. Tap 1 and Tap 2 correspond to high-speed and medium-speed, respectively. . . . .                                                                                                                                                                                                                                         | 15   |
| 2.3 Speed-torque curves for multi-speed PSC motor operating against a fan load . .                                                                                                                                                                                                                                                                                          | 19   |
| 2.4 Efficiency-capacitance curve for multi-speed PSC motor operating against a fan load. Speeds are determined by the developed torque against the fan load curve.                                                                                                                                                                                                          | 19   |
| 2.5 Circuit diagram for CHP-TRIAC topology . . . . .                                                                                                                                                                                                                                                                                                                        | 23   |

| Figure                                                                                                                                                                                                                                                                                            | Page |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 2.6 Circuit diagram for CHP-PWM topology . . . . .                                                                                                                                                                                                                                                | 23   |
| 2.7 Representation 1X-2LEG and 2X-2LEG: a) schematic representation, b) voltage vector capability. $v_{bus} = 1.0$ for 1X-2LEG topology and $v_{bus} = 1.0$ for 2X-2LEG topology. . . . .                                                                                                         | 25   |
| 2.8 Representation 1X-2LEG and 2X-2LEG: a) schematic representation, b) voltage vector capability. $v_{bus} = 1.0$ for 1X-2LEG topology and $v_{bus} = 1.0$ for 2X-2LEG topology. . . . .                                                                                                         | 25   |
| 2.9 Representation of 1X-3LEG and 2X-3LEG topologies: a) an illustration of the circuit topology in [2], b) the voltage vectors available to the three-leg inverter, including two zero vectors. $v_{bus} = 1.0$ for the 1X-3LEG topology, and $v_{bus} = 2.0$ for the 2X-3LEG topology. . . . .  | 27   |
| 2.10 Representation of 1X-3LEG and 2X-3LEG topologies: a) an illustration of the circuit topology in [2], b) the voltage vectors available to the three-leg inverter, including two zero vectors. $v_{bus} = 1.0$ for the 1X-3LEG topology, and $v_{bus} = 2.0$ for the 2X-3LEG topology. . . . . | 28   |
| 3.1 Schematic of 1.2X-3LEG inverter topology connected to a motor. The topology voltage asymmetry and the machine current asymmetry are noted by each transistor pair. . . . .                                                                                                                    | 33   |
| 3.2 Voltage vector illustration of the 1.2X-3LEG topology and the 1X-3LEG topology. The voltage boost realized by $v_c$ (vertical in the phase plane) is indicated. . . . .                                                                                                                       | 36   |
| 3.3 Illustration of the use of voltage modulators in the controlled motor system. This chapter makes use of the RL load. Once the voltage modulator has been validated, future chapters will make use of the complete dynamic motor model. . . . .                                                | 38   |
| 3.4 State-block diagram format of the switched-capacitor topology model . . . . .                                                                                                                                                                                                                 | 39   |
| 3.5 SPICE schematic used to demonstrate the voltage modeling. The output current source steps the current drawn from the pole at half the switching frequency. A bus voltage of 180V and a boost voltage of 20V are used for comparison to experimental validation of the converter. . . . .      | 40   |

## Appendix

## Figure

## Page

|      |                                                                                                                                                                                                                                                                                                                                                                                        |    |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| 3.6  | Comparison of experimental topology pole voltage to SPICE simulated pole voltage and model simulated pole voltage. The experiments were performed at $f_{sw} = 10\text{ kHz}$ , $v_{dc} = 159\text{ V}$ , $v_c = 20\text{ V}$ , $h_{11} = 0.5$ , $h_{13} = 0.25$ , and $h_{13} = 0.75$ . The experiment, simulation, and model were each run with zero output current.                 | 41 |
| 3.7  | Illustration of displacement factor and firing window for regulation of capacitor voltage of the buck-boost inverter leg . . . . .                                                                                                                                                                                                                                                     | 42 |
| 3.8  | Schematic of the line-operated motor. The current in each winding is greater than the input current, which demonstrates the potential for large circulating currents. . . . .                                                                                                                                                                                                          | 46 |
| 3.9  | Estimated motor efficiency as a function of applied stator voltage, based on measured motor power . . . . .                                                                                                                                                                                                                                                                            | 47 |
| 3.10 | Variation of winding voltage and efficiency vs. mmf ratio. The phase angle of the two winding currents is held at $90^\circ$ . Some interesting mmf ratios for this machine include: 1) ratio = 1.0: balanced excitation, 2) ratio = 1.15: optimal efficiency, 3) ratio = 3.0: line-operation mmf ratio (but the currents are not shifted by $90^\circ$ under line operation). . . . . | 49 |
| 3.11 | Block diagram of control of PSC motor with buck-boost inverter leg. The buck-boost inverter leg controller is able to reconstruct $v_p^*$ and simultaneously regulate the capacitor voltage. . . . .                                                                                                                                                                                   | 50 |
| 4.1  | Comparison of topology efficiency, motor efficiency, silicon VA, and passive VA for each of the major PSC inverter topologies . . . . .                                                                                                                                                                                                                                                | 60 |
| 5.1  | Waveforms from simulations illustrating the example of correct and incorrect modulation where $d_{12} = 1 - d_{32}$ ( $v_p$ tracks $d_{11}^*$ and there is no boost function). No dead time is included in this SPICE simulation, so there are some transients in the capacitor current. . . . .                                                                                       | 63 |
| 5.2  | Waveforms from simulations illustrating the modulation of the buck-boost inverter in all buck and boost modes. The capacitor voltage is fixed at $v_c = 0.2\text{ pu}$ for illustration of the switching functions. . . . .                                                                                                                                                            | 64 |

|                                                                                                                                                                                                                                  |      |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| Appendix                                                                                                                                                                                                                         |      |
| Figure                                                                                                                                                                                                                           | Page |
| 5.3 Auxiliary winding voltage waveforms using the buck-boost leg modulation for the inverter . . . . .                                                                                                                           | 65   |
| 5.4 Simplified schematic of proposed inverter illustrated as a 1X-3LEG inverter feeding an R-L load and the voltage capability hexagon illustrating switching states of (S1, S2, S3) . . . . .                                   | 67   |
| 5.5 A typical waveform of neutral voltage duty-cycle ratio command under trapezoidal modulation . . . . .                                                                                                                        | 68   |
| 5.6 Representative waveforms for trapezoidal modulation obtained using simulations                                                                                                                                               | 69   |
| 5.7 Comparison of distortion due to low frequency components in the main and auxiliary winding voltages for trapezoidal modulation . . . . .                                                                                     | 72   |
| 5.8 Comparison of phase angle between main- and auxiliary-winding voltage to firing window for the trapezoidal modulation strategy and a modulation index of 1.0 .                                                               | 74   |
| 6.1 Frequency response functions for $\tilde{v}_c/\tilde{d}_{12}$ and $\tilde{v}_c/\tilde{d}_{32}$ in a) buck mode and b) boost mode . . . . .                                                                                   | 79   |
| 6.2 Frequency response for the transfer function $\tilde{v}_c/\tilde{d}_{12}$ and $\tilde{v}_c/\tilde{d}_{32}$ . The following operating point quantities are chosen: $D_{12} = 0.5$ , $D_{32} = 0.4$ , $I_{p2} = 2.0$ . . . . . | 80   |
| 6.3 Start up voltage waveforms illustrating the operation of the buck-boost inverter exceeding $v_{bus}$ on the auxiliary winding. . . . .                                                                                       | 82   |
| 6.4 Diagram showing the HVAC cycle . . . . .                                                                                                                                                                                     | 84   |
| 6.5 Block diagram for the steady-state current controller . . . . .                                                                                                                                                              | 86   |
| 6.6 Comparison of optimal vs. proposed voltage, mmf ratio, and resulting efficiency                                                                                                                                              | 88   |
| 6.7 Simulation of voltage sag with constant V/Hz controller and sag follower controller                                                                                                                                          | 91   |
| 7.1 Types of simulation used in this research . . . . .                                                                                                                                                                          | 93   |

| Appendix |                                                                                                                                                                                                                                                                                                                                                                                                             | Page |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| Figure   |                                                                                                                                                                                                                                                                                                                                                                                                             |      |
| 7.2      | Voltage capability hexagon for the three-terminal variable-frequency drive a) without boost, b) with boost. The principle voltage vectors in the boost configuration are shown with thick arrows. . . . .                                                                                                                                                                                                   | 98   |
| 7.3      | Comparison of efficiency under trapezoidal modulation of 1X-3LEG topology and 1.2X-3LEG topology . . . . .                                                                                                                                                                                                                                                                                                  | 100  |
| 7.4      | Power loss a) in each stator winding and b) both the windings as a function of mmf ratio . . . . .                                                                                                                                                                                                                                                                                                          | 101  |
| 7.5      | Block diagram of simulated system. The simulated system includes the dc link, voltage generation, boost controller, modulation, and motor. . . . .                                                                                                                                                                                                                                                          | 102  |
| 7.6      | Block diagram of simulated system, as implemented in Simulink. . . . .                                                                                                                                                                                                                                                                                                                                      | 102  |
| 7.7      | Simulation results indicating the optimal mmf ratio and efficiency as a function of frequency . . . . .                                                                                                                                                                                                                                                                                                     | 103  |
| 7.8      | Boost capacitor current command ( $i_{c,pu}^*$ ), boost pole voltage command ( $d_{12}^*$ ), and boost duty cycle command ( $d_{32}^*$ ). Simulation conditions: $v_{bus} = 170\text{ V}$ , $v_c^* = 60\text{ V}$ , $m_i = 0.8$ , $\omega_e^* = 0.95\omega_b$ . . . . .                                                                                                                                     | 104  |
| 7.9      | Regulated boost capacitor voltage $v_c/v_b$ . Simulation conditions are the same as in Figure 7.8. . . . .                                                                                                                                                                                                                                                                                                  | 105  |
| 7.10     | Simulation results from a step reduction in frequency command. a) VI characteristic, b) torque and boost voltage, c) VI characteristic before the step in speed command, d) torque and speed before the step in speed command, e) VI characteristic after the step in speed command, f) torque and speed after the step in speed command. MMF ratio is set to 1.0, and flux level is set to 0.9 pu. . . . . | 106  |
| 8.1      | Block diagram and a photograph of the experimental setup . . . . .                                                                                                                                                                                                                                                                                                                                          | 109  |
| 8.2      | Efficiency of the PSC motor as capacitance is varied under 60 Hz operation . . . . .                                                                                                                                                                                                                                                                                                                        | 110  |
| 8.3      | Efficiency as input voltage is reduced under fixed frequency and fixed capacitance . . . . .                                                                                                                                                                                                                                                                                                                | 111  |

|                                                                                                                                                                                                                                 |      |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| Appendix                                                                                                                                                                                                                        |      |
| Figure                                                                                                                                                                                                                          | Page |
| 8.4 Voltage and current waveforms at an output frequency of 20 Hz. Under constant V/Hz, the output voltage is 0.3. The noise in the waveforms is primarily due to DAC output limits and oscilloscope quantization. . . . .      | 112  |
| 8.5 Voltage and current waveforms at an output frequency of 60 Hz. Under constant V/Hz, the output voltage is 1.0. The aux winding voltage is distorted because of the limited dc-bus voltage. . . . .                          | 113  |
| 8.6 Estimated efficiency as the angle between the main- and auxiliary-winding voltage varies. The measurement reaches a maximum at approximately 47 degrees. . . . .                                                            | 114  |
| 8.7 Efficiency as a function of mmf ratio. Modulation index is set to 0.67 and output frequency is set at 40 Hz to prevent the voltage limit from interacting with the efficiency study. . . . .                                | 114  |
| 8.8 MMF ratio as a function of frequency. The turns ratio is varied for each operating speed and the mmf ratio is recorded. . . . .                                                                                             | 115  |
| 8.9 Pole voltage and output voltage waveforms for 20 Hz output frequency . . . . .                                                                                                                                              | 116  |
| 8.10 Boost capacitor current command ( $i_{c,pu}^*$ ) and boost duty cycle command ( $d_{32}^*$ ). Experimental conditions: $v_c^* = 45V$ , $v_{bus} = 200V$ , $m_i = 0.8$ . This effect can be compared to Figure 7.8. . . . . | 117  |
| 8.11 Boost capacitor voltage during rated conditions at 60 Hz. Experimental conditions: $v_c^* = 45V$ , $v_{bus} = 200V$ , $m_i = 0.8$ . This plot can be compared to Figure 7.9. . . . .                                       | 118  |
| 8.12 Comparison of motor estimated efficiency under line operation, 1X-3LEG inverter operation, and 1.2X-3LEG inverter operation. This plot can be compared to Figure 7.3. . . . .                                              | 119  |

Appendix  
Figure

Page

|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |     |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 8.13 | Experimental auxiliary winding voltages and currents when the frequency command is stepped from $\omega_r = 1.0$ [pu] to $\omega_r = 0.75$ [pu]. In order to do this and not overload the machine, the 1X-3LEG topology was operated with the machine flux level set to 0.7 pu, and the 1.2X-3LEG topology was operated with the machine flux level set to 0.9 pu. The resulting frequency command for the 1X-3LEG topology was $\omega_e = 1.2$ [pu], and for the 1.2X-3LEG topology was $\omega_e =$ [pu]. a) auxiliary winding voltage and current for the 1X-3LEG topology. b) auxiliary winding voltage and current for the 1X-3LEG topology. c) zoomed view of voltage and current waveforms at $t = -0.05$ sec. d) zoomed view of voltage and current waveforms at $t = 7.94$ sec. . . . . | 120 |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|

## NOMENCLATURE

|         |                                            |
|---------|--------------------------------------------|
| IGBT    | Insulated Gate, Bipolar Transistor         |
| FET     | Field-Effect Transistor                    |
| $dV/dt$ | Change in voltage per unit of time         |
| PD      | Partial discharge                          |
| PSC     | Permanent Split Capacitor                  |
| HVAC    | Heating, Ventilation, and Air Conditioning |
| rpm     | rotations per minute                       |
| $\eta$  | efficiency                                 |
| IPM     | Integrated Power Module                    |
| P       | Number of motor poles                      |
| payback | Amount of time to recover investment cost  |
| VFD     | Variable Speed Drive                       |
| W       | Watts                                      |
| kW      | Kilowatts                                  |
| kW-h    | Kilowatt hours                             |
| ECM     | Electronically Commutated Motor            |

|               |                                                                   |
|---------------|-------------------------------------------------------------------|
| PM            | Permanent Magnet                                                  |
| Baseline      | Comparison value                                                  |
| AC            | Alternating Current                                               |
| VAC           | Volts AC                                                          |
| RMS           | Root Mean Squared                                                 |
| $r_{1m}$      | Main winding stator resistance                                    |
| $r_{1a}$      | Auxiliary winding stator resistance                               |
| $x_{1m}$      | Main winding stator leakage reactance                             |
| $x_{1a}$      | Auxiliary winding stator leakage reactance                        |
| $x_{mm}$      | Magnetizing reactance, referred to the main winding               |
| $x_{ma}$      | Magnetizing reactance, referred to the auxiliary winding          |
| $r_{2m}, r_2$ | Rotor resistance, referred to the main stator winding             |
| $r_{2a}$      | Rotor resistance, referred to the auxiliary stator winding        |
| $x_{2m}$      | Rotor leakage reactance, referred to the main stator winding      |
| $x_{2a}$      | Rotor leakage reactance, referred to the auxiliary stator winding |
| $N_m$         | Turns in the main winding                                         |
| $N_a$         | Turns in the auxiliary winding                                    |
| $a, N_a/N_m$  | Ratio of $N_a$ to $N_m$                                           |
| $\omega_r$    | Mechanical Rotor speed [rad/sec]                                  |
| $n_r$         | Rotor speed [rpm]                                                 |

|                |                                                                              |
|----------------|------------------------------------------------------------------------------|
| slip           | Normalized difference between $\omega_r$ and excitation frequency [unitless] |
| TRIAC          | Device used as an AC switch                                                  |
| PWM            | Pulse Width Modulation                                                       |
| chopper        | Circuit used to reduce the voltage magnitude                                 |
| CHP-TRIAC      | Chopper circuit built using TRIAC devices                                    |
| CHP-PWM        | Chopper circuit built using PWM                                              |
| 1X-2LEG        | Two-leg inverter topology with nominal bus voltage                           |
| 2X-2LEG        | Two-leg inverter topology with twice nominal bus voltage                     |
| 1X-3LEG        | Three-leg inverter topology with nominal bus voltage                         |
| 2X-3LEG        | Three-leg inverter topology with twice nominal bus voltage                   |
| 1.2X-3LEG      | Three-leg inverter topology with nominal bus voltage and 20                  |
| $v_{bus}$      | Bus voltage                                                                  |
| $v_{dc}$       | dc link voltage                                                              |
| $q_{ij}$       | Transistor $i$ connected to converter pole $j$                               |
| $d_{ij}$       | Duty cycle command for transistor $q_{ij}$                                   |
| $h_{ij}$       | Instantaneous switching function for transistor $q_{ij}$                     |
| $i_m$          | Current drawn by the main winding                                            |
| $i_a$          | Current drawn by the auxiliary winding                                       |
| $i_n, i_{com}$ | Current drawn by the neutral winding                                         |
| $i_p$          | Current supplied by the inverter pole                                        |

|                                  |                                                                            |
|----------------------------------|----------------------------------------------------------------------------|
| $i_{pi}$                         | Current supplied by inverter pole $i$                                      |
| $v_p$                            | Voltage applied across the output pole and the negative side of the dc bus |
| $v_{pi}$                         | Voltage applied across output pole $i$ and the negative side of the dc bus |
| $v_c$                            | Voltage across the boost capacitor for the 1.2X-3LEG inverter topology     |
| SPICE                            | Simulation Program for Integrated Circuit Emphasis                         |
| $\omega$                         | Reference frame frequency                                                  |
| $\omega_e$                       | Excitation frequency                                                       |
| $\sigma L_{sm}, \sigma_m L_{sm}$ | Main-winding stator leakage inductance                                     |
| $\sigma L_{sa}, \sigma_a L_{sa}$ | Auxiliary-winding stator leakage inductance                                |
| MMF Ratio                        | Normalized ratio of main-winding current to auxiliary-winding current      |
| VA                               | Volt Amperes                                                               |
| VA Study                         | Study of VA characteristics                                                |
| pu                               | per unit                                                                   |
| p.u.                             | per unit                                                                   |
| $P_b$                            | Base power                                                                 |
| $V_b$                            | Base voltage                                                               |
| $I_b$                            | Base current                                                               |
| $Z_b$                            | Base impedance                                                             |
| $\omega_b$                       | Base electrical frequency                                                  |
| $\omega_{mb}$                    | Base mechanical frequency                                                  |

|                 |                                                                |
|-----------------|----------------------------------------------------------------|
| $T_b$           | Base mechanical torque                                         |
| $f_{sw}$        | Switching frequency                                            |
| $P_{sw,IGBT}$   | IGBT switching losses                                          |
| $P_{cond,IGBT}$ | IGBT conduction losses                                         |
| $P_{sw,FET}$    | FET switching losses                                           |
| $P_{cond,FET}$  | FET conduction losses                                          |
| $E_{on}$        | Turn on loss                                                   |
| $E_{off}$       | Turn off loss                                                  |
| $v_{on}$        | On-state voltage drop                                          |
| $i_{p,rms}$     | RMS pole current                                               |
| $r_{ds,on}$     | on-state resistance                                            |
| SCR             | Silicon-controlled rectifier                                   |
| Phase plane     | Plane in which two variables are plotted                       |
| Quadrant I      | Quadrant I of the phase plane, $0 \leq \theta \leq \pi/2$      |
| Quadrant II     | Quadrant II of the phase plane, $\pi/2 \leq \theta \leq \pi$   |
| Quadrant III    | Quadrant III of the phase plane, $\pi \leq \theta \leq 3\pi/2$ |
| Quadrant IV     | Quadrant IV of the phase plane, $3\pi/2 \leq \theta \leq 2\pi$ |
| SVM             | Space Vector Modulation                                        |
| mmf             | Magneto-motive force                                           |
| V/Hz            | Ratio of voltage to frequency, used to indicate flux level     |

$f_{dq}$  Vector quantity, where  $f_{dq} = f_d + j \cdot f_q$

$f_{qd}$  Vector quantity, where  $f_{qd} = f_q - j \cdot f_d$

PCC Point of common coupling

## ABSTRACT

Permanent-split-capacitor (PSC) motors are very widely used in fixed-speed and multi-speed configurations, notably HVAC applications. Typical operation using a fixed-frequency supply results in poor motor efficiency and in large torque ripple at twice the electrical frequency. The feasibility of a variable-speed drive to provide stable variable-speed operation, improve steady-state and dynamic torque characteristics, and improve efficiency has commercial interest. Application of existing symmetric variable-speed drive designs to asymmetric PSC motors results in either excessive voltage stress applied to the motor's windings or in insufficient voltage applied to the auxiliary winding resulting in relatively low efficiency and large torque ripple at the motor's design point.

This research identifies key PSC motor characteristics and develops a variable-speed drive to improve operation. The developed variable-speed drive simultaneously reduces the dc bus voltage and increases motor efficiency at rated speed. The  $dV/dt$  applied across the motor windings is kept low, and an appropriate magneto-motive force is applied to the motor at all operating points. As a result, the motor and drive system efficiency is increased while preserving reliable motor operation.

The dissertation document presents the proposed topology, detailed modeling, comparative evaluation, simulation results, backed up by experimental evaluation that validate the feasibility of the approach.

# Chapter 1

## Introduction

Motors used for Heating, Ventilation and Air Conditioning (HVAC) systems represent an important opportunity for improvements in energy efficiency. A schematic of a typical residential HVAC system is illustrated in Figure 1.1, which most often employ single phase induction motors. Single phase induction motors of the Permanent-Split-Capacitor (PSC) type are among the most common. Since the application of PSC motors results in motors that cannot start into a high-torque load, they are applied to loads that require almost zero starting torque. In HVAC applications this is generally found in fan and pump loads. PSC motors are thus most often used in compressor lubrication oil pumps, compressor coolant water pumps, and condenser fans. They may also be applied to an evaporator fan (often this is the blower motor in residential units), but the power level for these motors is usually low. The condenser fans are located in physical proximity to the heat exchanger. In large installations this location is physically distant from the HVAC unit controller and compressor, while the compressor's controller, coolant system, and lubrication system are usually located in close proximity. Due to pump and fan design, it is often desirable to operate pump motors at high speed (3600 rpm), and fan motors at medium to low speed (800 rpm). As a result, the efficiency for condenser fans can suffer greatly as multispeed motors are operated at reduced speed through voltage control. A fan motor that was designed to run at 65% efficiency may operate near 40% during normal operation, and thus represents a significant opportunity for system efficiency improvements.

Permanent-Split-Capacitor (PSC) motors have a long history, almost dating back to the invention of the three-phase induction motor. PSC motors have been applied to systems since the 1930's, when capacitors transitioned from the glass condenser to the paper-and-oil capacitor. This change increased capacitance values, and increased the mechanical robustness, which allowed the capacitor to be physically mounted to the motor which may be in a vibrating environment. From the early 1920's to the mid 1940's and later, design objectives were incrementally developed to meet specific machine cost, breakdown torque, inrush current, and starting characteristics, often at the expense of reduced efficiency[3].

Today, PSC motors are often constructed with small-gauge wire, inexpensive steel, and consequently have relatively high winding resistance and high core loss. The resulting poor efficiency is complicated by the cost constraints placed on the selected value of PSC capacitance and the HVAC application usage [4]. By installing insufficient capacitance to balance the PSC machine, the motor is able to start in a known direction, but operating efficiency is reduced. In practice, the value of capacitance is often selected to be just high enough to reliably start the motor in the positive direction, and the HVAC application usage historically prefers to reduce the speed from the design point through some form of voltage control. The design efficiency of these machines seldom exceeds 60%, and the HVAC application efficiency usually is between 12%-40% [5].

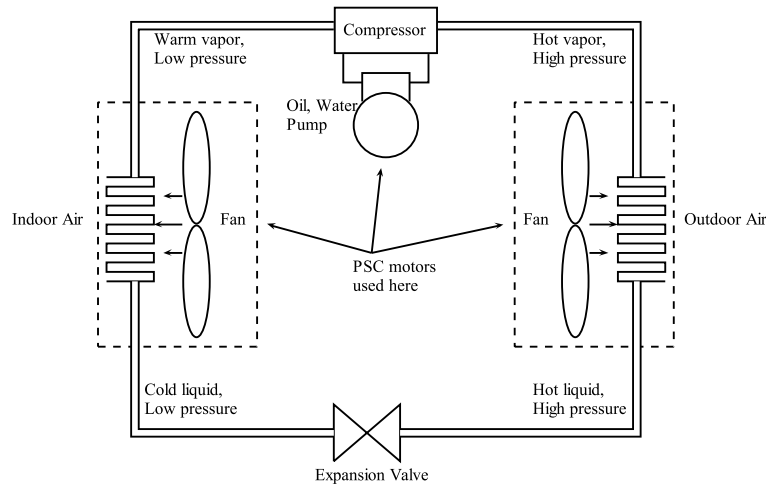


Figure 1.1 Schematic illustration of the basic HVAC cycle and usage of PSC motors. In residential HVAC systems, the condenser usually rejects heat to the air. In commercial HVAC systems, the condenser can reject heat to the air or to a water connection. In either case, the condenser may or may not be located in close proximity to the compressor and controller.

Furthermore, PSC motors comprise a significant portion of total motor production and application. Their large install base combined with their relatively poor efficiency results in a significant amount of wasted energy. It is estimated that fractional horsepower motor sales exceed \$10B annually [6]. Even if one assumes that the fractional horsepower PSC motors comprise \$1B of this market, that they average \$50 per motor, that they average 30% efficiency, PSC motor losses represent a power consumption of over 1 GW in wasted heat. By implementing a motor controller and power converter, there is an opportunity to greatly reduce this wasted energy. Even if only a small percentage of this can be avoided, a significant amount of energy can be saved by using a power converter to control the PSC motors in HVAC applications. This benefits electricity consumers as well as reduces carbon emissions. This thesis further develops a definitive and viable approach to realizing this benefit.

## 1.1 Research Motivation

In developing efficiency improvements for PSC motors, the trend in the literature (for example [7]), is that fully controllable semiconductor devices are too costly to justify their application to realizing variable speed drives for PSC motors in HVAC applications. However, the market price of fully controllable power semiconductor switches continues to decrease. Multiple semiconductor manufacturers produce low-cost, integrated power modules that may be used to operate a PSC motor. For example, in 2012, International Rectifier introduced a surface-mount IPM module that, properly applied, can be used with only copper pads for a heatsink, resulting in a low cost inverter for low power motors [8]. The application of power electronics to appliances and renewable energy sources continues to decrease the price of low-power semiconductor devices. In 2012, the pricing of power electronic devices is low enough that it does not dominate the cost of the power converter.

In order to objectively determine the feasibility of the application of power electronics to PSC motors in HVAC applications, market studies in devices for efficiency improvements in similar applications may be reviewed, for instance high efficiency lighting. Kisch presents in [1] the characteristics of the lighting market that help explain the 2002 market failure of introduction of Light Emitting Diode (LED) based illumination. The resulting market penetration curves shown in Figure 1.2 present acceptable criteria for lighting applications in terms of payback period. Although numerical values may differ between markets, the trend in this study and the trend in HVAC markets may be assumed to be similar, and this may be used as a comparison metric for analysis of feasibility of power electronic application to PSC motors in HVAC applications.

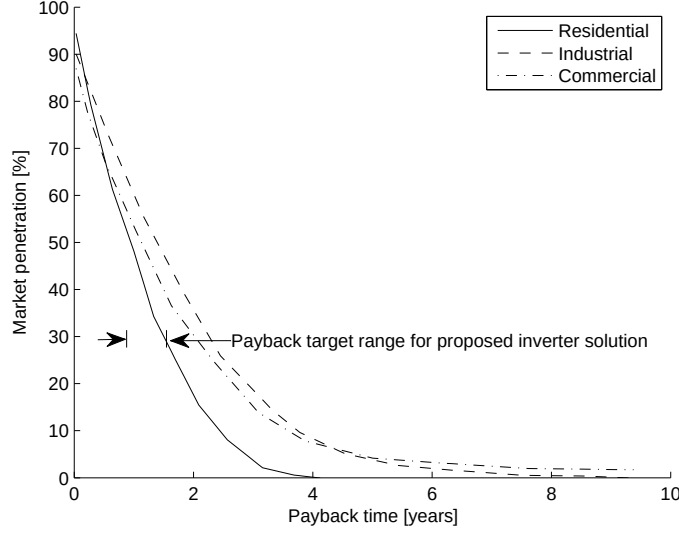


Figure 1.2 Graphical illustration of market penetration as a function of payback [1] for LED lighting

The simple payback time analysis is used in conjunction with Figure 1.2 to determine the feasibility of a given power electronic topology for realizing a variable speed drive for HVAC applications. In order to set a market penetration of 30%-50%, a maximum payback time of 2 years may be set. In order to estimate the payback time of a power converter for comparison to the curve in Figure 1.2, the payback period, in months, can be calculated as done in (1.1). In this calculation,  $\eta_{vfd}$  is the converter/motor system efficiency under variable frequency operation,  $\eta_{line}$  is the motor efficiency under line operation, including the capacitor on the auxiliary winding,  $P_{out}$  is the output power of the motor connected to its load, converter price is the end-consumer price of the power converter under development, electricity price is the market price of electricity, in \$/kWh, duty cycle is the duty cycle of the load, where 1.0 is running 100% of the time, and  $t_{payback}$  is the payback period, in months, resulting from the calculation.

$$P_{out,line} = \eta_{line} P_{in,line}$$

$$\begin{aligned}
P_{out,vfd} &= \eta_{vf} P_{in,vfd} \\
P_{savings} &= P_{in,line} - P_{in,vf} \\
&= P_{out} \left( \frac{1}{\eta_{line}} - \frac{1}{\eta_{vfd}} \right) \\
t_{payback} &= \frac{\text{converter price}}{\text{electricity price} \cdot \text{duty cycle} \cdot P_{out} \left( \frac{1}{\eta_{line}} - \frac{1}{\eta_{vfd}} \right)} 24 \frac{365}{12} \frac{1}{1000} \\
&= \frac{\text{converter price}}{\text{electricity price} \cdot \text{duty cycle} \cdot P_{out} \left( \frac{1}{\eta_{line}} - \frac{1}{\eta_{vfd}} \right)} \frac{1}{24} \frac{12}{365} 1000 \quad [1.1]
\end{aligned}$$

Table 1.1 Quantities used in simple payback calculation

| Quantity          | Value       | Description                                            |
|-------------------|-------------|--------------------------------------------------------|
| $P_{in,line}$     | 1400 [W]    | Motor input power, rated for line operation            |
| $P_{out,line}$    | 560 [W]     | Motor output power, rated for line operation           |
| $\eta_{line}$     | 0.4         | Motor efficiency when operated from the utility supply |
| $\eta_{vf}$       | 0.6         | Efficiency of motor and power converter                |
| electricity price | 0.12 \$/kWh | Average market price of electricity                    |
| converter price   | \$100       | Target market price of power converter                 |
| duty cycle        | 0.5         | Application duty cycle of the line-operated PSC motor  |

To illustrate this formula, an example is presented using the numerical values listed in Table 1.1. Assuming a market electricity price of \$0.12/kWh, a 3/4 hp load that runs 50% of the time, a motor efficiency of 40% under line operation, a converter that can provide 60% system efficiency, and a \$100 converter, the resulting payback time is 4.9 months. This calculation demonstrates that the payback calculation places the power converter that costs in the order of about \$100 in a feasible market on the basis of the current electricity price.

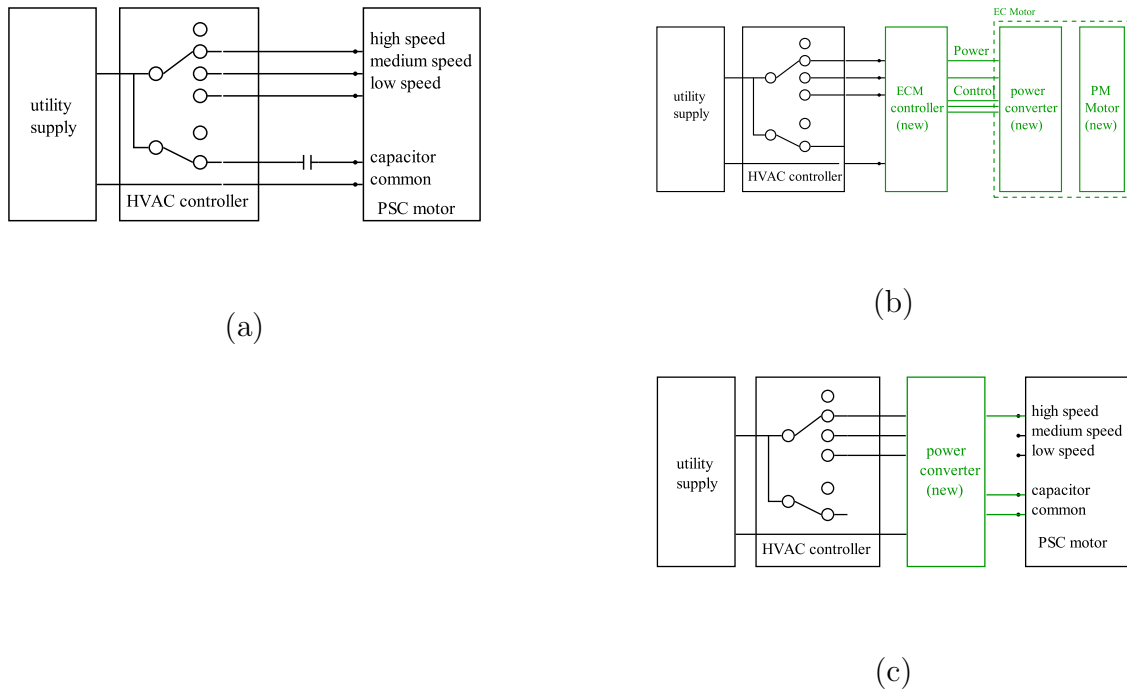


Figure 1.3 Application of the variable speed drive into the existing HVAC application: a) the existing PSC motor application, b) the upgraded application with the power converter installed, and c) the alternative upgrade approach using a PM motor

While the foregoing analysis demonstrates the case for applying a variable speed drive for HVAC applications, this work also focuses on the field upgrade of existing systems as illustrated in Figure 1.3. It may be observed that the HVAC controller in its simplest form uses electromechanical elements to switch between stator windings as the application needs. Since time constants in HVAC systems tend to be on the order of minutes, this primitive form of motor control is sufficiently to meet the application requirements.

In order to implement a variable speed drive for this application, one may generally consider the application of three-phase Permanent Magnet (PM) motors and three-phase induction motors, each associate drive electronics. Figure 1.3b illustrates the HVAC controlled motor that results from a three-phase PM motor approach, often referred to as the Electronically Commuted Motor (ECM). In this case, the old motor is removed from the assembly, a new motor is installed, a power converter is added, and an interface controller is added. On the

other hand, the approach illustrated in Figure 1.3c replaces only the PSC capacitor, and adds a power converter to the system, while retaining the PSC motor as is.

Since the volume of PSC motors in the manufacturing base is extremely high, the price of a PSC motor is considerably lower than the price of an equivalent three-phase motor, regardless of motor type. The PM/ECM motor as a retrofit option would involve the addition of an ECM interface controller, a teardown of the fan assembly, motor replacement, addition of a power converter, and a rebuild of the fan assembly. It is anticipated that, in most circumstances, the targeted variable-speed PSC option would provide 50%-75% of the PM/ECM efficiency improvement. The large variation in this estimate is due to the highly variable efficiency of a PSC motor. For example, the improvement of upgrading a 65% efficient PSC motor to an 80% efficiency ECM motor is not as significant as the improvement of upgrading a 30% efficient PSC motor to an 80% efficient ECM motor. A pay back period analysis on the basis of these assumptions and cost targets are shown in Table 1.2. It may be seen that the PSC retrofit option has a faster payback due to the small addition of new material and the simplicity of the install procedure. Therefore, this research focuses on the field retrofit of PSC motors with power converters to improve the efficiency of the large number of installed fans in the field, as well as near term OEM applications.

Table 1.2 Assumptions for payback sample points in analysis

| Target              | Output Power | Efficiency | Price | Payback |
|---------------------|--------------|------------|-------|---------|
| Line operated motor | 560 W        | 30%        | N/A   | N/A     |
| PSC Inverter Target | 560 W        | 60%        | \$100 | 2 years |
| ECM Retrofit        | 560 W        | 80%        | \$300 | 6 years |

In order to observe the sensitivity with respect to machine size, a scaling analysis for the payback period is performed in the fractional horsepower range. The payback time is complicated by the fact that inverter construction is quantized. In other words, there exists a

fixed inverter cost even if the output power approaches zero. Each inverter platform supports transistors up to a given size, then a larger inverter platform must be used when the power rating exceeds the capability of the transistors. This results in a pseudo staircase inverter cost function and a corresponding distorted sawtooth payback time as a function of motor power, which limits the lower limit of motor power. This effect is illustrated in Figure 1.4. Figure 1.4a illustrates the staircase cost function, and Figure 1.4b shows the distorted sawtooth payback time vs. motor power and the maximum payback limit on the dotted line. For this particular example, an arbitrarily selected target payback period of 3 years would not be feasible for this application's characteristics for a motor power of less than about 200 W.

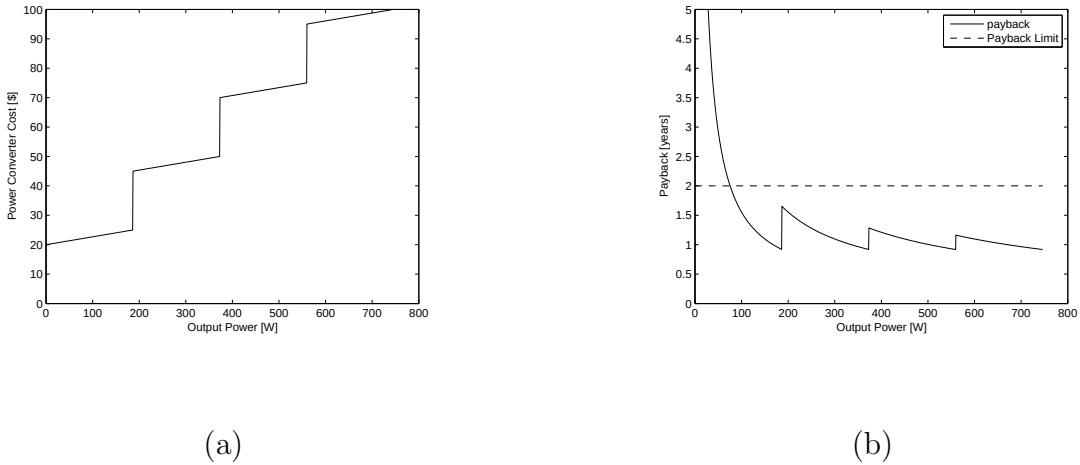


Figure 1.4 Illustration of example cost structure of an electronic power converter as a function of output power. Numerical thresholds and acceptance criteria would be driven by market studies and material cost.

In addition to the cost metric, the voltage stress a power converter places on motor windings can be significant, especially in the retrofit scenario, since the motor may not have necessarily been designed for the added stress. In the research area of partial discharge (PD) and winding stress, one approach that seems consistent with experience is the charge reversal theory [9, 10]. This suggests that for standard wire insulation techniques, the power converter output pulse amplitude must be limited below 400V. This limitation will also place a constraint

on developing suitable power converters with a retrofit view and therefore winding stress is identified as a critical inverter parameter in the forthcoming studies.

## 1.2 Research Objectives

The broad goal of this research is improved efficiency for HVAC systems that employ PSC motors using appropriate power converters. The following specific objectives are identified to realize this goal:

- Analyze various power converter topologies with respect to the PSC motor, and system efficiency
- Identify voltage stress that the various topologies applies to the PSC motor
- Develop of a new power electronic topology that meets the efficiency target and cost target with the voltage stress constraint
- Evaluate of the new power electronic topology against the existing power electronic topologies with respect to different metrics
- Develop a modulation strategy for the new power electronic topology
- Develop a control approach to meet motor and application requirements
- Verify the proposed concepts using computer simulations
- Demonstrate the proposed approach using an experimental prototype

There following chapter develop each of these specific objectives, documenting the study and successful realization of the goal.

### 1.3 Outline of this Dissertation

This dissertation is organized in the following chapters:

Chapter 2 reviews the state of the art research related to variable speed drives applied to PSC motors.

Chapter 3 proposes the new topology presented in this work.

Chapter 4 compares the new proposed topology with the state of the art topologies.

Chapter 6 develops the control strategy used with the developed power-electronic topology.

Chapter 5 develops the modulation required to realize the functional requirements of the power converter to drive the PSC motor.

Chapter 7 develops the simulation models required to analyze the power converter-PSC system and verify the performance of the system.

Chapter 8 demonstrates the experimental verification of the proposed topology using a laboratory scale prototype.

Chapter 9 summarizes the contributions made in this work, and identifies opportunities for future work.

Appendix A includes the key simulation and experimental parameters.

## Chapter 2

### Review of the State of the Art PSC Motors and Control

This chapter will review the development of PSC machine modeling, including approaches for multispeed operation, efficiency improvement, capacitor balance and winding stress trade offs, and will compare and contrast inverter topologies that have been investigated for use with PSC motors. Performance metrics will be established and the inverter topologies will be compared using these metrics. Finally, a comparison of existing topologies will be made on the basis of the performance metrics, and a research opportunity will be identified.

#### 2.1 PSC Motor Modeling

The earliest model still referenced today for PSC motors is based on the dual-revolving field theory [11]. This motor model decomposes the stationary, pulsating fields into two counter-rotating fields, and, using the asymmetric machine impedances, identifies under which conditions torque pulsations will vanish. This technique bears a strong resemblance to the uniform rotating field theory presented in three-phase induction-motor analysis. The dual-revolving field theory is a useful conceptual model as well as a viable initial approach for performing numerical computations.

With the introduction of the digital computer, more detailed machine models have been developed to include dynamic analysis on the basis of complex vectors and applied to the PSC motor as a specific case of an asymmetric two-phase machine. The general two-phase model has been applied to each of the specific capacitor motor configurations in [12]. As computers

facilitated the dynamic simulation of these motors, this problem has been explored in detail in [13] and later works. As the machine characteristics have become better understood, the machine fundamental relationships have been established, torque and efficiency constraints have been used to compute the optimal current vector for a given load output. These constraints have been identified and efficiency expressions have been obtained in [7] for fixed-frequency operation.

As real-time solution of the complex-vector approach became realizable, rotor-flux controllers have been applied to PSC machines. Jacobina et al. documented an approach to implementing such a controller in [14]. This approach can produce attractive dynamics, but has significant disadvantages, including the requirement of position sensing and current regulation into an asymmetric load [15]. Lorenz et al. documented issues that can occur when implementing current regulators in discrete motor controllers [16, 17, 18]. Due to the asymmetry of the machine and the performance limitations of reference frame transformation in discrete controllers used with PSC machines, these issues need to be carefully managed when designing current regulators.

Lesieutre showed in [19] that grid voltage sags can result in the unstable operation of PSC motors connected to air-conditioner loads. In order to accurately simulate this effect, many machines need to be interconnected by a simulated grid model. The complex-vector modeling approach accurately captures the dynamics of the PSC machine, but is computationally expensive and therefore is not well suited for simulating large numbers of machines connected to a power system. Lesieutre presented in [19] a simplified model that captures the primary effects of the PSC machine and is suitable for simulation of a large network of PSC motors connected to air conditioner loads. The resulting predicted response to utility voltage sags and the corresponding analysis suggest that an intelligent motor controller could mitigate the PSC motor stalls that result in grid voltage sags, and thereby prevent grid stability problems.

In summary, several models have been developed for the PSC motor. Today, the motor is well understood and best characterized by the complex space-vector model. This thesis will use the models presented above to propose a power electronic inverter topology suitable to the PSC machine and to propose a control strategy suitable to increasing motor efficiency in HVAC applications.

## 2.2 Multispeed Operation

Multispeed operation of PSC motors have been realized using multiple taps on the main winding that are designed to reduce the effective applied stator voltage. As the tap connection is changed from the high-speed winding to the medium-speed winding, the number of turns in the motor winding is changed so that the voltage across the full winding is reduced. An HVAC controller accomplishes this through the use of an electromechanical contactor, as illustrated in Figure 2.1. The HVAC controller safely switches between stator taps to achieve the desired speed for the application. This is often done by energizing the high-speed winding to get the motor started, and reducing to the medium-speed or low-speed setting after the controller detects it has reached normal operating speed. This allows the controller to reliably establish rotation in the positive direction. The corresponding speed-torque curves are shown in Figure 2.2.

The effect of reducing voltage but keeping the stator frequency constant is to reduce the machine's flux level, to decrease the slope of the speed-torque curve, while increasing machine losses. By doing this, the machine is able to reduce speed against a fan load with an inexpensive speed controller. Utility harmonics are minimized compared to many of the existing solid-state approaches, and a discrete form of speed control is economically realized. Unfortunately, the operating efficiency is significantly reduced.

Speed regulation performance is usually poor in PSC motors. Speed regulation usually refers to changes in speed for a change in load. Fan loads often consist of discrete fan blades, and the load presented to the motor is not uniform. The PSC motor therefore will operate within

a band on the speed-torque curve. When the slope of this curve becomes shallow, as in the case of medium-speed and low-speed settings, significant speed variation can occur, resulting in poor speed regulation. If a specific limit to speed regulation is required, motor designs may be specified to limit this variable.

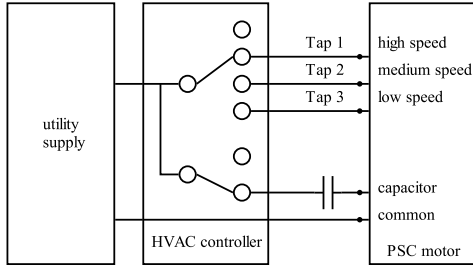


Figure 2.1 Multispeed PSC motor connected to a HVAC controller. The electromechanical switching elements are represented by mechanical switches.

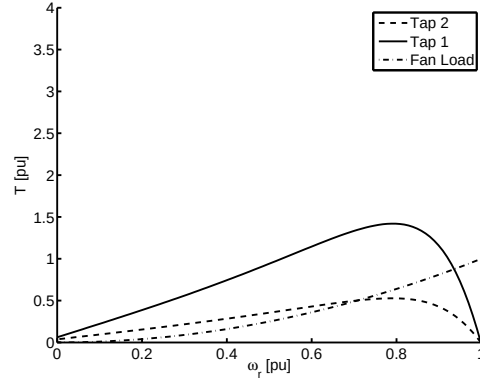


Figure 2.2 Torque-speed curve for a multispeed PSC motor. Tap 1 and Tap 2 correspond to high-speed and medium-speed, respectively.

## 2.3 Efficiency Improvement

The task of designing a set of windings for a PSC motor can be framed as an underdetermined problem. The outputs from the design procedure include  $r_2$ ,  $x_2$ ,  $x_m$ ,  $r_c$ ,  $r_{1m}$ ,  $r_{1a}$ ,  $x_{1m}$ , and  $x_{1a}$ . The inputs to the design procedure include the usual design inputs such as air gap width, slot depth, etc., but also include the choice of auxiliary winding wire size and turns ratio. The result is an infinite number of auxiliary windings that result in satisfactory machine performance. In response to this challenging design task, the usual procedure to designing an auxiliary winding in a PSC machine starts with the design of the main winding to satisfy the machine's breakdown torque requirements and operating performance. When the main winding design is completed, an auxiliary winding is then selected, constrained by slot area, inrush current, starting torque, and capacitor voltage [20, 21]. If the secondary constraints

violate the primary selection criteria, the selection criteria is modified and the process is repeated until all the design criteria are met.

The design process of a PSC motor's auxiliary winding is generally iterative, as described above. For each design, the constraints need to be checked, and the design modified until a satisfactory balance between the design criteria is met. This design process was developed prior to the development of the digital computer, and many design handbooks were created to help manage this process. As the digital computer has progressed, the use of the circle diagram [3] gradually diminished. Due to the age of this design procedure, the uncontrolled efficiency, and the iterative characteristic, it naturally follows that efficiency of these motors is not deterministic. Efficiency at the machine's rating point varies widely in fractional horsepower PSC machines with a mean of 50%, about 30% on the low end, and about 70% on the high end. Many PSC machines include multiple stator taps that effectively reduce the applied stator voltage. The result is that, for a 50% efficient design, the motor runs at 30% efficiency at medium speed and 20% efficiency at low speed. Numerical efficiency varies according to the machine design, and is not always controlled. Fan applications usually operate at lower speed tap settings. As Nailor states in [5], the application efficiency is often about 30% in a typical HVAC application.

Efficiency improvements of a machine with a mean application efficiency of 30% can be significant. For example, a 1-hp motor operating at an efficiency of 30% ( $\eta_{line}$ ) consumes over 2kW of power from the utility compared to the 900W that a similarly sized three-phase motor may consume (this assumes an efficiency of about 85%). If the efficiency is improved from 30% ( $\eta_{line}$ ) to only 40% ( $\eta_{vf}$ ), 335W of utility power is saved, which represents 45% of the machine's output power. However, it is often straightforward to improve the efficiency from 30% ( $\eta_{line}$ ) to 60% ( $\eta_{vf}$ ) at the medium speed setting, since the power converter can control the voltage applied to the high-speed winding to efficiently reduce the motor speed. In this case, approximately 1200W of utility power is saved. From a simple energy consumption perspective, it does not take a dramatic efficiency improvement to satisfy the the feasible payback constraint outlined in chapter 1. For example, given the efficiency improvement

from 30% ( $\eta_{line}$ ) to 40% ( $\eta_{vf}$ ) for a load of 1 hp and a duty cycle of 50%, the payback from (1.1) is 1.8 months. If the efficiency is improved from 30% ( $\eta_{line}$ ) to 60% ( $\eta_{vf}$ ), the payback is less than one month. On the other hand, the duty cycle of 3% would extend the payback period to 15 months. In addition, regulation and incentives can provide further motivation for consumers.

This section has reviewed why PSC motors tend to be inefficient. Based on first principles, there does not appear to be any fundamental reason why PSC motors cannot be built to run as efficiently as three-phase induction motors of equivalent size. The legacy of PSC motor development has led to a situation where inexpensive materials are used, small gauge wire is used to increase the turns ratio in the auxiliary winding, and to support the capacitor voltage boost effect. As a result, efficiency has not been particularly well controlled, and all these effects have combined today so that there are many millions of these inefficient motors installed.

## 2.4 Winding Stress

While variable-speed drives can improve part-load efficiency, they can also introduce winding voltage stress[10, 22] that should be managed in order to result in a reliable system that saves energy. Due to the limitations in inverter topologies, it is common in the literature [23] to set the bus voltage twice as high as the main winding requires. While this may not be an issue for 120 VAC machines, it can create a risk to partial discharge in 240 VAC and 277 VAC machines.

The charge reversal theory suggests that winding stress applied by inverters to motor windings is dominated by instantaneously reversing the polarity of the charges in the wire, in contrast to a slowly-varying electric field. Assuming this is the case, and that an inverter with a bus voltage that is rectified from the utility input, the motor insulation system needs to be able to withstand at least twice the inverter bus voltage in order to operate reliably. If a 120 VAC machine is excited with a standard rectifier-dc link-inverter arrangement, the

bus voltage is approximately 160 VDC. If a 240 VAC machine is excited with a standard rectifier-dc link-inverter arrangement, the bus voltage is approximately 320 VDC. If a 277 VAC machine is excited with a standard rectifier-dc link-inverter arrangement, the bus voltage is approximately 380 VDC. On the other hand, voltage doubling rectifiers result in bus voltages of 320 VDC, 640 VDC, and 780 VDC, respectively. In low-voltage motors, standard motor winding insulation results in a fixed voltage capability, regardless of voltage rating. Assuming a standard motor insulation process, it can be seen that a bus voltage of 320 VDC should be much less likely to exceed the winding's capability than a bus voltage of 640 VDC. Therefore, in order to operate 240 VAC and 277 VAC rated motors reliably, it is desirable to limit the bus voltage to less than 400 VDC.

## 2.5 Balanced Capacitance

The concept of balancing the capacitor motor for running operation is well established [24, 25]. However, component cost has led modern practice to limit the capacitor value to provide only the capacitive reactance necessary to establish enough average torque to start the motor in the forward direction. This results in significant torque vibration and poor efficiency at the designed operating point. To address the efficiency limitation, Huang proposed in [4] to perform field upgrades of the installed capacitance in order to improve the motor running efficiency. Simulation and experiment show that this results in an increase in efficiency at the rating point of the machine, but does not appear to have been adopted by the vendors, perhaps due to the difficulty in realizing solutions suitable for multispeed machines.

In the multispeed application, the torque-speed curve for a 3/4 hp PSC motor running against a fan load is illustrated in Figure 2.3. As seen in the figure, the machine operates most efficiently on the high speed setting, and its efficiency drops rapidly as it is operated on the medium-speed and low-speed settings. In fan and pump applications, the amount of capacitance that results in optimal efficiency is different for each fan speed setting in a multi-speed motor, as illustrated in Figure 2.4. In this figure, the rotor speed,  $\omega_r$  is expressed

in per unit, and is a result of the selected speed tap. At the high-speed setting, 10% slip is typical in PSC motors, and the rotor speed is therefore shown as 90%. For the medium-speed setting, 30% slip is common, and rotor speed is therefore shown as 70%. For a fixed value of capacitance, one of the motor speed settings will result in greatest efficiency, and the other motor speeds' efficiencies drop significantly. This fixed amount of capacitance is shown by the solid vertical black line in Figure 2.4. In order to optimize the capacitance for efficiency at all speed settings in a multispeed installation, a converter would be needed to reduce the effective capacitance, like the configuration presented in [26]. Otherwise, the efficiency is evident by locating the intersection between the solid black line (representing the fixed capacitance) and the efficiency curves (representing the operation of the motor for a given winding tap selection). In addition, the amount of capacitance that would need to be installed to accomplish the maximum efficiency for a selected tap setting is significantly greater than what is typically installed in a PSC application. For example, for a 3/4 hp motor, it is common to install 10  $\mu\text{F}$  of capacitance, which is significantly less than the optimum capacitance of 50  $\mu\text{F}$  visible in Figure 2.4.

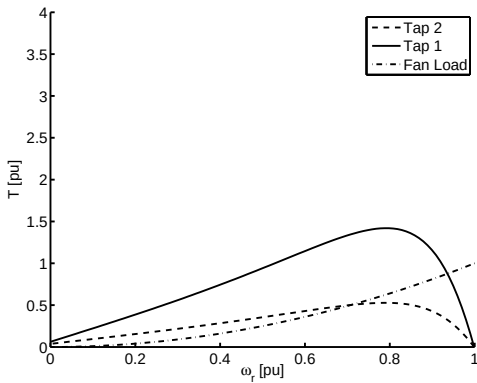


Figure 2.3 Speed-torque curves for multi-speed PSC motor operating against a fan load

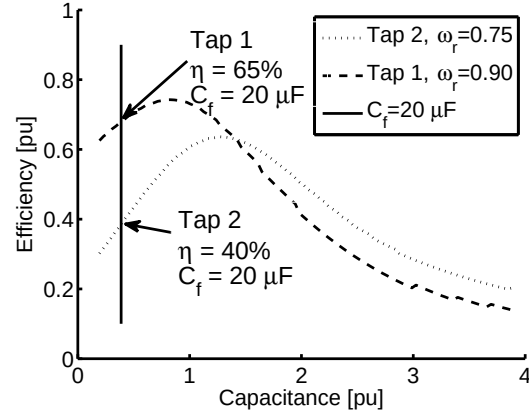


Figure 2.4 Efficiency-capacitance curve for multi-speed PSC motor operating against a fan load. Speeds are determined by the developed torque against the fan load curve.

## 2.6 Inverter Topologies

It is well known that significant energy usage can be saved in operating an induction machine by operating it with a variable-frequency supply [27, 28, 29, 30, 31, 26, 32]. While the energy savings in a three-phase machine system can be worse from a variable-frequency supply at rated speed, the motor efficiency can be improved under variable speed at rated speed for single-phase machines [4, 7].

On average, operating efficiency of PSC motors at their rated power output is about 50%, and rated slip is about 10% [33]. This poor operating efficiency is partly due large resistive losses due to the small wire used in small machines, and partly due to the poor mmf balance achieved by the capacitor across the operating space. Because of the poor mmf balance under line operation, it is straightforward for a two-phase supply to significantly improve the motor operating efficiency at rated speed, as well as reduced speeds. The criteria for maximizing efficiency is established in [7]. Mademlis et al. state that the maximum efficiency operating point and the minimum pulsating torque operating point do not coincide, but under most practical conditions they are close to each other [7].

While some of the literature implies that a PSC motor application cannot support the cost of many semiconductor switches, commercial PSC drives often consist of a TRIAC dimmer or a PWM chopper [34]. However, as introduced in chapter 1, market studies can be used to identify how energy-saving technology can be related to the consumer's payback time [1]. In conjunction with this result, using HVAC usage information, electricity prices, and the price of a small inverter, one can easily calculate the market feasibility of a small inverter to save otherwise wasted energy in a PSC motor. This section introduces power converter performance metrics, discusses the topologies discussed in the literature today, and discusses their trade offs.

### 2.6.1 Topology Comparison Metrics

In order to compare power converter topologies, performance metrics need to be established. This subsection defines the comparison metrics used to evaluate the topologies present in the state of the art.

#### 2.6.1.1 Motor Efficiency Improvement Capability

The motor efficiency improvement capability is an indication of absolute percentage increase in motor efficiency. For example, if a power converter is able to improve the motor efficiency from 65% to 75%, the motor efficiency improvement capability is 10%.

#### 2.6.1.2 Voltage Stress

The voltage stress metric captures the risk of damaging the motor insulation. Some topologies have no zero-state vectors, and are required to double pulse the motor in order to operate, some topologies require high values of dc bus voltage to operate the motor, and some topologies do both. This metric is the numerical ratio of the pulsed voltage amplitude to the peak magnitude of the voltage nominally applied across the main winding. For example, for a PSC motor rated for operation on a 240 VAC utility connection, a voltage stress rating of 1.0 means an inverter will apply a pulse of 0V to  $240\sqrt{2} = 340\text{V}$  across the motor winding. This metric neglects the overshoot due to transmission-line effects between the inverter and the motor.

#### 2.6.1.3 Power Converter Required Capacitance

The capacitance, if any, required by a power converter is compared to the direct connection of the utility to a rectifier to a dc link energy storage element. This criteria is intended as an explicit reminder that voltage-doubling rectifiers require the series connection of capacitors, and therefore require twice as much capacitance as do the directly-connected dc link

approaches. Since the passive energy storage elements are one of the most expensive items in this cost-sensitive application, this is a significant disadvantage.

### **2.6.2 AC TRIAC Variable-Voltage Controller (CHP-TRIAC)**

The AC TRIAC variable-voltage controller (CHP-TRIAC) is an ac switch connected in series with the utility and the PSC motor, as shown in Figure 2.5. The TRIAC is used to reduce the rms quantity of the voltage applied to the main terminals. This approach can incrementally improve the PSC motor efficiency with a very small electronics cost, as presented in [7]. The disadvantages to this approach include significant current harmonics, and since tuning must be done off line, implementation details prevent a generic application.

The voltage stress this device applies to the motor is 1.0 or less, since the TRIAC operates to reduce the applied utility voltage.

It is estimated that the efficiency improvement for this approach is less than 5%, and varies across the frequency range of interest.

Since this approach does not fundamentally change the machine's capability, it offers very little variable speed benefit for not very much cost.

### **2.6.3 AC PWM Variable-Voltage Controller (CHP-PWM)**

The AC pulse-width-modulation (PWM) chopper (CHP-PWM) is an ac switch connected in series with the utility and the PSC motor. One implementation is shown in Figure 2.6, though it is common in practice to replace two of the active switches with rectifiers. This PWM converter is used to reduce the rms quantity of the voltage applied to the main terminals and to reduce the current harmonics drawn from the utility, as compared to CHP-TRIAC. Fundamentally, this approach should result in identical motor efficiency and winding stress as CHP-TRIAC, though there are likely second-order differences in efficiency due to high-frequency PWM efficiency effects and to TRIAC motor current harmonics that each cause negative sequence motor torque.

The voltage stress this device applies to the motor is 1.0 or less, since the chopper circuit operates to reduce the applied utility voltage.

It is estimated that the efficiency improvement for this approach is less than 5%, and varies across the frequency range of interest.

Since this approach does not fundamentally change the machine's capability, it offers very little variable speed benefit for not very much cost. The electronics cost is greater than the CHP-TRIAC, and does not require any passives beyond the motor capacitor to operate.

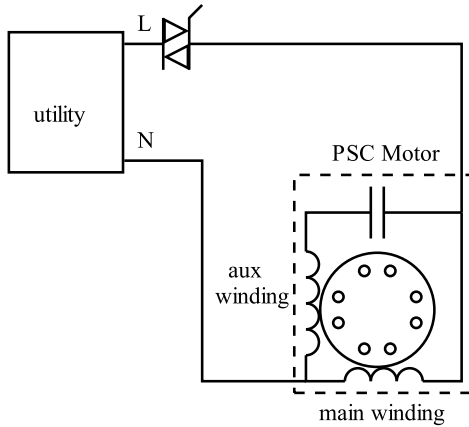


Figure 2.5 Circuit diagram for CHP-TRIAC topology

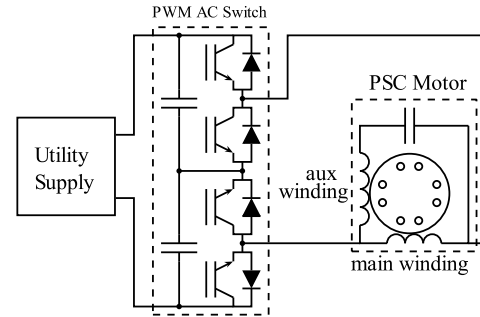


Figure 2.6 Circuit diagram for CHP-PWM topology

#### 2.6.4 Two-Leg Inverters (1X-2LEG and 2X-2LEG)

The two-leg inverters are connected to the PSC machine as shown in Figure 2.8a. The PSC capacitor is removed and the three-terminal inverter outputs are connected to the resulting three motor terminals. There are two variants considered for the two-leg inverters: 1) the bus voltage  $v_{bus}$  is directly rectified from the utility supply and is  $v_{ac,rms}\sqrt{2}$  in magnitude (1X-2LEG), and 2) the bus voltage  $v_{bus}$  is twice the magnitude of the rectified voltage and is  $v_{ac,rms}2\sqrt{2}$  in magnitude (2X-2LEG).

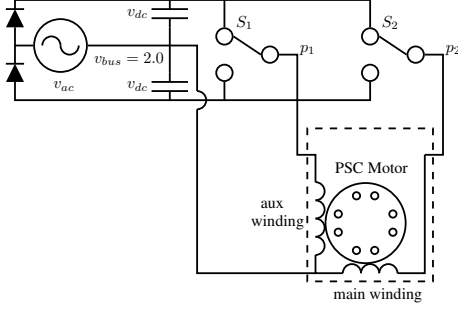
The resulting voltage vectors are tabulated in table 2.1 and are illustrated in Figure 2.8b. In these figures,  $S_1$  is connected to the midpoint of the dc link,  $S_2$  is connected to the auxiliary winding of the PSC machine, and  $S_3$  is connected to the main winding of the PSC machine. Since there are no zero vectors possible with this connection, this topology must double pulse the motor windings in order to implement any type of PWM modulation. In other words, the inverter will switch from  $-\frac{1}{2}v_{bus}$  to  $\frac{1}{2}v_{bus}$  or from  $\frac{1}{2}v_{bus}$  to  $-\frac{1}{2}v_{bus}$  during PWM commutation across both motor windings. As a result, even though the inverter can only apply  $1/2v_{bus}$  across each winding, the voltage stress will be  $v_{bus}$  across each winding. This results in a voltage stress value of 1.0 for 1X-2LEG and 2.0 for 2X-2LEG.

Table 2.1 Definition of switching vectors for 1X-2LEG and 2X-2LEG topologies

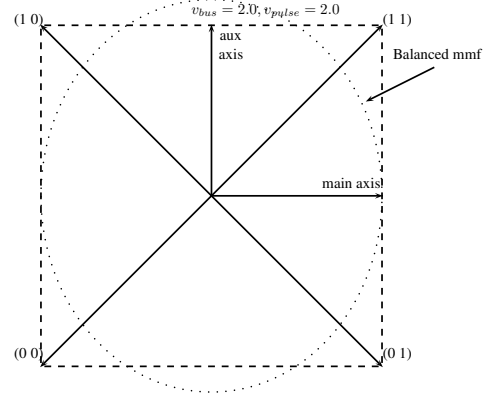
| $S_1$ | $S_2$ | vector | $v_{p1}$              | $v_{p2}$              | $v_{aux}$             | $v_{main}$            |
|-------|-------|--------|-----------------------|-----------------------|-----------------------|-----------------------|
| high  | high  | (1 1)  | $\frac{1}{2}v_{bus}$  | $\frac{1}{2}v_{bus}$  | $\frac{1}{2}v_{bus}$  | $\frac{1}{2}v_{bus}$  |
| high  | low   | (1 0)  | $\frac{1}{2}v_{bus}$  | $-\frac{1}{2}v_{bus}$ | $\frac{1}{2}v_{bus}$  | $-\frac{1}{2}v_{bus}$ |
| low   | high  | (0 1)  | $-\frac{1}{2}v_{bus}$ | $\frac{1}{2}v_{bus}$  | $-\frac{1}{2}v_{bus}$ | $\frac{1}{2}v_{bus}$  |
| low   | low   | (0 0)  | $-\frac{1}{2}v_{bus}$ | $-\frac{1}{2}v_{bus}$ | $-\frac{1}{2}v_{bus}$ | $-\frac{1}{2}v_{bus}$ |

The voltage capability of this topology is compared to the ideal balanced excitation—the voltage ellipse corresponding to a sinusoidal input that could result in balanced mmf—by illustration in Figure 2.1. Even with the bus voltage at twice the line input, this topology is still unable to meet the requirement of balanced excitation. As a result, the efficiency for 1X-2LEG is estimated to be significantly lower than the line operated motor. Steady-state simulation using the method developed in [19] predicts this topology can produce a motor efficiency capability rating of -20%.

The 2X-2LEG topology has more voltage to work with, but still does not quite have enough voltage to reproduce the balanced voltage illustrated in Figure 2.1. Simulation predicts the 2X-2LEG topology can produce a motor efficiency capability rating of +10%.

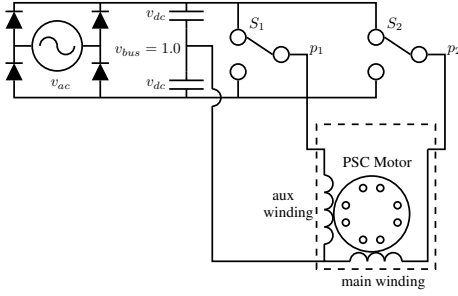


(a)

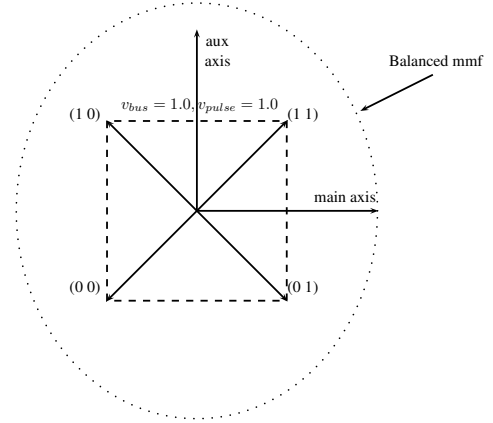


(b)

Figure 2.7 Representation 1X-2LEG and 2X-2LEG: a) schematic representation, b) voltage vector capability.  $v_{bus} = 1.0$  for 1X-2LEG topology and  $v_{bus} = 1.0$  for 2X-2LEG topology.



(a)



(b)

Figure 2.8 Representation 1X-2LEG and 2X-2LEG: a) schematic representation, b) voltage vector capability.  $v_{bus} = 1.0$  for 1X-2LEG topology and  $v_{bus} = 1.0$  for 2X-2LEG topology.

### 2.6.5 Three-Leg Inverters (1X-3LEG and 2X-3LEG)

The three-leg inverters are connected to the PSC machine as shown in Figure 2.9. The PSC capacitor is removed and the three-terminal inverter outputs are connected to the resulting three motor terminals. There are two variants considered for the two-leg inverters: 1) the bus voltage  $v_{bus}$  is directly rectified from the utility supply and is  $v_{ac}\sqrt{2}$  in magnitude (1X-3LEG), and 2) the bus voltage  $v_{bus}$  is twice the magnitude of the rectified voltage and is  $v_{ac}2\sqrt{2}$  in magnitude (2X-2LEG).

The resulting voltage vectors are tabulated in table 2.2 and are illustrated in Figure 2.8. Since there are no zero vectors possible with this connection, this topology must double pulse the motor windings. In other words, the inverter will switch from  $-v_{bus}$  to  $v_{bus}$  instantaneously, and vice versa across both motor windings. As a result, even though the inverter can only apply  $1/2v_{bus}$  across each winding, the voltage stress will be  $v_{bus}$  across each winding. This results in a voltage stress value of 1.0 for 1X-3LEG and 2.0 for 2X-3LEG.

Table 2.2 Definition of switching vectors for 1X-3LEG and 2X-3LEG topologies

| $S_1$ | $S_3$ | $S_3$ | vector  | $v_{p1}$              | $v_{p2}$              | $v_{p3}$              | $v_{aux}$  | $v_{main}$ |
|-------|-------|-------|---------|-----------------------|-----------------------|-----------------------|------------|------------|
| low   | low   | low   | (0 0 0) | $-\frac{1}{2}v_{bus}$ | $-\frac{1}{2}v_{bus}$ | $-\frac{1}{2}v_{bus}$ | 0          | 0          |
| low   | low   | high  | (0 0 1) | $-\frac{1}{2}v_{bus}$ | $-\frac{1}{2}v_{bus}$ | $\frac{1}{2}v_{bus}$  | 0          | $v_{bus}$  |
| low   | high  | high  | (0 1 1) | $-\frac{1}{2}v_{bus}$ | $\frac{1}{2}v_{bus}$  | $\frac{1}{2}v_{bus}$  | $v_{bus}$  | $v_{bus}$  |
| low   | high  | low   | (0 1 0) | $-\frac{1}{2}v_{bus}$ | $\frac{1}{2}v_{bus}$  | $-\frac{1}{2}v_{bus}$ | $v_{bus}$  | 0          |
| high  | high  | low   | (1 1 0) | $\frac{1}{2}v_{bus}$  | $\frac{1}{2}v_{bus}$  | $-\frac{1}{2}v_{bus}$ | 0          | $-v_{bus}$ |
| high  | low   | low   | (1 0 0) | $\frac{1}{2}v_{bus}$  | $-\frac{1}{2}v_{bus}$ | $-\frac{1}{2}v_{bus}$ | $-v_{bus}$ | $-v_{bus}$ |
| high  | low   | high  | (1 0 1) | $\frac{1}{2}v_{bus}$  | $-\frac{1}{2}v_{bus}$ | $\frac{1}{2}v_{bus}$  | $-v_{bus}$ | 0          |
| high  | high  | high  | (1 1 1) | $\frac{1}{2}v_{bus}$  | $\frac{1}{2}v_{bus}$  | $\frac{1}{2}v_{bus}$  | 0          | 0          |

The voltage capability of the 1X-3LEG topology is compared to the ideal balanced voltage excitation—the voltage ellipse corresponding to a sinusoidal input that could result in balanced mmf—by illustration in Figure 2.2. With the bus voltage equal to the rectified line

input value, the 1X-3LEG topology is not able to recreate the balanced voltage ellipse, but it is able to do this with the bus voltage equal to twice the rectified line input value. As a result, the efficiency for 1X-3LEG is estimated to be slightly lower than the line operated motor. Simulation predicts the 1X-3LEG topology can produce a motor efficiency capability rating of -10%.

The 2X-3LEG topology has sufficient voltage to recreate the balanced voltage ellipse. Simulation predicts the 2X-3LEG topology can produce a motor efficiency capability rating of +10%.

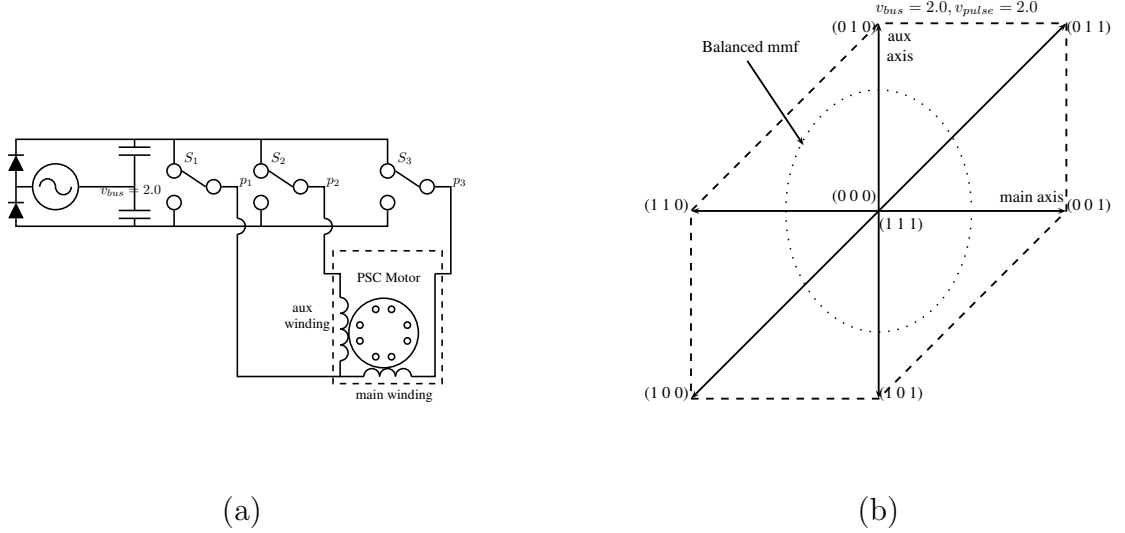


Figure 2.9 Representation of 1X-3LEG and 2X-3LEG topologies: a) an illustration of the circuit topology in [2], b) the voltage vectors available to the three-leg inverter, including two zero vectors.  $v_{bus} = 1.0$  for the 1X-3LEG topology, and  $v_{bus} = 2.0$  for the 2X-3LEG topology.

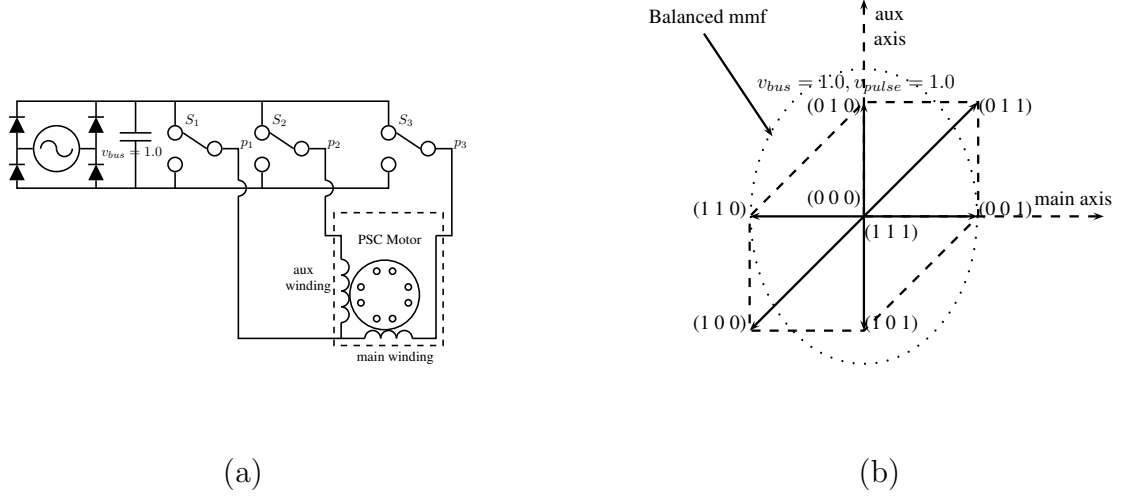


Figure 2.10 Representation of 1X-3LEG and 2X-3LEG topologies: a) an illustration of the circuit topology in [2], b) the voltage vectors available to the three-leg inverter, including two zero vectors.  $v_{bus} = 1.0$  for the 1X-3LEG topology, and  $v_{bus} = 2.0$  for the 2X-3LEG topology.

## 2.7 Comparison of Existing Topologies

The primary metric for topology evaluation is the combined PSC motor and drive operating efficiency. This thesis does not discriminate between front ends, and a fixed efficiency of 96% of the drive will be assumed where appropriate. The motor efficiency improvement depends greatly on the motor's stator resistance, rotor resistance, and core loss characteristics. While this makes a comprehensive analysis infeasible, a sample point can be taken for the sake of analysis. For this analysis, a sample 3/4 hp motor will be used.

The second metric for topology evaluation is the voltage stress each topology impresses on the PSC motor windings. This is important because, since this research focuses on retrofit benefit, the motors may not have the insulation system to withstand excessive voltage stress across the windings.

Since one of the most expensive parts in a power converter is the set of passive components, the third metric for topology comparison is a comparison of the passive elements. At this

Table 2.3 Comparison of PSC motor drive topologies present in the state of the art. The motor efficiency capability is an absolute efficiency improvement for a 120V, 3/4 hp motor.

The voltage stress is a normalized metric compared to the peak voltage applied by the utility line connection. The required capacitance is used to compare the voltage-doubling rectifiers to the normal rectifiers.

| Topology  | Motor Efficiency | Voltage Stress | Required Capacitance |
|-----------|------------------|----------------|----------------------|
| Line      | 40%              | <1.0 p.u.      | 1.56 p.u.            |
| CHP-TRIAC | 43%              | <1.0 p.u.      | 1.56 p.u.            |
| CHP-PWM   | 42%              | <1.0 p.u.      | 1.56 p.u.            |
| 1X-2LEG   | 29%              | 1.0 p.u.       | 1.0 p.u.             |
| 1X-3LEG   | 35%              | 1.0 p.u.       | 1.0 p.u.             |
| 2X-2LEG   | 50%              | 2.0 p.u.       | 2.0 p.u.             |
| 2X-3LEG   | 50%              | 2.0 p.u.       | 2.0 p.u.             |

point in the research, this is simply a statement about the connection of the rectifier to the dc bus, since the voltage doubling rectifiers use a series connection of capacitors to form the neutral point, and this reduces the effective capacitance value of the dc link.

The resulting metric comparison chart of these metrics is shown in Figure 2.3.

The highest performing topologies are those that double the line voltage to meet the desired voltage trajectory. If these candidates are rejected, the next highest performing topology is the 1X-3LEG topology. This research evaluates the 1X-3LEG topology and searches for an improved, asymmetric inverter that is better suited to the asymmetric PSC motor.

## 2.8 Selection of a Topology for Improvement

Of the existing topologies compared in Table 2.3, the 1X-3LEG topology may be identified to be the best overall topology, based on the comparison metrics. Unfortunately, for many PSC motors, it is unable to improve the motor efficiency compared to line operation. However, if by modifying the 1X-3LEG topology the motor efficiency can be significantly improved, the

resulting topology would result in the best topology in all categories. This research therefore focuses on improving the 1X-3LEG topology through a key topological innovation.

## Chapter 3

### Proposed Inverter Topology for PSC Motors

Chapter 1 introduced the potential benefit of operating a PSC motor from a variable-speed power converter, and chapter 2 summarized the power-converter topologies that have been developed to operate PSC motors. This chapter develops a topology that meets the requirements of the asymmetric PSC motor, incorporating a 'boost-capacitor' and a 'buck-boost' inverter leg. An analytical model is developed for the proposed topology and compared to experimental data for model validation. Finally, a control strategy for the buck-boost inverter leg that develops a required output voltage and simultaneously regulates boost capacitor voltage.

#### 3.1 Summary of PSC Motor Parameter Trends

As introduced in chapter 2, PSC motor design methods were developed starting in the 1930's and gradually changed to produce the PSC motor characteristics that are available today. The result is a family of motors with a wide spread in efficiency and satisfactory starting, and running characteristics for applications that do not require a lot of dynamic performance. When these motors are applied to HVAC loads, the efficiencies usually drop significantly, primarily due to the desired speed range. This results in application efficiencies around 30%. Since there are infinitely many main-to-auxiliary winding turns ratios that will satisfy a given design, the turns ratio appears to be bounded only by practical limits in auxiliary winding voltage rating and capacitor voltage rating. Practical voltage ratings of ac capacitors are

340-370 VAC. As a result, turns ratios vary, but are limited to the voltage rating of the capacitor. For 120 VAC machines, the turns ratio is often limited to 1.6, and for 240 VAC machines, the turns ratio is often limited to 1.2.

The insulation system is assumed to be uniform between the main- and auxiliary-winding, and to be the same as conventional three-phase machines. In this case, the insulation system in a 120 VAC machine can withstand twice the normalized voltage stress as that in a 240 VAC machine can. Stated another way, a 120 VAC machine can likely withstand the voltage stress from a voltage-doubling rectifier's inverter, while a 240 VAC machine likely cannot.

### 3.2 Proposed Inverter Topology

Chapter 2 identified and grouped the variable-speed-inverter topologies applied to PSC motors that have been discussed in the literature. The trade offs and compromises hint that a topology that can extend the voltage capability of the 1X-3LEG topology and reduce the voltage stress from the 2X-3LEG topology would result in an inverter topology that can meet the efficiency requirements and preserve the motor life expectancy of the PSC motor in HVAC applications.

The proposed inverter is shown schematically in Figure 3.1, where the PSC motor is indicated by two inductive loads. It exhibits one switched-capacitor inverter leg and two two-level inverter legs. It will be shown that it is capable of developing a 20% voltage boost capability (hence the 1.2X in the name) when connected to the majority of 240 VAC PSC motors.

The design goal for this converter is to achieve a 20% boost in voltage on pole  $p_2$ , while keeping  $v_{dc}$  at the nominal input voltage. If input current shaping is required, a power-factor controller can optionally be installed, but is not necessary for adequate motor performance. For a 240 VAC motor, the required boost from the inverter for the  $p_2$  pole is 65 VAC, and transistors  $q_{32}$  and  $q_{42}$  therefore need to block only 65V. Transistors  $q_{12}$  and  $q_{22}$  need to block  $v_{dc} + v_c$ .

In addition to the voltage asymmetry, the motor exhibits current asymmetry. Assuming balanced excitation ( $a = N_a/N_m$  and  $i_m = ai_a e^{-j\pi/2}$ ), the current returned through the common terminal of the motor carries rms current of magnitude  $i_n = i_m \sqrt{1 + 1/a}$ , as shown in (3.1). The mmf ratio resulting in optimum efficiency will deviate from this, as Mademlis discusses in [7], but this serves as a useful nominal value. As a result, the current rating for transistors  $q_{11}$ , and  $q_{21}$  should be greater than the current rating for the rest of the transistors. For the common turns ratio of  $a = 1.18$  in 240 VAC PSC machines, transistors  $q_{11}$  and  $q_{21}$  should be rated for about 1.35 times the current of the rest of the transistors. Both the voltage blocking asymmetry and the current rating asymmetry are illustrated in Figure 3.1.

$$\begin{aligned}
 i_n &= \sqrt{i_m^2 + i_a^2} \\
 &= \sqrt{i_m^2 + \frac{1}{a} \cdot i_m^2} \\
 &= i_m \sqrt{1 + \frac{1}{a}}
 \end{aligned} \tag{3.1}$$

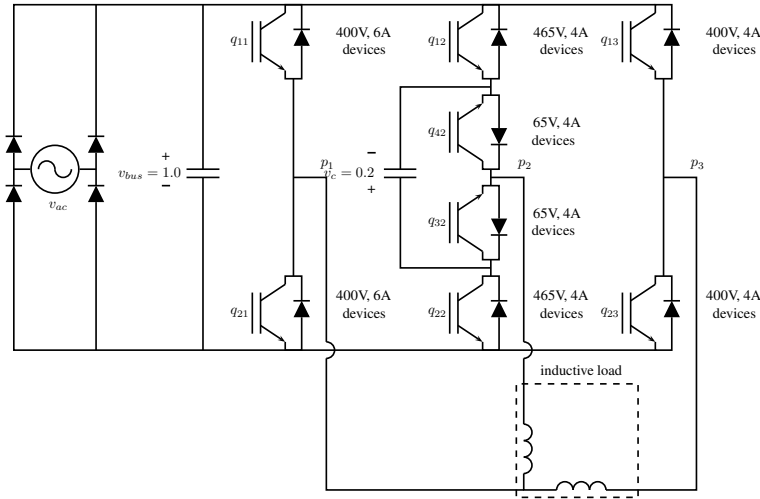


Figure 3.1 Schematic of 1.2X-3LEG inverter topology connected to a motor. The topology voltage asymmetry and the machine current asymmetry are noted by each transistor pair.

Table 3.1 Assignment of switch states to switching functions

| $h_{11}$ | $h_{31}$ | $q_{11}$ | $q_{21}$ | $q_{31}$ | $q_{41}$ | $h_{12}$ | $q_{12}$ | $q_{22}$ | $h_{13}$ | $q_{13}$ | $q_{23}$ |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 0        | 0        | off      | on       | off      | on       | 0        | off      | on       | 0        | off      | on       |
| 0        | 1        | off      | on       | on       | off      | 1        | on       | off      | 1        | on       | off      |
| 1        | 0        | on       | off      | off      | on       |          |          |          |          |          |          |
| 1        | 1        | on       | off      | on       | off      |          |          |          |          |          |          |

As a first step in developing a model for the proposed inverter, the relationship between various switching functions  $h_{ij}$  and the corresponding transistors  $q_{ij}$  are listed in Table 3.1. As indicated in figure 3.1, the quantity  $i$  in  $q_{ij}$  represents the voltage throw to which the transistor connects, and the quantity  $j$  represents the current pole for the appropriate composite switch. For example, the bottom switch in the neutral connection is labeled  $q_{21}$  because it connects throw 2 to pole 1. Since transistors  $q_{11}$  and  $q_{21}$  are operated in complementary mode, the switching function  $h_{11}$  uniquely determines the switching pattern of transistors  $q_{11}$  and  $q_{21}$ . Similarly, the switching functions  $h_{12}$ ,  $h_{32}$ ,  $h_{13}$  and their relationship to transistors  $q_{12}$ ,  $q_{22}$ ,  $q_{32}$ ,  $q_{42}$ ,  $q_{13}$ , and  $q_{23}$  are listed in Table 3.1.

### 3.3 Topology Model

In order to understand the 1.2X-3LEG topology sufficient to develop a control law, a model of the topology must be developed. Since no conventional method exists to analyze this topology from an ideal switch perspective, the circuit is divided into transistors and diodes, and the conduction paths for each active and passive switch are analyzed for each polarity of pole current, rather than attempt the application of averaged models directly to this topology. The bus voltage is assumed to be positive, and the boost capacitance is assumed to have a voltage that is zero or positive.

The comprehensive list of switching states for the switched-capacitor leg are summarized in Table 3.2, including the conduction modes that cause shoot through. This table is generated

by considering the conduction mode of each transistor and diode, and observing the pole voltage applied by the inverter leg for each direction of current flow from the inverter leg pole. The result is 16 conduction modes, 9 of which are non-destructive. As this table shows, there are only four voltages that the topology can apply at the pole, and only two nontrivial currents the topology can conduct into the capacitor. If the switches are operated in complementary mode ( $q_{12}$  and  $q_{22}$  are operated in complementary mode, and  $q_{32}$  and  $q_{42}$  are operated in complementary mode), then the conduction modes reduce from 16 to 4, as listed in Table 3.3.

Table 3.2 Switching states for the switched-capacitor leg

| $q_{12}$ | $q_{22}$ | $q_{42}$ | $q_{32}$ | $v_{p2}, i_{p2} > 0$ | $v_{p2}, i_{p2} \leq 0$ | $i_c, i_{p2} > 0$ | $i_c, i_{p2} \leq 0$ | comment        |
|----------|----------|----------|----------|----------------------|-------------------------|-------------------|----------------------|----------------|
| off      | off      | off      | off      | $-v_c$               | $v_{bus} + v_c$         | $i_{p2}$          | $-i_{p2}$            |                |
| off      | off      | off      | on       | 0                    | $v_{bus} + v_c$         | 0                 | $-i_{p2}$            |                |
| off      | off      | on       | off      | $-v_c$               | $v_{bus}$               | $i_{p2}$          | 0                    |                |
| off      | off      | on       | on       | N/A                  | N/A                     | N/A               | N/A                  | shoot through  |
| off      | on       | off      | off      | $-v_c$               | 0                       | $i_{p2}$          | 0                    |                |
| off      | on       | off      | on       | 0                    | 0                       | 0                 | 0                    |                |
| off      | on       | on       | off      | $-v_c$               | $-v_c$                  | $i_{p2}$          | $i_{p2}$             | charges cap    |
| off      | on       | on       | on       | N/A                  | N/A                     | N/A               | N/A                  | shoot through  |
| on       | off      | off      | off      | $v_{bus}$            | $v_{bus} + v_c$         | 0                 | $-i_{p2}$            |                |
| on       | off      | off      | on       | $v_{bus} + v_c$      | $v_{bus} + v_c$         | $-i_{p2}$         | $-i_{p2}$            | discharges cap |
| on       | off      | on       | off      | $v_{bus}$            | $v_{bus}$               | 0                 | 0                    |                |
| on       | off      | on       | on       | N/A                  | N/A                     | N/A               | N/A                  | shoot through  |
| on       | on       | off      | off      | N/A                  | N/A                     | N/A               | N/A                  | shoot through  |
| on       | on       | off      | on       | N/A                  | N/A                     | N/A               | N/A                  | shoot through  |
| on       | on       | on       | off      | N/A                  | N/A                     | N/A               | N/A                  | shoot through  |
| on       | on       | on       | on       | N/A                  | N/A                     | N/A               | N/A                  | shoot through  |

Table 3.3 Summary of switching states when switches are operated in pairs

| $q_{12}$ | $q_{22}$ | $q_{42}$ | $q_{32}$ | $v_{p2}, i_{p2} > 0$ | $v_{p2}, i_{p2} \leq 0$ | $i_c, i_{p2} > 0$ | $i_c, i_{p2} \leq 0$ | comments       |
|----------|----------|----------|----------|----------------------|-------------------------|-------------------|----------------------|----------------|
| off      | on       | off      | on       | 0                    | 0                       | 0                 | 0                    | bypasses cap   |
| off      | on       | on       | off      | $-v_c$               | $-v_c$                  | $i_{p2}$          | $i_{p2}$             | charges cap    |
| on       | off      | off      | on       | $v_{bus} + v_c$      | $v_{bus} + v_c$         | $-i_{p2}$         | $-i_{p2}$            | discharges cap |
| on       | off      | on       | off      | $v_{bus}$            | $v_{bus}$               | 0                 | 0                    | bypasses cap   |

Figure 3.2 shows the voltage vectors characteristic of the 1.2X-3LEG topology and the 1X-3LEG topology. The voltage hexagons for the 1.2X-3LEG topology and the 1X-3LEG topology are shown in dashed lines. The extra vertical displacement in the voltage hexagon is indicated by  $v_c$ .

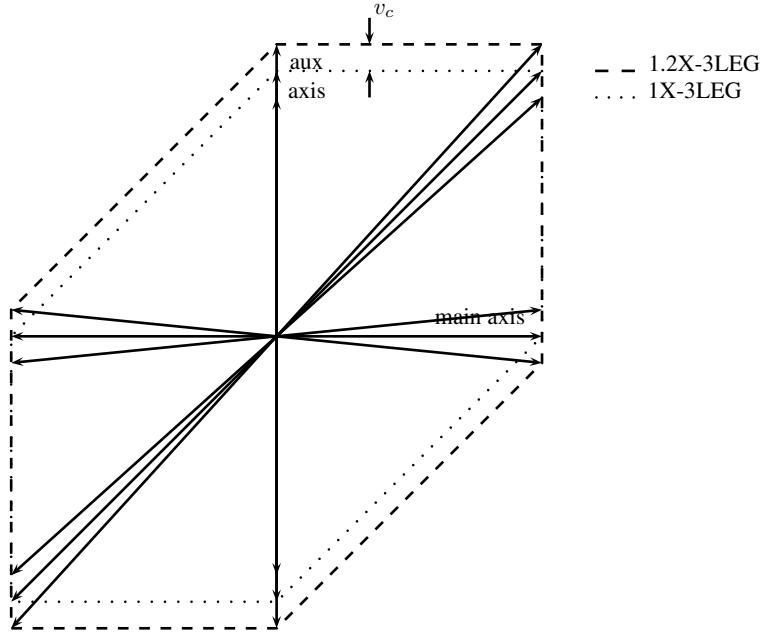


Figure 3.2 Voltage vector illustration of the 1.2X-3LEG topology and the 1X-3LEG topology. The voltage boost realized by  $v_c$  (vertical in the phase plane) is indicated.

The purpose in creating an inverter leg model is to develop a dynamic model of the inverter connected to a load, from which a control law will be established. The dynamic model

neglects the dynamics associated with the dc bus voltage, and includes the effect of the boost capacitor and the load inductance. To satisfy this requirement, a relationship between the pole voltage, pole current, and switching function is desired. To create this model from the above tables, Boolean logic is used to simplify the conduction modes above to the traditional power-electronic form of switching functions, as shown in (3.2) and (3.3).

$$\begin{aligned}
v_{p2} &= \overline{h_{12}}h_{32}(0) + \overline{h_{12}h_{32}}(-v_c) + h_{12}h_{32}(v_{bus} + v_c) + h_{12}\overline{h_{32}}(v_{bus}) \\
&= v_{bus}(h_{12}\overline{h_{32}} + h_{12}h_{32}) + v_c(h_{12}h_{32} - \overline{h_{12}h_{32}}) \\
&= v_{bus}h_{12} + v_c[h_{12}h_{32} - (1 - h_{12})(1 - h_{32})] \\
&= v_{bus}h_{12} + v_c(h_{12} + h_{32} - 1)
\end{aligned} \tag{3.2}$$

$$\begin{aligned}
i_c &= \overline{h_{12}}h_{32}(0) + \overline{h_{12}h_{32}}(i_{p2}) + h_{12}h_{32}(-i_{p2}) + h_{12}\overline{h_{32}}(0) \\
&= i_{p2}(\overline{h_{12}h_{32}} - h_{12}h_{32}) \\
&= i_{p2}[(1 - h_{12})(1 - h_{32}) - h_{12}h_{32}] \\
&= i_{p2}(1 - h_{12} - h_{32})
\end{aligned} \tag{3.3}$$

When (3.2) and (3.3) are connected to an inductance and a boost capacitor, a set of dynamic equations can be written. This results in the dynamic equations represented by the differential equation in (3.4) and the corresponding state equation in (3.5). The impedance represented by this model is an inductive load rather than a machine load with a back emf, which is sufficient at this point in the development. The objective of the model is to capture the dynamic V-I characteristics of the converter, and apply each commanded pole voltage to each of the inverter's output poles. In order to control current into a machine with a back emf, the back emf would be decoupled from the voltage command. The model shown in (3.5) is therefore sufficient to represent the dynamics of the converter. The modeling in this chapter focuses on only inverter pole 2 (with transistors  $q_{12}$ ,  $q_{22}$ ,  $q_{32}$ , and  $q_{42}$ ). Once the

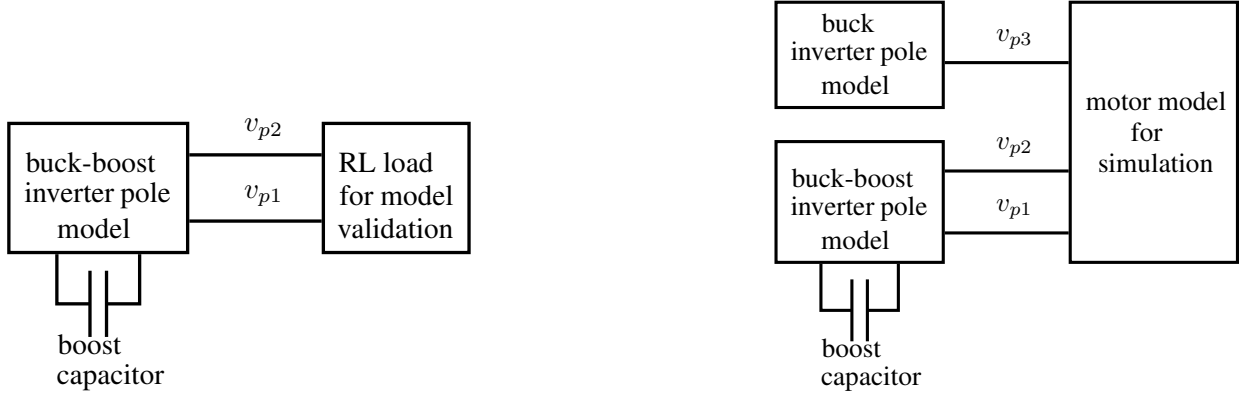


Figure 3.3 Illustration of the use of voltage modulators in the controlled motor system. This chapter makes use of the RL load. Once the voltage modulator has been validated, future chapters will make use of the complete dynamic motor model.

model for inverter pole 2 is complete, the other two poles of the inverter can be modeled as buck converters. Figure 3.3 illustrates the role of modeling the inverter poles in this chapter, which develops the constraints to take a commanded voltage,  $v_{p2}^*$ , and correctly output that voltage at the inverter pole,  $v_{p2}$ , while the control of the complete converter will be considered in subsequent chapters.

$$\begin{aligned}
 L \frac{d}{dt} i_{p2} &= v_{p2} - v_{p1} - R i_{p2} \\
 &= -R i_{p2} + v_{bus} (h_{12}) + v_c (h_{12} + h_{32} - 1) - v_{bus} (h_{11}) \\
 &= -R i_{p2} + v_{bus} (h_{12} - h_{11}) - v_c (1 - h_{12} - h_{32}) \\
 C \frac{d}{dt} v_c &= i_{p1} (1 - h_{12} - h_{32})
 \end{aligned} \tag{3.4}$$

$$\frac{d}{dt} \begin{bmatrix} i_{p2} \\ v_c \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} (1 - h_{12} - h_{32}) \\ \frac{1}{C} (1 - h_{12} - h_{32}) & 0 \end{bmatrix} \begin{bmatrix} i_{p2} \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} (h_{12} - h_{11}) \\ 0 \end{bmatrix} v_{bus} \tag{3.5}$$

In order to analyze the dynamic model for the buck-boost inverter leg, it is instructive to draw the state block diagram, which is shown in Figure 3.4. Careful inspection of the

block diagram reveals that the structure of the mathematical description of this inverter leg is similar to the structure of a dc-dc buck-boost converter. The structure enables the simultaneous control of inductor current and capacitor voltage through the control of  $h_{12}$ ,  $h_{32}$ , and  $h_{11}$ . The details of the control method will be developed in Chapter 6.

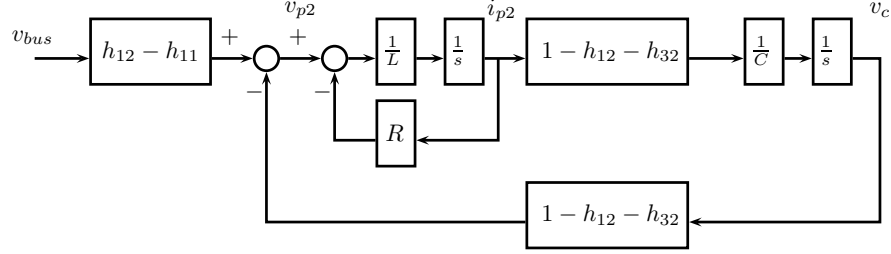


Figure 3.4 State-block diagram format of the switched-capacitor topology model

Before using this analytical model to develop a control law, it needs to be validated against established simulation methods and lab data. To perform this in the laboratory, the topology is energized with  $v_{bus} = 157 \text{ V}$ , and  $v_c = 20 \text{ V}$ . In order to keep the interpretation of the topology operation simple, the prototype topology was operated with zero output current and a fixed duty cycle. The buck switching function  $h_{12}$  is set to 50% duty cycle and the boost switching function  $h_{32}$  is set to one of two values: 25% duty cycle and 75% duty cycle. The model presented in (3.4) and (3.5) states that the output pole voltage should be independent of pole current. Since a current source was not available for validation of the experimental prototype, the experimental prototype was run at rated voltage without without any output current.

To compare with established simulation tools, a SPICE simulation is used under the same voltage conditions. The inverter output pole current was set to zero for a consistent comparison between experiment and simulation. The simulation schematic is shown in Figure 3.5. A 157 V dc supply is connected to  $v_{bus}$ , and a 20 V dc supply is connected in place of the the boost capacitance. The switching frequency is set to 10 kHz, and two simulations are run: one with a boost duty cycle of 25%, and one with a boost duty cycle of 75%.mini

In order to validate the model, the mathematical model is implemented in MATLAB and driven from the SPICE simulation inputs. The resulting plots from experiment, SPICE simulation, and the analytical model are overlaid and shown in Figure 3.6. The analytical model, SPICE model, and lab data agree very well.

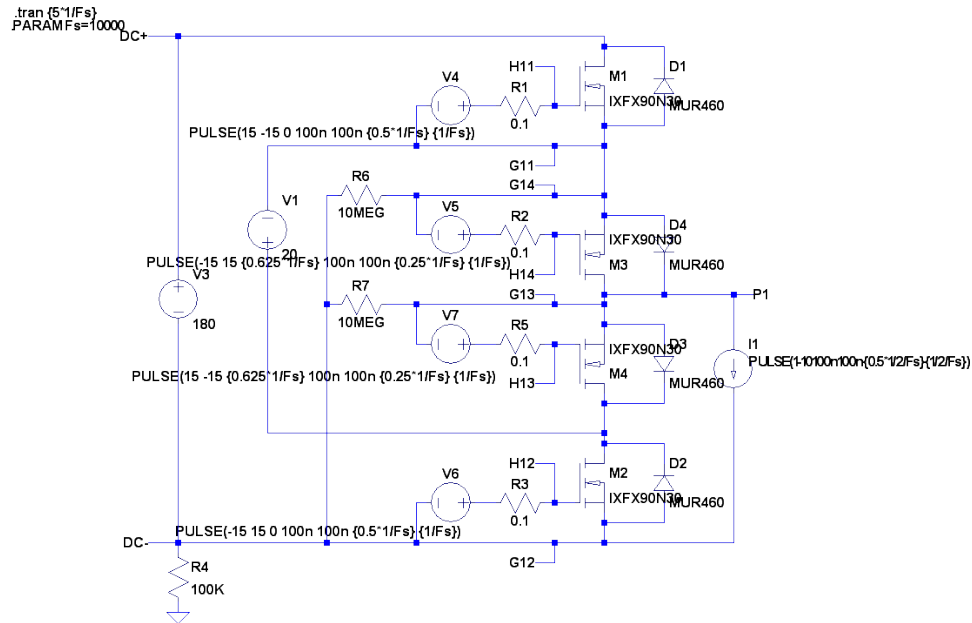


Figure 3.5 SPICE schematic used to demonstrate the voltage modeling. The output current source steps the current drawn from the pole at half the switching frequency. A bus voltage of 180V and a boost voltage of 20V are used for comparison to experimental validation of the converter.

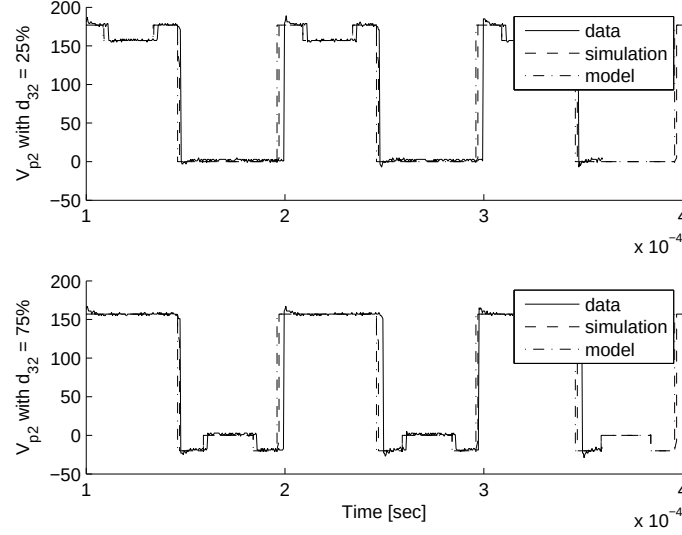


Figure 3.6 Comparison of experimental topology pole voltage to SPICE simulated pole voltage and model simulated pole voltage. The experiments were performed at  $f_{sw} = 10 \text{ kHz}$ ,  $v_{dc} = 159 \text{ V}$ ,  $v_c = 20 \text{ V}$ ,  $h_{11} = 0.5$ ,  $h_{13} = 0.25$ , and  $h_{13} = 0.75$ . The experiment, simulation, and model were each run with zero output current.

### 3.4 Limits of Capacitor Voltage Regulation

With a model of the buck-boost inverter leg established and validated, the limits of capacitor voltage regulation in terms of maintaining output currents can be developed. At a first glance, it would seem inconsistent for a single inverter leg to be able to control machine current and to use that same phase current to regulate the inverter leg's boost voltage. Indeed, there are physical limits to how this function can be accomplished. This section develops these limits, and identifies when the boost function can and cannot be successfully executed.

In order to provide a boost function, the boost capacitor voltage needs to be maintained. This requires charge balance of the capacitor, and can only be sustained for a critical combination of a critical displacement factor and firing window limit. Figure 3.7 illustrates what this looks like for a displacement factor of zero and a commanded turns ratio of 1.1. This excitation is common, due to the optimum flux level selection and the auxiliary winding

design. The displacement factor limit is not the motor power factor, but the displacement factor associated with the pole voltage and the pole current of the buck-boost inverter leg. Under capacitor (line) operation, the displacement factor of the auxiliary winding is typically zero, and under inverter operation, the power factor of the auxiliary-winding's inverter leg can be close to zero. The firing window refers to the portion of the current waveform (controlled to be sinusoidal) that needs to be used for the boost function.

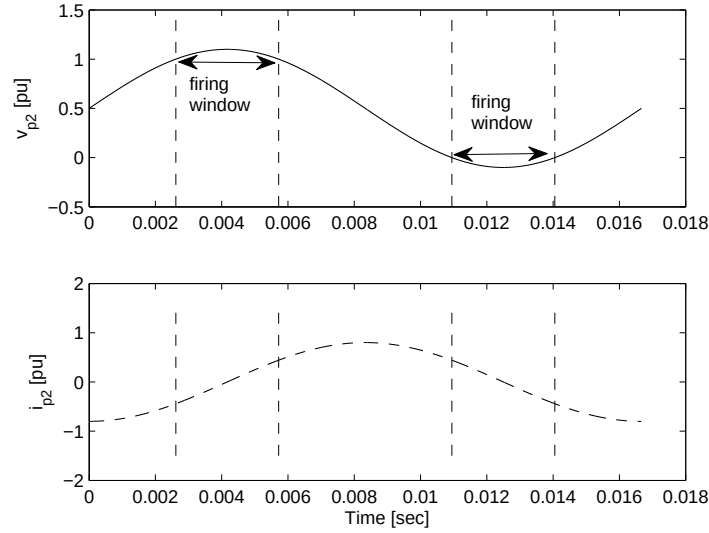


Figure 3.7 Illustration of displacement factor and firing window for regulation of capacitor voltage of the buck-boost inverter leg

The effect of the displacement factor limit and the firing window should be clear from Figure 3.7. If the power factor is zero, the magnitude of capacitor charge removal is minimized (from table 3.3, negative pole current does not charge the capacitor during boost mode). If the power factor equals 1, the magnitude of capacitor charge removal is maximized. Another way to think about this is that if the machine current crosses zero while the pole voltage command needs the boost function (near zero power factor), very little current will come in or out of the capacitor as the buck-boost leg applies the boost in voltage. If the firing angle is too wide, there will be insufficient time for the machine current to charge the capacitor before the next firing window, where boost capacitor discharge is needed. As the power

factor increases towards unity, the critical firing window narrows. It should be clear from the figure that a trigonometric relationship between firing angle and the half-bridge power factor exists. This relationship is given in (3.6). Since the exact form of the pole voltage is complicated by the modulation strategy, this analytical relationship is not developed further.

$$\begin{aligned}
 \text{charge removal} &\leq \text{charge injection} \\
 4 \int_0^\alpha i_p \sin(t - \phi) dt &\leq 4 \int_\alpha^{\pi/2} i_p \sin(t - \phi) dt \\
 \int_0^\alpha \sin(t - \phi) dt &\leq \int_\alpha^{\pi/2} \sin(t - \phi) dt
 \end{aligned} \tag{3.6}$$

In general, the constraint of the power factor and firing window result in a narrow but sufficient application space of the buck-boost inverter topology. It was noted above that the impedance angle of many PSC machines' auxiliary windings results in an auxiliary winding power factor (relationship of auxiliary winding voltage to auxiliary winding current) of 0.7 or less. For this numerical value of power factor, the buck-boost inverter leg is a practical solution to the auxiliary winding boost voltage problem.

### 3.5 Motor Efficiency and V/I Trajectories

Mademlis et al. present in [7] the off-line optimization of the motor efficiency for fixed speed operation. This assumes many constraints about the connected winding impedance network and frequency of operation, suitable to the controller they developed. Under variable speed, many of these assumptions do not hold.

Variable speed efficiency control of a PSC induction motor involves the manipulation of at least the following variables: 1) magnetizing flux, 2) stator mmf ratio, 3) stator current angle, 4) mechanical rotor speed, and 5) dynamic load torque. Under variable speed, there are multiple degrees of freedom. This section discusses the trade offs involved, and proposes an on-line strategy that can be employed to manage motor efficiency.

### 3.5.1 Motor Model

The dq motor model used in dynamic simulation is a combination of the models developed in [35] and in [36] and is given in (3.7) and (3.8). For dynamic analysis and simulation, this model can clearly be used as is. For steady-state analysis, the  $p$  operator is replaced by the  $j\omega$  operator. In this manner, the same motor model can be used throughout this research.

$$\begin{aligned}
pi_{ds}^s &= \frac{1}{\sigma L_{sm}} \left( v_{ds}^s - r'_{sm} i_{ds}^s + \frac{x_{mm}}{x_{rm}} \frac{r_{rm}}{x_{rm}} \psi_{dr}^s + \frac{N_m}{N_a} \frac{x_{mm}}{x_{rm}} \frac{\omega_r}{\omega_b} \psi_{qr}^s \right) \\
pi_{qs}^s &= \frac{1}{\sigma L_{sa}} \left( v_{qs}^s - r'_{sa} i_{qs}^s + \frac{x_{ma}}{x_{ra}} \frac{r_{ra}}{x_{ra}} \psi_{qr}^s - \frac{N_a}{N_m} \frac{x_{ma}}{x_{ra}} \frac{\omega_r}{\omega_b} \psi_{dr}^s \right) \\
\frac{p}{\omega_b} \psi_{dr}^s &= \frac{x_{mm}}{x_{rm}} r_{rm} i_{ds}^s - \frac{N_m}{N_a} \frac{r_{rm}}{x_{rm}} \frac{\omega_r}{\omega_b} \psi_{qr}^s + \frac{r_{rm}}{x_{rm}} \frac{\omega_r}{\omega_b} \psi_{dr}^s \\
\frac{p}{\omega_b} \psi_{qr}^s &= \frac{x_{ma}}{x_{ra}} r_{ra} i_{qs}^s + \frac{N_a}{N_m} \frac{r_{ra}}{x_{ra}} \frac{\omega_r}{\omega_b} \psi_{dr}^s + \frac{r_{ra}}{x_{ra}} \frac{\omega_r}{\omega_b} \psi_{qr}^s \\
T_e &= \frac{x_{mm}}{x_{rm}} \frac{1}{\omega_b} \left( \frac{N_a}{N_m} \psi_{dr}^s i_{qs}^s - \frac{N_m}{N_a} \psi_{qr}^s i_{ds}^s \right)
\end{aligned} \tag{3.7}$$

$$\begin{aligned}
x_{sm} &= x_{mm} + x_{lsm} \\
x_{sa} &= x_{ma} + x_{lsa} \\
x_{rm} &= x_{mm} + x_{lrm} \\
x_{ra} &= x_{ma} + x_{lra} \\
\sigma L_{sm} &= 1 - \frac{x_{mm}^2}{x_{sm} x_{rm}} \\
\sigma L_{sa} &= 1 - \frac{x_{ma}^2}{x_{sa} x_{ra}} \\
r'_{sm} &= r_{sm} + \left( \frac{x_{mm}}{x_{rm}} \right)^2 r_{rm} \\
r'_{sa} &= r_{sa} + \left( \frac{x_{ma}}{x_{ra}} \right)^2 r_{ra}
\end{aligned} \tag{3.8}$$

In order to control current, the back emf term in the stator equations can be decoupled, which leaves an inductive load governed by the R-L parameters  $\sigma L_{sm}$  and  $r'_{sm}$  on the main winding

and  $\sigma L_{sa}$  and  $r'_{sa}$  on the auxiliary winding. Since the buck-boost inverter leg is connected to the auxiliary winding, the auxiliary winding current becomes the pole current  $i_{p2}$ , and the inductance connected to the buck-boost inverter pole is  $\sigma L_{sa}$ . The voltage modulator would work to manipulate pole voltages  $v_{p2}$  and  $v_{p1}$  to reconstruct the commanded voltage across the auxiliary winding.

### 3.5.2 Line Operated PSC Motors and Circulating Currents Under Variable Frequency Operation

It is a difficult challenge to design a PSC motor's auxiliary winding to operate at an optimal efficiency point [20, 21, 3]. The optimal turns ratio,  $a$ , must be chosen such that an optimal capacitance connected to that winding will result in optimal efficiency for the rated load point. Not only does the capacitor need to be chosen in concert with the auxiliary winding design, but variation in any of these quantities will result in suboptimal performance. If the load point varies or if the capacitance value changes over time, the performance will degrade. In addition, installing a capacitor in series with the auxiliary winding is intentionally creating a resonant circuit with the hopes that the resonance will not get excited.

One role the fixed capacitor usually takes on is limiting the current that flows through the auxiliary winding. In this case, the currents result in unbalanced machine mmf, which give rise to significant torque pulsations. When viewed in the dual-revolving field theory framework [11], the torque pulsations give rise to significant negative-sequence torque, which results in excessive stator current harmonics, which are dissipated in the machine windings.

However, the capacitance can also create a resonant tank circuit, and can result in circulating currents between the stator main- and auxiliary-windings that do no work. These currents get dissipated as heat in the stator windings, and reduce efficiency. This effect is illustrated in Figure 3.8. which indicates the phasor values of the currents in the main winding and the auxiliary winding. This illustrates an example of the current drawn by each winding is greater than the input current, which results in a large amount of circulating current between

the main-winding and the auxiliary winding. The optimal mode of operation appears to be when the effects of negative sequence torque and circulating currents are balanced.

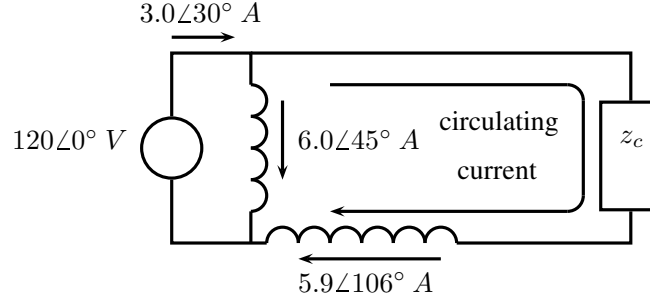


Figure 3.8 Schematic of the line-operated motor. The current in each winding is greater than the input current, which demonstrates the potential for large circulating currents.

Since the variable-speed controller manipulates the winding voltages, it is possible to operate the machine in this optimal mode of operation. However, it is also possible for the controller to operate the machine at a worse operating point than under capacitor operation. If the stator currents become dominated by circulating current, stator winding losses can easily overcome the machine rating. The variable-speed controller should ensure this operating mode is avoided.

In order for the controller to manage this trade off, the term mmf ratio is modified from the current ratio defined by Mademlis et al. in [7], and is shown in (3.9). For example, when the machine mmf is balanced, the mmf ratio is unity, and under line operation, the mmf ratio is often between 2 and 10. However, it is difficult to compare the concept of mmf ratio to mmf ratio under variable-speed operation, since the phase angle between currents cannot be directly controlled. The ratio of currents will decrease as capacitance is increased.

$$mmf_{ratio} = \frac{N_m |i_m|}{N_a |i_a|} \quad [3.9]$$

In this research, the mmf ratio will be used as a metric to evaluate the balance between torque pulsations, circulating current, and balanced mmf.

### 3.5.3 Loss Distribution and the Effect of Magnetizing Flux

PSC motors are often constructed from inexpensive materials, and core loss makes up a dominant portion of the motor losses. At rated frequency and rated voltage, the three principle loss components are roughly split equally in thirds: 1/3 of the machine losses are comprised of stator copper losses, 1/3 of the machine losses are comprised of rotor copper losses, and 1/3 of the machine losses are comprised of core loss [33].

PSC motors are designed to operate within a range of input voltage. In other words, the motor is designed to meet its specifications when operated from 110% voltage and from 85% voltage. This suggests that most PSC motors are designed with some margin and can therefore be underexcited and still produce the required torque for their rating point. When this happens, it is anticipated that motor efficiency will increase as the motor voltage is decreased and all other control variables are kept constant. This effect is described in [7] and is more directly shown in Figure 3.9.

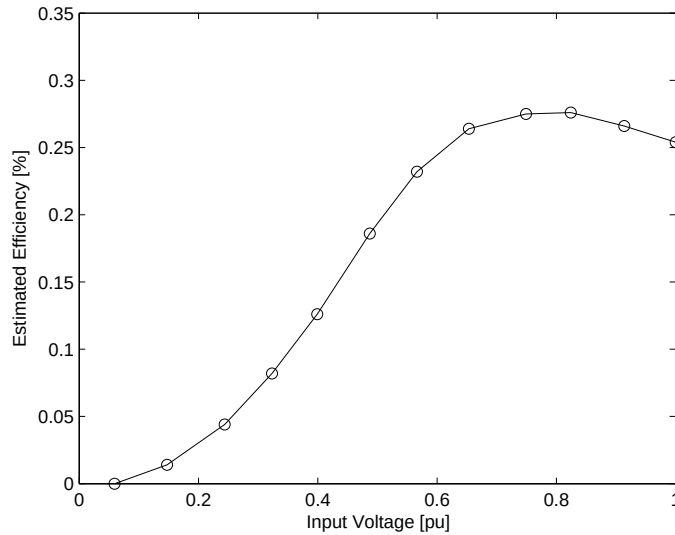


Figure 3.9 Estimated motor efficiency as a function of applied stator voltage, based on measured motor power

Under variable frequency operation, the frequency and flux should be selected to operate the machine with acceptable efficiency to work against the load with acceptable performance. For example, to work against a fan load, a  $(V/\text{Hz})^2$  relationship should be used to determine the flux level. For best results, the specific numerical value of voltage should be characterized for the specific machine under consideration, and 90% of nominal works well for many PSC motors. When the machine is controlled with a variable-speed controller, the efficiency should improve significantly for at least two reasons: 1) the flux level can be set to the optimal efficiency value for the load (90% in the above example for rated frequency), and 2) the circulating current condition can be eliminated, thereby minimizing stator and rotor copper losses.

#### **3.5.4 Effect of MMF Ratio on Efficiency**

Nonlinear programming of the PSC motor efficiency problem reveals that the efficiency is insensitive to small variations in current angle. The efficiency is therefore primarily a function of the load, machine flux level, and mmf ratio. The optimal mmf ratio should, by intuition, be bounded on the low end by the balance point, and on the high end by the line-operation mmf ratio. This is illustrated in Figure 3.10.

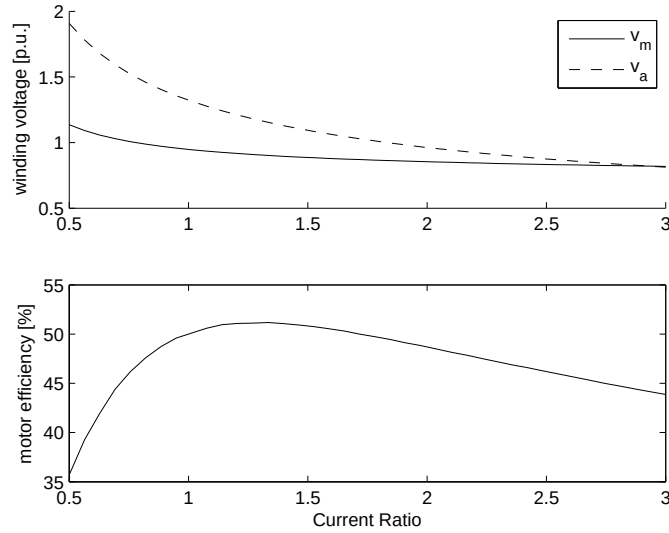


Figure 3.10 Variation of winding voltage and efficiency vs. mmf ratio. The phase angle of the two winding currents is held at  $90^\circ$ . Some interesting mmf ratios for this machine include: 1) ratio = 1.0: balanced excitation, 2) ratio = 1.15: optimal efficiency, 3) ratio = 3.0: line-operation mmf ratio (but the currents are not shifted by  $90^\circ$  under line operation).

### 3.6 Boost Leg Control

The objective of the boost leg controller is to generate duty-cycle commands that will regulate the boost capacitor voltage and that will faithfully recreate the commanded pole voltage. This is illustrated in block-diagram format in Figure 3.11. Functionally, the boost controller takes a pole voltage command and decouples the effects of capacitor voltage and duty cycles  $d_{12}$  and  $d_{32}$ .

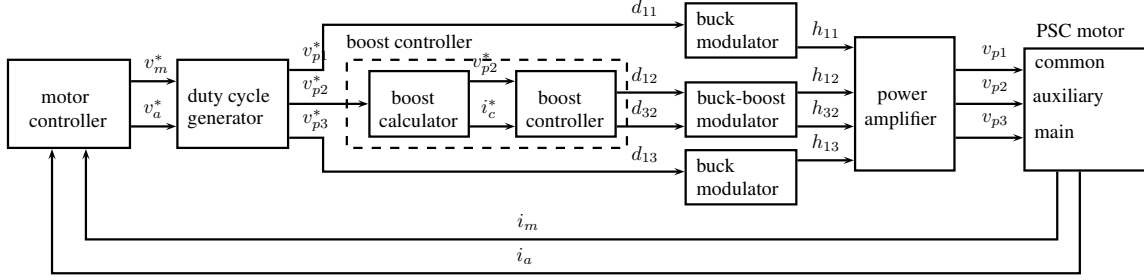


Figure 3.11 Block diagram of control of PSC motor with buck-boost inverter leg. The buck-boost inverter leg controller is able to reconstruct  $v_p^*$  and simultaneously regulate the capacitor voltage.

### 3.6.1 Boost Duty Cycle Generation and Decoupling $v_{p2}^*$ from Capacitor Voltage Regulation

In order to correctly control boost voltage within the constraints of the conducted machine currents, the analytical model in (3.10) is solved to directly express the switching functions in (3.11).

$$\begin{aligned} v_{p2} &= v_{bus} d_{12} - v_c (1 - d_{12} - d_{32}) \\ i_c &= i_{p2} (1 - d_{12} - d_{32}) \end{aligned} \quad [3.10]$$

$$\begin{aligned} d_{12} &= \frac{v_{p2}}{v_{bus}} + \frac{i_c}{i_{p2}} \frac{v_c}{v_{bus}} \\ d_{32} &= 1 - \frac{i_c}{i_{p2}} - \frac{v_{p2}}{v_{bus}} - \frac{i_c}{i_{p2}} \frac{v_c}{v_{bus}} \\ &= 1 - d_{12} - \frac{i_c}{i_{p2}} \end{aligned} \quad [3.11]$$

Since duty cycle ratio is limited to  $0 \leq d \leq 1$ , there are limits to the instantaneous and averaged numerical values that  $h_{11}$  and  $h_{31}$  can take. This constraint is given in (3.12) through (3.13).

$$\begin{aligned}
0 &\leq \frac{v_{p2}}{v_{bus}} + \frac{i_c}{i_{p2}} \frac{v_c}{v_{bus}} \leq 1 \\
0 &\leq 1 - \frac{i_c}{i_{p2}} - \frac{v_{p2}}{v_{bus}} - \frac{i_c}{i_{p2}} \frac{v_c}{v_{bus}} \leq 1
\end{aligned} \tag{3.12}$$

In order to control this topology, it will be shown that  $i_c^*$  is the manipulated input to the capacitor voltage controller. If the constraint equation is written in terms of  $i_c^*$  and  $v_{p2}$ , the constraint becomes that shown in (3.13).

$$\begin{aligned}
0 &\leq \frac{v_{p2}}{v_{bus}} + \frac{i_c^*}{i_{p2}} \frac{v_c}{v_{bus}} \leq 1 \\
0 &\leq 1 - \frac{i_c}{i_{p2}} - \frac{v_{p2}}{v_{bus}} - \frac{i_c^*}{i_{p2}} \frac{v_c}{v_{bus}} \leq 1
\end{aligned}$$

$$\begin{aligned}
-\frac{\frac{v_{p2}}{v_{bus}}}{\frac{v_c}{v_{bus}}} &\leq \frac{i_c^*}{i_{p2}} \leq \frac{1 - \frac{v_{p2}}{v_{bus}}}{\frac{v_c}{v_{bus}}} \\
\frac{\frac{v_{p2}}{v_{bus}}}{1 + \frac{v_c}{v_{bus}}} &\leq \frac{i_c^*}{i_{p2}} \leq \frac{-1 + \frac{v_{p2}}{v_{bus}}}{1 + \frac{v_c}{v_{bus}}}
\end{aligned} \tag{3.13}$$

$$\max \left( -\frac{v_{p2}^*}{v_c}, \frac{v_{p2}^*}{1 + \frac{v_c}{v_{bus}}} \right) < \frac{i_c^*}{i_{p2}} < \min \left( \frac{1 - \frac{v_{p2}^*}{v_{dc}}}{\frac{v_c}{v_{bus}}}, \frac{1 - \frac{v_{p2}^*}{v_{bus}}}{1 + \frac{v_c}{v_{bus}}} \right) \tag{3.14}$$

In order to correctly constrain the duty cycle ratios, the minimums and maximums given in (3.14) are applied to the four quantities identified in (3.13). If this is done, the duty cycle commands will correctly generate the commanded pole voltage and boost capacitor current.

When in boost mode, the commanded current command may be set to zero, since the limits will always result in a current command that is negative. A limit can be imposed on the current command if capacitor voltage cannot otherwise be maintained.

When in buck mode, the commanded current is generated from a boost capacitor voltage regulator, which will be developed in chapter 6. The required limits are imposed on this current command and faithfully result in the commanded voltage and current.

### 3.7 Summary

This chapter introduced the buck-boost inverter topology. In order to develop a control law for the power converter, an analytical model of the 1.2X-3LEG topology was developed and validated with SPICE simulation and laboratory data. The operation and limits to successful boost capacitor voltage regulation were identified and a control structure to regulate capacitor voltage and decouple capacitor voltage regulation from pole voltage output was developed.

## Chapter 4

### Comparative Evaluation

Chapter 1 introduced the potential benefit of operating a PSC motor from a variable-speed power converter, and chapter 2 summarized the power-converter topologies that have been developed to operate PSC motors. This chapter further develops comparison metrics and evaluates the proposed topology against the state of the art approaches.

#### 4.1 Topology Comparison and Selection

In order to compare the feasibility of semiconductor-based power converters, the price of semiconductors needs to be analyzed. Cost can be analyzed, but price is driven by many factors, and is difficult to accurately predict or analyze. A reasonable method to approximate price trends is a VA study. By studying the voltage-current product of power semiconductors, relationships that model the price drivers may be studied. For example, if a circuit is designed with power transistors that block 600 V in the off state, the VA product will track linearly with variation in device current capacity. If prices are sampled from distributors, the same trend can be observed, even though it is distorted with shifts in price as package sizes change and markets push economic forces.

In order to compare the available topologies, the following characteristics of the topologies are included in the VA study: 1) converter efficiency, 2) motor efficiency, 3) silicon VA utilization, and 4) passive VA utilization. By treating semiconductor VA on a normalized basis, inverter topology cost can be compared relatively independent of price. By treating

passive VA utilization the required passive devices can be compared between topologies. Efficiencies are compared using the traditional relationship of input power to output power.

#### 4.1.1 VA Rating Definitions

VA ratings can be divided into semiconductor VA and passive VA. The VA rating for semiconductors is defined as the blocking voltage of the semiconductor (i.e., the nominal dc link voltage of the converter) multiplied by the nominal rms current of the device. Worst case ratings would be included for worst-case design analysis, but for the comparison performed here, the nominal ratings are used. The VA rating for semiconductors is shown in (4.1).

$$VA_{si} = v_{block} i_{rms} \quad [4.1]$$

The VA rating for passive devices in the state-space representation of a power converter's energy storage elements can be characterized in at least two ways: 1) the product of the dc value of the element's state variable and the rms value of its covariable (for example, a capacitor's VA rating would be  $v_{cap,dc} i_{rms}$ , 2) the stored energy in the element (for example, a capacitor's VA rating would be  $\frac{1}{2} C v_{cap}^2$ ). The first method is used in this analysis, as shown in (4.2).

$$\begin{aligned} VA_{cap} &= v_{cap} i_{rms} \\ VA_{ind} &= i_{pole} v_{rms} \end{aligned} \quad [4.2]$$

#### 4.1.2 Per-Unit System

The per-unit system used in this evaluation is given below. The primary base quantities are given in (4.3), and the secondary quantities are given in (4.4). This is the same approach as is often taken in normalizing three-phase systems. The motor output power sets the base power, and the line voltage sets the base voltage. The base current is the ratio between

power and voltage, scaled by the number of phases in the motor. The secondary quantities are defined in the usual manner, and produce base impedance, frequency, and torque.

$$\begin{aligned}
 P_b &= P_R \\
 V_b &= V_{R,pk} \\
 I_b &= \frac{2 P_b}{2 V_b} \\
 &= \frac{P_b}{V_b}
 \end{aligned} \tag{4.3}$$

$$\begin{aligned}
 Z_b &= \frac{V_b}{I_b} \\
 \omega_b &= 2\pi F_b \\
 \omega_{mb} &= \frac{2}{P} \omega_b \\
 T_b &= \frac{2 P}{2} \frac{1}{2 \omega_b} V_b I_b \\
 &= \frac{P}{2} \frac{1}{\omega_b} V_b I_b
 \end{aligned} \tag{4.4}$$

Due to the low efficiency of PSC motors, currents will be significantly higher than 1.0 pu. To illustrate this effect, table 4.1 summarizes the per-unit scaling of a 1/6 hp PSC induction motor.

Table 4.1 Per-Unit Scaling of a 1/6 hp PSC Induction Motor

| Quantity | Value        | Quantity      | Value                 | Quantity | Value        | Quantity | Value |
|----------|--------------|---------------|-----------------------|----------|--------------|----------|-------|
| $P_b$    | 125 W        | $\omega_b$    | $377 \frac{rad}{sec}$ | $R_{1m}$ | $7.5 \Omega$ | $r_{1m}$ | 0.035 |
| $V_b$    | 169.7 V      | $P$           | 6                     | $R_{1a}$ | $15 \Omega$  | $r_{1a}$ | 0.071 |
| $I_b$    | 0.765 A      | $\omega_{mb}$ | $126 \frac{rad}{sec}$ |          |              |          |       |
| $Z_b$    | $213 \Omega$ | $T_b$         | 0.989 N-m             |          |              |          |       |

For this example motor, the nameplate current is 1.9A. Assuming a utility power factor of 0.8 (lag), the efficiency is 72%. Assuming a turns ratio of 1.2, and that the capacitor is able to balance the winding MMF's, the three machine currents are  $I_m = 1.72 [pu]$ ,  $I_a = 1.44 [pu]$ ,  $I_n = 3.51 [pu]$ . It is interesting that if an alternative normalization is used to set the rated current near 1.0 pu, the leakage reactance terms become close to the expected value of 0.1 [pu], and the resistance of the machine approaches the leakage impedance of 0.1 [pu]. It is not surprising that the impedance angle of the windings in this type of machine approach 45 degrees.

### 4.1.3 Comparison of Topologies 2X-2LEG with 1X-3LEG

The bulk semiconductor VA rating uses the definitions above and applies them to the topology under examination. The VA rating for a given topology is therefore the product of the number of devices, the blocking voltage, and the rms current through the device, as given in (4.5). The benchmark for this research is somewhat arbitrarily chosen to be that of 1X-3LEG. The relative VA for each topology is therefore the quotient of the topology's VA rating and the VA rating of the 1X-3LEG topology.

$$VA_{topology,si} = n \cdot v_{block} i_{rms} \quad [4.5]$$

The VA rating for the passive devices is determined by the VA rating for passive devices described above, multiplied by the number of passive devices required by the topology, as given in (4.6). The relative VA is normalized to the VA rating of the 1X-3LEG topology, as discussed above for the topology's semiconductor VA rating.

$$\begin{aligned} VA_{topology,capacitor} &= n \cdot v_{dc} i_{rms} \\ VA_{topology,inductor} &= n \cdot i_{dc} v_{rms} \end{aligned} \quad [4.6]$$

The switching losses and conduction losses are defined using the standard metrics for IGBT's and MOSFET's, and is given in (4.7) and (4.8).

$$\begin{aligned} P_{sw,IGBT} &= f_{sw} (E_{on} + E_{off}) \\ P_{cond,IGBT} &= v_{on} i_{p,rms} \end{aligned} \quad [4.7]$$

$$\begin{aligned} P_{sw,FET} &= f_{sw} (E_{on} + E_{off}) \\ P_{cond,FET} &= i_{p,rms}^2 r_{ds,on} \end{aligned} \quad [4.8]$$

For the semiconductor VA rating analysis, the bus voltage of the 2X-2LEG topology operates at twice the bus voltage of the 1X-3LEG topology, so the per-device semiconductor VA rating is double for the same output current. Similarly, the VA rating of the capacitance for the 2X-2LEG topology is double that of the 1X-3LEG topology due to the same output rms current, and the doubling of the bus voltage.

In order to compute efficiency, the machine model presented in (3.7) is specialized to the steady state, the main winding is excited with the maximum voltage that the topology can supply, and the currents are constrained to be orthogonal. The load is set to follow a simple fan curve, with rated power being delivered at maximum frequency. The efficiency is calculated as shown in (4.9). The losses in the passive components are assumed to be zero.

$$\begin{aligned} \eta_{motor} &= \frac{\omega_{rm} T_e}{\Re(V_m I_m^\dagger + V_a I_a^\dagger) + P_{core}} \\ \eta_{vfd} &= \frac{P_{out}}{P_{out} + P_{sw,IGBT} + P_{cond,IGBT} + P_{sw,FET} + P_{cond,FET}} \\ \eta_{system} &= \eta_{vfd} \eta_{motor} \\ P_{core,R} &= \frac{1}{3} \frac{1}{\eta_R} P_{out} \\ P_{core} &= P_{core,R} \left( \frac{V/Hz}{V/Hz_R} \right)^{2.5} \left( \frac{f}{f_R} \right)^{1.4} \end{aligned} \quad [4.9]$$

Table 4.2 List of symbols used in efficiency calculation

| Parameter       | Value    | Description                                  |
|-----------------|----------|----------------------------------------------|
| $V_m$           | 120 V    | Voltage phasor applied to the main winding   |
| $V_a$           | 173 V    | Voltage phasor applied to the aux winding    |
| $P_{out}$       | 125 W    | Rated motor output power                     |
| $P_{core,R}$    | 125 W    | Core loss at rated operating point           |
| $P_{core}$      | 125 W    | Core loss at operating point                 |
| $V/Hz_R$        | 2.0 V/Hz | Rated volts per hertz                        |
| $V/Hz$          | 2.0 V/Hz | Volts per hertz                              |
| $\eta_{vfd}$    | 0.95     | Efficiency of inverter topology              |
| $\eta_{motor}$  | 0.4      | Efficiency of motor under inverter operation |
| $\eta_{system}$ | 0.38     | Efficiency of motor and inverter as a system |

The resulting VA comparison of the 2X-2LEG and 1X-3LEG topologies is tabulated in table 4.3. The efficiency of the three-leg inverter suffers dramatically due to the reduced output voltage capability. The winding stress of the two-leg topology is high due to the voltage-doubling rectifier, and the capacitor bank in the two-leg inverter needs to withstand twice the voltage as the one in the three-leg inverter. In all other respects, the two converters are very similar. The semiconductors in the two-leg topology need to withstand twice the voltage as the ones in the three-leg inverter, so the efficiency per device is worse, but there are fewer devices. As a result, the converter efficiency is roughly equivalent.

Table 4.3 VA study comparison of 2X-2LEG and 1X-3LEG topologies

| Topology         | Silicon VA  | Passive VA  | Motor Efficiency | Converter Efficiency | System Efficiency | Winding Stress |
|------------------|-------------|-------------|------------------|----------------------|-------------------|----------------|
| Line             | 0           | 1.56        | 40%              | 100%                 | 40%               | <1.0           |
| CHP-TRIAC        | 0.17        | 1.56        | 43%              | 97%                  | 42%               | <1.0           |
| CHP-PWM          | 0.67        | 1.56        | 42%              | 97%                  | 41%               | <1.0           |
| 1X-2LEG          | 0.51        | 1.00        | 29%              | 97%                  | 28%               | 1.00           |
| 1X-3LEG          | 1.00        | 1.00        | 35%              | 94%                  | 33%               | 1.00           |
| 2X-2LEG          | 1.02        | 2.00        | 50%              | 96%                  | 48%               | 2.00           |
| 2X-3LEG          | 2.00        | 2.00        | 50%              | 93%                  | 47%               | 2.00           |
| <b>1.2X-3LEG</b> | <b>1.26</b> | <b>1.13</b> | <b>52%</b>       | <b>93%</b>           | <b>48%</b>        | <b>1.00</b>    |

#### 4.1.4 Comparison of Topologies and Remarks

Extending the approach from the previous section to all the topologies listed in chapter 2, the topologies are compared on a relative basis of efficiency, motor winding stress, semiconductor VA rating, and passive VA rating. The resulting comparison is shown in Figure 4.1.

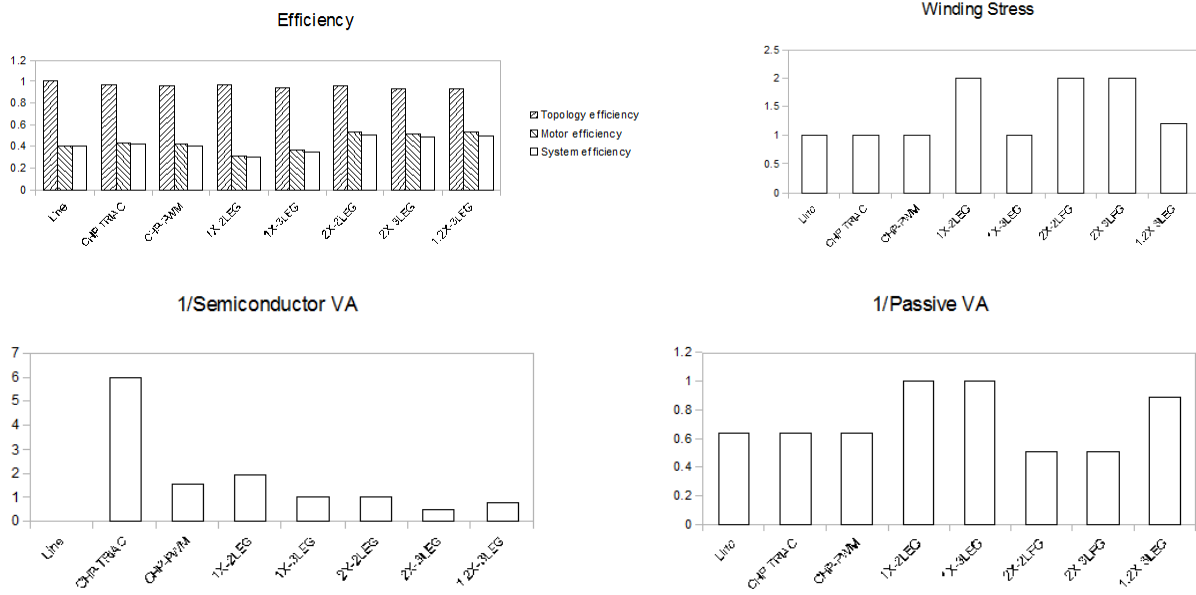


Figure 4.1 Comparison of topology efficiency, motor efficiency, silicon VA, and passive VA for each of the major PSC inverter topologies

Due to the poor resulting motor efficiency, the ac chopper circuits are not considered further. The 2X-2LEG topology spans an attractive voltage capability space, but the motor winding stress is high compared to the competing topologies. This further motivates the study of the 1X-3LEG topology for improvement. The rest of this research studies the 1.2X-3LEG topology, using the 1X-3LEG topology as a baseline for comparison purposes.

## 4.2 Summary

This chapter compared the proposed topology against the candidate topologies to be used in a PSC variable-speed drive. A VA study was introduced, and the attributes of each topology were included in the analysis. As a result of this analysis, the 1.2X-3LEG topology is identified to be a competitive candidate for the realizing the broad goals of this work. The remaining chapters of this dissertation will develop detailed modulation of the power converter and control of the inverter and motor as a system.

## Chapter 5

### Modulation Strategy for the Three-Leg Inverter

The previous chapters developed the motivation for using a three-leg buck-boost inverter with a PSC motor. The criteria for stable operation were identified, but not developed in detail sufficient to implement a complete switching converter. This chapter develops the modulation strategy necessary to operate the buck-boost inverter leg, and develops two modulation strategies to independently generate the main- and auxiliary-winding voltages using a three-leg inverter. The consequences of motor excitation with non-sinusoidal waveforms is examined, and a overall modulation strategy is selected.

#### 5.1 Buck-Boost Inverter Leg Modulation

The analytical model for the buck-boost inverter leg was developed in chapter 3. In order to regulate voltage on the boost capacitor, the boost leg needs to be modulated correctly. If incorrect modulation is performed, energy will be circulated in the PSC motor windings and inefficiently dissipated in their resistance, ripple current through the boost capacitor will exceed the capacitor's design limits, and the boost inverter leg will fail to perform its function.

##### 5.1.1 Boost Modulation Polarity Example

The duty-cycle ratio relationships identified in (3.11) and (3.13) determine the average duty ratios  $d_{12}$  and  $d_{32}$ , but they do not determine the phase relationship between  $h_{12}$  and  $h_{32}$ .

In order to develop the switching functions  $h_{12}$ , and  $h_{32}$  necessary to operate transistors  $q_{12}$  and  $q_{32}$ , the polarity of modulation of  $h_{12}$  and  $h_{32}$  needs to be correctly determined. In order to explore this, a SPICE simulation is used to set the duty ratio  $d_{12} = d_{32} = 0.5$ . The motor neutral connection is tied to the negative side of the dc bus. In this case, the pole voltage of the buck-boost inverter leg is described by (5.1), and the average value of the inverter pole's output voltage should be  $0.5 v_{bus}$ . However, in order to set the duty cycle, the boost switching function  $h_{32}$  can either be operated the same as the buck switching function  $h_{12}$ , or the  $h_{32}$  can be operated as the complement of  $h_{12}$ . Only one of these modes will result in the correct inverter pole voltage and pole current.

This effect is shown in Figure 5.1. The switching functions  $h_{12}$  and  $h_{32}$  are shown in the top two oscillograms. The third and fourth waveforms are the output pole voltage ( $v_{p2}$ ) and the boost capacitor current ( $i_c$ ). Since the boost transistors are not performing any boost function, the pole voltage should be proportional to the buck switching function  $h_{12}$ , and the capacitor current should be zero. It is clear from Figure 5.1 that when  $h_{32} = h_{12}$  (Figure 5.1a), the output is incorrect, and when  $h_{32} = 1 - h_{12}$  (Figure 5.1b), the output is correct.

$$\begin{aligned}
 d_{12} &= 0.5 \\
 d_{32} &= 0.5 \\
 v_{p2} &= v_{bus}d_{12} - v_c(1 - d_{12} - d_{32}) \\
 &= 0.5v_{bus}
 \end{aligned} \tag{5.1}$$

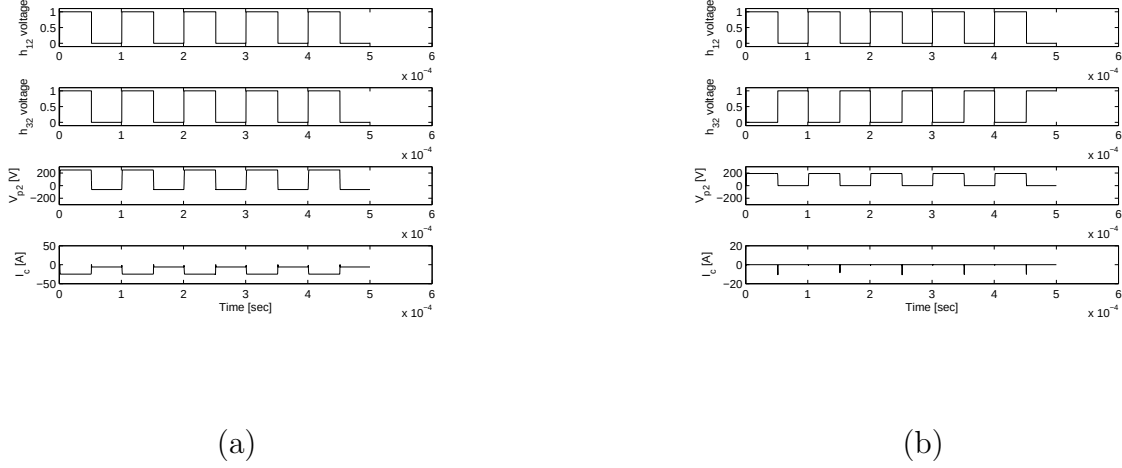


Figure 5.1 Waveforms from simulations illustrating the example of correct and incorrect modulation where  $d_{12} = 1 - d_{32}$  ( $v_p$  tracks  $d_{11}^*$  and there is no boost function). No dead time is included in this SPICE simulation, so there are some transients in the capacitor current.

Because of this effect, the modulation polarity shown in Figure 5.1b will be used in the rest of this research. If the duty-cycle ratio is limited as described in chapter 3 and operated with the correct polarity as shown in Figure 5.1b, the buck-boost inverter leg will output pole voltage commanded by the switching functions  $h_{12}$  and  $h_{32}$ .

### 5.1.2 Boost Modulation

The constraint developed in (3.13) results in the duty cycle ratios shown in (5.2). Since the switching function  $h_{32}$  is generated in complementary mode to  $h_{12}$ , as illustrated in Figure 5.1b, the duty cycle ratio  $d_{32}^*$  is output to  $d_{32}$ , the incorrect value of  $v_{p2}$  will be output at the inverter pole. On the other hand, if  $d_{32} = 1 - d_{32}^*$ , the correct value of  $v_{p2}^*$  will be output at the inverter pole.

$$\begin{aligned}
 d_{12}^* &= \frac{v_{p2}^*}{v_{bus}} + \frac{i_c^*}{i_{p2}} \frac{v_c}{v_{bus}} \\
 d_{32}^* &= 1 - \frac{i_c^*}{i_{p2}} - \frac{v_{p2}^*}{v_{bus}} - \frac{i_c^*}{i_{p2}} \frac{v_c}{v_{bus}}
 \end{aligned} \tag{5.2}$$

The operation of the buck-boost inverter leg is demonstrated in Figure 5.2. The pole voltage command and capacitor voltage are given in (5.3). Figure 5.2a shows the complementary characteristic of  $d_{12}$  and  $d_{32}$ , and Figure 5.2b shows the complementary characteristic of  $h_{12}$  and  $h_{32}$ .

$$v_c = 0.4 \text{ [pu]}$$

$$v_{p2}^* = 1.2 \sin(\omega_e t) \text{ [pu]} \quad [5.3]$$

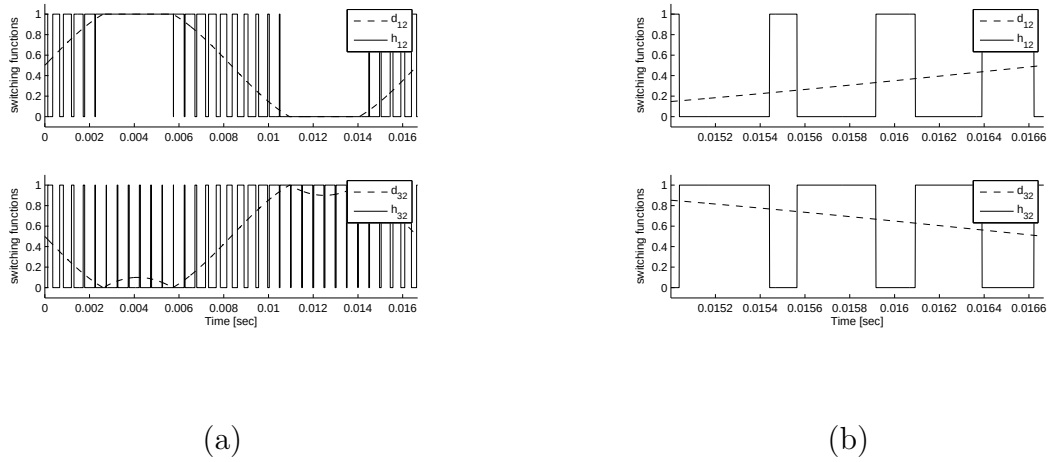


Figure 5.2 Waveforms from simulations illustrating the modulation of the buck-boost inverter in all buck and boost modes. The capacitor voltage is fixed at  $v_c = 0.2$  pu for illustration of the switching functions.

The commanded auxiliary-winding voltage command and the resulting auxiliary winding voltage are shown in Figure 5.3. For this example, the neutral voltage is tied to the negative dc bus terminal. The commanded auxiliary-winding voltage command is therefore offset and scaled by 0.5. From this figure it is clear that, assuming a constant  $v_c$ , the buck-boost inverter leg is able to apply greater than  $v_{bus}$  and less than 0 at the inverter leg pole output.

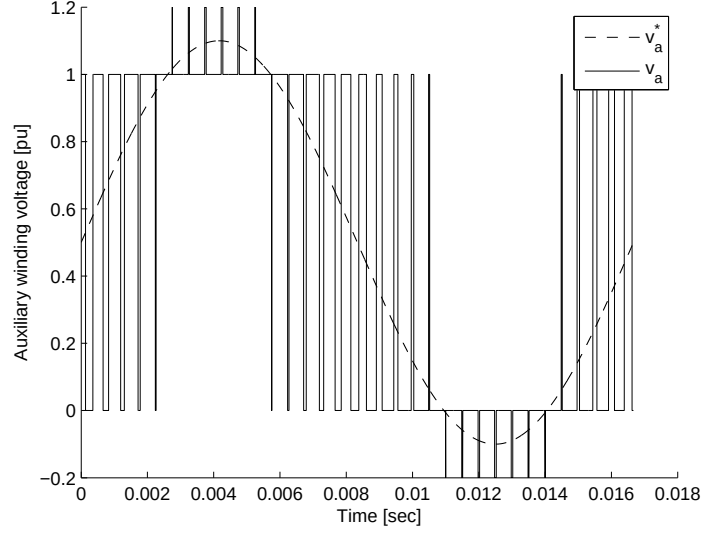


Figure 5.3 Auxiliary winding voltage waveforms using the buck-boost leg modulation for the inverter

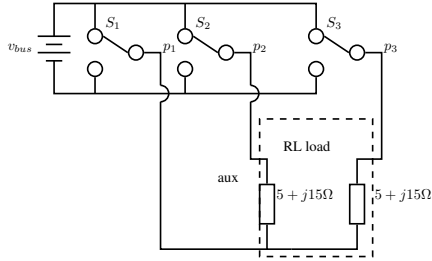
In order to apply independent voltages across the main winding and the auxiliary winding, the modulation of  $v_{p1}$ ,  $v_{p2}$ , and  $v_{p3}$  need to be coordinated in order to generate the desired voltages  $v_a$  and  $v_m$  across the auxiliary winding and the main winding, respectively.

## 5.2 Three-Leg Modulation

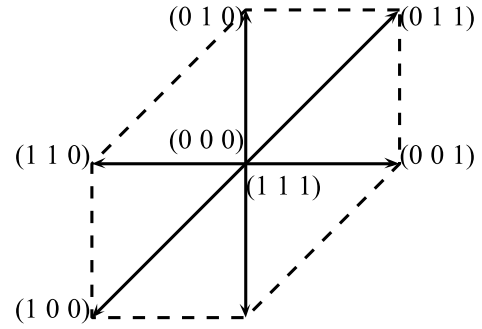
The task of modulating two phase voltages from three inverter legs is rich with trade offs. The basic categories of trade offs can be divided into two categories: 1) the controller reduces the modulation index to avoid distortion, and 2) the modulation index is raised above the distortion limit to increase output frequency. As shown above, the voltage capability hexagon becomes asymmetric (due to how the machine is connected), and that the machine windings are not a multiple of the topology output poles. If the machine had a fourth connection, modulation of the pole voltages becomes symmetric, overdetermined, and trivial. Several works in the literature present ways to approach this problem [37, 38].

When only three inverter output legs are connected to the three-terminal PSC motor, the inverter hexagon becomes skewed, and sinusoidal modulation of the output voltages cannot produce the voltage necessary to produce a smoothly rotating mmf in the machine at high modulation indices, as discussed in [39]. For this reason, much of the literature proposes the increase of dc-bus voltage in PSC inverters, thereby reducing the modulation index to about 0.5 (this may vary depending on the asymmetry of the machine). However, in looking at the voltage envelope of the power converter in Figure 5.4, it is clear that the 1X-3LEG topology is capable of delivering rated voltage in quadrants I and III. If the inverter is modulated so that a limited amount of distortion is intentionally added to the output waveforms, the motor winding stress can be reduced from the level that is required for no distortion.

This section develops a modulation strategy to solve the three-terminal PSC motor's modulation problem with the same basic assumption: the topology is able to deliver  $v_{bus}$  to the motor terminals in quadrants I and III, and the modulation strategy should not limit this to  $\frac{1}{2}v_{bus}$ , as is frequently done to reduce harmonic distortion in the voltage commands. This section develops a “trapezoidal” method, so named for the trapezoidal character of the neutral voltage reference waveform. This section concludes by evaluating the modulation strategy using a weighted harmonic distortion metric.



(a)



(b)

Figure 5.4 Simplified schematic of proposed inverter illustrated as a 1X-3LEG inverter feeding an R-L load and the voltage capability hexagon illustrating switching states of (S1, S2, S3)

### 5.2.1 Trapezoidal Modulation

If the commanded neutral voltage is set to a function of the arctangent of the commanded voltage angle, a reference voltage resembling a trapezoid results for the neutral voltage, as shown in Figure 5.5 for a turns ratio of  $a = 1.18$  and an auxiliary voltage command that lags the main voltage command by  $90^\circ$ . The remaining duty-cycle ratio commands for inverter legs 2 and 3 are slaved from the neutral voltage.

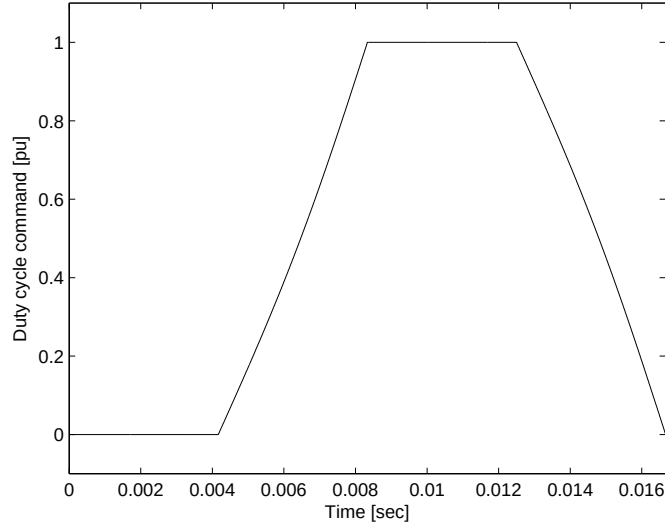


Figure 5.5 A typical waveform of neutral voltage duty-cycle ratio command under trapezoidal modulation

The neutral voltage command is set by the commanded angle, and the magnitude is set to transition from 0 to 1, regardless of the magnitude of the machine voltage commands. The result is the pole voltage command set in (5.4).

$$\begin{aligned} \theta^* &= \tan^{-1} \frac{v_a^*}{v_m^*} \\ d_{11} &= \begin{cases} 0 & 0 < \theta^* \leq \frac{\pi}{2} \\ \frac{2}{\pi} \left( \theta^* - \frac{\pi}{2} \right) & \frac{\pi}{2} < \theta^* \leq \pi \\ 1 & \pi < \theta^* \leq \frac{3\pi}{2} \\ \frac{2}{\pi} (-\theta^*) & \frac{3\pi}{2} < \theta^* \leq 2\pi \end{cases} \end{aligned} \quad [5.4]$$

If the neutral voltage is constrained, the pole voltages  $v_{p2}$  and  $v_{p3}$  are uniquely determined by  $v_m$ ,  $v_a$ , and  $v_{p1}$ . The relationship between the duty-cycle ratios and the neutral point voltage is given in (5.5).

$$v_a = v_{bus} (d_{12} - d_{11})$$

$$\begin{aligned}
v_m &= v_{bus} (d_{13} - d_{11}) \\
d_{12} &= d_{11} + \frac{v_a^*}{v_{bus}} \\
d_{13} &= d_{11} + \frac{v_m^*}{v_{bus}}
\end{aligned} \tag{5.5}$$

Representative waveforms for the trapezoidal modulation approach are shown in Figure 5.6. These demonstrate the pole voltage commands to each inverter leg and the resulting output voltage commands that result from appropriate limits to duty ratio of each transistor command. From these waveforms it is clear that the magnitude of the boost requirement and the waveform distortion is relatively low.

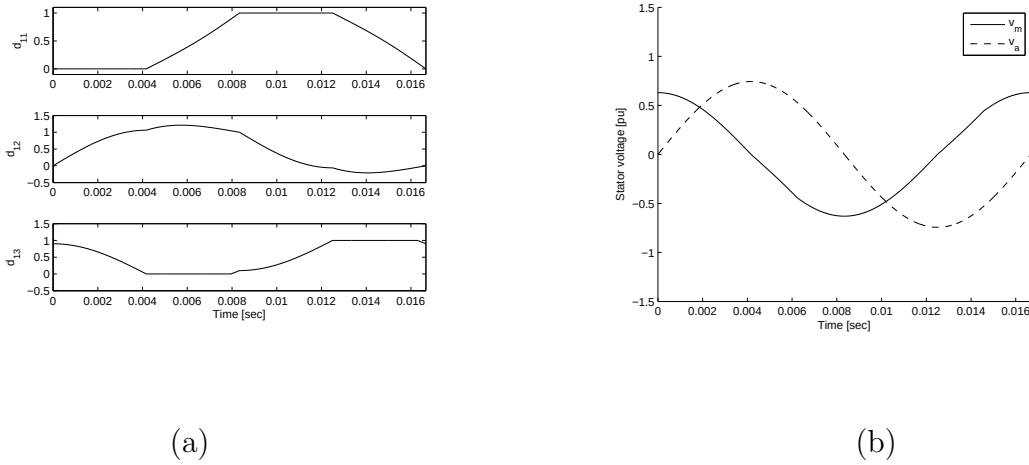


Figure 5.6 Representative waveforms for trapezoidal modulation obtained using simulations

$$\begin{aligned}
v_a &= v_{bus} (d_{12} - d_{11}) \\
v_m &= v_{bus} (d_{13} - d_{11})
\end{aligned} \tag{5.6}$$

### 5.2.2 Harmonic Distortion of Neutral-Voltage Trapezoidal Modulation

As general background, it is well documented [11, 3, 40, 20] that in order to eliminate the pulsating torque in PSC motors, the currents need to be balanced. It is also documented that this balance point will not result in the best operating efficiency [7]. In applying a variable speed drive to a PSC motor, a trade-off decision needs to be made to balance motor torque ripple and operating efficiency. This decision involves trade offs among operating efficiency, acoustic noise, and torque ripple.

In order to evaluate the distortion of neutral-voltage trapezoidal modulation, some observations of the PSC motor need to be made.

First, the impedances of the two machine windings are not symmetric. Often, the difference in impedance angles of the two windings is approximately 45 degrees. In such a case, the auxiliary voltage only needs to lead the main voltage by 45 degrees to set the machine currents at quadrature.

Second, the inverter topology naturally favors voltage angles of 45 degrees. If the auxiliary voltage leads the main voltage by 45 degrees, the 1X-3LEG topology can output  $v_a = \sqrt{2}v_m$  without any boost in the dc bus voltage.

Third, the closer the phase angle between voltages gets to zero, the better the waveform quality becomes. In the limiting cases, there is no distortion when the phase angle is zero, and there is maximum distortion when the phase angle is 90 degrees. At 90 degrees, the maximum rms voltage magnitude this topology can output without distorting the auxiliary voltage is  $1/2v_{bus}$ .

Fourth, in order to achieve the best efficiency possible, the mmf ratio should be less than the value set by balanced operation,  $|v_m| = a|v_a|$  [7]. The best motor efficiency occurs when the mmf ratio is between the high value common to line operation, and the low value set by balanced operation. As the mmf ratio is increased from balanced operation, the efficiency

improves, the required voltage by the auxiliary winding reduces, and the required boost in dc bus voltage reduces.

Finally, it is observed that the best flux level to set in a PSC motor is about 90% of rated flux [7]. This observation is intuitively consistent with the physical operation of the motor in its applications, since the motor must support its rated load torque at reduced voltage.

To compare the two modulation strategies, an auxiliary voltage is selected that sets the machine flux level to 90% of rated V/Hz, an optimum mmf ratio, and a current angle of 90 degrees. The comparison metrics for the modulation strategies are: 1) THD (i.e., waveform quality), and 2) amount of boost required to achieve 0 THD. The machine turns ratio is set at 1.18, a common turns ratio used in 240V PSC machines, and the auxiliary voltage angle are varied in this study.

Table 5.1 Summary of simulation parameters

| quantity    | value                       | quantity                          | value                            |
|-------------|-----------------------------|-----------------------------------|----------------------------------|
| $\vec{v}_m$ | $0.82\angle 57^\circ$ [pu]  | $\frac{1}{a} \frac{ i_m }{ i_a }$ | 1.5                              |
| $\vec{v}_a$ | $0.91\angle 144^\circ$ [pu] | $s$                               | 0.04                             |
| $\vec{i}_m$ | $1.57\angle 0^\circ$ [pu]   | $z_m$                             | $18\angle 56^\circ$ [ $\Omega$ ] |
| $\vec{i}_a$ | $0.89\angle 90^\circ$ [pu]  | $z_a$                             | $25\angle 49^\circ$ [ $\Omega$ ] |

The particular operating point for a 3/4 hp PSC induction motor is summarized in table 5.1. At this point, the duty cycle commands to the 1X-3LEG topology are summarized in Figure 5.6.

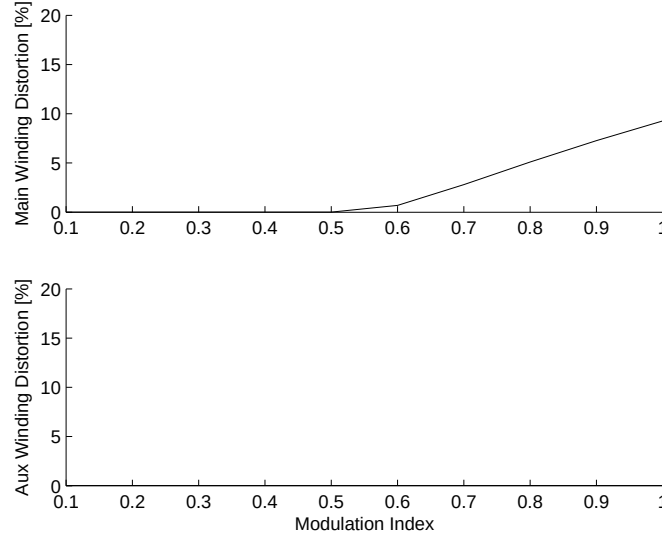


Figure 5.7 Comparison of distortion due to low frequency components in the main and auxiliary winding voltages for trapezoidal modulation

$$HD = \frac{|v_1|}{\sqrt{\sum_{k \neq 1}^{50} |v_k|^2}} \quad [5.7]$$

To compare the waveform quality, the metric of harmonic distortion given in 5.7. Since this analysis is used to compare the duty-cycle-ratio properties, the switching effects are not included.

To evaluate the waveform quality for trapezoidal modulation, the commanded voltages are set to 90 degrees phase difference and the magnitudes such that  $v_a = 1.18 \cdot v_m$ . Given the discussion above, this should represent the worst case evaluation of harmonic distortion for the modulation strategy. As shown in Figure 5.7, the HD metric is greater than zero for modulation indices greater than 0.6.

### 5.3 Consequences of Modulation Strategy on Capacitor Voltage Regulation

In chapter 3, the concept of a firing window was introduced to discuss the limits of boost capacitor voltage regulation under the assumption of sinusoidal voltage and sinusoidal current. However, as shown in the previous section, the pole current is controlled to be sinusoidal (since it is the same as one of the two motor currents), but the pole voltages  $v_{p2}$  and  $v_{p3}$  are significantly distorted. The result of this is that the firing window tends to be larger for trapezoidal modulation than it would be for sinusoidal modulation. On the other hand, sinusoidal modulation severely limits the voltage capability of the inverter to  $0.5 v_{bus}$ .

The firing window is defined to be the percentage of the fundamental cycle that the boost function depletes charge from the boost capacitor. This width depends strongly on the phase angle between the main- and auxiliary-winding current, and the asymmetry ratio between the main- and auxiliary-winding voltage. When operating a specific motor, the asymmetry ratio ( $a$ ) is fixed, and the phase angle is manipulated to constrain currents in quadrature, but will move as the operating point (speed and load) of the motor changes. The effect of the firing window as a function of voltage phase angle for trapezoidal modulation and a motor with a turns ratio of  $a = 1.18$  is shown in Figure 5.8. This shows that for a voltage phase angle of 60 degrees and higher that the firing window takes up 20% of the fundamental cycle, and that for a voltage phase angle of less than 60 degrees, the firing window takes up less than 10% of the fundamental cycle. The discontinuity at 60 degrees has to do with the differences in boundaries that are present in the voltage capability hexagon in the phase plane.

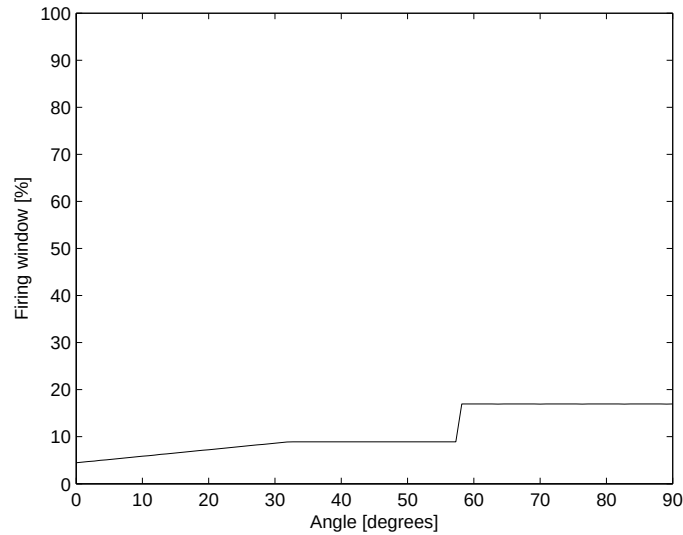


Figure 5.8 Comparison of phase angle between main- and auxiliary-winding voltage to firing window for the trapezoidal modulation strategy and a modulation index of 1.0

## 5.4 Summary

This chapter developed the switching strategy for the buck-boost inverter leg. With appropriate modulation and control, the buck-boost inverter leg decouples capacitor voltage regulation from boost voltage generation.

Two methods of three-leg inverter modulation were developed and compared. Based on the distortion metric that was developed, the trapezoidal modulation strategy was selected for this research.

Finally, the impact on the selection of modulation strategy on the feasibility of boost regulation was summarized. The latent benefit of trapezoidal modulation was identified.

## Chapter 6

### Dynamic Modeling and Control for the Three-Leg Inverter

Chapter 3 introduced the buck-boost inverter model and PSC machine model, and chapter 5 developed modulation strategies needed in order to realize a switching converter. In order to control the buck-boost controller's capacitor voltage, a controller needs to be developed that can regulate the boost capacitor voltage while simultaneously controlling the PSC motor current.

This chapter develops a control strategy to control the motor currents and the boost-capacitor voltage. Since the developed models are nonlinear, operating-point models need to be developed in order to develop a linear control strategy to the problem. A control strategy is then selected, controller gains are chosen, and the system is prepared for simulation.

Finally, the impact of the selected control strategy of large quantities of these machines connected to the utility supply is discussed. A strategy for managing the power drawn from the grid by a large network of variable-speed PSC motors is presented. The response of such a network of controllers to a sag in utility voltage is presented.

#### 6.1 Operating Point Model of the Converter

In order to develop a linear control strategy, an operating-point model of the plant needs to be developed. With the nonlinear converter model established and expressed in standard form, developing the operating-point model of the plant is a straight-forward procedure.

The nonlinear dynamic model for the converter is given in (6.1). This nonlinear model now includes as the pole series inductance the machine leakage inductance. The machine back-emf is assumed to be decoupled from the applied voltage, and neglected for the purpose of converter dynamic analysis. The operating-point model of the converter is obtained by taking partial derivatives of the nonlinear converter model, and is given in (6.3).

$$\frac{d}{dt} \begin{bmatrix} \sigma L_{sa} i_{p2} \\ C v_c \\ \sigma L_{sm} i_{p3} \end{bmatrix} = \begin{bmatrix} -R'_{1a} & -(1 - d_{12} - d_{32}) & 0 \\ (1 - d_{12} - d_{32}) & 0 & 0 \\ 0 & 0 & -R'_{1m} \end{bmatrix} \begin{bmatrix} i_{p2} \\ v_c \\ i_{p3} \end{bmatrix} \quad [6.1]$$

$$+ \begin{bmatrix} (d_{12} - d_{11}) \\ 0 \\ (d_{13} - d_{11}) \end{bmatrix} [v_{dc}] \quad [6.2]$$

$$\begin{aligned} \frac{d}{dt} \begin{bmatrix} \sigma L_{sa} \tilde{i}_{p2} \\ C \tilde{v}_c \\ \sigma L_{sm} \tilde{i}_{p3} \end{bmatrix} &= \begin{bmatrix} -R'_{1a} & -(1 - D_{12} - D_{32}) & 0 \\ (1 - D_{12} - D_{32}) & 0 & 0 \\ 0 & 0 & -R'_{1m} \end{bmatrix} \begin{bmatrix} \tilde{i}_{p2} \\ \tilde{v}_c \\ \tilde{i}_{p3} \end{bmatrix} \\ &+ \begin{bmatrix} (D_{12} - D_{11}) & -V_{bus} & (V_{bus} + V_c) & V_c & 0 \\ 0 & 0 & -I_{p2} & -I_{p2} & 0 \\ (D_{13} - D_{11}) & -V_{bus} & 0 & 0 & V_{bus} \end{bmatrix} \begin{bmatrix} \tilde{v}_{bus} \\ \tilde{d}_{12} \\ \tilde{d}_{11} \\ \tilde{d}_{32} \\ \tilde{d}_{13} \end{bmatrix} \quad [6.3] \end{aligned}$$

All the system variables except for  $v_c$  are large signal ac quantities and the control input for the system is the duty ratio  $d_{12} - d_{32}$ . In modeling such systems it is common to apply reference frame transformations to represent the system in the d-q coordinates. However, in this case, the reference frame theory cannot simultaneously eliminate the time dependence of all the motor impedances in the asymmetric motor[15] the machine quantities are ac quantities, and therefore the quantities  $I_{p2}$ ,  $I_{p3}$ ,  $\tilde{i}_{p2}$ , and  $\tilde{i}_{p3}$  reflect ac quantities at the

fundamental output frequency. Furthermore, the controller transfer function of interest is the relationship between the capacitor voltage and the duty ratio  $d_{12} - d_{32}$ . Therefore, the linearized model is used to develop the frequency response of the control transfer function at a range of operating conditions and a representative nominal operating point may be represented by the rms value of the pole current waveform etc. The resulting control transfer function may be used to design an appropriate voltage regulator.

To study the dynamics of the operating-point model, two scenarios are studied: buck mode and boost mode. For buck mode, the operating point of the boost duty cycle is set to be the complement of the buck duty cycle. This models the operation of entirely operating in buck mode. For boost mode, the operating point of the boost duty cycle is set by the constraints previously established and replicated in (6.4) with  $i_c^* = 0$  [pu].

$$\begin{aligned} -\frac{\frac{v_{p2}}{v_{bus}}}{\frac{v_c}{v_{bus}}} &\leq \frac{i_c^*}{i_{p2}} \leq \frac{1 - \frac{v_{p2}}{v_{bus}}}{\frac{v_c}{v_{bus}}} \\ \frac{\frac{v_{p2}}{v_{bus}}}{1 + \frac{v_c}{v_{bus}}} &\leq \frac{i_c^*}{i_{p2}} \leq \frac{-1 + \frac{v_{p2}}{v_{bus}}}{1 + \frac{v_c}{v_{bus}}} \end{aligned} \quad [6.4]$$

Using these constraints, the transfer function  $\tilde{v}_c = f(\tilde{h}_{12}, \tilde{h}_{32}, H_{12})$  can be studied in only three dimensions for the buck mode, boost mode, and for the response variables  $\tilde{v}_c/\tilde{d}_{12}$  and  $\tilde{v}_c/\tilde{d}_{32}$ . The buck- and boost-modes are shown in three dimensions for  $\tilde{v}_c/h_{12}$  in Figure 6.1. During buck mode, there is no energy being exchanged, so it should not be surprising that the phase response is flat. During boost mode, energy is exchanged, and the duty-cycle ratio is limited by the constraint in (6.4), so the phase response is not well damped, and a resonance is observed near the limits.

The three-dimensional plot obscures the details of the frequency response, but it helps to identify worst-case regions of the response map. For completeness, the frequency response function for nominal values of  $D_{12}$ ,  $D_{32}$ , and  $I_{p2}$  is plotted in Figure 6.2. These frequency-response functions suggest a PI controller to provide stiff dc control and to provide attenuation at higher frequencies. However, the controller needs to regulate dc voltage with a fast

response as the controller switches between buck mode and boost mode twice per fundamental output cycle. As a result of these competing requirements, a P-controller is selected to control capacitor voltage. The selection of the specific voltage regulator gain is iteratively selected based on the saturation of the controller signal, and can be automatically done online, if desired.

The dynamics of the power converter are largely governed by the quantity  $(1 - d_{12} - d_{32})$ . This quantity is usually small during buck mode, but may get close to 1 during boost mode. The result of these attributes is that the dynamic contributions of  $d_{12}$  on  $v_c$  tend to cancel out the dynamic contributions of  $d_{32}$  on  $v_c$ .

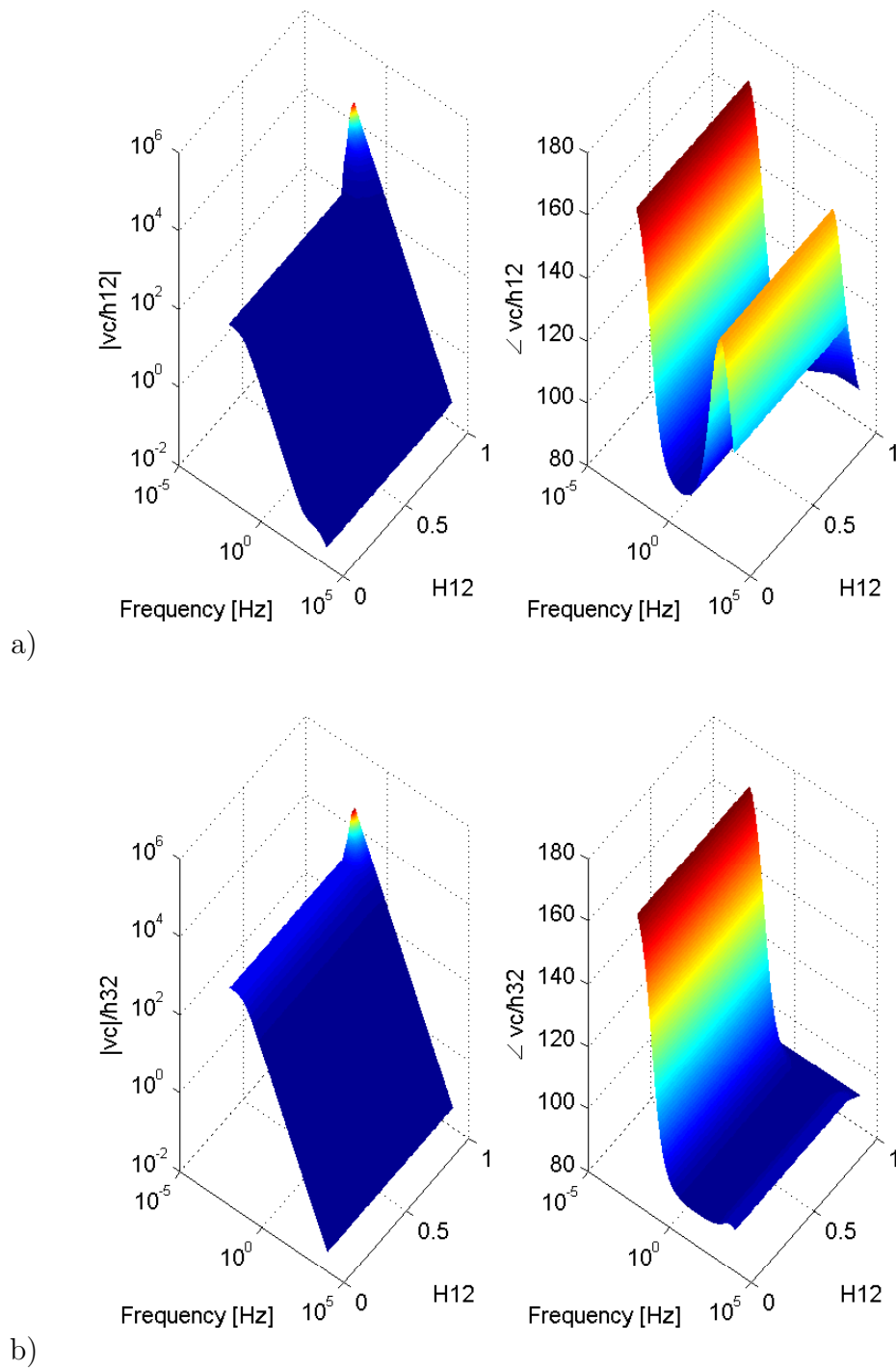


Figure 6.1 Frequency response functions for  $\tilde{v}_c/\tilde{d}_{12}$  and  $\tilde{v}_c/\tilde{d}_{32}$  in a) buck mode and b) boost mode

The closed-form expression for the MISO capacitor voltage transfer function is given in (6.5).

$$\begin{aligned} \tilde{v}_c = & - \frac{[(R'_{sa} + s \sigma L_{sa}) I_{p2} + (V_{bus} - V_c) (D_{12} + D_{32} - 1)] \tilde{d}_{12}}{s^2 C \sigma L_{sa} + s C R'_{sa} + (D_{12} + D_{32} - 1)^2} \\ & - \frac{[I_{p2} (R'_{sa} + s \sigma L_{sa}) + V_c (D_{12} + D_{32} - 1)] \tilde{d}_{32}}{s^2 C \sigma L_{sa} + s C R'_{sa} + (D_{12} + D_{32} - 1)^2} \end{aligned} \quad [6.5]$$

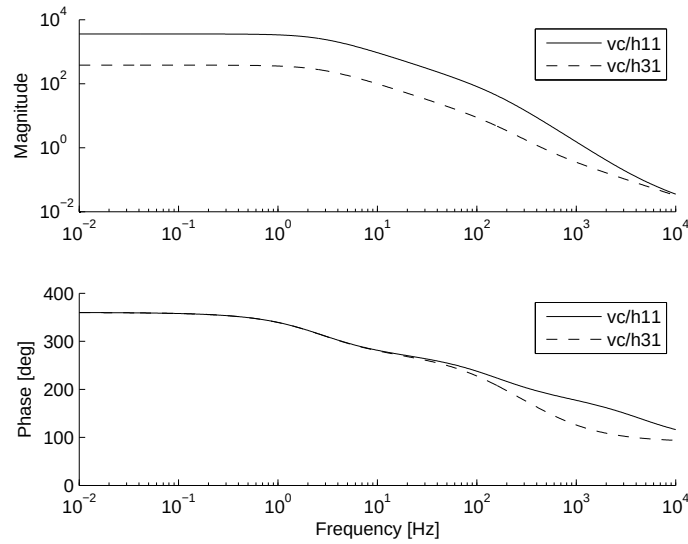


Figure 6.2 Frequency response for the transfer function  $\tilde{v}_c/\tilde{d}_{12}$  and  $\tilde{v}_c/\tilde{d}_{32}$ . The following operating point quantities are chosen:  $D_{12} = 0.5$ ,  $D_{32} = 0.4$ ,  $I_{p2} = 2.0$ .

The performance of this controller will be demonstrated after the rest of the controlled system has been developed. This subsection has developed the operating-point model of the buck-boost inverter leg, which is required to design a linear controller. The worst-case operating points have been identified, and the control gains should be selected to satisfy stability constraints for these worst-case operating points.

### 6.1.1 Capacitor Voltage Regulation

The control task of the capacitor voltage regulator is to use the buck-boost leg's pole current (which is either the machine's main-winding current or the auxiliary-winding current) to

maintain the boost capacitor voltage. As developed previously, this can only be done under a limited range of buck-boost leg power factor and firing window. If the power factor is too close to unity and the firing window is too wide, there is not enough time for the controller to balance charge on the capacitor.

Unfortunately, this requires the controller to switch between two linear control laws: the first to regulate the voltage during buck (normal) mode, and the second to transfer charge from the capacitor to the motor during boost mode. The stability of this approach is very difficult to prove in general, but the control law can restrict the general case to a continuous transition between the two modes through the use of the constraints developed previously in (3.13).

It is possible for this to result in an unsustainable voltage condition, though this should be unlikely for most practical connections to a PSC motor's auxiliary winding with modest voltage boost, as discussed previously. If this occurs, a limit may be imposed on the output current reference so that the capacitor voltage does not deplete. If the capacitor voltage depletes too severely, the constraints developed in (3.13) may result in an unstable operating point, due to the normalization of  $v_c$ . The result of this limit action is usually an increase in waveform quality distortion.

If the buck-boost inverter controller operation results in stable capacitor voltage regulation, the resulting topology provides the capability of exceeding the bus voltage by approximately  $1.4 v_{bus}$ , which is enough to provide balanced excitation of the auxiliary winding.

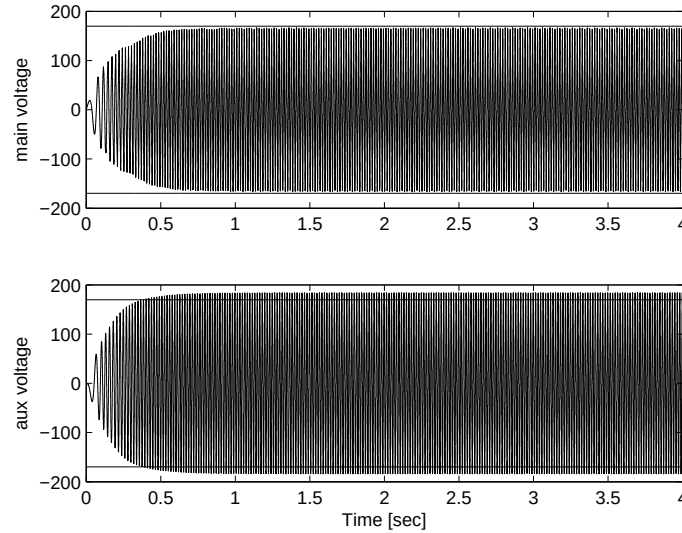


Figure 6.3 Start up voltage waveforms illustrating the operation of the buck-boost inverter exceeding  $v_{bus}$  on the auxiliary winding.

The operation of the buck-boost inverter operating a PSC induction motor is shown in Figure 6.3. The reference voltage on the main winding is limited in bandwidth, and therefore comes up to rated voltage at about 0.5 seconds. The angle controller's bandwidth is set to about 1 Hz, and the auxiliary winding syncs up and the voltage magnitude achieves steady state at around 1.5 seconds. The dc bus limit is drawn in a solid horizontal line, and the buck-boost inverter's ability to boost the winding voltage beyond the dc bus voltage is clearly visible as the auxiliary voltage exceeds the dc bus voltage during each half cycle.

A secondary attribute visible in this plot is that the winding boost voltage is usually less than the turns ratio would indicate. In this example, the turns ratio is 1.18, yet the boost required to balance the machine mmf is only about 1.12. When the machine equations are transformed to eliminate the rotor asymmetry, there still exists asymmetry in the stator leakage and stator resistance, which in this case limits the boost required by the auxiliary winding.

This section has presented the primary trade offs in selecting a control algorithm for the buck-boost inverter leg, and has demonstrated with dynamic simulation that the inverter leg can realize the required boost function needed by the PSC motor.

## 6.2 HVAC Dynamics and Motor Control

Before discussing motor control, a brief summary of HVAC dynamics is needed. The basic HVAC cycle consists of extracting heat from the cooling environment, compressing the fluid, moving the heated, compressed, fluid to a heat exchanger, returning heat to the outside air, and expanding the fluid to restart the cycle, as illustrated in Figure 6.4. Although this process is not linear, the effective time constants in this system are often bounded by times of 1 minute to 1 hour, depending on the system under control.

The most common application of PSC motors in this cycle are water pumps (for component cooling), oil pumps (for component lubrication and component cooling), and fan motors (for component cooling and for heat exchangers). None of these applications require torque control to respond faster than the rotor short circuit time constant, so any motor control strategy will meet the application performance requirements. Since this research focuses on the problem of developing a power electronic converter that can deliver the appropriate excitation to the machine, and because the application does not require high-performance torque control, a simple machine controller is acceptable.

This section develops the control strategy used in this research. With the control strategy developed, it uses nonlinear programming to demonstrate the optimal machine efficiency possible and compare it to the proposed control strategy.

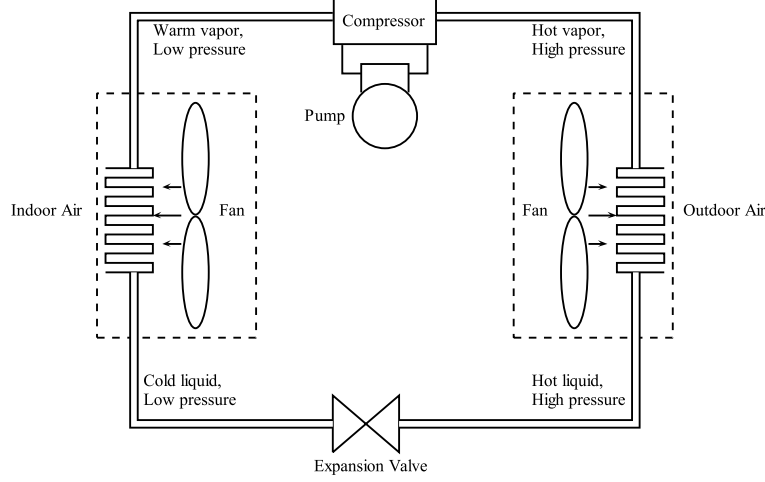


Figure 6.4 Diagram showing the HVAC cycle

### 6.2.1 Proposed Approach to Control Stator Current

The PSC induction motor equations shown in (6.6) suggest that for constant speed, there should exist a given fixed-frequency excitation that will result in orthogonal currents at only that frequency. This approach was taken early in the development of PSC modeling by Morrill [11].

$$\begin{aligned}
 \frac{p}{\omega_b} i_{ds}^s &= \frac{1}{\sigma L_{sm}} \left( v_{ds}^s - r'_{sm} i_{ds}^s + \frac{x_{mm}}{x_{rm}} \frac{r_{rm}}{x_{rm}} \psi_{dr}^s + \frac{N_m}{N_a} \frac{x_{mm}}{x_{rm}} \frac{\omega_r}{\omega_b} \psi_{qr}^s \right) \\
 \frac{p}{\omega_b} i_{qs}^s &= \frac{1}{\sigma L_{sa}} \left( v_{qs}^s - r'_{sa} i_{qs}^s + \frac{x_{ma}}{x_{ra}} \frac{r_{ra}}{x_{ra}} \psi_{qr}^s - \frac{N_a}{N_m} \frac{x_{ma}}{x_{ra}} \frac{\omega_r}{\omega_b} \psi_{dr}^s \right) \\
 p \psi_{dr}^s &= \frac{x_{mm}}{x_{rm}} r_{rm} i_{ds}^s - \frac{N_m}{N_a} \frac{r_{rm}}{x_{rm}} \frac{\omega_r}{\omega_b} \psi_{qr}^s + \frac{r_{rm}}{x_{rm}} \frac{\omega_r}{\omega_b} \psi_{dr}^s \\
 p \psi_{qr}^s &= \frac{x_{ma}}{x_{ra}} r_{ra} i_{qs}^s + \frac{N_a}{N_m} \frac{r_{ra}}{x_{ra}} \frac{\omega_r}{\omega_b} \psi_{dr}^s + \frac{r_{ra}}{x_{ra}} \frac{\omega_r}{\omega_b} \psi_{qr}^s \\
 T_e &= \frac{x_{mm}}{x_{rm}} \frac{1}{\omega_b} \left( \frac{N_a}{N_m} \psi_{dr}^s i_{qs}^s - \frac{N_m}{N_a} \psi_{qr}^s i_{ds}^s \right)
 \end{aligned} \tag{6.6}$$

It should therefore be possible to, at least on a steady-state basis, formulate a controller that excites the main winding with line voltage and manipulates the voltage across the auxiliary winding to constrain the phase angle between the currents to be 90 degrees and the

magnitudes to balance the MMF. This approach cannot be used to control current with a bandwidth higher than about 1 Hz, but this is sufficient to control HVAC applications. For this class of application, the performance restriction is not as bad as it might appear. For example, compressor applications require high starting torque, but they do not require fast dynamic response. The high-bandwidth controller would be necessary if the application needed to cancel torque vibrations [41], or if the application wanted to detect spatial harmonic signatures [42]. These effects are rarely important to existing application of PSC motors, but could become important in the future.

The current controller used in this research achieves steady-state current control by computing phase and magnitude information for each of the machine's currents. Since imbalance can easily occur using this approach, a three-phase PLL approach cannot be used. Instead, the commanded excitation frequency is used in combination with the measured current to lock on to the fundamental of the known excitation frequency. The currents are then normalized, and the two currents are multiplied. The result, given in (6.7), shows that this product consists of two terms: 1) a signal that is proportional to the angle when the angle is small, and 2) a signal that contains a high-frequency term. When the high-frequency term is filtered from the piece of the signal that contains the angle information, an angle error term is left.

$$\begin{aligned}
 i_m \cos(\omega t) \cdot ai_a \cos(\omega t - \phi_a) &= \frac{1}{2} i_m ai_a \cos[\omega t - (\omega t - \phi_a)] + \frac{1}{2} i_m ai_a \cos[\omega t + \omega t - \phi_a] \\
 &= \frac{1}{2} i_m ai_a \cos(\phi_a) + \frac{1}{2} i_m ai_a \cos(2\omega t - \phi_a) \quad [6.7]
 \end{aligned}$$

The steady-state current controller is shown in Figure 6.5. The voltage command generator uses the flux trajectory and optionally compensates for utility voltage sags. The phase regulator and magnitude controller use the outputs of each PLL block to normalized the current signals and to compute the phase error and the current magnitude. A PI controller is then formed to control the magnitude and phase of the current signal. The winding voltage commands are then generated by an incrementing angle.

The modulator uses the winding voltage commands and the trapezoidal modulation strategy to generate the three pole voltage commands. The limits to winding-voltage commands and to pole-voltage commands are listed in Table 6.1. The boost voltage is allowed to exceed the duty cycle limits by 0.5.

The boost controller accepts a boost voltage command from  $-0.5$  to  $1.5$  and manages the boost capacitor to achieve the commanded voltage. This is done to deliver the voltage below 0 and above 1 that the trapezoidal modulator commands. As a result, the power converter's voltage capability for the auxiliary winding is extended.

The power converter consists of power semiconductors and sensing circuits. The voltage across the boost capacitor is fed back to the boost controller, and the dc link voltage is fed back to the voltage command generator. The machine currents are fed back to the phase and magnitude controllers.

Table 6.1 Limits on winding and pole voltage commands

| Quantity   | Lower Limit        | Upper Limit       |
|------------|--------------------|-------------------|
| $v_m^*$    | $-1$               | $1$               |
| $v_a^*$    | $-\frac{N_a}{N_m}$ | $\frac{N_a}{N_m}$ |
| $v_{p1}^*$ | $0.0$              | $1.0$             |
| $v_{p2}^*$ | $-0.5$             | $1.5$             |
| $v_{p3}^*$ | $0.0$              | $1.0$             |

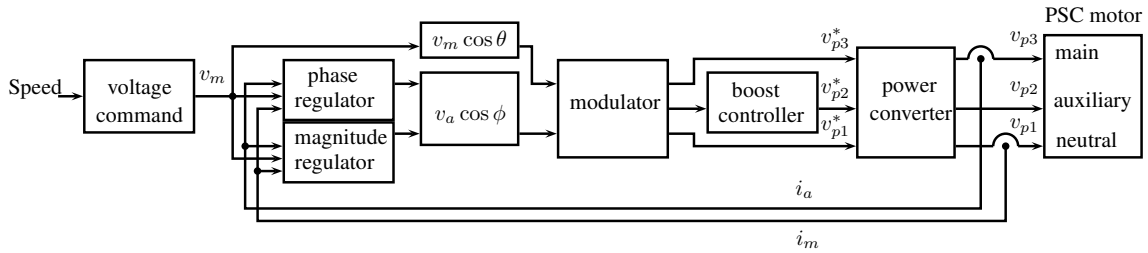


Figure 6.5 Block diagram for the steady-state current controller

The response of this controller is a steady-state controller that is able to maintain currents in quadrature with a bandwidth of about 1 Hz, which is sufficient for present application of PSC motors in HVAC applications.

### 6.2.2 Optimal Efficiency Control

The efficiency of a PSC motor was optimized for fixed speed generic applications in [7]. This solution used off-line tuning for the controller and could handle most load types. The general case for variable speed introduces another degree of freedom that significantly adds to the solution complexity.

To explore this problem, nonlinear programming was used to solve the constrained problem of a PSC induction motor operating against a fan load with a simple model of magnetic saturation, using the saturation model in [19]. The currents were constrained to be in quadrature, and the voltages were manipulated at each operating point to optimize efficiency. The result is a variable slip frequency and mmf ratio that result in optimal efficiency for all operating points, assuming a fan load. The voltage variation, mmf ratio, and efficiency are plotted in Figure 6.6.

The voltage variation indicates that since the machine flux level is set optimally, the machine does not saturate until the load demands it. The optimal voltage variation therefore departs from the  $(V/Hz)^2$  curve at the saturation point, about 3/4 base speed. The mmf ratio variation closely follows that results from Mademlis, who states in [7] that the optimal mmf ratio will deviate slightly from the balance point. Furthermore, it should be intuitive that the optimal efficiency should be somewhere between the balance point and the fixed capacitor operating point, since capacitor operation results in very little current being conducted by the auxiliary winding.

Finally, the efficiency curve is interesting. First, the optimal efficiency is bounded by the resistance of the machine. The performance curves of the inverter-operated PSC induction machine closely represent those of a highly resistive three-phase machine. The resistance

falls off relatively rapidly as the excitation speed reduces. On the other hand, the torque capability and motor efficiency are both dramatically improved over capacitor line operation. The bulk efficiency improvement comes from inverter operation and operating close to the balance point of the machine. Further improvements can be made by trading off the effects of torque pulsations inherent to increasing the mmf ratio for its improved efficiency. Finally, it is theoretically possible that real-time optimization of losses could achieve some efficiency result, but it is not clear that this will be significant, due to the asymmetric and nonlinear impedance that prevents direct application of vector control to this class of motor.

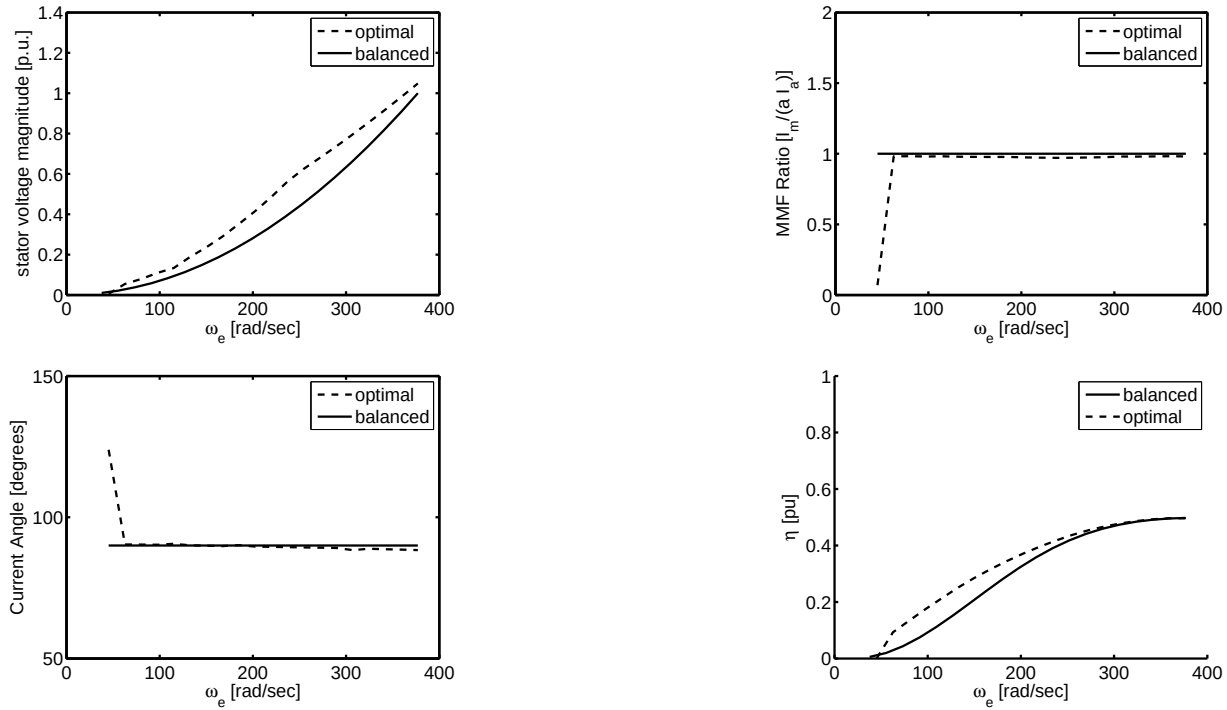


Figure 6.6 Comparison of optimal vs. proposed voltage, mmf ratio, and resulting efficiency

The proposed mode of operating the PSC motor, shown in Figure 6.6, is to constrain the machine flux according to the  $(V/Hz)^2$  curve, underfluxing the machine to about 90% of rated flux at rated speed. The result is the ability to meet the machine rating point and maintain good efficiency across the entire operating range.

Achieving an online optimization of efficiency may be possible, but it is not likely that the HVAC market could sustain the cost of a real-time microprocessor to implement its algorithm. Field orientation could be used, but its implementation is nontrivial in a PSC machine due to the reasons listed previously.

### 6.3 Utility Connection and Utility-VFD Dynamics

Utility-connected PSC motors applied to air-conditioner compressor loads result in stalls under voltage sag conditions[43, 44, 19]. When high-performance VFD's are connected to the utility, they act as constant-power loads to the utility and exacerbate grid stability problems. Because of the large number of installed PSC motors in HVAC applications, it is desirable to control the VFD so that it behaves as a constant current load to the utility. By doing this, even if the VFD-operated PSC motors locally dominate the utility dynamics, the utility will be able to supply the load in a stable manner, as developed further.

The inverter current, bus voltage, pole voltages, and pole currents are related as shown in (6.8). The motor output power is defined by the product of the rotor speed and the electromagnetic torque. Power balance is applied to balance the inverter power and the output power. For this analysis, motor losses are neglected. The inverter power is therefore equated to motor output power in (6.9).

$$\begin{aligned}
 v_{p1} &= (1 - h_{11}) v_{dc} \\
 v_{p2} &= (1 - h_{12}) v_{dc} \\
 v_{p3} &= (1 - h_{13}) v_{dc} \\
 i_{inv} &= h_{11} i_{p1} + h_{12} i_{p2} + h_{13} i_{p3}
 \end{aligned} \tag{6.8}$$

$$P_{out} = \omega_r T_e$$

$$= \omega_r \frac{2}{2} \frac{P}{2} \frac{x_m}{x_r} \left( \frac{N_a}{N_m} i_{qs}^s \psi_{dr}^s - \frac{N_m}{N_a} i_{ds}^s \psi_{qr}^s \right)$$

$$\begin{aligned} P_{inv} &= P_{out} \\ v_{dc} i_{inv} &= \omega_r \frac{2}{2} \frac{P}{2} \frac{x_m}{x_r} \left( \frac{N_a}{N_m} i_{qs}^s \psi_{dr}^s - \frac{N_m}{N_a} i_{ds}^s \psi_{qr}^s \right) \end{aligned} \quad [6.9]$$

Since machine rotor flux is assumed to be conserved (this result is arrived independently using the principle of virtual work and the principle of constant flux linkage), the only variables the inverter has to manipulate the motor power are excitation frequency and motor current. Based on this development, the control structure illustrated in Figure 6.5 will automatically result in a passive system with attractive grid stability characteristics. While this approach does not provide the capability to dynamically cancel process vibrations (for example, periodic pulsating torque in a compressor load), it satisfies the dynamic control requirements for fan and pump applications.

If traditional field orientation is to be applied to the PSC machine, the current regulator should be tuned so that the process needs are met and that the inverter-machine combination acts as a constant current load. This accomplishes the same utility interaction benefit described in this section. However, this tuning process is application dependent and in general is challenging to accomplish. If the current regulator is too responsive, it is easy for the inverter to appear to the utility as a constant power load. If the current regulator is too sluggish, the motor controller does not provide enough capability to control the load in a stable manner. As stated above, this research focuses on the development of the power electronics, and uses the steady-state current controller described above.

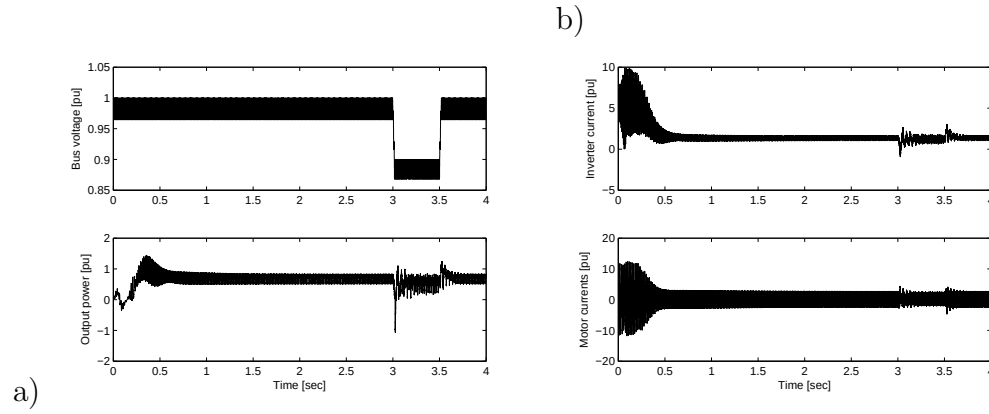


Figure 6.7 Simulation of voltage sag with constant V/Hz controller and sag follower controller

The utility sag simulation results are shown in Figure 6.7. The bus voltage, motor output power, inverter input current, and motor current are shown. As the bus voltage sag is detected, the controller reduces the output frequency, and, as shown above, the steady-state inverter input current stays constant. This approach presents a constant-current load to the utility, and presents a more grid-friendly load to the utility than traditional high-performance vector-control drives. If these controllers are installed in a large network of PSC machines, the grid should be more stable than with the line-operated motors.

During the sag event, the motor output power is reduced and the steady-state current drawn by the inverter remains constant. Due to the dc-bus sag, the modulation index increases, which results in a more distorted current waveform. When the dc bus voltage returns to normal, the inverter is able to return to the steady-state operating point prior to the voltage sag.

## 6.4 Summary

This chapter developed the operating-point model of the buck-boost converter and identified the controller to be used with the buck-boost inverter. The benefits and drawbacks to vector control of PSC motors was discussed, and the efficiency penalty of vector control was

identified. The proposed current controller was presented, and its efficiency characteristics were summarized. Finally, a utility sag compensator was presented, and simulation results demonstrated its operation.

The remaining chapters in this work demonstrate a simulated system of one PSC connected to a fan load and demonstrate the key elements of operation on prototype hardware.

## Chapter 7

# Simulation of the Proposed PSC Motor Drive

## 7.1 Simulation Models

In order to establish the feasibility of the proposed PSC motor drive system, various computer simulation models have been developed and used. A classification of these models into various categories is illustrated in Figure 7.1. All of these models represent the same machine, expressed in slightly different forms. Each form of the model has its advantages. For instance, the dynamic form enables the exploration of switching dynamics, torque transients, controller stability, and utility dynamics (of a small number of interconnected systems). While selected simulation results from these models have been presented in the previous chapters in the context of the discussion, a summary of the results from these simulations are presented in this chapter.

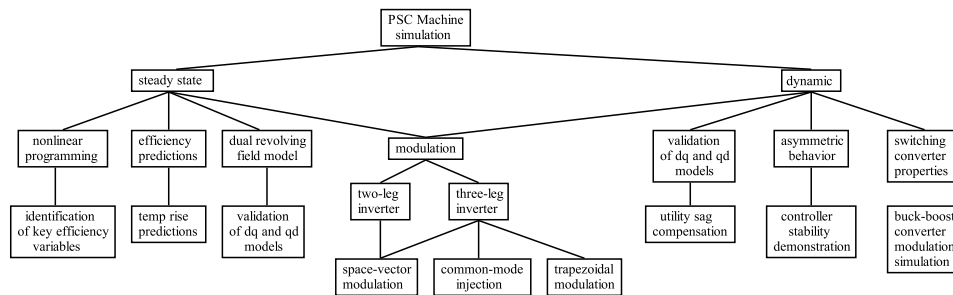


Figure 7.1 Types of simulation used in this research

### 7.1.1 dq- and qd- Models

Complex vector machine models in dq- and qd-coordinates are equally represented in the literature. Vector representation of the variables in the dq model is shown in (7.1), and the qd model is shown in (7.2). The complex vectors in these cases are expressed as:

$$f_{dq} = f_d + j \cdot f_q \quad [7.1]$$

$$f_{qd} = f_q - j \cdot f_d \quad [7.2]$$

The qd vector model is used to develop the machine model presented in [13] and [12]. The dq vector model is developed using a different approach in [14]. These models are expressed in stator flux voltage and rotor flux voltage. The simulation model used in this research selects stator current and rotor flux as state variables. This development is well documented, such as that performed in [36]. The dq machine model is presented in (7.3), the qd machine model is presented in (7.4), and the machine constants for both models is presented in (7.5). Each of these models have been simulated in different cases in order to verify conformance with the results from particular references as appropriate and model consistency has been verified.

$$\begin{aligned} p i_{ds}^s &= \frac{1}{\sigma_m L_{sm}} \left( v_{ds}^s - r'_{sm} i_{ds}^s + \frac{x_{mm} r_{rm}}{x_{rm} x_{rm}} \psi_{dr}^s + \frac{N_m x_{mm} \omega_r}{N_a x_{rm} \omega_b} \psi_{qr}^s \right) \\ p i_{qs}^s &= \frac{1}{\sigma_a L_{sa}} \left( v_{qs}^s - r'_{sa} i_{qs}^s - \frac{N_a x_{ma} \omega_r}{N_m x_{ra} \omega_b} \psi_{dr}^s + \frac{x_{ma} r_{ra}}{x_{ra} x_{ra}} \psi_{qr}^s \right) \\ \frac{p}{\omega_b} \psi_{dr}^s &= \frac{x_{mm} r_{rm}}{x_{rm}} i_{ds}^s - \frac{N_m \omega_r}{N_a \omega_b} \psi_{qr}^s - \frac{r_{rm}}{x_{rm}} \psi_{dr}^s \\ \frac{p}{\omega_b} \psi_{qr}^s &= \frac{x_{ma} r_{ra}}{x_{ra}} i_{qs}^s + \frac{N_a \omega_r}{N_m \omega_b} \psi_{dr}^s - \frac{r_{ra}}{x_{ra}} \psi_{qr}^s \\ T_e &= \frac{x_{mm}}{x_{rm} \omega_b} \frac{1}{\omega_b} \left( \frac{N_a}{N_m} \psi_{dr}^s i_{qs}^s - \frac{N_m}{N_a} \psi_{qr}^s i_{ds}^s \right) \end{aligned} \quad [7.3]$$

$$\begin{aligned}
pi_{qs}^s &= \frac{1}{\sigma_m L_{sm}} \left( v_{qs}^s - r_{sm}' i_{qs}^s + \frac{x_{mm}}{x_{rm}} \frac{r_{rm}}{x_{rm}} \psi_{qr}^s - \frac{N_m}{N_a} \frac{x_{mm}}{x_{rm}} \frac{\omega_r}{\omega_b} \psi_{dr}^s \right) \\
pi_{ds}^s &= \frac{1}{\sigma_a L_{sa}} \left( v_{ds}^s - r_{sa}' i_{ds}^s + \frac{N_a}{N_m} \frac{x_{ma}}{x_{ra}} \frac{\omega_r}{\omega_b} \psi_{qr}^s + \frac{x_{ma}}{x_{ra}} \frac{r_{ra}}{x_{ra}} \psi_{dr}^s \right) \\
\frac{p}{\omega_b} \psi_{qr}^s &= \frac{x_{mm}}{x_{rm}} r_{rm} i_{qs}^s + \frac{N_m}{N_a} \frac{\omega_r}{\omega_b} \psi_{dr}^s - \frac{r_{rm}}{x_{rm}} \psi_{qr}^s \\
\frac{p}{\omega_b} \psi_{dr}^s &= \frac{x_{ma}}{x_{ra}} r_{ra} i_{ds}^s - \frac{N_a}{N_m} \frac{\omega_r}{\omega_b} \psi_{qr}^s - \frac{r_{ra}}{x_{ra}} \psi_{dr}^s \\
T_e &= \frac{x_{mm}}{x_{rm}} \frac{1}{\omega_b} \left( \frac{N_a}{N_m} \psi_{qr}^s i_{ds}^s - \frac{N_m}{N_a} \psi_{dr}^s i_{qs}^s \right)
\end{aligned} \tag{7.4}$$

$$\begin{aligned}
x_{sm} &= x_{mm} + x_{lsm} \\
x_{sa} &= x_{ma} + x_{lsa} \\
x_{rm} &= x_{mm} + x_{lrm} \\
x_{ra} &= x_{ma} + x_{lra} \\
\sigma_m L_{sm} &= 1 - \frac{x_{mm}^2}{x_{sm} x_{rm}} \\
\sigma_a L_{sa} &= 1 - \frac{x_{ma}^2}{x_{sa} x_{ra}} \\
r_{sm}' &= r_{sm} + \left( \frac{x_{mm}}{x_{rm}} \right)^2 r_{rm} \\
r_{sa}' &= r_{sa} + \left( \frac{x_{ma}}{x_{ra}} \right)^2 r_{ra}
\end{aligned} \tag{7.5}$$

### 7.1.2 Expression of State-Space Models in Steady State

In order to express the dq- or the qd-models in the steady state, the  $p$  operator is replaced by  $j\omega_e$ , as presented in [12]. In this manner a numerically simple expression can be obtained for the state equations.

The resulting equations become the steady-state equations in (7.6).

$$\begin{aligned}
j\omega_e i_{ds}^s &= \frac{1}{\sigma_m L_{sm}} \left( v_{ds}^s - r'_{sm} i_{ds}^s + \frac{x_{mm} r_{rm}}{x_{rm} x_{rm}} \psi_{dr}^s + \frac{N_m x_{mm} \omega_r}{N_a x_{rm} \omega_b} \psi_{qr}^s \right) \\
j\omega_e i_{qs}^s &= \frac{1}{\sigma_a L_{sa}} \left( v_{qs}^s - r'_{sa} i_{qs}^s - \frac{N_a x_{ma} \omega_r}{N_m x_{ra} \omega_b} \psi_{dr}^s + \frac{x_{ma} r_{ra}}{x_{ra} x_{ra}} \psi_{qr}^s \right) \\
\frac{j\omega_e}{\omega_b} \psi_{dr}^s &= \frac{x_{mm} r_{rm}}{x_{rm}} i_{ds}^s - \frac{N_m \omega_r}{N_a \omega_b} \psi_{qr}^s - \frac{r_{rm}}{x_{rm}} \psi_{dr}^s \\
\frac{j\omega_e}{\omega_b} \psi_{qr}^s &= \frac{x_{ma} r_{ra}}{x_{ra}} i_{qs}^s + \frac{N_a \omega_r}{N_m \omega_b} \psi_{dr}^s - \frac{r_{ra}}{x_{ra}} \psi_{qr}^s \\
T_e &= \frac{x_{mm}}{x_{rm} \omega_b} \frac{1}{\omega_b} \left( \frac{N_a}{N_m} \psi_{dr}^s i_{qs}^s - \frac{N_m}{N_a} \psi_{qr}^s i_{ds}^s \right)
\end{aligned} \tag{7.6}$$

Even if the full dynamics of the model are retained (compared to the model developed in [19]), this steady-state model results in considerably faster analytical results than the full dynamic model presented above. The steady-state form enables the rapid predication of average and pulsating torque, predicted efficiency, efficiency optimization, and fundamental-frequency modulation trade offs.

### 7.1.3 Nonlinear Programming and Identification of Key Efficiency Variables

The operation of a variable-frequency drive connected to a PSC motor has a number of degrees of freedom than indicated by the number of manipulated inputs. In order to determine which control variables most affect motor efficiency, the nonlinear programming method presented in [45] and implemented by the MATLAB function `fmincon` in the optimization toolbox is used to determine the optimal operating points of a variable-frequency controlled PSC motor operating against a fan load. In order to do this, the operating point (speed and slip) is constrained, and the electrical operating point that results in the maximum efficiency is determined. To inspect convergence, plots of the convergence factors were plotted across all input variables. This method identified that the motor efficiency is sensitive to current phase angle, and that operating with current phase angle different from 90 degrees causes a reduction in motor efficiency.

The analysis identifies that key efficiency variables include: 1) stator mmf ratio, and 2) machine flux level. These are equivalent to the observations made about fixed-frequency optimizations by Mademlis et al. in [7].

The results from the analysis predicts that PSC motor efficiency improves with a slight reduction in machine flux level (or operating voltage). A particular PSC motor may run with a rated slip of 12% with a stator voltage of 120 VAC/60 Hz under line operation with a PSC. However, under inverter operation this motor could run with a slip of 4%. This means that the inverter can operate the motor at 55 Hz and obtain the same operating point. With this reduced frequency and the optimal flux level in this machine, the inverter could operate at 100 VAC for optimal efficiency. This operating point corresponds to a modulation index of 0.83, and is very favorable for the three-terminal VFD capability hexagon (see Figure 7.2). Thus, the operating slip under variable frequency is lower than that of line operation, which has a positive implication for the case of the reduced voltage dc bus inverter. These effects become particularly manifest because practical machine designs are constrained to meet a given torque specification even when the voltage drops below nominal values, say,  $-20\%$ .

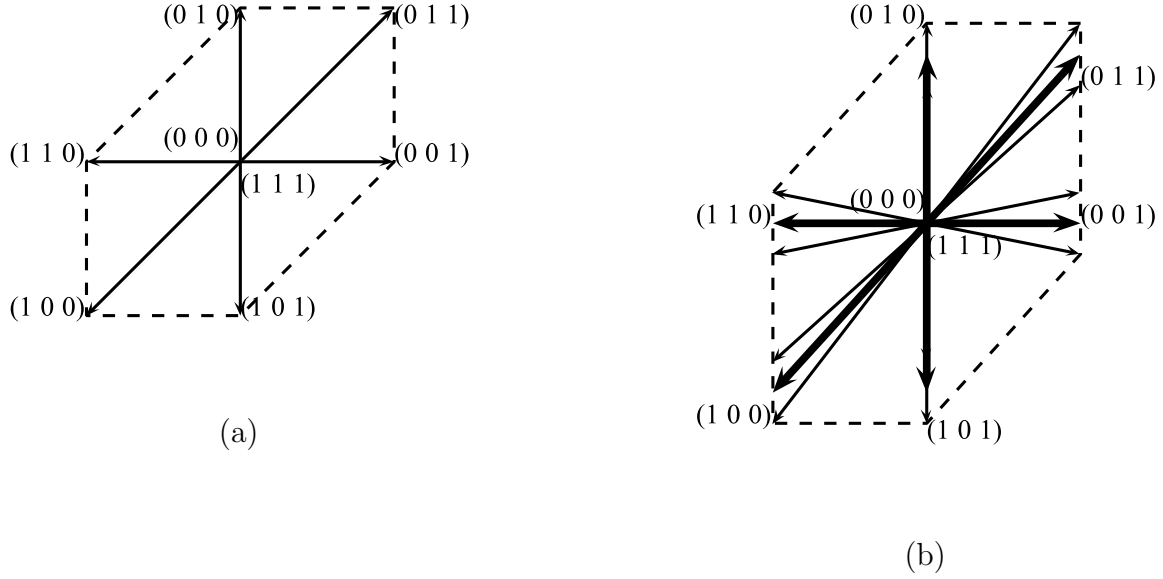


Figure 7.2 Voltage capability hexagon for the three-terminal variable-frequency drive a) without boost, b) with boost. The principle voltage vectors in the boost configuration are shown with thick arrows.

The influence of auxiliary winding to main winding mmf ratio on efficiency is significant, also in agreement with the analysis Mademlis in [7]. It is widely believed that the ideal operating point for a PSC motor is that of balanced excitation [11, 24, 4]. The balance point is the condition where the machine mmf's caused by excitation of the two windings are equal in magnitude and phase shifted by 90 degrees. This means the currents are unbalanced by the ratio of the two magnetizing reactances. The mmf ratio is defined as the ratio of currents normalized by the turns ratio,  $a$ , and is given in (7.7). For balanced operation, this quantity is unity. As this quantity increases, the motor's operation approaches that of line operation with a capacitor installed. Under this condition, the magnitude of the auxiliary winding's current is much reduced from the main winding's current.

$$MMF_{ratio} = \frac{1}{a} \frac{|i_{m,rms}|}{|i_{a,rms}|} \quad [7.7]$$

When the mmf ratio is unity, torque pulsations can be set to zero, as described in [11] and [12]. However, when the mmf ratio is increased towards a critical value, the motor's efficiency increases. It is important to note that classical vector control requires the motor to operate under balanced condition, with the mmf ratio set to unity. Therefore, in the case of the PSC motor, although vector control can result in high-performance torque control, it does not guarantee the best overall efficiency.

#### **7.1.4 Prediction of Efficiency Benefits**

This work has developed a topology that can efficiently develop the necessary motor torque to satisfy the motor load without additional winding stress. The 1X-3LEG and 1.2X-3-LEG topologies are compared using detailed simulations under trapezoidal modulation strategy. The 1X-3LEG topology can deliver good efficiency up to about 70% of rated speed before efficiency begins to decrease, while the 1.2X-3LEG topology allows the motor to operate efficiently up to 100% of rated speed. This effect is illustrated in figure 7.3. Practically, the 1X-3LEG topology is able to provide a 5%-10% efficiency benefit at rated speed, compared to line operation. The 1.2X-3LEG topology is able to provide an additional 5% efficiency benefit at rated speed, compared to the 1X-3LEG topology. If sinusoidal modulation is used and the bus voltage is limited to a simple rectification of the utility supply, the motor efficiency deteriorates beyond about 30%-50% of rated speed.

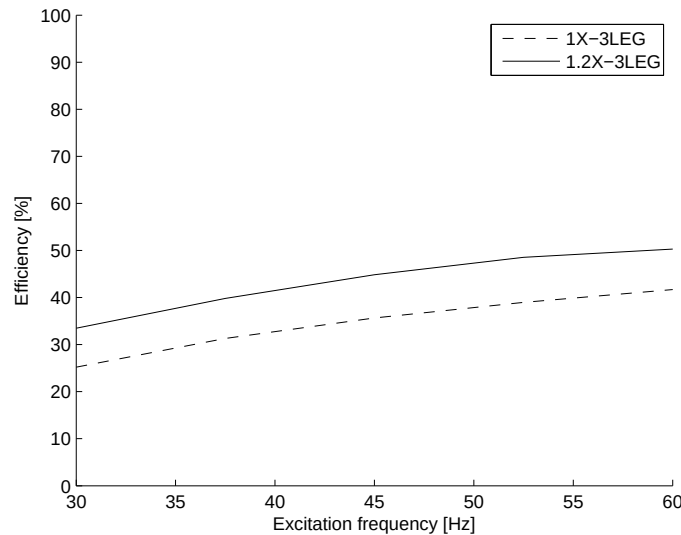


Figure 7.3 Comparison of efficiency under trapezoidal modulation of 1X-3LEG topology and 1.2X-3LEG topology

### 7.1.5 Power Loss Predictions

As stated above, the line application of PSC motors (with capacitor) results in a high mmf ratio. As a result, the auxiliary winding typically carries much less current than the main winding. Therefore the auxiliary winding usually does not need to be thermally protected, and any motor winding protection is installed in close proximity to the main winding. If the auxiliary winding carries too much current, the resulting operation could result in undetected auxiliary winding damage. This eventually would result in an inoperable motor, since the main winding alone is incapable of starting the motor. The thermal management of both windings needs to be considered when operating in this mode.

Since operating temperature is the result of thermal integration of losses, the stator copper losses may be used to obtain a good indication of stator operating temperature. The phasor model is used to predict power loss in each winding as a function of mmf ratio. The result is shown in Figure 7.4. As stated above, the balanced mmf condition corresponds to a mmf ratio of 1, and line operation is well above 2 for the 3/4 hp motor used in this simulation.

When operating at a the balance point (mmf ratio is 1), the losses in the stator winding are not minimized. The optimal operating point suggests that a mmf ratio greater than 1 will result in higher efficiency. The line-operation operating point suggests that a high mmf ratio (the exact value depends on the machine) results in poor efficiency. By operating at the optimal point, somewhere between these two extremes, the total losses in the motor windings is reduced, and the motor windings operate near each of their current-carrying design point. Care should be taken when applying such a variable-speed drive to a field-retrofit motor that the motor's auxiliary winding can safely conduct the extra current.

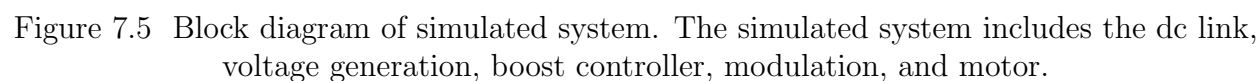


Figure 7.4 Power loss a) in each stator winding and b) both the windings as a function of mmf ratio

## 7.2 System Simulation

This section shows the simulation results of the inverter, motor, and load as a complete system. The dc link is simulated by a constant voltage with a five percent 120 Hz component. This is achievable with either a PFC front end, active front end, or a sufficiently large amount of capacitance in the dc link. The buck-boost controller is demonstrated in simulation of a 3/4 hp PSC motor, and the properties of the buck-boost inverter control signals are shown during rated operation. Selected results are presented in this section.

The simulation block diagram is shown in Figure 7.5. The simulation platform is Simulink, and the converter is modeled from the nonlinear inverter model developed in Chapter 3. The



The top-level model used to simulate the system in the Simulink environment is shown in Figure 7.6. This block diagram shows the simulated dc-bus with 5% ripple, the current controller, the duty-ratio generator (includes boost controller), modulator, motor model, and load model. The output scopes are used to plot simulation outputs.



### 7.2.1 Efficiency vs. MMF Ratio

The optimal mmf ratio and efficiency at different excitation frequency are shown for a 1 hp PSC machine in Figure 7.7. For this machine, the optimal mmf ratio is bound between about 1.2 and 1.4. The efficiency is bound by the characteristically large stator resistance, and the efficiency reduces significantly as the frequency is reduced. These effects are justifiable, since the optimal mmf ratio should lie somewhere between the line operated operating point and the balance point. For example, for the simulated 1 hp motor, the line operated case results in a mmf ratio of about 3, the optimal efficiency results in a mmf ratio of about 1.4, and the balanced mmf ratio is defined to be 1.0. The motor angle is constrained to be  $90^\circ$  and the load power is constrained to be balanced. The remaining variables (voltage, current, slip) are allowed to vary in order to satisfy the optimal efficiency constraint. The result is roughly a constant slip frequency characteristic.

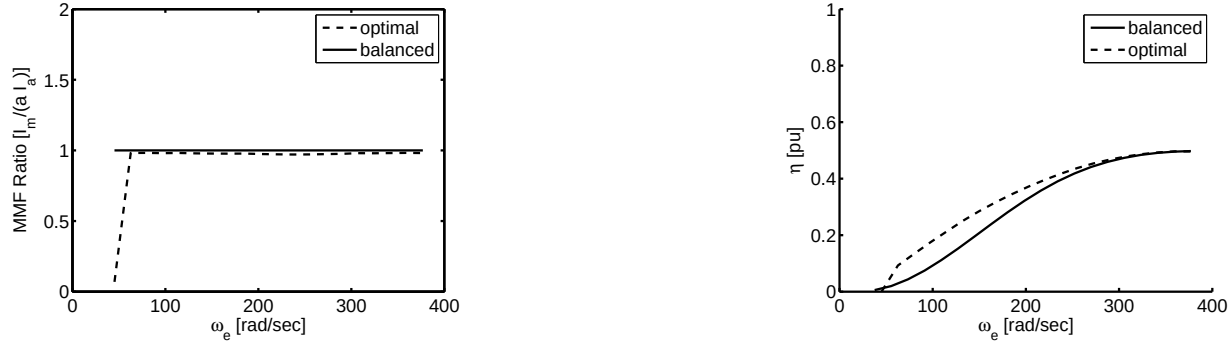


Figure 7.7 Simulation results indicating the optimal mmf ratio and efficiency as a function of frequency

### 7.2.2 Voltage Generation of the Buck-Boost Inverter Leg

Characteristic waveforms of the buck-boost inverter during boost mode operation are shown in Figure 7.8. The boost capacitor current command, pole voltage command, and boost duty-cycle ratio are shown. The capacitor current waveforms in the 'charging' and 'discharging' intervals and the corresponding duty ratio signal may be clearly observed.

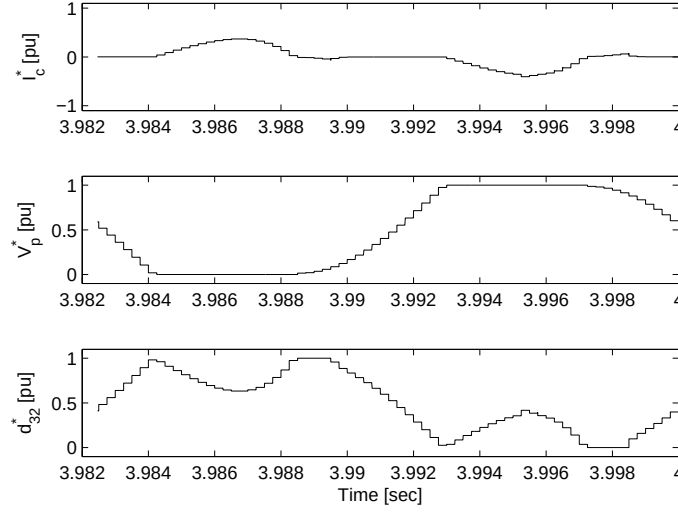


Figure 7.8 Boost capacitor current command ( $i_{c,pu}^*$ ), boost pole voltage command ( $d_{12}^*$ ), and boost duty cycle command ( $d_{32}^*$ ). Simulation conditions:  $v_{bus} = 170\text{ V}$ ,  $v_c^* = 60\text{ V}$ ,  $m_i = 0.8$ ,  $\omega_e^* = 0.95\omega_b$ .

The resulting regulated boost capacitor voltage is shown in Figure 7.9. The ripple in the regulated voltage is less than 0.2 V, which is very small. The amount of boost capacitance is  $3000\text{ }\mu\text{F}$ , and the capacitance in the dc link is  $1200\text{ }\mu\text{F}$ . Since the voltage rating on the boost capacitor bank is low, this represents roughly the same stored energy as is in the dc bus capacitor bank.

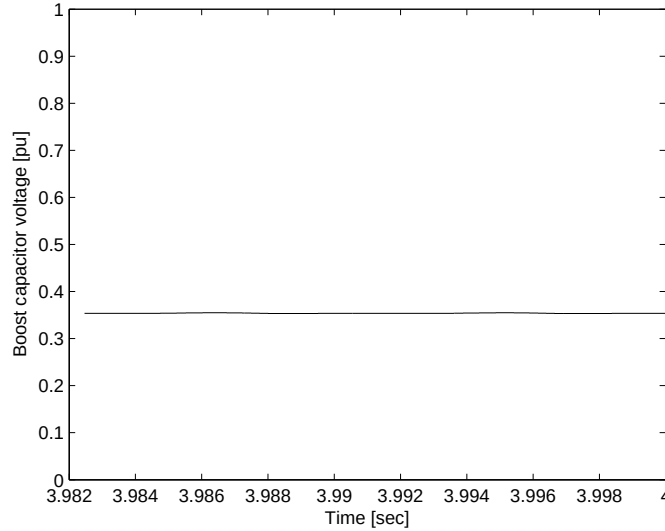


Figure 7.9 Regulated boost capacitor voltage  $v_c/v_b$ . Simulation conditions are the same as in Figure 7.8.

### 7.3 Response to Change in Frequency

A simulation is run to line start the PSC machine with balanced excitation, and then a step reduction in speed command is executed at  $t = 4$  s, at which time the speed command is stepped from  $\omega_e = 1.0$  to  $\omega_e = 0.75$ . The voltage command is generated from a  $(V/Hz)^2$  characteristic. The machine flux level is set to 0.9 pu, and the mmf ratio is set to 1.0. The mmf ratio is set to 1.0 to illustrate torque dynamics, since the torque ripple should be zero. Figure 7.10 shows the simulated voltage, current, torque, and boost voltage waveforms. Zoomed-in views of voltage, current, speed, and torque are shown before and after the step in speed command. The current distortion is significant at rated speed, but drops almost to zero after the speed command is reduced. The torque pulsations contain some 120-Hz content before  $t = 4$  s, and the torque pulsations after  $t = 4$  s is dominated by switching noise. This is the expected behavior when the mmf ratio is set to 1. The boost capacitor voltage is regulated to operate at 60 V, and comes up in less than 0.25 s.

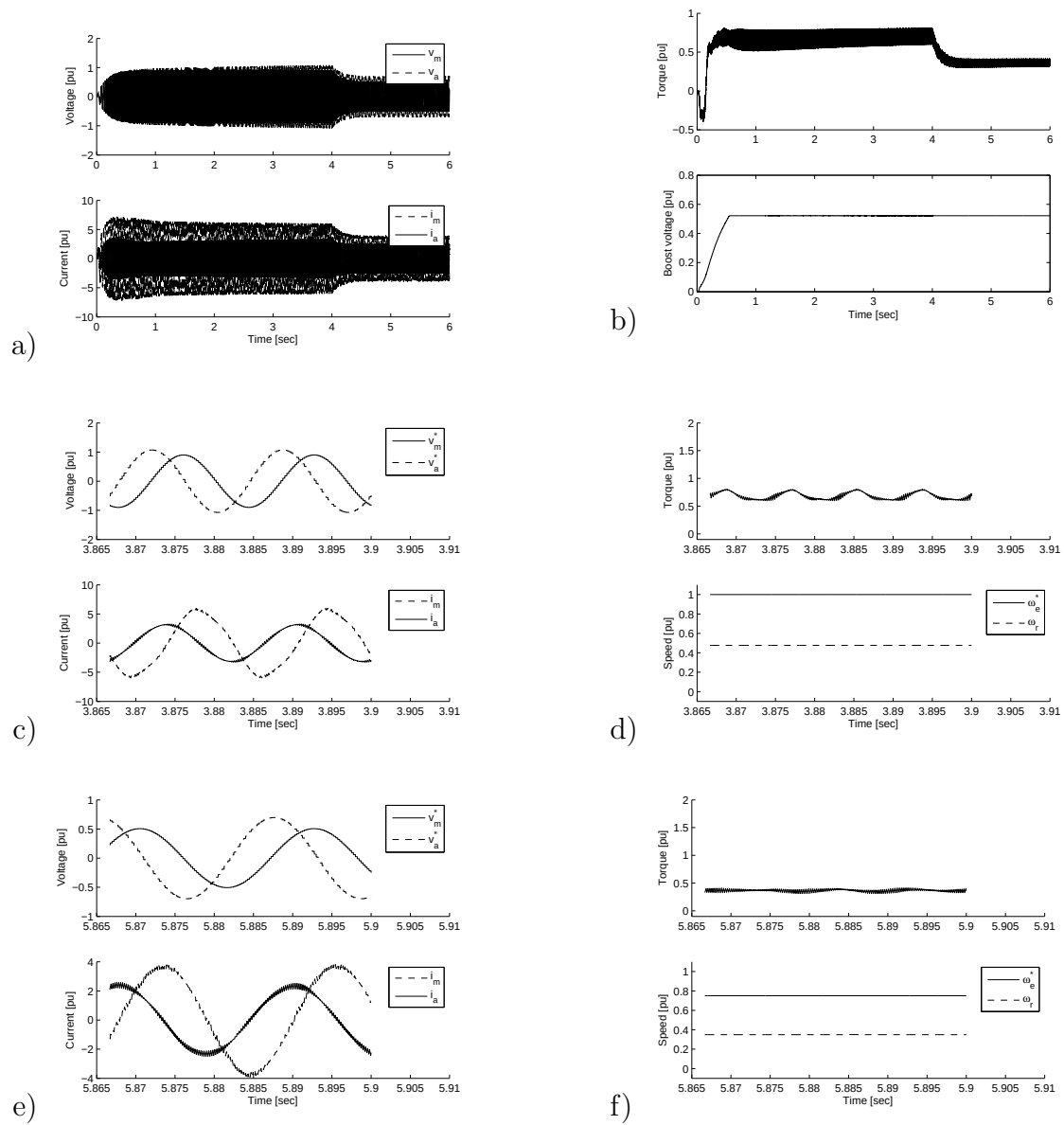


Figure 7.10 Simulation results from a step reduction in frequency command. a) VI characteristic, b) torque and boost voltage, c) VI characteristic before the step in speed command, d) torque and speed before the step in speed command, e) VI characteristic after the step in speed command, f) torque and speed after the step in speed command. MMF ratio is set to 1.0, and flux level is set to 0.9 pu.

## 7.4 Simulation Summary

This chapter has presented a summary of the simulation models and results used to verify the modulation strategies and formulation of the control of the buck-boost inverter. Use of the simulation tool to identify thermal management issues system trade offs have been discussed.

The simulation results show the efficiency benefits from the use of the buck-boost inverter using the trapezoidal modulation strategy for the 1.2X-3LEG inverter, the operation of the proposed variable speed drive system using PSC motor suitable for HVAC systems, and regulation of the boost capacitor voltage regulator with orthogonal motor current .

## Chapter 8

### Experimental Prototype 1.2X-3LEG PSC Motor Drive

The foregoing chapters in this thesis have developed an inverter that can significantly improve the efficiency of a PSC motors. The operational trade offs were explored in simulation, and the operation of the inverter topology have been identified. This chapter demonstrates the feasibility of the simulation on a sample motor using an experimental prototype.

The sample motor is characterized by the motor parameters listed in Table A.3. Through experiment, the turns ratio between the auxiliary and main windings was estimated to be 1.5.

A block diagram and a photograph of the experimental system is shown in Figure 8.1. The TMS320F28335 floating-point DSP has been used to execute the control algorithm, sample voltages and currents, and generate the transistor switching patterns. Most of the data was recorded using isolated D/A converters from the DSP system. The rest of the data were recorded using a PZ4000 power meter and isolated differential probes. The commands to the controller were generated with a custom PC application and sent to the controller using an isolated RS232 communication link.

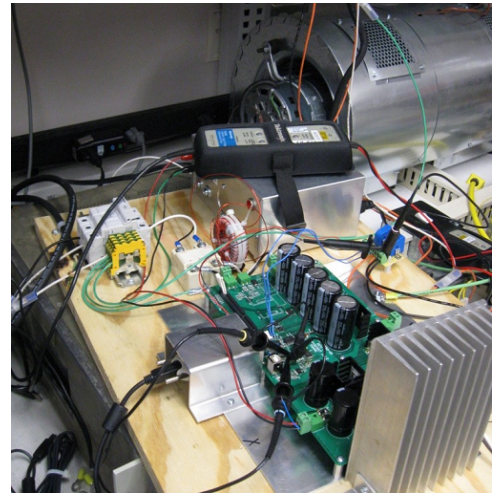
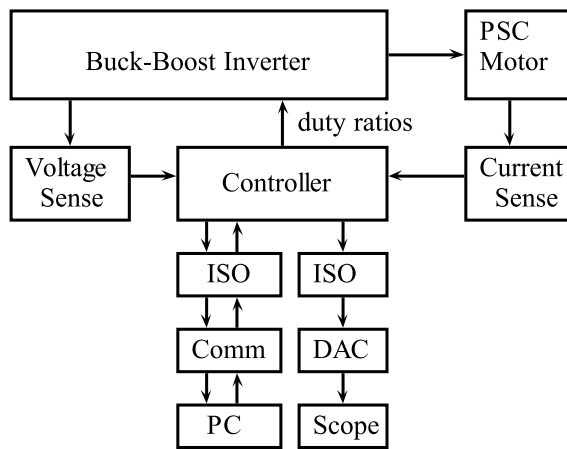


Figure 8.1 Block diagram and a photograph of the experimental setup

In order to demonstrate the feasibility of the buck-boost inverter circuit, the dc bus was set to 180 V, with the boost capacitor voltage commanded to be 45 V. This provides enough voltage to energize the auxiliary winding with a boost ratio of 1.5, and demonstrates the feasibility of the boost capacitor voltage regulation and the performance of the boost capacitor control algorithm.

This chapter demonstrates each of the salient properties of the experimental setup, and references the simulation where appropriate.

## 8.1 Line Operation of the PSC Motor

The experimental PSC motor was tested to understand the baseline performance levels of the system. Two aspects of line operation are studied: estimated efficiency as a function of capacitance, and estimated efficiency as a function of input voltage.

### 8.1.1 Efficiency as Capacitance is Varied

As listed in Table A.3, the nameplate capacitance for the sample motor is 20  $\mu\text{F}$ . In the case of experiments, the capacitance was varied from 3.5  $\mu\text{F}$  to 30  $\mu\text{F}$  using a fixed frequency,

variable-voltage sinusoidal supply, set at 60Hz and 115V. The output efficiency is estimated based on measured motor input power and an estimated output power. The motor speed is measured, and the mechanical output power is estimated as shown in (8.1). The resulting efficiency trend follows the same pattern identified in simulation, and shows a reasonable efficiency with the rated capacitance.

$$P_{out,est} = 100 \left( \frac{\omega_r}{109.9} \right)^3 [\text{W}] \quad [8.1]$$

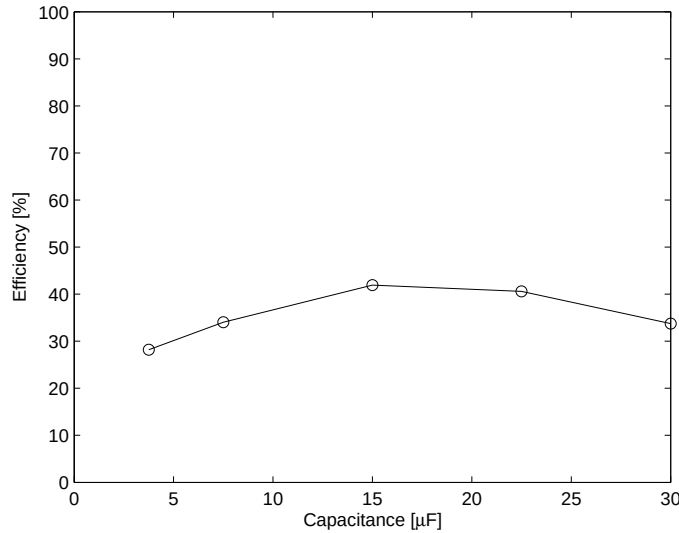


Figure 8.2 Efficiency of the PSC motor as capacitance is varied under 60 Hz operation

### 8.1.2 Efficiency as a Function of Input Voltage and Flux Selection

The motor sample available did not provide any voltage taps. In order to emulate a tapped winding, stator voltage was reduced using a variac. The resulting estimated efficiency is shown in Figure 8.3. The efficiency trend is similar to the trend observed by Mademlis et al. in [7].

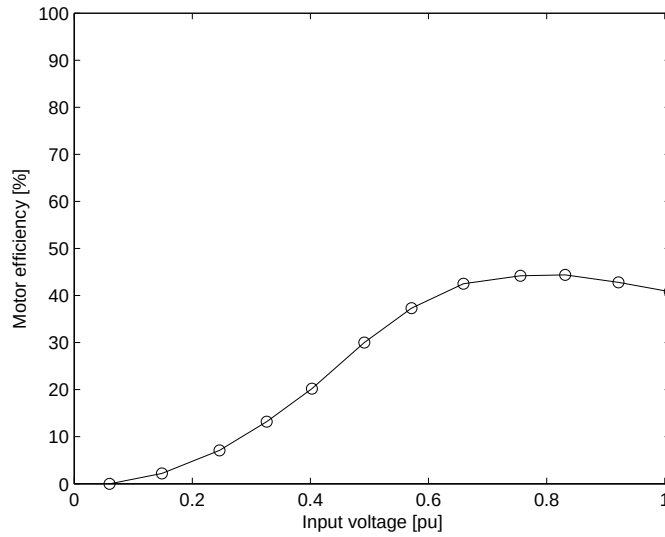


Figure 8.3 Efficiency as input voltage is reduced under fixed frequency and fixed capacitance

## 8.2 PSC Motor using 1X-3LEG Inverter

The experimental motor was driven using the prototype inverter in various operating conditions. The manifestation of unbalanced impedance among the windings and the influence this has on the phase relationships between voltage and current is illustrated in Figure 8.4, operating at a modulation index of 0.3 and an output frequency of 20 Hz. The phase angle of the currents in the auxiliary-winding and the main windings are in quadrature, while the phase angle between the corresponding voltages is approximately 50 degrees.



Figure 8.4 Voltage and current waveforms at an output frequency of 20 Hz. Under constant V/Hz, the output voltage is 0.3. The noise in the waveforms is primarily due to DAC output limits and oscilloscope quantization.

To illustrate the limits of the 1X-3LEG converter at a modulation index of  $m_i = 1.0$ , the inverter is operated at the motor's rated frequency and modulation index of  $m_i = 1.0$ . The boost capacitor is regulated at 0V. The resulting commanded output voltages and duty-cycle ratios are shown in Figure 8.5. In this mode of operation, it is interesting that the motor cannot achieve the nameplate power and stay below the motor's stator current rating. Even though the motor draws less total power than it does under capacitor operation, the main-winding power is higher, and the auxiliary-winding power is negative, compared to line operation (capacitor connection). As a result, the motor operates more efficiently overall than it does under line operation, but the windings are more stressed than they are under line (capacitor) operation.

It is observed that for this motor sample, the optimal voltage phase angle is around 50 degrees. With this phase angle, there is very little distortion in the output waveforms, beyond the clipping that occurs due to the bus voltage limit at high modulation indices. This effect is observable in Figure 8.5.



Figure 8.5 Voltage and current waveforms at an output frequency of 60 Hz. Under constant V/Hz, the output voltage is 1.0. The aux winding voltage is distorted because of the limited dc-bus voltage.

To observe the effect that the phase angle between winding voltages has on efficiency, the phase angle is varied from approximately 30 degrees to 60 degrees. Variation in the voltage phase angle more than this resulted in substantial increases in stator current. As Mademlis et al. discuss in [7], the efficiency changes if the phase angle is close to the maximum-efficiency operating point, but the efficiency is insensitive to change at this operating point. In this data, this occurs near a phase angle of 45-50 degrees. This effect is shown in Figure 8.6. When exploring this operating point, the mmf ratio is set to the optimum operating point of 0.9.

### 8.3 Efficiency and MMF Ratio

The second primary variable that influences efficiency is mmf ratio. In order to prevent the voltage limit from interacting with motor efficiency, the modulation index was set to 0.67 and the output frequency was set to 40 Hz.

The resulting efficiency is shown in Figure 8.7. The voltage angle is set to the optimum of 45 degrees. The trend shown in the figure follows the same pattern identified in simulation. For this motor, the mmf ratio that results in the best efficiency is approximately 1.0, and varies from about 0.9 to 1.3, depending on the speed and load.

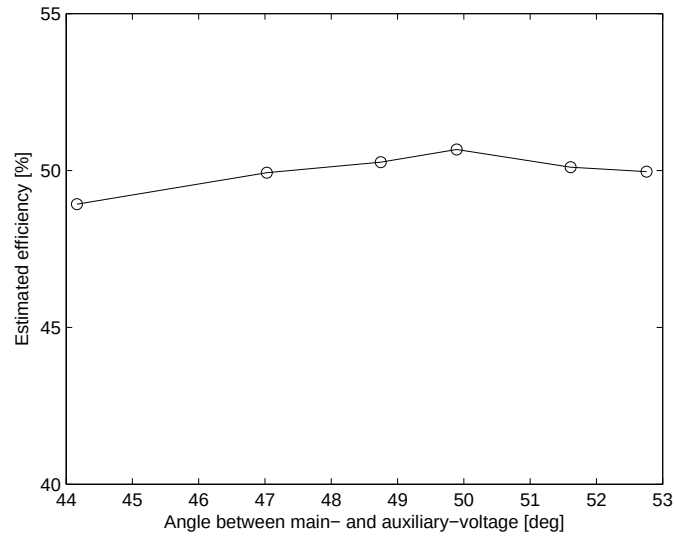


Figure 8.6 Estimated efficiency as the angle between the main- and auxiliary-winding voltage varies. The measurement reaches a maximum at approximately 47 degrees.

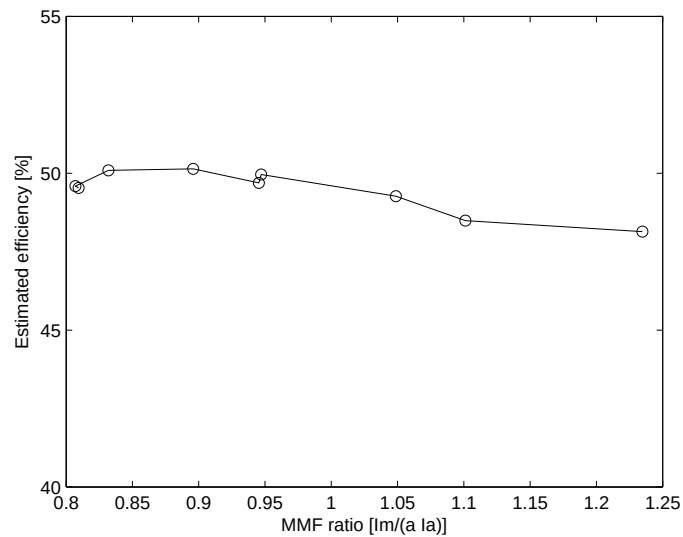


Figure 8.7 Efficiency as a function of mmf ratio. Modulation index is set to 0.67 and output frequency is set at 40 Hz to prevent the voltage limit from interacting with the efficiency study.

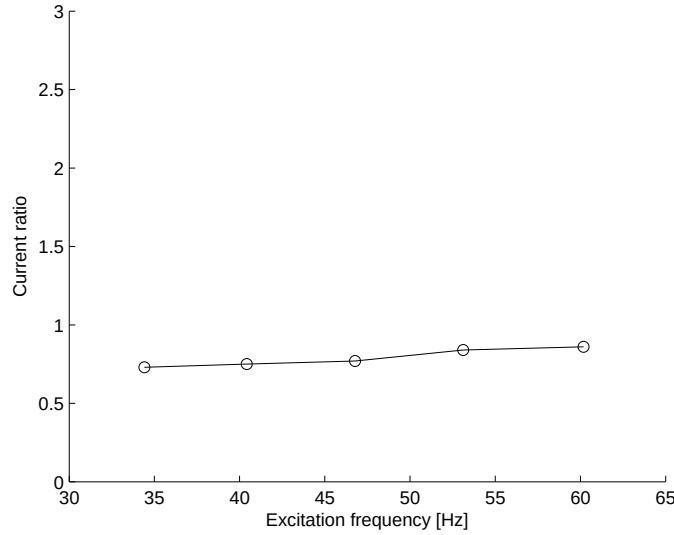


Figure 8.8 MMF ratio as a function of frequency. The turns ratio is varied for each operating speed and the mmf ratio is recorded.

In order to study the effect of varying the mmf ratio at different frequencies a manual search approach was used. The mmf ratio was adjusted to achieve a local minimum of motor input power while constraining the load to meet the motor's rated condition. The result is the mmf ratio to minimize input power at different frequencies are shown in Figure 7.7. Over this range of mmf ratios, the auxiliary winding voltage magnitude varied from 1.3 per unit and 1.7 per unit, and phase angle from 40 degrees to 60 degrees.

## 8.4 Trapezoidal Modulation

In order to demonstrate the trapezoidal modulation of the inverter within the buck operating region, the waveforms in Figure 8.9 is shown. The figure indicates the auxiliary winding voltages being sinusoidal, while the pole voltage commands following the trapezoidal and piecewise sinusoidal segments. The test conditions are shown for a modulation index of  $m_i = 0.3$  and an output frequency of 20 Hz.

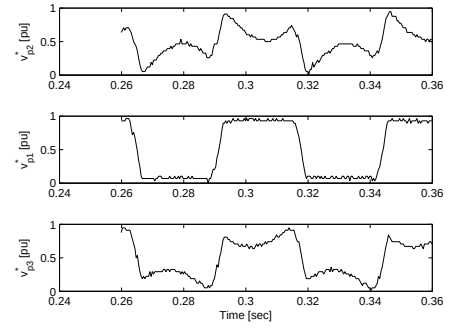
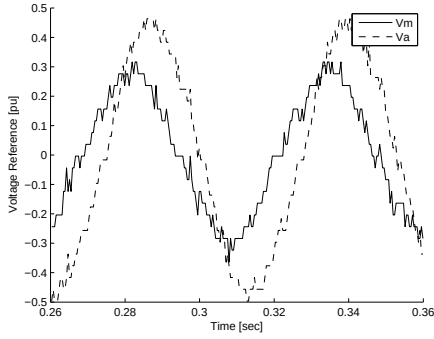


Figure 8.9 Pole voltage and output voltage waveforms for 20 Hz output frequency

## 8.5 Boost Voltage Generation

In order to evaluate the boost function in an extreme situation, the converter was operated at a modulation index of  $m_i = 1.0$  and an output frequency of 60 Hz. The commanded machine asymmetry was set to the machine's optimum of  $a = 1.5$ , and the voltage phase angle was set to about 50 degrees.

The resulting waveforms are shown in Figures 8.10 and 8.11. In Figure 8.10 the capacitor current command has a zero average value, which means the controller is able to regulate the capacitor voltage. The pole voltage of the auxiliary winding indicates the boost region in the capacitor voltage and corresponding duty-cycle. With a controller gain of  $K_p = 1.0$  [pu], the duty-cycle ratio  $d_{32}$  shows the desired inverse sine wave peak during the boost regions, and shows an unsaturated mode of operation (i.e., there is regulation headroom) during the boost voltage regulation regions.

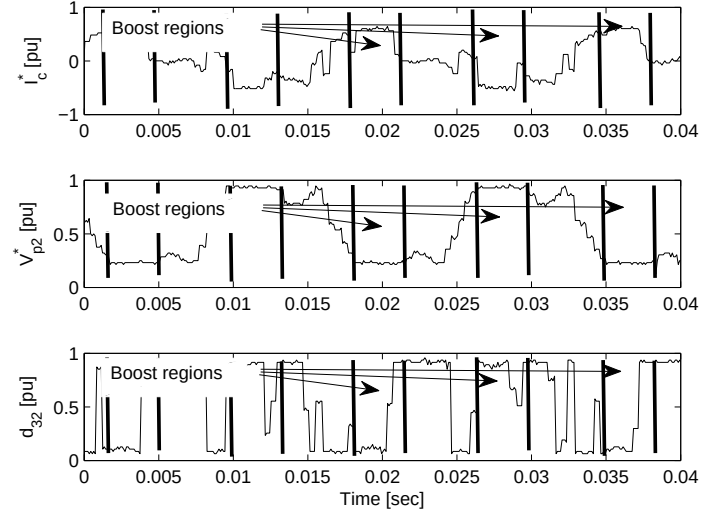


Figure 8.10 Boost capacitor current command ( $i_{c,pu}^*$ ) and boost duty cycle command ( $d_{32}^*$ ). Experimental conditions:  $v_c^* = 45V$ ,  $v_{bus} = 200V$ ,  $m_i = 0.8$ . This effect can be compared to Figure 7.8.

A waveform of the boost capacitor voltage under these conditions is shown in Figure 8.11. It may be seen that the average value of the voltage follows the command, even at the extreme asymmetry ratio of  $a = 1.5$ . There is significantly more voltage ripple in this boost capacitor voltage waveform than was present in the simulation results (Figure 7.9). The design of the boost capacitor needs further optimization.

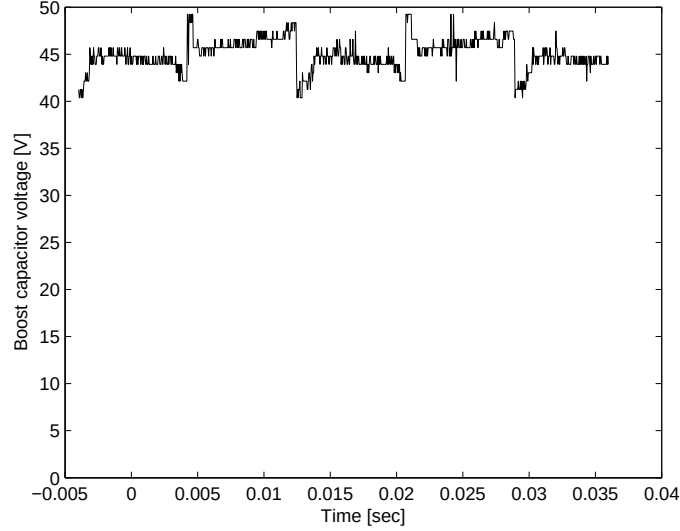


Figure 8.11 Boost capacitor voltage during rated conditions at 60 Hz. Experimental conditions:  $v_c^* = 45V$ ,  $v_{bus} = 200V$ ,  $m_i = 0.8$ . This plot can be compared to Figure 7.9.

## 8.6 Efficiency Comparison

The final result is efficiency comparison between the line-operated motor (capacitor connection), trapezoidal modulation of the 1X-3LEG inverter, and the 1.2X-3LEG inverter. These are compared across the speed range of interest in Figure 8.12. This represents the predicted efficiency very well. The boost converter shows an improved efficiency below a modulation index of  $m_i = 0.7$  due to the small amount of harmonic distortion commanded by trapezoidal modulation.

When operated by the 1X-3LEG topology, the motor cannot meet the rated load and stay within the rated current. The motor efficiency is overall better than it is under capacitor operation, but this is because the auxiliary winding is supplying negative power. This is equivalent to the circulating current argument presented in Figure 3.8.

The data in Figure 8.12 show that the 1X-3LEG topology cannot meet the required load, and it exceeds the stator current rating by 25% when it attempts to do so. In order to meet the load, the excitation frequency needs to be increased to about 65 Hz, and the current

exceeds rating by 50%. Although not shown in this figure, in order to keep the motor within its rated winding design, the motor needs to be operated at 70% of rated flux, and the efficiency is worse than it is for line operation. In addition, the motor is unable to meet its rating point in this condition. The excitation needs to be increased to 90 Hz to meet rated load at this operating point. On the other hand, the 1.2X-3LEG topology meets the machine design point, meets the required load, and improves efficiency by at least 10% absolute and 25% relative at all operating points.



Figure 8.12 Comparison of motor estimated efficiency under line operation, 1X-3LEG inverter operation, and 1.2X-3LEG inverter operation. This plot can be compared to Figure 7.3.

## 8.7 Response to Change in Frequency

Figure 8.13 shows experimental data when the frequency command is stepped so that the rotor speed transitions from  $\omega_r = 1.0$  to  $\omega_r = 0.75$ . For this experiment, the 1X-3LEG topology operates the motor at a flux level of 0.7 pu so that it does not overload the motor. In order for the fan to reach rated load, the frequency command is set to 65 Hz. The 1.2X-3LEG topology operates the motor at a flux level of 0.9 pu and  $\omega_e = 1.0$ . It is expected that the auxiliary winding voltage for the 1.2X-3LEG topology will be distorted and that the auxiliary-winding voltage for the 1.2X-3LEG topology will not. This can be seen in Figure 8.13c and Figure 8.13d.

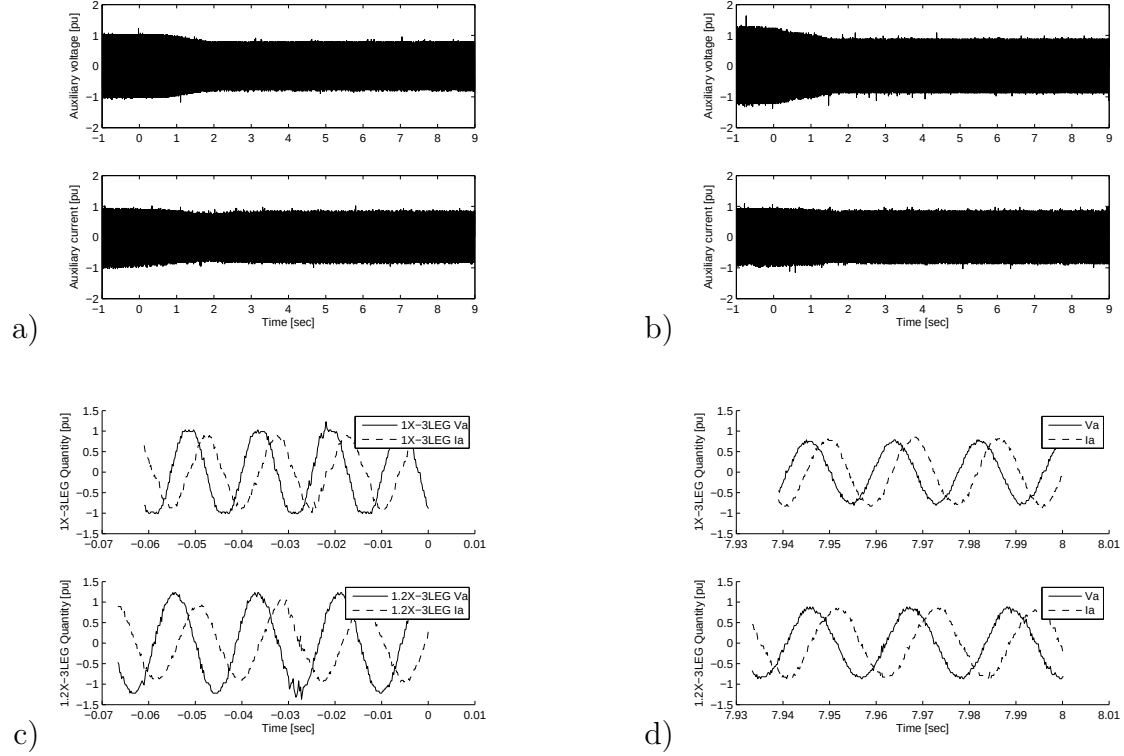


Figure 8.13 Experimental auxiliary winding voltages and currents when the frequency command is stepped from  $\omega_r = 1.0$  [pu] to  $\omega_r = 0.75$  [pu]. In order to do this and not overload the machine, the 1X-3LEG topology was operated with the machine flux level set to 0.7 pu, and the 1.2X-3LEG topology was operated with the machine flux level set to 0.9 pu. The resulting frequency command for the 1X-3LEG topology was  $\omega_e = 1.2$  [pu], and for the 1.2X-3LEG topology was  $\omega_e =$  [pu]. a) auxiliary winding voltage and current for the 1X-3LEG topology. b) auxiliary winding voltage and current for the 1X-3LEG topology. c) zoomed view of voltage and current waveforms at  $t = -0.05$  sec. d) zoomed view of voltage and current waveforms at  $t = 7.94$  sec.

## 8.8 Summary

An experimental demonstration of the 1.2X-3LEG inverter topology has been presented and compared with the 1X-3LEG inverter and line operation using a prototyped system. The characteristic of motor efficiency as a function of machine flux level, mmf ratio, and current phase angle was presented. The efficiency improvement attainable by the 1.2X-3LEG inverter

was presented, and was shown to perform superior to the other candidates under all operating conditions.

## Chapter 9

### Conclusions and Future Work

The work presented in this thesis was motivated from a critical evaluation of incorporating power-electronic devices to improve the performance of PSC motors used in HVAC applications. A new power converter for the PSC motor with competitive performance attributes has been developed and demonstrated. This chapter summarizes the contributions of this research, identifies the open questions raised by this work, and summarizes the key results presented in this dissertation.

#### 9.1 Contributions

This section summarizes the contributions made in this work. These include the development of the topology, its modeling, evaluation, control, modulation, simulations and experimental demonstration.

##### 9.1.1 Development of Design and Evaluation Criteria for PSC Motor drive for HVAC System

On the basis of analyzing of the relationship between payback periods of energy efficient devices in HVAC applications and their initial costs, a retrofit approach using PSC motors to enable variable speed HVAC systems has been proposed in this thesis. Various design criteria

besides cost, including power converter efficiency, motor efficiency, power converter VA ratings, passive VA ratings, and motor winding stress have been identified as key performance criteria to evaluate classical approaches as well the proposed alternative.

### **9.1.2 Development of the 1.2X-3Leg Inverter Topology**

On the basis of the established design criteria, a new power converter topology that has competitive performance levels has been developed. As outlined in chapter 4, the VA characteristics of the converter combines the attributes of to the best among class of PWM inverters available today. The proposed topology uses a 'buck-boost' inverter leg that is self-powered from the motor currents to provide additional voltage required to drive the auxiliary winding of the PSC motor.

### **9.1.3 Development of a Model for the Proposed Inverter**

Traditional modeling techniques are insufficient to analyze the operation of power converter, due to power transfer phenomena happening at switching frequency as well as power frequency. A model for this power converter was developed from first principles, and this model has been used to compare its performance, develop control and modulation approaches, backed up by computer simulations and experimental verification.

### **9.1.4 Comparative Evaluation of the 1.2X-3Leg Inverter Topology**

On the basis of the established design criteria, a new power converter topology that has competitive performance levels has been developed. As outlined in chapter 4, the VA characteristics of the converter are combines the attributes of to the best among class of PWM inverters available today. The proposed topology uses a 'buck-boost' inverter leg that is self-powered from the motor currents to provide additional voltage required to drive the auxiliary winding of the PSC motor.

The resulting model was used to develop a control strategy for the buck-boost inverter leg, and the criteria for stable operation of this inverter leg was established.

Finally, the dynamic model was specialized to the case of steady state in order to reduce the computational burden in exploring steady state conditions, such as finding optimal efficiency operating points.

### **9.1.5 Development of Modulation Strategies for the Proposed Inverter**

While space vector modulation techniques have been well-established for classical three phase inverters, two-leg and four-leg inverters, this work has developed them for the proposed three-leg inverter. A simple extension of the approach, labeled trapezoidal modulation strategy which features a trapezoidal neutral voltage waveform has been proposed. A harmonic distortion metric has been defined and used to compare the synthesized waveform quality of the two modulation strategies. Based on this quantitative metric, the trapezoidal modulation strategy has been found to be superior.

### **9.1.6 Development of Control Approach for the Proposed Inverter**

A controller was developed that is able to regulate the boost capacitor voltage for the operating points that a realizable system experiences. The conditions under which the boost capacitor regulation fails was identified.

A controller was developed that is able to regulate steady-state motor current when synchronous frame current regulation is not feasible. A key variable for this controller is the stator mmf ratio. The influence of mmf ratio on motor efficiency was discussed.

The problem of voltage collapse during a utility sag event was discussed. To mitigate this and related problems, a grid sag compensator was developed to present a friendly load to the utility. Since it is possible that a large number of inverters could be installed at a given

PCC, it is highly desirable for each inverter-controlled PSC motor to present a friendly load to the utility.

### **9.1.7 Simulation of the Proposed Inverter**

An analytical model of the proposed inverter was developed from first principles. This model was implemented in MATLAB/Simulink.

SPICE simulations of the proposed inverter were developed using standard components in LTSPICE, which is freely available. Targeted SPICE simulations were used to validate the model that was implemented in MATLAB/Simulink.

The SPICE model of the converter and the analytical model of the converter were validated against measurements of the prototype converter made in the laboratory. SPICE simulations were used to validate the analytical model against laboratory test cases and additional test cases that are difficult to test in the laboratory.

After validating the model, it was directly used in MATLAB/Simulink simulations.

### **9.1.8 Experimental Prototype Development of the Proposed Inverter**

A prototype of the proposed inverter was built and tested on a 1/6 hp motor with a 1/6 hp fan load. The performance of the proposed inverter was compared to the performance of the best of the inverters listed in Chapter 2, and to the performance of the motor operated under fixed frequency.

The sag compensator was shown to draw constant current from the utility in simulation. Unfortunately, due to instrumentation limitations and lack of available compressor loads, the sag compensator was not demonstrated in the laboratory.

## 9.2 Future Work

This section identifies the open questions raised by this work that may be addressed by future research.

### 9.2.1 Asymmetric Current Regulators for use with the Asymmetric PSC Motor

Current regulation of asymmetric loads is a challenging research area. Current can be controlled with stationary reference frame current controllers, but this approach does not result in high performance current control. A better alternative is to regulate current in the synchronous reference frame, but the presence of asymmetric vectors would require multiple reference frames, etc. Although the stator current can be controlled to balance the machine mmf, but a second harmonic will be present insofar as the leakage impedance is not symmetric. Open research questions include the exploration of transformations that can systematically result in good current regulation performance of the asymmetric PSC machine. On the basis of that questions such as flux estimation and speed estimation can be studied further.

### 9.2.2 Development of Rotor Speed Estimation

The estimation of rotor speed includes slip calculation and depends on vector control to eliminate the q-axis flux by aligning the d-axis with the rotor flux vector. If the q-axis flux is non zero, the state of the art in speed estimation must rely on nonphysical methods to extract the speed signal. These methods can achieve decent steady-state accuracy, but usually exhibit poor dynamic performance. An open area of research is the high-performance estimation of rotor speed.

### 9.2.3 Development of Efficiency Optimizing Search Controller

If the rotor speed can be estimated with sufficient bandwidth, a search controller can be developed to constrain mechanical output power, and search for a minimum in motor power, thereby maximizing motor efficiency. In addition, a comparison of signal-processing methods with a high-performance method would be instructive.

### 9.2.4 Space-Vector Modulation and Optimal Modulation

Space-vector modulation was explored, but the unbalanced mapping from two command quantities to three inverter outputs results in undesirable motor voltages. Further study is needed to make space-vector modulation feasible for PSC motors.

This research developed a three-terminal modulation strategy that can be used with a three-leg inverter connected to a PSC motor. This strategy is not necessarily the optimal way three pole voltages can be used to reconstruct the two commanded winding voltages. An interesting research area is the search for an optimal duty-cycle generator for the three-terminal inverter. The objective functions could include waveform distortion (balanced against the motor operating point), as well as average torque and pulsating torque.

### 9.2.5 A Unified Control Law for Buck-Boost Inverter Leg

This research has presented a controller that is able to regulate the boost capacitor voltage and develop the modulated output voltage simultaneously, but it switches between two operating regimes. While exhaustive simulations have shown this approach to lead to acceptable results, the performance of the controller and the converter may be further improved through the development of a uniform control law that accounts for low frequency and high frequency behavior simultaneously.

### 9.2.6 System Implementation Issues

Although this work has demonstrated the technical viability of the 1.2X-3Leg inverter to drive the PSC motor in HVAC applications in a competitive manner, further developments in the area of ElectroMagnetic Interference (EMI) , machine torque ripple, vibrations, etc. are topics to be studied further before the approach can reach the customer.

### 9.2.7 Field Commissioning

The practical method of commissioning and self-commissioning the inverter in the field needs to be implemented. Fortunately, the current controller developed in this research is not sensitive to very many parameters, and they can be detected during field startup without great difficulty.

## 9.3 Summary

This chapter summarized the contributions and identified the items reserved for future work in the development of variable speed drives for PSC motors. The economic viability and technical feasibility of a variable speed drive has been developed and the constraints for successful operation in each domain has been identified.

This dissertation started with the research on two-leg and three-leg inverters and extended them to meet the application needs of inverters in HVAC applications. These include a cost-effective approach to vary the applied frequency to a PSC motor while preserving the reliable motor operation and improving efficiency. The evaluation metrics to compare inverter topologies on a normalized basis of cost was presented.

A new topology was developed that met all the design criteria stated above. A control method was developed to control current in the PSC motor sufficient for the HVAC load. Modulation strategies were developed to implement the voltage modulator required by motor

controllers. A metric was developed to compare the waveform quality of these modulation strategies, and a modulation strategy was selected based on this metric.

Simulation and experimental results were presented that validate the operation of the inverter topology developed in this research. The efficiency benefits were presented and validated by experimental results at the speeds of interest to the HVAC loads.

The contributions of this work to the research community are in the area of power converter development, modulation, and control. Research items identified for future work are further refinements to the dynamic performance of the converter developed in this research.

It is hoped that the developments described in this work will pave the way to successful adoption of variable speed drives in HVAC applications, and lead to energy and cost savings.

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## APPENDIX

### Simulation and Experimental Parameters

This chapter lists the parameters used by the simulation models and the experimental setup.

#### A.1 Simulation Parameters

Table A.1 lists the simulated motor parameters. These parameters were estimated from no-load and locked-rotor tests of the experimental motor.

The tests on the experimental motor were not consistent between the main- and auxiliary-winding. When testing the motor under inverter operation, the turns ratio was estimated at  $a = 1.5$ . The main-winding experimental data were used for the stator leakage, magnetizing branch, and rotor equivalent circuit parameters. The experimental data were used for the auxiliary-winding resistance and leakage inductance. The magnetizing branch and rotor branch equivalent circuit parameters were derived from the turns-ratio relationship.

Table A.1 Simulated motor parameters

| Parameter | Value         | Description                                            |
|-----------|---------------|--------------------------------------------------------|
| $V_R$     | 115 V         | nameplate voltage                                      |
| $P_R$     | 1/6 hp        | nameplate power                                        |
| $F_R$     | 60 Hz         | nameplate frequency                                    |
| $P$       | 6             | number of poles                                        |
| $n_R$     | 1050 rpm      | nameplate rpm                                          |
| $R_{1m}$  | $7.2 \Omega$  | main-winding stator resistance                         |
| $R_{1a}$  | $15.4 \Omega$ | auxiliary-winding stator resistance                    |
| $X_{1m}$  | $6.75 \Omega$ | main-winding stator leakage reactance                  |
| $X_{1a}$  | $6.5 \Omega$  | auxiliary-winding stator leakage reactance             |
| $a$       | $1.5 \Omega$  | turns ratio between main-winding and auxiliary winding |
| $X_{mm}$  | $43 \Omega$   | magnetizing reactance                                  |
| $X_{2m}$  | $6.75 \Omega$ | stator-referred rotor leakage reactance                |
| $R_{2m}$  | $14.9 \Omega$ | stator-referred rotor resistance                       |

The simulation values for the inverter are listed in Table A.2. The bus voltage is set by the rating for the motor.

Table A.2 Simulation inverter parameters

| Parameter         | Value              | Description                                        |
|-------------------|--------------------|----------------------------------------------------|
| $C_{dc}$          | 1200 $\mu\text{F}$ | dc-link capacitance                                |
| $C_{boost}$       | 3000 $\mu\text{F}$ | boost capacitance                                  |
| $v_{boost}^*$     | 60 V               | commanded value for boost voltage                  |
| $i_{boost,limit}$ | 2 [pu]             | limit value for boost capacitor current command    |
| $K_{p,boost}$     | 1.0 [pu]           | control gain for boost controller                  |
| $K_{p,phase}$     | 1                  | proportional gain for current phase controller     |
| $K_{i,phase}$     | 12.6               | integral gain for current phase controller         |
| $K_{p,mag}$       | 1                  | proportional gain for current magnitude controller |
| $K_{i,mag}$       | 6.3                | integral gain for current magnitude controller     |

## A.2 Experimental Parameters

Unfortunately, a 3/4 hp test setup was unavailable. A 1/6 hp motor was used for test validation, and detailed equivalent circuit data is still unavailable. Locked-rotor tests and no-load tests were run at different excitation frequencies, but the results were not consistent. A more detailed test for the no-load case where the rotor is spun at synchronous frequency instead of unloaded would need to be run to get accurate results. The nameplate data for the test motor is listed in Table A.3.

Table A.3 Experimental motor parameters

| Parameter | Value            | Description            |
|-----------|------------------|------------------------|
| $V_R$     | 115 V            | nameplate voltage      |
| $I_R$     | 1.9 A            | nameplate current      |
| $n_R$     | 1050 rpm         | nameplate rpm          |
| $P_R$     | 1/6 hp           | nameplate output power |
| $C_R$     | 20 $\mu\text{F}$ | nameplate capacitance  |

The inverter parameters for the experimental setup is listed in Table A.4. The capacitance, current, and voltage ratings for the capacitors is included, and the control gains for the current controller and the boost controller are included.

Table A.4 Experimental inverter parameters

| Parameter          | Value                      | Description                                                   |
|--------------------|----------------------------|---------------------------------------------------------------|
| $C_{dc}$           | $5 \times 220 \mu\text{F}$ | dc-link capacitance                                           |
| $i_{dc,ripple}$    | 0.75 A                     | ripple current rating for dc-link capacitance (per capacitor) |
| $v_{dc}$           | 400 V                      | voltage rating of dc-link capacitors                          |
| $C_{boost}$        | $5 \times 680 \mu\text{F}$ | boost capacitance                                             |
| $i_{boost,ripple}$ | 1.2 A                      | ripple current rating for boost capacitance (per capacitor)   |
| $v_{boost}$        | 63 V                       | voltage rating of boost capacitors                            |
| $v_{boost}^*$      | 45 V                       | commanded value for boost voltage                             |
| $i_{boost,limit}$  | 2.0 [pu]                   | limit value for boost capacitor current command               |
| $K_{p,boost}$      | 1.0 [pu]                   | control gain for boost controller                             |
| $K_{p,phase}$      | 0.001 [pu]                 | proportional gain for current phase controller                |
| $K_{i,phase}$      | 0.0001 [pu]                | integral gain for current phase controller                    |
| $K_{p,mag}$        | 0.0001 [pu]                | proportional gain for current magnitude controller            |
| $K_{i,mag}$        | 0.00001 [pu]               | integral gain for current magnitude controller                |