CURRENT SOURCE INVERTERS FOR SYNCHRONOUS ELECTROSTATIC MACHINE DRIVES

by

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Abstract

Recent advancements in synchronous electrostatic machines resulted in multiple orders of magnitude improvement in their torque density. This improvement made them competitive with electromagnetic machines in macro-scale applications requiring low speed direct drives or position and hold operation. However, the torque-density improvements result in a high pole count, medium-voltage, low-current machine, i.e. a high -frequency, high-impedance machine. Conversely, magnetic machines often possess relatively lower pole counts and operate with higher currents and lower voltages resulting in lower-frequency, lower-impedance machines. Therefore, the conventional drives and power electronics for magnetic machines are not suitable for the operation of the synchronous electrostatic machines.

In this dissertation two level inverters are investigated for their suitability in electrostatic drive systems. However, to implement two level inverters switches capable of blocking the rated line-line voltage of the machine are required. A review of available medium voltage devices documents the lack of suitable monolithic switches for the low current and high frequency required for the electrostatic machine. Previous super-cascode work was evaluated and a new normally-on super-cascode was implemented. The characterization of the switch was utilized in a comparison of the voltage source and current source inverter topologies where it was determined that the current source inverter is better suited for a general-purpose variable frequency electrostatic drive application. The voltage source inverter had presented greater control/dynamics challenges but could be the preferred solution for a specific position and hold drive with proper design of the required output

filter. A CSI system was implemented with a fast output voltage loop (for torque modulation) and a slower dc-link controller. This configuration was shown to result in an unstable dc-link and a virtual resistance was utilized to stabilize the system. A system loss analysis confirmed the predicted loss dependencies from the topology evaluation and parasitic capacitance was identified as the key parasitic element that must be minimized in all system components.

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Table of Contents

List of Figures

List of Tables

Nomenclature

$\mathbf{x}$	Time varying quantity
$\mathbf{X}$	dc quantity
$\widehat{\boldsymbol{X}}$	Peak ac quantity
$\mathbf{X_{rms}}$	Root-mean-squared quantity
$\tilde{\boldsymbol{x}}$	Small-signal quantity
$\mathbf{V}$	Voltage
$\mathbf{V_{fw}}$	Froward voltage drop of a diode
$\mathbf{I}$	Current
$\mathbf{R}$	Resistance
$\mathbf{R_{on}}$	Semiconductor on-state resistance
$\mathbf{R_{th}}$	Thermal resistance
$\mathbf{C}$	Capacitance
$\mathbf{Z}$	Complex Impedance
$\mathbf{M_i}$	Back Magnetomotive force
$\mathbf{P}$	Power
$\boldsymbol{\gamma}$	Internal motor torque angle
$\boldsymbol{\theta}$	Machine Terminal power factor angle
$\boldsymbol{\eta}$	efficiency
$\mathbf{N}$	Inductor and Transformer turn count
$\mathbf{m}$	Modulation depth
$\mathbf{f_{sw}}$	Switching frequencies of converters
$\mathbf{f_e}$	Fundamental electrical frequency in Hz
$\boldsymbol{\omega_e}$	Fundamental electrical frequency
$\boldsymbol{l}$	Length. Used for air gap, winding length, magnetic path length
$\boldsymbol{K_P}$	Proportional gain
$\boldsymbol{K_I}$	Integral gain

Introduction

Over the past decade significant research effort into improving the torque density of electrostatic machines has resulted in a three-phase separately excited synchronous electrostatic machine (SEM) that is competitive with niche air cooled magnetic machines [1]. These electrostatic machines have the potential to displace electromagnetic machines in low-speed direct drive applications which can be explained by their capacitive terminal properties. The benefits of these terminal properties are best understood by comparing an inductor to a capacitor. Storing energy in an inductor's magnetic field is lossy due to the current that must continuously flow. Conversely, storing energy in a capacitor's electric field requires maintaining a voltage on the capacitor which is slowly drained by the parallel leakage resistance. At low frequency, a standard capacitor is an order of magnitude (or more) less lossy than a standard inductor. The inductor in this analogy is the magnetic machine whose torque is proportional to current, and the capacitor is the electrostatic machine whose torque is proportional to voltage. Therefore, to maintain high torque at hold or low speed the electromagnetic machines incur significant conduction losses. The SEM, which is the focus of this work, has been shown to have an order of magnitude lower stall loss than a comparable magnetic machine [1]. This machine technology and design concepts used to achieve these improvements are documented in [2]. To realize the potential improvements provided by the SEM power electronics designed for its specific application are necessary, otherwise at a system level the losses will not be improved. Since this is the first documented power electronics work for SEMs, a fundamental two-level

inverter design to investigate and understand the challenges associated with electrostatic drives was desired.

Chapter 1 reviews past electrostatic machines and their drive systems, and concludes that development in this space is decidedly ad hoc, i.e. there is no foundation broadly transferable to the SEM. Chapter 2 develops a super-cascode with suitable specifications for a two-level inverter. Design rules for super-cascodes in electrostatic drives are presented and characterized experimentally. In Chapter 3 a model of the super-cascode was utilized in a simulation-based comparison between the voltage source and current source inverters. Current source inverters were found to have qualities better suited for a general-purpose variable speed drive while the voltage source inverter has potential in position and hold applications but it less suitable for continuous motoring. Passive component design and parasitic element management significantly affect both drive types.

Chapter 4 develops the theoretical foundation of a current source inverter system fed by a large voltage gain front end converter with a regulated dc-link current. An average model of the system showed that the high-performance inverter voltage controller developed in [3] presents a constant power load to the dc-link. The constant power load characteristic results in a right-hand-plane pole and two different controllers to stabilize the system were proposed. The first controller offsets the effective negative incremental resistance of the constant power load with a virtual dc-link resistance, shifting the pole to the left-hand-plane. This controller has excellent small signal characteristics of stability and disturbance rejection; however, it has reduced large signal performance, i.e. limited load transient and command tracking capability. An alternative controller addresses the instability by decoupling the voltage disturbance created by the inverter voltage controller on the dc-link.

This method improves the load transient capability and with an effective lower impedance dc-link has improved dc-link command tracking but has limited unmodelled disturbance rejection.

The hardware implementation of the inverter is documented in Chapter 5 and the system testing is presented in Chapter 6. The system testing confirmed the system modeling and the effectiveness of the proposed control methods in stabilizing the system. A system loss analysis confirmed the simulated loss dependencies from Chapter 3 and identified parasitic capacitance as the key element that must be minimized for the system subcomponents.

Chapter 7 provides a comprehensive summary and conclusion of the work, accompanied by the contributions and recommended future work in the topic of power electronics for electrostatic drives.

Chapter 1: Background

1.1 Electrostatic Machines and Their Drives

Electrostatic machines have attracted interest over the years for various applications, ranging from micro-electro mechanical system (MEMS) motors for miniaturized pumps and turbines [4] to mega-watt scale design analysis for power generation [5][6]. Electrostatic actuators such as dual excitation multiphase electrostatic drive (DEMED) linear machines [7] and dielectric electro active polymer (DEAP) gripper actuators [8] have generated interest as well.

In the micro-scale nNm are achieved at high speed 20,000 RPM to produce appreciable MEMS power (mW). Since these machines possess small physical dimensions (microns) it is easy to produce high fields with comparatively low voltage ratings (<500V) which allows for a wide range of suitable power electronics. However, their main issue is extremely high fundamental frequencies up to 2 MHz, which is solved by implementing a simplified 9-level inverter. The inverter topology is not a traditional high power multi-level inverter but instead series connected outputs from high frequency transformers [9]. The topology, shown in Figure 1-1, utilized minimal control complexity, is highly modular and does not require a multitude of isolated gate drivers.

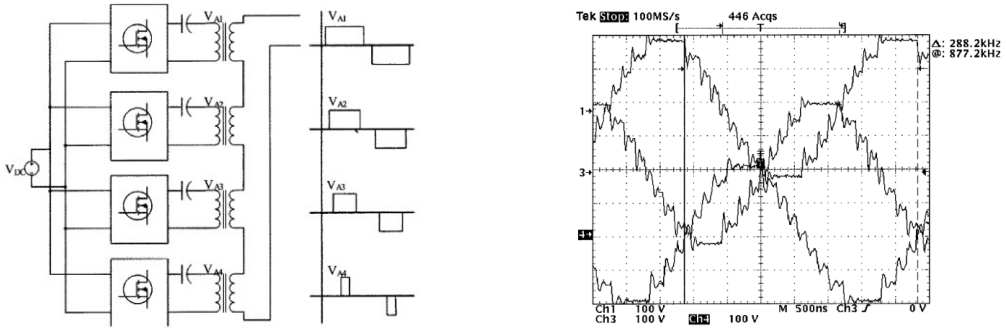

Figure 1-1. Multi-level topology and waveforms for driving high speed (20,000 RPM) micro-scale machines ©IEEE [2004] [9]

The work presented in this dissertation focuses on a machine with significantly higher voltage (7kV) at fractional to integer Hp ratings and much lower fundamental frequency. The transformers operate at fundamental frequencies in the 9 level topology proposed in [9], meaning at the hundreds of Hertz range needed for the work here the transformers would be physically large. Furthermore, they would not be suitable for dc applications. With the increased voltage and power compared to the MEMS-scale applications, the transformer isolation and parasitic circuit elements would become a significant challenge as well.

The proposed rotational machines in the MW scale of [5] and [6] are variable capacitance machines utilized as generators. These machines provide an interesting solution for direct connection of wind-power generation to HVDC transmission. They conceptually require quite simple power electronics, shown in Figure 1-2, consisting of a dc-power supply and two diodes per-phase to manifest a high voltage dc (HVDC) charge pump. However, the work does not translate to the synchronous electrostatic machine which requires controlled sinusoidal excitation.

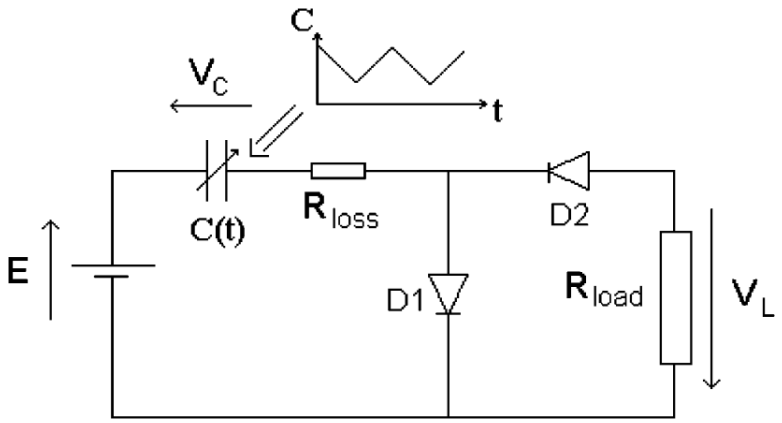

Figure 1-2. Variable Capacitance DC Generator ©IEEE [2009] [6]

The linear machines of [7] had complementary work developing drives in [10]. These machines have access to both stator and rotor terminals analogous to doubly fed induction machines. These machines require two balanced three-phase drives to create the travelling waves necessary for force production and the drive topology is shown in Figure 1-3. The researchers here were also looking to simplify the power electronics and focused on leveraging low voltage linear power amplifiers and step-up transformers. They utilize signal modulation and dual frequency excitation to create dc-terminal voltages that avoid saturating the step-up transformer. However, this machine is a linear machine with two three-phase terminals and not intended for continuous power conversion. The dual frequency modulation is lost for a machine with a single set of three-phase terminals and the transformer step-up approach is no longer suitable.

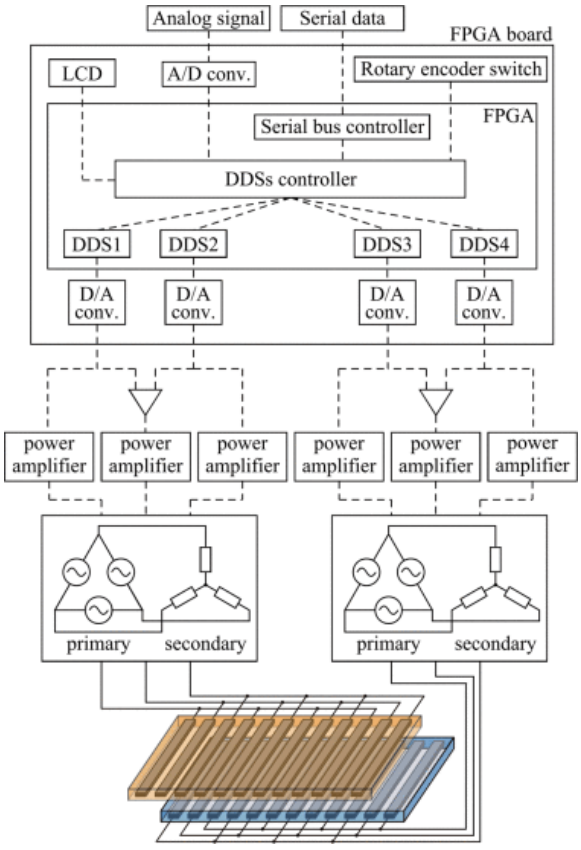

Figure 1-3. Linear electrostatic motor drive ©IEEE[2011] [10]

The electrostatic actuators of [8] are linear actuators that require single phase dc medium voltage (~2.5kV) to create a gripping force proportional to the applied voltage squared. Since this type of machine presents capacitive terminal properties it requires a supply that can quickly charge and discharge a capacitor. There are a multitude of capacitive charging circuits but one fundamental topology providing low-cost simple power-electronics with high voltage-gain is the flyback converter. Utilizing bidirectional versions, power supplies with 2.5kV outputs and fast rise times of 5ms can be achieved [11][12]. This work is of relevant for position and hold application of the synchronous electrostatic machine and was briefly explored in [13], but it is not the focus of the dissertation.

1.1.1 Synchronous Electrostatic Machine

The electrostatic machines reviewed in the prior section were focused on niche applications where conventional electromagnetic machines struggle (size or loss). It is clear that due to the comparably low torque density of electrostatics, electromagnetic counterparts have been the machines of choice for the general-purpose applications at the macro scale. To improve the torque density gap, research focused on increasing the surface area per unit volume, utilizing a liquid optimized for field breakdown, permittivity and viscosity, and embracing high pole counts and medium voltage designs [1]. This culminated in a three-phase separately excited synchronous electrostatic machine (SEM) that is competitive with modern air-cooled electromagnetic machine in torque-density and has an order of magnitude lower electrical loss.

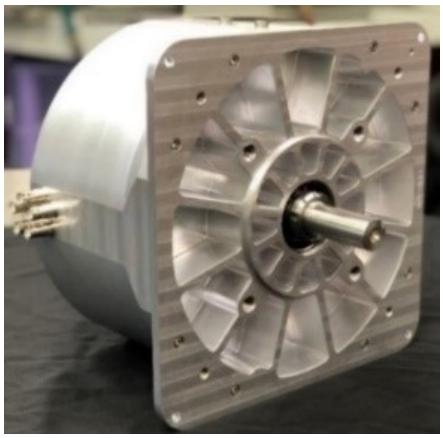

Figure 1-4. Synchronous Electrostatic Machine

Table 1-1. Machine Parameters

V_s	Peak Line-Neutral Stator Voltage	4 kV
V_f	Field Excitation Voltage	7 kV
R_s	Stator Line-Neutral Resistance	1.6 MΩ
C_s	Stator Line-Neutral Capacitance	13.8 nF
C_m	Mutual Capacitance	2.2 nF
M_i	Back MMF	$C_m V_f \omega_e$
Poles	Poles	96
T_R	Rated Torque	9 Nm

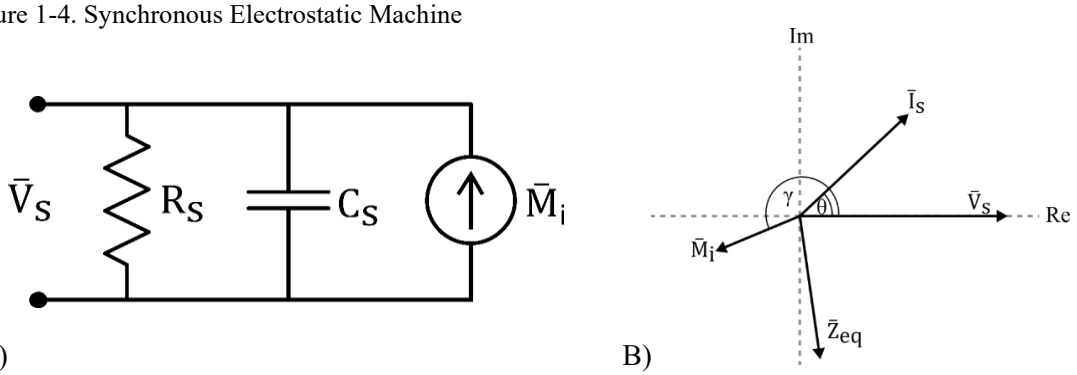

Figure 1-5. A) per-phase equivalent circuit of three-phase separately excited SEM B) Phasor diagram of equivalent circuit

The synchronous electrostatic machine (SEM), shown in Figure 1-4, is a three-phase separately excited synchronous machine with the name plate parameters of Table 1-1. The simplest model is a per-phase line-neutral equivalent circuit, shown in Figure 1-5-A, which is useful for deducing the machine's behavior. This model captures the electric field provided from the excited field plates and their coupling to the stator through the mutual capacitance as a speed-dependent back current or magneto-motive-force (MMF) i.e. the current source M_i (note the back MMF does not serve a function from an Ampere's Law perspective, but the term provides a functional familiarity as the dual to back EMF). The equivalent phase-neutral stator capacitance C_s is the sum of the mutual and leakage capacitances, and stator parallel resistance R_s represents the main electrical losses of the machine. The speed dependent back-mmf is governed by (1-1), and mechanical power is

defined as the real power sourced or sunk into M_i expressed in (1-3). In this dissertation the machine is always operated at its maximum torque per volt (MTVP), i.e. $\gamma = -180$ for motoring. Comprehensive machine design is detailed in [2] and the torque modulation, including self-sensing in [3].

$$\bar{M}_i = V_f \omega_e C_m \angle \delta \tag{1-1}$$

$$P_{mech} = \frac{3}{2} \mathbb{R}\left\{\overline{V_s}\overline{M_i}^*\right\} \tag{1-2}$$

$$P_{mech} = \frac{3}{2} V_s M_i \cos(\gamma) \tag{1-3}$$

$$T_e = \frac{P_{mech}}{\omega_r} \tag{1-4}$$

$$\omega_e = Poles * \omega_r \tag{1-5}$$

Combining equations (1-1) through (1-5)

$$T_e = \frac{3P}{2} V_s V_f C_m \cos(\gamma) \tag{1-6}$$

Using the model of the machine at rated voltage and torque Figure 1-6-A shows the constant and low electrical loss of 14 W. Due to this, high electrical efficiency is reached above 100 RPM. Figure 1-6-B shows the minimal line current and the relatively low magnitude back-mmf. This low back-mmf results in a low power factor at high speeds as the stator impedance decreases with frequency. With minimal heating due to electrical losses there is no need to de-rate the machine in position and hold applications, and it can achieve excellent performance in low speed direct drive applications. It was reported in [14] that the SEM machine, with a higher performance liquid, achieved 8 Nm of holding-torque with only 5W of loss. A comparable electromagnetic servo machine required 100W of loss for the same torque [14].

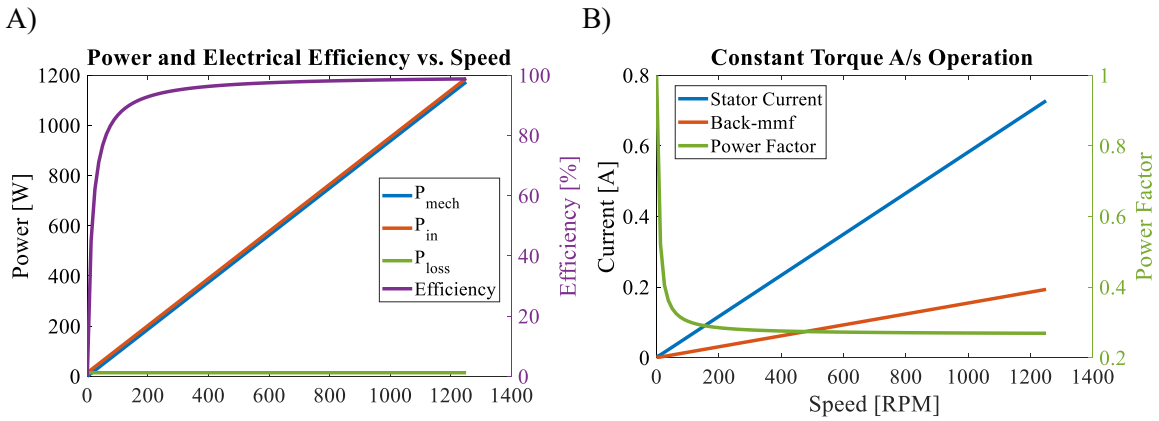

Figure 1-6-Machine characteristics vs speed: Power and Torque (A) Machine currents and power factor (B)

1.2 Review of commercial and research medium voltage semiconductors

Before the recent advancements in silicon-carbide, medium-voltage solid-state devices primarily consisted of slow large silicon-devices. Their main use being MW size and higher targeting medium voltage drives for industrial applications, HVDC transmission and power quality and control for ac grid applications. Medium voltage silicon-carbide devices have had significant investment in working towards entering these markets as well. Figure 1-7, taken from an overview paper on Silicon Carbide (SiC) written by engineers from ABB [15], shows the traditional use of Si devices and where emerging SiC can have an impact. This figure summarizes how wide bandgap devices are increasing power density by increasing the switching frequency of higher power density converters. However, the graph on the right, shows a trend where with increased device blocking voltage the current ratings (and in turn power) of the devices increases with the device voltage. This is unfortunate for the SEM application where high voltage devices at low current are needed.

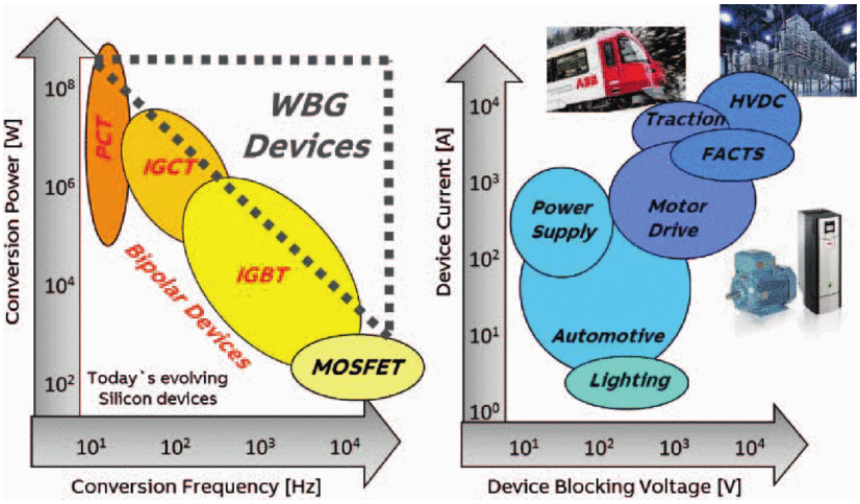

Figure 1-7. Application Space for semiconductor devices © [2018]IEEE [15]

The unique characteristics of the SEM creates some challenges when implementing the hardware for the electrostatic drives. With the medium-voltage line-line rating (7kV) but low power (<5kW) there is no commercial monolithic semiconductor switch available that is suitable for a SEM high-performance drives. Naturally, the semiconductor industry produces devices and modules with ratings aligned to market pull. Looking at the offerings of Digi Key in Figure 1-8, shows the lack of Metal Oxide Semiconductor Field Effect Transistors (MOSFET) and Insulated Gate Bipolar Transistors (IGBT) in suitable voltage range and of Silicon Controlled Rectifiers (SCR) with low current. One exception would be in the diode market there are suitable fast high voltage diodes that can be utilized, and series connection of diodes is relatively straight forward.

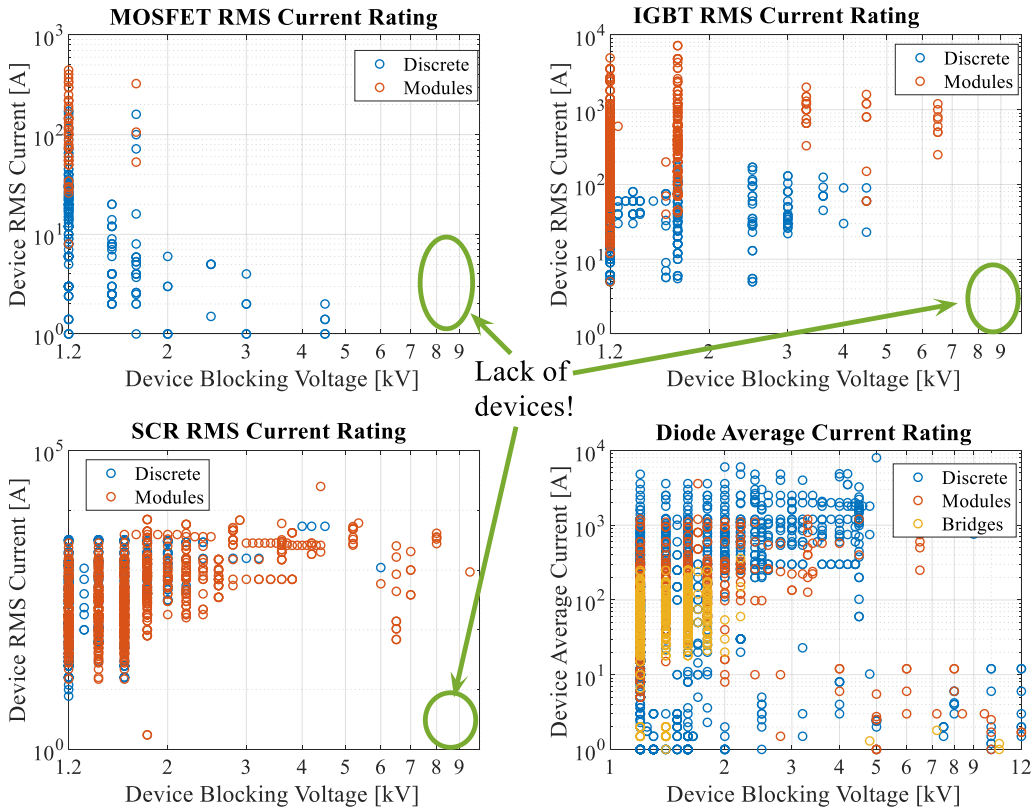

Figure 1-8. Semiconductor Switches available from Digi Key

1.2.1 Silicon Devices

There has been over half a century of research and development in fully controlled silicon power devices. As the technology matured the rated off-sate voltage was pushed continually higher. Applications with very high voltage continue to use thyristors where the devices extremely low loss on-state characteristics with package offerings of 1.5 to 6.25 kA and maximum voltages of 8.5 kV [16]. However, in PWM inverters a controlled turn-off is required resulting in integrated gate commutated thyristor (IGCT) and insulated gate bipolar transistor (IGBT) having significant development in the last two decades.

The IGCT is particularly well suited for high current since its on-sate is like a traditional thyristor. They come packaged in full 150mm press-pack “hockey-puck” packaging that provides inherent double layer cooling [17]. With their hard turn on characteristics circuits

limiting the di/dt are necessary; limiting their high frequency operation. They have very high current capabilities with asymmetric, symmetric, and reverse conducting (integrated diode) versions of devices, leading to their application in low speed, low pulse count medium voltage drives [17].

The IGBT is probably one of the most used power electronic devices of the last two decades with its dominance of the 600 V to 1700 V high current market. With advancements in the device structure the voltage rating and current ratings of IGBTs are pushing into the 6.5 kV and 2400 A module ratings[18]. While thyristors and IGCTs are packaged at a wafer level, IGBTs are generally utilized in multi-chip power modules. Each individual chip is rated from 50 to several hundred amperes and chips or modules are paralleled to reach the 2400 A range. These packages are an engineering feat in themselves with the modern LinPack enabling high power densities [19]. With continual improvement in IGBT performance there are variants optimizing switching vs conduction vs robustness. All in all, the IGBTs provide high current power conversion into the low kHz of switching speed.

There are discrete IGBTs from IXYS (now owned by Littefuse) with 2.5 to 4 kV voltage ratings in TO-254 style packaging [20]. With ratings in the 20 to 90 A these devices still have significant capacitance and are older non-punch through IGBTs with slow switching characteristics and tail currents. IXYS also offers similar MOSFETs with a maximum voltage of 4.7 kV and high on resistance 20 – 625 Ω [21]. These devices were considered for series connection but the requirements of a medium-voltage isolated gate-driver for each one resulted in an overly complicated gate drive requirement which ended up significantly exceeding the power switches in volume and cost.

1.2.2 Silicon Carbide Research

The Power America Manufacturing Institute encouraged interaction between chip developers, research universities, national labs, power module developers, and system developers to pursue collaborative research and development [22], [23]. This resulted in medium voltage devices in the 3.3 kV to 10 kV range receiving significant research investment pushing the boundaries of where low-voltage wide band gap devices have had commercial success. While SiC pushes the boundaries of what is capable with unipolar devices (MOSFETs) there is a point above 10 kV where SiC IGBTs and thyristors become competitive [24]–[26]. These are very much in the research phase at present and are not considered for use here but will merit serious attention in the years to come.

On the SiC MOSFET front the 10 kV SiC device is an ideal candidate for this work. The current rating of the prototype Wolfspeed 10kV chip is 10 A throughout research papers and announcements [27], [28]. Unfortunately at this time the focus is on multi-chip power modules targeting current ratings in the 100 A or above that would cover parts of the area of IGBTs in Figure 1-7 [29]–[31]. At this point it is likely that the current rating of the die will only increase as the manufacturing process is improved and die impurities are lowered; a common trend in power semiconductors as shown in Figure 1-8. If electrostatic machines garner commercial traction, interest in low current packaging of these devices would provide significant power density benefits.

One type of device not mentioned until now is the SiC Junction Field Effect Transistor (JFET) [32]. This is a unipolar device with a very simple structure resulting in a fast, low on-resistance, normally on switch. As a monolithic switch it is limited to low voltage but in research applications it has been series connected to create effective medium voltage

three terminal devices [33]–[36]. This structure is referred to as a super cascode and is investigated in depth in Chapter 2, where a targeted state of the art review on super-cascode implementations is performed.

1.3 Research Opportunities

The review of available medium voltage devices reveals there is clearly not an ideal single device solution for this application. To solve this problem for SEM drives the problem can be tackled from two ends:

1) create a switch from series connected devices that emulates a single a monolithic device from a terminal/controller perspective,

2) topologically, by using multi-level converters.

It is without question that multi-level converters introduce significant system complexity. The increased system complexity can be worthwhile when it provides additional performance benefits such as reduced total harmonic distortion, fault tolerance or reduced dv/dt. If the power being processed is significantly large that the added costs in gate drives, power supplies, advanced controls, and energy storage does not significantly increase the overall cost, then the tradeoff can be made.

Since the work presented in this dissertation composes the first power electronic drive for the SEM, the establishment of a drive baseline is desired, and the two-level inverter approach was chosen. However, a switch capable of blocking the rated voltage of the machine is required. Chapter 2, focuses on the design and characterization of a low current three terminal medium voltage switch, constructed from series connection of normally on JFETs.

Chapter 2: Normally-On Super Cascode

Chapter 1 identified the lack of semiconductors suitable for the medium voltage and low current that are necessary for high performance SEM drives. This chapter focuses on the development of a JFET super-cascode suitable for SEM drives. Prior research on designing and optimizing variations of super-cascodes is presented followed by a section on the design and packaging of a prototype suitable for the SEM with the target ratings in Table 2-1.

Table 2-1. Super-Cascode Design Goals

Rated Current	2 A_{rms}
Target Switching Frequency	20 kHz
Breakdown Voltage	>10 kV

The steady state machine model from section 1.1.1 evaluated at maximum operating point requires a peak phase current of 0.8A at 2 kHz. A switch capable of 2 A_{rms} and 20 kHz switching allows for evaluating a large operating range and design headroom for future machines with improved dielectric liquids. The machine voltage rating of 7 kV line-line drives a desired voltage rating exceeding 10 kV to provide voltage margin concerning switching and load transients. The switching frequency of 20 kHz arises from the 96 poles of the machine combined with a theoretical max speed of 1250 rpm, yielding a 2 kHz electrical fundamental frequency. Servo performance of vector controlled synchronous machines requires a minimum of ten times the fundamental frequency amount [37], i.e. 20 kHz.

2.1 Super-cascode state of the art

A SiC JFET cascode, Figure 2-1-A, enhances the high voltage blocking and fast switching performance of a normally-on SiC JFET with the traditionally desired normally-off characteristic of a silicon metal-oxide field effect transistor (MOSFET). This is achieved by placing the devices in series and coupling the gate of the JFET with the source of the MOSFET via a diode. The JFET gate-source voltage, which must be negative for the device to be off as shown in Figure 2-1-B, is dependent on the MOSFET drain-source voltage. The origin of the cascode name comes from before solid-state devices when two triodes were combined in a "**cas-**cade configuration to replace a pen-**tode"** [38].

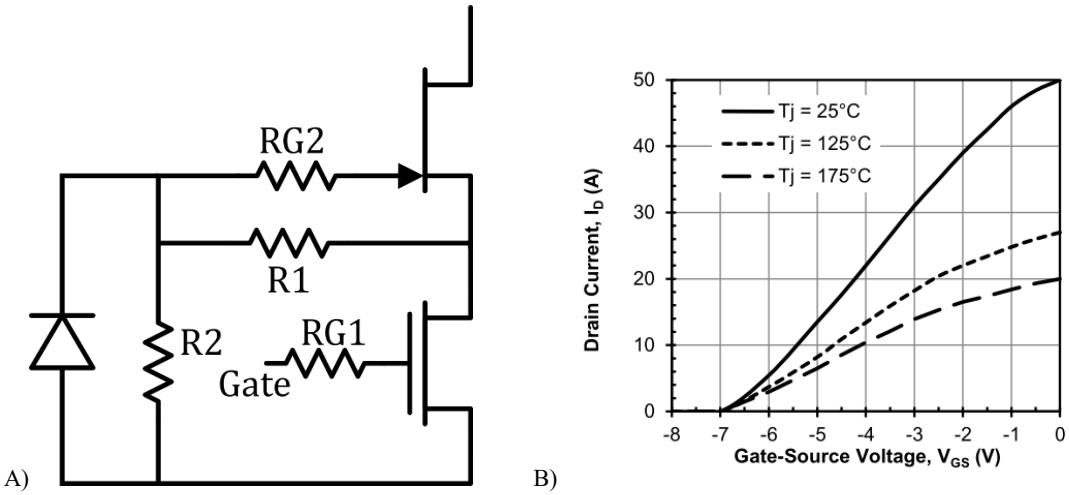

Figure 2-1. A) Fundamental Cascode Structure B) Normally-on JFET transfer characteristics [39]

To understand the switching sequence, a sketch of a turn-off transition is shown in Figure 2-2. Starting from the on-state the gate-driver of the controlled bottom switch (MOSFET) is turned off and the gate-source voltage transitions through the miller plateau (top plot) during which the drain-source voltage of the controlled device increases (plot 2). The gate network, R1 and R2 in Figure 2-1, creates a voltage divider where the gate-source voltage of the cascoded device is the negative of the voltage across R1. Due to gate

resistance, capacitance, and the miller plateau of the cascoded device the internal gate-source voltage of the cascoded device goes through a transition similar to a device being controlled by a gate-driver. This delayed response is sketched in plot 3 of Figure 2-2. Finally, the drain-source voltage of the cascoded device rises and the switch is fully turned off (plot 4). Since the voltage divider creates a negative gate-source voltage during the off-state and zero volts during the on-state, normally-on devices (JFETs in this case) are ideal for cascodes. The voltage blocking capability can be further extended by placing more JFETs in series with successive gate-coupling networks, each dependent on the drain-source voltage of the device below them [36].

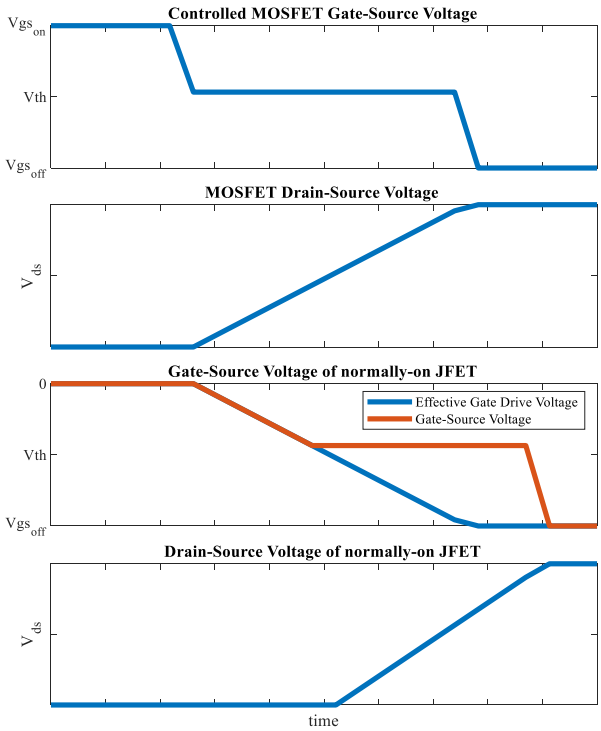

Figure 2-2. Sketch of normally off cascode turn off sequence

This configuration with multiple JFETs is called a super-cascode and work on gate coupling networks for improved switching performance has been done over the last two decades. Switching performance was improved in [40] by the addition of RC networks

which provide faster turn-on transitions and improved dynamic voltage sharing during turn-on and off. A variation of the RC networks was implemented in [34], where scaling values of capacitors for each switch in the stack further improved switching performance and replaced the low voltage silicon MOSFET with a 1.2kV SiC MOSFET. Additionally, the gate network was driven positive to drive the JFETs in the stack above 0 volts gate to source. A more complex balancing network of alternating diodes and resistors with multiple passive devices referenced to the source of the controlled MOSFET was developed in [35] . However, since resistors and capacitors are connected from the topmost device to the lowest, the scaling versus voltage of this network is more difficult to implement due to the increased voltage requirement.

All these coupling networks try to improve balancing between devices and decrease overall switching loss. This is achieved by adding stored energy in the gate network that can be utilized to turn-on the devices more quickly. The added capacitance in the network cause the turn-off transitions to increase since the stored energy must be replaced. The balance between turn-on and turn-off losses ultimately depends on the operating point, circuit parasitics, and the free-wheeling diode in the switching circuit. All the state of the art super-cascode research has focused on traditional voltage stiff dual active bridges [41], [42] that prefer normally-off switches. The work presented in the coming sections focuses on developing a normally-on super-cascode prototype and experimentally comparing the fixed capacitance method from [40] and the scaling capacitance method from [34] at operating points suitable for SEM drives. The normally-on characteristic is preserved in this work such that it is more suitable for use in current source inverters and has not been shown in the literature elsewhere.

2.2 Super-Cascode Design

To achieve the requirements of the switch laid out in the introduction, the 80mΩ 1.2kV SiC JFET from United SiC [32] is used in this super-cascode. Since a normally-on characteristic is desired, the traditionally normally-off controlled device at the base of the stack is replaced with the 80mΩ JFET as well. Twelve JFETs are connected in series (Figure 2-3) where eleven are passively controlled by the gate network and the bottom device is the controlled device.

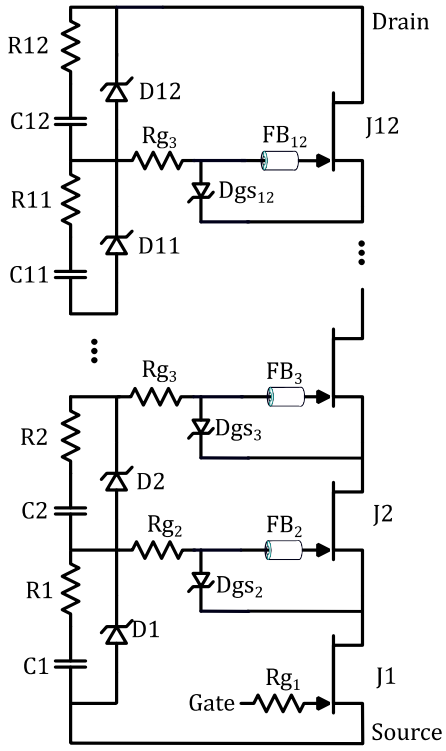

Figure 2-3. Implemented Super-Cascode

Table 2-2. JFET Super-Cascode Components

J1-J12	80 mΩ 1.2kV UJN1208K
R1-R12	10 Ω
C1-C12	NPO Ceramic Capacitor, value dependent on design
D1-D12	2x P4SMA TVS Diodes in Series
FB	AB3X2X3W Ferrite Bead
Dgs	18 V Zener Diode
Rg1	10 Ω
Rg3	0 Ω

The gate coupling networks used are based off of the work done in [34], [40], but, the gate coupling diodes were changed to transient voltage suppressing (TVS) diodes to provide more robust over-voltage protection. This was a concern because in a CSI the super-cascode will have to balance the voltages across the devices at the fundamental

frequency, not just during switching transients. Two P4SMA TVS diodes [43], one 376V diode and one 468V diode, in series are used in the coupling network clamping the JFET gate-drain voltage at 1kV. Across the gate-source pins of each JFET there is a 18V Zener diode. The Zener diode across the gate limits the negative gate voltage as well as establishing the bias current for the gate-coupling TVS diodes. To suppress high frequency ringing on the gate, small ferrite beads [44] are placed around the gate pins of the JFET. A summary of the devices with their respective reference designators is provided in Table 2-2. With twelve devices each limited to 1kV, a 12kV three terminal switch is realized, meeting the voltage requirement.

The packaging goals for the super-cascode were to have a reasonable mounting structure with a common heatsink for all devices. The ability to prototype the switch without needing a power-module manufacturing equipment was a requirement. The super-cascode developed here has 12 devices, which creates a packaging challenge, since the pads on the back of the TO-247 components are electrically connected to the drain of the device. The choice is to either have 12 independent floating heatsinks per super-cascode or electrical isolation between the devices and a large heatsink. The second approach of using a high voltage thermal interface pad was chosen for this implementation. To ensure good heat transfer to the pad and heatsink a structure was 3D printed. This structure mounts to the heatsink and applies pressure to the top of JFETs as shown in the cutaway of the stack-up in Figure 2-4.

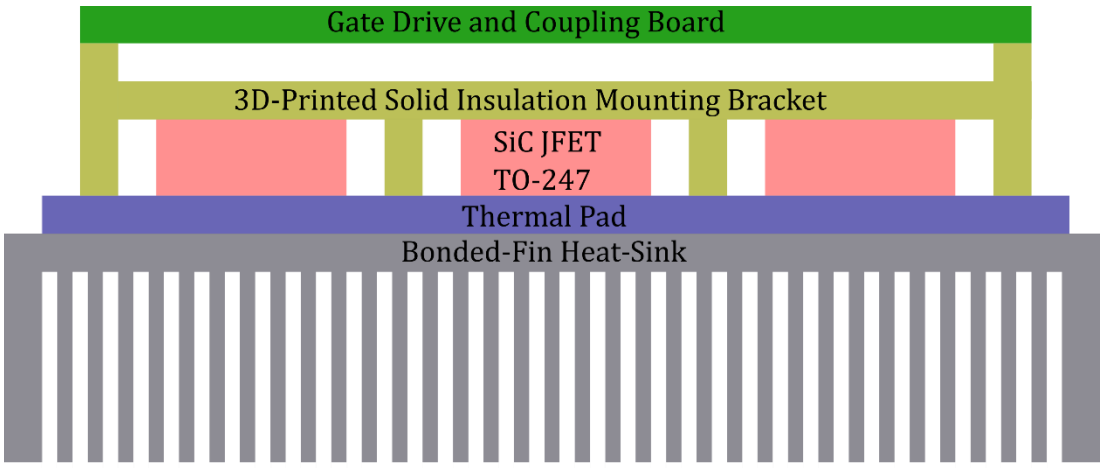

Figure 2-4. Cutaway of simplified super-cascode stackup.

A variety of different interface pads were surveyed, ranging from standard silicon pads, to isolating tapes shown in Table 2-3. The selected pad is an aero-gel pad from Taica North America and is 2mm thick and has 6.5 W/m-K thermal conductance and a 27.2 kV dc voltage rating [45]. Using equation (2-1, where k is the thermal conductivity of the pad and the device area is 322 mm^2, results in a thermal resistance for the pad of 1W/°C for each JFET for an overall junction to heatsink thermal resistance of 2.1W/°C per JFET. The thermal resistance is given per JFET because the switching loss is unbalanced and the worst-case losses for a single device are the limiting thermal factor.

$$R_{th} = \frac{l_{thickness}}{A_{dev} * k} \tag{2-1}$$

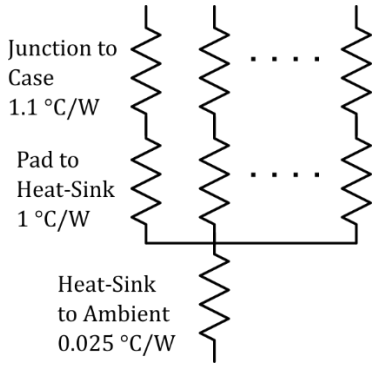

Figure 2-5. Super-cascode Thermal Circuit

Table 2-3. Survey of Isolating Thermal Pads and their performance

Pad Type	Mnfg	Part Number	k (W/(m-K))	Thickness (mm)	Dielectric Rating (kV/mm)	# layers	R_{th} (C/W)	Voltage Rating (kV)
Silicone Pads	3M	5591-25	1	2.5	8	1	7.8	20
	3M	5583S	1	1.5	8	1	4.7	12
	3M	5584	1.1	1.5	7	1	4.2	10.5
	3M	5595	1.6	1	8	2	3.9	16
	3M	5516	3.1	1	3.2	4	4.0	12.8
	3M	5516S	3.1	0.5	5.2	4	2.0	10.4
	3M	5519	4.9	1	4.9	3	1.9	14.7
	3M	5514	1.6	0.25	14	4	1.9	14
Tapes	3M	8926-05	1.5	0.5	15	2	2.1	15
	3M	8926-025	1.5	0.25	15	3	1.6	11.25
	3M	8940	0.4	0.19	33	2	2.9	12.54
	3M	8820	0.6	0.5	26	1	2.6	13
	3M	9882	0.6	0.5	30	1	2.6	15
Acrylic Interface Pad	3M	5570N	1.3	0.5	20	1	1.2	10
	3M	5571	2	1	13	1	1.6	13
	3M	5590H	3	1	33	1	1.0	33
	3M	5578H	3.5	1	16	1	0.9	16
Gel Pad	Taica North America	COH-4065LVC	6.5	1	13.6	1	0.5	13.6
	Taica North America	COH-4065LVC	6.5	2	13.6	1	1.0	27.2
	Taica North America	COH-4000LVC	6.5	2	12.5	1	1.0	25

2.3 Super-Cascode Testing

Six identical super-cascodes were built for integration into a 3-phase CSI. They were all tested for on-state and off-state characteristics and a separate one was built exclusively for dynamic characterization. The gate-coupling networks were changed on single (separate) super-cascode to compare the different gate coupling methods.

2.3.1 Static Characteristics

The super-cascode on-state characteristics at zero volts on the gate-source terminals of the controlled JFET, are shown in Figure 2-7. The super-cascode comes in just under 1 Ω of on-resistance with the gate driver disconnected, meeting the normally-on design requirement. Using a 10 kV hi-pot tester and a 6 ½ digit multimeter the drain-source off-state leakage and isolation to ground were tested. The overall low leakage currents for the six super-cascodes are shown in Figure 2-8 vs. applied terminal voltage. The sudden increases in leakage are due to the difference in leakage current from one JFET to the next. Since this super-cascode relies on the Zener and TVS networks to limit the device voltages, these effects are apparent. If resistors are used to diminishes the leakage resistance differences between devices in series these effects would not be seen, but the overall leakage current would be inherently larger. The device datasheet provides a wider range for leakages, but the ones assembled in the super-cascodes were of typical value or lower. To ensure the thermal pad had adequate voltage standoff, the six super-cascodes were mounted to a heatsink, and hipot-tested. Overall low leakage current (~2 uA) corresponding to high insulation resistance (5 GΩ) is shown for all six super-cascodes in Figure 2-9.

Figure 2-6. Top) Assembled Super-Cascode with mounting bracket, back and front views. Bottom) Super-Cascode with accompanying gate driver

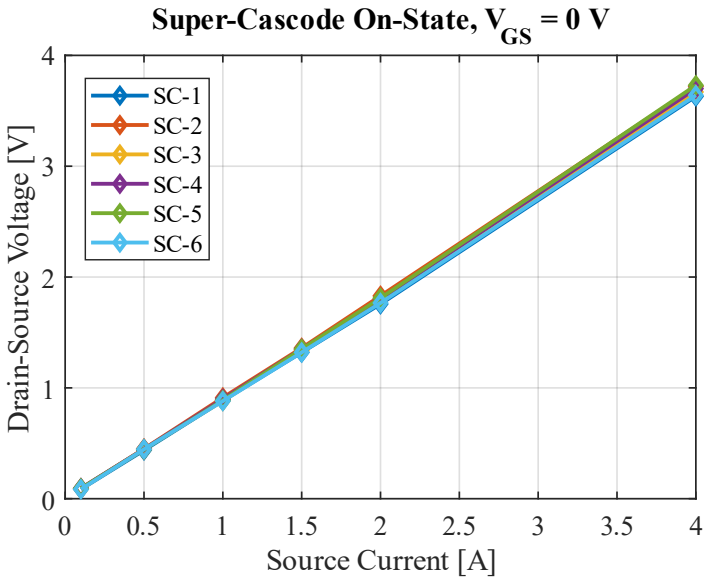

Figure 2-7. Measured On-State characteristics show casing normally-on behavior with zero gate-source voltage applied. Test data for six super-cascodes built at ambient temperature.

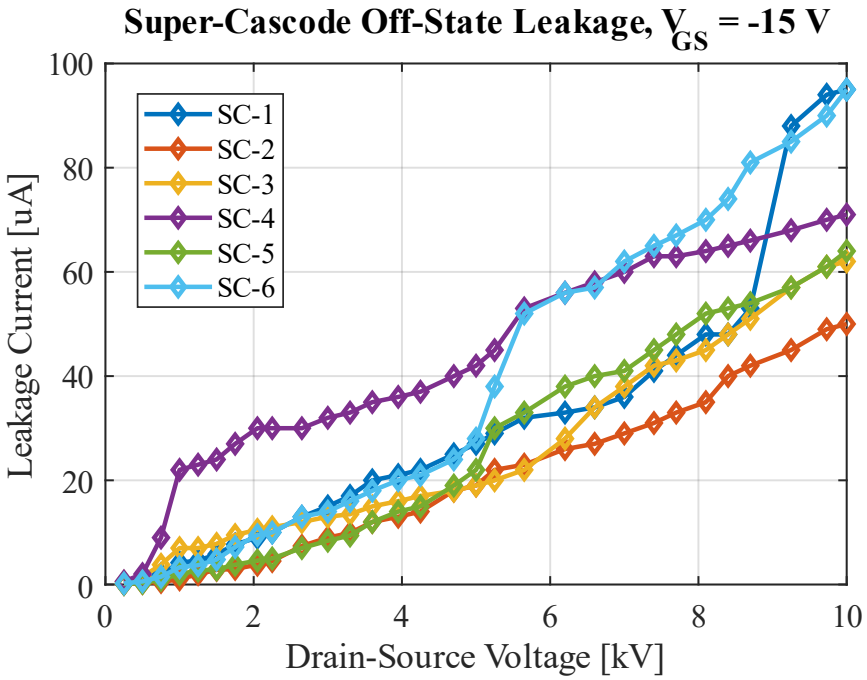

Figure 2-8. Measured leakage current of Super-Cascode in off-state across high voltage drain-source terminals of device. Characteristics of six super-cascodes built

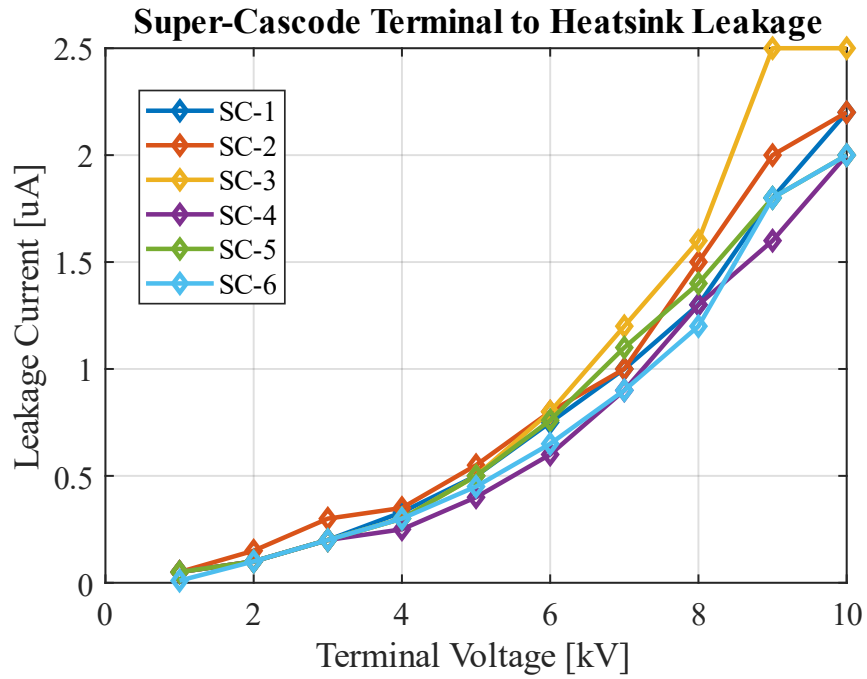

Figure 2-9. Measured leakage current to ground when mounted to heatsink with high voltage isolated thermal pad for six super-cascodes

2.3.2 Dynamic Characteristics

Switching performance for a single semiconductor switch is always difficult to determine. Modeling and datasheets provide means to estimate but there are always unknowns; for a super-cascode it becomes even more difficult. To determine which of the two selected gate coupling techniques would provide the best performance a clamped inductive load (CIL) test was done. Three implementations were tested, one with fixed 100 pF capacitance across each device as in [40], and two with scaling capacitances starting at 50 pF and 100 pF as determined in [34]. The diode used in the CIL is a 10kV diode from hvgtsemi [46]. Testing at 0.5, 1, and 2 amperes and 3, 5 and 7 kilovolts was performed to determine the performance over a wide operating range.

An example of the different effects the coupling network has on the waveforms is shown in Figure 2-10, where the scaling capacitor version speeds up the turn-on transition to the detriment of the turn-off transition. The extra capacitance takes longer to charge at turn-off, leading to the slower rise time but providing a faster turn-on.

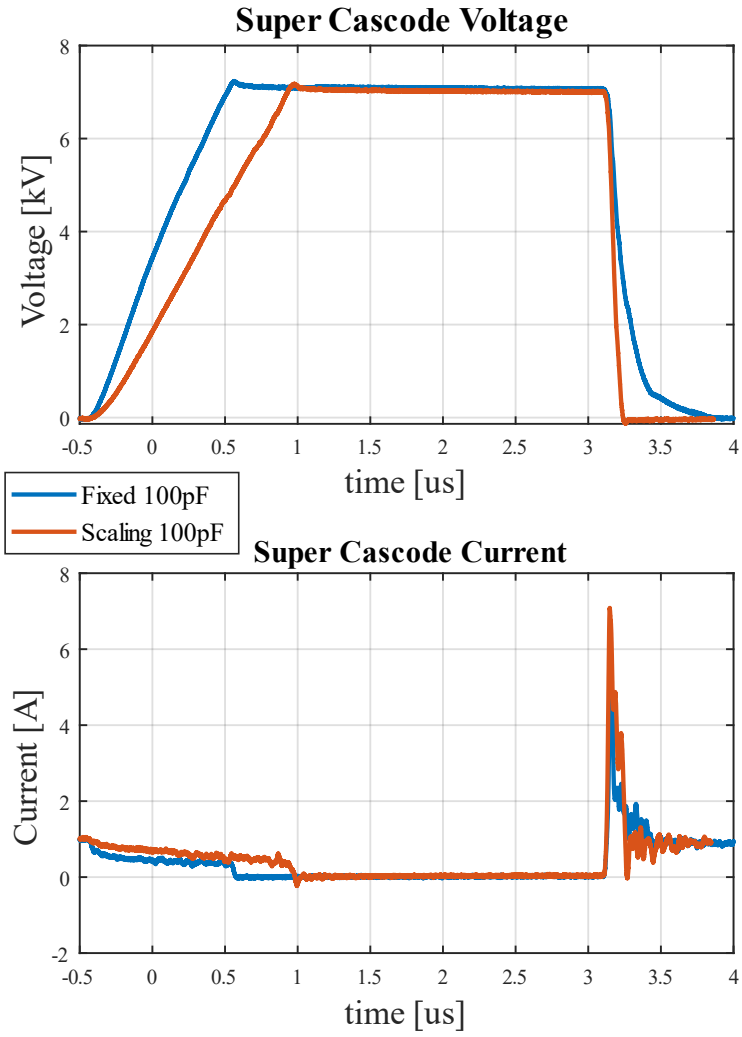

Figure 2-10. Measured waveforms of Super-Cascode showing effects the gate coupling network has on switching waveforms.

All three versions provided comparable performance and the breakdown of losses are shown in the following figures. The turn-on losses vs current in Figure 2-11 shows that the scaling capacitance provides a faster overall turn-on. However, as shown in Figure 2-10, adding this extra capacitance degrades the turn-off. Figure 2-12 shows the severity of this effect on the turn-off energy loss over all test-points. Finally, in Figure 2-13 we can see that the overall losses are negatively impacted by the additional capacitance that the scaling version requires.

The instrumentation and test equipment consisted of a 12-bit MDA800A oscilloscope, 100:1 4 kV GE3425 [47] and CP030 [48] current probe. The dc-link of the CIL was split such that the super-cascode switched from -3.5 kV to 3.5 kV, which allows the 100:1 probe to be utilized. Waveform analysis was carried out directly on oscilloscope and a DSP was utilized to provide the gate pulses.

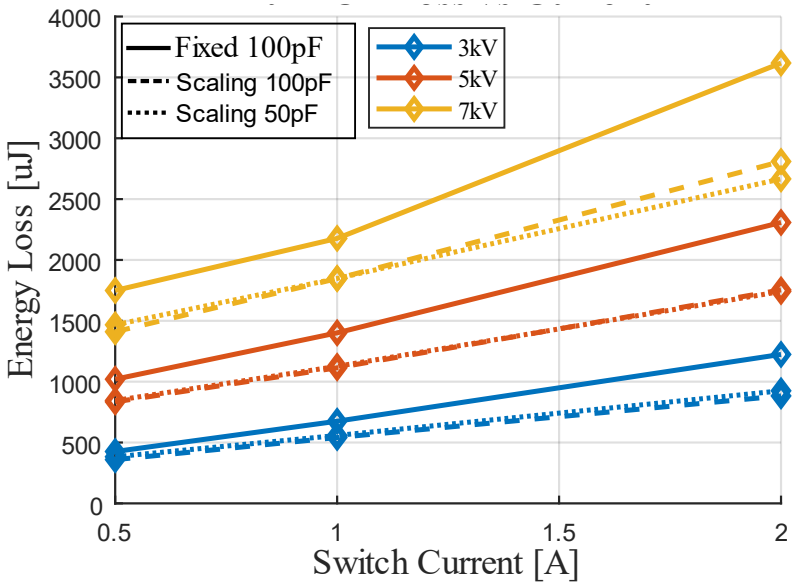

Figure 2-11. Measured turn-on switching loss in clamped inductive load

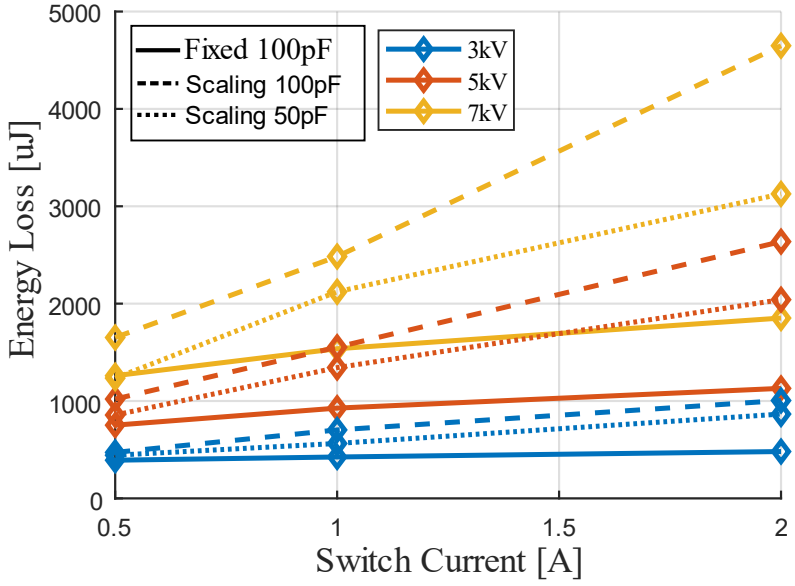

Figure 2-12. Measured turn-off switching loss in clamped inductive load

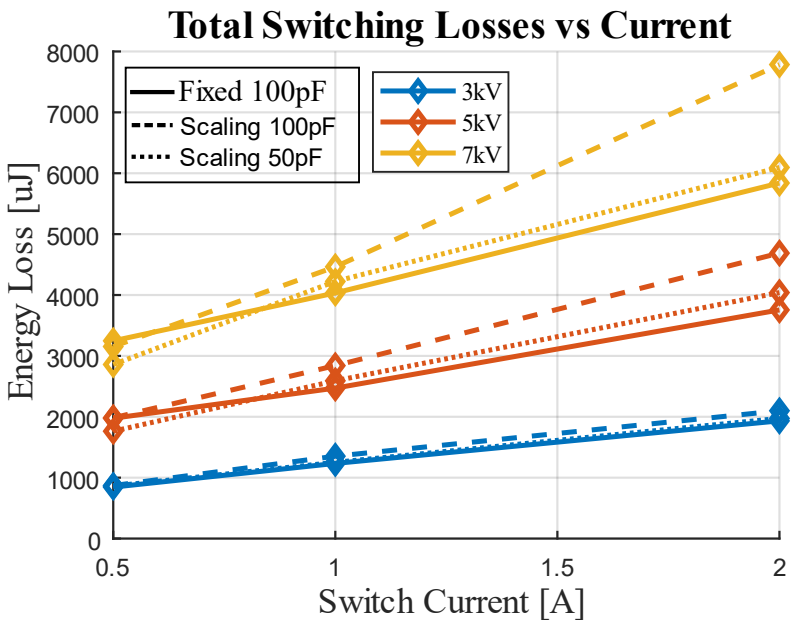

Figure 2-13. Combined measured turn-on and turn-off switching loss.

While overall low switching loss and fast transition are important for inverter performance, care must be taken to not over-stress an individual device in the super-cascode. If one of the JFETs in a super-cascode is experiencing significantly more loss than the rest, it will limit switching frequency or how much current the whole super-cascode can handle. To better understand the sharing, the cascode was divided into quadrants to identify how well balanced the different implementations are.

The tests were repeated at 7 kV and the voltage across every three devices was probed to determine the power loss per quadrant. Figure 2-14 shows that for all three implementations the bottom quadrant (first devices to receive gate signals) has the highest loss. It also showed that, in general, the top three devices are not being fully utilized and there still exists room for improvement.

The test was repeated at 7 kV but with the voltage probes on the bottom three devices (lower quadrant) to determine the limiting power loss for the super-cascodes. These results

are shown in Figure 2-15, where it is evident that for conditions other than the 0.5 A, the fixed 100 pF implementation provides the best solution. That implementation will minimize the overall switching losses of the super-cascode and the worst-case switching loss for a single device over a wide range of dc-link currents. The six super-cascodes used for the work in the following chapters utilize the 100 pF implementation.

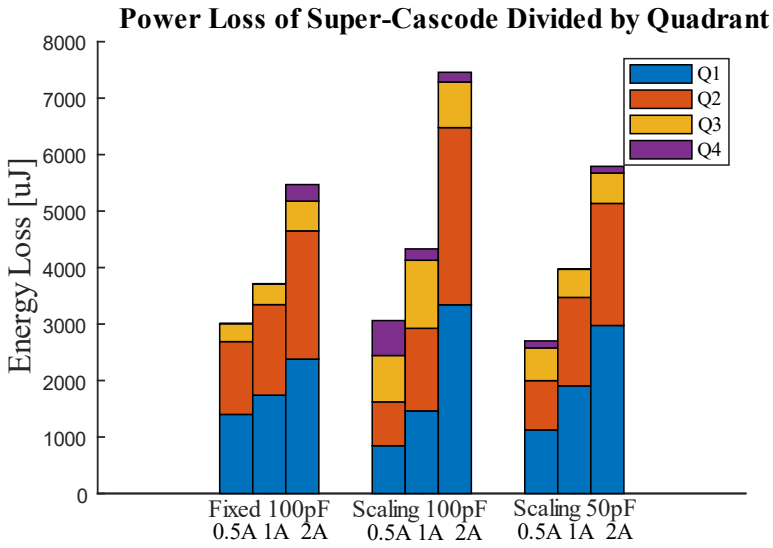

Figure 2-14. Measured switching loss in Super-cascode comparing the effectiveness of the different balancing networks. Divided by Quadrant to determine overall balancing, Q1 is considered the bottom 3 devices in series stack and for all balancing methods has the most loss.

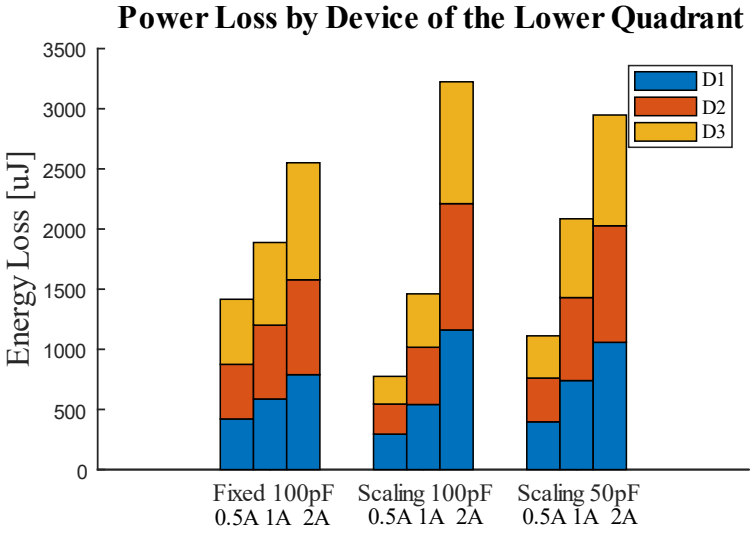

Figure 2-15. Measured switching loss in bottom 3 devices of Super-Cascode to show worst-case loss for the different balancing network. The lowest device in the stack has the highest loss, and the fixed capacitance method minimizes it as the current increases. Data shown here is for 7 kV dc-link

2.4 Chapter Summary

Chapter 2 focused on the development and design of a medium-voltage low-current high-speed JFET super-cascode. The previous work in super-cascodes was reviewed and two types of gate networks were tested for the voltage and current ratings of the SEM application. A key differentiator between previous work and the super-cascode developed was maintaining the normally-on nature of the JFETs. This is important as the eventual system implemented in later chapters uses a current source inverter where normally-on devices are preferred.

The dynamic characterization revealed the fixed capacitance method outperformed the scaling ones in terms of total losses over a wide range. Eventually the required dc-link current for this SEM was lowered to minimize system loss and the 50pF scaling option might be a suitable choice as well. However, the waveforms of the scaling capacitance in Figure 2-10 show the very fast turn on introduced by the scaling capacitance. As will be shown in *Chapter 5* and *Chapter 6*, the parasitic capacitance in the system is already causing high peak current due to the dv/dt produced by the fixed capacitance super-cascode. If the scaling capacitance were utilized, it would be crucial to investigate the potential negative effects introduced by the even faster edge rates.

The initial development of the electrostatic drive utilized a series stack of normally-off devices [49], [50]. These required an individual high voltage gate driver for each one, and even though there were only 4 devices for a 10kV switch, the overall implementation requires more volume as shown by side-by-side image of the two solutions in Figure 2-16

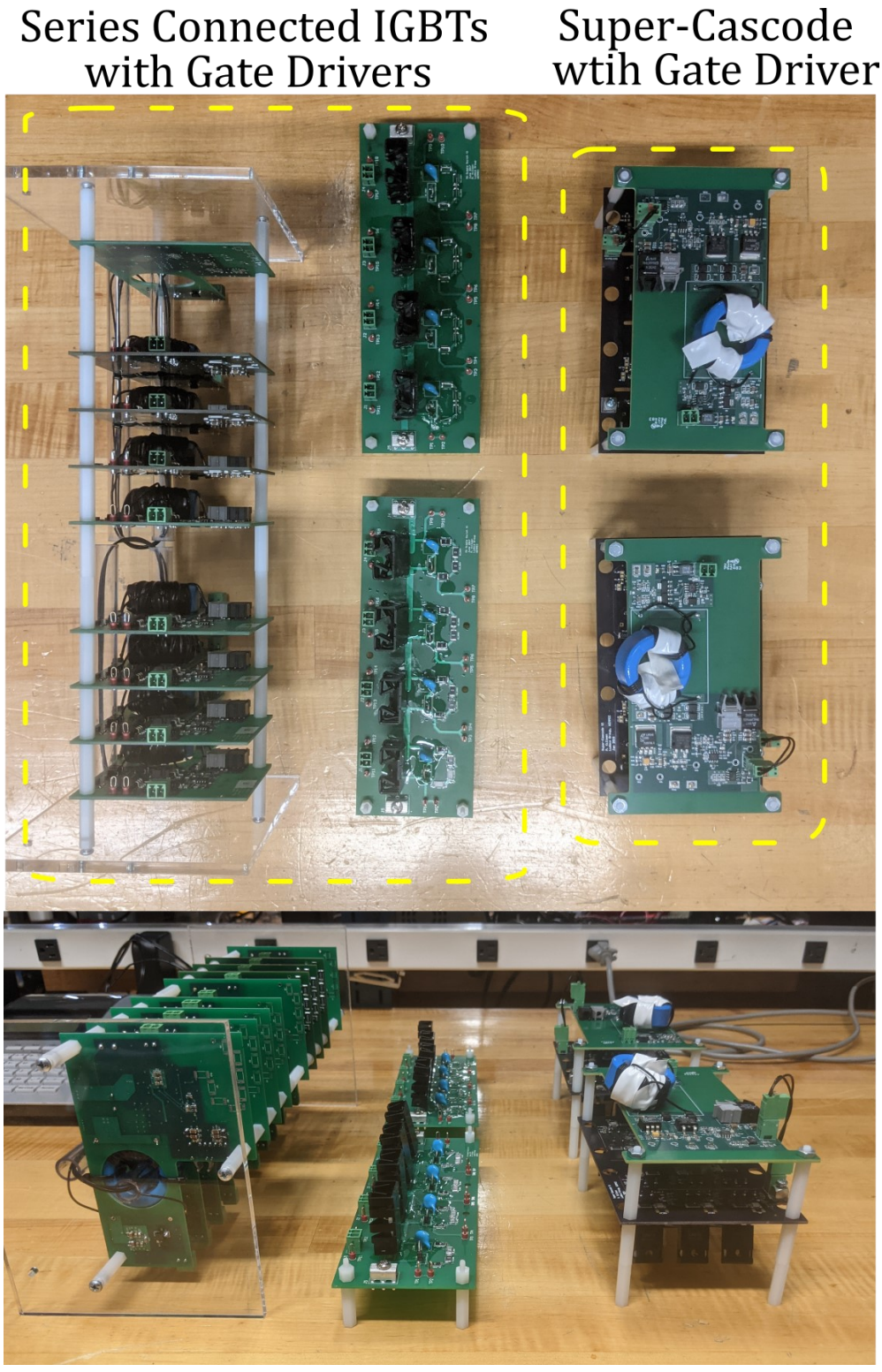

Figure 2-16. Side by side view of series connected IGBTs used in [49], [50] compared to super-cascode developed in Chapter 2

Chapter 3: Topology Evaluation for Variable Frequency Drives

This chapter evaluates the standard two-level inverter stages (VSI and CSI) as general-purpose variable frequency SEM drive candidates using the dynamic and static semiconductor characterization results from *Chapter 2*. Models of the semiconductors, electrostatic machine, and magnetic components were combined to perform a simulation-based comparison between the standard two-level voltage and current source inverter topologies. Designs for the necessary CSI dc-link and the VSI output filters are included in section 3.3 and the improved generalized Steinmetz equation algorithm from [51] was used to model magnetic core loss. A sweep of operating conditions consisting of various speeds, output voltages and dc-link voltage/currents were simulated, and the resulting losses and harmonic content are in section 3.4. Finally, the simulation results and implementation considerations are used for comparison between the two inverter topologies in section 3.5.

The comparison shows that the current source inverter is a better choice for a variable-speed drive with a wide operating range, especially at higher speeds. The voltage source inverter topology is speed limited due to the resonance between the inductive output-filter and capacitive machine. However, at low speeds, the VSI could provide higher efficiency (~90%) over a wide operating range, suitable for “position and hold” applications.

3.1 Inverter Models

A simplified CSI system topology is shown in Figure 3-1, including the dc-link inductor (L_{dc}) and semiconductors as the major loss components. The super-cascode developed in *Chapter 2* was designed for the medium voltage and low current requirements of an SEM drive. The diode utilized in the super-cascode characterization establishes reverse voltage blocking capability in the switches, as necessitated by a CSI.

The inductance value of the dc-link inductor pair is determined by the energy storage and peak-peak ripple requirements. Since the losses of the inductor depend on the input voltage waveform, a square wave voltage source emulating a generic switch-mode converter operating at the switching frequency of the CSI is used to provide the input power. Minimizing switching ripple content reduces core loss and enables the modulator and machine controller to be modelled as linear systems at power frequencies for control purposes. Additionally, the inductor must be sized to handle system load transients without dropping too low in current or saturating. To minimize this constraint, *Chapter 4* investigates dc-link control methods necessary to avoid increasing the dc-link inductance.

Since the topology evaluation includes a variable dc-link, the inductor must provide minimal current ripple at the low current (lowest energy storage condition) while not saturating or incurring significant loss at the higher current levels. When operating at 18kHz switching frequency, a 4 H dc-link inductance is required to maintain the current ripple below 10% peak-peak across all operating points. Despite this seemingly large value, at the low current level of 800 mA only 1.3 J of energy is stored. In Figure 3-1-A the inductance is split between two, 2 Henry inductors and the details on the design and loss modeling of these inductors are in subsection 3.3.

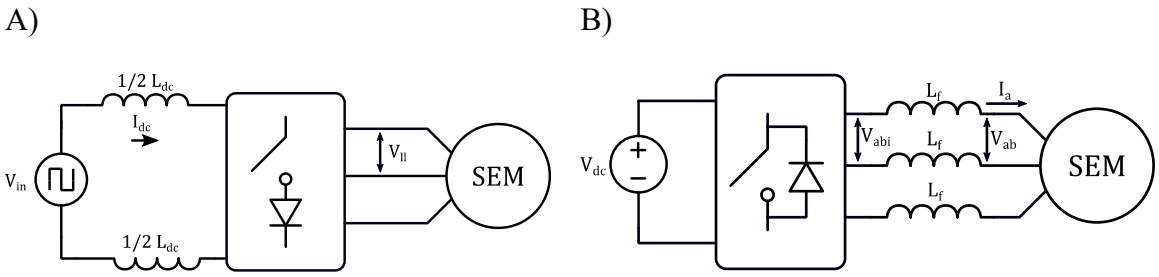

Figure 3-1 Simplified simulated system diagrams CSI (A) and VSI (B)

When connecting a VSI system to the SEM an inductive output filter is required to match the machine capacitive terminals to the PWM voltage output of the VSI. The value of inductance, L_f, in Figure 3-1-B, is critical in providing sufficient line impedance to prevent current inrush on the phase capacitance and must be chosen carefully to avoid resonance in the system. The dc-link capacitor is omitted since capacitor losses are generally significantly lower than inductor and semiconductor losses. The super-cascodes from *Chapter 2* are capable of reverse conduction so synchronous switching is assumed and diode conduction losses during dead time are not included for model simplicity.

Table 3-1 summarizes the losses included in each system evaluation. The details of the component model for the semiconductors are presented in *Section 3.2* followed by the dc-link and output inductor designs in *Section 3.3*.

Table 3-1. Summary of losses modelled, and method used

Super-Cascode Conduction	On-resistance in simulation
Super-Cascode Switching	Lookup table with interpolation between data-points
Diode Conduction	Forward voltage and on-resistance in simulation. Not included in VSI system since synchronous switching of super-cascode used.
Inductor Conduction	Linear resistance in simulation
Inductor Core Loss	Post-processed with iGSE algorithm and datasheet parameters

3.1.1 VSI Output Filter Resonance

The necessary line inductors in a VSI and SEM system create a second order L-C filter with the machine terminals. To avoid resonances the filter must be placed below the high frequency harmonic content from the PWM switching frequency and above the fundamental frequency. A regularly sampled SVPWM scheme introduces non-negligible harmonics of the fundamentals, which is exasperated by the low switching to fundamental frequency ratio [37]. The traditional VSI implementation with an electromagnetic machine does not encounter these harmonics resonance issues the first order R-L filter presented by the machine and generally are not a problem unless the ratio of switching to fundamental frequency becomes low.

However, with the L-C filter needed for an SEM system these harmonics can be amplified creating large currents, incurring losses, torque ripple, and potentially saturating and damaging the line-filter and machine. As it will be shown in section 0, the switching loss is a dominating loss in the system so increasing the switching frequency above 18 kHz is not desirable. This results in each inductor design imposing a maximum speed on the machine to limit harmonic problems. The resonance issues of the VSI driven SEM systems are the dual of issues encountered by magnetic machines driven by CSIs. However, modern switches capable of operating in at 100 kHz or above enable the use of CSI for magnetic machines [52], [53].

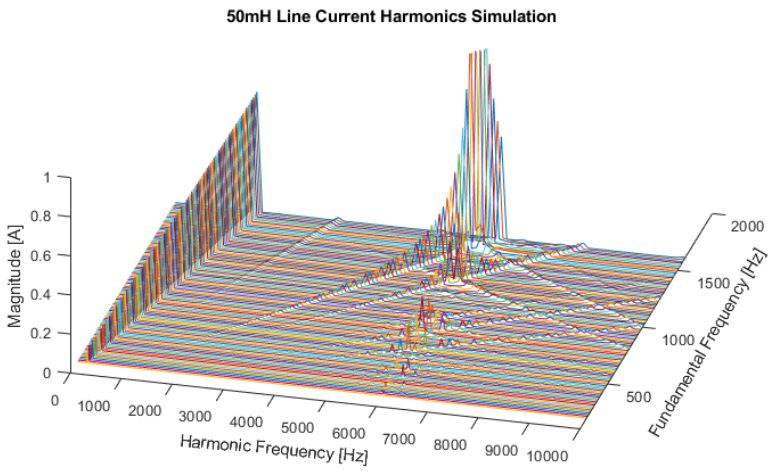

Figure 3-2. Line Current Harmonics of VSI with 50mH output inductor (Filter 1)

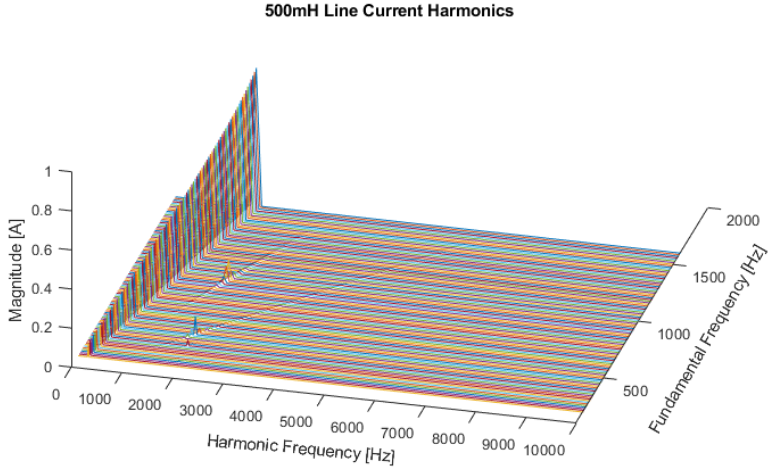

Figure 3-3. Line Current Harmonics of VSI with 500mH output inductor (Filter 2)

To understand this VSI inductor design problem, two inductor values are utilized. Filter 1 was sized at 50 mH which creates a resonant point at 6 kHz. Filter 2 was sized at 500 mH which creates a resonant point at 1.9 kHz. An initial simulation sweep focused on revealing the resonance issues and the harmonic spectrum for the phase current versus fundamental frequency are shown in the waterfall plots of Figure 3-2 for filter 1 and Figure 3-3 for filter 2. A series line resistance of 50 Ω was included in these simulations to provide some damping. The resonance issue becomes severe for the 50 mH inductor when the harmonics of the fundamental and harmonics of the switching frequency are amplified together. This

occurs above 1000 Hz fundamental which corresponds to 625 RPM in this example. The second filter option with the lower frequency cut-off removes much more of the switching frequency harmonic content, resulting in much lower total harmonic distortion (THD) in the current waveforms. However, amplification of the fundamental starts to occur as speed increases, so the maximum fundamental frequency for this design is set where the filter gain is 1.05 V/V. This occurs at 400 Hz corresponding to 250 RPM.

3.2 Semiconductor Models

The super-cascode from *Chapter 2* has twelve 80mΩ JFETs connected in series and utilizes a passive gate network to control the switching transitions of the series-stack of devices. Different gate-network designs were evaluated and the data for the fixed-capacitance gate-network is utilized for this study. The data used to create loss models for the switches in PLECs and the turn-on and turn-off look-up tables are shown in Figure 3-4. The diodes in the switching events contribute reverse-recovery losses since silicon diodes were utilized in the clamped inductive load (CIL) and those losses are included in the turn-on look-up table. The super-cascode while in the on-state conducts current bidirectionally and is modelled as a 1 Ω resistor. The diode model utilizes the basic forward voltage and on-state resistance. The on-sate loss parameters for the semiconductors are summarized in Table 3-2.

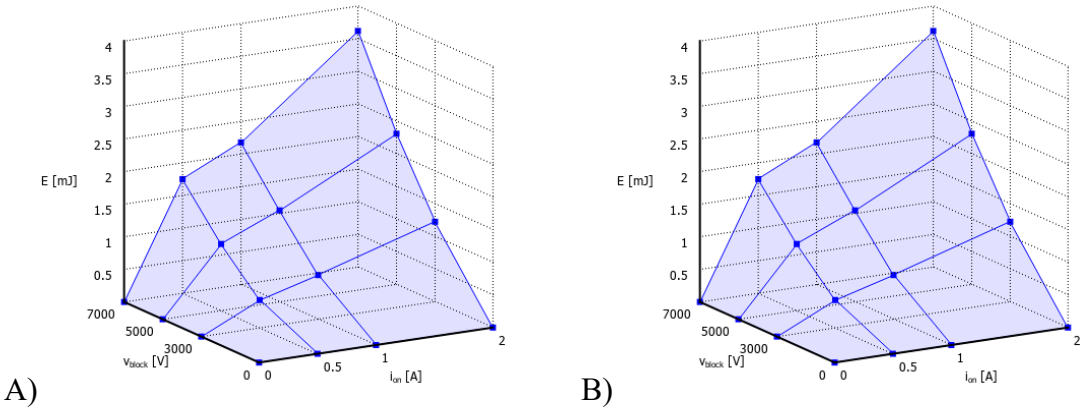

Figure 3-4. Super-Cascode Turn-On (A) and Turn-Off (B) Switching Energy Lookup Table

Table 3-2. Semiconductor Static Characteristics

Symbol	Parameter	Value
$R_{on,\,SC}$	Super-Cascode On-Resistance	1Ω
$R_{on,\,D}$	Diode On-Resistance	3 Ω
V_{fw}	Diode Forward Voltage	7 V

3.3 Magnetic Design and Modeling

The design of inductors for the two systems utilized the area product approach for core selection and the general design rules from [54]. This method allows for rapid iteration of designs providing a reasonable approximation of the inductors including weight, volume, copper loss and core loss. MetGlas amorphous metal 2605SA1 [55] was selected for the dc-link inductor. This core material has a peak flux density between 1.4~1.6 T, and thin laminations allow for high frequency flux ripple. The flux ripple must be kept low (0.1~0.3 T), which aligns with the low dc-link current ripple requirements.

The MPP powder core from Mag-Inc was selected for the VSI output filters [56]. The ac flux ripple consists of the fundamental component and the PWM harmonic content, making the low core loss of the MPP construction a good choice. The peak current requirements for the two filter designs were obtained from the initial frequency sweep that

determined the maximum operating frequency for each design. Table 3-3 summarizes the inductor design specifications.

Table 3-3. Target Inductor Specifications

Inductor	Inductance [H]	Core Material	Core Shape	Operating Peak Flux Density [T]	Operating AC Flux Density [T]	Peak Current [A]	Number of Inductors Per System
dc-link	2	2605SA1	CC	1.2	0.12	0.84	2
Filter 1	0.05	MPP	Toroid	0.2	0.2	1.1	3
Filter 2	0.5	MPP	Toroid	0.2	0.2	0.2	3

To guide a designer on appropriate core selection, [54] provides a utilization factors to ensure enough window space for winding and an appropriate conductor current density are selected. Table 3-4 summarizes the values used here. The wire insulation factor for the filter designs is lower due to the lower RMS current allowing for smaller wire gauge. The smaller wire gauge has a higher proportion of insulation to copper area leading to a poor S_1 factor. Since the inductors are all required to block medium voltage quad-coated magnetic wire was selected. The insulation factor S_4 was set to 0.5 which corresponds to half the winding area after factors S_1, S_2 and S_3 are accounted for. This is reserved for insulation, specifically winding-to-core and layer-to-layer to support the medium voltage.

Table 3-4. Winding Area Utilization Factors

Inductor	Wire Insulation Factor S_1	Fill Factor S_2	Usable Window Area S_3	Insulation Factor S_4	Overall Window Utilization K_u	Current Density J [A/cm^2]
dc-link	0.756	0.9	0.75	0.5	0.255	300
Filter 1	0.662	0.9	0.75	0.5	0.223	300
Filter 2	0.574	0.9	0.75	0.5	0.194	300

Utilizing the design specifications and utilization factors the three inductors were designed and are summarized in Table 3-5. The low RMS current requirement of the designs lead to wire selection in the 22 to 30 AWG size, lessening the impact of skin

effects. Considering the high-level design comparison goal of this paper, only a linear resistance was utilized for copper loss while proximity effects were neglected.

Table 3-5. Inductor Design Summary

Inductor	Core Number	# Turns	Gap or permeability	Wire Gauge [AWG]	DC Resistance [Ω]	Core Volume [cm^3]	Core Weight [Kg]	Window Utilization K_u	AC Flux [T]
dc-link	AMCC-125	1029	0.24mm	22	8.6		1.166	0.16	0.045
Filter 1	0055909A2	1622	$14u_o$	26	23.9	43.4	0.339	0.11	0.15
Filter 2	C055192A2	2006	$60u_o$	29	58.1	28.6	0.23	0.19	0.23

The magnetic core losses are post-processed in MATLAB from the time-domain flux waveform, B(t), determined from the current waveform, i(t), via equations (3-1) and (3-2). Where N is the number of turns, l_m and l_{gap} in cm, are the magnetic path length and gap-length, respectively.

$$B_{MetGlas}(t) = i(t)\frac{0.4\pi N}{l_{gap}+l_m/u_r}10^{-4} \text{ [T]} \tag{3-1}$$

$$B_{MPP}(t) = i(t)\frac{0.4\pi N u_r}{l_m}10^{-4} \text{ [T]} \tag{3-2}$$

The core loss density is calculated from the time domain flux waveforms utilizing the improved generalized Steinmetz equation (iGSE) algorithm [51] with code provided from magnetic design group at Dartmouth [57]. This method provides a balance between readily available core information from manufacturers (k, α and β of the Steinmetz's equation (3-3)) and accuracy of losses. The manufacturer provided frequency parameters α assume the frequency input f is in kHz and the power density calculations from (3-3) have various units while the iGSE code assumes MKS units. The k parameter is modified per (3-4) to account for the kHz conversion. The core loss calculations for the MetGlas material are also divided by 1000 to correct power density scaling (i.e. mW vs W). With these modifications the provided code from [57] reproduces the datasheet curves for single frequency sinusoid waveforms in [55], [56] but are not included here. Additionally, only a single set of parameters can be input to the algorithm for a given flux waveform. To

determine when the high vs low frequency parameters should be used the frequency of the dominant waveform harmonic was selected.

$$P = kf^{\alpha}B^{\beta}\ ,\ \left[\frac{W}{volume}\right] or\ [\frac{W}{mass}] \tag{3-3}$$

$$k_n = k10^{-3\alpha} \tag{3-4}$$

Table 3-6. Parameters for core loss

Material	k	k_n	α	β
MetGlas 2605SA1	6.5	1.918E-4	1.51	1.74
MPP 60u (F<10 kHz)	80.12	6.078E-2	1.04	1.585
MPP 60u (F>10 kHz)	31.32	2.431E-3	1.37	1.585
MPP 14u (F<10 kHz)	64.02	2.994E-2	1.11	1.074
MPP 14u (F>10 kHz)	21.06	1.526E-3	1.38	1.074

3.4 Simulation Results

The CSI and VSI systems modelled in the previous section were evaluated over the full torque-speed range of each system. Additionally, the dc-links for both systems were varied. When sweeping the dc-link in the CSI, a maximum duty ratio of 95% was utilized when determining if a given operating point is achievable for a given dc-link. When the dc-link voltage was swept in the VSI system, a voltage value of 500 V above the peak line-to-line voltage operating point was used. Table 3-7 summarizes the operating points evaluated for all three systems. The efficiency of the CSI over the simulated operating range is shown in Figure 3-5. Figure 3-6 shows the efficiency of the VSI systems for various line-neutral voltages at the maximum dc-link voltage. The efficiency of the VSI system at reduced line-neutral voltages with varying dc-link is shown in Figure 3-7. The harmonics content of the VSI and CSI system is summarized in Table 3-8.

Table 3-7. Operating Conditions Evaluated

System	Fundamental Frequency	Mechanical Speed	dc-link	Peak Line-Neutral Voltage	Switching Frequency
CSI	10 → 2000 Hz	6 → 1250 RPM	200 → 800 mA	1 → 4 kV	18 kHz
VSI, Filter 1	10 → 1000 Hz	6 → 625 RPM	2.2 → 7.4 kV	1 → 4 kV	18 kHz
VSI, Filter 2	10 → 400 Hz	6 → 250 RPM	2.2 → 7.4 kV	1 → 4 kV	18 kHz

Table 3-8. CSI and VSI systems metrics vs frequency

		Electrical Frequency [Hz]	10	40	80	180	400	600	800	1000	1500	2000
		Speed [RPM]	**6**	**25**	**50**	**113**	**250**	**375**	**500**	**625**	**940**	**1250**
CSI [1] dc-link current ripple [%]		200 mAdc	1.26	3.22	4.50	4.40	10.2					
		800 mAdc	0.18	0.28	0.38	1.49	0.97	0.97	1.16	1.43	2.59	5.43
VLL THD [%]	**CSI [1]**	200 mAdc	0.20	0.43	0.76	1.18	2.00					
		800 mAdc	0.51	0.63	1.09	1.94	3.67	4.98	6.06	6.98	8.31	11.87
	Filter 1 50 mH [2]	Vln = 2 kV Vdc = 4kV	5.74	4.45	4.47	4.51	4.66	6.23	7.58	5.25		
		Vln = 4kV Vdc = 7.4kV	5.85	4.61	4.62	4.66	4.84	6.56	8.06	5.49		
	Filter 2 500 mH [2]	Vln = 2kV Vdc = 4kV	5.59	0.40	0.40	0.48	0.92					
		Vln = 4kV Vdc = 7.4kV	5.59	0.41	0.42	0.51	1.03					
VSI Phase Current THD [%]	**Filter 1 50 mH [2]**	Vln = 2kV Vdc = 4kV	5618	1780	893	430	187	131	103	77		
		Vln = 4kV Vdc = 7.4kV	6380	1989	989	474	206	147	116	85		
	Filter 2 500 mH [2]	Vln = 2kV Vdc = 4kV	900	163	84	39	17					
		Vln = 4kV Vdc = 7.4kV	1027	181	92	43	19					
VSI RMS Phase Current [mA]	**Filter 1 50 mH [2]**	Vln = 2kV Vdc = 4kV	113	109	109	112	124	142	165	182		
		Vln = 4kV Vdc = 7.4kV	224	215	215	220	240	272	312	334		
	Filter 2 500 mH [2]	Vln = 2kV Vdc = 4kV	18	12	15	27	59					
		Vln = 4kV Vdc = 7.4kV	36	22	29	49	106					

(1) For the CSI system the peak Line-Neutral Voltage shown at rated condition (4kV) for both 200mA and 800mA

(2) For the VSI system the dc-link is set to the required voltage for the given line-neutral voltage

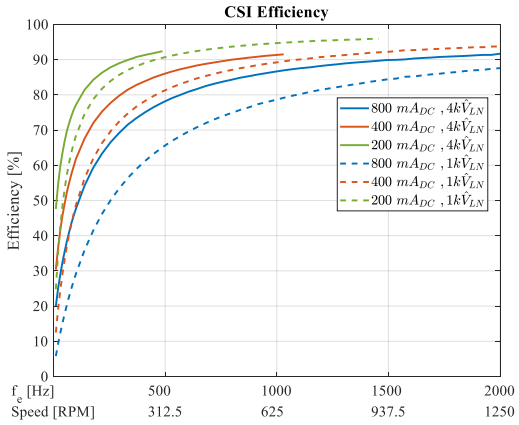

Figure 3-5. CSI Efficiency vs dc-link current and line-neutral voltage

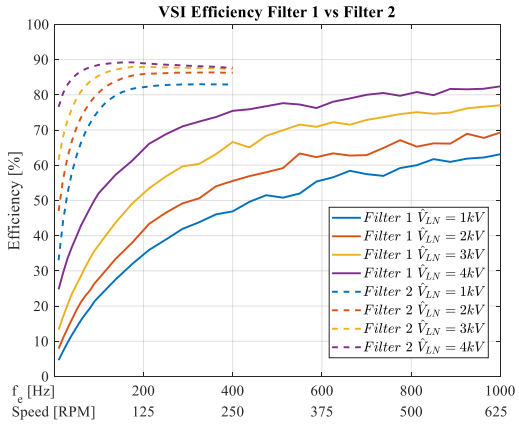

Figure 3-6. VSI Efficiency vs line-neutral voltage with Filter 1 and Filter 2 at 7.4 kVdc

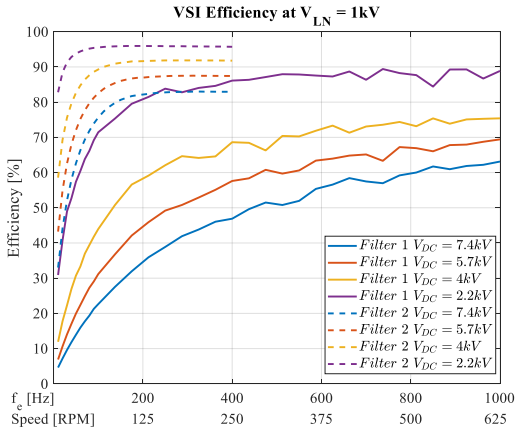

Figure 3-7. VSI Efficiency at low output voltage with variable dc-link voltage

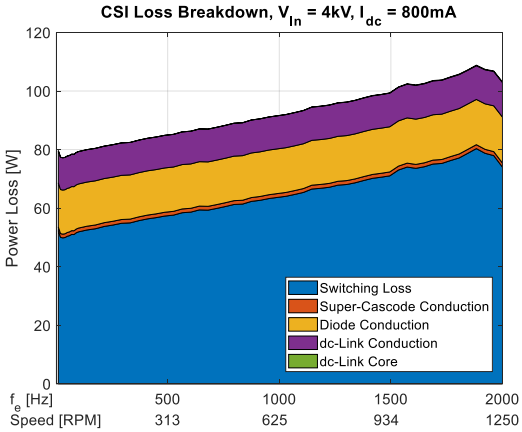

Figure 3-8. CSI system loss breakdown at rated output voltage and dc-link

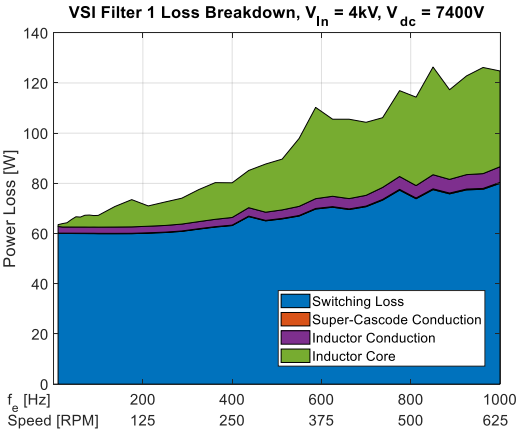

Figure 3-9. VSI system loss breakdown with Filter 1 (50mH) at rated output voltage

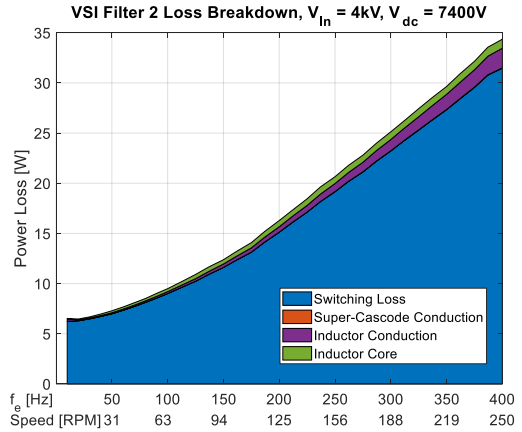

Figure 3-10. VSI system loss breakdown with Filter 2 (500mH) at rated output voltage

3.5 Discussion

A CSI and two VSI systems were modelled and simulated to understand the performance tradeoffs between the two topologies. The VSI requires an output line inductance that limits the maximum achievable speed due to resonance of the PWM content and second order filter created by the line inductance and machine capacitance. Filter 1 was designed to minimize the inductor size and push the speed of the VSI. Filter 2 was designed to avoid resonances and minimize the harmonic content of the system. The high-level efficiency and impacts the filter design have on efficiency are discussed in the following sub-sections. Additionally, a few practical implementation considerations are discussed along with the limitations of the modeling.

3.5.1 Performance Comparison

The simulation results showed that it is possible to achieve high electrical efficiency utilizing either the VSI or CSI systems under the right conditions. The CSI is shown to achieve high efficiency (>90%) at high torque as the speed increases in Figure 3-5. The efficiency can be improved at low speed by utilizing a variable dc-link current for both low torque and/or low speed operating points. The impact of the filter design on the efficiency of the VSI system is clear in Figure 3-6. The Filter 1 configuration had a peak efficiency of 82% at rated conditions and it never achieved efficiency above 90% at any operating point, even with a variable dc-link (Figure 3-7). While the VSI system with Filter 2 does not achieve 90% efficiency at rated dc-link it does have a good efficiency (>85%) at rated Torque over most of its operating speed range. However, Figure 3-7 shows that if a variable dc-link is utilized the efficiency at lower torque is sustained above 90% for the majority of the speed range.

The component loss breakdown of each system at their rated dc-link and torque provides a clear understanding of what is determining the system efficiency. In Figure 3-8 the losses of the CSI system start high at 80 W, and only increase by ~30% to 105 W over the full range. This is driven by the fixed dc-link current and output-voltage leading to high switching loss over the full range. By reducing the dc-link current the switching losses and dc-link losses are directly reduced, increasing the efficiency at lower speed and lower torque.

The effects the filter designs in the VSI system have on efficiency is understood from the RMS line-current and THD values in Table 3-8. The higher frequency crossover of Filter 1 did not sufficiently filter the PWM voltage waveform leading to high frequency harmonic phase currents at all operating points. This drives up the switching loss and inductor loss components in the loss-breakdown of Figure 3-9. The losses start high, 60 W, and are doubled to 120 W at the maximum speed of the system, which is only the mid-point of the CSI speed range. However, when the 500 mH inductor (Filter 2) is utilized Table 3-8 shows the harmonic content is more filtered leading to a phase current that is more dependent on the fundamental component. The loss breakdown for the VSI system with Filter 2 in Figure 3-10 shows that the reduced high frequency component reduces the semiconductor and core losses significantly. This results in the system starting at 7 W at 10 Hz (6.25 RPM) and since the losses are now heavily speed dependent, they increase by 5x to 35 W at max speed of 400 Hz (250 RPM).

3.5.2 Modeling Limitations

There are some limitations with the modeling of the super-cascode. A lack of switching loss data in the 100 mA to 500 mA results in the model linearly scaling the switching loss down to 0 J. However, due to the effective drain-source capacitance of the super-cascode there will always be a minimum switching energy. This limitation effectively lowers the simulated losses of the CSI at low dc-link currents and of the VSI systems at low fundamental frequencies.

When considering loss models for the inductors, due to the purely high-level paper design a few difficult to estimate components were not modelled. The inductors (both dc-link and filter inductors) are high turn-count, high inductance designs. The high turn-count likely requires multiple layers leading to increased proximity effect losses that were not included. Additionally, the parasitic capacitance incurred from the multiple layer windings could limit the effective frequency of an inductor.

3.5.3 Implementation Considerations

Careful consideration for the cooling of the super-cascodes is essential. Adding parasitic capacitance between device and heatsink, and between super-cascodes in the inverter would increase switching loss. Using thermal pads with low permittivity or utilizing ceramic heatsinks should be considered to minimize this effect.

Additional analysis and optimization of the inductors is required to minimize the parasitic capacitance and proximity effects in practice. Moving to multiple series connected inductors may ease inductor design in several ways. 1) The voltage isolation for an individual inductor would be reduced. This allows for higher window utilization and smaller cores. 2) Parasitic capacitance of each inductor would be in series with the next

inductor which reduces capacitances. 3) Smaller cores with lower layer count could have lower proximity effects and core loss.

If fault tolerance is a concern when considering core materials for the CSI dc-link inductor, utilizing a powdered core would provide some over-current ride-through capability. A gapped design, like the one used in this study, limits the fault tolerance of the dc-link. During an over current condition, the dc-link could saturate, and the inductance will collapse leading to a system fault. If a powdered core inductor were utilized, the distributed air gap would provide soft saturation and a gradual inductance roll-off, thereby reducing the impact of transients.

3.6 Chapter Summary

The CSI and VSI topologies were modelled and simulated with attention towards semiconductor and magnetic core losses in prospective electrostatic drive systems. It was shown that the CSI is a good option for higher-speed applications. Additionally, if a variable dc-link is implemented the CSI can provide high efficiency (>90%) over a wide operating range. The VSI system is speed limited due to resonance of the output filter and requires a higher ratio of switching frequency to fundamental frequency. It should be noted that in applications utilizing current source inverter for magnetic machines, the resonance between an output filter and machine is also encountered. Control methods using virtual resistance have been used to damp this resonance in current source rectifiers [58, Ch. 11] and are being explored in research for motor drive applications [59]. The switching loss was shown to be the largest loss component in all systems and therefore imposes a practical maximum speed for the VSI with a given semiconductor switch. With proper filter design

that reduces the switching frequency content of the line-currents the VSI losses become speed dependent, allowing higher efficiency than the CSI at lower speeds.

Overall, this simulation study has shown the dominant loss in the system is driven by a high switching frequency requirement. This switching frequency requirement is driven by the relatively high fundamental frequency resulting from the high pole-count (P = 96) of the machine. If the speed of the machine were limited it would be recommended to use the CSI with the lowest possible switching frequency with a variable dc-link current to retain the high electrical efficiency that a synchronous electrostatic machine can provide. Conversely, the CSI dc-link introduces inherent conduction losses that would impact position and hold drives, resulting in the VSI being the recommended topology for those applications. A summary of the inverter application matrix is shown in Table 3-9.

Table 3-9. Inverter Topology Application Matrix

Application	**VSI**	**CSI**
Position and Hold	Yes	No
Low Speed Only	Yes	Yes
Wide Speed Range	No	Yes

Chapter 4: Current Source Inverter Theoretical Development

The evaluation of the common two-level inverter topologies in *Chapter 3* found the current source inverter to be suitable for a general-purpose variable frequency drive with reduced dynamic complexity when compared to a VSI with an output filter. However, *Chapter 3* focused on the performance of the inverter stage but neglected several important system level challenges consisting of:

1) Matching the high impedance motor to low impedance power sources, e.g. LV mains
2) Regulating the dc-link current, i.e. there is no natural current source

Chapter 4 addresses these challenges by analyzing a cascaded power topology consisting of an isolated full-bridge regulating the dc-link current, followed by the current source inverter regulating the terminal voltage and torque of the SEM. The following sub sections derive the dynamic model of the system suitable and two dc-link controllers are proposed.

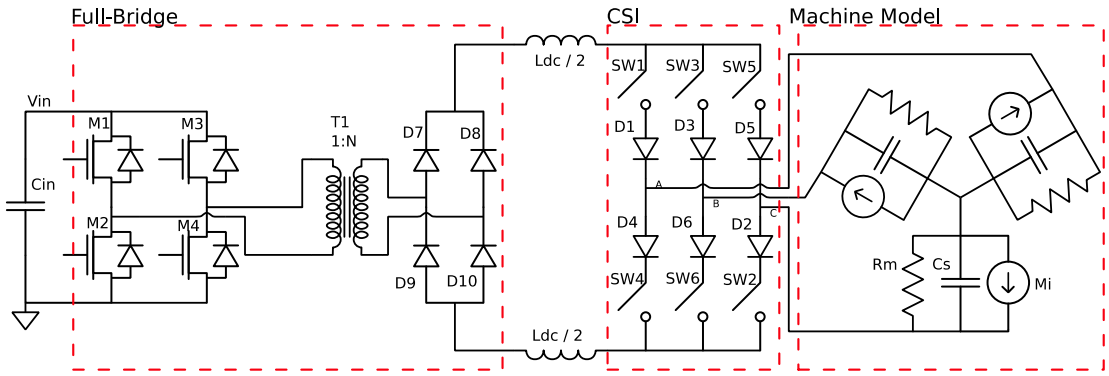

Figure 4-1. Current source drive with isolated full-bridge front end

One of the purposes of this work is to explore the challenges associated with driving a medium-voltage low-current SEM from a low-voltage power source. Traditionally, the

voltage level in power systems is increased to reduce conduction loss, most notably in power transmission and distribution. However, as the electrical energy approaches the point of load it is stepped down in voltage to match the lower impedance of loads. Since the SEM is a primarily a low-speed torque-producing machine, it is in a non-traditional operating space that requires medium-voltage with comparably very low power requirements i.e. it has high impedance. When the SEM is operated at 400 RPM at rated torque the output power is 375 W, i.e. orders of magnitude below the power levels associated with conventional medium-voltage power distribution or drives. Therefore, this implementation uses an input voltage of 280 Vdc which is derivable from standard low-voltage 3-φ sources.

The low input voltage to the system introduces the requirement of providing approximately 25 V/V gain between the input voltage and the SEM 7 kV peak line-line voltage. Current source inverters are derived from the boost converter and provide inherent voltage gain. However, utilizing the CSI for voltage gain requires increasing the dc-link current, which as shown in *Chapter 3*, has a significant impact on semiconductor losses. Therefore, in this implementation the front-end is a full-bridge isolated converter that can provide significant voltage gain via a transformer as shown in Figure 4-1 and regulate a variable dc-link to reduce losses. This topology allows the front-end devices to have low-voltage ratings, thus reducing the size and cost while increasing performance. The diode-rectifier stage limits the drive to two-quadrant (motoring) operation.

4.1 System Model

The circuit diagram in Figure 4-1 was converted to an average model suitable for control analysis and fast simulation in Appendix A. The machine was modeled using a d-q reference frame where the *q* axis aligns with the real axis and the *d* axis aligns with the negative imaginary axis per [60]. Aligning the field on the *d* axis ensures the resultant speed-dependent back-mmf is aligned with the *q* axis and is defined by (4-1).

$$M_i = \omega_e C_m V_f \tag{4-1}$$

The maximum torque per volt (MTPV) is determined by the angle gamma, with MTPV occurring at 180° for motoring or 0° for generating. Using peak quantities, the electrical torque is defined in (4-2), where negative *q* axis voltage results in positive torque.

$$T_e = -\frac{3}{2} Poles C_m \hat{V}_q V_f \tag{4-2}$$

To simplify the model, diode drops, on-state losses and switching loss of semiconductors are neglected. The CSI is modelled using averaging techniques and is transformed to the d-q reference frame per [61]. The front-end full bridge is modelled as a simple average voltage source, proportional to the input voltage, transformer turns ratio and front-end modulation depth. The complete derivation of the model is included in *Appendix A* and the differential equations describing the modelled system are:

$$L_{dc}\frac{di_{dc}}{dt} = -R_{dc} i_{dc} - \frac{3}{2} m_q v_q - \frac{3}{2} m_d v_d + v_g \tag{4-3}$$

$$C_s \frac{dv_q}{dt} = m_q i_{dc} - \frac{v_q}{R_s} - C_s \omega_e v_d + C_m \omega_e v_f \tag{4-4}$$

$$C_s \frac{dv_d}{dt} = m_d i_{dc} - \frac{v_d}{R_s} + C_s \omega_e v_q \tag{4-5}$$

The equivalent circuit of the three equations is shown in Figure 4-2, which is suitable for control analysis and simulation of system dynamics well below the switching frequency.

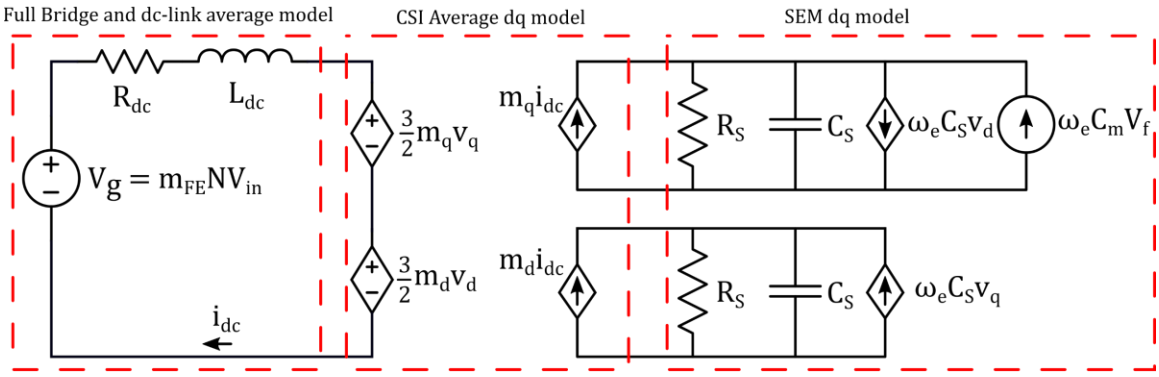

Figure 4-2. Physical System Averaged Model

4.2 dc-link Stability

Conventional CSIs used with electromagnetic machines control torque in the motor by having the front-end converter regulate the current while the inverter modifies the applied vector angle with a fixed modulation depth as shown in Figure 4-3 [62], [63]. Modern CSI implementations use wide bandgap devices allowing for higher switching frequencies resulting in higher bandwidth control [64]. These systems utilize the front-end controller to regulate the dc-link current at a high frequency, designating it as the inner loop in the system. The inverter stage regulates the output voltage and/or current in a slower outer loop shown in Figure 4-4. Overall, this approach enables the implementation of high performance modulation schemes that assume a fixed dc-link current [65], [66]. Significant load transients can limit dynamic performance and power feed forward can reduce these effects [64].

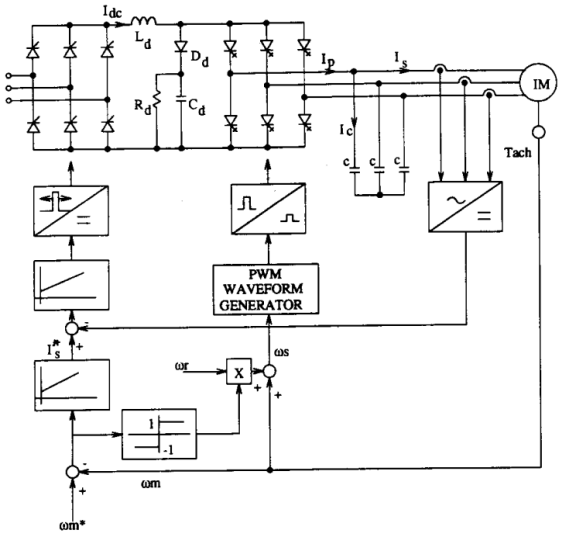

Figure 4-3. Traditional current control in back-to-back CSI systems with an electromagnetic machine ©IEEE [1992] [62]

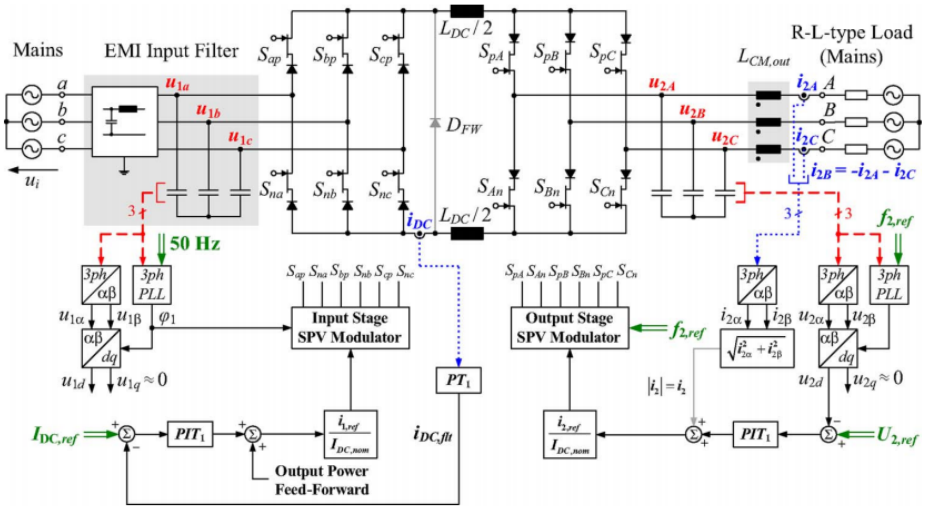

Figure 4-4. Advanced dc-link current control in back-to-back CSI with inner dc-link current loop ©IEEE [2009] [64]

The system in this work is implemented with the inverter voltage regulator (machine torque modulator) being the faster inner control loop while the front-end controls the average current in the dc-link with a lower bandwidth PI regulator. Additionally, the modulation implementation utilizes the dc-link current command when determining the space vector dwell times. This can have significant implications on the stability of the dc-link as shown cascaded power systems with slow dc-link control [67]. If utilized in a servo

application, the dc-link controller must be able to reject the disturbances presented by the CSI during large torque step commands while being the slower control loop. Therefore, the stability of the dc-link controller is analyzed with the effects of the voltage loop treated as the inner loop in the system. The stability of current source rectifier systems in regeneration mode depends on the dc-link inductance value for active power loads [67]. It will be shown that for this system, the small-signal stability is not dependent on the dc-link inductance but rather the output power of the inverter and dc-link resistance.

The complex vector voltage regulator (CVVR) for the SEM was developed in [14]. It is a PI controller with pole/zero cancellation and cross-coupling decoupling defined by equations (4-6) and (4-7). The proportional and integral voltage regulator gains are set based on the desired bandwidth, f_{bw}, and the machine parameters per equations (4-8) and (4-9) respectively.

$$i_q^* = m_q^* i_{dc} = \left(v_q^* - v_q\right)\left(K_{vp} + \frac{K_{vi}}{s}\right) + \left(v_d^* - v_d\right)\frac{K_{vp}\omega_e}{s} \tag{4-6}$$

$$i_d^* = m_d^* i_{dc} = \left(v_d^* - v_d\right)\left(K_{vp} + \frac{K_{vi}}{s}\right) - \left(v_q^* - v_q\right)\frac{K_{vp}\omega_e}{s} \tag{4-7}$$

$$K_{vp} = 2\pi f_{bw} C_s \tag{4-8}$$

$$K_{vi} = \frac{K_{vp}}{R_s C_s} \tag{4-9}$$

To analyze the stability of this multiple-input multiple-output (MIMO) non-linear system an operating point evaluation was undertaken with the system input defined as average dc-link input voltage, v_g, and system output the dc-link current, i_{dc}. Small signal quantities are denoted by "~" and steady state quantities by capital letters. The system is operated at MTPV and the steady-state d-axis voltage is zero. The resultant 5th order system is defined by equations (4-10) through (4-14).

$$\tilde{m}_q I_{dc} = -\tilde{v}_q \left(K_{vp} + \frac{K_{vi}}{s}\right) - \frac{\tilde{v}_d K_{vp} \Omega_e}{s} \tag{4-10}$$

$$\tilde{m}_d I_{dc} = -\tilde{v}_d \left(K_{vp} + \frac{K_{vi}}{s}\right) + \frac{\tilde{v}_q K_{vp} \Omega_e}{s} \tag{4-11}$$

$$\tilde{v}_q \left(sC_s + \frac{1}{R_s}\right) = \tilde{\imath}_{dc} M_q + \tilde{m}_q I_{dc} - \tilde{v}_d C_s \Omega_e \tag{4-12}$$

$$\tilde{v}_d \left(sC_s + \frac{1}{R_s}\right) = \tilde{\imath}_{dc} M_d + \tilde{m}_d I_{dc} + \tilde{v}_q C_s \Omega_e \tag{4-13}$$

$$\tilde{\imath}_{dc}(sL_{dc} + R_{dc}) = \tilde{v}_g - \frac{3}{2}\tilde{v}_q M_q - \frac{3}{2}\tilde{m}_q \hat{V}_q - \frac{3}{2}\tilde{v}_d M_d \tag{4-14}$$

Table 4-1. System parameters for stability evaluation

Input Voltage	V_{in}	280 Vdc
Transformer Turns Ratio	$N = N_s/N_p$	7.4 V/V
dc-link Inductance	L_{dc}	3.4 H
dc-link Resistance	R_{dc}	40
CVVR Bandwidth	f_{bw}	150 Hz
Stator Resistance	R_S	1.6 MΩ
Stator Capacitance	C_S	13.8 nF
Mutual Capacitance	C_m	2.2 nF
Poles	P	96

Table 4-2. Steady state operating point for stability evaluation

Field Voltage	V_F	7 kV
q-axis Voltage	V_q	4 kV
d-axis Voltage	V_d	0 kV
dc-link Current	I_{dc}	400 mA
Fundamental Frequency	Ω_e	640 Hz

The system has a complicated closed form symbolic solution so insight into the system is more easily achieved from a pole and zero migration plot. The system was evaluated with the parameters of Table 4-1 at the base operating point of Table 4-2. The small-signal transfer function of dc-link input voltage to dc-link current, i_{dc}/v_g, evaluated at this operating point has a right-hand-plane (RHP) pole. The migration of the pole vs speed and voltage in Figure 4-5 shows that as the operating point increases the pole moves further

into the RHP. In Figure 4-6-A an increase in the dc-link inductance with the aim of stiffening the dc-link only reduces how far into the RHP the pole migrates but does not shift the pole to the left-hand-plane (LHP). However, increasing the dc-link resistance does shift the RHP to the LHP as shown in Figure 4-6-B. To simplify and understand the nature of this instability the inverter is modelled as a constant power load.

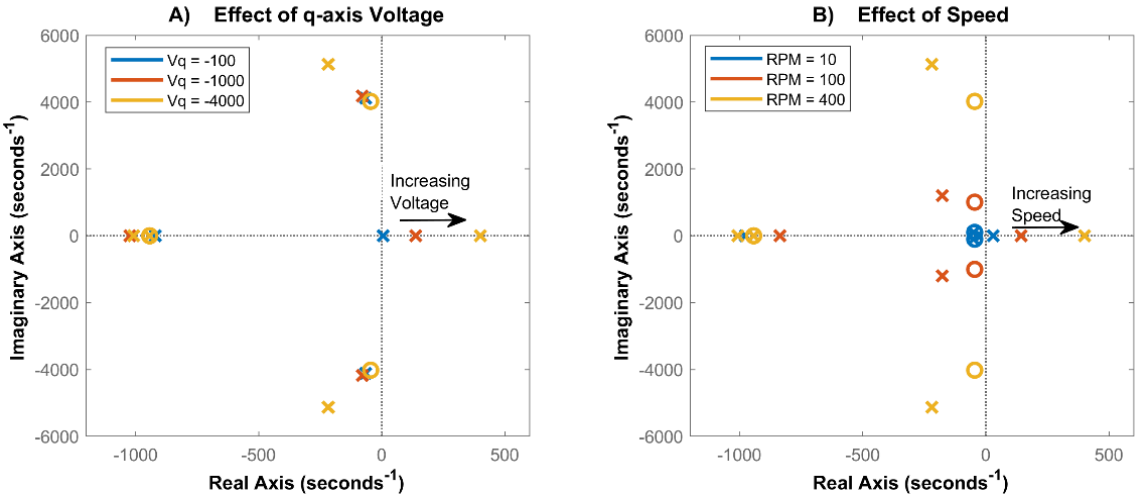

Figure 4-5. Effects of q-axis voltage (A) and speed (B) on linearized i_{dc}/v_g system pole zero location

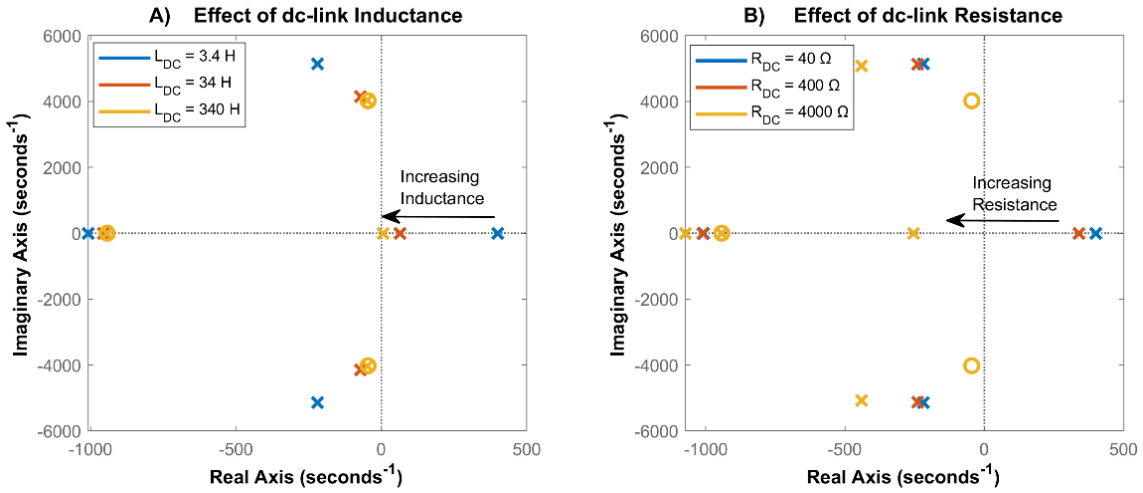

Figure 4-6. Effect of dc-link inductance (A) and resistance (B) on linearized i_{dc}/v_g system pole zero location

4.2.1 Constant Power Load Model

The relative high bandwidth of the CVVR compensates for any changes in the dc-link current maintaining the torque output of the CSI. This behavior can be modelled by the constant power load defined by (4-15) and the stability of this system can be evaluated by utilizing a simple first order model of the system shown Figure 4-7.

$$P_o = v_{dc,o} i_{dc} \tag{4-15}$$

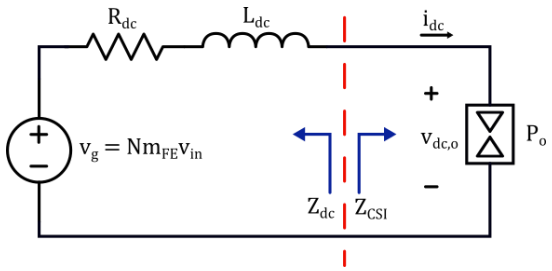

Figure 4-7. dc-link model with a constant power load

The stability is analyzed by inspecting the impedance looking up-stream, Z_{dc}, and down-stream, Z_{CSI}, at the interconnection point as shown in Figure 4-7. The up-stream impedance is the inductance and resistance of the dc-link (4-16).

$$Z_{dc} = R_{dc} + sL_{dc} \tag{4-16}$$

The low frequency impedance of the CSI when modelled as constant power load appears as the negative incremental impedance (4-17). The negative incremental-impedance created by the constant power load can lead to instabilities in interconnected power systems [68]–[71].

$$Z_{CSI} = \frac{\partial v_{dc,o}}{\partial i_{dc}}\bigg|_{I_{dc},V_{dc}} = \frac{\partial}{\partial i_{dc}}\left(\frac{P_o}{i_{dc}}\right)\bigg|_{I_{dc}} = -\frac{P_o}{I_{dc}^2} \tag{4-17}$$

Evaluating the small signal transfer function (4-18) for stability results in the simple requirement (4-19), that the resistive power load must be higher than the constant power

load created by the higher bandwidth CVVR. The constant power for the SEM machine is defined in (4-21). The pole location from (4-19) matches the unstable pole of the complete system exactly when located at the complex-plane origin.

$$\frac{\tilde{\imath}_{dc}}{\tilde{v}_g} = \frac{1}{\mathrm{Z_{CSI}} + Z_{dc}} = \frac{1/\mathrm{L_{dc}}}{s + \frac{I_{dc}^2 R_{dc} - P_o}{I_{dc}^2 L_{dc}}} \tag{4-18}$$

$$s = -I_{dc}^2 R_{dc} + P_O < 0 \tag{4-19}$$

$$P_O = \frac{3}{2}\left(\frac{V_q^2}{R_S} + \frac{V_d^2}{R_S} - \omega_e C_m V_f V_q\right) \tag{4-20}$$

To stabilize the system two methods are investigated. The first method shifts the right-hand-plane pole by introducing virtual resistance that offsets the negative incremental resistance of the constant power load. The second method decouples the constant power load from the front-end controller by decoupling the voltage disturbance generated by the q-axis of the inverter.

4.3 Front-End Controller with Virtual Damping Resistance

The previous section showed the existence of a right-hand-plane pole caused by the constant power load presented by the CVVR controlling the SEM torque at a higher bandwidth than the front-end controller. This section focuses on the shifting the pole of (4-19) into the left-hand-plane by introducing a virtual resistance that increases the effective dc-link resistance and ensuring (4-19) is negative. The inclusion of a virtual resistance provides an open-loop stable enhanced system plant around which a dc-link controller can be tuned. A simplified system block diagram is shown in Figure 4-8 with a proportional-integral controller.

If the required damping resistance were implemented with a physical resistor it results in limiting the system efficiency to 50%. Active damping via virtual impedances have been utilized for stabilizing systems with constant power loads [69], [72]. Virtual resistances have been utilized extensively in CSI systems as well but generally they have been applied to minimizing the resonance of the output filters required for conventional machines [73]–[75].

The proposed proportional-integral (PI) dc-link current controller, shown in Figure 4-8, is tuned around the system plant and the virtual resistance, where H(s) is the system plant from equations (4-10) through (4-15). The units of the PI controller are Ohms and Ohm/sec, producing a primary side voltage command which is converted to a modulation command, M_{FE}, for the front-end full bridge. The necessary virtual resistance for stability was modelled as a dc-link resistance that modifies the voltage command from the PI controller output through negative current feedback. Since the controller operates on the primary side of the front-end transformer, the feedback from the virtual resistance to the voltage command is scaled by the transformer turns-ratio N. The current regulator parameters for the modelled system are shown in Table 4-3 and the bode plots for the open-loop and closed loop responses of the enhanced system plant and compensated system are shown in Figure 4-9 and Figure 4-10 respectively. The controller structure provides infinite gain margin and 100° of phase margin evaluated at this maximum operating point.

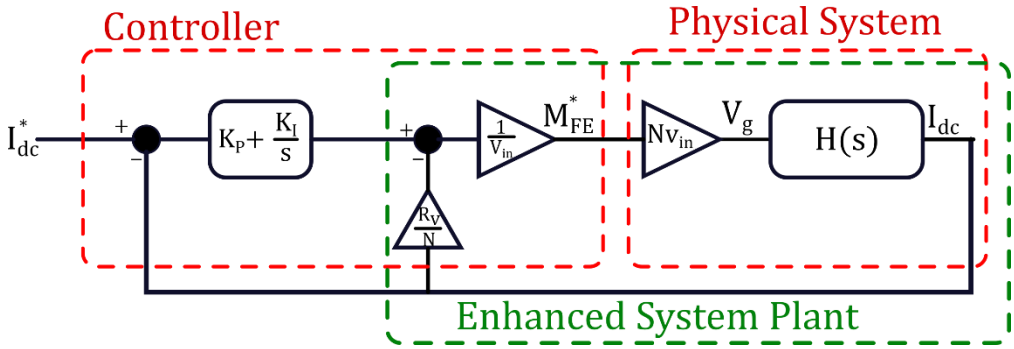

Figure 4-8. dc-link Feedback controller

Table 4-3. Current Regulator Parameters

Current Regulator Proportional Gain	K_P	20 Ω
Current Regulator Integral Gain	K_I	100 Ω/s
Virtual Resistance	R_V	3000 Ω

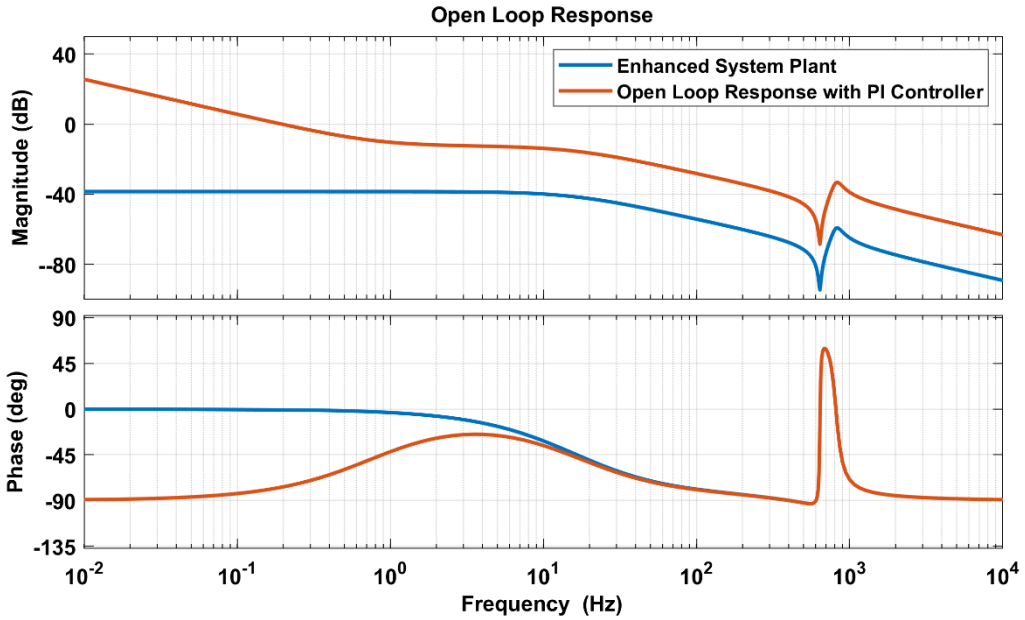

Figure 4-9. Open Loop Response of system with virtual resistance and PI controller

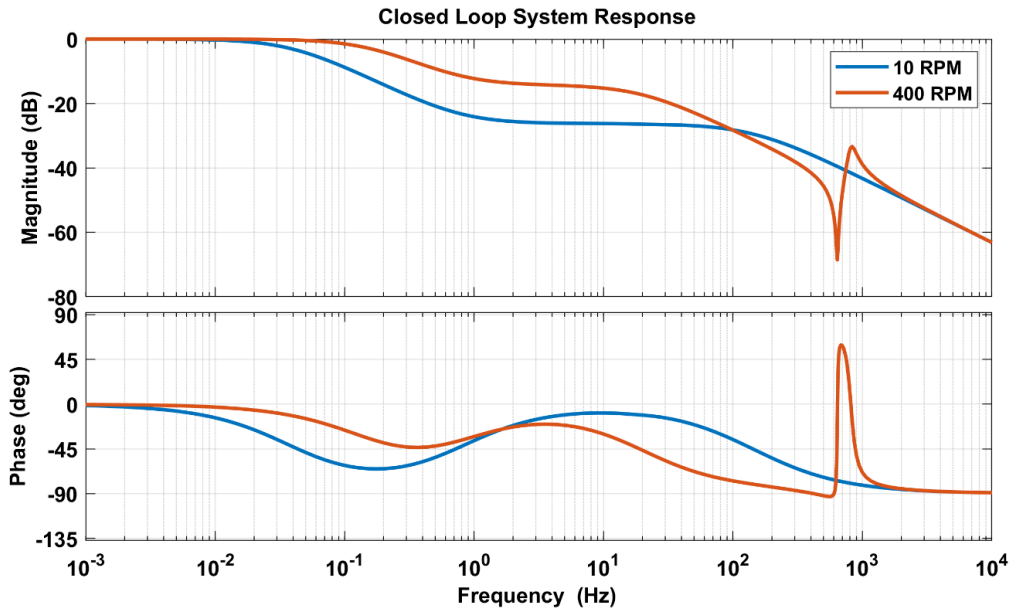

Figure 4-10. dc-link current regulator closed loop response at rated torque for 10 RPM and 400 RPM

Chapter 3 showed that the system requires a variable dc-link to achieve higher efficiency at low speed or low torque. However, the bandwidth of the current regulator at 1 mHz or less depending on the load/speed as shown in Figure 4-10, provides a slow response to command changes. The bandwidth of the system is kept low overall such that the stabilizing effects of the virtual resistance are easily shown. Changing the tuning of the PI controller could be used to increase the bandwidth.

Another method to improve the command response and enable an outer controller to dynamically change the dc-link current would be to use a command feed forward to remove the virtual resistance from the system time-constant as shown in Figure 4-11. While the feed-forward term does not change the stability of the controller the net effect from a dc-link command response perspective is an additional high proportional gain as shown in (4-22). Now, when the closed loop response of the system is evaluated at higher loads/speeds, above unity gain occurs as shown in Figure 4-12. As will be shown in simulation this will result in undesired dc-link current overshoot if fast dc-link command

changes occur. The limiting of the dc-link command rate change is one of the limitations of using the virtual resistance for stability.

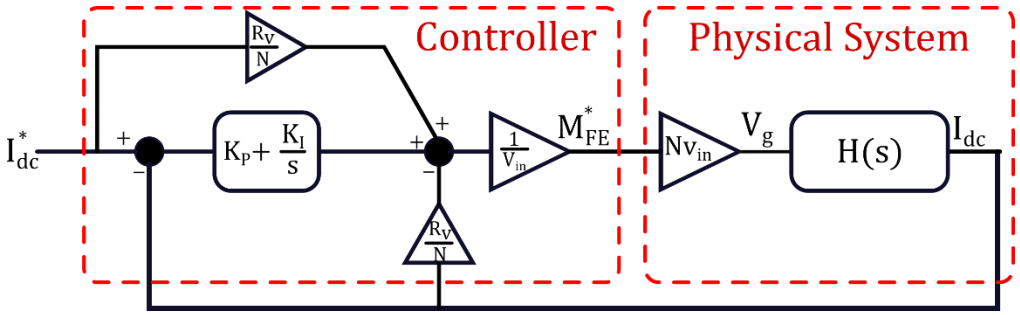

Figure 4-11. dc-link controller with virtual resistance in the feed-forward

$$V_g = N\left[(I^*_{dc} - I_{dc})\left(K_P + \frac{K_I}{s}\right) + I^*_{dc}\frac{R_V}{N} - I_{dc}\frac{R_V}{N}\right] \quad (4\text{-}21)$$

$$V_g = N(I^*_{dc} - I_{dc})\left(K_P + \frac{R_V}{N} + \frac{K_I}{s}\right) \quad (4\text{-}22)$$

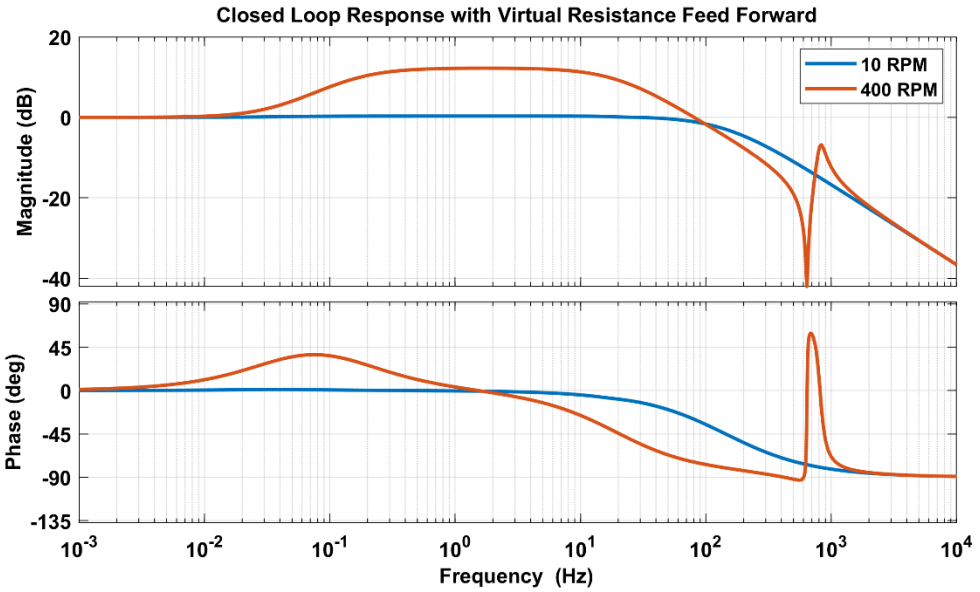

Figure 4-12. Resonance due to effective high gain caused by virtual resistance feed-forward

The controller for the dc-link was discussed in a small signal stability context, however if the SEM is utilized in a servo application the ability to withstand torque-steps is a requirement. First the disturbance rejection of the dc-link is analyzed in this subsection and then simulation was utilized for large signal response to understand the effects of torque-

steps on the dc-link in section 4.5. A rapid change in CSI load or a drop in the system input voltage would appear as a voltage disturbance on the dc-link, which can cause the current in the dc-link to decrease. However, if the dc-link current droops the gain margin can be degraded since stability criteria of (4-19) is dependent on the steady state current and can ultimately become unstable. Fortunately, the virtual resistance that is necessary for stability also contributes to improving disturbance rejection. To understand this effect, the CVVR and CSI are modelled as simple voltage disturbance to the current regulator as shown in Figure 4-13.

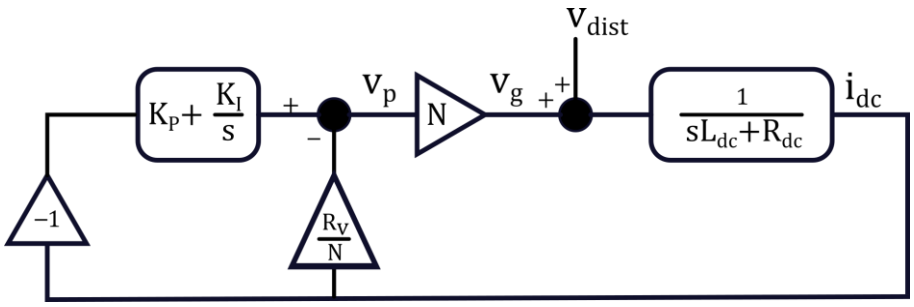

Figure 4-13. Simplified dc-link disturbance rejection block diagram

When the load impedance of a current regulator is increased the ability to reject voltage disturbances is improved [76]. The virtual resistance used for stability increases the effective impedance of the dc-link along with the proportional gain expressed in (4-23). This effect translates to the full system model and the increasing stiffness of the dc-link is shown in Figure 4-14. Increasing dc-link inductance would increase stiffness as well, but as will be shown in the dc-link implementation section 5.2, the challenges are significant when implementing a high inductance with low parasitic capacitance.

$$\frac{V_{dist}}{i_{dc}} = R_{dc} + R_V + NK_P + \frac{NK_I}{s} + sL_{dc} \tag{4-23}$$

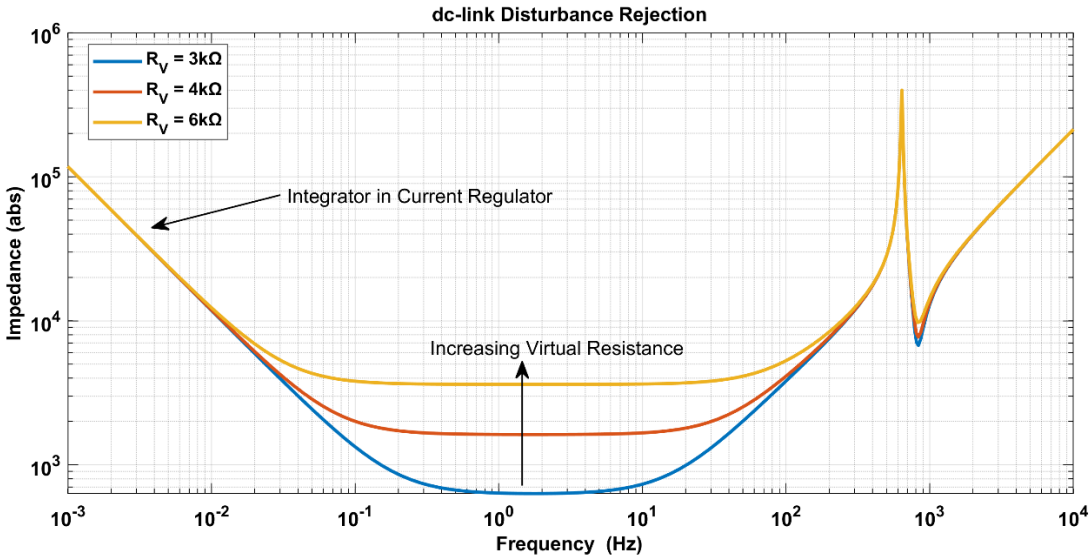

Figure 4-14. Effect of virtual resistance on dc-link disturbance rejection of complete model evaluated at rated torque and 400 RPM

The increased disturbance rejection provided by the virtual resistance is enough at low speeds and smaller torque steps to maintain a dc-link. However, simulation in section 4.5 will show that at higher speeds an increase in torque results in a significant disturbance, causing the dc-link current to drop and the stability criteria of (4-19) to be violated.

4.4 Front-End Controller with q-axis Voltage Decoupling

The instability of the dc-link is caused by the inner control loop of the CVVR appearing as a destabilizing constant power load with a negative incremental resistance. The previous section proposed a controller that off-sets the incremental resistance with a virtual resistance. The virtual resistance results in a shift of the unstable pole to the left-hand-plane. This section proposes decoupling the effects of the CVVR from the front-end controller.

Removing the effects of active loads via power decoupling terms to stabilize dc-links has been proposed numerous times in literature [67], [77]–[79]. The power decoupling method has been used in voltage dc-link systems with minimal dc-link capacitance, where

load transients would collapse the dc-link voltage [78], [79]. The decoupling terms in those systems reduces the energy storage requirement of the dc-link allowing capacitor to be sized for switching frequency components instead of load transients. The system in [77] is a back-to-back CSI system where a decoupling term is proposed for the dc-link current controller. The voltage decoupling term, $v'_{in,}$ is generated from the measured output-voltage and modulation commands of the controller and is added to the command of the dc-link PI controller as shown in Figure 4-15.

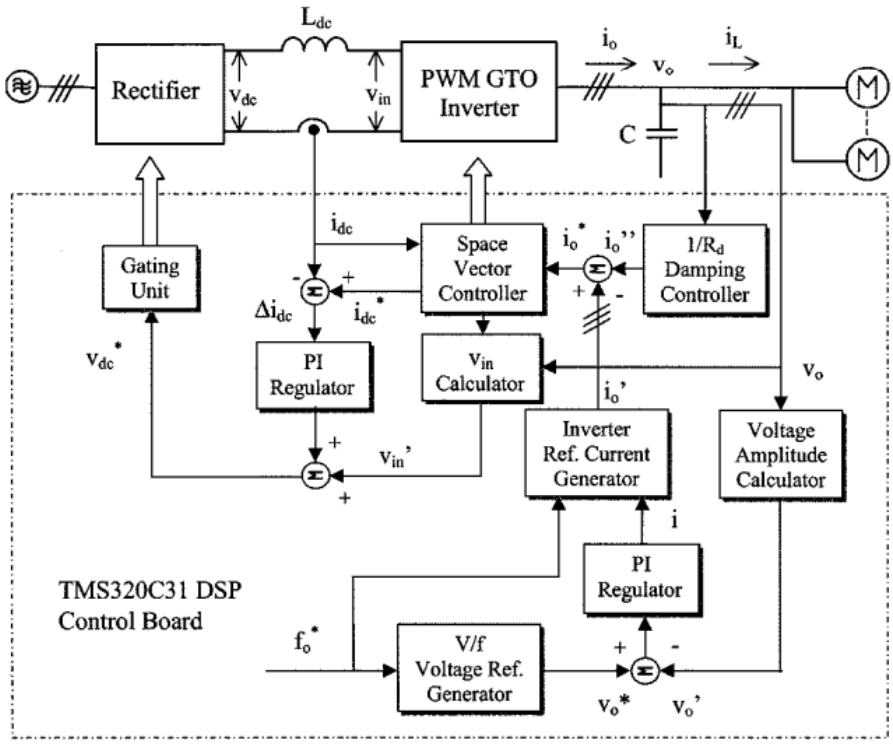

Figure 4-15. CSI system with voltage decoupling term for active front end ©IEEE [2001] [77]

The method from [77] is adapted for use in this system, however the commanded q-axis voltage instead of the measured voltage is utilized. The operation of the CSI in this work is limited to MTPV so only the q-axis is decoupled. As shown in Figure 4-2, the q-axis voltage is reflected to the dc-link by the q-axis modulation and scaled by 3/2. Additionally, the decoupling voltage term is referenced for the primary side resulting in (4-24). A pseudo

block diagram of the system in Figure 4-16 shows both the decoupling term and the system disturbance. The reference frame transforms and PWM modulators are not included.

$$v_{q\_rf} = \frac{1}{N}\frac{3}{2} m_q^* v_q^* \tag{4-24}$$

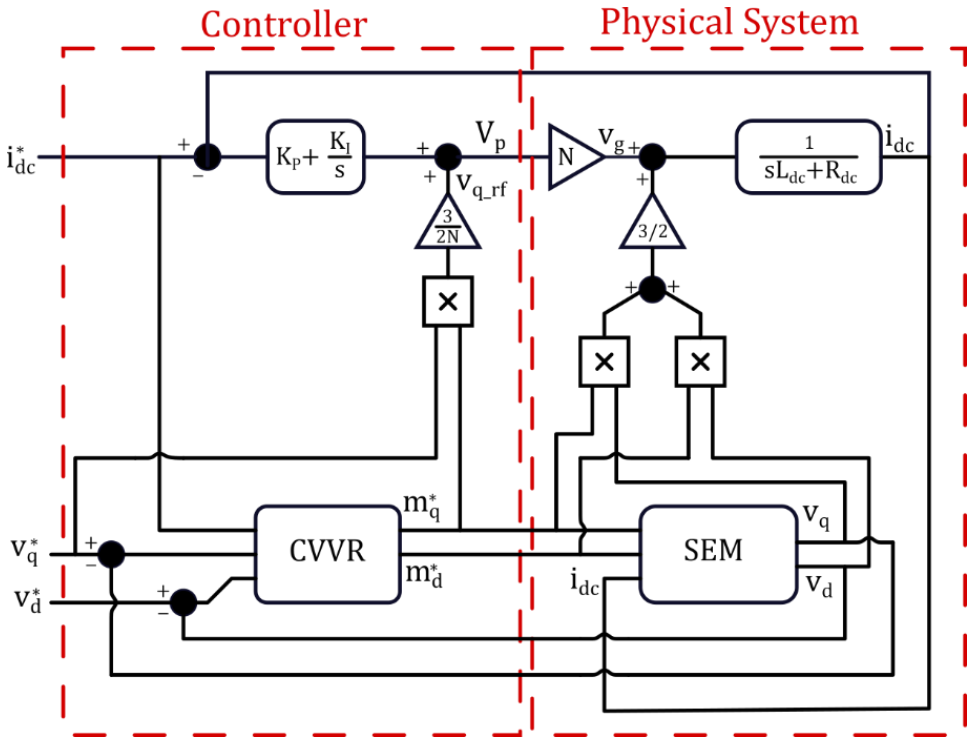

Figure 4-16. System controller pseudo block diagram with q-axis voltage decoupling controller

The decoupling term (4-24) uses commanded values that result from a closed loop control path, i.e., the modulation depth contains information from the measured output voltage and dc-link current due to the closed loop CVVR. Therefore, this approach is a form of state feedback decoupling, thus the nomenclature of decoupling is maintained instead of feed-forward as it is sometimes referred to elsewhere. The use of the commanded voltage will cause the system to preemptively increase the front-end voltage command due to the lag between commanded and actual voltage during torque transients. To reduce this effect, the voltage-commands of the CVVR should be limited to the bandwidth it is tuned

for. The benefit of using the commanded value is avoiding potential noise issues introduced by the voltage sensors.

One of the benefits of the virtual damping resistance was increasing the disturbance rejection to the dc-link controller. The increased disturbance rejection is required in the virtual resistance controller to withstand torque steps. Conversely, the voltage decoupling controller inherently has the commanded load dynamics incorporated and does not need the increased disturbance rejection. The disturbance rejection of the decoupling-based controller is therefore determined by the physical dc-link impedance and PI controller per (4-25). The reduced disturbance rejection will result in higher dc-link ripple compared to the virtual resistance controller if there are significant unmodelled system components.

$$\frac{V_{dist}}{i_{dc}} = R_{dc} + NK_P + \frac{NK_I}{s} + sL_{dc} \tag{4-25}$$

4.5 Simulation

The average model of Figure 4-2 with the CVVR controller and two proposed dc-link current regulators are evaluated in simulation to confirm the analytical modelling of the system. The simulations in this section focused on fixed speed operation. In addition to the controllers discussed, saturation blocks limiting the inverter to linear operation (no over-modulation) and the front-end modulation depth to 95% were included. The PLECS model utilized in this simulation is included in *Appendix D*.

The small-signal modeling and instability issues of the dc-link were confirmed by utilizing slow q-axis ramps increasing the output power until the instability is encountered. A 100 second torque ramp from 0 to 4kV was applied to the model operating at 400 RPM (640 Hz) with a 400mA dc-link and the parameters from Table 4-1 of Table 4-2. The instability of the dc-link was encountered (R_V = 0 in Figure 4-17) and both the virtual

resistance and q-axis voltage decoupling controllers stabilized the system. A similar set of tests on the physical system is performed in *Chapter 6* confirming the small-signal stability of the system with both controllers.

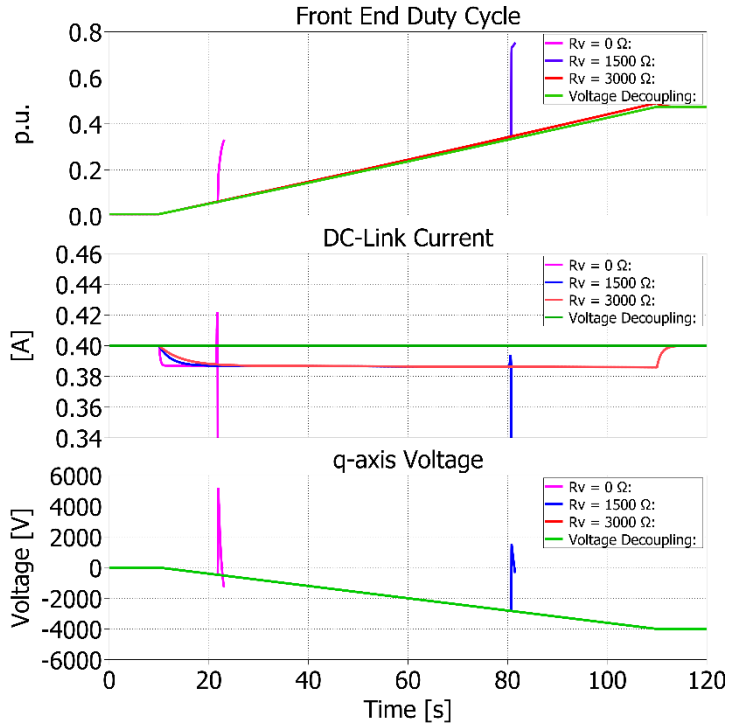

Figure 4-17. Simulation showing dc-link instability dependent on q-axis voltage at 400 RPM and stabilizing effect of virtual resistance and q-axis voltage decoupling methods

When discussing disturbance rejection in Figure 4-14, it was shown that increasing virtual resistance would reduce the current drop caused by a torque command change. However, in Figure 4-17 the dc-link current droops to 390 mA during the slow q-axis voltage ramp for both 1500 Ω and 3000 Ω of virtual resistance. The response is the same in this instance since the ramp is slow enough the disturbance rejection is determined by the integral controller as shown in Figure 4-14. If the ramp command time is reduced to 10 ms the positive effect of virtual resistance on disturbance rejection as well as its limitations cab be seen in Figure 4-18. The minimum amount of virtual resistance introduced to stabilize the steady state operating point is insufficient during fast command changes.

Increasing the virtual resistance past the steady state requirement can provide the necessary disturbance rejection to survive fast torque transients. The best response among the methods is demonstrated by the decoupling controller, where the dc-link current initially increases sharply but overall deviates minimally from the command 400 mA. The waveform of the controller with q-axis voltage decoupling is shown zoomed-in in Figure 4-19 with the controller decoupling voltage and the actual voltage. The utilization of the command voltage instead of measured voltage results in the decoupling term of the controller preemptively delivering energy to the dc-link, causing an increase in dc-link current.

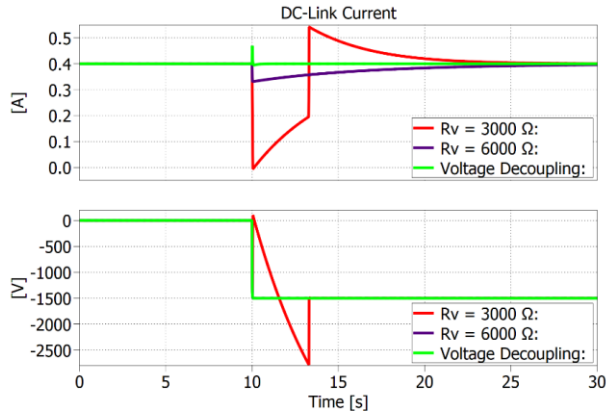

Figure 4-18. Time-domain simulation of the effect of virtual resistance on disturbance rejection. 400 RPM with 1.5kV q-axis torque ramp.

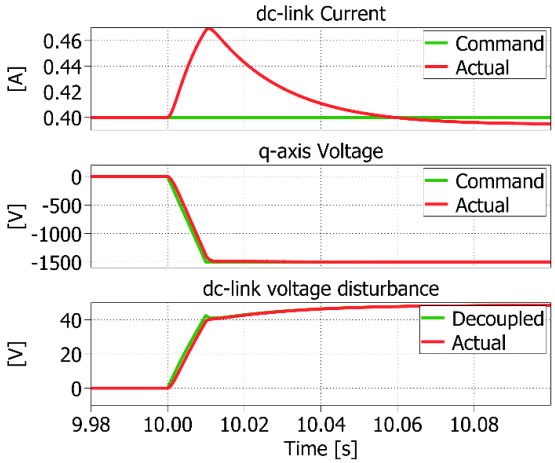

Figure 4-19. Difference between decoupled voltage disturbance and actual voltage during q-axis torque step leading to increase in dc-link current

Chapter 3 predicts the improved performance of the system with a variable dc-link and the two controller's response to dc-link current command changes were evaluated in simulation. Figure 4-20-A shows the expected slow response of the dc-link controller with virtual resistance and the improved response of the controller with q-axis voltage decoupling since the PI controller does not have to overcome the virtual resistance. The zoomed-in transient in Figure 4-20-B shows that the CVVR must react to this disturbance and that for both controllers introducing a ramp rate limit on the command change would be beneficial.

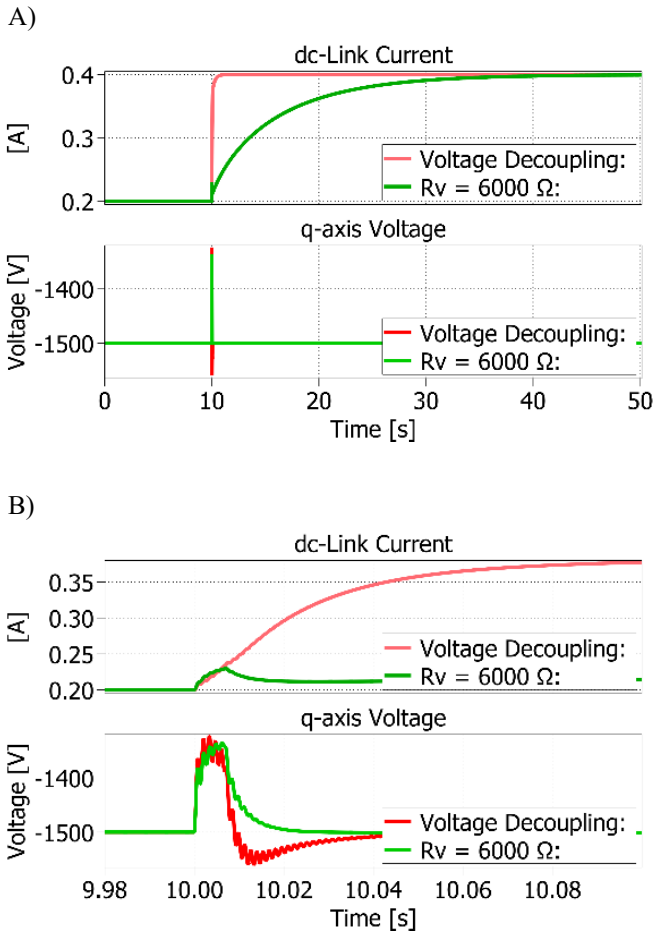

Figure 4-20. System response to dc-link current command change A) complete response B) initial q-axis voltage transient

4.6 Chapter Summary

The system model including the front-end and dc-link was developed, and the control of the dc-link current was explored. A proposed control method where the inner loop is the CVVR torque modulator and the dc-link current control is an outer loop revealed the existence of a right-hand-plane pole destabilizing the dc-link. The instability is caused by the relatively high bandwidth of the CVVR and its requirement of a stiff dc-link. Modeling the CVVR and CSI as a constant power load showed that the instability is directly related to the negative incremental impedance determined by the output power. Two control methods to stabilize the system were proposed. The first utilized a virtual resistance to offset the constant power load resulting in a shift of the pole to the LHP. The virtual resistance is a linear gain with a simple implementation providing high disturbance rejection. However, it limits the response time of the dc-link to dc-link command changes since the PI controller must overcome a large time constant.

The second control method proposed decoupling the disturbance of the CVVR and CSI from the front-end controller enabling the implementation of a simple PI controller. This non-linear control enables the dc-link current to withstand large load transients while maintaining a faster dc-link current command response. However, the system has reduced disturbance rejection to unmodelled system dynamics compared to the virtual resistance method. Simulation of the system confirmed the output power dependent instability of the system and both controllers stabilized the dc-link. These conclusions are confirmed on the hardware system in *Chapter 6*.

Chapter 5: Hardware Implementation

This *Chapter* focuses on the implementation of the subcomponents in the schematic diagram of Figure 4-1, consisting of the:

1) Inverter, consisting of JFET super cascode and diodes
2) dc-link magnetics
3) Front-end, including transformer and rectifier

The implementation of the various system subcomponents had progressive evolutions throughout the development of the drive. The main improvement targets during each iteration focused on reducing parasitic capacitance with the aim of improving efficiency. The most effective of which was reducing the capacitance of the super cascodes by first utilizing six floating heat-sinks, and eventually no heatsinks at all. The dc-link inductor utilized for most of the testing had a resonance just above the switching frequency and an attempt to improve the resonance is documented. The following sub-sections document the subcomponents and their variations. The software implementations of this drive are documented in [3]. The circuit diagrams for the system control PCBs are documented in Appendix B of this document.

5.1 CSI Hardware

Chapter 2 focused on the development of a medium voltage normally-on JFET super-cascode for use in the SEM drive. The simple implementation of fixed resistive and capacitive dynamic balancing network of [40] was found to be the best implementation for the low-current (<1 A) medium voltage (10 kV) application. Switch development focused mainly on clamped inductive load testing which allowed for maximizing measurement

accuracy and allowing for rapid changing of the various dynamic balancing networks evaluated. While this is effective for evaluating the dynamic balancing of the super cascode, it minimized the system parasitics that are introduced in a complete inverter.

The high impedance of a medium-voltage low-current system increases the drive sensitivity to the influence of parasitic capacitance of components. Normally parasitic capacitive coupling is sufficiently high impedance that it does not influence bulk drive behavior, but in low load current operation, this is not so. At turn-on, the super-cascodes create high dv/dt events leading to significant displacement currents in the system that contribute to switching loss. At turn-off events, the capacitance must be charged from the dc-link, leading to long voltage rise times. The charging and discharging of the capacitance results in increased switching loss and contributes to drive non-linearities due to long turn-off times.

The simplified system diagram of Figure 5-1 shows an example of how these parasitic capacitances interact with a switching event. In this example, the high side switch of phase C is on so the dc-link terminal is connected to node C, the line-line capacitors represent the machine with an assumed state of (5-1).

$$v_C > v_B > v_A \tag{5-1}$$

The inverter is transitioning from an SW6 to SW2 being closed. This is a turn-on event for the super-cascode of SW2 and turn-off event for the diode of SW6. This causes V_N to change from V_B to V_C, resulting in dv/dt events on the parasitic capacitances in the system as shown in Figure 5-1 and the resultant switched current is (5-2). The grayed elements in Figure 5-1 have a comparably minor change in voltage and therefore do not contribute displacement current in this example.

$$i_{sw2} = i_{dc} + C_{dc}\frac{dv_{PN}}{dt} + C_{sw}\left(\frac{dv_{AN}}{dt} + \frac{dv_{BN}}{dt}\right) \tag{5-2}$$

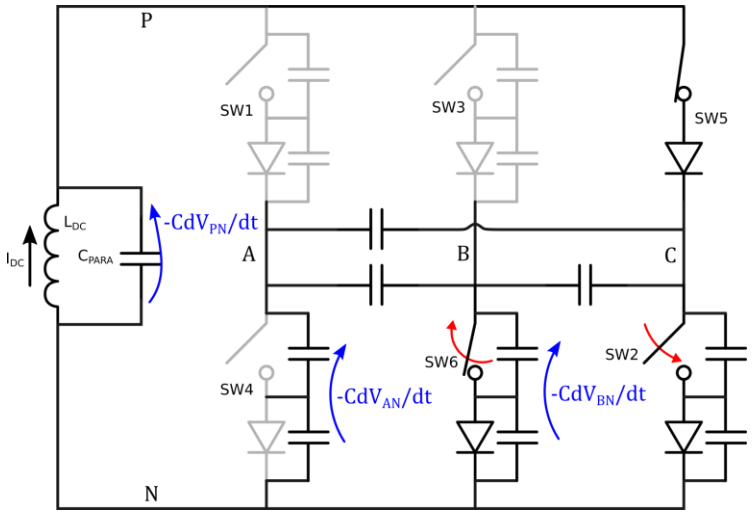

Figure 5-1. Sources of parasitic displacement currents during turn on of SW2

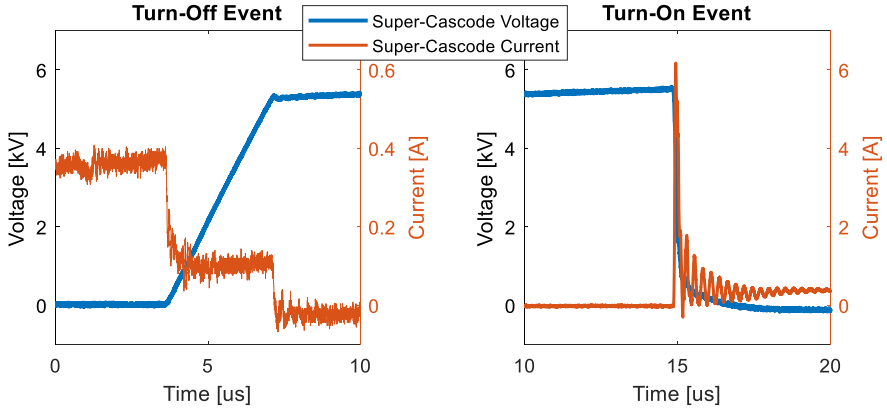

Figure 5-2. Measured switching events in CSI system demonstrating the influence of parasitic capacitance.

An example of the additive effect can be seen in the turn-on event in Figure 5-2 where a 5.5 kV transition in under 500ns results in a 6 A peak turn-on current for a 400 mA dc-link. This excludes the peak current that is inherent in discharging the super-cascodes own parasitic capacitance that is not in the current probes path. At a turn-off event between a super-cascode and a diode turn-on, the charge for changing the voltage of the parasitic capacitors in the system comes from the dc-link current. This results in a current divider during the transition where the dc-link current is split into current charging the load, and

the numerous parasitic capacitors in the system. In the turn-off event of Figure 5-2, it is observed roughly 1/3 of the dc-link current is left to charge the output capacitance of the switch, resulting in a 3.5 μs rise time. These switching characteristics contribute to the non-linearities of the drive that affects the self-sensing control in [80]. Higher dc-link currents reduce the rise-time, but overall losses are still increased.

These switching events are confirmation that in a high-voltage low-current system, a designer must minimize the parasitic capacitance of the power-electronics. Parasitic inductance is a minor concern, since a 6 A, 250 ns transition on a 1 μH parasitic loop, results in 24 V of overshoot. This is the dual of a high-current low-voltage problem, e.g. 200 V and 100 A, where significant effort in reducing loop inductances in switch nodes is a priority for more traditional power electronics.

The super-cascode from *Chapter 2* was tested in a clamped inductive load (CIL) setup and was not mounted to a heatsink during the transient testing. This facilitated tuning and probing of the super-cascode necessary for gate network design but as a result neglected the impact of parasitic capacitance of the devices to the heatsink. When mounted with a 2mm high-voltage thermal isolation pad to a heatsink, the super-cascodes have between 10-20 pf of isolation capacitance per device, resulting in a combined 150 to 200 pF of parasitic capacitance per switch to the heatsink as shown in Figure 5-3. If the heatsink is a common heatsink for all devices, then additional coupling paths exist between super-cascodes that are not drawn in the simplified drawing of Figure 5-1. The evolution of the super cascode inverter mounting is shown in Figure 5-4, from a common heat sink to heatsink segmented per switch and finally individual devices with no heatsink.

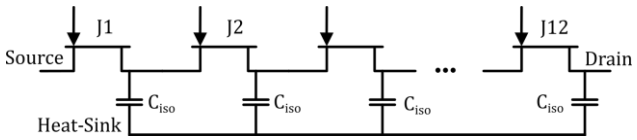

Figure 5-3. Parasitic Capacitance of JFET Super-Cascode

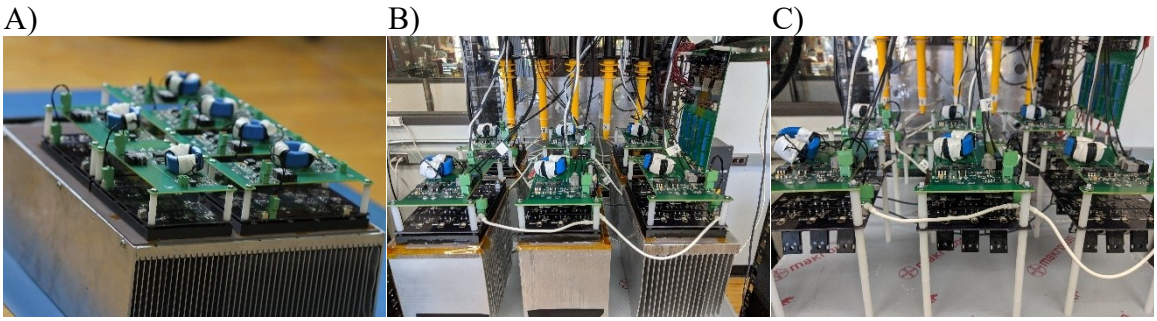

Figure 5-4. Evolution of Super Cascode A) Single Heatsink B) Individual Heatsinks C) No Heatsinks

The clamped inductive load testing utilized fast silicon diodes HVR5510U10 with a 1 A data sheet rating [46]. However, the packaging is a through hole potted plastic component with minimal capability for cooling, limiting the continuous current below 0.2A. Additionally, the PN junction diodes exhibit reverse recovery losses dependent on the di/dt applied to them. Therefore, in implementation of the CSI the diodes utilized consisted of four series connected 3.3kV SiC Schottky MPS diodes from GeneSiC [81]. These Schottky diodes have reduced on-state voltage and reduced capacitive switching effects compared to the silicon PN diodes. The packaging of the diodes allows for board mount cooling simplifying the thermal design and the diode stage of the inverter is shown in Figure 5-5.

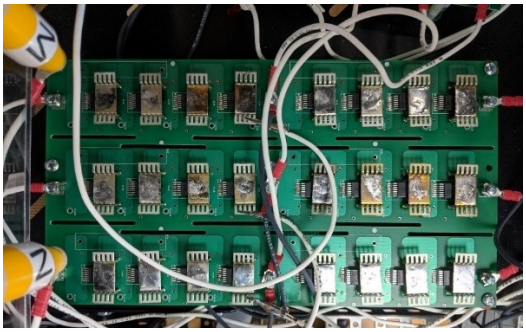

Figure 5-5. CSI diodes consisting of series connected 3.3kV SiC Schottky MPS diodes

5.2 dc-Link Inductor

The dc-link inductor is critical in providing a stiff current input to the current source inverter so that linear modulation can be assumed. The sizing of the inductor value is determined by several key aspects that affect the required energy storage:

1) Dc-link current
2) CSI load
3) PWM switching frequency and modulation scheme
4) Input frequency content
5) Load dynamics

At low dc-link currents more inductance is required since the stored energy is dependent on the current squared (5-3). The numbered items 2-4 above are all closely related and ultimately affect the inductance value by changing the duration and magnitude of volt-seconds applied, affecting how often and how much energy is removed/added to the inductor. Increasing the inductance or dc-link current reduces the relative size of the removed energy which reduces the current ripple and improves drive linearity.

$$E = \frac{1}{2} L_{dc} I_{dc}^2 \tag{5-3}$$

[82] provides an analytical method to size the dc-link inductor for a given ripple specification considering items 1-3, however it neglects the effect of the input waveform. The dc-link input voltage for the system documented in this dissertation is a high frequency voltage PWM. Additionally, the front-end switching frequency is operated at a different switching frequency than the CSI complicating an analytical analysis. Optimizing the inductor is left as future work, and in this dissertation the sizing of the inductor was done in simulation. In *Chapter 3* the dc-link current ripple vs operating frequency at rated output

voltage is reported in Table 3-8 for a 4 H inductor. Ultimately a 3.4 H inductor was utilized for testing due to self-resonance frequency issues. The modulation scheme utilized in *Chapter 3* and *Chapter 6* for the efficiency testing is the four pulse sequence from [83].

Regarding the energy storage needed for load dynamics it was shown that the inductance does not play a key role in small signal stability in section 4.2, but it does affect the disturbance rejection of the dc-link and its ability to support torque steps per equation (4-23). However, creating a multi-henry inductance with minimal capacitance is challenging as will be shown in this section. Therefore, the load dynamics were handled in control by a combination of virtual resistance and voltage decoupling terms as detailed in section *Chapter 4*.

The dc-link evolved during development with progressive improvements and one alternative design for comparison. All designs considered and utilized are based on amorphous alloy 2605SA1 cores that have a saturation flux density of 1.4 T and are capable of 50 kHz operation if the peak-peak current is kept low [84]. The main inductor design shown in Figure 5-7 uses AMCC-100 cores, and it was used for most of the testing in *Chapter 6*. A variation utilizing much smaller AMCC-10 cores was also tested for a comparison in performance.

The dc-link inductor design utilized the established area product methodology from [85]. This method allows for quick selection of the core given an inductance, peak current, and ripple frequency. Following this method requires setting factors for insulation, current density, and target flux density in the cores based on guidelines in [85]. The winding to insulation ratio was set to 1:1 allowing for significant spacing between layers of windings. The insulation factor is in addition to the copper to insulation ratio of the enameled wire

itself. The extra insulation is required to reduce the parasitic capacitance of the coils and reduce the proximity effects due to high turn counts.

With a switching frequency of 18 kHz the dc-link inductor must have high impedance, significantly above the switching frequency, or else it will not function as a stiff current source. Additionally, as discussed in the previous subsection any parasitic capacitance in the dc-link will contribute switching loss as shown in Figure 5-1. With a desired inductance of 4 H, 5 pF of parallel capacitance will result in a self-resonant frequency of 36 kHz. Custom bobbins with multiple sections were utilized, increasing the total space allocated to insulation. A single section bobbin causes large layers of windings to form resulting in the parasitic capacitances shown in the equivalent circuit of Figure 5-6-A. However, utilizing a multi-section bobbin (Figure 5-6-B) reduces the individual layer-layer capacitances and places more of them in series to reduce the overall capacitance. This has diminishing returns however, since two coils are used per inductor and the coils are capacitively coupled to the core providing an alternative high frequency path. This is aggravated in the designs used in this work because the 2605SA1 cores are relatively conductive compared to a powdered core or ferrite.

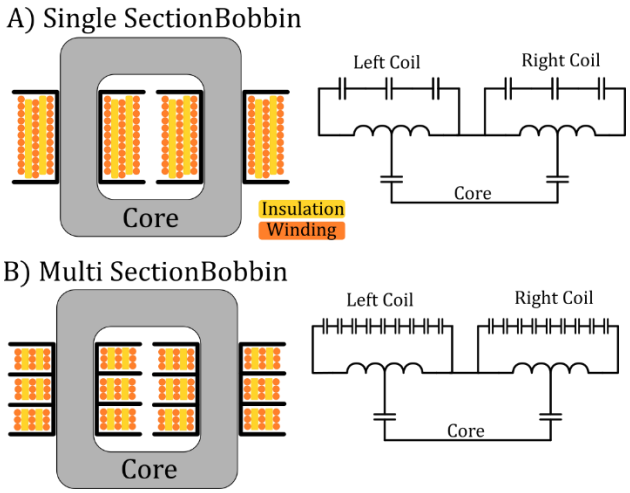

Figure 5-6. Parasitic capacitance of inductors and bobbins A) single section B) multi-section

The main inductor design with AMCC-100 cores (Figure 5-7) used custom bobbins that provided a total of eight winding areas reducing the maximum turn to turn voltage and reducing the parasitic capacitance. The windings were made with 22 AWG wire and 528 turns. The turn count was selected because it offers a wide range of possible inductance and peak currents achievable by varying the gap. Figure 5-8 shows the inductance and saturation current vs gap size for this winding. The inductors were characterized on an E4990A Impedance analyzer and the resistance and capacitance of the base coil pair is in Table 5-1. The saturation current value was measured by applying a step dc-voltage from a low voltage current limited supply. The knee of the current waveform is the saturation current.

Table 5-1. AMCC-100 Inductor Parasitics

Parameter	Description	Value
$R_{S,\,dc}$	Winding resistance measured from primary at dc without core	8.2 Ω
$R_{S,\,20\,kHz}$	Winding resistance measured from primary at 20 kHz without core	11 Ω
C_P	Parallel capacitance	20 pF

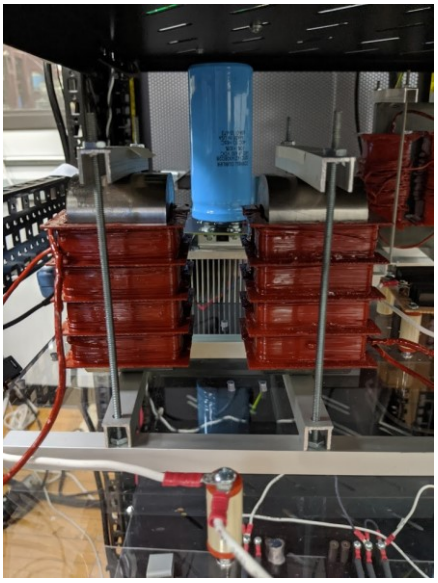

Figure 5-7. AMCC-1000 dc-link inductors

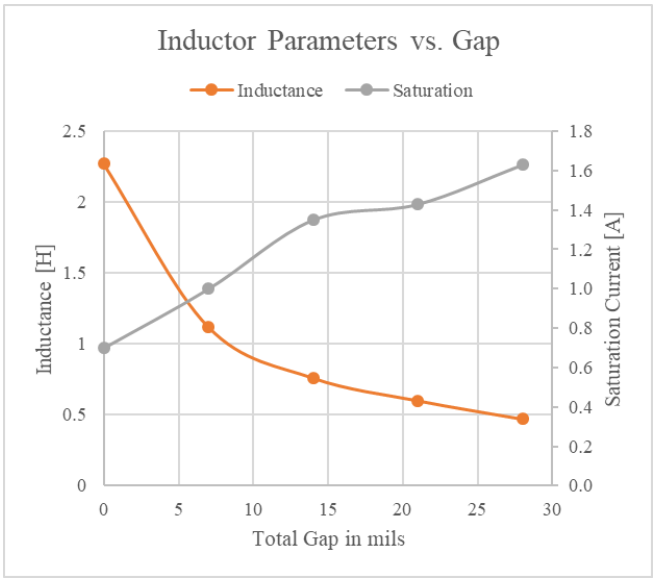

Figure 5-8. Single dc-link inductor inductance and saturation current vs gap

The initial goal was to utilize two AMCC-100 inductors, one on the high side and one on the low as shown in Figure 4-1. However, the parasitic capacitance was 20 pF per inductor creating a self-resonance right around the target switching frequency. To compensate four inductors were utilized providing a total parasitic capacitance of 5 pF. Since the four inductors are not identical additional resonances occur and a dip in impedance before the self-resonance point is seen in the impedance measurements of Figure 5-9. More careful construction of the coils with specific attention to spacing between layers would reduce this effect.

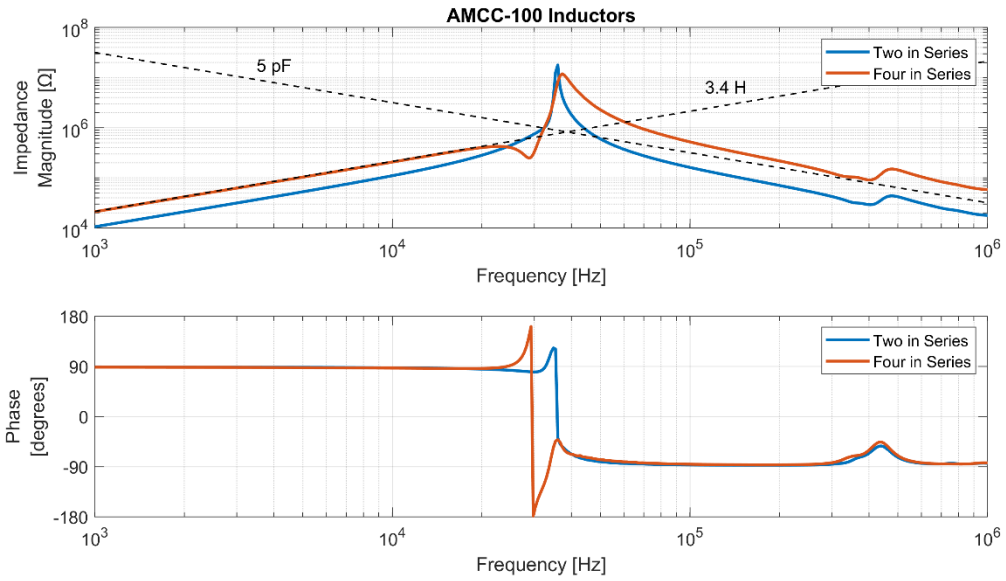

Figure 5-9. Measured Impedance of AMCC-100 Inductors

The loss breakdown analysis in *Chapter 6* shows that the inductors have higher loss than predicted in *Chapter 3*. An alternative design with reduced magnetic material was constructed utilizing ten series connected smaller inductors with AMCC-10 cores. The multiple inductors in series allow for further reduction of overall parasitic capacitance while simultaneously reducing the magnetic material from 4 kg to 2 kg. However, the inductors are still high turn count, requiring smaller gauge wire resulting in an increase in

dc resistance of the dc-link inductor bank. These inductors utilized 3-section bobbins and the parasitics of a single coil are shown in Table 5-2. One half of the dc-link for each design is shown in Figure 5-10 including the non-conductive mounting utilized to reduce stray capacitance.

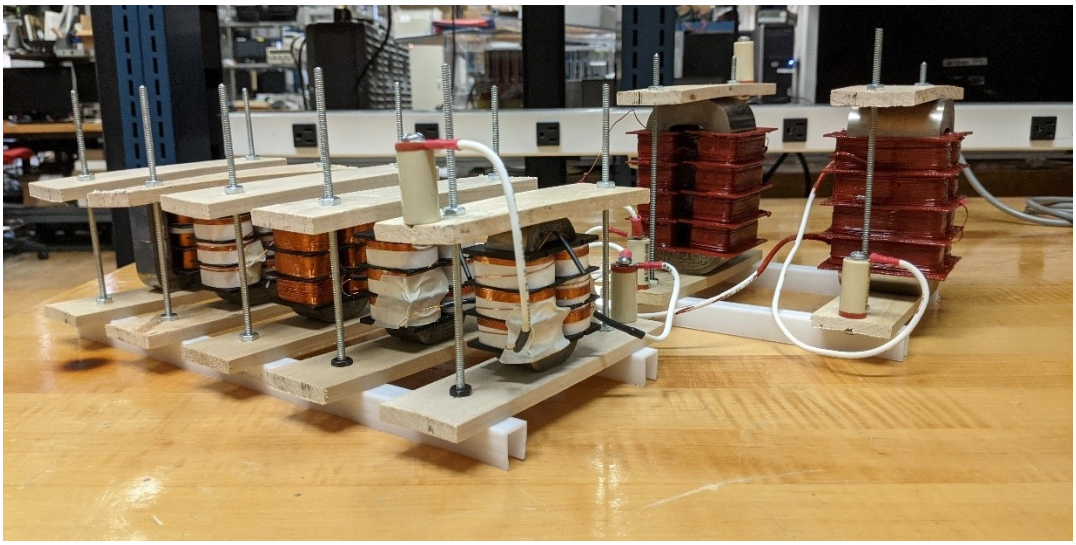

Figure 5-10. Side by side picture of five AMCC-10 inductors with two AMCC-100 inductors

The individual coils achieved extremely low parasitic capacitance (5 pF) and ideally with 20 of them in series (2 per inductor) the total capacitance would be 0.25 pF. However, the parasitic capacitance between coil and core and between coils resulted in a net capacitance of 1 pF at high frequency and multiple resonances and interactions reducing the impedance in the 30 to 70 kHz range. The impedance of half the inductor bank and the full inductor bank is shown in Figure 5-11, and the effects due to slight differences in inductance and parasitics is clear. The two inductor designs are compared for differential and common mode impedance in Figure 5-12 and Figure 5-13 respectively. *Chapter 6* section 6.4.2 discusses the two different designs impact on the overall system.

Table 5-2. AMCC-10 Coil without core parasitics

Parameter	Description	Value
$R_{S,\,dc}$	Winding resistance measured from primary at dc without core	14 Ω
$R_{S,\,20\,kHz}$	Winding resistance measured from primary at 20 kHz without core	15 Ω
C_P	Parallel capacitance	2.5 pF

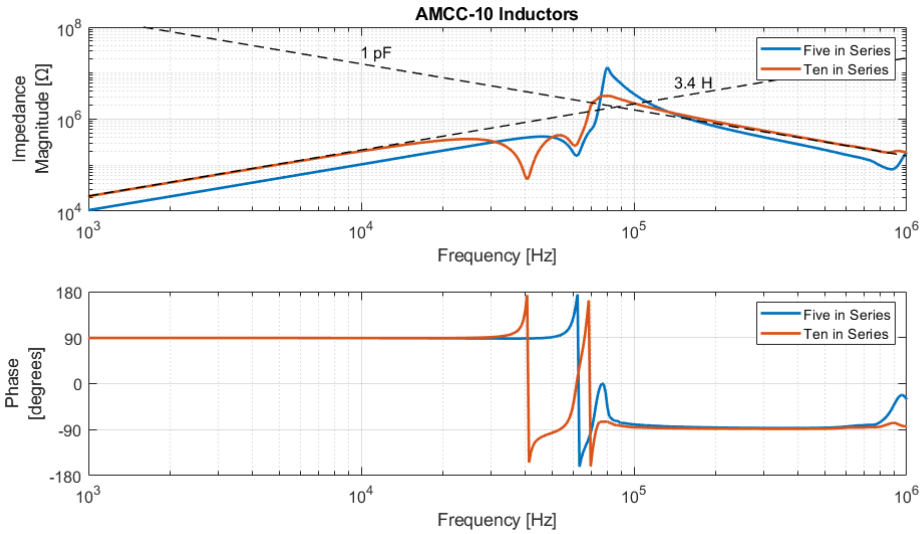

Figure 5-11. Measured Impedance of AMCC-10 Inductors

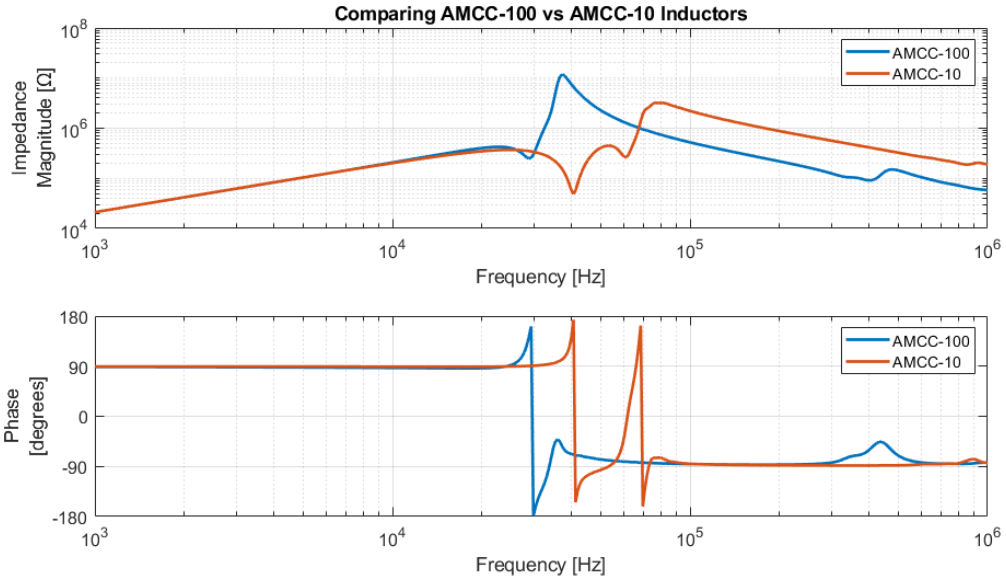

Figure 5-12. Comparing overall impedance of AMCC-100 vs AMCC-10 inductors

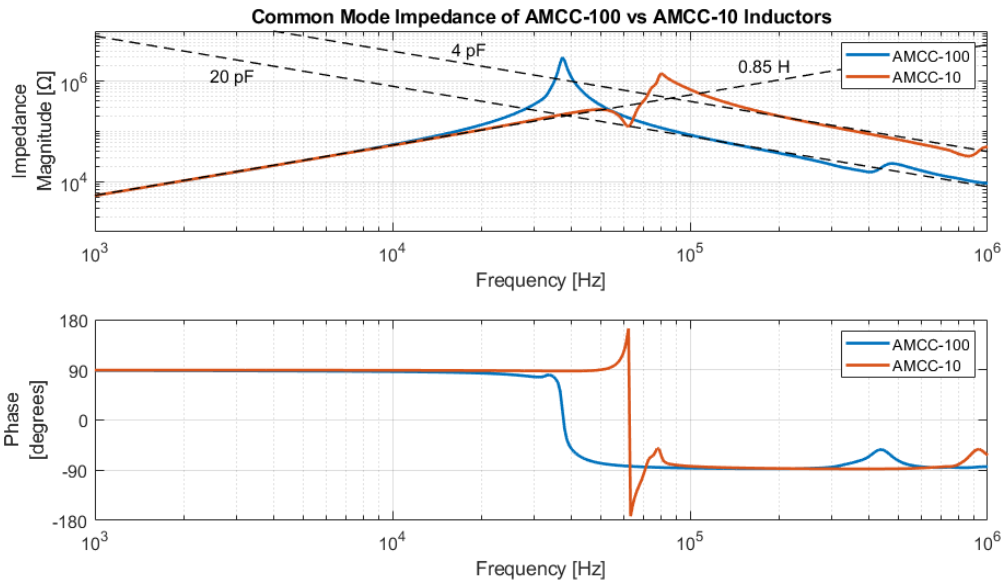

Figure 5-13. Common Mode impedance of dc-link variants

5.3 Front-End Hardware

The implementation of the front-end full-bridge power electronics and rectifying diodes was relatively simple excluding the magnetics. A commercial off the shelf (COTS) 3-phase 1200V, 80mΩ SiC MOSFET power module [86] and the companion evaluation board were utilized [87]. The evaluation board, shown in Figure 5-14, provides a high frequency decoupling capacitor and isolated gate drivers with over current protection. Additional bulk input capacitance and a 1 uF film capacitor in series with the output were added. The series film capacitor is required to prevent the transformer form saturating because average current mode control was utilized. One phase of the six-pack module was not utilized.

With a transformer turns ratio of 7.4 V/V and an input voltage of 280 Vdc, the rectifier must support 2 kV with additional headroom for switching transients. Initially the rectifying diodes for the front-end were the 5A 3.3kV diodes [81] from GeneSiC. However, due to excessive leakage inductance on the transformer, two diodes were used in series to provide margin for voltage overshoot.

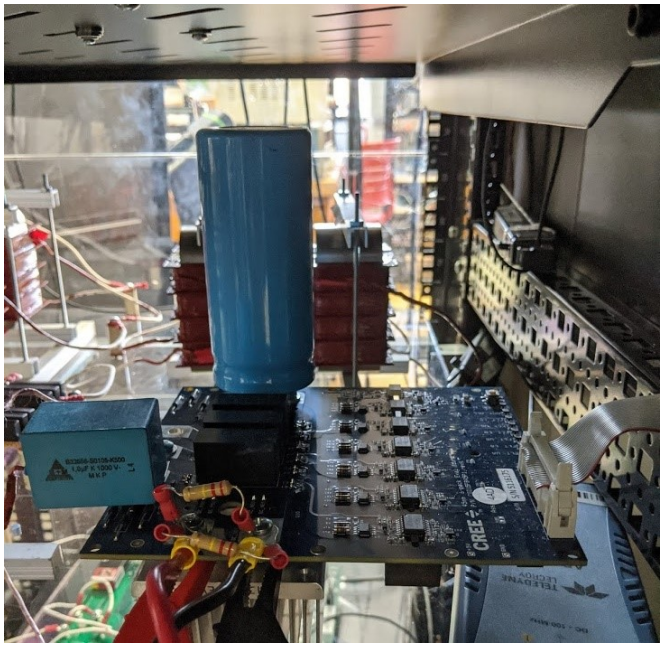

Figure 5-14. Front-end full bridge with decoupling and dc-blocking capacitors

The core was selected using the core area product and general process described in [88]. This process utilizes several factors to help rapidly select a core from manufacturers data sheets that will meet the design requirements. It will not inherently provide an optimum design since these factors estimate winding window utilization, expected core loss based on waveform shape and core shape, and current densities from estimated thermal resistances. The window utilization was set to 0.2 to allow for plenty of space for potting and voltage clearance. The selected core is the FERROXCUBE U93/76/16 ferrite U core [89]. Utilizing the design methods from [88] results in a functional but non-optimized design due to the overhead factors and rule of them. The optimization of the front-end transformer is included in the recommended future work.

With a core that can handle the maximum power pre-selected the design criteria for a given operating point focused on limiting the magnetizing current, either to prevent core saturation or unnecessary losses in the low voltage semiconductors. The peak flux density

of design was set at 0.2 Tesla, which is well within the capabilities of ferrite at 20 kHz. A design target of 10% of the power transfer current was utilized as the upper bounds on magnetizing current to reduce conduction losses in the transformer and primary-side power electronics. Reducing these targets further would be a tradeoff with increased isolation capacitance, turn-turn capacitance, and series resistance due to more windings. Equations (5-4) through (5-6) below show the quick design steps starting with dc-link current.

$$I_m = \frac{I_{dc}}{N} * 0.1 \tag{5-4}$$

$$L_m = \frac{V_p}{2\, I_m f_{sw}} \tag{5-5}$$

$$N_P = \sqrt{L_m \mathcal{R}_{core}} \tag{5-6}$$

To handle the isolation voltage between primary and secondary, and turn-turn voltage breakdown on the secondary a custom bobbin was utilized. First the secondary is wound on a bobbin with multiple sections limiting the max turn-turn voltage to 1/8th total voltage. Then a cover of 14mil Nomex was constructed and utilized as a mold that was then filled with potting material. After potting, the primary winding was wound on to the bobbin followed by a coating of varnish was applied via vacuum pressure impregnation (VPI). The finished transformer is shown in Figure 5-15.

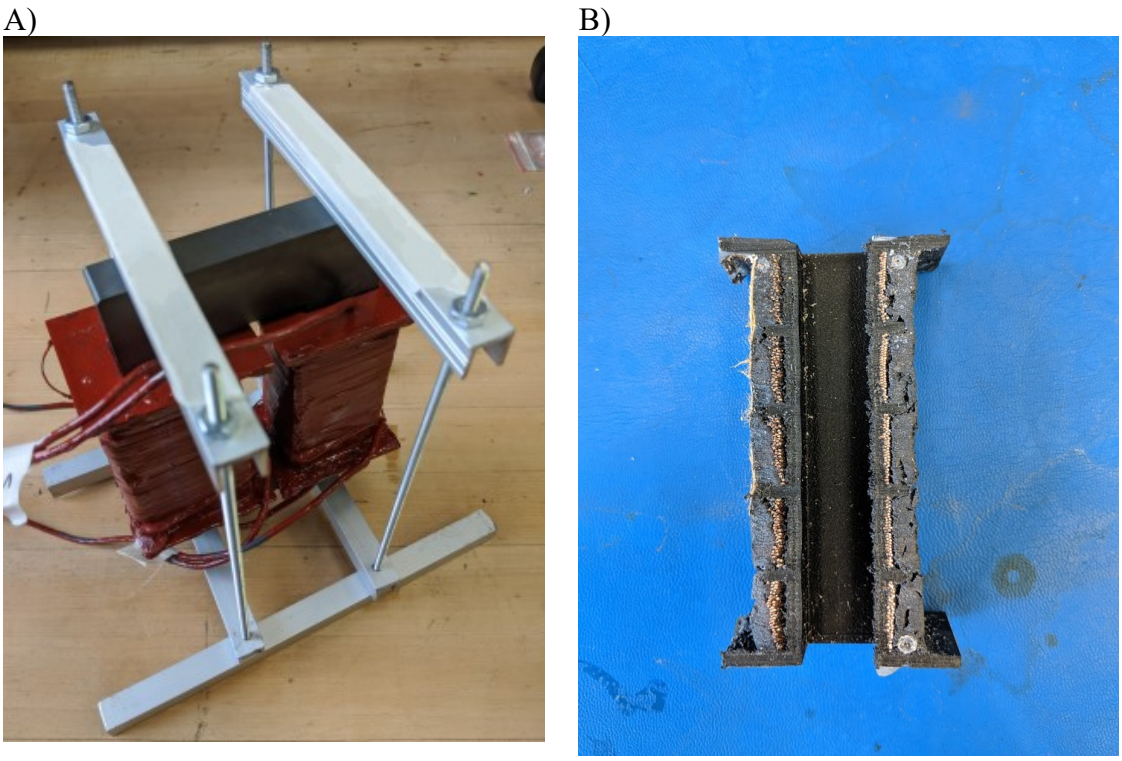

Figure 5-15. A) Front-end step-up transformer B) transformer winding cut in half showing turn-turn isolation and primary to secondary isolation.

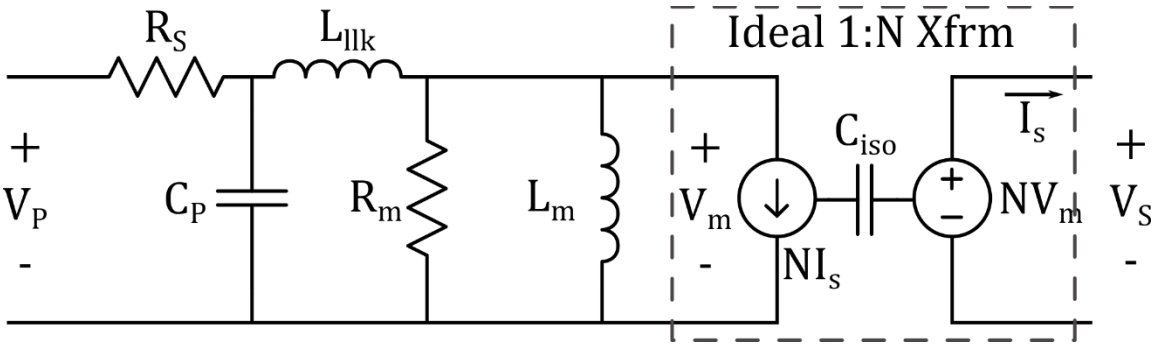

Figure 5-16. Transformer Circuit Model, primary referenced

The built transformers were characterized on an E4990A Impedance analyzer and shown in Table 5-3. The series resistance of the coils was measured with the bobbins not on cores, so the resistance of each coil could be measured independently. The leakage and magnetizing inductance values were determined from standard open circuit and short circuit tests form the primary side. The isolation capacitance between primary and secondary was measured with the terminals shorted.

Table 5-3. Front-end step-up Transformer Parameters

Parameter	Description	Values
$R_{S,\ p\text{-}dc}$	Primary winding resistance measured from primary at dc without core	0.14 Ω
$R_{S,\ s\text{-}dc}$	Secondary winding resistance, measured at dc on secondary without core	2.8 Ω
$R_{S,\ p\text{-}20\ kHz}$	Primary winding resistance measured from primary at 20 kHz without core	0.25 Ω
$R_{S,\ s\text{-}20\ kHz}$	Secondary winding resistance measured from primary at 20 kHz without core	4.2 Ω
L_{llk}	Leakage inductance measured on primary, secondary shorted	0.05 mH
L_m	Magnetizing inductance measured on primary, secondary open circuited	12 mH
N	Transformer turns ratio Ns/Np	7.4
C_P	Parallel capacitance, measured on primary	2000 pF
C_{iso}	Isolation capacitance, measured with windings shorted	80 pF

5.4 Common Mode

Current source inverters create common mode components and can be modelled as a voltage source [52]. These common mode components lead to additional current flowing in the system resulting in excess power loss and can lead to interference. A schematic diagram of the drive with important parasitic common mode components is shown in Figure 5-17 and the common mode voltage source of the CSI is defined from the 5 terminals of the inverter to ground in (5-7).

$$V_{cm} = \frac{V_{ag} + V_{bg} + V_{cg}}{3} - \frac{V_{pg} + V_{ng}}{2} \tag{5-7}$$

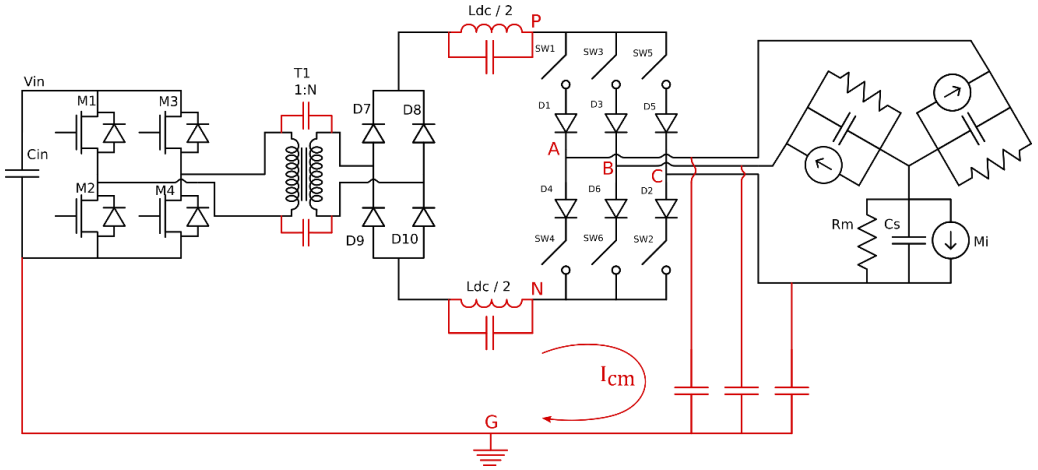

Figure 5-17. SEM drive schematic with important common mode components included

This voltage source has a high frequency component produced by the switching action of the inverter and a low frequency component from the SVPWM changing sectors at six times the fundamental frequency. These components can be seen in the waveform of Figure 5-18 when the system is simulated with 300 pF of capacitance to ground per-phase. With the sector changes producing a transient at six times the fundamental superimposed by the switching frequency effects. The Fourier decomposition of the common mode waveform in Figure 5-19 shows the significant low frequency components. The common mode current that flows in the system is determined by the equivalent common mode impedance of the power electronics and machine.

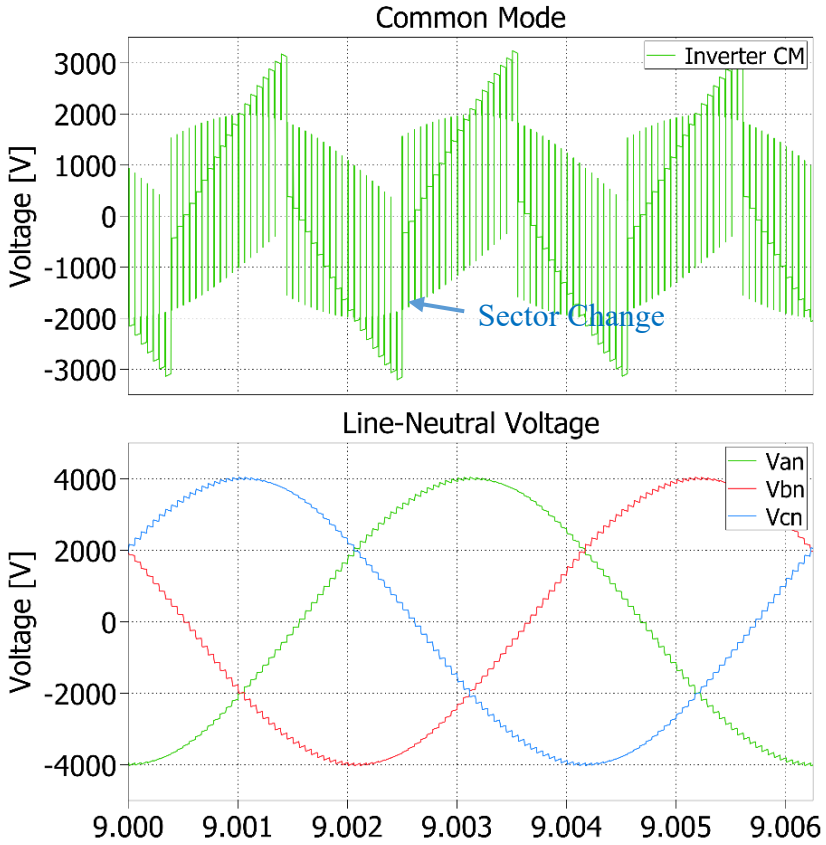

Figure 5-18. Simulated Inverter Common Mode Voltage and SEM Line-Neutral Voltage operating at rated torque, 100 RPM, and 18 kHz switching frequency

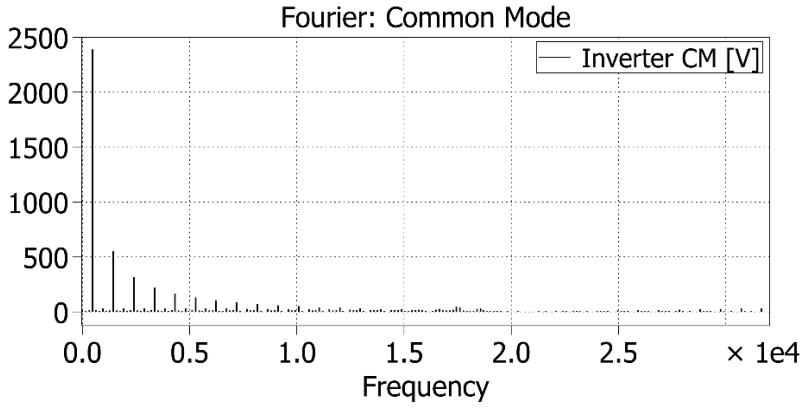

Figure 5-19. Fourier decomposition of common mode voltage waveform

The main elements affecting the impedance between the inverter and ground are the motor parasitic capacitance and the cabling between the drive and machine as shown in the simplified equivalent circuit of Figure 5-20. The machine is modelled with a π circuit consisting of a capacitance from stator to ground, and rotor to ground, combined with the common mode coupling between the stator and rotor. The system utilizes three 1-φ 12-foot safety high voltage coax cables [90] to connect the inverter cabinet to the drive. These cables provide double insulation and combined with the mating connectors make a touch safe connection for the medium-voltage drive system. However, the shield of the coax-cable is grounded and increases the system parasitic capacitance to ground. The measured parasitic capacitance elements are shown in Table 5-4.

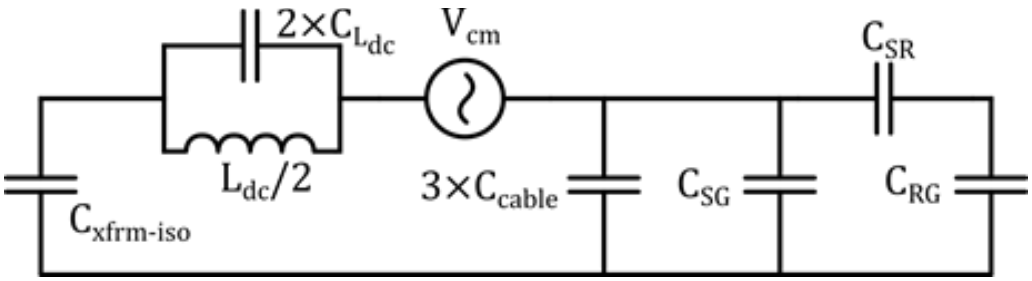

Figure 5-20. Simplified Common Mode Equivalent Circuit

Table 5-4. Measured System Common Mode Capacitances

Transformer	$C_{xfrm\text{-}iso}$	80 pF
dc-link Inductor	C_{Ldc}	10 pF
Cable-Capacitance	C_{cable}	360 pF
Stator-Ground	C_{SG}	980 pF
Rotor-Ground	C_{RG}	180 pF
Stator-Rotor Common Mode	C_{SR}	1400 pF

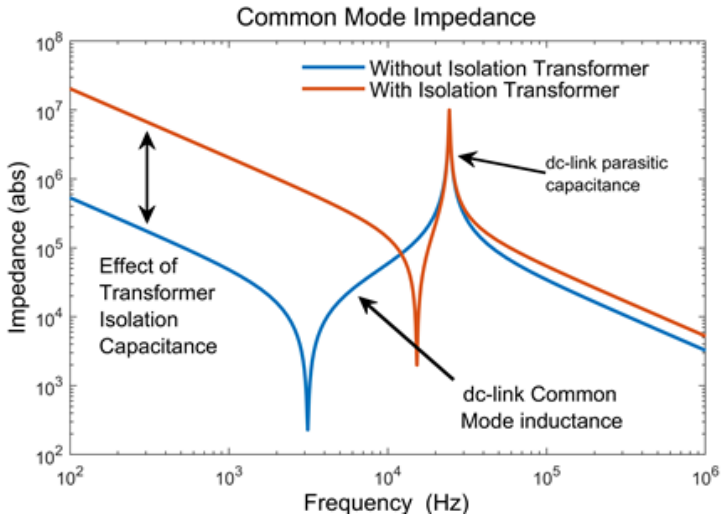

Figure 5-21. Effects of isolation transformer on common mode impedance

The parasitic capacitance of the magnetic components is in series with the output impedance and influences the overall impedance of the circuit. The inductor provides increasing impedance up to its resonance frequency. The isolation transformer introduces a series capacitance, and if designed properly, can increase the low frequency impedance by an order of magnitude as shown in Figure 5-21.

Increasing the low frequency common mode impedance of the SEM drive is necessary to suppress the low frequency multiples of the fundamental component of the common mode source. Without this impedance in the system it was observed in testing that increased

common mode content caused measurement error on voltage and current sensors that limited the implementation of self-sensing control. If the super-cascode heatsinks were grounded the impedance would be further reduced, negatively impacting performance.

5.5 Chapter Summary

This chapter covered the hardware implementation of the CSI system including the dc-link and front-end components. The CSI was implemented with the normally-on JFET super cascodes developed in *Chapter 2*. However, in the CIL testing of *Chapter 2*, the parasitic components affecting the performance of the switches was not considered. Here it was shown how parasitic capacitances contribute additional switching loss in the system. These components are significant due to the high impedance of the system, resulting in small capacitors (1 ~ 100 pF range) contributing currents during dv/dt events whose peaks larger than the average dc-link current. The implication of these effects is that the parasitic capacitances introduced by heatsinks can have a significant effect on system performance, and these are confirmed in *Chapter 6.*

The dc-link inductor while storing minimal energy (<1 J) is required to be 3.4 H. This creates an implementation challenge since a tiny capacitance of a few pF results in a self-resonance just above the switching frequency. Multi section bobbins and series connection of inductors were implemented to mitigate the problem. However, it was shown with an alternative design incorporating 10 series connected small inductors, that there are diminishing returns on this strategy. The series connection stops behaving as a bulk inductor and capacitor, introducing multiple resonances, and coupling elements lowering the impedance of the inductor over certain frequency ranges. This is an inherent problem with the medium voltage low power nature of this machine. However, as the power of the

machine increases, the current level required to drive them will increase resulting in the necessity of a lower value of inductance. The stored energy will increase, and the size/weight of the inductor might increase as well, the self-resonance problem will improve at lower inductor values. This trend is supported by the success of high-power medium-voltage CSIs in large industrial and utility applications that are widely in use.

The common mode impedance of the machine and drive components were measured and the critical components necessary to provide an overall high impedance loop were identified. The machine and cabling have comparably high capacitance so the magnetic components in the system are used to increase the loop impedance. At low frequencies, the isolation transformer of the front-end must have a low isolation capacitance to limit the ground currents flowing in the system. At high frequency, the dc-link inductors parasitic capacitance dominates the overall impedance.

The next chapter characterizes the losses of the system and validates the control theory developed in *Chapter 4.*

Chapter 6: SEM Drive System Testing

The testing of the SEM drive detailed in *Chapters 4 and 5* is presented in this Chapter. First the system modeling, dc-link instability and proposed controllers of *Chapter 4* are evaluated. The effectiveness of the virtual resistance in stabilizing the dc-link is confirmed and correlated with theory. The limitations regarding increased load changes of the controller with virtual resistance are confirmed and the improved performance of the controller with voltage decoupling is shown.

Next a loss characterization of the drive vs load, fundamental frequency, dc-link current, and switching frequency was performed. The losses are analyzed, and a sensitivity analysis compares the impacts of the system parameters on the losses. Accurate measurement of power in and out of the dc-link is challenging due to the medium voltage PWM content, but a loss breakdown utilizing modified test setups and thermal measurement is presented. Finally, the impacts of the heatsink and dc-link designs are compared.

The SEM drive system utilized two loads for characterization. The first load is a configurable passive R-C load bank used to emulate the effective machine impedance vs operating point. The load consisted of five 100 kΩ resistors configurable in series-parallel combinations and a 14 nF film capacitor. This load was utilized to evaluate the power electronic losses vs operating point, simplifying the power electronics loss measurements. The second load utilized the SEM mounted on a dynamometer for evaluation of the dc-link dynamics. The dyne machine was set in constant speed-mode, and the torque was controlled via the CVVR and SEM. The dynamics of the dc-link were confirmed with

signal injection from the front end full-bridge. More information on the dyne setup is in [3].

6.1 dc-link Control

An inherent dc-link instability caused by the interaction of the CVVR torque modulator and dc-link was shown analytically and in simulation in *Chapter 4*. This section utilizes small signal perturbation to confirm the system modelling and the effectiveness of the virtual resistance in stabilizing the system. The improvements to disturbance rejection and capability of the dc-link to withstand torque transients provided by the virtual resistance is demonstrated as well. Additionally, the response provided by the alternative controller with q-axis voltage decoupling is compared to the controller with virtual resistance.

6.1.1 Small Signal Injection Method

The established method of signal injection and measuring the corresponding response was utilized to confirm the small signal modelling of the system in *Chapter 4*. The DSP controller for the system generated a chirp signal that is injected at the output of the PI controller as shown in Figure 6-1. The dc-link response of the system was then extracted from the sensed dc-link current. An example of the time-domain injected signal, control response and dc-link response are shown in Figure 6-2 with the average steady state value removed. The implementation on the DSP limited the frequency resolution and sampling due to limited storage. Separate chirps for each decade of frequency measured were utilized to increase the resolution and allow for modification of the injection magnitude. At low frequencies, the undamped system required small injections or else it caused the small signal assumptions to no longer be valid. Conversely, the damped system required a larger injection to cause a response. At higher frequencies, the dc-link impedance is determined

by the inductance and not the controller, so both the damped and undamped testing utilized the same injection percentage. This same increased impedance of the dc-link reduces the measured response, which ultimately degrades signal to noise ratio above 100 Hz. Attempts to inject larger signals resulted in non-linear operation of the system.

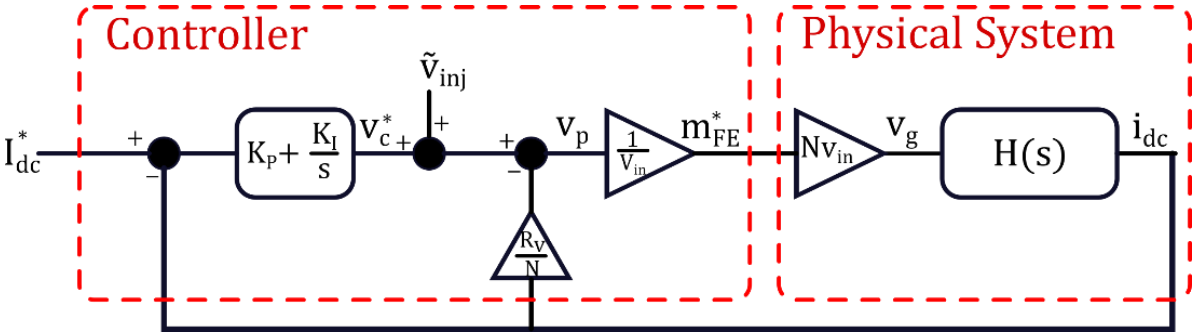

Figure 6-1. Small signal injection for dc-link dynamic testing

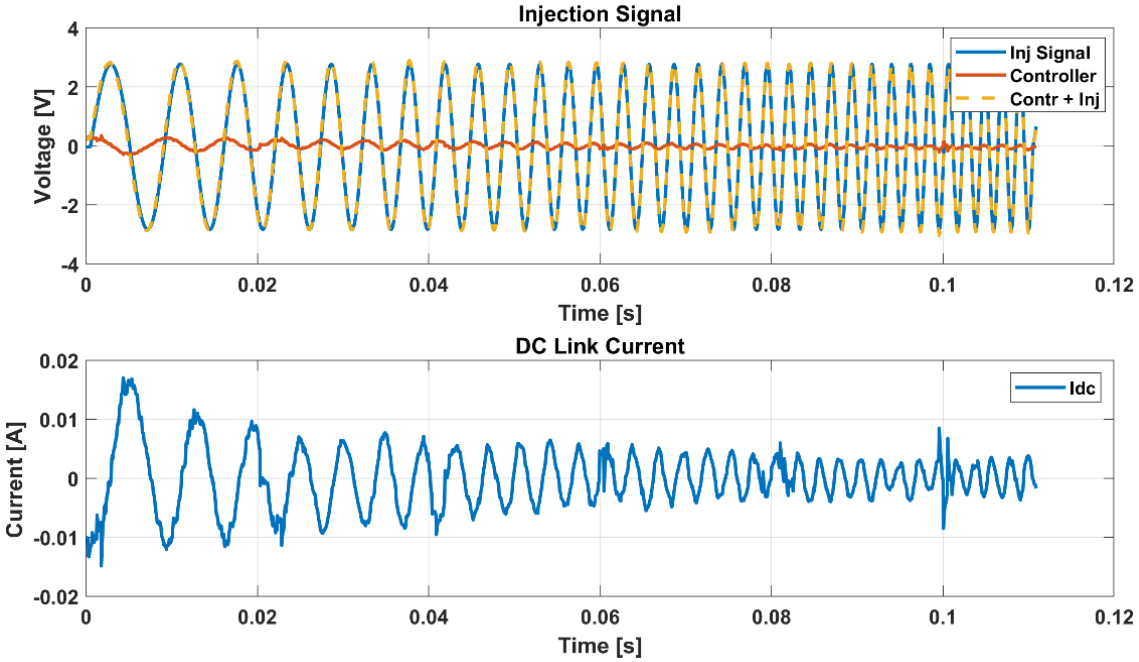

Figure 6-2. Example measured injected signal and response in time-domain

6.1.2 Measured Dynamic Response

The system was operated on the dyne at a constant speed with the parameters in Table 6-1. The existence of the instability was confirmed by providing a slow (-50V/s) q axis voltage ramp command at 200 RPM. The slow q axis voltage ramp in Figure 6-3 confirms that without the virtual damping resistance when the output power of the CSI increases the stability condition of (4-19) is not met, causing the dc-link to oscillate and eventually collapse. The CVVR controller detects the fault and stops the output voltage while the dc-link recovers. When the virtual damping resistance is added, the dc-link current is stable, and the system completes the command.

Table 6-1. Operating point and control parameters used during dc-link control testing

Field Voltage	V_F	3 kV
dc-link Current	I_{dc}	200 mA
Proportional Gain	K_P	20
Integral Gain	K_I	100
Virtual Damping Resistance	R_V	3000 Ω
CVVR Bandwidth	F_{CVVR}	150 Hz

A stable operating point of 100 RPM and -500 V q axis voltage were utilized so the system could be characterized with and without the virtual damping resistor effects. The measured closed-loop system response results are overlaid with the analytical model in Figure 6-4. The analytical model loss mechanisms were calibrated with the measured system losses. The signal to noise ratio reduced the matching between the measured and analytical results at frequencies above 100 Hz,

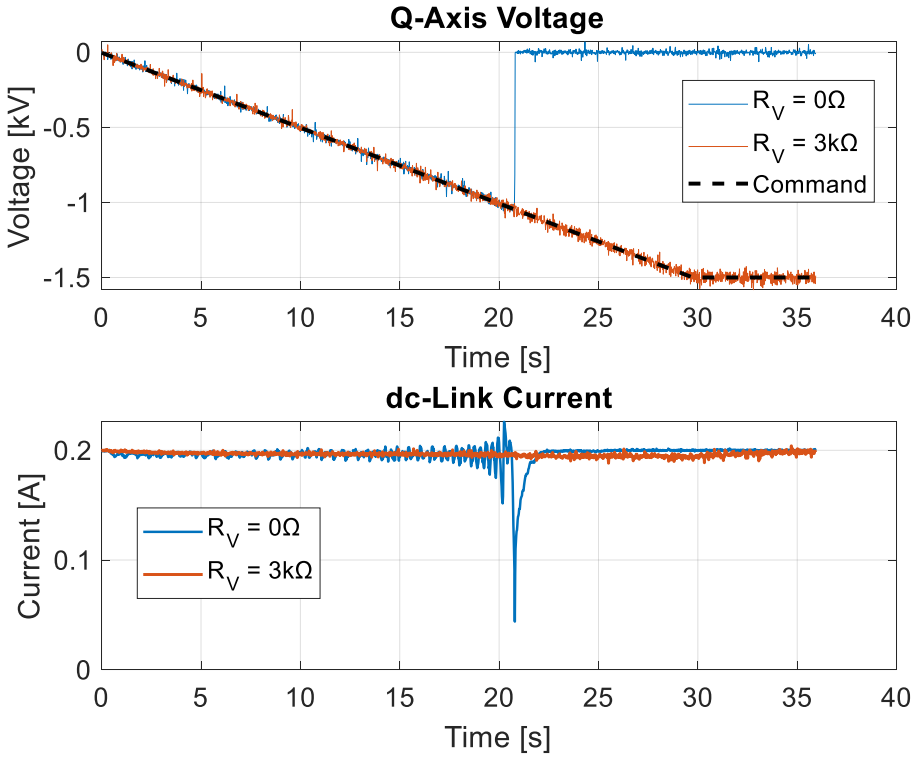

Figure 6-3. Measured slow q axis ramp showing the small-signal instability of the dc-link

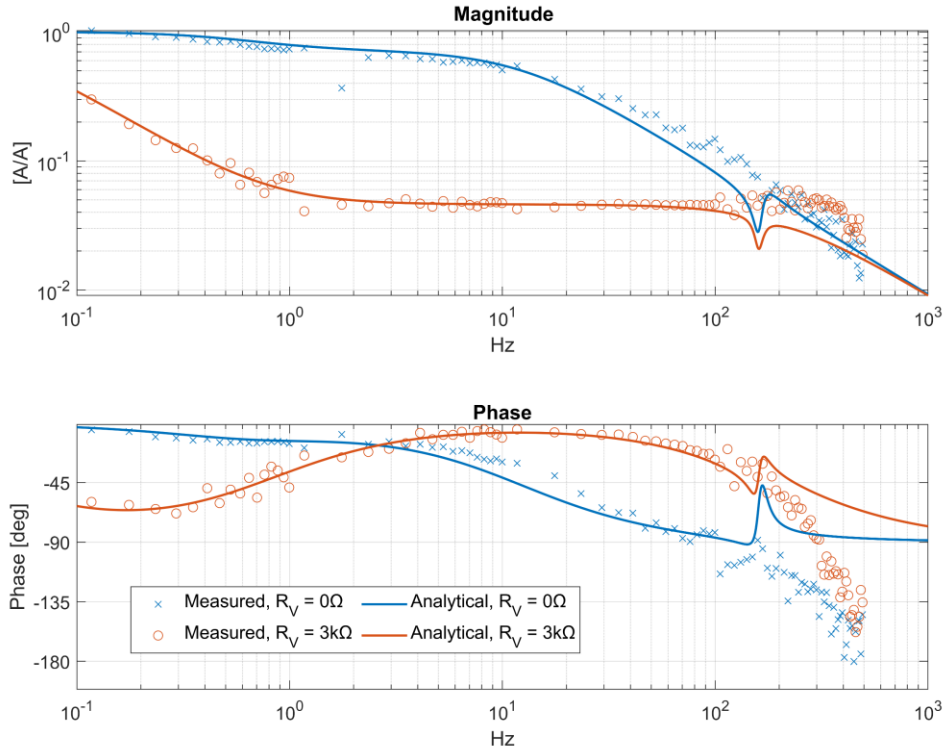

Figure 6-4. Measured vs. Analytical closed loop transfer function with and without virtual damping at 100RPM and -500V q axis

The CSI and SEM system with a torque modulator bandwidth of 150 Hz is capable of fast torque steps (14ms rise time) [14], that must be rejected. However, Figure 6-4 shows the low bandwidth (<0.1Hz) of the front-end system so the PI controller will not provide significant response. The analytical model in *Chapter 4* shows that when CSI changes output voltage the dc-link will be subjected to a voltage disturbance. The front-end was utilized to artificially provide a disturbance to the dc-link and the dynamic stiffness of the dc-link can be measured. Figure 6-5 shows the effects virtual resistance has on the dc-link impedance and is overlaid with the analytical dc-link impedance.

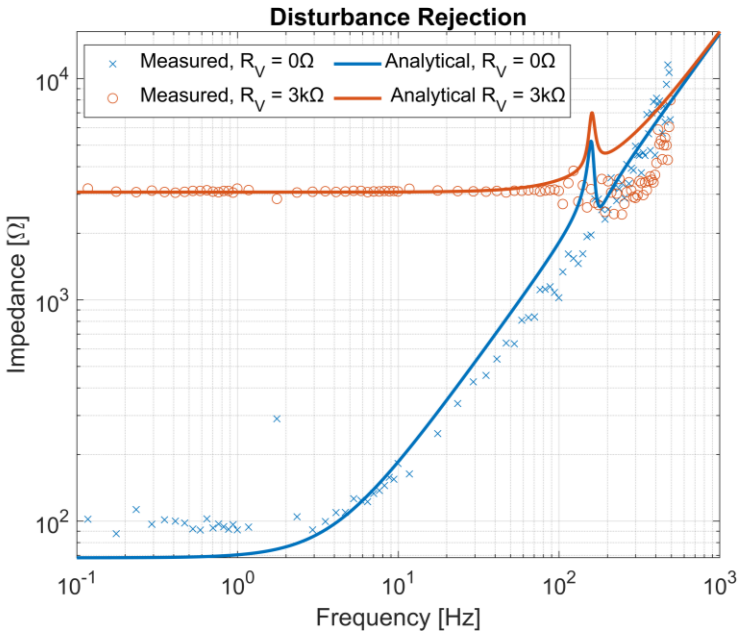

Figure 6-5. Measured vs Analytical dc-link disturbance rejection with and without virtual damping at 100RPM and -500V q axis

The increased dc-link impedance enables the system to withstand increased SEM torque dynamics by minimizing the disturbance to the dc-link current. The effects of this increased impedance are clearly seen in Figure 6-6, where -1 kV *q* axis voltage ramps were commanded from the CVVR with increasing ramp rates. For the slowest ramp of 1000 V/s, the system without damping sees a significant drop (25%) in the dc-link current but

manages to ride through the transient. When the ramp rate increases to 18 kV/s (middle set of graphs) the dc-link collapses entirely and the CVVR stops the transient. In contrast, when the virtual damping is utilized, the dc-link response to a 90 kV/s ramp-rate is virtually identical to the 1 kV/s ramp-rate.

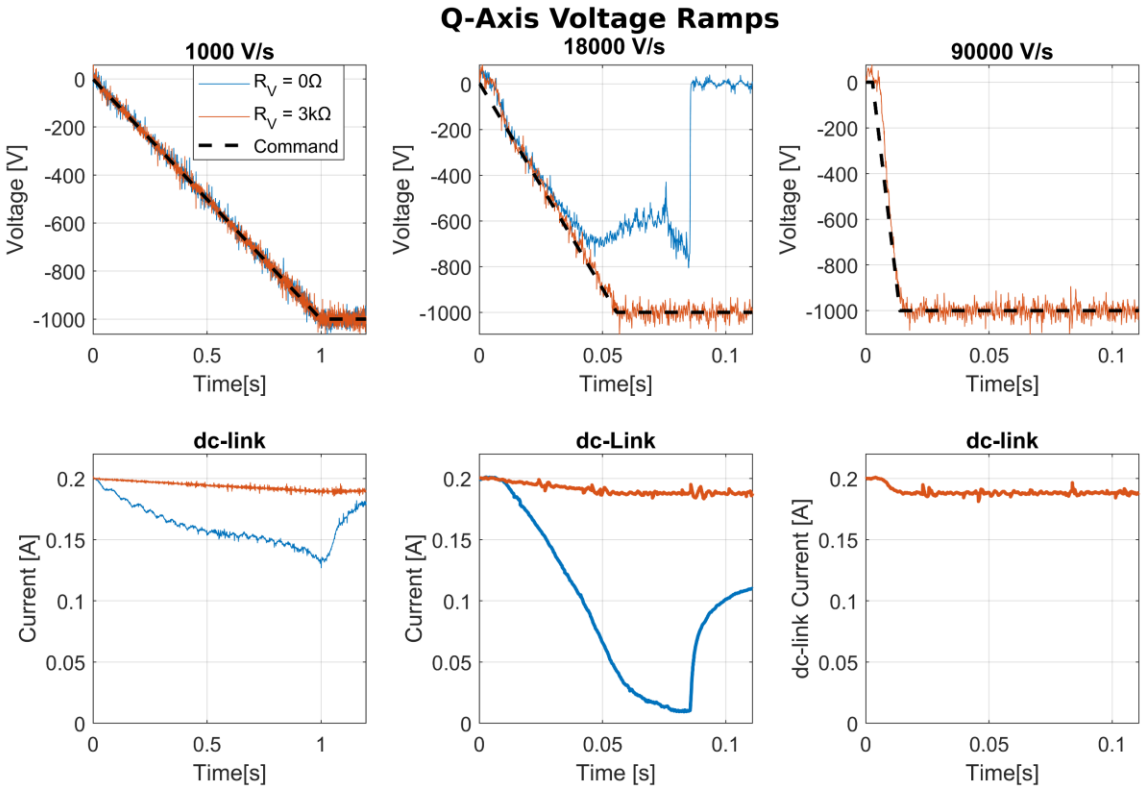

Figure 6-6. Effect of a 1kV q axis voltage ramp with increasing ramp rate on dc-link current with and without virtual damping at 100 RPM

Chapter 4 predicted the reduced effectiveness of the virtual damping resistance when the load transients are increased. Figure 6-7 shows that increasing the speed to 200 RPM and the torque step to 1.5 kV reaches the limits of the 3 kΩ virtual resistance with a significant drop in dc-link current causing the system to encounter a non-linearity. Figure 6-8 shows the system initially operating at the reduced dc-link current and then abruptly recovering to the commanded dc-link current response. The front-end commanded voltage and CVVR commanded currents are included in Figure 6-8 to show that this is not a system

saturation problem. As shown in the initial transient of Figure 6-7 the virtual resistance to 6 kΩ limits the droop in dc-link current and maintains the linear operation of the system. However, the increased time-constant of the system is visible in the longer time capture in Figure 6-8 where the dc-link still has not returned to steady-state after 4 seconds.

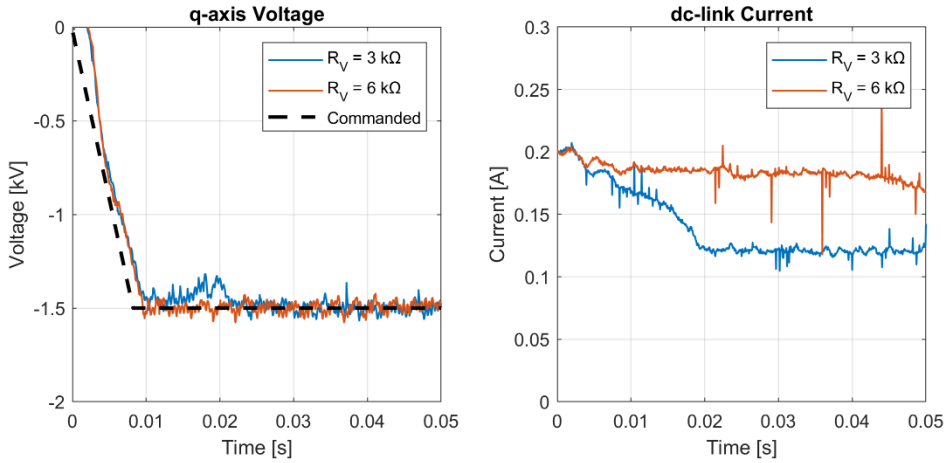

Figure 6-7. dc-link response to q-axis step at 200 RPM with different virtual resistance values

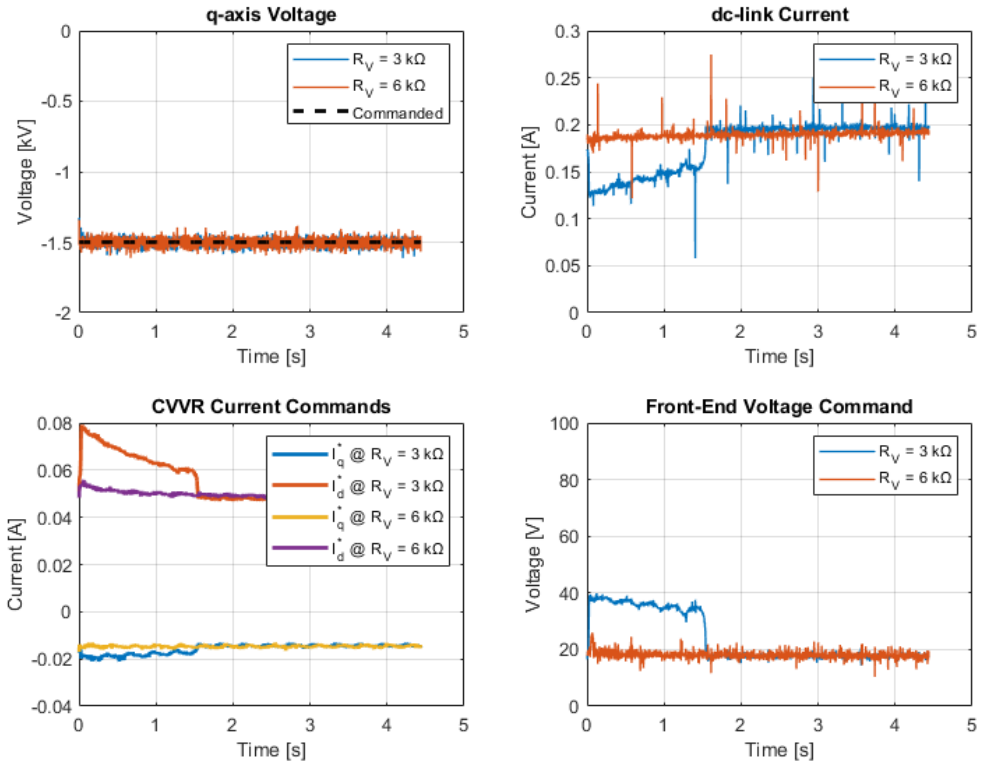

Figure 6-8. Extended response of system to q-axis step response at 200 RPM showing non-linearity when insufficient virtual resistance is utilized

6.1.3 Virtual Resistance vs. q-axis Voltage Decoupling

An alternative controller that overcomes the time-constant and load-step size limitations of virtual resistance by decoupling the voltage disturbance created by the q-axis of the CVVR and SEM on the dc-link was proposed in *Chapter 4*. However, the implementation utilizes a commanded q-axis voltage signal and simulation in *Chapter 4* predicted an initial overshoot in dc-link current. Figure 6-9 shows the stable response of the system to a 10 ms, 1.5 kV q-axis ramp command and the expected dc-link current overshoot when the measured q-axis voltage lags the commanded voltage.

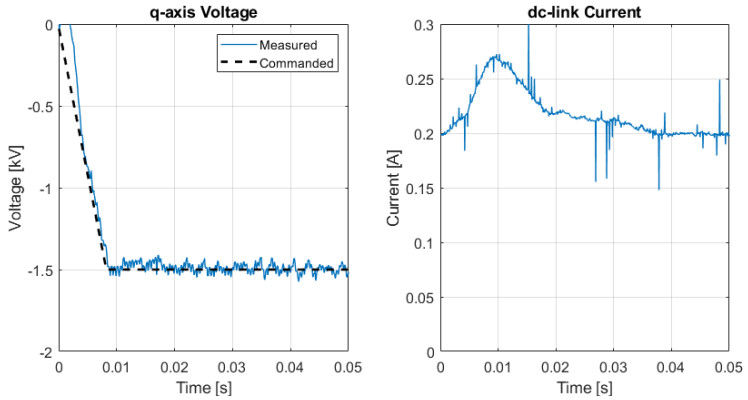

Figure 6-9. Response of system to q-axis voltage steps at 200 RPM with voltage decoupling

The extended response of the system with q-axis voltage decoupling is plotted in Figure 6-10 along with the extended response of the system with virtual resistance. These waveforms show a low frequency ripple content in the CVVR d-axis current command and measured dc-link current. The system conveniently provided an unexpected disturbance at the mechanical rotational frequency of 3.33 Hz, i.e. 200 RPM, which resulted in an unmodelled reactive power component. The controller with q-axis voltage decoupling only removes commanded q-axis disturbances and the reduced disturbance rejection of the dc-link when stabilized using q-axis decoupling instead of virtual resistance was predicted in *Chapter 4*. Conversely, the controller with virtual resistance offers increased disturbance

rejection to all unmodelled disturbances and therefore the dc-link current response does not show this ripple content. The frequency spectrum in Figure 6-11 shows the harmonics content of the commanded front-end voltage output of the controller with virtual damping, and a 3.3 Hz component is present. This was done to confirm the unmodelled disturbance was due to the system and not the implemented q-axis decoupling controller.

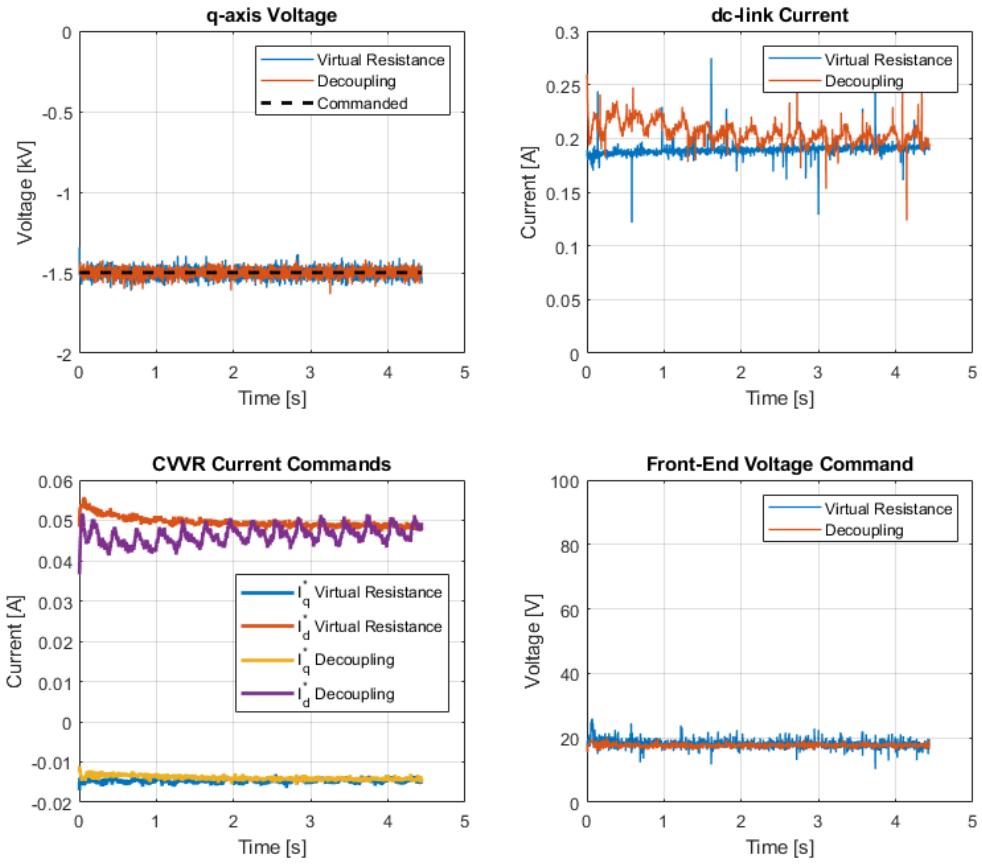

Figure 6-10. Extended response of system to q-axis voltage steps at 200 RPM with virtual resistance and with voltage decoupling.

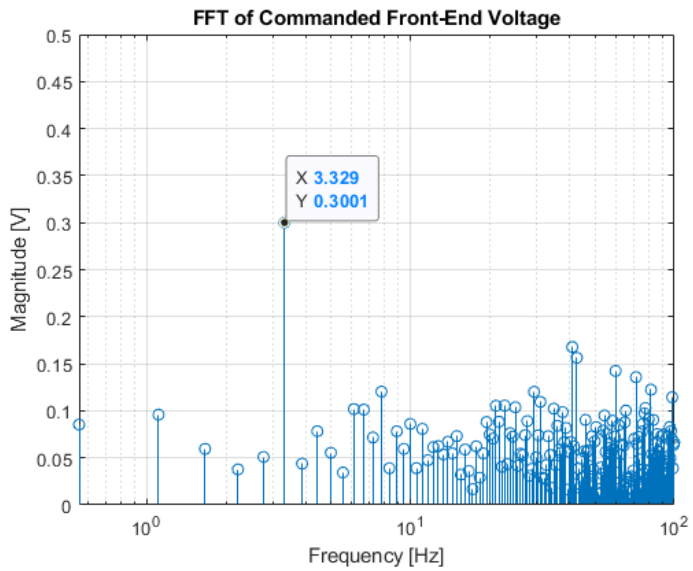

Figure 6-11. Fourier decomposition of command front-end voltage output of dc-link controller with virtual resistance

6.2 Loss Measurement and Sensitivity Analysis

Measuring PWM currents and voltages at a sufficient accuracy level for power loss evaluation is always challenging and it is further complicated by the medium voltage and high common mode components of this system. Specifically, the dynamic response of high voltage probes can have significant impact on measurement accuracy. Researches evaluated a variety of single ended and differential probes for medium voltage application in [91], and concluded the high attenuation ratios of 1000:1 had trouble accurately capturing the high frequency content created in voltage PWM waveforms. Higher end probes providing multiple compensation adjustments offer advantages but required specialty equipment to correctly tune. If set incorrectly, additional error could just be introduced.

The dynamic characterization of the super-cascode in *Chapter* 2 utilized a split dc-link capacitor allowing for the utilization of lower voltage 100:1 probes with a peak rating of 4 kV with a 100 MHz bandwidth and 1% accuracy rating [47]. Additionally, a setup specific

for CIL allows for minimizing the measurement geometry and prioritizing the sensing of the device under test. However, in the CSI system this was no longer possible and measurement of voltages exceeding 4kV to ground was necessary. This required the use of 1000:1 40 MHz 6% accurate probes [92]. It was found that the lower bandwidth and higher inaccuracy of the probes distorted the PWM waveform compared to the 100:1 1% accurate probes. However, if the probes were all compensated equally it was possible to create differential measurements using the 1000:1 probes that matched the 100:1 probes for the content of the fundamental frequency. Utilizing the same setup, and commanding the same output current, the line-line voltage of the system created from single ended measurements for the 100:1 and 1000:1 probes are shown to be within 1% of each-other to the max rating of the 100:1 probes in Figure 6-12.

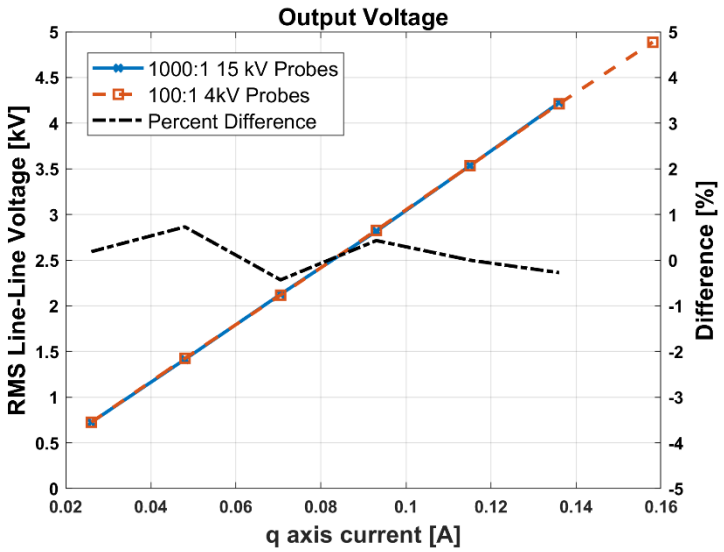

Figure 6-12. Measured output voltage comparison between 100:1 and 1000:1 probes

With the 1000:1 probes validated for low frequency measurements the system losses are evaluated at the input and outputs of the system where the waveforms are suitably filtered. The low voltage input power was calculated from RMS voltage and current digital multi-meters (DMM) measurements. The output power was calculated from measured

oscilloscope RMS voltage waveforms and known resistive load value. With only these two measurement points it is not possible to directly parse the losses between the different power conversion stages. To provide insight into the losses, the system parameters consisting of dc-link current, switching, fundamental frequency, output voltage, and output power were varied as summarized in Table 6-2.

Table 6-2. System Operating Point Variation for sensitivity analysis

dc-link Current	I_{dc}	200 → 400 mA
Inverter Switching Frequency	$f_{sw,\ CSI}$	9 → 18 kHz
Fundamental Frequency	f_e	200 → 800 Hz
Output Voltage	V_{LL}	2.1 → 4.9 kVrms
Output Power	*Po*	10 →525 W

The measured system loss vs parameter changes are plotted in Figure 6-14 where linear curves were fit to the data for each operating voltage in 700 V increments from 2.1 to 4.9 kV_{rms}. The linear equations were good fit for the data with high r-square values for the majority of the lines fitting above 0.95 as shown by the histogram in Figure 6-13. The very low fitted values are for the variable output power curves that had minimal slope. The complete curve fit parameters and r-squared values are included in Appendix C.

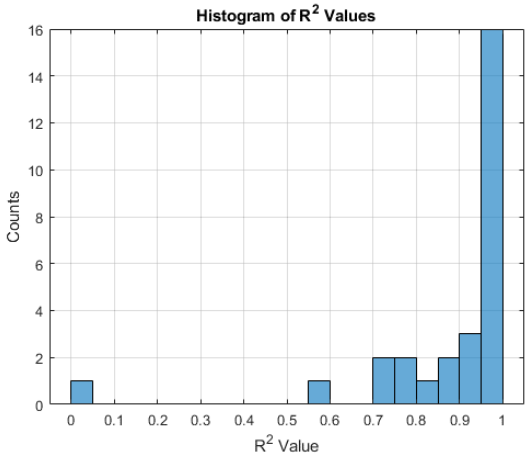

Figure 6-13. Histogram of curve fit r-square values

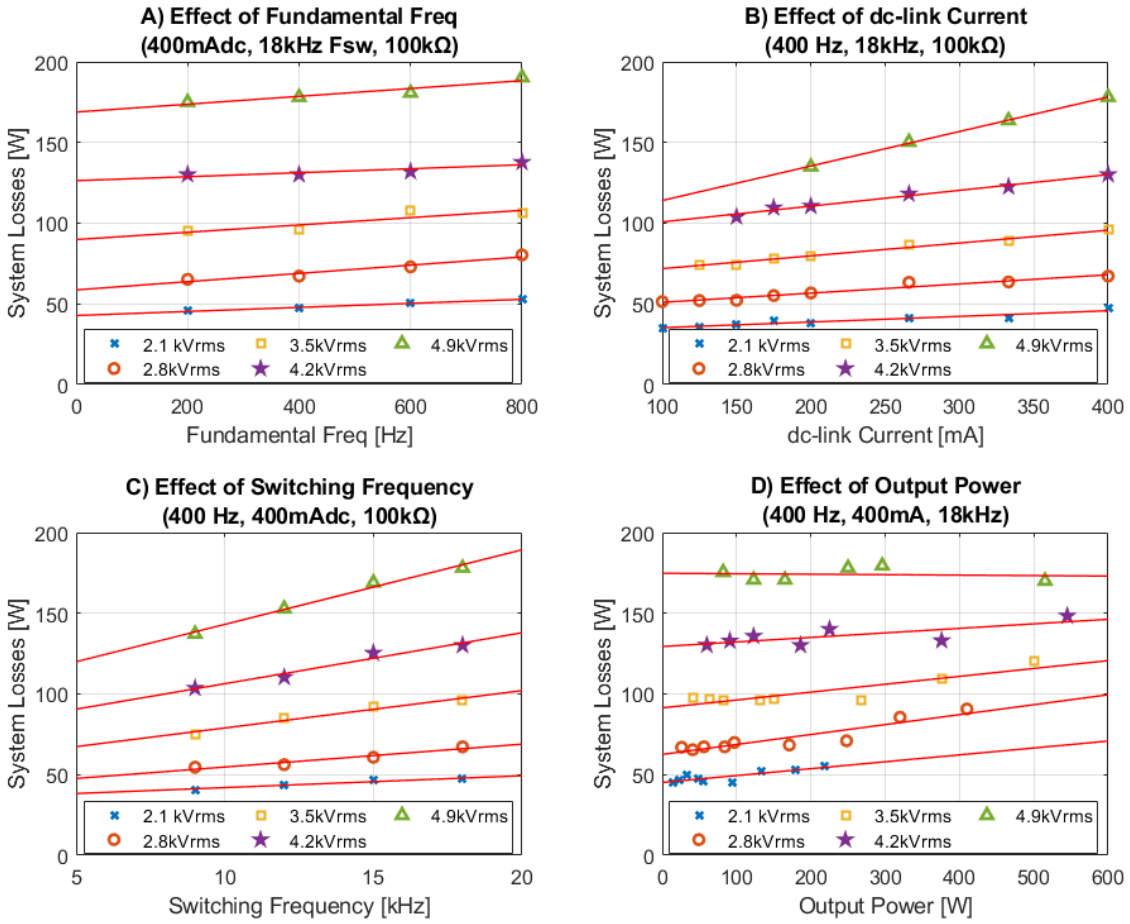

Figure 6-14. Measured system loss vs parameter changes for various line-line operating voltages

The dc-link current and switching frequency had significant effects on the losses as expected from [93]. However, the dominant loss characteristic was the output voltage, which had a quadratic effect on the system losses. The results are plotted vs output voltage at 400 Hz fundamental frequency in Figure 6-15-A. At maximum output voltage the losses are reduced by 24% by reducing the dc-link current and then an additional 22% by lowering the switching frequency. Using the slopes of the fitted lines the sensitivity of the system losses was defined for each parameter in (6-1). Where P is the system power loss dependent on the varied parameter x and x are the parameters in Table 6-2. The sensitivities are

normalized to the maximum system power loss of the result and the maximum value of the varied parameter x.

$$S_x^P = \frac{\max(x)}{\max(P)} \frac{\partial P(x)}{\partial x} \tag{6-1}$$

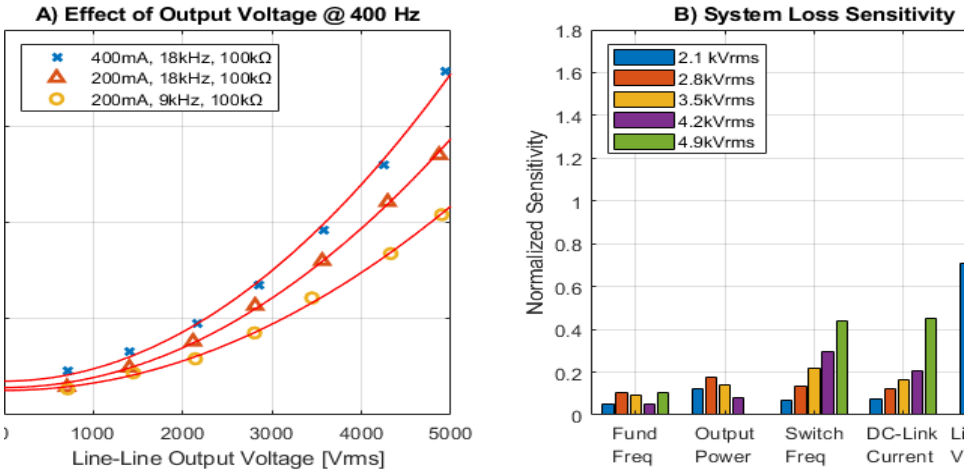

Figure 6-15. A) Measured system loss vs Output Voltage B) Sensitivity of Loss vs parameter change

The loss sensitivities are graphed in Figure 6-15-B and while the losses are higher than desired, they do confirm several key predicted modeling outcomes from *Chapter 3:*

- Significant dependence on dc-link current and switching frequency
- Minimal effect of fundamental frequency and output power on loss

In addition, the clear effect of voltage and its quadratic effect on system losses is dominant. The system losses being most dependent on output voltage is consistent with parasitic capacitance combined with switching frequency being significant contributors to the losses. In Figure 6-16-A the impact of reducing the switches' parasitic capacitance by removing the heat-sinks shows a reduction in system losses by 20 W (13%) at 18 kHz and by 10W (10%) at 9kHz. The curve fits from Figure 6-16-A were utilized to calculate a difference in power loss trends between the two systems and plotted in Figure 6-16-B. Here, the curves for the different switching frequencies nearly match, showcasing the

system loss dependence on the interaction of parasitic capacitance, switching loss and voltage. The raw data points were not compared due to variations in voltage operating point making comparison inconsistent.

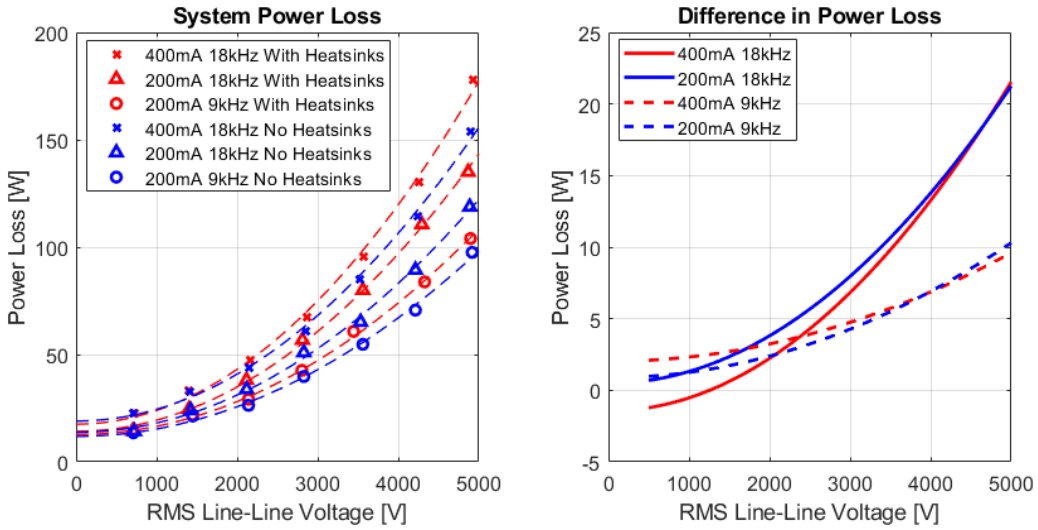

Figure 6-16. Measured effects of removing heatsinks on system power loss

Leakage resistances and magnetic core losses are other system parasitics that contribute losses relative to output voltage. The dc-link has increased dc-link current ripple due to increased PWM content from the CSI dc-link terminals as the with output voltage increases. The increase in current ripple leads directly to increased core and conduction losses. Since the magnetics were not optimized in this system there is significant core material. Specifically, four AMCC-100 [55] core sets were utilized with a combined mass of 4 kg. The excess core material results in increased losses even though the core loss density is low. A variation with a different inductor design is compared in 0. Regarding the leakage resistances, the off-state and isolation resistance was shown to be in the range of 100 MΩ in *Chapter 2*. The off-state leakage currents of the diodes are greater than 100MΩ per device [81]. To better understand the cause of the system losses a breakdown of the losses per subcomponent and type of loss is in the next section.

6.3 Loss Breakdown

The efficiency testing of the system in the previous section revealed significant losses in the drive system and attributed a significant portion to increased switching loss caused by parasitic capacitance. This section further estimates the breakdown of the losses by subcomponent and type by combining analytical estimates with three focused tests consisting of:

1. Front-end efficiency testing on R-L Load
2. Thermal characterization of super-cascode for estimate of loss from thermal measurement
3. Modified dc-link testing introducing a capacitor to dc-link to filter voltage measurement

The first two tests were utilized to set a baseline for losses in the system and serve more for increasing the confidence in the results from the third test. The first test provides a base line for understanding the losses in the front-end power electronics and transformer. The full bridge is expected to have good performance since it is an 80mΩ SiC power module utilized at a relatively low frequency (20 kHz) and low current (less than 2 A average input current). The majority of the front-end losses are expected in the transformer due to the high turn-count secondary. It should be noted that the losses of the dc-link are also included in this measurement so they cannot be used for direct comparison with the full system. Additionally, the full system will have increased losses in the dc-link due to the switching voltage waveforms of the CSI instead of the ideal load resistance of this test.

The front-end was evaluated at 200mA and 400mA dc current from 25 to 400 W and the system power loss and efficiency is shown in Figure 6-17. These numbers are not used

directly in the loss breakdown at the end of this section but serve as sanity check and the main takeaways are:

- The front-end can achieve high efficiency, but at light loads still has significant power loss
- The dc conduction loss of the 32 Ω inductor (AMCC-100 design) accounts for 1.5 W at 200mA and 6W at 400mA.
- Attributing ~15 to 25 W of loss to the front-end is reasonable, but it does include some dc-link inductor loss

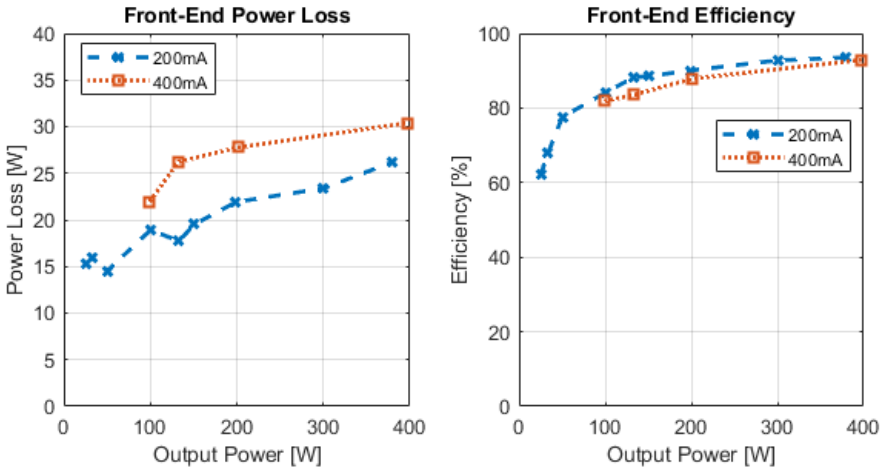

Figure 6-17. Measured Front-End losses when loaded with dc-link inductor and resistance

The second test focused on the thermal package temperature of the super-cascode JFET devices. Not only did removing the heatsinks from the super-cascodes lowered the losses significantly but it also provided an opportunity for a power loss estimate from a temperature measurement. Without a heatsink and no forced air cooling there a significant temperature change was occurring on the TO-254 packaged devices but to estimate the losses from the temperature a thermal characterization was performed first. A dc-current was utilized to excite accurately measured power loss in the JFETs and a Flir E8 thermal camera was utilized for temperature measurements [94]. The measured temperature and

thermal resistance are plotted vs the power loss in Figure 6-18. Natural convection results in a non-linear thermal resistance, however for these devices once the power loss was above a ¼ W it stabilized and the thermal resistance was averaged as 47 °C/W.

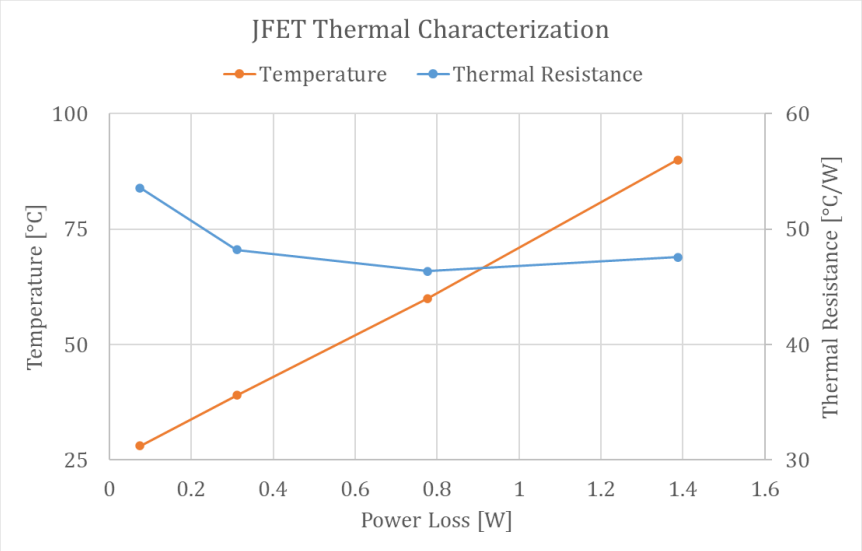

Figure 6-18. Measured TO-254 JFET Thermal Characteristics

This thermal resistance value was utilized to estimate the losses of the CSI when operating normally. The temperature of devices is dominated by switching loss in this application and as was shown in the dynamic characterization of *Chapter 2,* the effect of using non-scaling capacitors causes the devices at the base of the series stack to disproportionality carry the majority of the switching loss. This was visible in Figure 6-19-A where at a peak switch voltage of 2 kV only the bottom two devices (Box 1 and Box 2) are hot. As the voltage increases to 7 kV the seventh device (Box 1 of Figure 6-19-B) has an increased was as hot as devices 1 through 6. The system was operated at a 400 Hz fundamental, 200mA dc-link with 9 kHz switching and the estimated loss of the super-cascodes from thermal-camera is plotted in Figure 6-22. This closely tracked the results graphed in the same figure that were obtained from the third experiment and analytical estimate.

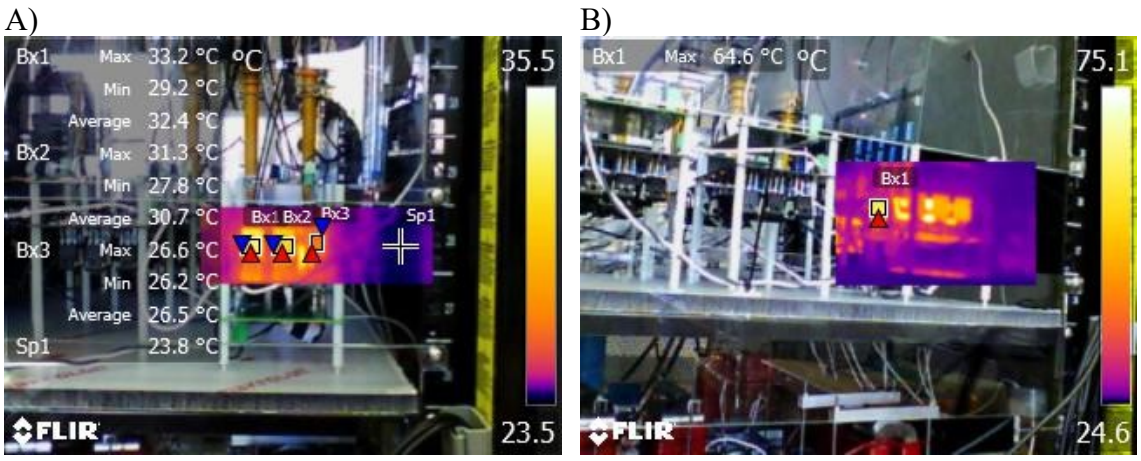

Figure 6-19. Thermal Image of Super-Cascode A) At 2kV line-line peak B) at 7kV line-line peak

The final experiment utilized for breaking down the losses utilized a modified dc-link to alleviate the dc-link voltage measurement issue. The dc-link inductor design with four series connected AMCC-100 inductors allowed for an insertion of a capacitor splitting the dc-link in two halves as shown in Figure 6-20. A small high voltage 30 nF capacitor from Prof. Ludois' personal collection was utilized to create a filtered voltage which provided a measurement point to create another reference power measurement other than the system input and output power measurements. The high voltage differential probes HVD3605A were utilized [95] with the controller measured dc-link current for the mid-point power reference. It should be noted, that the introduction of the capacitor to the dc link (filtering the voltage) makes the testing conditions of the front end and half the dc-link similar to the front-end testing of Figure 6-17.

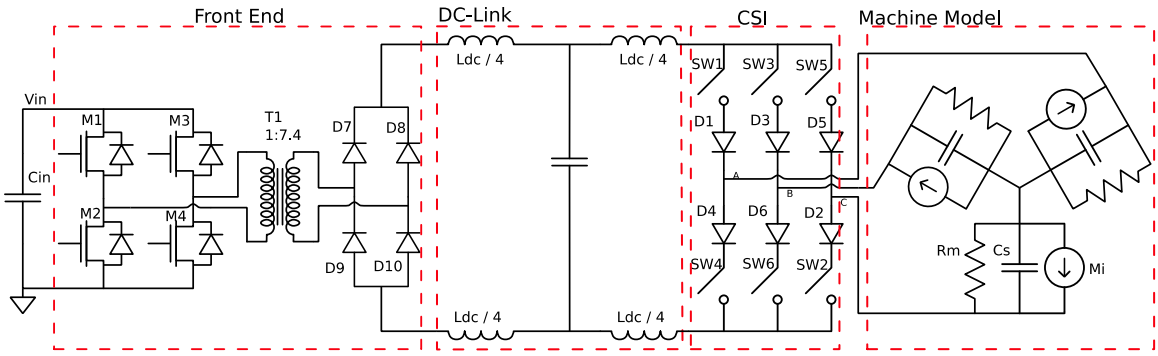

Figure 6-20. Split dc-link with capacitor for power loss breakdown measurement

The system was tested on the RC load configured for 100 kΩ and 14 nF, operating at 400 Hz fundamental, 200mA dc-link and 9 and 18 kHz switching and these results were used for the loss breakdown of Figure 6-22. A graphical representation of how the breakdown was performed is shown in Figure 6-21 where three measurement points serve as baselines for subtracting off more easily estimated losses, e.g. conduction loss. The equations for the calculated conduction losses are:

$$Rectifier\ Conduction = 4I_{dc}V_f \tag{6-2}$$

$$dc-link\ conduction = 4I_{dc}^2R_{dc} \tag{6-3}$$

$$Inverter\ Conduction = 2I_{dc}^2R_{on,sc} + 8I_{dc}V_f \tag{6-4}$$

It was shown in the sensitivity analysis in the previous section the relationship with frequency is linear. Therefore, the switching loss was estimated from the difference in the 9kHz and 18 kHz measurement. The remaining losses in each section are attributed to the catch all categories of front-end and stray.

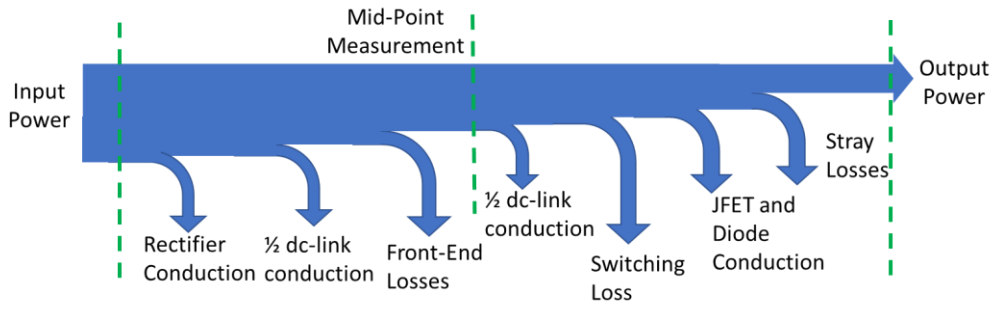

Figure 6-21. Graphical representation of loss breakdown by component from measurement

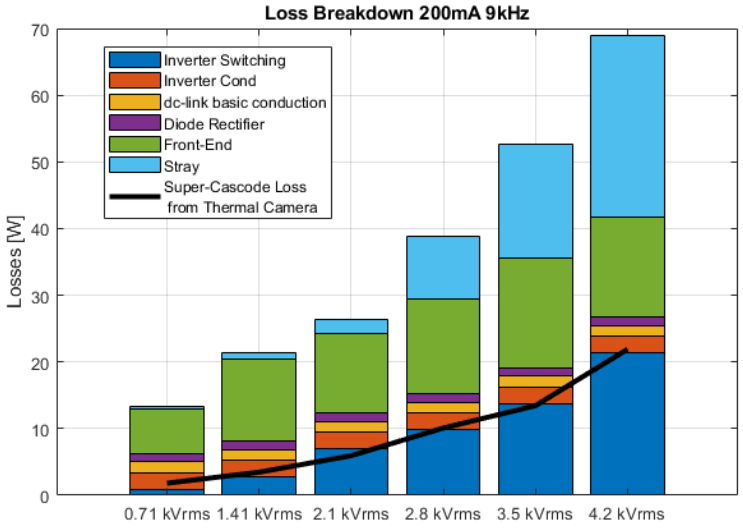

Figure 6-22. Estimated Loss breakdown of CSI system vs Output Voltage, with thermal image loss estimate correlated with super-cascode loss

The resultant loss breakdown vs operating voltage is visualized in the stacked bar graph of Figure 6-22, where the super-cascode loss from the thermal estimate were overlaid. The key takeaways from the loss breakdown are:

- Two independent estimates of super-cascode losses give similar results
- The super-cascode is no longer dominating the total system loss
- The front-end "catch all" loss and the independent front-end testing loss are in the same range, providing confidence to the loss breakdown
- The unaccounted-for stray loss is significant as the voltage increases.

It was discussed in the implementation section that the dc-link inductor was not optimized and had excessive core material. Since the losses increased with output voltage, core losses could be expected to rise as well, since the dc-link current ripple increases with voltage (and/or load). In the following section an attempt at reducing this loss by implementing a variation of the dc-link design is shown. Off-state losses due to resistance

were not accounted for but high pot testing of inverter line-line terminals and line-ground terminals (Table 6-3) resulted in MΩ of leakage resistance, which would only account for 3W of the stray losses at maximum voltage.

Table 6-3. Inverter leakage resistances

V (kV)	Measure Current (mA)			Resistance (MΩ)		
	AB	CB	CG	AB	CB	CG
0.5	0.03	0.03	0.09	16.7	16.7	5.6
1	0.06	0.06	0.16	16.7	16.7	6.3
1.5	0.09	0.08	0.22	16.7	18.8	6.8
2	0.12	0.09	0.32	16.7	22.2	6.3
2.5	0.16	0.12	0.36	15.6	20.8	6.9
3	0.17	0.16	0.45	17.6	18.8	6.7
3.5	0.19	0.16	0.54	18.4	21.9	6.5
4	0.22	0.19	0.6	18.2	21.1	6.7
4.5	0.25	0.22	0.7	18.0	20.5	6.4
5	0.25	0.25	0.76	20.0	20.0	6.6

6.4 Variations

The development of this work included a few variations of components and their effects on the system are document in this section. Both variations are related by the effect of capacitance on the system. The first variation focuses on the parasitic coupling between super-cascodes and the second on increasing the self-resonant frequency on the dc-link inductor while also reducing magnetic core material.

6.4.1 Single vs Six Heatsink for super cascodes

This testing was performed when the RC load was utilized to emulate the equivalent machine impedance at full field voltage. Therefore, the system losses and the difference between them are plotted vs equivalent RPM for three different fixed output voltages Figure 6-27. The difference in system losses is worse at higher voltage, following the overall trend expected from the effect of increased capacitance in the system and the

presented data from the previous section. Inspecting the super cascode current during switching events for both systems in Figure 6-24 drives home the effect capacitance is having on the switching loss. Simple use of individual heatsinks per super cascode provided a reduction in peak current by ~25% and the turn-off time was reduced since there was less linear parasitic capacitance to charge.

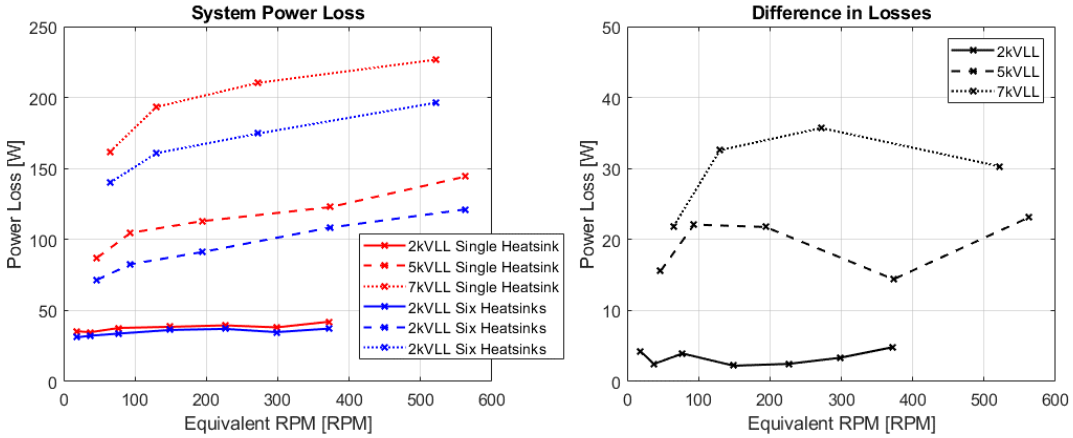

Figure 6-23. Measured effect of heatsink configuration on system power loss

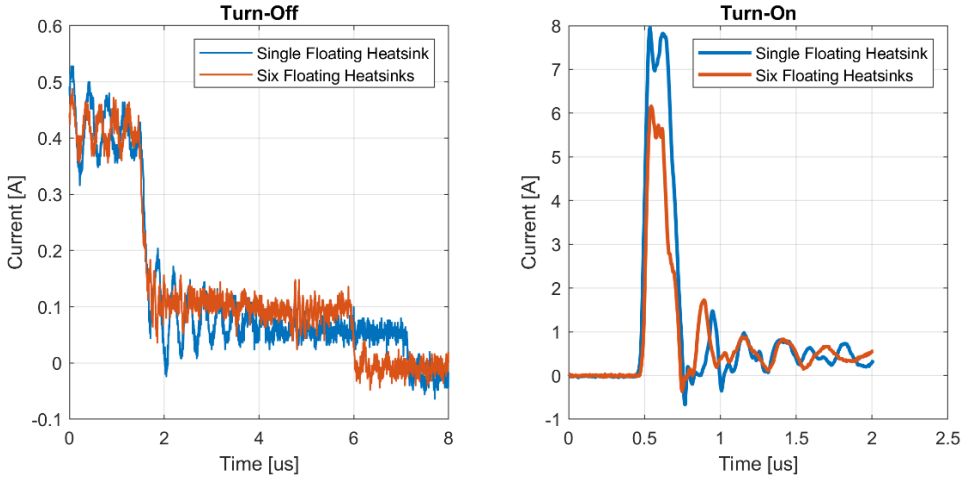

Figure 6-24. Measured effects of heatsink configuration on switching event duration and peak current for a 400mA 5.5 kV switching event on the CSI

6.4.2 dc-link inductor designs

The loss breakdown revealed a significant portion of unaccounted for losses in the system. Potential contributors to the stray loss and difficult to model and measure are core loss and proximity losses of the inductor. Additionally, the characterization of the dc-link inductor in *Chapter 5* shows the self-resonant frequency of the inductor is around 40 kHz with higher than desired parasitic capacitance. A new design with the concept of utilizing many series connected smaller inductors was attempted and the characterization of the inductors was compared in *Chapter 5*, showing the increased self-resonant frequency. This new design, using AMCC-10 cores, has half the magnetizing inductance but a 1/5 of the equivalent parallel parasitic capacitance. However, the series connection results in roughly 3-4x increase in dc resistance.

The new design, with its lower parasitic capacitance presented significantly higher impedance at high frequency. The dc-link current waveforms and harmonic spectrum are shown in Figure 6-25, where the high frequency content is significantly more damped. The effects translate to the common mode in Figure 6-26, where the high frequency content of the line-ground voltage at the inverter output terminal is reduced. However, as shown in *Chapter 5,* the distributed nature of the series connected inductor lowered the impedance due to resonances in the critical frequency range above the switching frequency and increased content in the 18 kHz range was measured.

In Figure 6-27, the effects on system losses are shown. At 200mA the effects were minimal resulting in a slight increase of 4 W for the AMCC-10 design and at 400 mA a significant increase of 16 – 18 W was measured. An analytical estimate from the change in dc-link resistance calculated by (6-5) is plotted predicting the increase in power loss.

$$P_{diff} = I_{dc}^2 R_{dc-AMCC-10} - I_{dc}^2 R_{dc-AMCC-100} \quad (6\text{-}5)$$

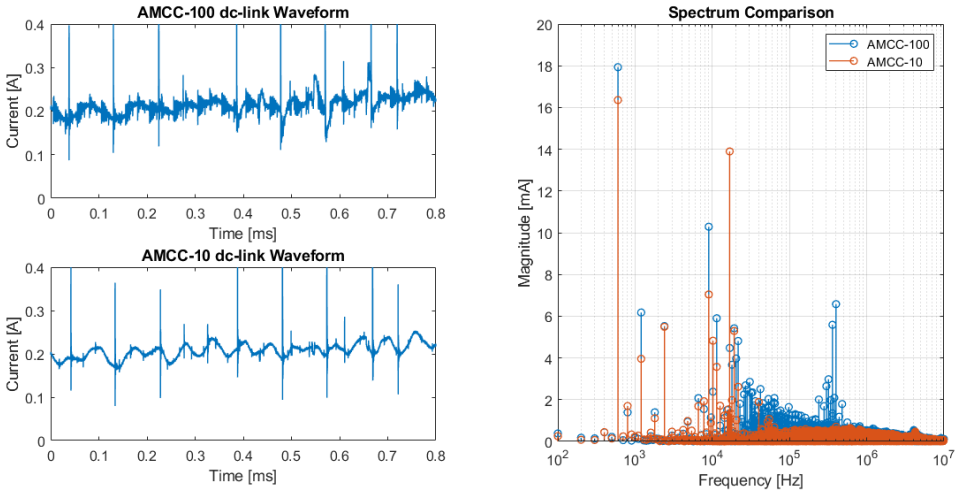

Figure 6-25. Effect of dc-link high frequency impedance on current spectrum

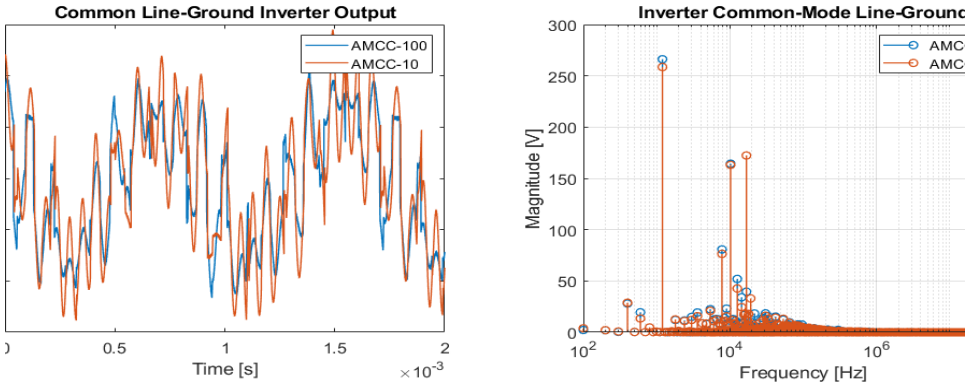

Figure 6-26. Effects of dc-link Inductor on Common Mode

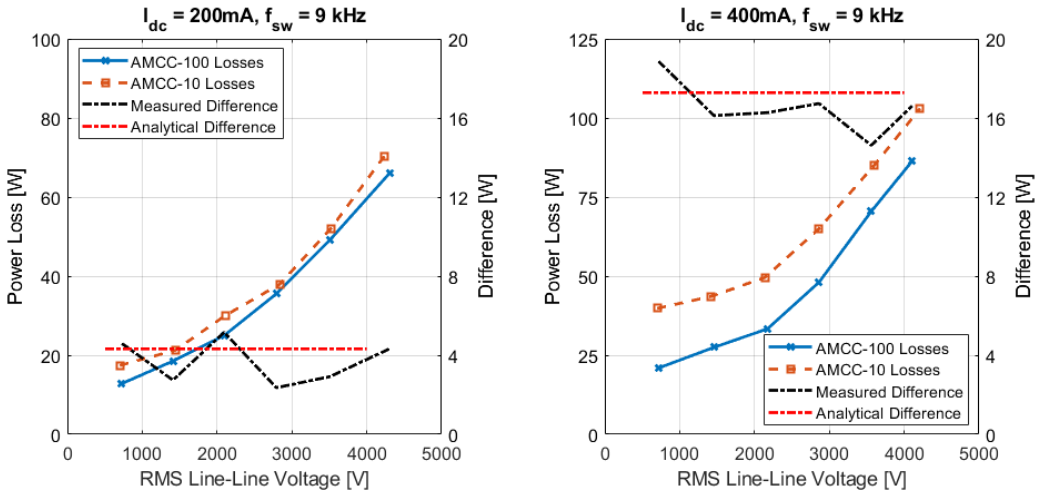

Figure 6-27. Measured difference in system power loss between AMCC-100 and AMCC-10 dc-link inductor designs

6.5 Chapter Summary

This chapter focused on extensive testing of the drive system consisting of the front-end, dc-link and inverter focusing on the dc-link control and power losses of the system. Example waveforms produced showing the sinusoidal medium voltage line-line waveforms and the PWM voltage input of the CSI is shown in Figure 6-28.

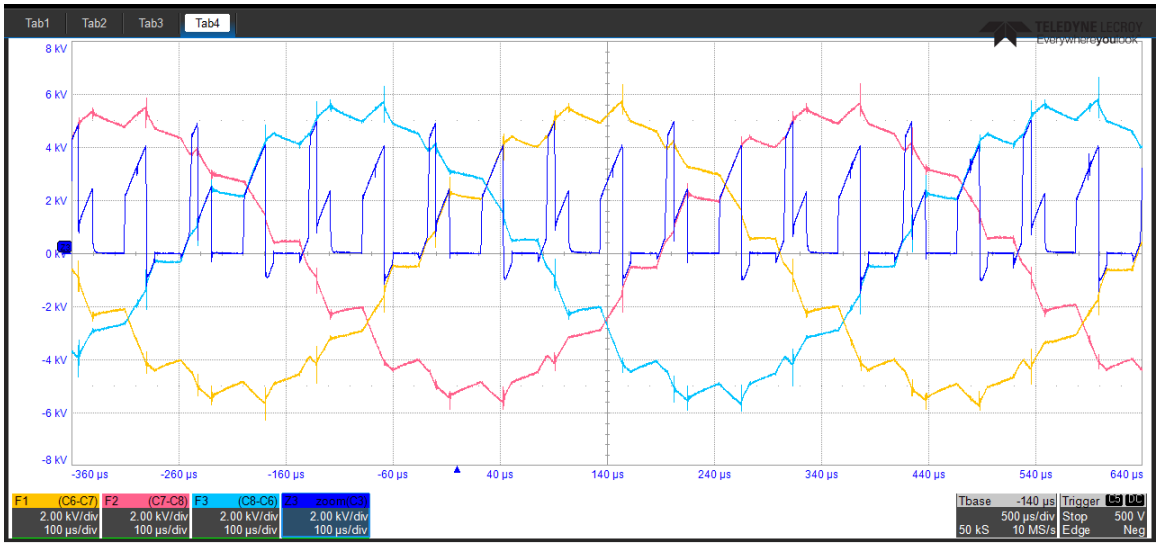

Figure 6-28. Measured waveforms of Line-Line voltage of CSI and dc-link output voltage

Chapter 4 derived an analytical model of the dc-link which showed the existence of a right-hand plane pole caused by the inner torque modulator of the motor, and two different dc-link controllers were proposed to stabilize the system. The control testing in *Chapter 6* confirmed the existence of the instability and the small-signal model of the system was verified. The controller with virtual resistance was shown to stabilize the system at steady state and provide increased dynamic stiffness of the dc-link. The limitations of the virtual resistance at providing enough dynamic stiffness to withstand increasing torque steps was confirmed. The alternative controller, which decouples the q-axis voltage disturbance on the dc-link, does not have the same limitation at increased loads. The predicted increase in dc-link current due to the decoupling terms' dependence on q-axis voltage command was

confirmed. However, the alternative controller was theorized to have reduced dynamic stiffness to unmodelled system components. The reduced dynamic stiffness of the dc-link lead to the discovery of a mechanical system disturbance, which resulted in increased dc-link current ripple due to the increase in reactive power flow in the system.

The extensive loss evaluation of *Chapter* 6 confirmed these expected loss relationships from the topology evaluation in *Chapter* 3 which predicted:

- switching loss to be the largest loss in the system,
- a significant dependence on dc-link current and output voltage
- the output power and fundamental frequency

The sensitivity analysis showed a linear dependency on switching frequency and dc-link current. However, the output voltage influencing the switching losses was shown to be the most significant component with a voltage-squared dependence. The relationship was determined to be associated with super-cascode parasitic capacitance and the minimization of inter and intra capacitances reduced the system losses significantly.

The loss breakdown attempted to parse the losses to subsystems and component by breaking down test components, using thermal imaging, and introducing dc-link capacitors to create another power measurement point. The losses of the super-cascodes were confirmed by two independent methods and do not completely dominate the system loss overall after multiple iterations of reducing their parasitic capacitance. A modified dc-link inductor was utilized with half the core material with the goal of reducing core-losses in the system and increase high-frequency dc-link impedance. However, the design increased the dc-resistance and in the end the overall losses increased by the amount expected to be

recouped. The modified design did improve the high frequency dc-link impedance, reducing the harmonic content of the dc-link current and line-ground common mode voltage of the inverter at high frequency. The lack of a reduction in power loss with the half core material (with similar flux ripple) supports the loss modeling of *Chapter 3*, where core losses were not a significant contribution. It is difficult to measure and compare proximity losses, especially without being able to directly measure the power loss of the dc-link inductor under normal operating conditions. It is recommended in the future works section in *Chapter 7,* that a detailed loss analysis of the dc-link and inverter be validated to determine the source of the remaining unattributed losses in the system.

Chapter 7: Conclusions, Contributions and Recommended Future Work

7.1 Conclusion

Review of the state of the art revealed that previous electrostatic machines targeted niche applications with drives that do not translate to general purpose variable frequency applications. The SEM is the first electrostatic machine to have competitive torque density with air cooled magnetic machines, therefore a modern power electronic drive platform for this machine had never been reported on. The machine optimization in previous work lead to a high impedance machine requiring a medium voltage drive at relatively low power levels. This characteristic of extremely high impedance is new to the variable frequency drive domain where torque is traditionally dependent on current, leading to comparably low impedance motors. With no variable frequency electrostatic drive foundation to build from, this dissertation set out to explore how a standard two-level inverter system would operate and what challenges it would encounter.

The first barrier to electrostatic drives is the lack of suitable medium voltage switches to implement a two-level drive. A switch capable of blocking the rated peak line-line voltage of the machine is required and is further complicated by the relatively high electrical frequency required for the drive (one of the primary handles to increase torque density of the machine was maximizing the pole count for a given gap). The high pole count causes the fundamental electrical frequency of the machine to reach 640 Hz at 400 RPM, a challenge for medium voltage power electronics. The high fundamental frequency increases the required switching frequency in the 10 kHz range, a decade beyond normal

medium voltage drive switching frequencies. The combined requirement of relatively high switching frequency and medium voltage essentially rules out traditional medium voltage silicon devices. Silicon devices, reviewed in *Chapter 1*, are suitable for line frequency operation or very low switching frequencies and are generally designed for much higher power and current, i.e. lower impedance, systems. Therefore, a series connection of devices designed to operate as a simple three terminal switch with a single gate driver was chosen. One such composite switch is a JFET super-cascode where normally-on devices are connected in series with a passive gate coupling network that enables the entire series-stack to be driven with a traditional gate driver. Super-cascodes have been utilized in the past but focused on applications with capacitive dc-links where a normally-of device was the controlled device in the series stack, resulting in a normally-off super-cascode. The super-cascode developed was utilized in a current source inverter and the normally-on characteristics on the JFET are maintained to create a normally-on super cascode.

Chapter 2 developed the normally-on super cascode with the target specifications of the devices focused on the required current and voltages of the SEM driven in this dissertation. It was shown that while the more advanced gate coupling networks provided an improvement in the balance of losses in the device, the trade-off was really balancing turn-on losses vs. turn-off losses. The increased capacitance in the gate network provided stronger effective gate drivers for the series connected devices reducing the turn-on and losses. However, the increased capacitance resulted in an increased turn-off duration and switching loss since the capacitance had to be recharged and the energy is not recovered. Previous work developing super-cascodes targeted higher currents (10A and above) such

that the turn-off time and loss was not dominated by the gate-network capacitance but rather by the switch dynamics making this tradeoff more valuable.

The standard two-level current-source and voltage-source inverters were compared for their suitability as electrostatic drives in Chapter 3. The CSI at a fundamental level, is the ideal topology for driving electrostatic machines. Its output directly modulates the ampere-seconds, i.e. charge, into the electrostatic machine providing a direct handle on the charge level. The CSI simplifies torque modulation and is the direct dual of a voltage source inverter controlling the flux of an electromagnetic machine. However, the dc-link inductor required for a CSI introduces the conduction losses and core losses that the SEM eliminates. To compensate for this, a variable dc-link would have to be used to minimize the conduction loss.

Conversely, a VSI driving the SEM was shown to be the dual of a CSI driving an electromagnetic machine. The capacitive terminal characteristics of the SEM requires the implementation of an inductive output filter that introduces higher order dynamics. Modern systems utilizing CSIs with electromagnetic machines can overcome this limitation by utilizing high switching frequencies approaching 100 kHz, creating a high enough separation between the required output filter and switching frequency. However, due to the comparably reduced switching performance of the super-cascode this is not feasible (even at ~20 kHz switching) and the VSI limits the maximum speed of the SEM. One of the main benefits of the VSI based system is that the losses are speed dependent, resulting in improved performance at low speed compared to the CSI, where losses were found to be torque dependent. Ultimately, the CSI was chosen due to its reduced output dynamics and

better performance as a general variable frequency drive. However, for reduced speed position and hold applications the VSI merits consideration.

The theoretical development of a CSI system including a front-end and dc-link current control was the focus of *Chapter 4*. An average model for the system was developed and combined with the CVVR torque modulator developed in previous work. The system operates in a cascaded power topology where the dc-link current controller is a slower outer loop and the voltage (torque modulator) is the faster inner loop. This resulted in the CSI and torque modulator behaving as a constant power load with a negative incremental resistance for the dc-link current. The constant power load nature of the cascaded power system was shown to cause a pole to migrate to the right-hand-plane if the losses in the system were lower than the CSI output power. Two controllers were proposed to stabilize the system.

The first controller proposed used a virtual resistance to overcome the negative resistance of the constant power load, resulting in an open-loop stable enhanced system plant. The stable enhanced plant was then controlled with a simple low bandwidth PI controller regulating the dc-link current. The virtual resistance also provides increased dynamic stiffness facilitating increased load steps. However, to support rated torque steps increasingly large values of virtual resistance would be necessary. The drawback of increasing the virtual resistance is a reduction dc-link command response since the time-constant of the system in further increased. A second controller targeting the system instability by directly decoupling the voltage disturbance of the CSI was proposed. The controller utilizes a decoupling term computed from the commanded q-axis voltage and the q-axis modulation signal. The direct decoupling of the q-axis voltage command enables

this controller to withstand larger torque steps than the controller with virtual resistance. However, the improved command response of the second controller comes with the tradeoff of reduced effective dc-link impedance, thus reducing disturbance rejection to the unmodelled system components.

The hardware implementation of the CSI and front-end was documented in *Chapter 5*. The parasitic capacitance of the system subcomponents was identified as the key parameter that needed to be managed. In the case of the inverter, any additional capacitance added (in the 100 pF range) results in increased displacement currents caused by the high dv/dt in the medium voltage drive, causing increased switching loss. The implementation of the dc-link inductor showed that a high inductance and low energy storage dc-link is readily implemented, creating an inductor with a high self-resonance frequency is challenging. Even a few pico-farads of capacitance can reduce the self-resonance frequency to the range affected by the PWM harmonic content. This challenging aspect of SEM drives has the potential to be reduced as machines increase in power, increasing the required dc-link current which will in turn reduce the value of inductance needed. There would be more stored energy and the challenges of the dc-link regarding losses would still be significant, but the resonance issue could decrease.

The machine has significant capacitance to ground affecting the common mode impedance of the system and two key components in the drive system were identified to increase the common mode impedance. The dc-link inductor inherently provides high impedance as the frequency increases, but its parasitic capacitance ultimately dominates the system common mode impedance at high frequency. At low frequency, the front-end

isolation transformer can provide increased low frequency impedance if its isolation capacitance is minimized.

Finally, the proposed controls of *Chapter 4* were combined with the hardware of *Chapter 5* and system level testing was presented in *Chapter 6*. The dc-link instability was confirmed, and the proposed solution of virtual resistance successfully stabilized the dc-link current control. Additionally, the virtual resistance was shown to provide increased dynamic stiffness to the dc-link current controller, allowing for increase torque dynamics of the CVVR. The alternative controller utilizing the q-axis voltage decoupling was also shown to stabilize the system. However, the use of the q-axis command voltage instead of measured, resulted in the controller preemptively increasing the power into the dc-link, leading to a dc-link current spike during torque transients. The reduced effective dc-link impedance allows for faster dc-link current command changes but inherently has lower disturbance rejection to unmodelled system components.

Chapter 6 also included a characterization and sensitivity analysis of the losses in the power electronic drive system. A sensitivity analysis where the key system parameters of dc-link current, output power, fundamental frequency, switching frequency, and output voltage were independently varied to understand the nature of their effects on the system losses. The key outcomes were the confirmation of modeling in *Chapter 3*, which predicted:

- the independence of losses from output power and fundamental frequency
- A linear dependence of loses on switching frequency and dc-link current

However, the effects of output voltage on the losses were underestimated in *Chapter 3*. The sensitivity analysis revealed the system losses to be dominated by the operating voltage with a squared dependence on it. Modifications were implemented to reduce the parasitic capacitance of the super-cascodes by removing common heatsinks. This resulted in significant (13%) reduction in losses that were shown to be co-dependent on the switching frequency. A loss breakdown showed that with the heatsinks removed, the super-cascodes were no longer the dominating loss in the system. The losses of the super-cascodes were verified with two distinct methods, increasing the confidence in the losses attributed to the super-cascodes.

Ultimately, a complete traditional two-level inverter with an active front-end SEM drive operating from a low voltage source was implemented. The design and characterization of the system subcomponents was documented and detailed. The system model was combined with the established machine torque modulator and a suitable control method for the dc-link current developed. This drive is the first documented general purpose variable frequency drive and has been utilized by Ghule where he investigated the control and self-sensing of the machine in [14], [50], [96].

The following subsection considered the implications of increased machine torque and power on the power electronic drives. The contributions of this dissertation are detailed in the section 7.2 followed by recommended future work to expand and improve power electronics for synchronous electrostatic machines.

7.1.1 Impacts of machine scaling on power electronics

The main challenge encountered throughout the hardware development has been the significant influence of small amounts of parasitic capacitance on the performance of a high impedance drive. Parasitic capacitance on the order of magnitude of 10 to 100 pF in heatsinks and semiconductor devices resulted in increased switching loss. Even smaller values in the range of 5 to 10 pF reduced the self-resonance frequency and effective impedance of the dc-link. Fortunately, these issues should be reduced as the torque and power of SEM increase. The next stage of SEM development is focusing on increasing torque and power by increasing the stator and rotor electrode surface area, i.e., increasing mutual capacitance. The stator voltage will not increase proportionally if the gap size and electric field are maintained therefore resulting in a decrease of machine terminal impedance. The reduction of machine terminal impedance has the potential to ease the drive power electronic design. Assuming an increase in output power comes from a significant increase in torque with no significant change to the operating speed range, two scenarios are considered:

1) a single order of magnitude increase in output power
2) multiple orders of magnitude increase in output power.

The drive for a single order increment in power from the 1 kW to the 10 kW range could potentially be implemented with the same techniques developed in this dissertation. The increased power would require an increase in dc-link current which reduces the dc-link inductor self-resonant challenge. While the increase in power will inherently increase the overall physical size of the dc-link inductor due to increased energy storage requirement, it will inherently be handled by the increase in dc-link current per equation (7-1). The

increase in dc-link current enables a reduction of the value of inductance and therefore turn number on the magnetic core. Lowering the turn count of the inductor could enable a reduction of the parasitic capacitance of the inductor. Reducing either the dc-link inductance value or the parasitic capacitance would cause an increase of the self-resonant frequency per equation (7-2).

$$E = \frac{1}{2} L_{dc} I_{dc}^2 \tag{7-1}$$

$$\mathrm{f}_{\mathrm{resonant}} = \frac{1}{2\pi\sqrt{L_{dc} C_{dc}}} \tag{7-2}$$

The reduction of the self-resonant frequency problem eases the dc-link design, potentially lowering conduction losses and enabling higher frequency operation of the front-end converter. The higher frequency operation of the front-end would allow for potentially controlling the dc-link current as the inner current loop in the system, easing the control problems of *Chapter 4*.

The reduction in machine impedance and inherent increase in dc-link current would also affect the losses of the super-cascodes. The super-cascodes utilized 80 mΩ devices which are rated for significantly higher currents (~10 to 20 A) with proper cooling. A simplified switching loss model can be expressed by (7-3). *Chapter 6* showed that for the present system the voltage squared term had a significant impact on the system losses. An increase in dc-link current to levels more in line with the device ratings, would cause the switching losses to be governed more by the traditional voltage and current term in (7-3). A reassessment of the super-cascode gate network and an increase in cooling performance (while limiting parasitic capacitance) would be necessary to implement a higher power drive with the super-cascodes.

$$\mathrm{E_{sw}} = \frac{1}{2} t_{sw} V I + \frac{1}{2} C\, V^2 \tag{7-3}$$

If the machines were to scale to the 100 kW to 1 MW range and above without a significant increase in stator voltage (e.g. remained in 10 to 30 kV range), then the state of the art of drives for medium voltage electromagnetic machines should be thoroughly reviewed. Without a revolutionary change in dielectric liquid or design paradigm the pole count of SEMs will likely continue to be relatively high. The increase in current and power would likely make high switching frequency two-level converters quite challenging to implement. However, there has been significant advancements in multilevel converters both in research and industrial applications [97]–[99] which could potentially map over to high power SEM drives.

7.2 Contributions

1. Implementation of first normally-on super cascode for use in medium voltage high impedance CSI systems suitable for switching frequencies up to 18 kHz
    - Review of previous developed super-cascode balancing methods and applied them to medium voltage and high impedance SEM application
    - Experimentally determined the preferred balancing method for the super-cascode in the SEM application
2. Identified VSI topology for use in low speed, and position and hold SEM drives with the following outcomes:
    - Losses are dependent on speed and not only torque output
    - Output filter must provide significant attenuation of PWM harmonics or core losses of filter design increase significantly eliminating the benefits of the VSI
    - Maximum speed is limited by the resonance between output filter and machine requiring higher ratio of switching frequency to fundamental frequency
    - Variable dc-link improves losses but limits torque dynamics, since dc-link voltage limits maximum torque
3. Identified CSI topology for use in general purpose SEM drives via simulation analysis with the following conclusions:
    - Losses dependent on dc-link current and output torque, not power and speed
    - Variable dc-link is necessary for lowering losses over the full operating range of the SEM, but would limit torque and speed dynamics

- Switching loss of the super-cascode the most significant loss component
- Core losses of the dc-link inductor are minimized due to the low flux ripple in the inductor.

4. Designed and modelled CSI system with front-end operating from a low-power low-voltage source
    - Designed front-end converter with isolation transformer providing voltage gain and increased common mode impedance
    - Complete system model used for identification of dc-link instability when operated with an outer dc-link control loop
    - Identification of self-resonance issue in dc-link inductor, and proposed and evaluated design methods for minimizing dc-link capacitance
5. Proposed, analyzed, and implemented dc-link controller utilizing virtual damping resistance to compensate for effective negative incremental resistance
    - Specified design criteria for minimum dc-link resistance needed (virtual or actual) to guarantee small signal stability
    - Validated the effectiveness of virtual resistance to stabilize system and provide increased dynamic stiffness
    - Demonstrated the limitations of the virtual resistance when subjected to faster torque transients
    - Identified the dc-link current command tracking limitations of controller with virtual damping resistance

6. Implemented dc-link controller with q-axis voltage decoupling as an alternative stabilizing method
    - Overcomes the high load step limitations of virtual resistance method
    - Identified limitation of q-axis voltage command usage in the controller
    - Demonstrated the limitations of the controller at rejecting unmodelled system disturbances on the dc-link.
7. Performed detailed loss analysis of implemented system confirming the relationships predicted by the simulation analysis
    - Confirmation of the modeling outcomes of Chapter 3 regarding system power loss dependencies on dc-link current, switching frequency, output power, and output frequency
    - Identification of system losses on a voltage squared dependence attributed to switching loss interacting with system parasitic capacitance
    - Experimentally verified the effects of intra super-cascode capacitance and inter super-cascode capacitance have on the switching losses
    - Documented the effects of dc-link parasitic capacitance on high frequency content created by high dv/dt of super-cascode

7.3 Recommended Future Work

The future work section is split into the three categories, echoing the work and chapters documented in this dissertation. Namely, medium voltage switches for SEMs, topology evaluation for future machines, and continued implementation improvements and development of present system.

When the super-cascode was developed in this work, a near term view focusing on the needs of the present machine and potential fluid upgrades (~2-3x increase in torque) was taken. Because of this the focus of the clamped inductive load was from 0.5 to 2 amps. Future larger machines will require higher current and the super-cascode should be evaluated across higher currents and voltages.

- Thermal considerations focusing on the use of ceramic or other nonconductive, low parasitic capacitance thermal solutions will be necessary at higher powers.
- Robustness of overvoltage withstand capability of super-cascode in case of accidental open circuit condition

The SiC JFET has not had the commercial success of SiC MOSFETs and therefore there is a limited number of suppliers and the long-term existence of these switches is not guaranteed. Monolithic medium voltage SiC devices are experiencing active development and when they become available their use in this application should be examined. Alternatively, a series connection of switches where normally-off 1200V SiC MOSFET are series connected with a single gate driver which has been reported in [100]. However, it lacks several key features of the JFET super-cascode. Recommended future work regarding this area includes:

- Understanding of the necessary protections for normally-off devices in a CSI
- Investigate the use of normally-off series connected devices with a single gate driver

The system developed in this work provided an excellent platform for evaluation of the SEM, but numerous power electronic challenges, both hardware and control, were encountered. The recommended future work focused on improving the dc-link control in this dissertation is:

- Explore the utilization of measured q-axis voltages instead of commanded voltage to reduce the dc-link current overshoot. However, the impacts of filters and system noise must be considered
- Investigate the possibility of combining the increased disturbance rejection of the virtual resistance with the q-axis decoupling term
- Study the challenges of implementing torque control via modulation of dc-link current where the inverter only modifies applied vector angle
- Investigate the challenges in implementing a high-speed dc-link controller

On the hardware side of the system, there is significant room for improvements of the dc-link and front-end regarding their parasitics. The front-end transformer was designed with a desire for high magnetizing inductance and low isolation capacitance resulting in significant leakage inductance.

- Optimization of dc-link inductor design, focusing on dc resistance and isolation capacitance

- Implementation of a bidirectional power flow front end enabling generating operation
- Reduction of front-end leakage inductance allowing for higher frequency operation of front-end
- Innovative non-contact voltage and current sensing techniques for high noise high impedance systems

The electrostatic machine utilized in this work was the first prototype of the three-phase separately excited variety, and was developed in [2] and by C-motive Technologies. The machine is a great demonstrator and to find a more competitive advantage over traditional electromagnetic machines, future prototypes will provide orders of magnitude higher torque for low speed direct drive systems [101]. This increase in torque and output power results in a need to re-evaluate some of the key work developed in this dissertation. Potential research opportunities to compliment this increased power level of the machine include:

- Understand the system level EMI/EMC implications that will become more important as the machine technology matures
- Expand the topology review to multilevel topologies where benefits of reduced switch voltage and dv/dt could outweigh the control complexities
- Consider using super-cascode in multi-level converters to minimize number of levels necessary
- Investigate power generation applications of electrostatic machines and their effects on power systems

Conversely, the present machine was shown to have comparable performance in position and hold drives vs electromagnetic machines [1]. However, the CSI system developed here has inherent losses due to conduction losses in the dc-link. One proposed method [13] utilizes small single-phase bidirectional dc-dc converters to create a differential drive that reduces the power conversion stage from two to one. One significant challenge would be the control of such a system, combining the non-linear nature inherent in large signal modulation of dc-dc converters with the SEM.

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Appendix A: System Model Derivation

The system control development documented in *Chapter 4* used an average model for stability analysis of the dc-link current controller. The system, shown in Figure A-1, is modelled using average modelling techniques. The front-end is duty cycle control and a simple model by inspection of the average dc-link input voltage is defined in (A-1), where m_{fe} is the front-end modulation depth.

$$v_g = m_{fe} N v_{in} \tag{A-1}$$

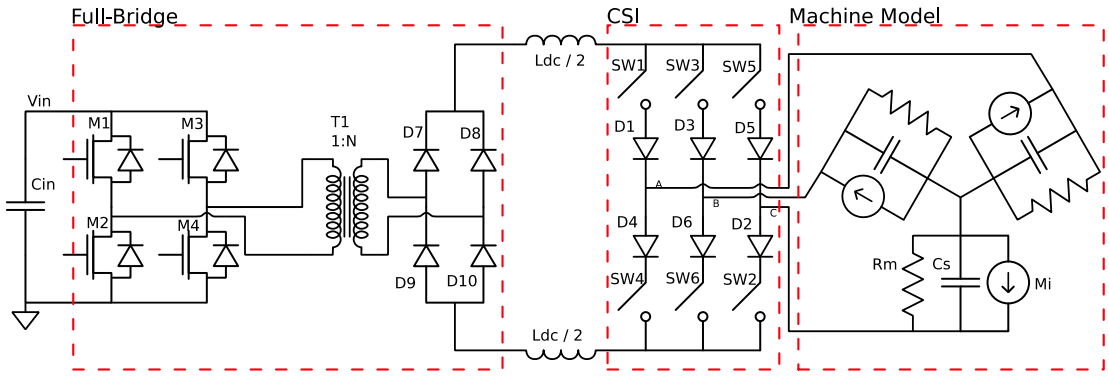

Figure A-1. Current source drive with isolated full-bridge front end

Defining switching functions for each switch sw_x where x is the number for the switch and utilizing the constraint for a CSI of:

$$sw_1 + sw_3 + sw_5 = 1 \tag{A-2}$$

$$sw_2 + sw_4 + sw_6 = 1 \tag{A-3}$$

The phase currents are defined as

$$i_{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} sw_1 - sw_4 \\ sw_3 - sw_6 \\ sw_4 - sw_2 \end{bmatrix} * i_{dc} \tag{A-4}$$

Assuming switching frequency much higher than fundamental and applying averaging

$$m_{abc} = \begin{bmatrix} m_a \\ m_b \\ m_c \end{bmatrix} = \begin{bmatrix} sw_1 - sw_4 \\ sw_3 - sw_6 \\ sw_4 - sw_2 \end{bmatrix} \tag{A-5}$$

$$i_{abc} = m_{abc} * \ i_{dc} \tag{A-6}$$

dc-link current equation from KVL

$$L_{dc}\frac{di_{dc}}{dt} = -i_{dc}R_{dc} - m_{abc}^{T}v_{abc} + v_g \tag{A-7}$$

with matrix dimensions [1x1] = [1x1] – [1x3][3x1] + [1x1]

Defining the three capacitor voltages

$$v_{abc} = \begin{bmatrix} v_{aN} \\ v_{bN} \\ V_{cN} \end{bmatrix} \tag{A-8}$$

The mmf current with no phase angle.

$$i_{mmf} = \begin{bmatrix} \omega_e C_m V_f \cos(\omega t) \\ \omega_e C_m V_f \cos(\omega t - \frac{2\pi}{3}) \\ \omega_e C_m V_f \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \tag{A-9}$$

dc-link current equations based on KCL at each phase node. Capacitor currents and resistor currents defined from phase node to neutral:

$$C_S\frac{dV_{abc}}{dt} + \frac{v_{abc}}{R_s} = i_{abc} + i_{mmf} \tag{A-10}$$

$$C_s\frac{dV_{abc}}{dt} = i_{abc} - \frac{v_{abc}}{R_s} + i_{mmf} \tag{A-11}$$

$$C_s\frac{dV_{abc}}{dt} = m_{abc}i_{dc} - \frac{v_{abc}}{R_s} + i_{mmf} \tag{A-12}$$

With matrix dimensions [3x1] = [3x1][1x1] – [3x1] + [3x1]

Applying magnitude invariant dq0 transform with q axis on real axis, d on negative imaginary axis and

$$x_{qd0} = \frac{2}{3} T x_{abc} \tag{A-13}$$

$$T = \begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ \sin(\omega t) & \sin\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{matrix} \leftarrow q\ axis \\ \leftarrow d\ axis \\ \leftarrow zero\ component \end{matrix} \tag{A-14}$$

Using $\left(\frac{2}{3} T^T\ T\right) = I_{3x3}$ and inserting between m_{abc} and v_{abc} in current equation

$$L_{dc} \frac{di_{dc}}{dt} = -i_{dc} R_{dc} - m_{abc}^T \left(\frac{2}{3} T^T\ T\right) v_{abc}\ + v_g \tag{A-15}$$

$$L_{dc} \frac{di_{dc}}{dt} = -i_{dc} R_{dc} - \left(\frac{2}{3} T m_{abc}\right)^T \frac{3}{2} \left(\frac{2}{3}\ T v_{abc}\right)\ + v_g \tag{A-16}$$

$$L_{dc} \frac{di_{dc}}{dt} = -i_{dc} R_{dc} - \frac{3}{2} m_{qd0}^T v_{qd0}\ + v_g \tag{A-17}$$

Chain rule and derivative of transformation matrix necessary for voltage equations

$$\frac{d}{dt}(T v_{abc}) = T \frac{d}{dt} v_{abc} + \frac{d}{dt} T * v_{abc} \tag{A-18}$$

$$\frac{d}{dt} T = \omega_e \begin{bmatrix} -\sin(\omega_e t) & -\sin\left(\omega_e t - \frac{2\pi}{3}\right) & -\sin\left(\omega_e t + \frac{2\pi}{3}\right) \\ \cos(\omega_e\ t) & \cos\left(\omega_e t - \frac{2\pi}{3}\right) & \cos\left(\omega_e t + \frac{2\pi}{3}\right) \\ 0 & 0 & 0 \end{bmatrix} \begin{matrix} \leftarrow q\ axis \\ \leftarrow d\ axis \\ \leftarrow zero\ component \end{matrix} \tag{A-19}$$

Looking at the transform matrix and its derivative shows that row 1 and 2 are swapped. And is the speed dependent d and q axis cross coupling terms. Going back to capacitor equation (A-12) and multiplying both sides by 2/3T

$$C_s \frac{2}{3} T\ \frac{dV_{abc}}{dt} = \frac{2}{3} T m_{abc} i_{dc} - \frac{2}{3} T v_{abc} \frac{1}{R_s} + \frac{2}{3} T i_{mmf} \tag{A-20}$$

$$C_s \frac{d}{dt}\left(\frac{2}{3} T v_{abc}\right) - C_s \frac{2}{3} \frac{d}{dt} T * v_{abc} = m_{qd0} i_{dc} - \frac{v_{qd0}}{R_s} + i_{mmf-qdo} \tag{A-21}$$

$$C_s \frac{d}{dt} v_{qd0} = m_{qd0} i_{dc} - \frac{v_{qd0}}{R_s} + i_{mmf-qdo} + C_s \frac{2}{3} \frac{d}{dt} T * v_{abc} \tag{A-22}$$

The mmf in qd0 coordinates

$$I_{mmf-qd0} = \begin{bmatrix} \omega_e C_m v_f \\ 0 \\ 0 \end{bmatrix} \tag{A-23}$$

Assuming balanced excitation, zero axis dropped and left with the following

$$C_s \frac{d}{dt} \begin{bmatrix} v_q \\ v_d \end{bmatrix} = \begin{bmatrix} m_q \\ m_d \end{bmatrix} i_{dc} - \frac{1}{R_s} \begin{bmatrix} v_q \\ v_d \end{bmatrix} + \omega C_s \begin{bmatrix} -v_d \\ v_q \end{bmatrix} + \begin{bmatrix} \omega_e C_m V_f \\ 0 \end{bmatrix} \tag{A-24}$$

Defining the three non-linear equations:

$$\frac{di_{dc}}{dt} = -\frac{i_{dc} R_{dc}}{L_{dc}} - \frac{3}{2L_{dc}} m_q v_q - \frac{3}{2L_{dc}} m_d v_d + \frac{v_g}{L_{dc}} \tag{A-25}$$

$$\frac{dv_q}{dt} = \frac{m_q i_{dc}}{C_s} - \frac{v_q}{R_s C_s} - \omega v_d + \frac{\omega_e C_m v_f}{C_s} \tag{A-26}$$

$$\frac{dv_d}{dt} = \frac{m_d i_{dc}}{C_s} - \frac{v_d}{R_s C_s} + \omega_e v_q \tag{A-27}$$

The equivalent circuit of Figure A-1 is defined by equations (A-25) through (A-27) and shown in Figure A-2.

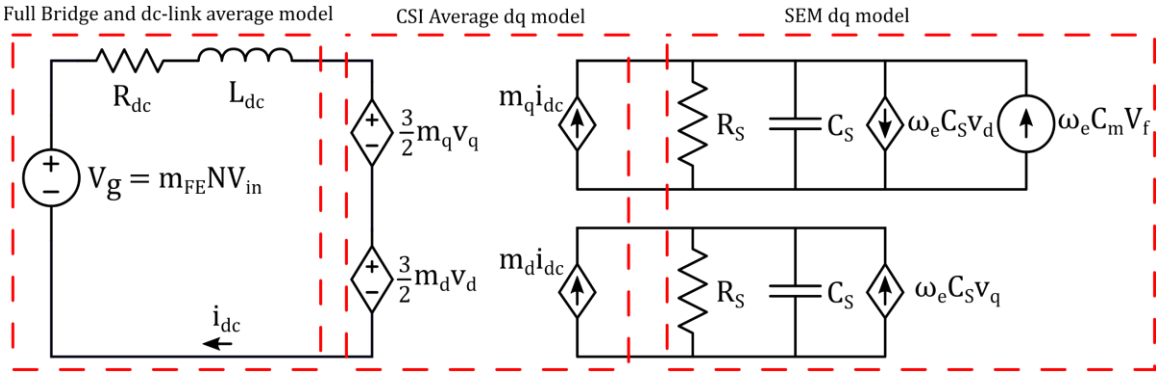

Figure A-2. Physical System Averaged Model

Appendix B: Schematics

B.1 Medium Voltage Gate Driver

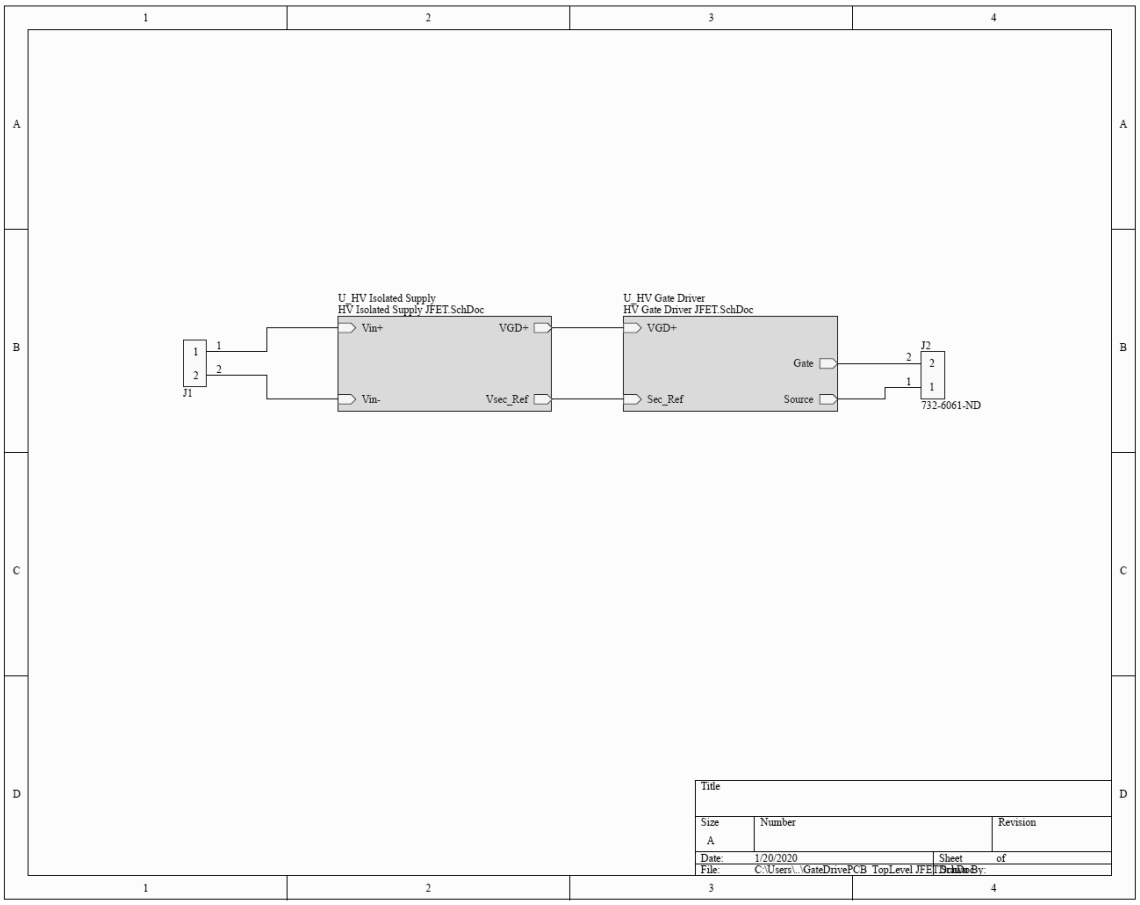

Figure B-1. Top Level Schematic of High Voltage Gate Driver

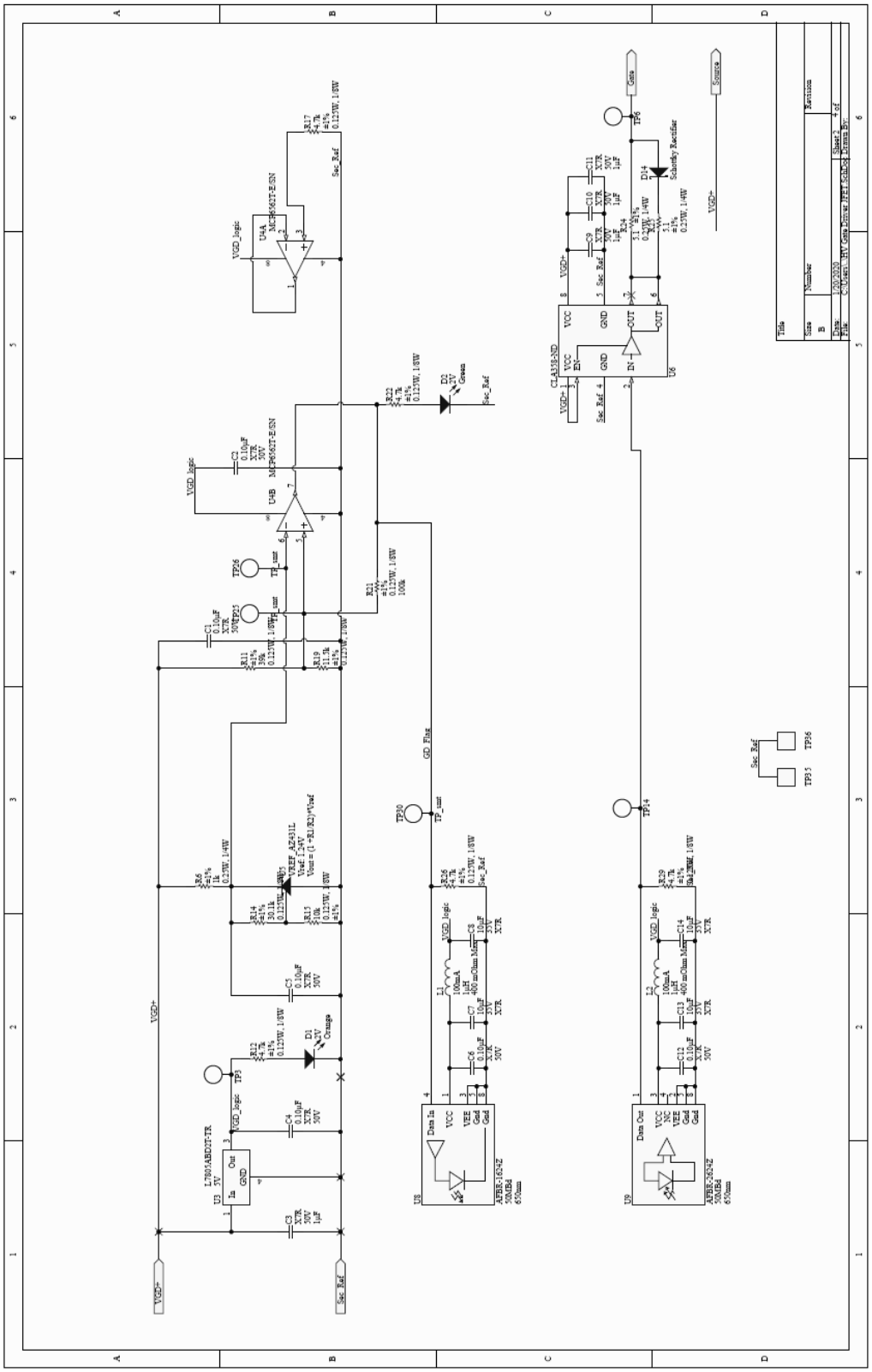

Figure B-2. Gate Driver Output Stage Schematic

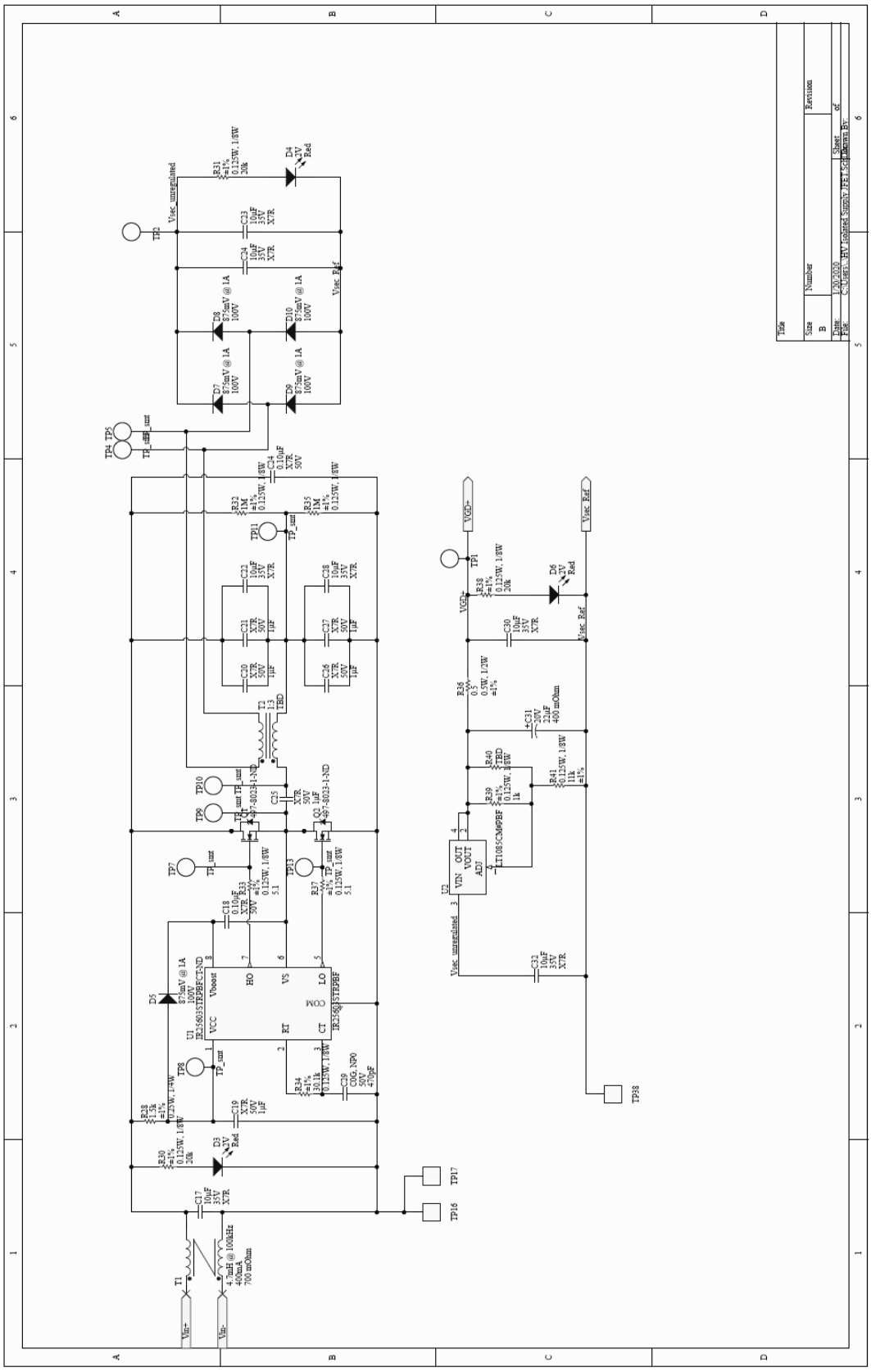

Figure B-3. Schematic of Gate Driver Isolated Power Supply

B.2 DSP Breakout board

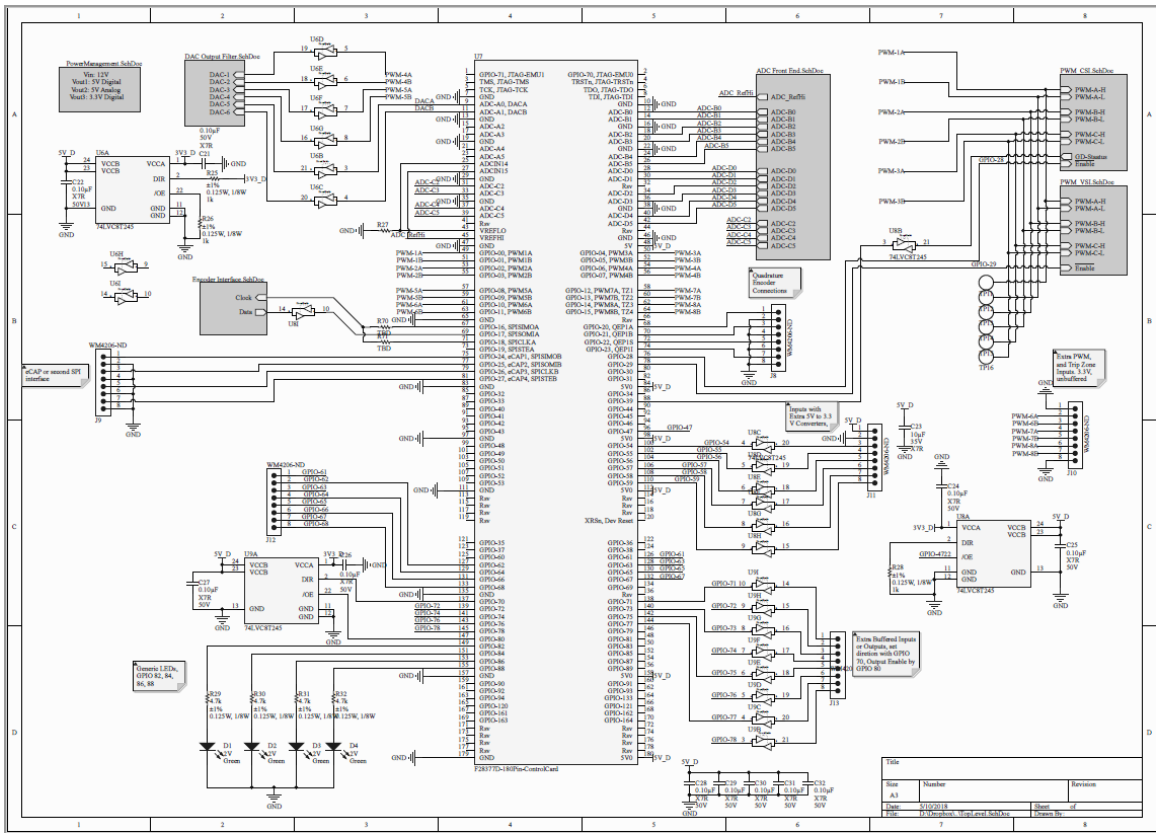

Figure B-4. Top Level Schematic of DSP breakout board

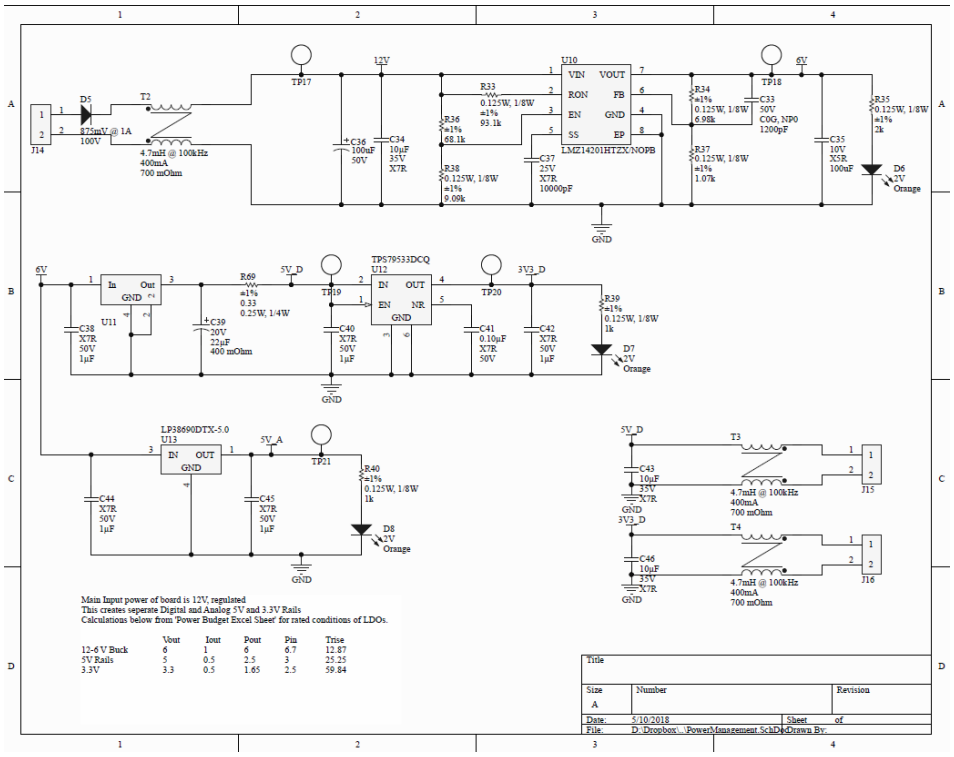

Figure B-5. Schematic of DSP Breakout Board Auxiliary Power

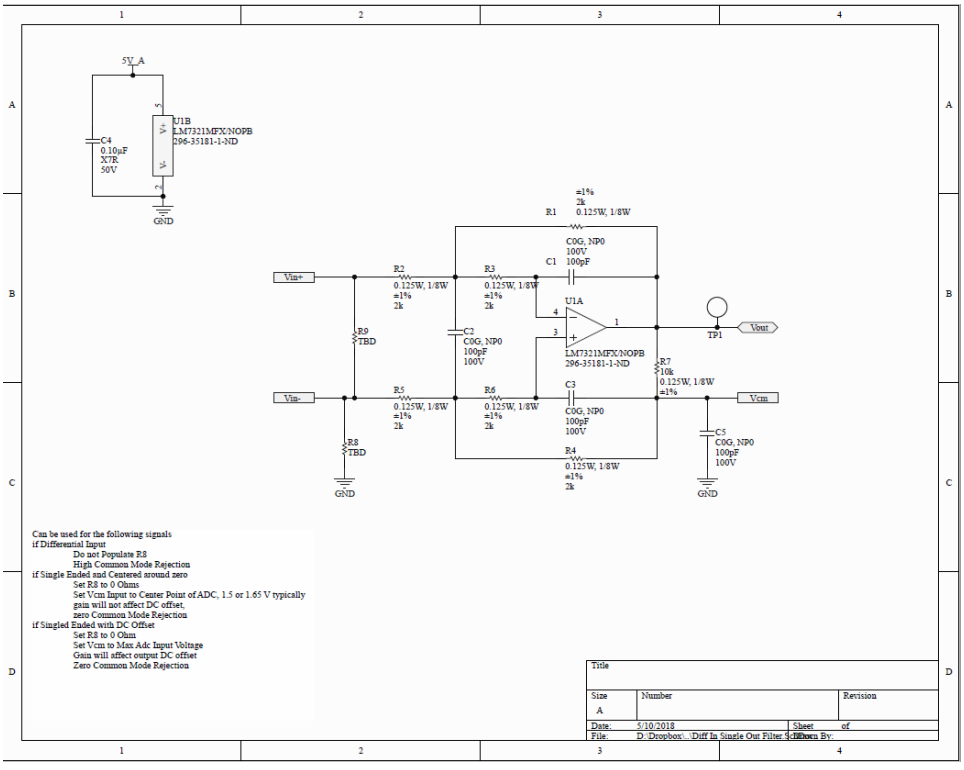

Figure B-6. ADC Differential to Single Ended Interface Schematic

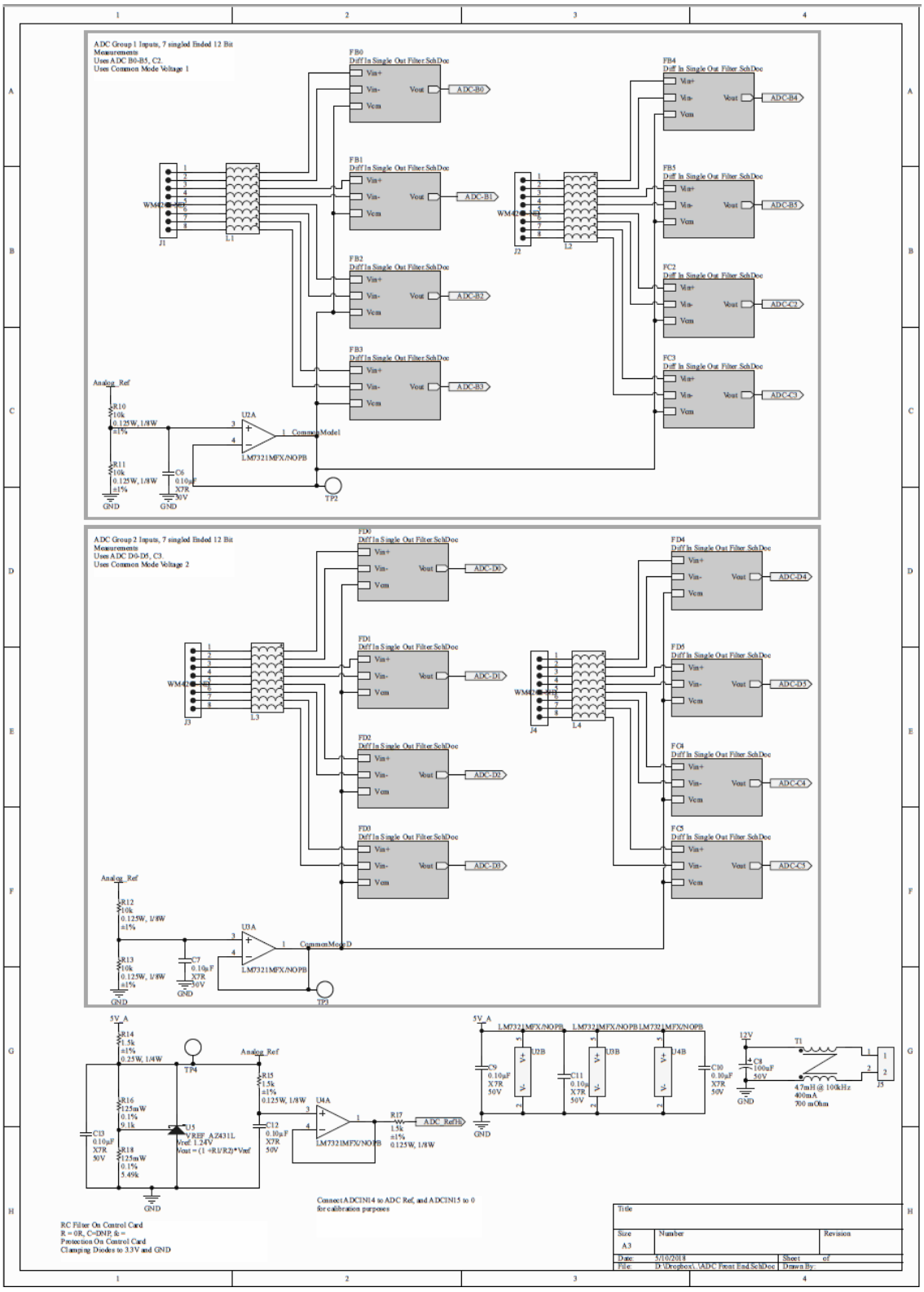

Figure B-7. ADC Interface Schematic

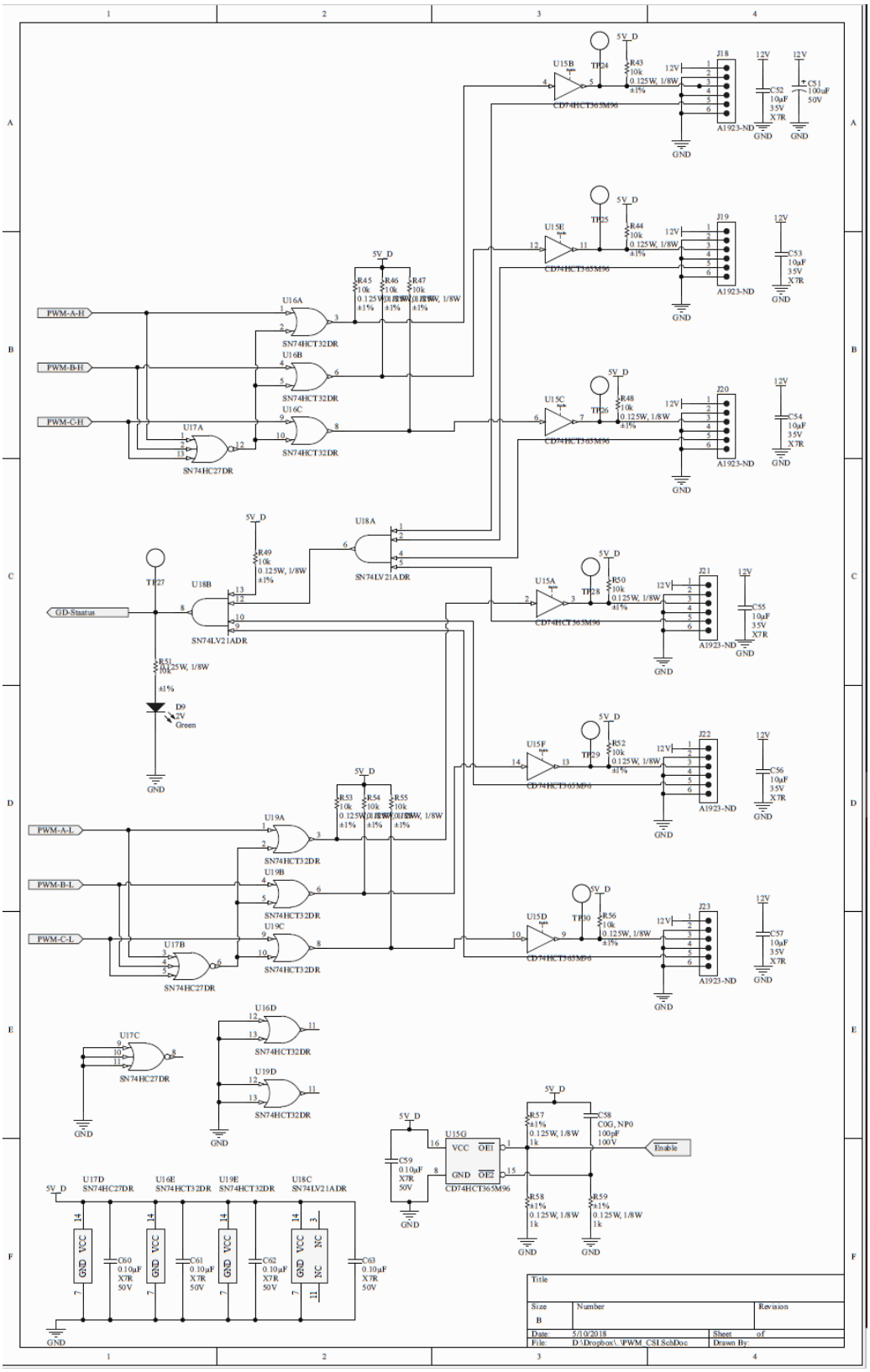

Figure B-8. Schematic of PWM buffers with CSI hardware overlap protection

B.3 Voltage and Current Sensing

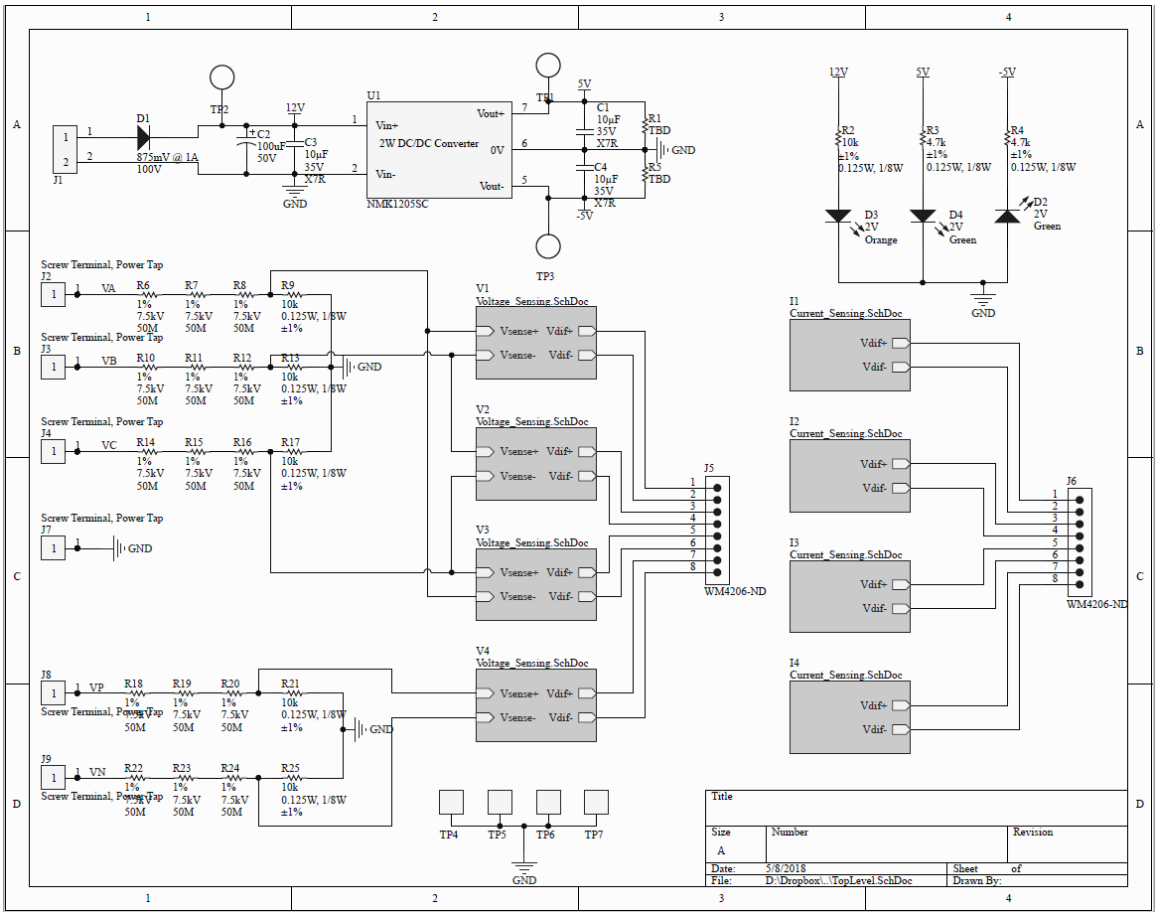

Figure B-9. Voltage and Current Sensing Top Level Schematic

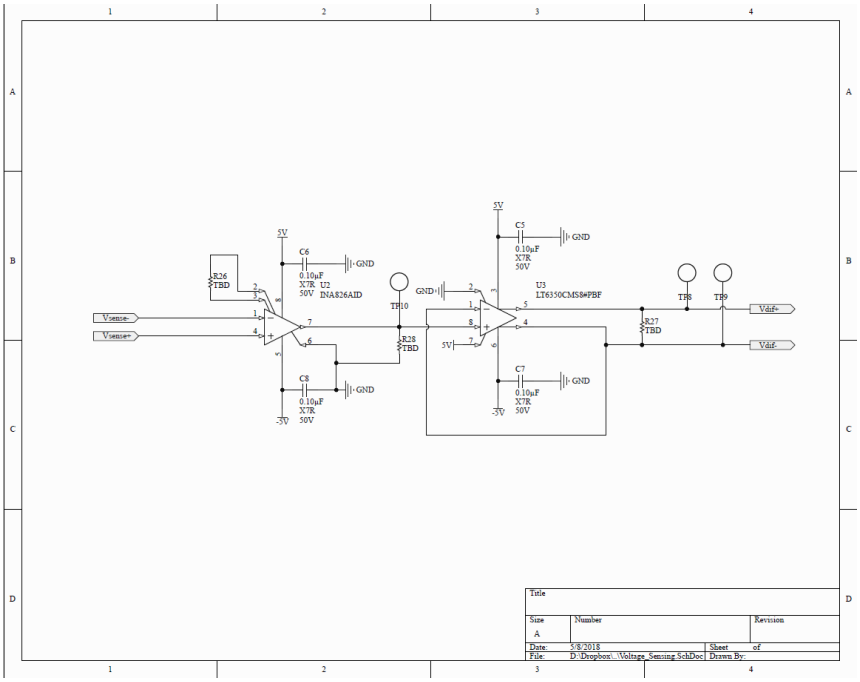

Figure B-10. Voltage Sensing Schematic

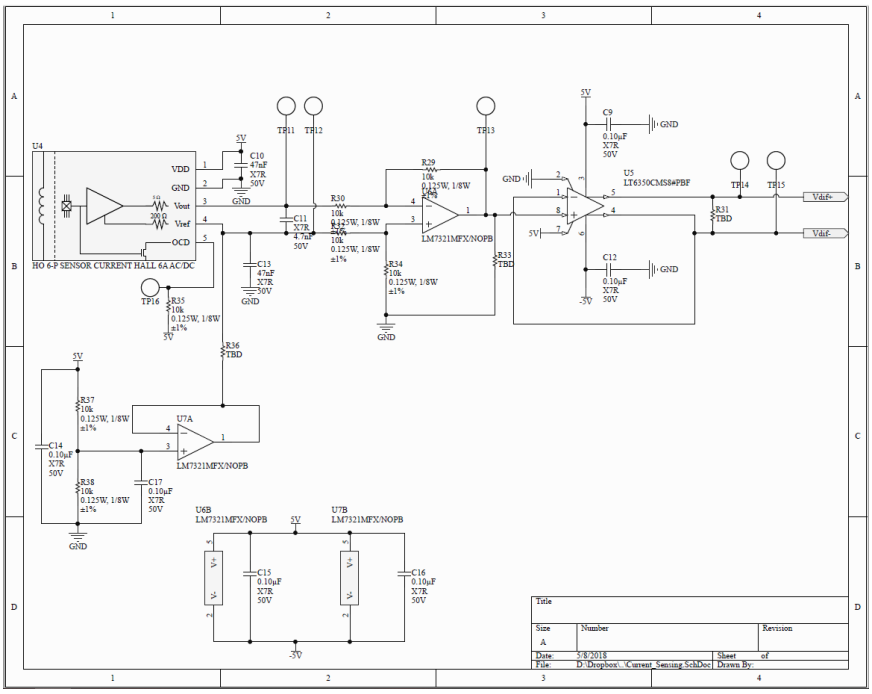

Figure B-11. Current Sensing Schematic

Appendix C: Curve Fit Equations

$$P_{Loss} = p_1 x + p_2$$

Table C-1 System losses of linear curve fit parameters presented in *Chapter 6*

Parameter Varied	Vll [RMS]	p1 Value	p1 Units	p2 [W]	R2
Fe	2.1	0.01254	W/Hz	42.78	0.979065
Fe	2.8	0.025586	W/Hz	58.629	0.945812
Fe	3.5	0.022646	W/Hz	89.8435	0.749131
Fe	4.2	0.012344	W/Hz	126.342	0.780791
Fe	4.9	0.02432	W/Hz	168.881	0.898927
Idc	2.1	0.035093	W/mA	31.7027	0.890254
Idc	2.8	0.05698	W/mA	45.24659	0.952494
Idc	3.5	0.079419	W/mA	63.8735	0.98241
Idc	4.2	0.097794	W/mA	91.01287	0.984167
Idc	4.9	0.213872	W/mA	92.66931	0.999194
Fsw	2.1	0.734333	W/kHz	34.604	0.949017
Fsw	2.8	1.417267	W/kHz	40.5319	0.93803
Fsw	3.5	2.311767	W/kHz	55.7929	0.951698
Fsw	4.2	3.157067	W/kHz	74.7636	0.961605
Fsw	4.9	4.6261	W/kHz	96.8239	0.986315
Po	2.1	0.042765	W/W	45.11852	0.705372
Po	2.8	0.061615	W/W	62.51423	0.849018
Po	3.5	0.04883	W/W	91.35235	0.774597
Po	4.2	0.028132	W/W	129.3802	0.565022
Po	4.9	-0.00285	W/W	174.7738	0.011665

$$P_{Loss} = p_1 x^2 + p_2$$

Table C-2. System losses vs voltage curve fit parameters presented in *Chapter 6*

Idc [mA]	Fsw [kHz]	Heat Sink	p1 [W/V²]	p2 [W]	R2
400	18	Yes	6.39E-06	17.56277	0.996631
400	9	Yes	4.88E-06	17.98724	0.997689
400	18	No	5.47E-06	19.01181	0.996643
400	9	No	4.58E-06	15.96553	0.989104
200	18	Yes	5.17E-06	14.24132	0.998934
200	9	Yes	3.83E-06	12.75016	0.998365
200	18	No	4.34E-06	13.75945	0.997227
200	9	No	3.45E-06	11.87389	0.996557

Appendix D: PLECS Simulation Model

Table D-1. System parameters utilized in *Chapter 4* simulations

$\boldsymbol{R_S}$	$\boldsymbol{1.6\ M\Omega}$
$\boldsymbol{C_S}$	$13\ nF$
$\boldsymbol{C_m}$	$2.2\ nF$
$\boldsymbol{R_{dc}}$	$40\ \Omega$
$\boldsymbol{L_{dc}}$	$3.4\ H$
$\boldsymbol{N}$	$7.4\ V/V$
$\boldsymbol{V_{in}}$	$280\ V$
$\boldsymbol{K_P}$	20
$\boldsymbol{K_I}$	100
$\boldsymbol{f_{BW}}$	$150\ Hz$
$\boldsymbol{K_{VP}}$	$2\pi f_{BW} C_S$
$\boldsymbol{K_{VI}}$	$\frac{K_{VP}}{R_S C_S}$

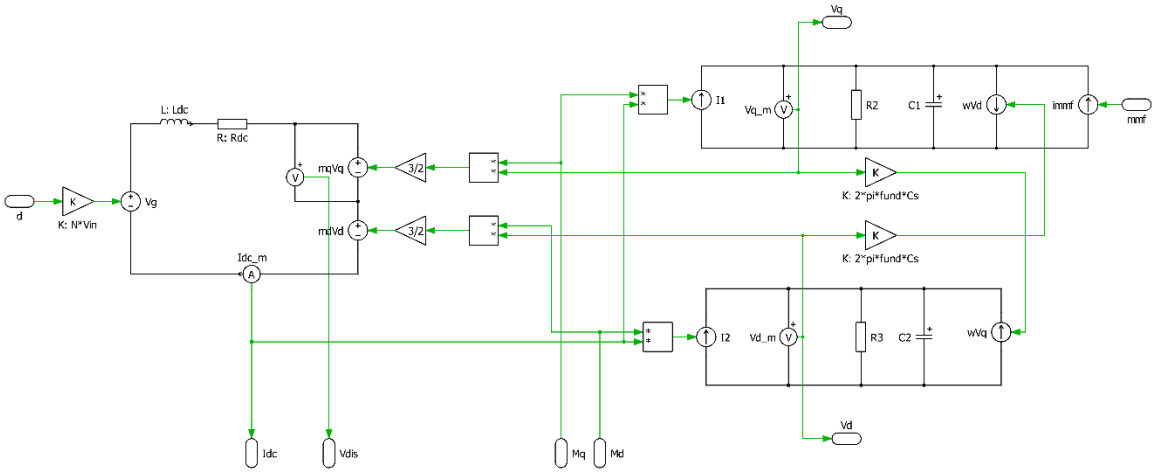

Figure D-1. PLECS Model of Front-end, CSI, and SEM utilized in *Chapter 4* simulation study

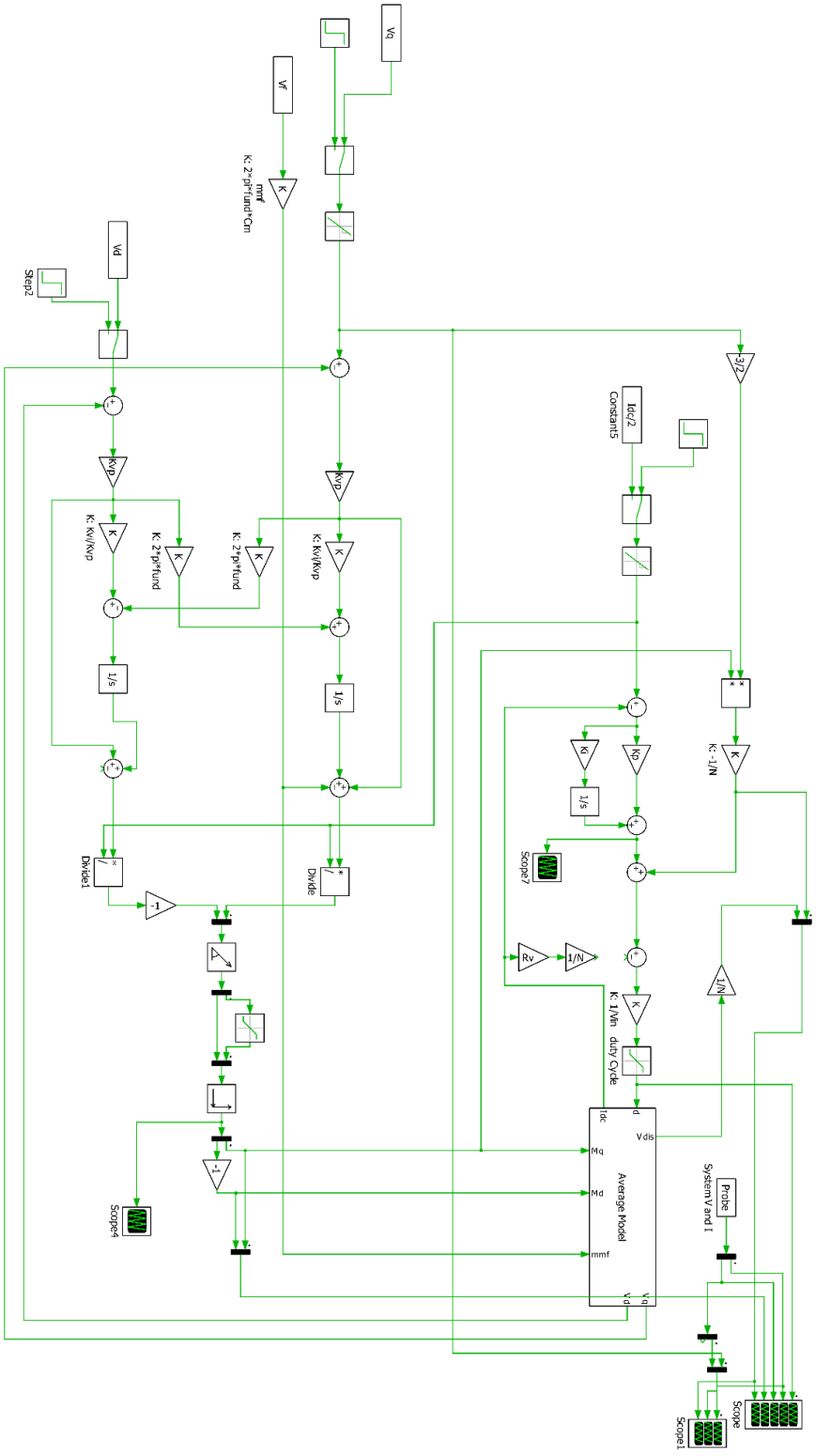

Figure D-2.. PLECS Model of control loops used in *Chapter 4* simulation study