Cryogenic measurement of gate-defined quantum dots in Si/SiGe heterostructures for quantum computation

by

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Abstract

This thesis describes work towards building a quantum computer out of gate-defined quantum dots in Si/SiGe heterostructures and primarily addresses two of the DiVencenzo criteria: scalability and measurement.

Chapters one and two provide an introduction to quantum computation and top-gated semiconductor quantum dots, with notes about the fabrication of quantum dots, modeling quantum dots with a simple capacitor model, the theory of Coulomb blockade thermometry, the theory of bias spectroscopy in quantum dots, and methods for spin-to-charge conversion in quantum dots.

Chapter three presents data from characterization of the first quantum dot in a Si/SiGe nanomembrane, a new material that may have applications for the scalability of Si/SiGe quantum dots. Previous to the work presented in chapter three, all gate-defined quantum dots in Si/SiGe heterostructures were formed on top of strain-graded virtual substrates; yet the strain grading process necessarily introduces misfit dislocations into a heterostructure, which have the potential to impact qubit performance and/or reduce uniformity between qubits. The use of a SiGe nanomembrane as the virtual substrate enables the strain relaxation to be entirely elastic, eliminating the need for misfit dislocations.

Chapter four provides a practical guide to cryogenic amplification, which has been used to improve charge-sensing measurements inside a dilution refrigerator. The chapter first provides a brief outline of different cryogenic amplification techniques that have been or could be employed to improve charge sensing, and then focuses on the implementation of a

two-stage capacitively-coupled cryogenic HEMT amplifier. Using this amplifier, we report a charge sensitivity of 230 μeV/$\sqrt{\text{Hz}}$.

Chapter five presents a study in how to improve heat sinking of a cryogenic amplifier in a dilution refrigerator so as to mitigate its detrimental impact on a nearby quantum dot. While the power consumption of a cryogenic amplifier can cause a significant increase in the electron temperature of a nearby quantum dot, we present evidence that these detrimental effects can be mitigated through an enhanced heat sinking technique, where the cryogenic amplifier is heat sunk to a printed circuit board (PCB) separate from the PCB of the sample.

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It goes without saying that the members of the Eriksson group contributed greatly to the success of this thesis. Postdocs were an essential source of knowledge in an arcane field, so I'd like to thank Jon Prance, Dohun Kim, Dan Ward, Luke Smith, and Evan MacQuarrie. I also need to thank past and present graduate students affiliated with the Eriksson group: Ryan Foote, Brandur Thorgrimsson, Adam Frees, Cameron King, Sam Neyens, Tom McJunkin, J.P. Dodson, Nathan Holman, Joelle Baer, Gabrielle Jaffe, Xian Wu, and Robert Mohr. Your assistance and camraderie over the years made this thesis possible!

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Chapter 1

Introduction to quantum computing

Quantum computers have the potential to speed up particular computational tasks relative to classical computation; this computational speedup comes from the quantum computer's use of quantum bits (qubits) rather than classical bits. Whereas a classical bit is always either in a 0 or 1 state, a quantum bit can be in a superposition of the quantum computational basis states $|0\rangle$ or $|1\rangle$. The quantum state of a single, arbitrary qubit can be expressed as

$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle\,,$$

where $\alpha, \beta \in \mathbb{C}$ such that $\alpha^2 + \beta^2 = 1$. The "global phase" $e^{i\mathrm{Arg}(\alpha)} = e^{i\gamma}$ of $|\psi\rangle$ is unmeasureable and can be factored out, giving

$$\begin{aligned} |\psi\rangle &= e^{i\mathrm{Arg}(\alpha)}\left(|\alpha|\,|0\rangle + |\beta|e^{i(\mathrm{Arg}(\beta)-\mathrm{Arg}(\alpha))}\,|1\rangle\right) \\ &= e^{i\gamma}\left(\cos(\theta/2)\,|0\rangle + \sin(\theta/2)e^{i\phi}\,|1\rangle\right), \end{aligned}$$

where $\phi = \mathrm{Arg}(\beta) - \mathrm{Arg}(\alpha) \bmod 2\pi$, and $\theta = 2\arccos(|\alpha|)$. Ignoring the global phase, two parameters alone define the quantum state $|\psi\rangle$: θ, which is a real number between 0 and π; and ϕ, which is a real number between 0 and 2π. The range of these variables suggests that $|\psi\rangle$ can arbitrarily be represented on the surface of a sphere, called the Bloch sphere. As

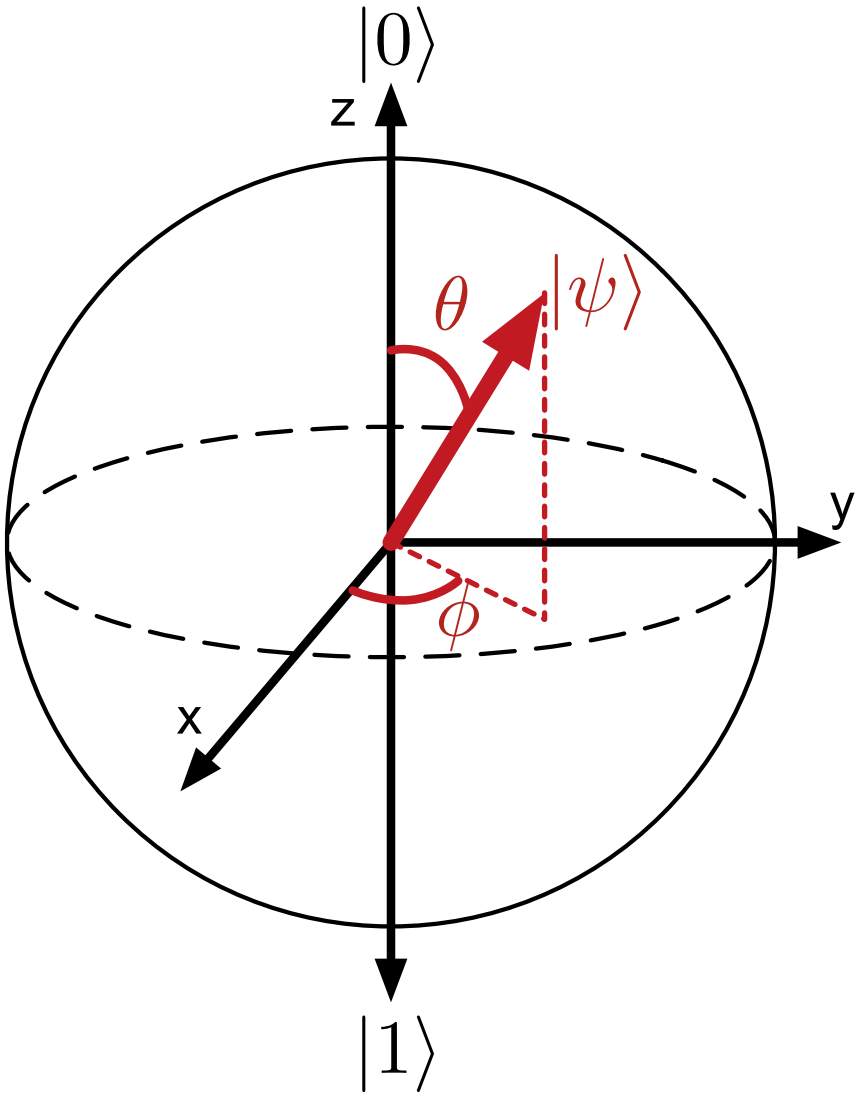

Figure 1.1: Depiction of the Bloch sphere. The top and bottom of the Bloch sphere are the basis states $|0\rangle$ and $|1\rangle$ respectively, with everywhere else on the sphere representing a superposition of these basis states. A two-level quantum state $|\psi\rangle$ can arbitrarily be represented on the sphere, with the polar angle corresponding to the probability of getting $|0\rangle$ upon measurement of $|\psi\rangle$ and the azimuthal angle ϕ corresponding to the relative phase of the basis states in $|\psi\rangle$.

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depicted in Figure 1.1, the top and the bottom of the Bloch sphere are the states $|0\rangle$ and $|1\rangle$ respectively, with everywhere else on the sphere representing a superposition of these basis states. Measurements of $|\psi\rangle$ in the $\{|0\rangle, |1\rangle\}$ basis result in $|0\rangle$ with probability $|\alpha|^2$ and $|1\rangle$ with probability $|\beta|^2$. Due to wavefunction collapse, the wave function state becomes

either $|0\rangle$ or $|1\rangle$ after measurement, depending on what was measured. While there are only 2^N possible outcomes for full measurement of an N-qubit quantum computer's state in the $\{|0\rangle, |1\rangle\}$ basis, just the same as for an N-bit classical computer, the state of the quantum computer before measurement has many more degrees of freedom. These additional degrees of freedom in the unmeasured quantum state allow for "quantum parallelism," which results in speedup for particular computational tasks. Speaking loosely, quantum computers provide speedup for "needle-in-a-haystack" types of problems [1], i.e. scenarios where the correct solution is lost in a vast set of potential solutions yet can be easily verified as being the correct solution when found. Perhaps most famously, Shor's algorithm uses the quantum Fourier transform to provide super-polynomial speedup over the best known classical algorithms for factoring prime numbers [2]. Alternatively, Grover's quantum search algorithm provides polynomial speedup over some of the best known classical search algorithms [3]. Outside of search algorithms, quantum computation may be useful as an efficient way to simulate the evolution of quantum systems [4].

While the potential of quantum computation is immense, there's a big caveat: nobody has yet produced a large scale quantum computer. One of the things currently holding quantum computers back is that any physical realization of a two-level quantum system will be subject to environmental noise that can alter its state, resulting in computational errors. While some quantum systems are more strongly coupled to their environment than others, no qubit can be completely isolated from its environment due to the need for external manipulation. For a single two-level qubit, the most common types of errors are type I and type II errors: type I errors result from a relaxation process between the excited and ground computational state, whereas type II errors result from decoherence of the relative phase between computational states. The fidelity $\mathcal{F}$ of gate operations (loosely defined as the likelihood that a particular operation will succeed) is an important parameter for comparing different qubit implementations. However, having an excellent fidelity alone is not enough to make a useful quantum computer; as has been shown in reference [5], quantum computers

may not provide an actual speedup in time if the time to perform a gate operation is too long. Thus it is important to compare both fidelity and gate speeds between different methods for implementing a quantum computer. Other factors are important as well for building a scalable quantum computer: David DiVencenzo outlined five criteria necessary for building a full quantum computer, which I summarize as follows [6]:

1. **Scalability**: a scalable physical system with well-characterized qubits
2. **Initialization**: all qubits can be consistently initialized in a particular quantum state
3. **Memory**: decoherence times that are long enough to perform the desired quantum algorithm, and much longer than individual gate operation times
4. **Manipulation and Fidelity**: the ability to perform a universal set of gate operations on the state of the quantum computer with high fidelity
5. **Measurement**: the ability to measure individual qubits with little measurement error

1.1 Outline of thesis

This thesis describes work towards building a quantum computer out of gate-defined quantum dots in Si/SiGe heterostructures and primarily addresses two of the DiVencenzo criteria: scalability and measurement.

Chapter two provides a brief overview of quantum dots, with notes about the fabrication of quantum dots, modeling quantum dots with a simple capacitor model, the theory of Coulomb blockade thermometry, the theory of bias spectroscopy in quantum dots, and methods for spin-to-charge conversion in quantum dots.

Chapter three presents data from characterization of the first quantum dot in a Si/SiGe nanomembrane, a new material which may have applications for the scalability of Si/SiGe quantum dots. Previous to the work presented in chapter three, all gate-defined quantum dots in Si/SiGe heterostructures were formed on top of strain-graded virtual substrates; yet

the strain grading process necessarily introduces misfit dislocations into a heterostructure, which have the potential to impact qubit performance and/or reduce uniformity between qubits. The use of a SiGe nanomembrane as the virtual substrate enables the strain relaxation to be entirely elastic, eliminating the need for misfit dislocations.

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Chapter five presents a study in how to improve heat sinking of a cryogenic amplifier in a dilution refrigerator so as to mitigate its detrimental impact on a nearby quantum dot. While the power consumption of a cryogenic amplifier can cause a significant increase in the electron temperature of a nearby quantum dot, we present evidence that these detrimental effects can be mitigated through an enhanced heat sinking technique, where the cryogenic amplifier is heat sunk to a printed circuit board (PCB) separate from the PCB of the sample. Whereas previous work has shown electron temperatures in excess of 200 mK with $\sim$10 μW power dissipation in a nearby amplifier, the enhanced heat sinking technique allows an electron temperature of $\sim$150 mK with 10 μW power dissipation.

Chapter 2

Top gated quantum dots for quantum computation

2.1 Theory of quantum dots

Spin-based qubits may be suitable for building a scalable quantum computer: the basic idea is that a particle's spin is a natural quantum system that can have long decoherence times due to the relative weakness of magnetic forces [7,8]. Fast measurement and manipulation of the spin state can be achieved by coupling the spin to electric forces [9,10]. Yet in order for a particle's spin to have long decoherence and relaxation times, the particle must be trapped and isolated from environmental noise. One method for trapping a particle is to confine it inside of a solid state device [9,11]. Semiconductor band engineering allows one-dimensional confinement of conduction-band electrons, resulting in a two-dimensional electron gas (2DEG): this has been achieved in both Si/SiGe heterostructures and GaAs/AlGaAs heterostructures [12,13]. Once electrons have been confined into a 2DEG, they can be further confined using electrostatic gates, resulting in a 0-dimensional quantum dot. If the electron's coherence length is long enough in this material, the quantum dot will have discrete energy levels. When there are many electrons in a quantum dot, the energy associated with their mutual

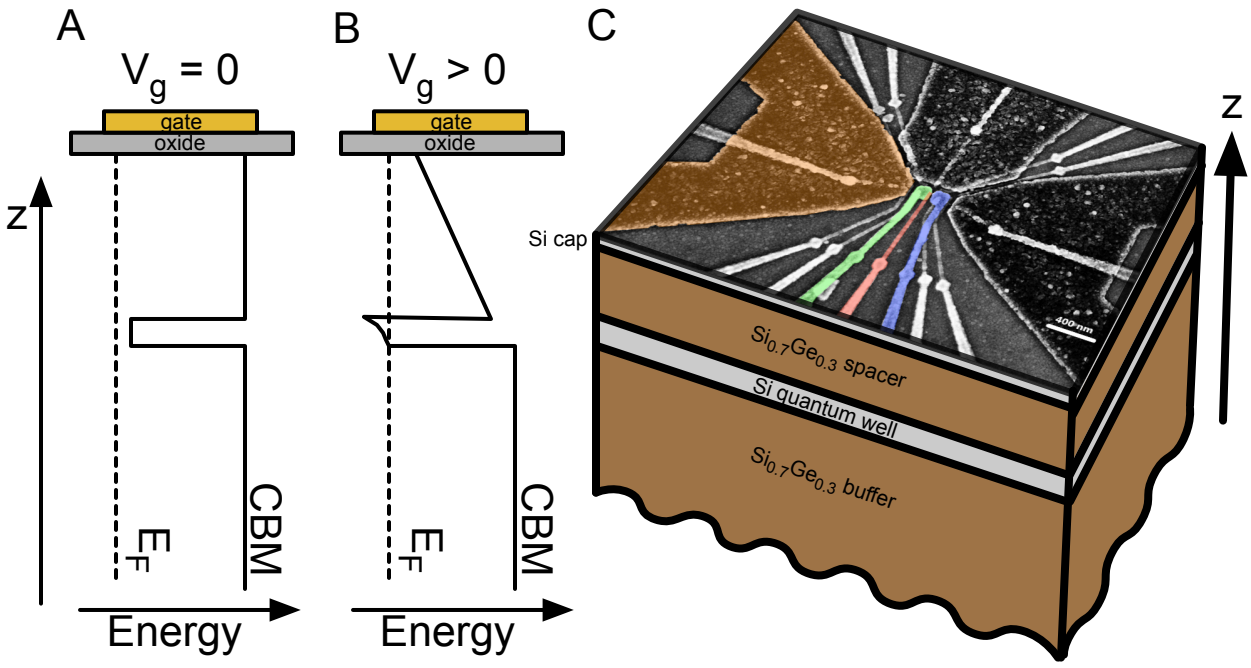

Figure 2.1: Panels A and B depict band diagrams for a Si/SiGe heterostructure without dopants. In panel A, the conduction band minimum (CBM) never falls below the Fermi level E_F because no voltage is applied to the accumulation gate. In panel B, a postive voltage is applied to the electrostatic gate and the conduction band minimum falls below the Fermi level in the strained Si quantum well, where a two-dimensional electron gas forms. Panel C shows a cross-sectional schematic diagram of a heterostructure, with an SEM image of a quantum dot gate pattern on top.

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electrical repulsion dominates the total energy of the quantum dot; yet when there are fewer electrons in a quantum dot, other effects like spin and orbital energy may become relevant and the quantum dot can be thought of as an "artificial atom" [14].

Multiple quantum dots can be created next to each other, which can be coupled capacitively or by allowing electrons to coherently tunnel between quantum dots. An electon's spin state can be coupled to its spatial state in several ways [9, 10], allowing the spin state to be addressed via the electric force; the same electrostatic gates that confine the electron can then be used to manipulate its spin state.

In terms of material, quantum dot qubits have been demonstrated in both Si and GaAs devices. Using Si as a host material may prove advantageous because Si has an abundant spin-0 isotope (^{28}Si), which offers a path towards incredibly long spin lifetimes [8]. Addition-

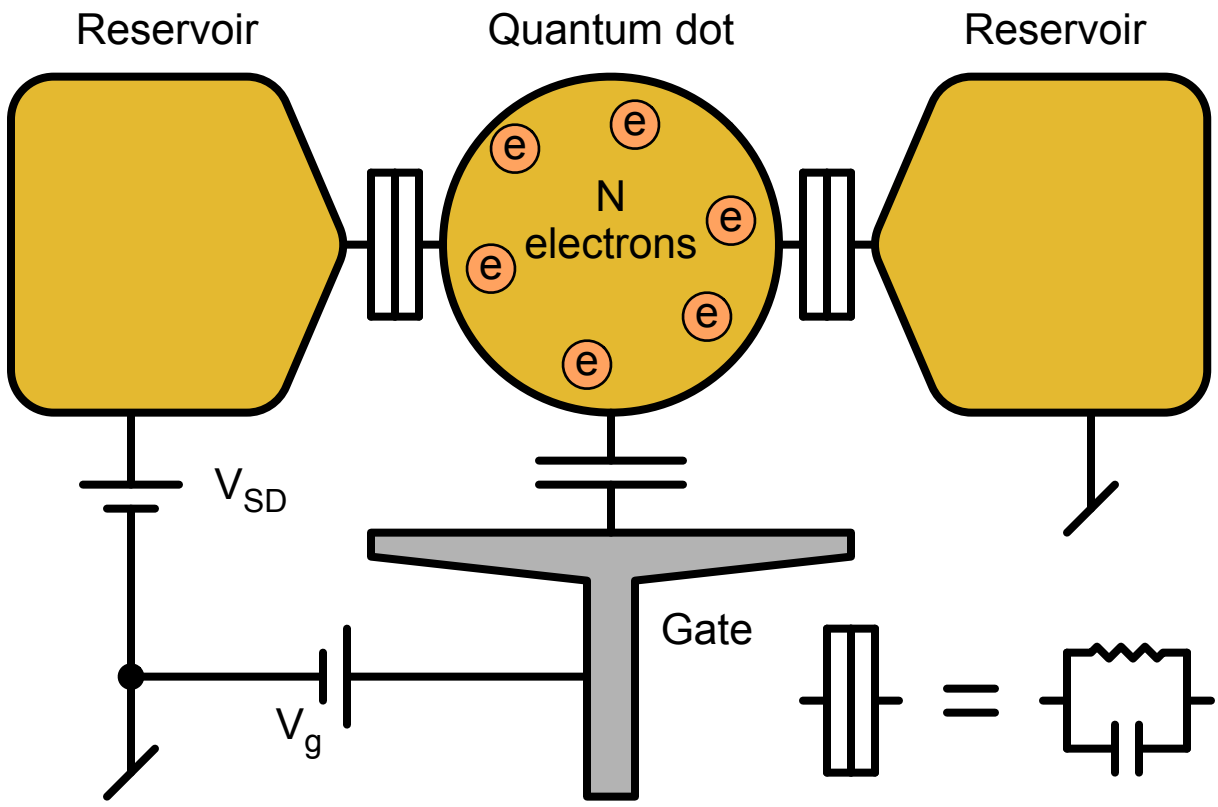

Figure 2.2: Schematic depiction of capacitive model of quantum dots.

ally, the semiconductor industry has already developed many techniques for processing Si devices, which may be useful for scaling up a quantum computer hosted in Si. Historically, quantum dot qubits were demonstrated in GaAs/AlGaAs heterostructures before Si/SiGe heterostructures [15, 16]; this may be because Si has some distinct disadvantages relative to GaAs when considered as a material for quantum dots. Electrons in Si have a larger effective mass than they do in GaAs, which has two results: first, electron mobility tends to be smaller in Si than in GaAs systems; second, given the same potential barrier, electrons in Si will have a smaller tunnel rate than in GaAs systems. Both of these detrimental effects can be mitigated in Si by fabricating quantum dots on a smaller length scale than in GaAs. One further disadvantage that Si has relative to GaAs systems is that Si and Ge are not lattice matched, which means that Si/SiGe heterostructures need to employ strain management techniques that are not required for GaAs/AlGaAs heterostructures [17, 18]. Despite

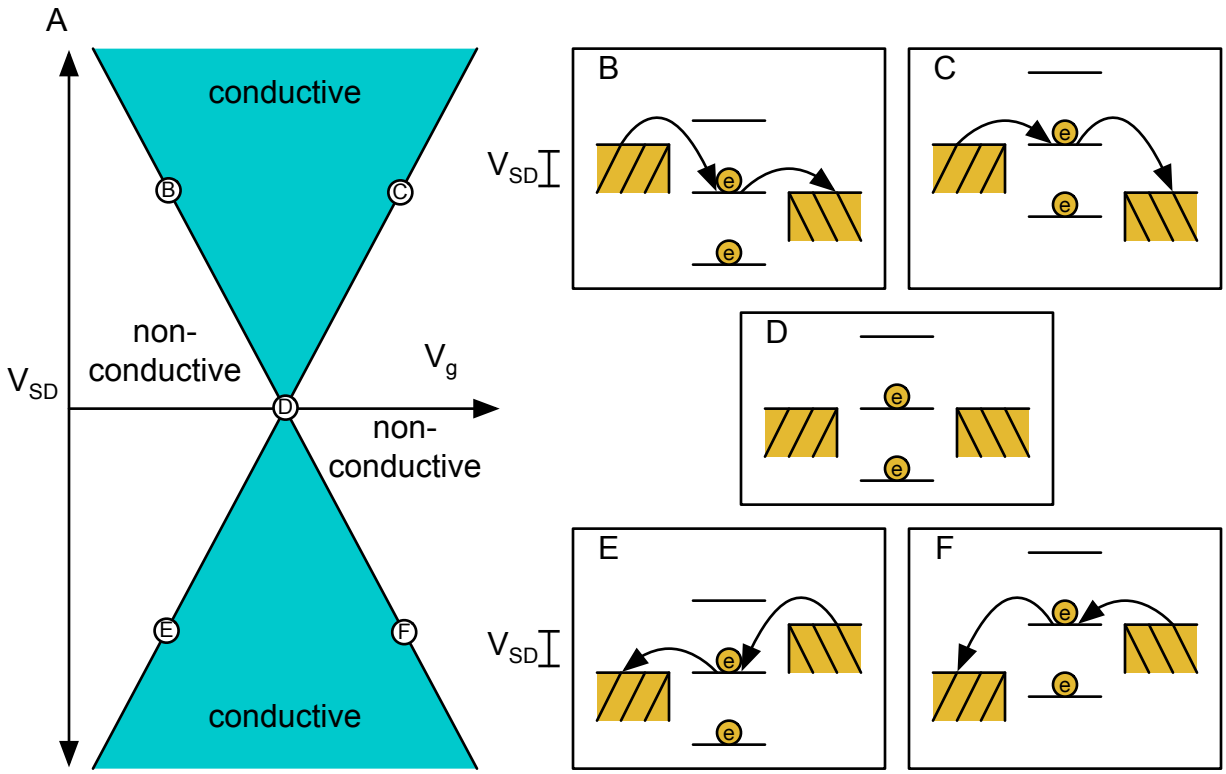

Figure 2.3: Bias spectroscopy can be used to extract the lever arm for a particular gate. The source-drain bias across the quantum dot V_{SD} is varied, as well as the voltage on the gate V_g. Whenever the electrochemical potential of the quantum dot is between the energy of the source and drain, electrons tunnel through the quantum dot, and the quantum dot's conductance becomes non-zero. The transition from a conductive quantum dot to a non-conductive quantum dot indicates that the dot's chemical potential is lined up with one of the reservoirs, which allows the gate voltage to be scaled by its effect on the quantum dot's energy.

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the additional complications of quantum dots in Si relative to GaAs, the ability to isotopically purify Si is immensely valuable and makes quantum dots in Si worth pursuing. The remainder of this thesis will exclusively focus on quantum dots in Si/SiGe heterostructures.

An example of a Si/SiGe heterostructure used to host quantum dots is depicted in Figure 2.1. The heterostructure includes a 12.5 nm tensile-strained layer of Si between two layers of relaxed $Si_{0.7}Ge_{0.3}$. The conduction band minimum of the strained Si layer is lower than that of the SiGe, which means that electrons prefer to accumulate in the Si quantum well. Because the heterostructure depicted in Figure 2.1 is an accumulation mode device,

electrons only accumulate when a positive voltage is applied to the electrostatic gates that are patterned on top of the heterostructure. When such a voltage is applied, the conduction band minimum in the quantum well passes below the substrate's Fermi level and a 2DEG accumulates there. Ohmic contacts are created far from the active region of the device using ion implantation of ^{31}P donors, which allows electrical access to the 2DEG.

In a simple capacitance model [19–22] (depicted in Figure 2.2), the electrostatic energy of the N-electron state of the quantum dot is

$$U(N) = \frac{(Ne)^2}{2C} - Ne\psi_{\text{ext}}.$$

The first term in $U(N)$ comes from the electrons within the quantum dot interacting with each other, as though they were charging a capacitor C; the second term comes from the electrons interacting with an electric potential generated by external sources, ψ_{ext}. Often a quantum dot's electrostatic energy dominates over other energy terms, but finding the quantum dot's total free energy $F(N) = U(N) + \Sigma_{p=1}^{N} E_p$ requires adding the energy of each occupied single-particle state E_p, which may include corrections for Zeeman splitting and orbital energy terms. Transitions between the N and N-1 electron state can happen when

$$\begin{aligned} E_F &= F(N) - F(N-1) \\ &= U(N) - U(N-1) + E_N \\ &= (N - 1/2)\frac{e^2}{C} - e\psi_{\text{ext}} + E_N, \end{aligned}$$

where E_F is the Fermi level in the leads. Thus, in the limit where $e^2/C \gg E_N$, transitions occur periodically in ψ_{ext} with charging energy e^2/C.

The conductance of the quantum dot near a transition (considered as $G = I/V_{\text{SD}}$ in the linear limit $V_{\text{SD}} \to 0$) can be found by using the grand canonical ensemble. In the resonant

tunneling regime, reference [19] shows that the conductance of the quantum dot is

$$G = G_{\max} \cdot \cosh^{-2}\left(\frac{\Delta_{\min}}{2k_B T_e}\right),$$

where $G_{\max}$ is the conductance of the quantum dot at its peak, k_B is the Boltzmann constant, T_e is the electron temperature, and $\Delta_{\min}$ is $F(N)-F(N-1)-E_F$ with N chosen to minimize its absolute value; the resonant tunneling regime is when $h\Gamma \ll k_B T_e \ll \Delta E$, where h is the Planck constant, Γ is the total rate at which electrons tunnel through the quantum dot, and ΔE is the energy level spacing. This formula is useful as it can be used to determine the electron temperature from a Coulomb blockade peak. Because $e\psi_{\text{ext}}$ usually varies linearly with the voltage on one of the electrostatic gates V_g, $\Delta_{\min}$ can often be approximated near a Coulomb blockade peak as $-\alpha_g(V_g - V_0)$, where α_g is the lever arm for gate g and V_0 is the voltage at which $E_F = F(N) - F(N-1)$ for the appropriate N, which gives

$$G = G_{\max} \cdot \cosh^{-2}\left(\alpha_g \frac{V_g - V_0}{2k_B T_e}\right).$$

The half-width-at-half-max for this transition with respect to gate g can be found by solving

$$\cosh^{-2}\left(\alpha_g \frac{V_g}{2k_B T_e}\right) = \frac{1}{2}$$

for V_g, giving a full-width-at-half-max of FWHM $\approx 3.53 k_B T_e/\alpha_g$. If α_g is known for a particular gate, a Coulomb blockade peak can be fit with this function and the electron temperature can be extracted; this is referred to as Coulomb blockade thermometry. However, in order to apply this formula, it is important to make sure that the quantum dot is in the resonant tunneling regime, which can be verified by checking two things: first that the transition is thermally broadened rather than tunnel-rate broadened (i.e. $h\Gamma \ll k_B T_e$), which can be checked by varying the tunnel rate and showing that the width of the peak doesn't change. Second, it should be verified that the height of the Coulomb blockade peak

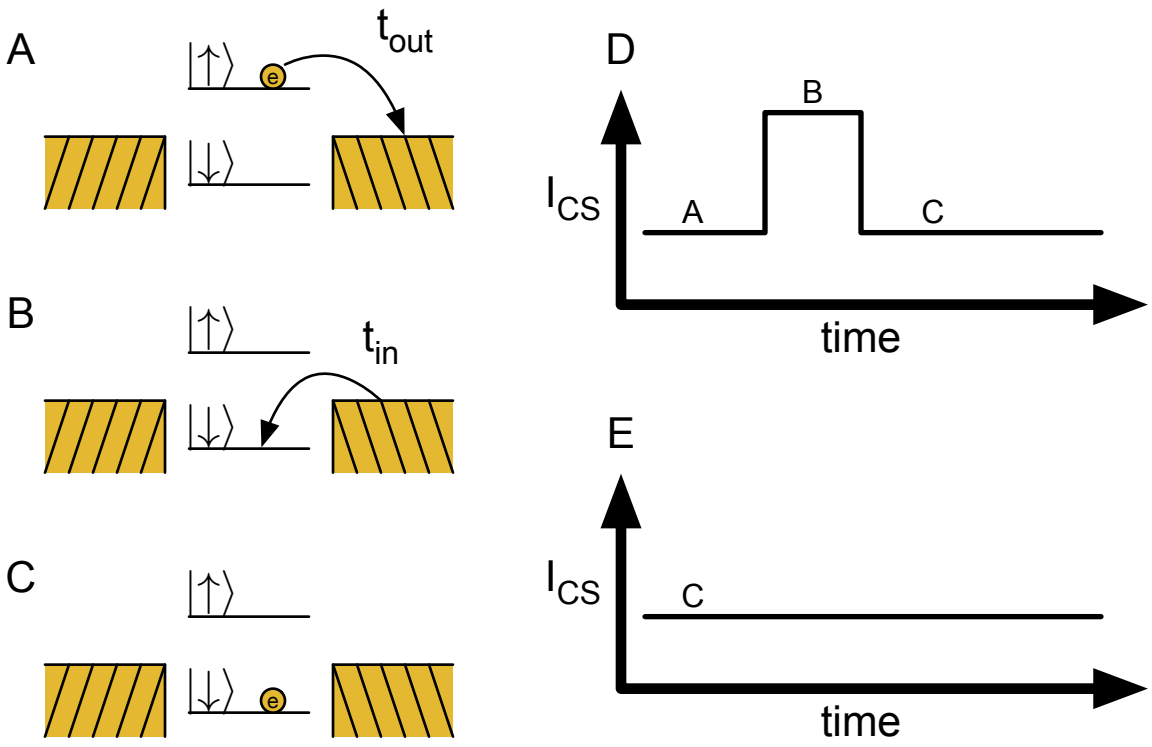

Figure 2.4: Panels A-C offer a schematic depiction of how the spin state of a single-electron quantum dot can be measured using a charge transition [23]. First, the energy of the spin states is split, for instance by applying an external magnetic field; then the quantum dot is tuned such that the electrochemical potential of the spin states straddle the Fermi level in a nearby electron reservoir. In this configuration, if the quantum dot is in the excited spin state (depicted in panel A), the electron will tunnel out of the quantum dot to the electron reservoir with some characteristic tunneling time t_{out}. When the electron tunnels out of the quantum dot (depicted in panel B), this can be measured using a nearby charge sensor. Subsequently, an electron will tunnel back into the quantum dot from the electron reservoir to fill the ground spin state with characteristic time t_{in}. Once the ground spin state of the quantum dot is filled (depicted in panel C), no more transitions will occur. Panel D (E) depicts the idealized conductance of a nearby charge sensor when the quantum dot starts in the excited (ground) spin state.

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decreases with increasing temperature, indicating that the quantum dot is not operating in the classical regime where $\Delta E \ll k_B T_e$.

The lever arm α_g for a particular gate g can be determined from bias spectroscopy of the quantum dot. In a bias spectroscopy measurement, the source-drain bias across the quantum dot V_{SD} is varied, as well as the voltage on the gate V_g. Whenever the electrochemical

potential for the Nth level state of the quantum dot $\mu(N) = F(N) - F(N-1)$ is between the energy of the source and drain, electrons tunnel through the quantum dot, and the quantum dot's conductance becomes non-zero. The transition from a conductive quantum dot to a non-conductive quantum dot indicates that the dot's chemical potential is lined up with one of the reservoirs, which allows the gate voltage to be scaled by its effect on the quantum dot's energy.

Changes in the number of electrons confined in the quantum dot can be observed by positioning a charge sensor near to the quantum dot. This charge sensor could be either a single electron transistor (SET), a quantum point contact (QPC) or even another quantum dot. Being sensitive to changes in the local electrostatic potential, the conductance of the charge sensor will change whenever an electron tunnels into or out of the quantum dot. While spin qubits generally use a computational basis whose states do not differ in terms of the number of electrons in the quantum dot, spin-to-charge conversion (depicted in Figure 2.4) allows their computational basis to be measured using a charge transition [16,23–25]. When the energy of spin states differ, the electrochemical potential of a quantum dot can be tuned such that it is energetically favorable for an electron in the higher energy state to tunnel out of the quantum dot, but not for an electron in the lower energy state. Thus if the quantum dot is in the excited spin state, an electron transition will occur; if the quantum dot is in the ground state, an electron transition will not occur.

Chapter 3

Characterization of a gate-defined double quantum dot in a Si/SiGe nanomembrane

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3.1 Abstract

We report the fabrication and characterization of a gate-defined double quantum dot formed in a Si/SiGe nanomembrane. In the past, all gate-defined quantum dots in Si/SiGe heterostructures were formed on top of strain-graded virtual substrates. The strain grading process necessarily introduces misfit dislocations into a heterostructure, and these defects introduce lateral strain inhomogeneities, mosaic tilt, and threading dislocations. The use of a SiGe nanomembrane as the virtual substrate enables the strain relaxation to be entirely

elastic, eliminating the need for misfit dislocations. However, in this approach the formation of the heterostructure is more complicated, involving two separate epitaxial growth procedures separated by a wet-transfer process that results in a buried non-epitaxial interface 625 nm from the quantum dot. We demonstrate that in spite of this buried interface in close proximity to the device, a double quantum dot can be formed that is controllable enough to enable tuning of the inter-dot tunnel coupling, the identification of spin states, and the measurement of a singlet-to-triplet transition as a function of an applied magnetic field.

3.2 Introduction

Quantum dots in group-IV semiconductor heterostructures have the potential to be suitable for scalable quantum computing, and have made important steps in recent years towards that goal [9,11]. Quantum dot qubits in silicon can be formed in several different ways by harnessing a combination of spin and/or charge states: successful realizations have demonstrated the single-spin qubit [27–30], the singlet-triplet qubit [31, 32], the charge qubit [33–35], the exchange-only qubit [36], and the hybrid quantum dot qubit [37, 38]. While metal-oxide-semiconductor devices can confine electrons at the Si-oxide interface independent of the Si strain state, Si/SiGe heterostructures only confine electrons in the Si quantum well if that well is under tensile strain, a state that is typically achieved by epitaxial growth on relaxed SiGe [39]. Strain grading methods enable the growth of such relaxed SiGe buffer layers, allowing the confinement of electrons in a Si quantum well, and the formation of two-dimensional electron gases with very high mobility [13, 40].

However, the goal of making a large array of uniform Si/SiGe quantum dots is still a major challenge that must be overcome if they are to be used in a scalable quantum computer. A fault tolerant quantum computer may require as many as 10^8 simultaneously tuned qubits [41], yet typical strain-graded heterostructures have qubit-affecting inhomogeneities on the length scale of a single qubit [42]. Three types of wafer inhomogeneities

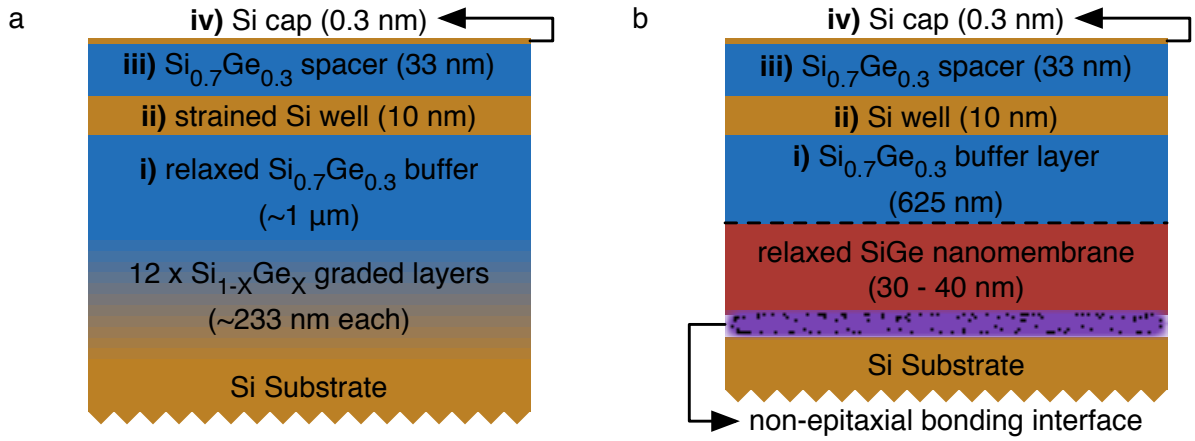

Figure 3.1: Traditional and nanomembrane-based Si/SiGe heterostructures for quantum dots. a) Schematic depiction of a traditional heterostructure, showing the strain-grading method of strain relaxation. Slowly increasing the Ge concentration during growth reduces the density of misfit dislocations and reduces defect bunching. The SiGe buffer, strained Si well, SiGe spacer, and Si cap layers (labeled i-iv respectively) are grown on top of the graded layers. A challenge in working with such strain-graded heterostructures is that the misfit dislocations that are a necessary part of this process contribute to inhomogeneities across an otherwise uniform wafer. b) Schematic depiction of the heterostructure used here, in which the SiGe layer is relaxed elastically using a nanomembrane-based method. The heterostructure below the dashed line is formed by transferring an elastically relaxed SiGe nanomembrane to a new handle wafer, where a non-epitaxial bonding interface is formed. The nanomembrane has no added dislocations, because it was grown below the critical thickness necessary for misfit dislocations, and then was released into liquid solution. After transfer, the SiGe buffer layer, Si quantum well, SiGe spacer, and Si cap (labeled i-iv respectively) were grown by chemical vapor deposition.

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have been studied in detail: variation of lateral strain, mosaic structure, and disorder on Si/SiGe interfaces. Strain inhomogeneities will cause variation in the band gap offset [43], and strain-graded heterostructures have been shown to include $\pm 0.10\%$ variations in strain over an area of 260 μm^2 [44]. Mosaic structure (i.e., tilting of crystalline lattice vectors) typically varies enough to impact spin qubits over length scales of one micron [42]. In addition, atomic level disorder on the interface between Si and SiGe layers, including single atomic steps, can greatly suppress the singlet-triplet splitting in quantum dots [45, 46].

All three of these qubit-affecting defects are known to be caused by misfit dislocations, defects that are intentionally introduced as a part of the strain grading process [17]. A het-

erostructure formed through strain grading processes is depicted in Figure 3.1a. Regardless of how gradually strain is introduced into a heterostructure, strain grading processes will create a buried network of misfit dislocations [18]. As a consequence, one of the root causes of heterostructure inhomogeneities cannot be eliminated without adopting a new method of strain relaxation.

A liquid release method of elastic strain relaxation has been proposed as a path towards the production of highly uniform heterostructures, because it provides a path to the formation of relaxed SiGe without the introduction of misfit dislocations [44, 47–49]. The process begins by growing a layer of SiGe on silicon-on-insulator (SOI) such that its thickness is below the critical thickness necessary to form misfit dislocations. This single crystal SiGe nanomembrane is then released into liquid solution through subsequent HF, KOH, and H_2O dips. Free of any rigid substrate, the nanomembrane elastically relaxes to its natural lattice constant. Finally, the nanomembrane is transferred to a new Si handle wafer where it can undergo further epitaxial growth to form the rest of the heterostructure. Figure 3.1b depicts a heterostructure created using the liquid release method of strain relaxation. Micro-Raman spectroscopy has shown that there is less lateral strain variation in such transferred nanomembrane heterostructures than in conventionally-strain-graded heterostructures [44]. Previous work has shown that electron gases formed in transferred nanomembranes already have electron mobility in the range 40,000–80,000 $cm^2/(V{\cdot}s)$ at a carrier density of $4{\times}10^{11}$ cm^{-2} [49], a mobility that in principle is high enough to form gate-defined quantum dots [50, 51]. However, the nanomembrane transfer process necessarily introduces a non-epitaxial interface between the Si handle wafer and the transferred SiGe nanomembrane. While this interface is approximately 625 nm distant from the quantum dots, larger than the size of the device itself, this interface has the potential to disrupt the stability of single-electron devices if it increases charge instability (switching noise) in the sample.

Here we report the first fabrication and characterization of a double quantum dot formed

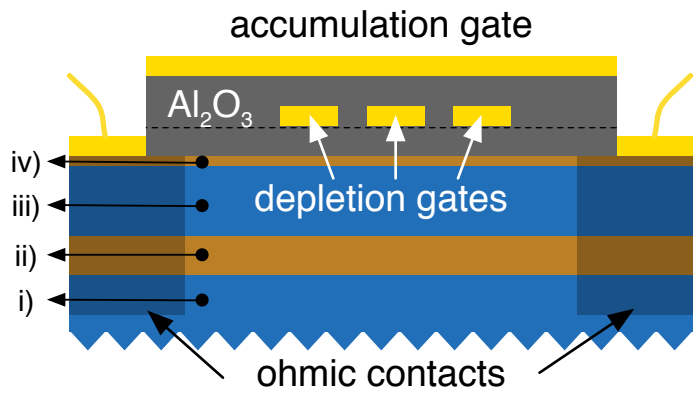

Figure 3.2: Schematic depiction of a cross-section of the measured device. The heterostructure layers are labeled with the same roman numerals as in Figure 3.1b. A 10 nm layer of Al_2O_3 was added to the heterostructure via atomic layer deposition, and ohmic contacts were created through ion implantation. Fine feature depletion gates (Ti/Au) were metallized on top of the oxide; a second layer of Al_2O_3 was deposited, followed by another layer of Ti/Au gates. The dashed line in the diagram shows the boundary between the first and second layer of Al_2O_3.

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in a Si/SiGe nanomembrane heterostructure. We show that the nanomembrane heterostructure supports the formation and measurement of high-quality, gate-defined quantum dots, including the ability to reach the few electron regime, the ability to coherently tune the inter-dot tunnel coupling of two quantum dots, stability under the application of RF pulses, and sufficient repeatability to enable the performance of magnetospectroscopy of the quantum dot energy levels. These results provide strong evidence that the presence of a non-epitaxial interface between the silicon handle wafer and the wet-transferred nanomembrane does not degrade in an observable way the stability or performance of gate-defined quantum dots.

3.3 Methods

Figure 3.2 shows a schematic cross section of the Si/SiGe nanomembrane-based double quantum dot studied here, in which all carriers are induced by gates and no dopants are placed in the active area of the device [52–55], eliminating a key source of charge noise [56]. After the second heterostructure growth on the elastically relaxed SiGe nanomembrane, a 10 nm

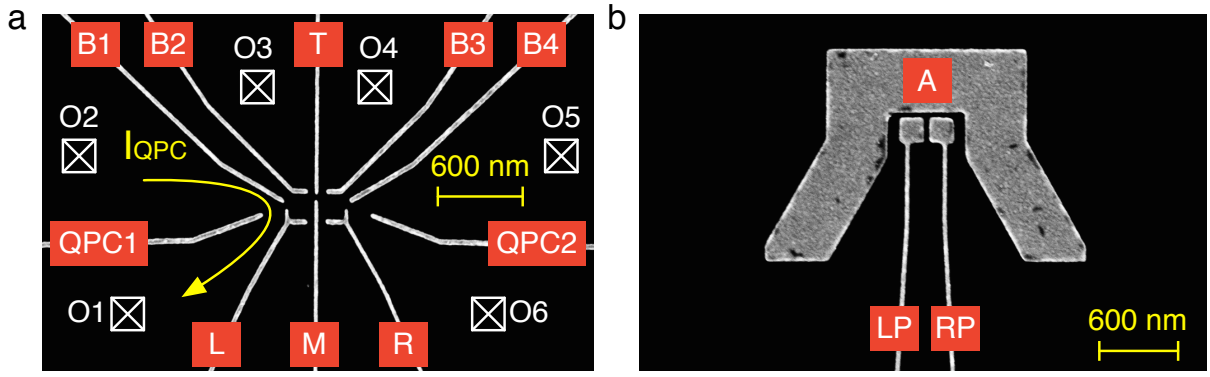

Figure 3.3: Double quantum dot fabricated on a Si/SiGe nanomembrane. a) SEM image of a test pattern whose gate design is identical to the lower layer of gates used for the measured device. The lower layer of gates includes two quantum point contacts for charge sensing (QPC1-2), four barrier gates (B1-4) and a top gate (T) for controlling access to electron reservoirs, left and right plunger gates outfitted for RF control of the dot (L and R), and a middle (M) gate intended to control the inter-dot tunnel rate. The charge sensing experiments reported below were performed with current flowing along the path indicated by the yellow arrow, around QPC1 and through the left quantum point contact. b) SEM image of a device whose gate design is identical to that of the upper layer of gates of the measured device. The upper layer of gates includes an accumulation gate (A) that controls all of the electron reservoirs, and the left and right paddle (LP and RP, respectively), which control the energy of the left and right dot, respectively.

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layer of Al_2O_3 was grown by atomic layer deposition (ALD). To create ohmic contacts, regions of oxide were etched away, and at these locations ^{31}P donors were implanted with a density of 5×10^{15} cm^{-2}; these regions were subsequently covered with 4 nm Ti and 36 nm Au. The lower layer of gates was patterned using e-beam lithography and metallization with an e-beam evaporator (2 nm Ti/20 nm Au). Figure 3.3a shows a scanning electron microscope (SEM) image of a test pattern whose gate design is identical to the lower gate layer for the device studied here. This lower layer includes two quantum point contacts for charge sensing (QPC1,2), four barrier gates (B1-4) and a top gate (T) for controlling the electron reservoirs, left and right plunger gates outfitted for RF control of the dot (L and R), and a middle gate (M) intended to control the inter-dot tunnel rate. A second layer of Al_2O_3 was grown using ALD, this time with a thickness of 80 nm, followed by an upper layer of accumulation gates, which was patterned and metallized with 2 nm Ti and 20 nm Au.

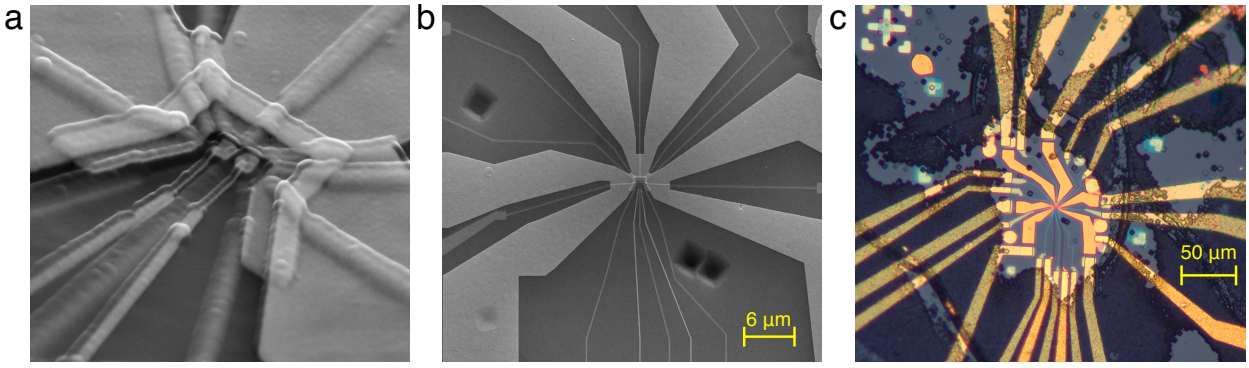

Figure 3.4: Double quantum dot fabricated on a Si/SiGe nanomembrane. a) Angled SEM image of the measured device, showing the union of two layers of electrostatic gates separated by oxide. No scale bar can be provided because the image was taken at an angle. b) SEM image of the measured device and the surrounding heterostructure. The gate patterns from panels b and c were placed to avoid visible defects, like the pits seen in this image. Gate A was extended from what is shown in panel c from the dot region all the way to the ohmic contacts. c) Optical image of the measured device, showing rips and folds in the nanomembrane, which appeared during the liquid release and cleaning processes and are discussed in more detail in the text.

Figure 3.3b shows a test pattern whose gate design is identical to the upper gate layer for the device studied here and includes a left and right paddle for changing dot occupation (PL and PR) and an accumulation gate to regulate access to the ohmic contacts (A). In a final lithography step, this accumulation gate was extended all the way to the ohmic contacts. Figure 3.4a is a tilt-view SEM image of the completed device. Figure 3.4b is a larger-scale, top-down SEM image of the device and the surface of the surrounding heterostructure. Aside from a few pit defects, the heterostructure is quite uniform in the vicinity of the completed double quantum dot, demonstrating that membrane transfer is compatible with smooth and flat heterostructure regions. Figure 3.4c is an optical image at an even larger scale of the completed device; on this scale numerous tears and gaps are visible in the nanomembrane, and the device was carefully designed and fabricated to fit onto a clean and uniform portion of the nanomembrane. It is interesting to consider the structure of the interface between the nanomembrane and the substrate. While the small available area in this sample precludes scanning transmission electron microscopy (STEM) measurements in this work, previous

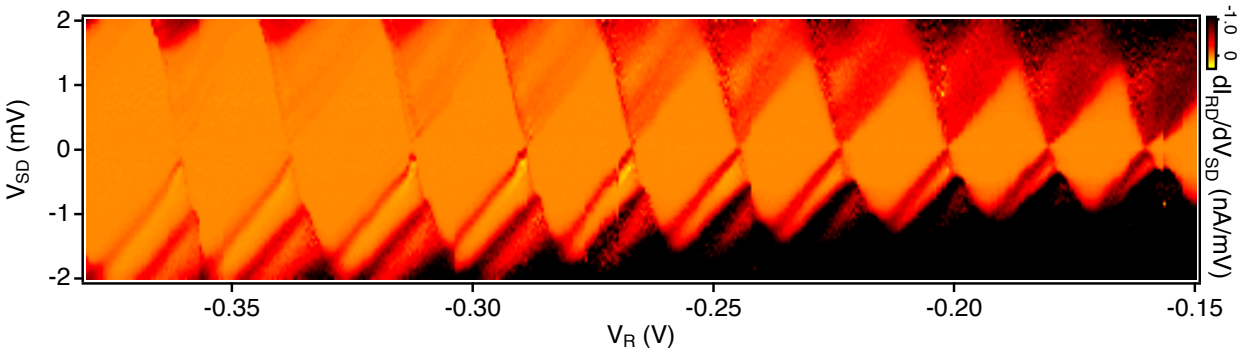

Figure 3.5: Characterization of a single dot formed on the right side of the device, RD: Bias spectroscopy in the many electron regime, plotting the differential conductance across RD with current flowing from O3 to O4. Coulomb blockade is manifest with variation of the voltage on gate R (V_{R}) and the source-drain bias (V_{SD}).

STEM measurements on transferred membranes have shown the interfacial region to have a thickness between 1 and 3 nm [57]. While this non-uniformity is present in the measured device and made the fabrication more challenging, it does not appear to be an inevitable part of nanomembrane devices; the damage observed in Figure 3.4c could have been avoided by carefully regulating the sonication power used during the cleaning step immediately prior to the second epitaxial growth. The completed double quantum dot structure was mounted in a dilution refrigerator with a base temperature of $\sim$40 mK.

3.4 Results and Discussion

We first present measurements of a single quantum dot formed on the right side of the device (RD), which could be measured both by transport through the quantum dot between ohmic contacts O3 and O4 and by charge-sensing by measuring the current through the left quantum point contact, that is to say around QPC 1 and between ohmic contacts O1 and O2. Figure 3.5 shows the differential conductance across the quantum dot as a function of the applied source-drain bias voltage and the voltage on gate R. Numerous Coulomb diamonds are visible with no significant background charge rearrangement, demonstrating the stability of the background charge environment provided by the nanomembrane.

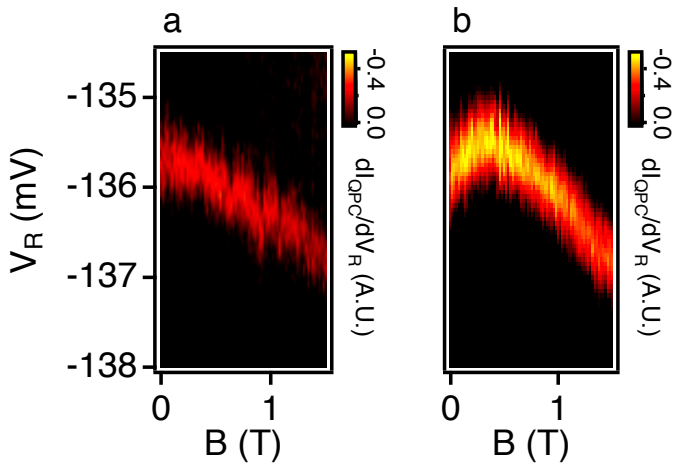

Figure 3.6: Characterization of a single dot formed on the right side of the device, RD. Panels a and b present charge-sensing measurements using the left quantum point contact, with current flowing around QPC1 from O1 to O2. Panels a and b show the results of magnetospectroscopy on the 0-to-1 and 1-to-2 electron transitions, respectively. The singlet and triplet two-electron states are degenerate at 0.38 T, which corresponds to a zero-field singlet-triplet splitting of 44 μeV. Panel b has the same vertical scale range as panel a and is shifted by -75.5 mV.

The Coulomb diamonds in Figure 3.5 increase in size with each expelled electron as gate voltage V_{R} is made more negative, moving from right to left in the figure. Continuing in this direction, the quantum dot was brought into the few-electron regime by tuning the voltages on gates R and RP. Further characterization in the few-electron regime was performed by charge sensing using the left quantum point contact, performing a lock-in measurement of the current between ohmic contacts O1 and O2 while modulating V_{R}. Figure 3.6a shows the results of magnetospectroscopy for a transition where the number of valence electrons changes from zero to one (below we show evidence that there may be an additional closed shell of electrons). As the in-plane magnetic field B is increased from 0 T to 1.5 T, the transition from zero to one electron occurs at progressively lower values of V_{R}, consistent with loading a spin-down electron. Figure 3.6b shows the results of an analogous magnetospectroscopy measurement on the 1-to-2 electron transition; in this case, as the applied magnetic field increases from 0 T to 0.38 T, the transition from one to two electrons occurs at progressively higher values of V_{R}, consistent with a transition from a single spin-down electron to a two-

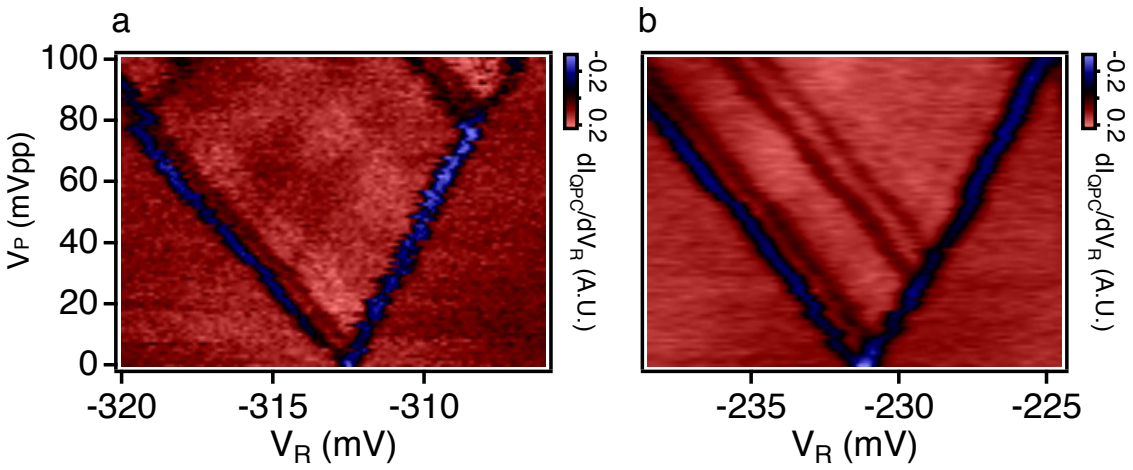

Figure 3.7: Characterization of a single dot formed on the right side of the device, RD. Panels a and b present charge-sensing measurements using the left quantum point contact, with current flowing around QPC1 from O1 to O2. Panels a and b present pulsed-gate spectroscopy on the 0-to-1 electron transition and the 1-to-2 electron transition respectively. Panels a and b are obtained by measuring the differential conductance of the QPC with respect to gate R while pulse trains of peak-to-peak amplitude V_{P} are applied to gate R at frequencies 1.0 MHz and 500 kHz, respectively, which enables the characterization of excited states of the dot [60]. Panel a shows an excited state 56 μeV above the 1 electron ground state (likely a valley excitation). Panel b shows an excited state 50 μeV above the 2 electron state (likely a triplet state where one electron has accessed the valley excited state from panel a).

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electron singlet (S) state. In contrast, from $B = 0.38$ T to 1.5 T the transition from one to two electrons occurs at progressively lower values of V_{R}, consistent with the transition from a single spin-down electron to a two-electron triplet T_- state. The transition of the two-electron ground state from singlet to triplet at $B = 0.38$ T corresponds to a zero-field singlet-triplet splitting of 44 μeV, comparable to values observed in quantum dots grown on conventional strain-graded heterostructures [31, 58, 59].

To probe the excited states of the dot, pulsed-gate spectroscopy was performed, with a square wave voltage applied to gate R enabling loading of excited states [61, 62]. The gate lever arms used to convert the voltage on gate R to the electrostatic energy of the right dot are $\alpha_{\mathrm{R,RD}} = 78$ μeV/mV for the 0-to-1 electron transition and $\alpha_{\mathrm{R,RD}} = 45$ μeV/mV for the 1-to-2 electron transition and were extracted from the slope of the transition lines in

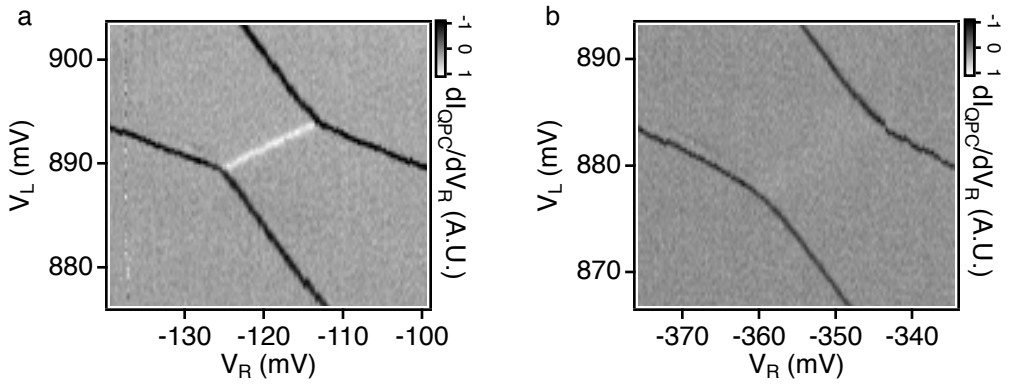

Figure 3.8: Measurements of a double quantum dot formed in a nanomembrane, demonstrating a highly tunable inter-dot tunnel coupling. Charge sensing is performed by modulating the voltage applied to gate R at 213 Hz and performing a lock-in measurement of the real component of the response of the current from O1 to O2. Panels a and b show stability diagrams measured by varying V_R and V_L. A negative current response (a dark line) is observed when an electron transitions from either dot to a reservoir, and a positive current response (a white line) occurs at the polarization line at which an electron shifts between the dots. a) Stability diagram obtained with $V_M = 0.926\ V$, where the inter-dot tunnel coupling is small. The polarization line is sharp because the tunnel rate is low and thus the lifetime broadening is small. b) Stability diagram obtained with $V_M = 0.974\ V$, where the tunnel coupling is high. The polarization line is barely visible because it is strongly lifetime-broadened.

Figures 3.6b,c. Figure 3.7a shows data for the 0-to-1 transition; in this panel, a series of 420 ns square pulses with amplitude V_P was applied to gate R with a repetition rate of 1 MHz. The single-electron excited state with the lowest energy is 56 μeV above the ground state, an energy that is consistent with a predominately valley-like excitation in Si/SiGe quantum devices [46, 52, 63, 64]. In the upper left corner of Figure 3.7a a line extends towards the lower left and intersects with the so-called "loading line." This line would correspond to an excited state of the 0-electron configuration, and thus it suggests the presence of a closed shell of electrons in the quantum dot. Figure 3.7b shows pulsed-gate spectroscopy for the 1-to-2 electron transition. For this transition, a series of 800 ns square pulses with amplitude V_P was applied to gate R with a repetition rate of 500 kHz, which allowed loading of the two-electron excited states. Three two-electron excited states are visible; the two-electron excited state with the lowest energy sits 50 μeV above the two-electron ground state, consistent with the singlet-triplet splitting observed in Figure 3.6b.

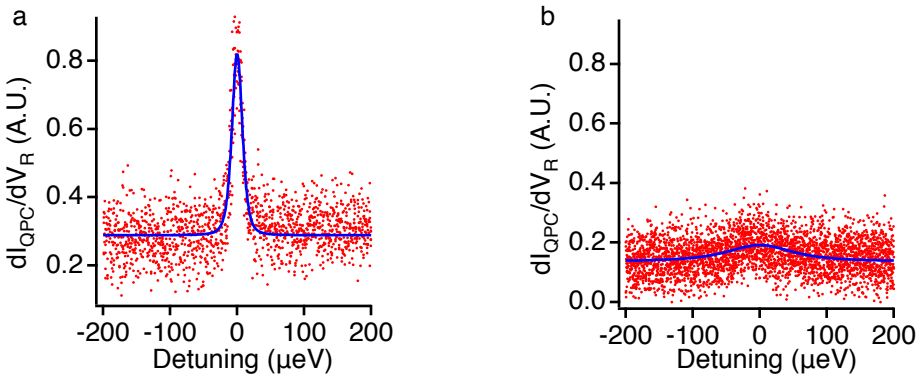

Figure 3.9: Panels a) and b): Tunnel couplings are extracted from the stability diagrams in Figure 3.8 panels a and b, respectively, by converting measured voltages into detuning using gate lever arms and fitting the transition widths, following Ref. [65]. The gate lever arm $\alpha_{\mathrm{R,RD}}$ was extracted from the magnetospectroscopy data of Figure 3.6; other pertinent gate lever arms were then obtained geometrically using the data in Figure 3.8.

We now discuss the formation of a double quantum dot, for which gate M was used to control the inter-dot tunnel rate. Figures 3.8a,b show stability diagrams for the device, with Figure 3.8a acquired with $V_{\mathrm{M}} = 0.926$ V and Figure 3.8b acquired with $V_{\mathrm{M}} = 0.974$ V. The difference in tunnel rate between these two stability diagrams can be observed in two ways: first, while the polarization line in Figure 3.8a appears as a sharp, white line, the polarization line in Figure 3.8b is barely visible. This difference arises because in Figure 3.8a the tunnel coupling is small, so the energy eigenstates transition abruptly from one charge state to the other. In contrast, when the tunnel coupling is large, the polarization line is very broad, indicating a much smoother transition in the charge state composition of the energy eigenstates [65]. Second, whereas the dot-to-reservoir electron transitions in Figure 3.8a have sharp corners at their junction with the polarization line, the dot-to-reservoir electron transitions in Figure 3.8b show significant rounding near junctions with the polarization line, a phenomenon that arises because the increased tunnel coupling reduces the kinetic energy for electrons in the double quantum dot [66].

To extract the tunnel coupling from Figure 3.8a, Figures 3.9a,b plot the lock-in signal as a function of the electrostatic energy difference between the left and right dots (the detuning),

effectively superposing sections through the polarization line with many different values for the total double-dot energy. Each data point was projected onto the detuning axis using the pertinent gate lever arms; $\alpha_{\mathrm{R,RD}}$ was established from the magnetospectroscopy data, and the other lever arms were determined geometrically from the slopes of the transition lines in Figure 3.8a and the value of $\alpha_{\mathrm{R,RD}}$. Following the approach of Ref. [65], we express I_{QPC}, the current through the charge-sensing QPC, as

$$I_{\mathrm{QPC}} = I_0 + \frac{\Delta I_{\mathrm{QPC}}}{2}\left[1 - \frac{\varepsilon}{\Omega}\tanh\left(\frac{\Omega}{2k_BT}\right)\right] + \Gamma\varepsilon,$$

where ε is the detuning, $\Omega = \sqrt{\epsilon^2 + 4\Delta^2}$ is the energy difference between the two eigenstates, k_B is the Boltzmann constant, T is the electron temperature, I_0 is a current offset fit parameter, ΔI_{QPC} is a parameter for fitting the quantum point contact's sensitivity to an inter-dot charge transition, and Γ is a parameter characterizing gate-to-QPC crosstalk. The current offset I_0 typically ranged from 200 pA to 1 nA, which is comparable to other studies [51, 62, 67]. The data from Figures 3.9a,b are fit with $\partial I_{\mathrm{QPC}}/\partial V_R =$

$$\alpha_{\mathrm{R},\epsilon}\frac{\Delta I_{\mathrm{QPC}}}{2}\left[\left(\frac{\epsilon^2}{\Omega^2} - 1\right)\frac{\tanh\left(\frac{\Omega}{2k_BT}\right)}{\Omega} + \frac{-\epsilon^2/\Omega^2}{2k_BT\cosh^2\left(\frac{\Omega}{2k_BT}\right)}\right] + \alpha_{\mathrm{R},\epsilon}\Gamma,$$

where $\alpha_{\mathrm{R},\epsilon} = \partial\epsilon/\partial V_{\mathrm{R}}$ is the lever arm that converts changes in the voltage on gate R to changes in the detuning. The electron temperature T was taken to be 50 mK, consistent with the width of the dot-to-reservoir transitions (assumed to be primarily temperature broadened). The fits to the data in Figures 3.9a,b yield $\Delta/\mathrm{h} = 0.97\pm0.08$ GHz and $\Delta/\mathrm{h} = 9.1\pm0.8$ GHz, respectively, where Δ is the inter-dot tunnel coupling. The QPC sensitivity ΔI_{QPC} was found to be roughly 2 pA in the fit, consistent with an independent measurement, and corresponding to a fractional change in resistance comparable to that found in other charge sensing measurements [51]. Figure 3.10 presents the results of a similar analysis for a total of 7 datasets, demonstrating the achievement of a wide range of tunnel couplings

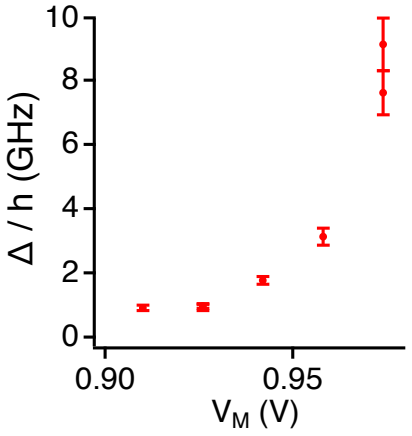

Figure 3.10: Plot of the extracted tunnel coupling Δ over a range of values for V_{M}, showing that the tunnel coupling can be tuned over a wide range. The error bars are derived from an unweighted least-squares fit.

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for various values of V_{M}. The extraction of Δ is difficult for very large tunnel couplings, as is clear from Figure 3.9b; for this reason, we plot two values of the tunnel coupling for $V_{\mathrm{M}} = 0.974$ V in Figure 3.10, which were extracted from two different stability diagrams taken roughly a day and a half apart. Similarly, two values for the tunnel coupling are plotted for $V_{\mathrm{M}} = 0.926$ V, values which were extracted from separate stability diagrams taken roughly a day apart. In comparison to the data points for $V_{\mathrm{M}} = 0.974$ V, the two data points for $V_{\mathrm{M}} = 0.926$ V are in such close agreement that they are difficult to distinguish.

Finally, Figure 3.11 reports measurement of a double-dot stability diagram in the presence of short voltage pulses, demonstrating the stability of the device in the presence of very high-bandwidth driving. An arbitrary wave generator with a rise time of 40 ps was used to apply a series of 200 ps square pulses to gate L at a repetition rate of 20 MHz, which caused abrupt changes in the electric potential of the dots. When either dot was energetically close to a charge transition, applying such a series of pulses was likely to induce charge transitions in the dot, which caused a change in QPC current ΔI relative to a similar sequence of null pulses. Figure 3.11 shows the derivative of ΔI with respect to V_{R}, which highlights regions where a charge transition is induced by the applied sequence of square pulses. The

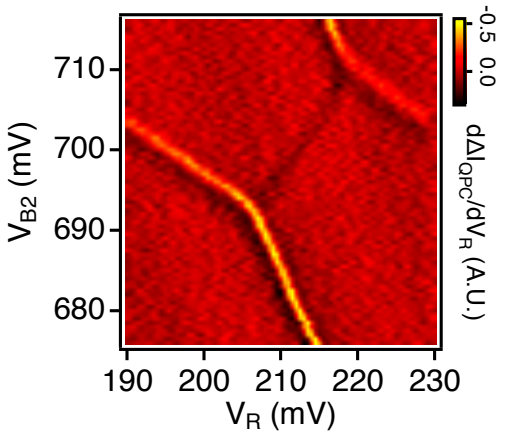

Figure 3.11: Charge stability diagram extracted by applying nominally 200 ps square pulses to gate L, which creates a current response ΔI in the left QPC, thereby demonstrating charge stability under application of high frequency pulses.

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nanomembrane heterostructure of this device provides a stable electrostatic environment for the quantum dots, even when the double quantum dot system is driven by high-bandwidth voltage pulses.

3.5 Conclusions

The results discussed above demonstrate a new path towards the confinement of electrons in Si/SiGe gate-defined quantum dots: we have reported characterization of a double quantum dot formed in a heterostructure created using the liquid release method of strain relaxation. This method of strain relaxation is a powerful tool for the formation of heterostructures with much better uniformity than those created through conventional relaxation methods. The key advantage of this approach is that it does not depend on the insertion of misfit dislocations for strain relaxation, and instead it relies entirely on elastic relaxation of a single-crystal SiGe membrane. In addition, in the future it may be possible to place membrane-based quantum well heterostructures over arrays of back-gates, providing a functionality that is required for a recently proposed surface code spin qubit architecture [68]. The measurements we report here address the stability of a double quantum dot fabricated on a Si/SiGe

heterostructure grown epitaxially on such a transferred, relaxed SiGe nanomembrane. We demonstrated that the liquid release method of strain relaxation can produce quantum dots that are stable under a wide range of measurement conditions, and we showed that the inter-dot tunnel coupling was easily tuned over a wide range of values. The buried interface created during the wet transfer of the relaxed nanomembrane is far less controlled than the purely epitaxial heterostructures that in the past were used exclusively for Si/SiGe quantum dot experiments. The results presented above provide significant evidence that this interface formed 625 nm below the quantum well does not preclude the formation of high-quality and stable double quantum dots.

3.6 Acknowledgements

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Chapter 4

A practical guide to cryogenic amplification

4.1 Introduction

While spin qubits have acheived long coherence and relaxation times by using the spin degree-of-freedom, fast readout times are typically achieved by converting from spin to charge states [16, 23–25]; thus charge detection is an important tool for state readout of semiconductor spin qubits. Yet finding a fast, reliable, and scalable method of charge detection with a good signal-to-noise ratio (SNR) remains a challenge for the field, given that samples must be placed within an ultra-low temperature cryostat (commonly a dilution refrigerator).

Perhaps the most straightforward way to use a quantum point contact (QPC), single electron transistor (SET), or quantum dot (QD) for charge sensing is to apply a source-drain bias and measure the resulting current using a room temperature transimpedance amplifier. Under this method (depicted in Figure 4.1), the measured current is sensitive to local changes in the electrostatic potential. When properly set up, the DC current passing through one of these charge sensors might be ∼1 nA, while the change in current resulting from a single charge transition might ∼100 pA. Commercially available current pre-amplifiers can easily

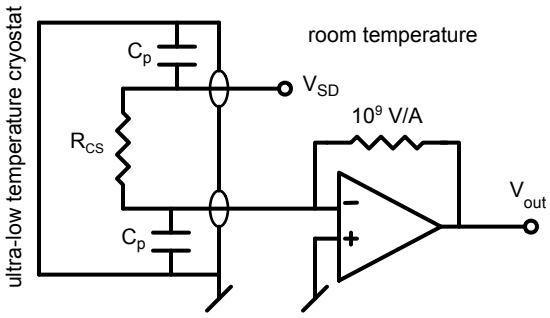

Figure 4.1: Circuit diagram depicting how a room temperature transimpedance amplifier can be used to measure the resistance of a charge sensor (R_{CS}): a source-drain bias (V_{SD}) is applied across the charge sensor and the resulting current is measured. Detection of a single electron transition typically involves measurement of a ∼100 pA shift in current, which can easily be detected by commercially available transimpedance amplifiers in a limited bandwidth (e.g. 100 Hz); yet the SNR for detecting a single electron transition will suffer at higher bandwidths. For quantum computing, the necessity of placing the qubit and charge sensor within an ultra-low temperature cryostat introduces additional complications for high bandwidth measurements: first, ultra-low temperature cryostats introduce additional noise into current measurements, particularly tribo-electric noise arising from vibrations. Second, the wiring constraints of ultra-low temperature cryostats generally introduce ∼100 pF of parasitic capacitance C_p between the charge sensor and room temperature electronics, which can further limit a measurement's bandwidth.

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detect a 100 pA signal in a limited bandwidth (e.g. 100 Hz), but even in an ideal case the signal-to-noise ratio will suffer at larger bandwidths [69]. For instance, the DLPCA-200 transimpedance amplifier from Femto has a bandwidth of up to 500 KHz on the 10^4 V/A sensitivity setting, but has a minimum specification of 2.4 nA_{RMS} of input-referred noise with this setting. While the input-referred noise can be lowered by going to a higher current sensitivity with this amplifier, such a change would increase the input impedance of the amplifier, resulting in a smaller bandwidth. To achieve less than 50 pA_{RMS} input-referred noise with the DLPCA-200 from Femto, one would have to increase the sensitivity to 10^7 V/A, where the amplifier only has 50 KHz bandwidth. Other transimpedance amplifiers (such as the DL1211 from DL Instruments) are limited by a comparable trade-off between noise and bandwidth.

Outside of ideal cases, the necessity of placing the qubit and charge sensor within an

ultra-low temperature cryostat introduces additional complications on measurements with bandwidths above ∼50 KHz: first, ultra-low temperature cryostats introduce additional noise into current measurements, particularly tribo-electric noise arising from vibrations. Dry dilution refrigerators, where pulse-tube coolers drive additional vibrations, are particularly hurt by tribo-electric noise [70]. Second, the wiring constraints of ultra-low temperature cryostats often impose additional bandwidth limitations on the electrical lines used for measurement. Each electrical line passing from room temperature down to the cold stages of an ultra-low temperature cryostat needs to be heat sunk and filtered in order to prevent radiative and conductive heating of the sample being measured. In short: room temperature transimpedance amplifiers work nicely for low frequency charge detection, but complications arise when one needs a larger measurement bandwidth.

A higher SNR can be achieved by introducing cryogenic amplification between the charge sensor and room temperature electronics, and numerous approaches have been studied and implemented. These differing approaches can be broken into three broad classifications: current-to-current amplification, RF reflectometry, and dispersive gate readout.

Cryogenic current-to-current amplification uses a non-linear active electronic component (typically a HEMT or HBT) in order to boost the current passing through a charge sensor before it exits to room temperature. This form of cryogenic amplification makes improvements over normal current measurement in two ways: first, any tribo-electric noise that is introduced after amplification will have a reduced effect on the signal-to-noise ratio. Second, the parasitic capacitance between the sample and amplifier (which can limit measurement bandwidth) can be largely eliminated simply by moving the amplifier closer to the sample. One example of current-to-current amplification placed a cryogenic HEMT amplifier on the still of a dilution refrigerator [71]; while this approach showed an increased measurement bandwidth, it was still hampered by a large parasitic capacitance between the sample and amplifier. Other work has positioned current-to-current amplification right next to the sample, heat sinking the amplifiers to the mixing chamber of the dilution refrigerator; promising

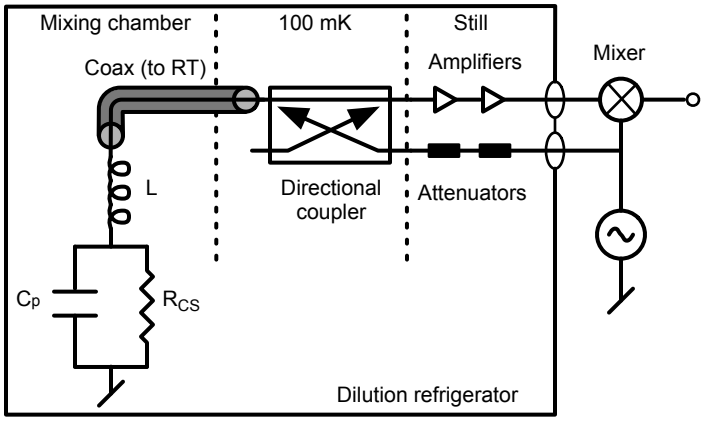

Figure 4.2: Circuit diagram for RF reflectometry, where a charge sensor is measured through its damping of a resonant circuit. The resonant circuit is used to terminate a transmission line, and is set up such that its reflection coefficient is sensitive to changes in the impedance of the charge sensor. Microwaves are applied to the resonant circuit from room temperature, passing through several attenuators; due to a directional coupler, the reflected wave is amplified rather than attenuated on the way back to room temperature, where it is processed using an IQ mixer.

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increases in SNR have been shown using this technique [69, 72, 73]. Yet the primary disadvantage of heat sinking an amplifier to the mixing chamber of a dilution refrigerator is that any heat dissipation from the amplifier has the potential to heat the sample being measured.

Another way to avoid the detrimental impact of parasitic capacitance is RF reflectometry, where a charge sensor can be measured through its damping of a resonant circuit (depicted in Figure 4.2). The resonant circuit is used to terminate a transmission line, and is set up such that its reflection coefficient is sensitive to changes in the impedance of the charge sensor. In this case, the capacitance to ground between the resonant circuit and amplification is not eliminated, but rather contributes to the characteristic impedance of a transmission line, where the total capacitance does no harm. Yet while RF reflectometry mitigates the effects of parasitic capacitance between the resonant circuit and cryogenic amplification, successful measurement depends on the capacitance of the resonant circuit, which puts constraints on device packaging and sample parasitics [74–77].

Dispersive gate readout is another important technique for sensing charge transitions in quantum dot qubits. Rather than using an auxiliary charge sensor (like a QPC, QD, or

SET), dispersive gate readout probes the capacitance of a quantum dot directly in order to detect charge transitions [78, 79]. Some approaches to dispersive gate readout have attached a quantum dot sample to a resonant circuit and measured shifts in the circuit's reflection coefficient much like other RF reflectometry approaches [80]; the advantage of this approach is that eliminating an auxiliary charge sensor saves space on the quantum dot sample. Other promising work has used a microwave cavity coupled to a quantum dot for charge sensing [81–83].

While there are advantages and disadvantages associated with each of the cryogenic amplification schemes described above, charge sensitivity is commonly reported as the figure of merit for comparison [80, 81, 84, 85], which is defined as

$$\text{Charge Sensitivity} = \frac{e}{\text{SNR}_\text{i} \cdot \sqrt{\text{BW}}} \simeq \frac{e \cdot \sqrt{\tau_\text{int}}}{\text{SNR}_\text{i}},$$

where BW is the time-domain bandwidth of the measurement, τ_int is the integration time used to take an electrical measurement, and SNR_i is the signal-to-noise ratio calculated as a current ratio σ_s/σ_n, where σ_s is the RMS value of the current signal and σ_n is the RMS value of the current noise. This definition for signal-to-noise ratio is common in the context of image processing and edge detection [86], though it's worth mentioning that a different definition is common in the context of electronics [87]: the signal-to-noise ratio can also be defined as the power ratio $\text{SNR}_\text{p} = \sigma_s^2/\sigma_n^2$. In order to keep charge sensitivity the same regardless of whether one reports SNR_p or SNR_i, charge sensitivity is defined differently when using SNR_p:

$$\text{Charge Sensitivity} = \frac{e}{\sqrt{\text{SNR}_\text{p} \cdot \text{BW}}} \simeq e\sqrt{\frac{\tau_\text{int}}{\text{SNR}_\text{p}}}.$$

It's also worth noting that the two definitions for charge sensitivity maintain the same tradeoff between signal-to-noise ratio and bandwidth (i.e. the tradeoff associated with white noise). Both definitions for signal-to-noise ratio are acceptable, but SNR_p can be misleading

when reported with the threshold method commonly used to identify charge transitions. The threshold method of charge detection identifies charge transitions whenever a measured current passes a pre-determined threshold [23]; a current above the threshold corresponds to one charge state and a current below the threshold corresponds to the other. If the charge transitions produce a a random telegraph signal (i.e. a signal that jumps between two different values) and the noise is Gaussian [84], then the probability that the threshold detection method makes a measurement error is

$$\frac{1-\mathrm{erf}\left(\frac{\mathrm{SNR}_i}{\sqrt{2}}\right)}{2}=\frac{1-\mathrm{erf}\left(\sqrt{\frac{\mathrm{SNR}_p}{2}}\right)}{2};$$

thus $\mathrm{SNR_i}$ can be interpreted intuitively as the number of standard deviations beyond the mean that a measurement must be to result in error. Because this interpretation does not hold for $\mathrm{SNR_p}$, we exclusively report signal-to-noise ratios throughout this work as defined for $\mathrm{SNR_i}$. In terms of charge sensitivity, reflectometry style measurements and current-to-current amplification schemes are competive [69, 73–77], however there are secondary considerations that differentiate the two. The primary disadvantage of reflectometry style measurements is that these methods require additional electrical components that can be unreliable at cryogenic temperatures and are bulky (i.e. difficult to fit inside a dilution refrigerator). The primary disadvantage of cryogenic amplification is the need to expend power on a cold stage of an ultra-low temperature cryostat.

This chapter will provide a practical guide for implementing current-to-current amplification for fast charge detection of quantum dot qubits.

4.2 Different implementations of cryogenic amplifiers

Even when looking exclusively at schemes of current-to-current cryogenic amplification, there exists a wide diversity of approaches. Several questions present themselves in designing a

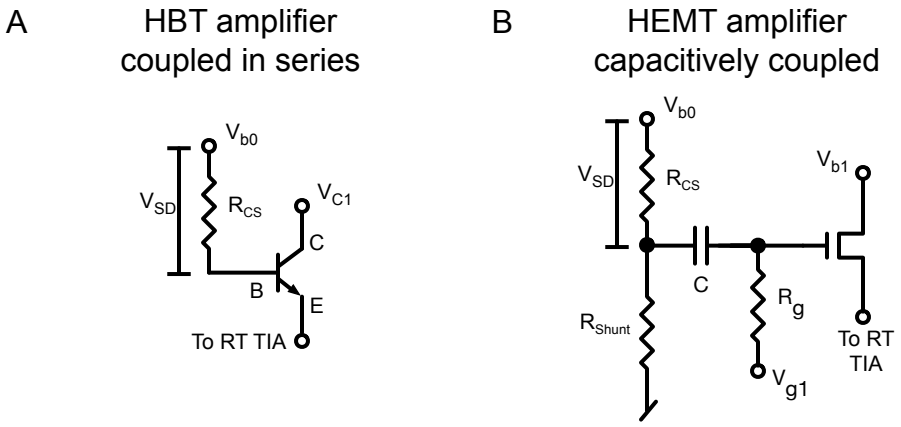

Figure 4.3: A charge sensor can either be placed in series with an electrical component for current-to-current amplification, or alternatively, capacitively coupled. The circuit diagram in panel A shows a configuration where the base of a HBT is placed in series with a charge sensor. The externally applied voltage bias V_{b0} is shared between the charge sensor and the HBT; thus the actual source-drain voltage across the charge sensor V_{SD} depends sensitively on the non-linear electrical properties of the HBT. The circuit diagram in panel B shows a configuration where a charge sensor is capacitively coupled to the gate of a HEMT; the current passing through the charge sensor in this configuration does not pass through the HEMT, but rather passes through a shunt resistor (R_{Shunt}). While the source-drain bias across the charge sensor (V_{SD}) in this configuration is less than the externally applied voltage bias V_{b0}, the linear behavior of the shunt resistor makes the difference more reliable. An offset voltage (V_{g1}) can be applied to the gate of the HEMT using the resistor R_g.

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cryogenic current-to-current amplifier.

First, what components can be used to provide amplification? Most commercially available electrical components are rated for -80° C, at best. One approach is to fabricate a HEMT along with the sample to be measured, thereby bypassing the need to find a reliable commercial electronic component [72]; yet this approach can add additional complexity into an already difficult fabrication process. Both HBTs (heterojunction bipolar transistors) [69,88,89] and HEMTs (high electron mobility transistors) [71,73] have been identified over the years as functioning at low temperatures. This distinction between HEMT and HBT component choice forms the first primary classification of approaches to cryogenic amplification.

Second, will the charge sensor be placed in series with the electrical component or, alter-

natively, capacitively coupled? Figure 4.3 displays circuit diagrams for both arrangements. Placing the charge sensor in series with the base of an HBT, for example, may provide advantages in terms of low-power consumption and ultimate noise performance [69]; however, this configuration means that any source-drain bias applied external to the dilution refrigerator will be shared between the charge sensor and the electrical component. If that electrical component is an HBT, where the conductance between the base and emitter is a non-linear function of the applied bias, this can make it difficult to interpret the resulting signal: when the conductance of the charge sensor changes in response to a charge transition, the voltage division between the charge sensor and the HBT changes, thus changing the source-drain bias across the charge sensor. As an alternative to placing the charge sensor in series with the active electrical component, the charge sensor can be capacitively coupled to the amplifier using a shunt resistor and capacitor. In this configuration, the charge sensor is placed in series with a resistor, whose conductance is not a function of the applied bias; thus any change in the conductance of the charge sensor has only a moderate effect on the source-drain bias of the charge sensor.

Third, how many cryogenic amplification stages will be used? Some amplifier designs use multiple stages of amplification in order to affect the gain-vs.-power consumption scaling. Because the total power consumption of a capacitively-coupled amplifier scales additively with the number of stages, whereas gain scales multiplicatively, additional stages of amplification can reduce the total amount of power required to achieve a fixed gain. Yet the trick of adding additional stages of amplification is not always useful: each stage of amplification will both boost the signal and introduce noise. Adding an additional stage of amplification isn't worth it if the additional amplification stage introduces more noise than it eliminates.

Finally, where will each stage of the amplifier will be positioned within the cryostat? Figure 4.4 displays three different schemes for heat sinking a cryogenic amplifier. In a dilution refrigerator, the sample will be heat sunk to the mixing chamber; an amplifier could be positioned on the mixing chamber as well, but then any heat dissipated by the

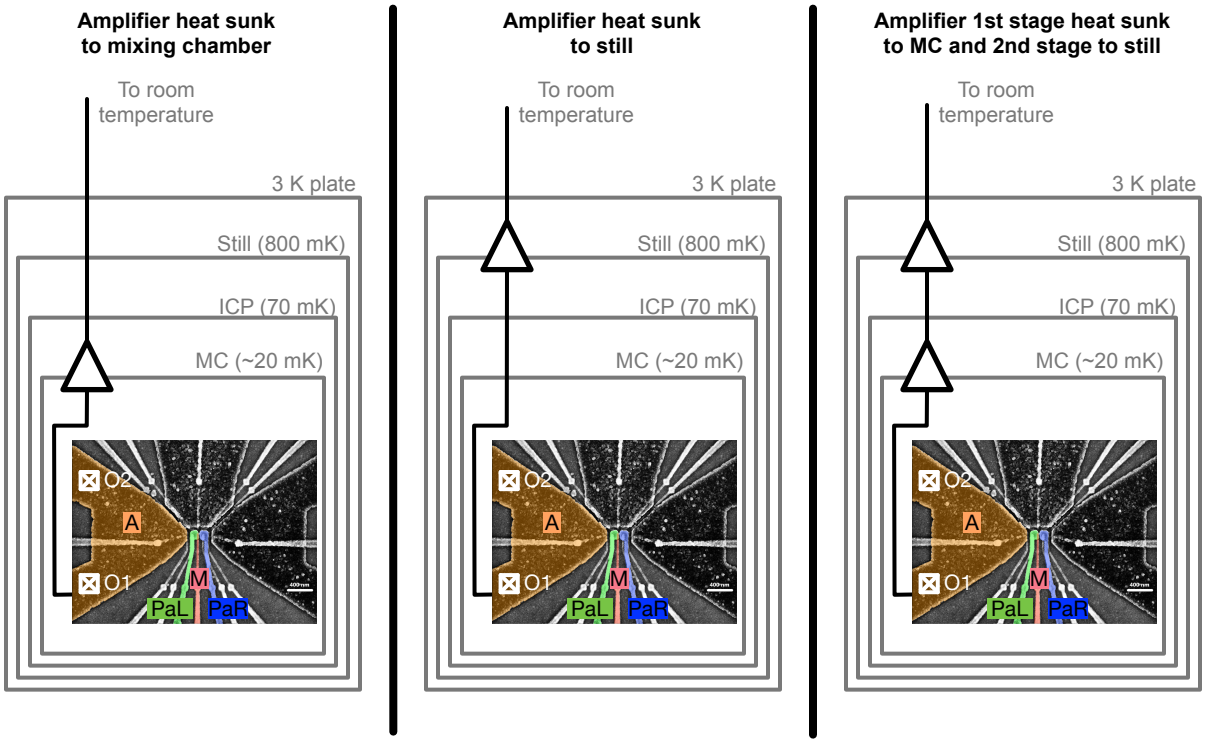

Figure 4.4: Panels A, B and C each depict a different heat sinking scheme that could be used with current-to-current amplification in a dilution refrigerator. Panel A depicts a cryogenic amplifier heat sunk to the mixing chamber along with the sample to be measured. The mixing chamber of a dilution refrigerator typically has 1-400 μW cooling power at 100 mK, but even 10 μW of power concentrated next to the sample could cause a local heating effect. Panel B depicts a cryogenic amplifier positioned on the still of the dilution refrigerator, which typically has $\sim$10 mW cooling power; the downside with this scheme is that the amplifier would inevitably be further away from the sample than the scheme in panel A, which could introduce additional noise and parasitic capacitance into the measurement. Panel C depicts a heat sinking scheme where two stages of the amplifier are split between different cold stages: one stage on the mixing chamber and one stage on the still. While this approach might reduce the amount of power dissipated right next to the sample, the parasitic capacitance between the amplifier stages would dramatically increase and could start to impact the rise time of the amplifier.

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amplifier would have to be absorbed by the mixing chamber. The mixing chamber of a dilution refrigerator typically has 1-400 μW cooling power at 100 mK, but even 10 μW of power concentrated next to the sample could cause a local heating effect. Alternatively, an amplifier could be positioned on the still of the dilution refrigerator, which typically has $\sim$10 mW cooling power. The downside to positioning an amplifier on the still of a dilution

refrigerator is that the amplifier would inevitably be further away from the sample than if it were positioned on the mixing chamber, and as the distance between sample and amplifier increases, so too does the parasitic capacitance between sample and amplifier. Additionally, as the amplifier gets further from the sample, more triboelectric noise will be introduced before amplification. The final downside to positioning the amplifier on the still of the dilution refrigerator is that the amplifier itself would be hotter; if the noise of the amplifier were temperature dependent (e.g. in the case of Johnson noise), a colder amplifier might result in lower noise. If the amplifier design includes multiple stages of amplification, it might be advantageous to position one stage right next to the sample, and then place the next stage on the still. While the approach of splitting cryogenic amplification over multiple locations potentially has the advantage of reducing the amount of power dissipated right next to the sample, the parasitic capacitance between the amplifier stages would dramatically increase and could start to impact the rise time of the amplifier.

Having outlined four broad classifications for contemporary approaches to current-to-current amplification, the focus will now be narrowed to one particular implementation of amplifier: a capacitively coupled two-stage cryogenic HEMT amplifier positioned on the mixing chamber of a dilution refrigerator, which was first proposed and implemented by Tracy, et al [73]. The next section will provide more details about the design of this particular amplifier.

4.3 Understanding the amplifier's circuit diagram

The two-stage cryogenic HEMT amplifier can be better understood by breaking the circuit diagram down into three capacitively coupled stages, which are depicted in Figure 4.5; the stages are labeled as the 0th stage, the 1st stage and the 2nd stage. The capacitive coupling between stages allows each stage to be tuned independently. The first and second stage of the amplifier each have two tuning parameters: a source-drain bias for that stage's HEMT

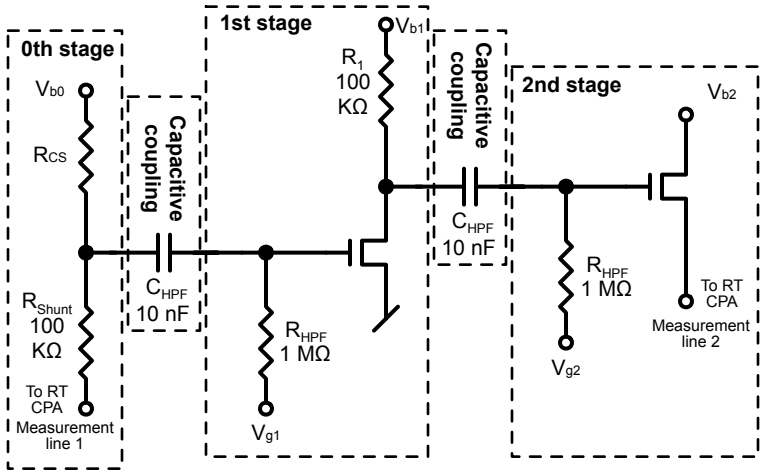

Figure 4.5: Circuit diagram for the two-stage cryogenic HEMT amplifier, with dashed boxes outlining the 0th, 1st, and 2nd stages of the amplifier, and the capacitive coupling between them. The capacitive coupling between stages allows each stage to be tuned independently. The first and second stage of the amplifier each have two tuning parameters: a source-drain bias for that stage's HEMT (V_{b1}, V_{b2}), and an offset gate voltage (V_{g1}, V_{g2}) used to make the current passing through the HEMT sensitive to changes in gate voltage. The current passing through the charge sensor can be measured without amplification using a room temperature transimpedance amplifier attached to measurement line 1; the amplified current can be simultaneously measured using a room temperature transimpedance amplifier attached to measurement line 2.

(V_{b1}, V_{b2}), and an offset gate voltage (V_{g1}, V_{g2}) used to make the HEMT sensitive to changes in gate voltage. The current passing through the charge sensor can be measured without amplification using a room temperature transimpedance amplifier attached to measurement line 1; the amplified current can be simultaneously measured using a room temperature transimpedance amplifier attached to measurement line 2.

The amplifier can be further understood (as shown in Figure 4.6) by breaking each stage down into basic circuit elements: high pass filters, low pass filters, and voltage dividers. The 0th stage is a voltage divider where V_{Div0} depends on R_{CS}. The voltage V_{Div0} can affect $V_{\mathrm{g,HEMT1}}$ by going through the first stage's high pass filter, thereby changing $R_{\mathrm{HEMT,1}}$. The first stage HEMT is part of another voltage divider whose division determines the voltage

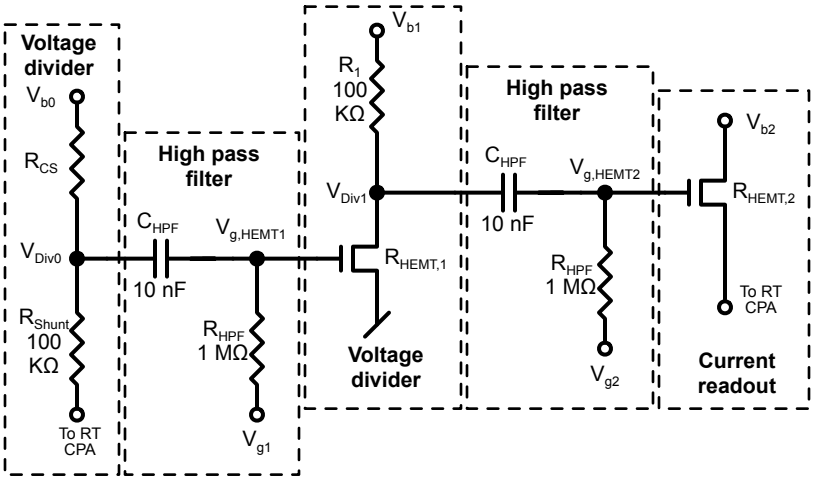

Figure 4.6: Circuit diagram for the two-stage cryogenic HEMT amplifier, with dashed boxes outlining the basic circuit elements that compose the amplifier. The 0th stage of the amplifier is a voltage divider where V_{Div0} depends on R_{CS}. V_{Div0} then passes through a high pass filter into the first stage of the amplifier, where V_{Div0} affects $V_{\mathrm{g,HEMT1}}$. The first stage HEMT is part of another voltage divider; thus sudden changes in V_{Div0} affect R_{HEMT1}, which affects V_{Div1}. The voltage at V_{Div1} passes through another high pass filter to affect $V_{\mathrm{g,HEMT2}}$, which in turn affects R_{HEMT2}. A bias is applied across the second stage HEMT, so changes in the resistance of the second stage HEMT cause a change in current, which is read out using a room temperature amplifier. In summary, sudden changes in R_{CS} create changes in the current read out of the second stage of the amplifier at room temperature.

V_{Div1}; thus sudden changes in V_{Div0} affect $R_{\mathrm{HEMT,1}}$, which affects V_{Div1}. The voltage at V_{Div1} can affect $V_{\mathrm{g,HEMT2}}$ by passing through the second stage's high pass filter, which in turn affects $R_{\mathrm{HEMT,2}}$. A bias is applied across the second stage HEMT, so changes in the resistance of the second stage HEMT cause a change in current, which is measured using a room temperature amplifier. In summary, sudden changes in R_{CS} create changes in the current measured through the second stage of the amplifier at room temperature.

The value of the 0th stage shunt resistor R_{Shunt} is one of the most important parameters in the amplifier; multiple considerations must be taken into account when deciding its value. First, the rise time of the amplifier is generally limited by $R_{||}C_{\mathrm{p}}$, where $R_{||}$ is the parallel resistance of R_{CS} and R_{Shunt}, so choosing a lower value for R_{Shunt} allows a faster rise time. Second, the value of the 0th stage shunt resistor affects how sensitive the amplifier is to changes in the resistance of the charge sensor. Finally, changes in the resistance of the

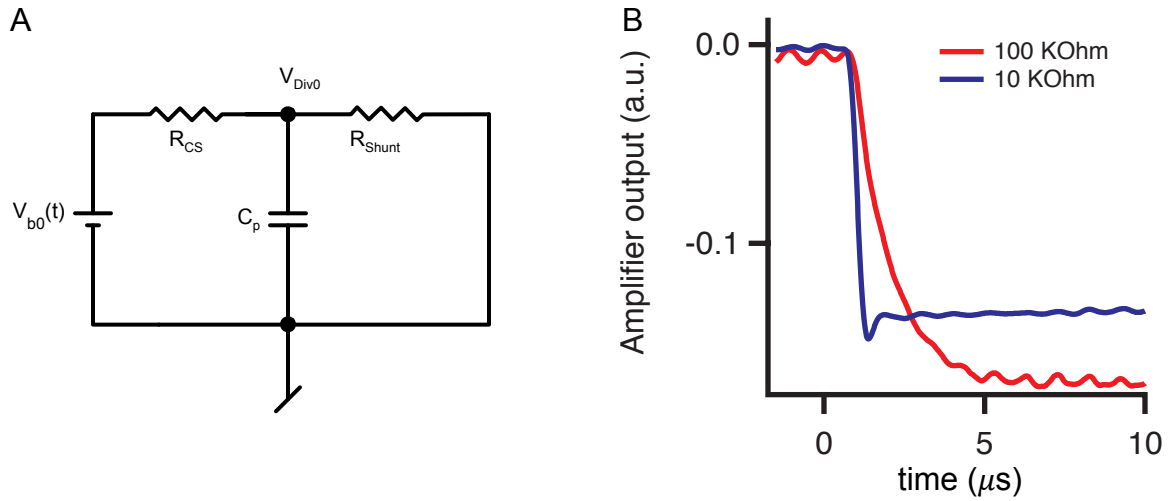

Figure 4.7: Experimental verification that the rise time of the cryogenic amplifier is limited by the first stage. Panel A provides a circuit diagram of the 0th stage of the amplifier, with parasitic capacitance included; analyzing this circuit shows that the time constant governing the rise of V_{Div0} is $R_{||}C_{\mathrm{p}}$, where $R_{||}$ is the parallel resistance of R_{CS} and R_{Shunt}. Panel B shows the rise time of a two-stage HEMT amplifier that was characterized with a 10 MOhm resistor in place of a charge sensor. The edge of a square voltage pulse was applied to V_{b0} (as labeled in Figure 4.5), resulting in a response at the output of the amplifier, as plotted above. This was repeated for two different values for R_{Shunt} (specifically 100 KOhms and 10 KOhms) with parasitic capacitance held fixed. The rise time for $R_{\mathrm{Shunt}} = 100$ KOhms was $\sim$2.5 μs, whereas the rise time for $R_{\mathrm{Shunt}} = 10$ KOhms was $\sim$250 ns. The linear scaling of the rise time with the input resistance of the amplifier suggests that the rise time for the whole amplifier was dominated by the rise time of the 0th stage.

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charge sensor will affect the source-drain bias across the charge sensor; however, this change is reduced with smaller R_{Shunt}. The value $R_{\mathrm{Shunt}} = 100$ KOhms was chosen because it is significantly smaller than the expected resistance of the charge sensor during operation, yet large enough for the amplifier to have good sensitivity.

Circuit analysis shows that the time constant governing the rise of V_{Div0} is $R_{||}C_{\mathrm{p}}$, where $R_{||}$ is the parallel resistance of R_{CS} and R_{Shunt}. Looking exclusively at the 0th stage of the amplifier (depicted in Figure 4.7), we can work out the differential equation governing V_{Div0}. While this analysis does make an approximation by looking only at the 0th stage of the amplifier, the actual rise time is very close to the approximate answer because the ignored parts of the circuit have relatively high resistance (the high pass filter includes a

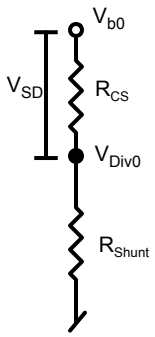

Figure 4.8: Circuit diagram for the 0th stage of the amplifier without parasitic capacitance, which can be used to understand why the gain of the amplifier scales with the value of R_{Shunt}. Circuit analysis indicates that the amplifier is most sensitive to changes in R_{CS} when $R_{\text{Shunt}} \approx R_{\text{CS}}$, and that gain of the amplifier increases with increasing R_{Shunt} as long as $R_{\text{Shunt}} < R_{\text{CS}}$.

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1 MOhm resistor, which is much larger than R_{Shunt}=100 KOhms; and the HEMT should have ∼1 GOhm isolation from the gate to source or drain) and thus have little effect on the voltage division determining V_{Div0}. The differential equation governing V_{Div0} is as follows:

$$\dot{V}_{\text{Div0}} = \frac{V_{b0}(t)}{R_{\text{CS}} C_p} - \frac{V_{\text{Div0}}}{R_{||} C_p}.$$

This differential equation suggests that the voltage V_{Div0} undergoes an exponential decay towards its equilibrium voltage with time constant $R_{||}C_p$ whenever $V_{\text{b0}}(t)$ is constant in time. This is an important result because the rise time for the whole amplifier is typically limited by the rise time of the 0th stage (verified experimentally in Figure 4.7). However, if changes were made to the amplifier design, such as splitting the two amplification stages between the mixing chamber and the still, it is possible that other parts of the amplifier circuit could begin to limit the rise time.

While the rise time of the amplifier decreases with smaller values for R_{Shunt}, so too does the total gain of the amplifier (assuming that $R_{\text{Shunt}} < R_{\text{CS}}$). Figure 4.8 displays the 0th stage of the amplifier without parasitic capacitance, which can be used to understand why the gain of the amplifier is affected by the value of R_{Shunt}. As described earlier, the amplifier

registers changes in the voltage on the first stage HEMT of the amplifier, and the output of the amplifier is proportional to these changes. The voltage between the charge sensor and the shunt resistor is

$$V_{\mathrm{Div0}} = V_{\mathrm{b0}} \frac{R_{\mathrm{Shunt}}}{R_{\mathrm{Shunt}} + R_{\mathrm{CS}}},$$

whose value is sensitive to changes in R_{CS}, under the assumption that R_{CS} is not much smaller than R_{Shunt}. The partial derivative

$$\frac{\partial V_{\mathrm{Div0}}}{\partial R_{\mathrm{CS}}} = -V_{\mathrm{b0}} \frac{R_{\mathrm{Shunt}}}{(R_{\mathrm{Shunt}} + R_{\mathrm{CS}})^2},$$

represents how sensitive the amplifier is to changes in R_{CS}, and its absolute value is maximized with respect to R_{Shunt} when

$$\begin{aligned} 0 &= \frac{\partial}{\partial R_{\mathrm{Shunt}}} \frac{\partial V_{\mathrm{Div0}}}{\partial R_{\mathrm{CS}}} \\ &= V_{\mathrm{b0}} \frac{R_{\mathrm{Shunt}}^2 - R_{\mathrm{CS}}^2}{(R_{\mathrm{Shunt}} + R_{\mathrm{CS}})^4} \\ &\implies R_{\mathrm{Shunt}} = R_{\mathrm{CS}}. \end{aligned}$$

In other words, the amplifier is most sensitive when $R_{\mathrm{Shunt}} \approx R_{\mathrm{CS}}$, and the sensitivity of the amplifier increases with increasing R_{Shunt} as long as $R_{\mathrm{Shunt}} < R_{\mathrm{CS}}$.

We can also calculate the amount by which the bias across the charge sensor changes with fluctuations in R_{CS}, as a function of R_{Shunt}. The equilibrium bias across the charge sensor is

$$V_{\mathrm{SD}} = V_{\mathrm{b0}} \frac{R_{\mathrm{CS}}}{R_{\mathrm{Shunt}} + R_{\mathrm{CS}}}.$$

For small changes in R_{CS}, changes in V_{SD} are proportional to

$$\frac{\partial V_{\mathrm{SD}}}{\partial R_{\mathrm{CS}}} = V_{\mathrm{b0}} \frac{R_{\mathrm{Shunt}}}{(R_{\mathrm{Shunt}} + R_{\mathrm{CS}})^2},$$

whose value is minimized when R_{Shunt} is small (again assuming that $R_{\mathrm{Shunt}} < R_{\mathrm{CS}}$).

Name	Filtering	Frequency Range	Cabling
Low frequency manipulation and readout "DC" lines	3x copper-powder boxes 2-stage RC filter (3dB = ∼150 KHz)	DC - 50 KHz	cryogenic loom
HF readout	3x 80 MHz LPFs (VLF-80+)	DC - 80 MHz	coaxial cable
RF manipulation	23 dB attenuation bias tee	5 KHz - ∼20 GHz	coaxial cable

Table 4.1: Details about the filtering used to integrate a quantum dot sample and a cryogenic amplifier into a dilution refrigerator. Electrical filtering helps to reduce radiative heating of the quantum dot sample when it is attached to the mixing chamber of the dilution refrigerator.

4.4 Integration of a cryogenic amplifier into dilution refrigerator wiring

Electrical lines passing into a dilution refrigerator must be heat sunk and filtered in order for the sample being measured to achieve an appropriate temperature. This section will address how a quantum dot sample and a cryogenic amplifier can be integrated into a dilution refrigerator with the appropriate filtering. In particular, this section will outline three tiers of electrical filtering (each with different functionality) that were used with the two-stage cryogenic HEMT amplifier to measure a quantum dot sample in a dilution refrigerator; the three tiers are summarized in Table 4.1. The first tier is low frequency filtering (<50 KHz), which can be used for low frequency manipulation and readout. The second tier is high frequency readout (<80 MHz), which was only used to measure the current passing through the second stage of the cryogenic amplifier. The final tier is for RF manipulation (5 KHz - ∼20 GHz), which was only used to manipulate the voltage on gates in the quantum dot sample.

The low frequency readout and manipulation lines are advantageous because they use space efficiently and, due to heavy filtering, have little impact on the temperature of the sample to be measured. In this filtering tier, cryogenic loom carries a voltage from room

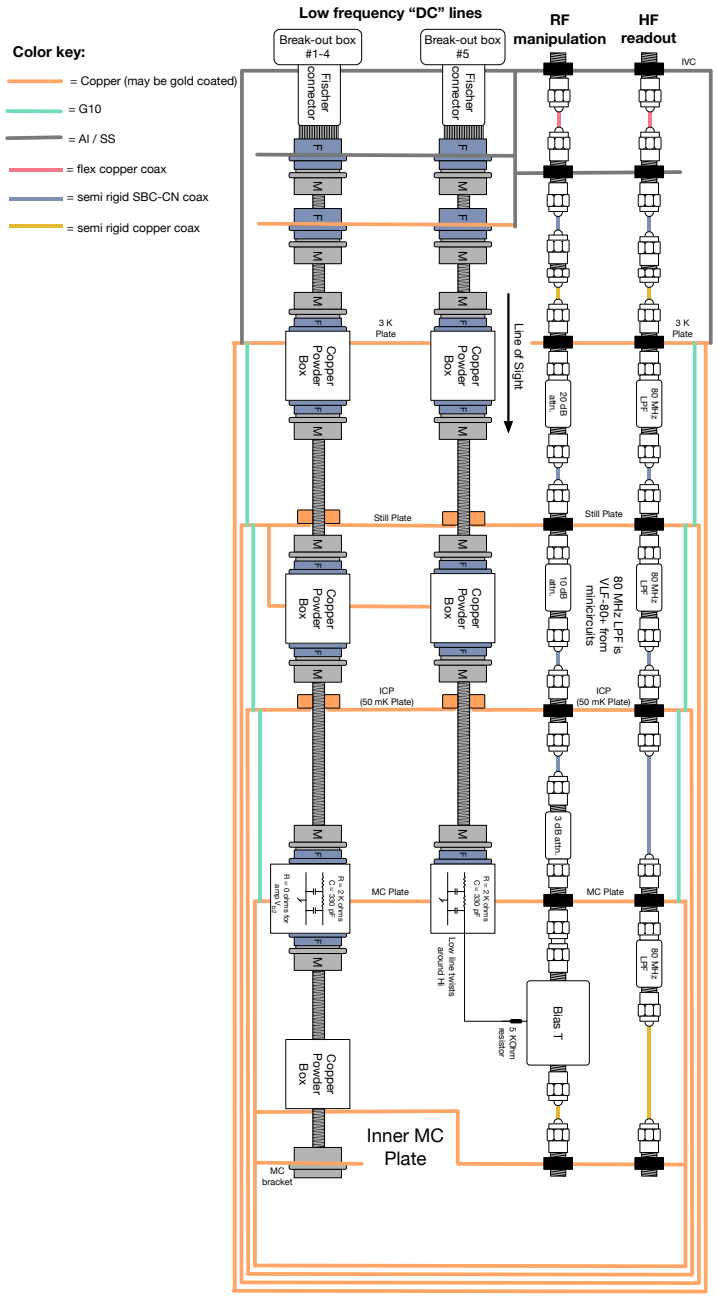

Figure 4.9: Schematic diagram of three types of electrical filtering for use in a dilution refrigerator: low frequency, RF manipulation, and HF readout. More details can be found in the text.

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temperature down to the mixing chamber of the dilution refrigerator; the loom passes through copper powder boxes on the 3K, still and mixing chamber cold stages of the dilution refrigerator. The voltage also passes through a two-stage RC filter on the mixing chamber, with

a cutoff frequency of ∼150 KHz. The downside to these low frequency lines is that they can't be used for manipulation or measurement above ∼50 KHz. Two things prevent these lines from being useful at higher frequencies: first, the lines are purposely filtered above a frequency of ∼150 KHz and additional capacitance introduced by the copper-powder boxes further limits the bandwidth; second, these lines are not well shielded from each other, such that significant cross-talk could develop between the lines at frequencies above ∼50 KHz.

The cryogenic amplifier is designed to have a much higher bandwidth than is compatible with cryogenic loom; thus high frequency measurement lines are used to measure the current coming out of the cryogenic amplifier's second stage. The high frequency measurement lines make several improvements over the low frequency lines: coaxial cable shields the current on its way to room temperature and prevents cross talk between signal lines. Additionally, the two-stage RC filters and copper-powder boxes are replaced with three 80 MHz low pass filters that are heat sunk at the 3K, still, and mixing chamber stages of the dilution refrigerator. These low pass filters are less resistive than the two-stage RC filters, which is important for two reasons: first, excess resistance in series with second stage HEMT reduces the amount by which the current passing through the second stage HEMT changes as a function of the second stage HEMT's resistance. Second, the same current passing through excess resistance uses more power; thus, having excess resistance in series with the second stage HEMT can cause unnecessary heating.

The final tier of electrical filtering is useful for RF manipulation of quantum dot gate voltages. Coaxial cable passes from room temperature to a bias tee on the mixing chamber of the dilution refrigerator, where it is added to a voltage coming from a low-frequency line; the summed voltage passes to a gate on the quantum dot sample. The bias T introduces a 5 KHz high pass filter to the RF manipulation line, and the coaxial cable introduces a frequency dependent attenuation that limits the manipulation bandwidth to ∼20 GHz. Additional attenuators are added to the coaxial cable (10 dB on the 3K plate, 10 dB on the still, and 3dB on the mixing chamber) in order to reduce radiative heating of the sample;

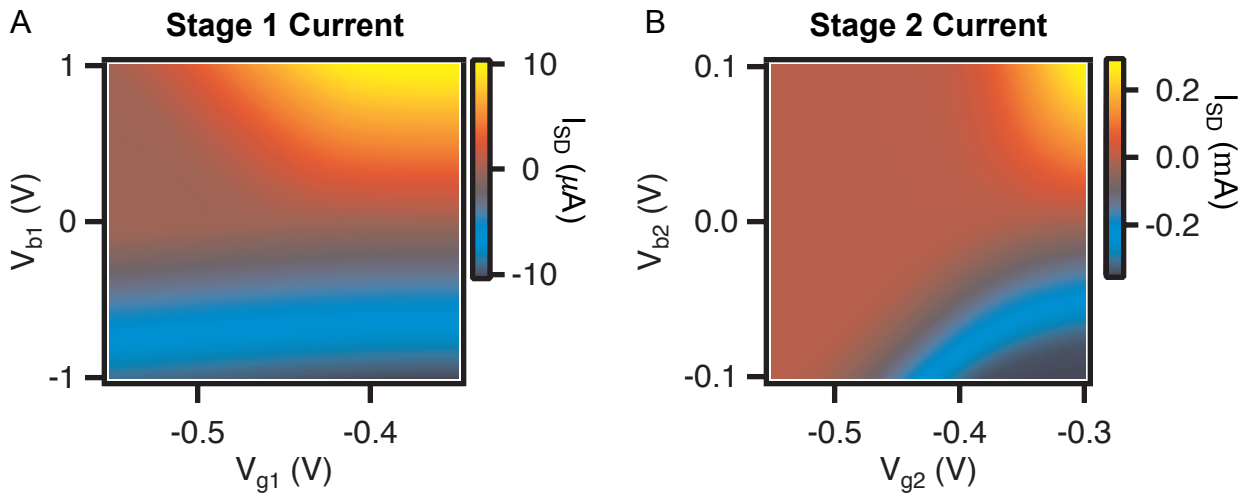

Figure 4.10: Independent characterization of each stage of the cryogenic amplifier at ∼7 K. The current passing through each stage was measured using a Keithley 2400 sourcemeter as a function of the offset gate voltage (V_{g1} and V_{g2}) and source drain bias (V_{b1} and V_{b2}) applied to each stage.

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the attenuators also help to heat sink the coaxial cable.

4.5 Operation of the cryogenic amplifier

Once the cryogenic amplifier has been properly loaded into a dilution refrigerator with a sample attached, it still needs to be tuned in order to work well. Fortunately, tuning the cryogenic amplifier is not nearly as involved a process as is tuning a quantum dot. Setting up the cryogenic amplifier to provide useful increases in bandwidth can take less than an hour, though optimization of the amplifier will take longer.

Each stage of the cryogenic amplifier should be characterized independently before the amplifier is used to make measurements of its attached sample. A Keithley 2400 sourcemeter allows the current passing through each stage of the amplifier to be measured at the same time as the applied voltage. Applying a negative voltage to the gate of each HEMT will "pinch off" the current passing through that HEMT, as seen in Figure 4.10. As an initial guess, the amplifier will have the highest gain when each of its HEMTs is half-way pinched

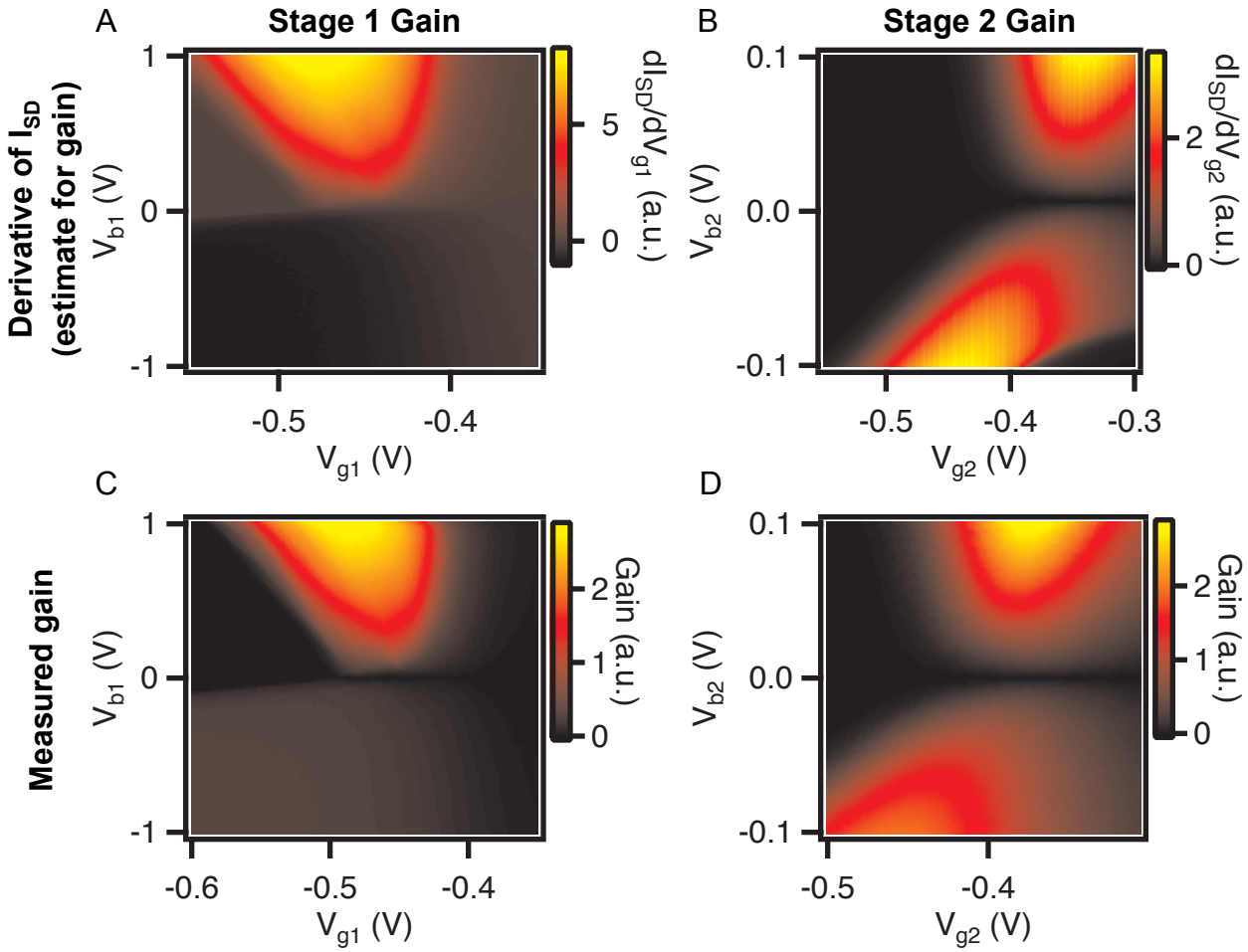

Figure 4.11: Gain of the cryogenic amplifier as a function of each stage's tuning parameters, measured at ∼7 K. The total gain for the amplifier is estimated in panels A and B using the derivative of the current displayed in Figure 4.10 with respect to the gate voltage. The gain of the amplifier was measured directly in panels C and D by comparing the current observed at the output of the amplifier with a fixed current signal induced on the sample.

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off; a slightly better guess is to tune the amplifier to where the absolute value of the derivative of the current passing through each stage of the amplifier with respect to the gate voltage is maximized, as is shown in Figure 4.11. While there are slight variations among different HEMTs, looking at past data can also give provide an initial guess for where the amplifier settings should be set. These measurements should not be taken when the amplifier is at room temperature, as the pinchoff characteristics of the HEMTs change significantly between room temperature and cryogenic temperatures.

Once initial characterization of the amplifier has occured, any Keithley 2400 sourcemeters should be removed from the amplifier circuit and replaced with low-noise voltage sources, such as a SIM 928 module from SRS. Current passing through the second stage of the amplifier should be measured using a room temperature transimpedance amplifier attached to measurement line 2; the chasis ground of this amplifier should be connected to measurement ground, and its output voltage should pass through a differential isolating amplifier (such as the SR560 from SRS) in order to maintain the experiment's star-ground. The output of the isolating amplifier can be attached to either a lockin or oscilloscope as appropriate. The bias applied to the first and second stage of the amplifier can also be filtered to further reduce noise, with the caveat that the output impedance of the filter must be significantly less than the input impedance for that stage of the amplifier. For example, when setup properly the total resistance of the first stage of the amplifier is $\sim$200 KOhms; thus the output impedance of any filter used on V_{b1} should be significantly less than that ($\leq$ 2 KOhms recommended). The resistance of the second stage of the amplifier is $\sim$ 2 KOhms, when properly set up, so any filter applied to V_{b2} should have a very low output impedance ($\leq$100 Ohms recommended).

After making initial guesses for the tuning of the cryogenic amplifier and setting up the amplifier as such, it should be ready for measurement. However, once a signal originating from the quantum dot sample is observed with the cryogenic amplifier, the gain should be calibrated. The best way to calibrate the gain of the amplifier is to simultaneously look at the amplified and unamplified current passing through the sample. The unamplified current can be measured with measurement line 1 using a room temperature transimpedance amplifier with a known gain; the amplified current can be simultaneously measured with measurement line 2. The ratio of the amplified current to the unamplified current gives the gain of the cryogenic amplifier; however, this calculation assumes that both measurements observe the same current. To ensure that this calibration of the gain is valid, a current signal should be generated at a frequency that can be measured without attenuation both with and without

the cryogenic amplifier. This means that the commonly observed current must be above the cut-off frequency of the cryogenic amplifier's high pass filters, but also below the high pass cutoff for the unamplified current. The next section describes how to generate this current signal using a lockin amplifier.

After determining the gain of the cryogenic amplifier for a single tuning, the cryogenic amplifier should be retuned to maximize the actual measured gain, rather than the estimated gain (nevertheless, as seen in Figure 4.11, the gain estimated from the derivative of the pinchoff curves is a good guide). By measuring a fixed current signal and varying the parameters of each stage of the amplifier, changes in the gain of the amplifier (relative to the gain established previously) can be measured by observing changes in the output signal of the amplifier. While the performance of the cryogenic amplifier is not always best where the gain is maximized, it is a good place to start. To fully optimize the noise performance of the cryogenic amplifier, one should measure both the gain of the amplifier as a function of the tuning parameters, and the noise at the output of the amplifier. Dividing the noise at the output of the amplifier by the gain of the amplifier gives the noise referred-to-input, which is ultimately the most important measure of the amplifier's performance.

4.6 Common measurements made using cryogenic amplifier

There are two big differences between measurements made with and without the cryogenic amplifier: first, the output of the cryogenic amplifier is capacitively coupled to the input (Figure 4.6 highlights the 16 Hz high pass filters), which means that the cryogenic amplifier is only useful when it is measuring a current that changes in time. Second, buffered readout is necessary to take full advantage of the cryogenic amplifier's large bandwidth; without buffered readout, the time required to communicate between electrical instruments can significantly slow down the measurement process. This section will provide greater detail about

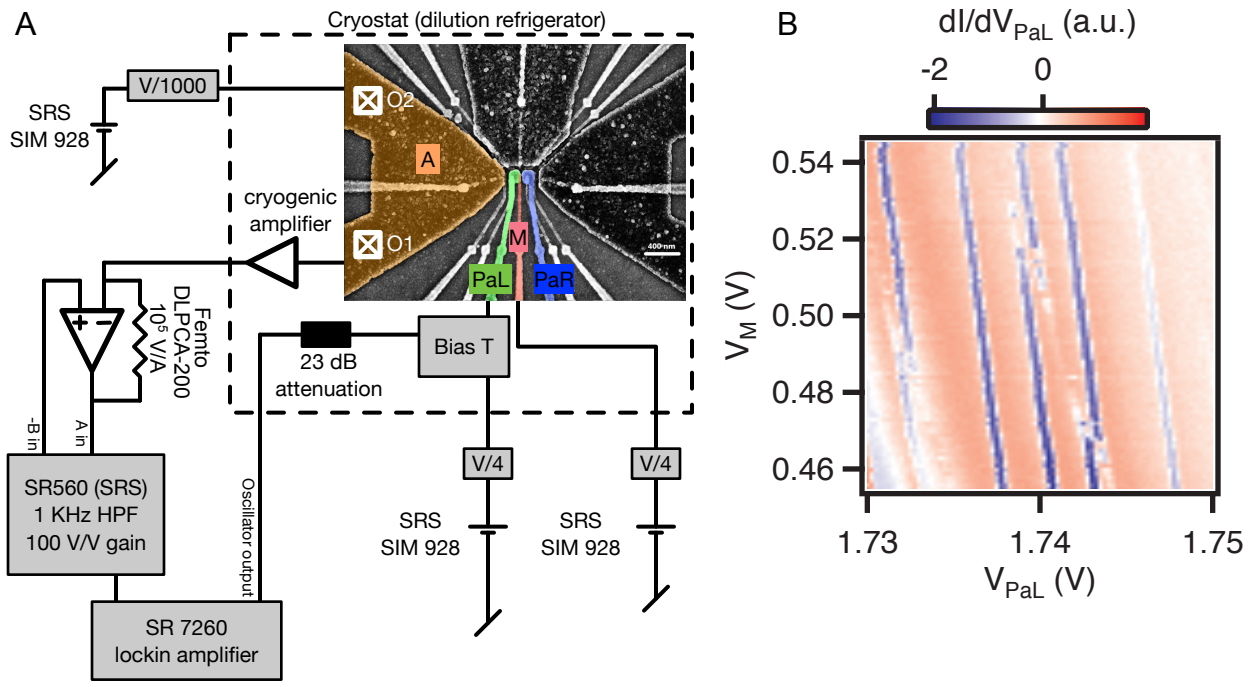

Figure 4.12: Charge transitions observed in a quantum dot sample, measured using a two-stage cryogenic HEMT amplifier in conjunction with a lockin amplifier. Panel A displays an SEM image of the quantum dot sample being measured and also sketchs the circuit used to measure the charge transitions. In this measurement, a quantum dot was formed under gate A and used to sense charge transitions in quantum dots that were formed under gate PaL and PaR. A source-drain bias was applied to ohmic contact O2 and the resulting current was measured through ohmic contact O1. The voltage on gate PaL was modulated at 150 KHz via an RF manipulation line (more details provided in Figure 4.9) using the oscillator of a lockin amplifier; this modulation created a current signal that was amplified by the cryogenic amplifier, and measured at room temperature using a transimpedance amplifier in conjunction with an isolation amplifier and the lockin amplifier. Panel B shows the quantum dot's response to modulation as a function of the voltage on gates PaL and M, which were varied by setting the voltage supplied by two Sim 928 voltage source modules from SRS.

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some of the different types of measurements that can be made with the cryogenic amplifier.

Using a lockin amplifier is a good way to confirm that the cryogenic amplifier is working right after initial calibration. The oscillator of the lockin can be used to modulate the voltage on a gate in the quantum dot sample or the source-drain bias across the charge sensor; modulation in this way creates an oscillatory current signal that bypasses the high pass filters of the amplifier. Attaching the output of the cryogenic amplifier (after the transimpedance

amplifier and isolating amplifier) to the input of the lockin allows measurement of this oscillatory current. As depicted in Figure 4.12, a charge stability diagram can be obtained using this measurement scheme by varying the voltage on gates in the quantum dot sample. This measurement scheme is advantageous because the frequency of modulation can be easily varied in this configuration, which is a useful tool for assessing the bandwidth of the cryogenic amplifier.

For a good signal, the modulation frequency should be above the frequency of the cryogenic amplifier's high pass filters, but should also be within the frequency range of the electrical line that is used to apply the modulation. For instance, if modulation is being applied via the low-frequency lines, the frequency should not go above a few 10's of KHz. Alternately, if the modulation is being applied via the RF-lines, the frequency should be above 5 KHz, and lower than the expected bandwidth of the amplifier ($\sim$500 KHz).

Buffered measurement, which involves timed manipulation and measurement of the sample, can significantly reduce the overall time required to take a measurement. Without buffered measurement, the communication time between instruments can limit the speed at which data is gathered. For instance, the measurement scheme shown in Figure 4.13 uses an AFG to manipulate the voltage on gate PaL in the depicted sample. The AFG is triggered by the oscilloscope and outputs a 200 cycle burst of 200 Hz triangle waves. The triangle waves are applied to gate PaL, creating a current signal that overcomes the cryogenic amplifier's high pass filters; the cryogenic amplifier boosts this current signal and it is measured at room temperature using a transimpedance amplifier in conjunction with an isolation amplifier and an oscilloscope, which records the output of the amplifier as a function of time. The data recorded by the oscilloscope is then binned according to the voltage on gate PaL and averaged to form a single line scan (only data from the downward sloping portion of the triangle wave was used for the plot in Figure 4.13). This process is repeated with different voltages applied to gate PaR, resulting in a two-dimensional stability diagram. In this configuration, each line of data in the two-dimensional plot can take less than a second to gather and

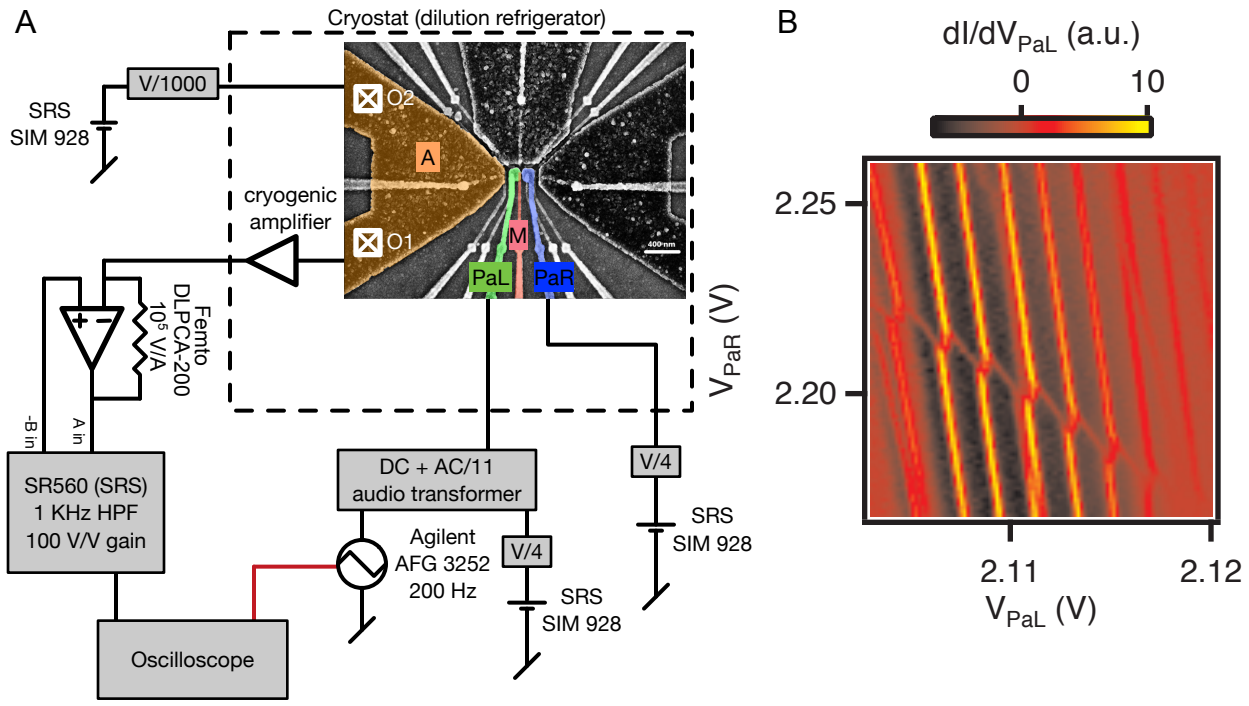

Figure 4.13: Charge transitions observed in a quantum dot sample, measured using buffered readout of a two-stage cryogenic HEMT amplifier. Panel A displays an SEM image of the quantum dot sample being measured and also sketchs the circuit used to measure charge transitions. For the measurement displayed in panel B, a quantum dot was formed under gate A and used to sense charge transitions in quantum dots that were formed under gate PaL and PaR. A source-drain bias was applied to O2 and the resulting current was measured through O1. The voltage on gate PaL was varied using a 200 cycle burst of 200 Hz triangle waves output by an AFG that was triggered by the oscilloscope; this variation of the voltage on gate PaL created a current signal that was amplified by the cryogenic amplifier, and measured at room temperature using a transimpedance amplifier in conjunction with an isolation amplifier. The output of the isolation amplifier was sent to an oscillocope where it was recorded as a function of time. The data collected by the oscilloscope was binned according to the voltage on gate PaL and averaged to form a single line scan. The process was repeated with different voltages applied to gate PaR, resulting in the two-dimensional stability diagram presented in Panel B. Each line of data in the two-dimensional plot took less than a second to gather and process; the entire plot was taken in a little over a minute.

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process; the entire plot might take a little over a minute.

A two-dimensional stability diagram can be taken even faster with the measurement scheme depicted in Figure 4.14. Two AFGs are used to manipulate the voltage on gates PaL and M. The AFG connected to gate PaL outputs 200 cycles of a 200 Hz triangle wave,

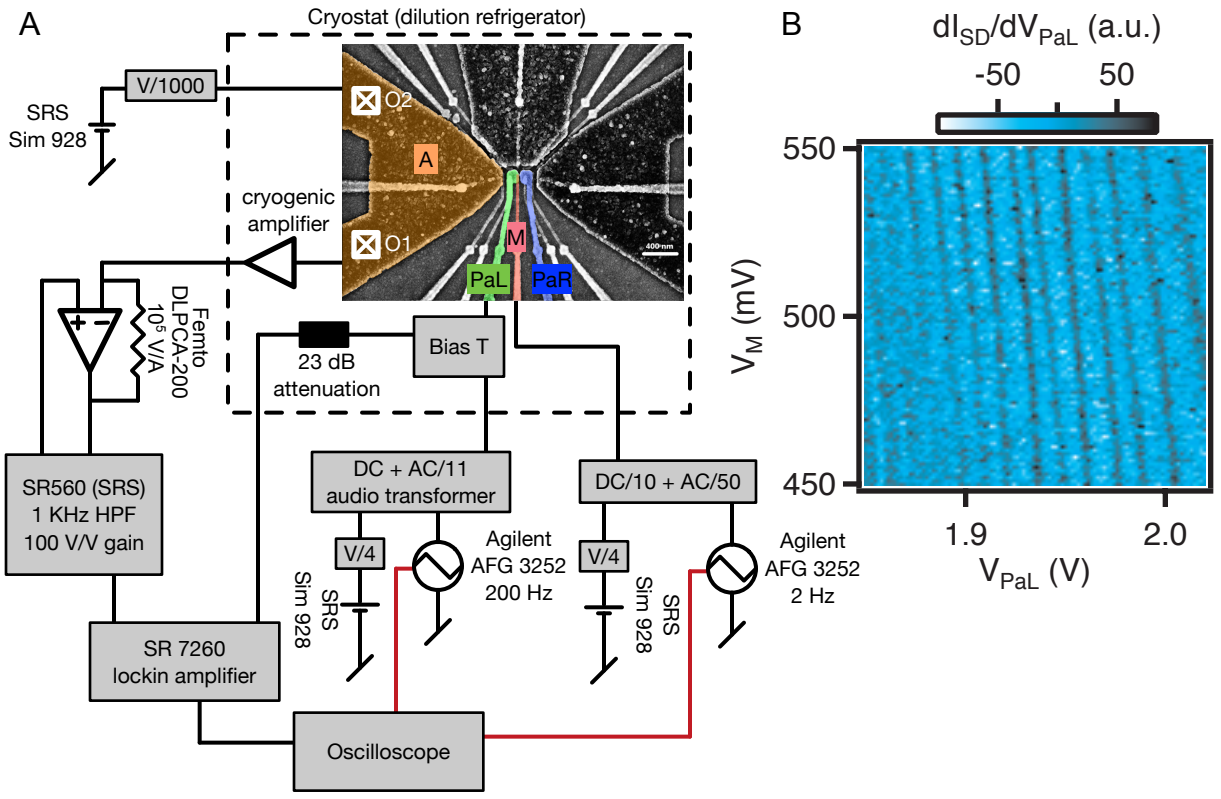

Figure 4.14: Charge transitions observed in a quantum dot sample, measured using buffered readout of a two-stage cryogenic HEMT amplifier. Panel A displays an SEM image of the quantum dot sample being measured and also sketchs the circuit used to measure charge transitions. For the measurement displayed in panel B, a quantum dot was formed under gate A and used to sense charge transitions in a quantum dot that was formed under gate PaL. A source-drain bias was applied to O2 and the resulting current was measured through O1. The voltage on gate PaL was modulated at 150 KHz via an RF manipulation line (more details provided in Figure 4.9) using the oscillator of a lockin amplifier; this modulation created a current signal that was amplified by the cryogenic amplifier, and measured at room temperature using a transimpedance amplifier in conjunction with an isolation amplifier and the lockin amplifier. The output of the lockin amplifier was sent to the oscillocope where it was recorded as a function of time. Panel B shows the quantum dot's response to modulation as a function of the voltage on gates PaL and M. The voltages on gates PaL and M were both varied using an AFG that was triggered by the oscilloscope; the AFG attached to gate PaL output a 200 cycle burst of 200 Hz triangle waves and the AFG attached to gate M outputs 1 cycle of a 1 Hz triangle wave. The data collected by the oscilloscope was binned according to the voltages on gates PaL and M. The data for the entire plot took about a second to measure and process.

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and the AFG connected to gate M outputs 1 cycle of a 1 Hz triangle wave. Both AFGs are triggered by the oscilloscope, and data from the output of the cryogenic amplifier is again

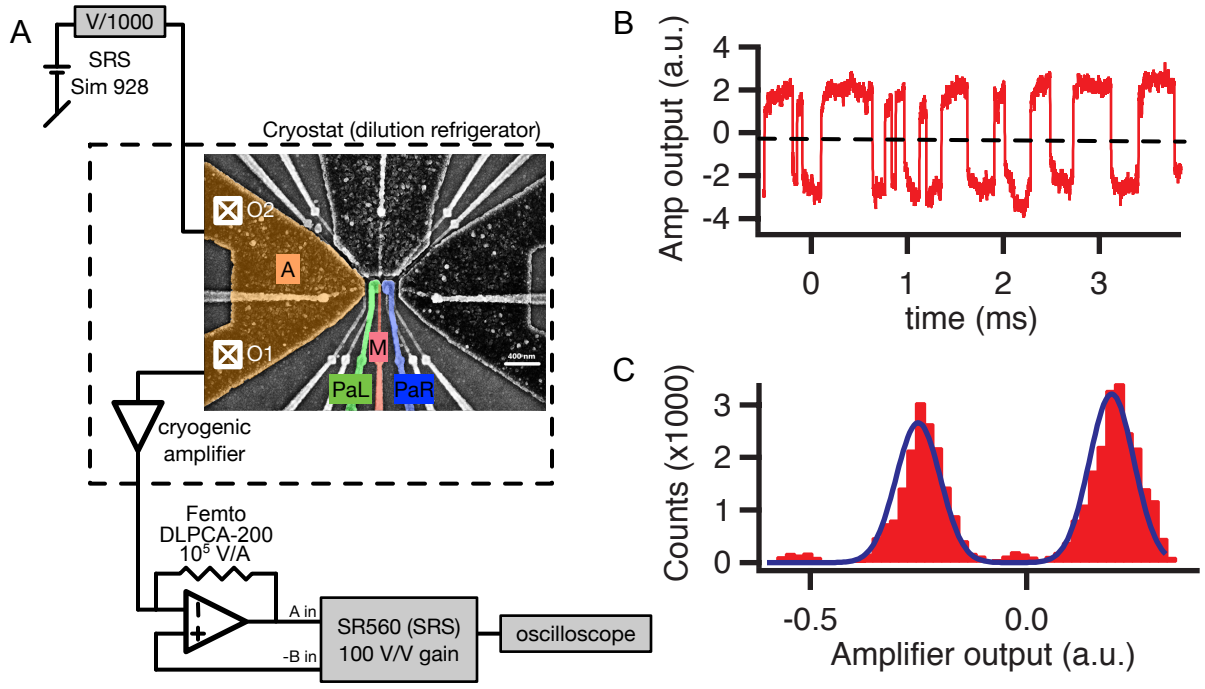

Figure 4.15: Single shot charge transitions observed in a quantum dot sample, measured using a two-stage cryogenic HEMT amplifier. Panel A displays an SEM image of the quantum dot sample being measured and also sketchs the circuit used to measure charge transitions. For the measurement displayed in panel B, a quantum dot was formed under gate A and used to sense charge transitions in a quantum dot that was formed under gate PaL. A source-drain bias was applied to O2 and the resulting current was measured through O1. The quantum dot under gate PaL was tuned such that its electro-chemical potential was aligned with the Fermi level of a nearby electron reservoir; in this configuration thermal fluctuations caused an electron to intermittently tunnel onto and off of the quantum dot. These charge transitions caused the current passing through the charge sensor to change, and these changes in current were amplified by the cryogenic amplifier and then measured at room temperature using a transimpedance amplifier in conjunction with an isolation amplifier and an oscilloscope. Panel B shows the output of the cryogenic amplifier as a function of time. The dashed line represents a threshold value to mark charge transitions: voltages below the line represent the N electron charge configuration and voltages above the line represent the N+1 electron configuration. Panel C shows a histogram of the data from panel B. The histogram is fit with a double gaussian, which allows a SNR of 4.35 to be extracted from this measurement. Given that the rise time of the amplifier in this configuration was $\sim$1 μs, the charge sensitivity is 230 $\mu\text{eV}/\sqrt{\text{Hz}}$.

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recorded as a function of time by the oscilloscope. The data from the oscilloscope is binned according to the voltages on gates PaL and M (only data from the downward portion of the triangle waves was used for the plot in Figure 4.14). The averaging time per point was 20 μs;

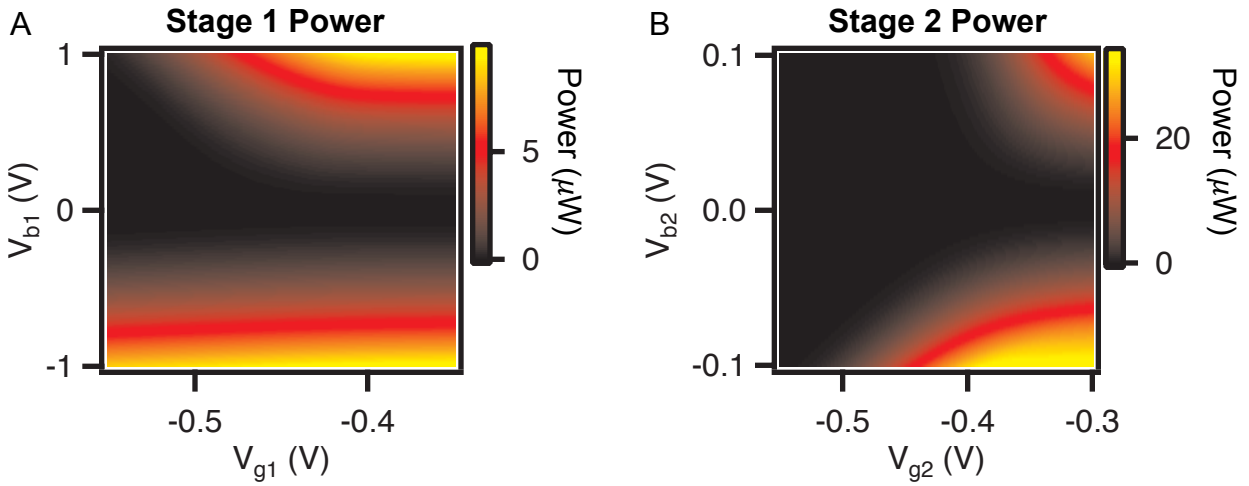

Figure 4.16: The power dissipation for each stage of the amplifier as a function of that stage's tuning, calculated (from the data in Figure 4.10) by multiplying the current passing through each HEMT by the applied voltage.

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it took roughly a second to measure and analyze the data for the whole plot.

The last measurement scheme highlighted in this section can be used to measure thermally-induced single-shot charge transitions; this measurement scheme is perhaps the simplest measurement to set up (in the sense that the sample need not be actively manipulated) but requires tuning the sample such that the electro-chemical potential of the quantum dot is lined up with the Fermi level in a nearby electron reservoir. In this configuration, thermal fluctuations will cause an electron to intermittently tunnel into and out of the quantum dot, resulting in a random telegraph signal in the charge sensor. The random telegraph signal bypasses the cryogenic amplifier's high pass filter, and can be measured at room temperature using an oscilloscope. Charge transitions can be identified either through a threshold method or by using wavelet edge detection [90].

4.7 The amplifier's effect on electron temperature

As shown in the previous section, current-to-current amplification is a powerful tool for increasing the signal-to-noise ratio of high bandwidth charge detection measurements. How-

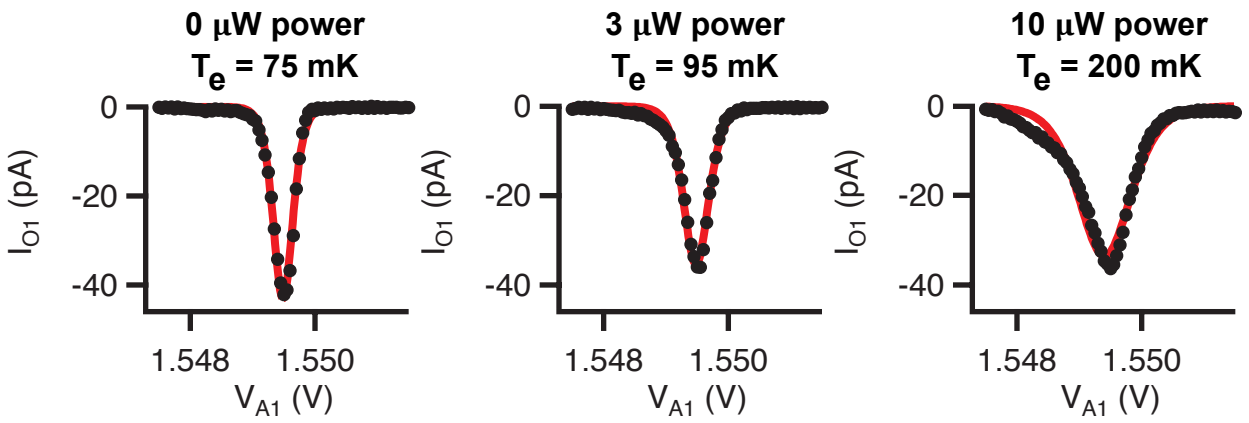

Figure 4.17: Data from Coulomb blockade thermometry performed in the quantum dot sample depicted in Figure 4.15, for various amounts of power dissipation in the attached cryogenic amplifier. The Coulomb blockade peaks were fit with the equation presented in the text to extract an electron temperature. The electron temperature was 75 mK while the cryogenic amplifier was off (i.e. dissipating 0 μW of power); the electron temperature was 95 mK with 3 μW of power dissipation; and the electron temperature was 200 mK with 9 μW of power dissipation.

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ever, the primary downside to this form of cryogenic amplification is that the amplifier dissipates heat (as shown in Figure 4.16), which could increase the electron temperature of a nearby quantum dot sample. Previous studies that attached a cryogenic amplifier to the mixing chamber of a dilution refrigerator observed electron temperatures in excess of 200 mK with $\sim$10 μW power dissipation [72, 73]. This section will provide details about the amplifier's heating effect when the sample and amplifier are heat sunk to the same printed circuit board (PCB). The next chapter provides details about improvements that can be made in the heat sinking of the amplifier in order to mitigate this heating effect, specifically moving the amplifier to a separate PCB and heat sinking it directly to the mixing chamber.

Figure 4.17 presents data from Coulomb blockade thermometry performed in the quantum dot sample depicted in Figure 4.15, for various amounts of power dissipation in the attached cryogenic amplifier. Before measurement, the quantum-dot sample was mounted on a two-layer PCB primarily composed of copper and Rogers 4350 dielectric, along with the two-stage cryogenic HEMT amplifier depicted in Figure 4.5. This PCB was then attached

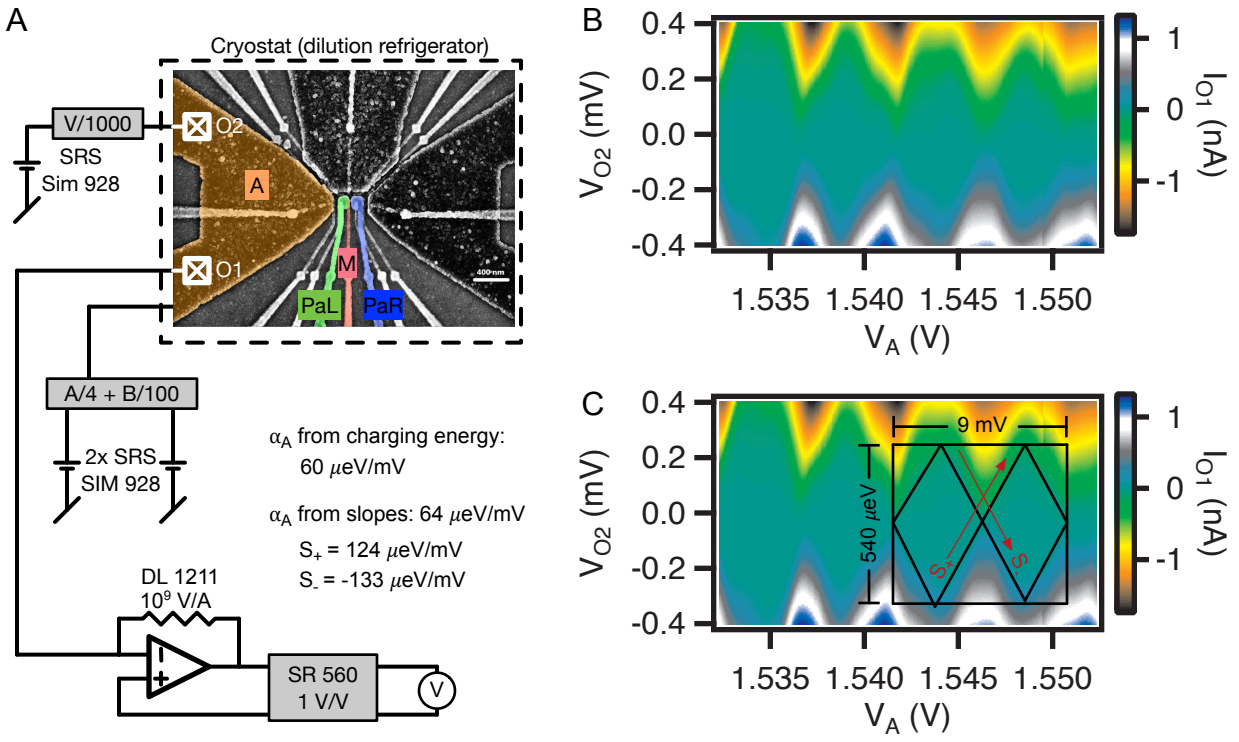

Figure 4.18: Extraction of gate lever arm using bias spectroscopy. Panel A presents the circuit diagram used for the bias spectroscopy measurement, along with an SEM image of the quantum dot sample. Both the source-drain bias V_{O2} applied to O2 and the voltage V_A applied to gate A were varied, and the current passing through the quantum dot was measured through O1. Panel B depicts the current as a function of V_{O2} and V_A. Panel C presents the same data as Panel B, but lines are drawn over the data to guide the eye. The lever arm α_A for gate A was extracted through two methods: first by observing that an extra electron is added to the quantum dot for every 4.5 mV change in V_A, and that the charging energy of the quantum dot was 270 μeV; this method gives $\alpha_A = 60$ μeV/mV. The second method examines the slopes associated with a single Coulomb blockade peak as a function of V_{O1} and V_A. The positive slope S_+ is 124 μeV/mV and the negative slope S_- is -133 μeV/mV, which gives $\alpha_A = 64$ μeV/mV.

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via a copper bracket to the mixing chamber of a CF-450 dilution refrigerator made by Leiden Cryogenics. The sample was cooled to the dilution refrigerator's base temperature of ~20 mK. A quantum dot was formed under gate A; a 15 μV bias was applied to O2 and the current passing through the quantum dot was measured through O1 using a room temperature transimpedance amplifier, as depicted in Figure 4.1. Coulomb blockade peaks were demonstrated by variation of the voltage on gate A, V_A. In accordance with reference [19], the electron temperature was extracted by fitting the current passing through the quantum

dot with the function

$$I_{\mathrm{QD}}(V_{\mathrm{A}}) = I \cdot \cosh^{-2}\left(\alpha_{\mathrm{A}} \frac{V_{\mathrm{A}} - V_0}{2k_{\mathrm{B}}T_e}\right),$$

where I is the size of the current peak, V_0 is the voltage on gate A at which the peak was centered, k_{B} is the Boltzmann constant, T_e is the electron temperature, and α_{A} is the lever arm for gate A. The formula presented above assumes that the current passing through the quantum dot is proportional to the quantum dot's conductance for a fixed source-drain bias; however, quantum dot samples sometimes exhibit a non-linear current-rectification effect near low-bias Coulomb blockade that can distort this relationship. In this case, the source-drain bias across the quantum dot is large enough that non-linear effects are minimal, though we cannot rule out the possibility that there is some small effect on the shape of the current peaks presented in Figure 4.17. A better method for extracting the electron temperature (employed in the next chapter) would measure the change in current passing through the quantum dot in response to a change in source-drain bias (this measurement could be performed by manually changing the source-drain bias and directly measuring the resultant change in current, or by modulating the source-drain bias and measuring the current response using a lockin amplifier). The value $\alpha_{\mathrm{A}} = 60$ μeV/mV was extracted by performing bias spectroscopy on the quantum dot (depicted in Figure 4.18), and was held fixed while fitting for the electron temperature. This same measurement was performed while the cryogenic amplifier was dissipating three different levels of power. The electron temperature was 75 mK when the cryogenic amplifier was off (i.e. dissipating 0 μW of power); the electron temperature was 95 mK with 3 μW of power dissipation; and the electron temperature was 200 mK with 9 μW of power dissipation. For context, four of this quantum dot sample's gates were attached to RF manipulation lines. Compared to other spin qubit implementations, 75 mK and 100 mK are relatively low electron temperatures. A wide range of electron temperatures have been reported for successful spin qubit implementations: 80 mK is reported in [36]; 100 mK is reported in [91]; 120 mK is reported in [32]; 130 mK is reported in [92]; 140 mK is reported in [37]; 150 mK is reported in [93]; 160 mK is reported

in [94]; 200 mK is reported in [95]; and 240 mK is reported in [73].

Chapter 5

Heat sinking of two-stage cryogenic HEMT amplifier

5.1 Abstract

Cryogenic amplification is a powerful tool for increasing the signal-to-noise ratio of high bandwidth charge detection. We provide an in-depth study of the heating effect that cryogenic amplifiers have on a nearby charge sensor when both are heat sunk to the mixing chamber of a dilution refrigerator. While the power consumption of a cryogenic amplifier can cause a significant increase in the electron temperature of a nearby quantum dot sample, we present evidence that these detrimental effects can be mitigated through an enhanced heat sinking technique, where the cryogenic amplifier is heat sunk to a printed circuit board (PCB) separate from the PCB of the sample.

5.2 Introduction

Type IV semiconductor spin qubits are potentially suitable for scalable quantum computing [9,11] and have made progress towards that goal in recent years [27–38,92,96]. While spin qubits have acheived long coherence and relaxation times by using the spin degree-of-freedom,

fast readout times are typically achieved by converting from spin to charge states [16,23–25]; thus charge detection is an important tool for state readout of semiconductor spin qubits. Finding a fast, reliable, and scalable method of charge detection with a good signal-to-noise ratio (SNR) remains a challenge for the field, given that samples must be placed within an ultra-low temperature cryostat (commonly a dilution refrigerator).

Charge sensors, such as single electron transistors (SETs) and quantum dots (QDs), can be capacitively coupled to the qubit and read out using a room temperature transimpedance amplifier (TIA), but the signal-to-noise ratio of such measurements tend to suffer at higher frequencies [69]. For instance, the DLPCA-200 transimpedance amplifier from Femto has a bandwidth of up to 500 KHz on the 10^4 V/A sensitivity setting, but has a minimum specification of 2.4 nA_{RMS} of input-referred noise with this setting. While the input-referred noise can be lowered by going to a higher current sensitivity with this amplifier, such a change would increase the input impedance of the amplifier, resulting in a smaller bandwidth. To achieve less than 50 pA_{RMS} input-referred noise with the DLPCA-200 from Femto, one would have to increase the sensitivity to 10^7 V/A, where the amplifier only has 50 KHz bandwidth. Other transimpedance amplifiers (such as the DL1211 from DL Instruments) are limited by a comparable trade-off between noise and bandwidth.

Better noise and bandwidth properties can be achieved by introducing cryogenic amplification between the charge sensor and room temperature electronics. Some approaches have placed cryogenic amplifiers at an intermediate cold stage of the dilution refrigerator, but this approach can be hampered by a large parasitic capacitance between the sample and amplifier [71]. One way to avoid the detrimental impact of parasitic capacitance is RF reflectometry where the charge sensor can be measured through its damping of a resonant circuit; yet while RF reflectometry mitigates the effects of parasitic capacitance between the resonant circuit and cryogenic amplification, successful measurement depends on the capacitance of the resonant circuit, which puts constraints on device packaging and sample parasitics [74–77, 85]. Other promising work has used a microwave cavity coupled to a

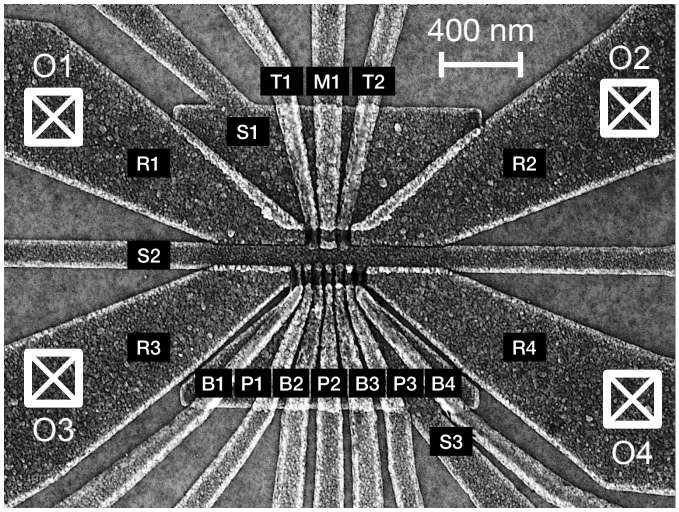

Figure 5.1: SEM image of a triple-quantum-dot device that was created by patterning overlapping aluminum gates on a Si/SiGe heterostructure; the device measured here had the same gate pattern. The design of the triple-quantum-dot device allows for three quantum dots on the bottom half of the device and one quantum dot on the top half of the device for charge sensing. The gates were designed to function in the following way: the four reservoir gates R1-4 allow electron reservoirs to be accumulated to the right and left of the active region of the device; the three screening gates S1-3 prevent electrons from accumulating in unwanted regions; the three paddle gates P1-3 accumulate quantum dots on the bottom half of the device; gate M allows a quantum dot to be accumulated on the top half of the device for charge sensing; and the six barrier gates T1-2 & B1-4 control the tunnel barriers between the quantum dots and the electron reservoirs. Four phosphorus doped ohmic contacts O1-4 allow electrical access to the electron reservoirs. The input of the cryogenic amplifier was attached to O2.

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quantum dot for charge sensing [81–83]. In either case, overcoming the detrimental effects of parasitic capacitance through RF measurement requires bulky microwave components that must be placed inside the tight confines of a dilution refrigerator.

Another way to overcome parasitic capacitance is to move cryogenic amplification closer to the sample being measured, heat sinking any amplifiers to the mixing chamber of the dilution refrigerator; previous attempts have shown promising increases in SNR using this technique [69, 72, 73]. The primary disadvantage of heat sinking an amplifier to the mixing chamber of a dilution refrigerator is that any heat dissipation from the amplifier has the potential to heat the sample being measured. While previous studies briefly considered the impact of the amplifier's power dissipation, observing electron temperatures in excess of 200

Heterostructure feature	Thickness
Relaxed $Si_{0.7}Ge_{0.3}$ buffer	170 nm
Strained Si well	9 nm
Relaxed $Si_{0.7}Ge_{0.3}$ spacer	40 nm
Si cap	1 nm

Table 5.1: Details about the Si/SiGe heterostructure used to fabricate the triple-quantum-dot device that was measured in this work.

mK with ∼10 μW power dissipation, they also called for greater investigation [72, 73].

Here we investigate a novel and enhanced method for heat sinking a cryogenic amplifier to the mixing chamber of a dilution refrigerator. Whereas previous work positioned the cryogenic amplifier on the same PCB as the sample to be measured [69, 72, 73], we place the cryogenic amplifier on a separate PCB from the sample; this separate amplifier PCB is then directly heat sunk to the mixing chamber, and only electrically connected to the sample's PCB via a short stainless steel coax. This enhanced heat sinking technique seeks to combine the advantages of the approach pursued by Vink, et al. [71] (placing amplification on the still), with the advantages of the approach pursued by Pettersson, et al. [72] and Tracy, et al. [73] (placing amplification on the same PCB as the sample): positioning the amplifier close to the sample allows for a small parasitic capacitance between sample and amplifier (6 pF in this case, compared to 50 pF in reference [71]); yet heat sinking the amplifier to its own PCB mitigates the heating associated with the amplifier's power consumption (as reported below, we observe an electron temperature of ∼150 mK with 10 μW power, whereas electron temperatures in excess of 200 mK were observed with similar power in references [72] and [73]).

5.3 Methods

A two-stage cryogenic HEMT amplifier was used to amplify the current passing through a quantum dot charge sensor in a triple-quantum-dot device; measurements were performed

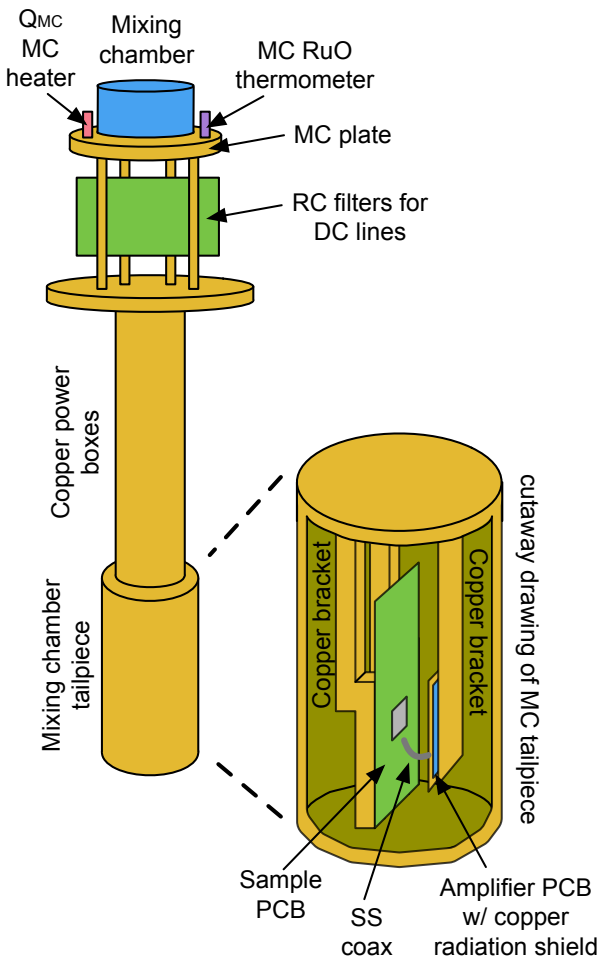

Figure 5.2: Schematic diagram of the enhanced heat-sinking technique used to isolate a triple-quantum-dot sample from a cryogenic amplifier when both are heat sunk to the mixing chamber of a dilution refrigerator. The triple-quantum-dot sample was mounted on a PCB which was attached to the mixing chamber of the dilution refrigerator via a copper bracket. The cryogenic amplifier was mounted on a second PCB that was attached to the mixing chamber via a separate copper bracket. A copper radiation shield was placed over the cryogenic amplifier to block black-body radiation that might pass between the amplifier and the triple-quantum-dot sample. The amplifier PCB and the sample PCB were electrically connected using a 2 cm length of flexible ultra-miniature stainless steel coax.

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in a Janis JDR-100 dilution refrigerator. The triple-quantum-dot device was fabricated by J. P. Dodson at the University of Wisconsin- Madison with overlapping aluminum gates [28, 54, 97] on a Si/SiGe heterostructure grown by Lisa Edge of HRL Laboratories, as shown in Figure 5.1. Details about the Si/SiGe heterostructure are listed in Table 5.1. After

a 5 nm Al_2O_3 gate oxide was deposited on top of the heterostructure using atomic layer deposition, three layers of self-oxidized Al gates were deposited by e-beam evaporation. The thickness of the three aluminum gate layers, moving away from the heterostructure, was 33 nm, 44 nm, and 55 nm respectively. The design of the triple-quantum-dot device allows for three quantum dots on the bottom half of the device and one quantum dot on the top half of the device for charge sensing. The gates were designed to function in the following way: the four reservoir gates R1-4 allow electron reservoirs to be accumulated to the right and left of the active region of the device; the three screening gates S1-3 prevent electrons from accumulating in unwanted regions; the three paddle gates P1-3 accumulate quantum dots on the bottom half of the device; gate M allows a quantum dot to be accumulated on the top half of the device for charge sensing; and the six barrier gates T1-2 & B1-4 control the tunnel barriers between the quantum dots and the electron reservoirs. Four phosphorus doped ohmic contacts O1-4 allow electrical access to the electron reservoirs. The input of the cryogenic amplifier was attached to O2.

The triple-quantum-dot sample was mounted on a two-layer PCB primarily composed of copper and Rogers 4350 dielectric; the sample PCB was then attached to the mixing chamber of the dilution refrigerator via a copper bracket, as depicted in Figure 5.2.

The cryogenic amplifier was mounted on a two-layer PCB primarily composed of copper and Rogers 4350 dielectric. The amplifier PCB was then attached to the mixing chamber of the dilution refrigerator via a copper bracket, as depicted in Figure 5.2. A thinner dielectric thickness (0.031 inches) was chosen for the amplifier PCB in order to reduce the thermal impedance between the amplifier components and the copper bracket to which it was attached. Apiezon N-grease was applied to the back of the amplifier PCB to further improve heat sinking to its copper bracket. Finally, a copper radiation shield was placed over the cryogenic amplifier to block black-body radiation that might pass between the amplifier and the triple-quantum-dot sample. A ruthenium oxide (RuO) thermometer was mounted on the amplifier PCB in a 4-probe configuration in order to monitor the temperature on the

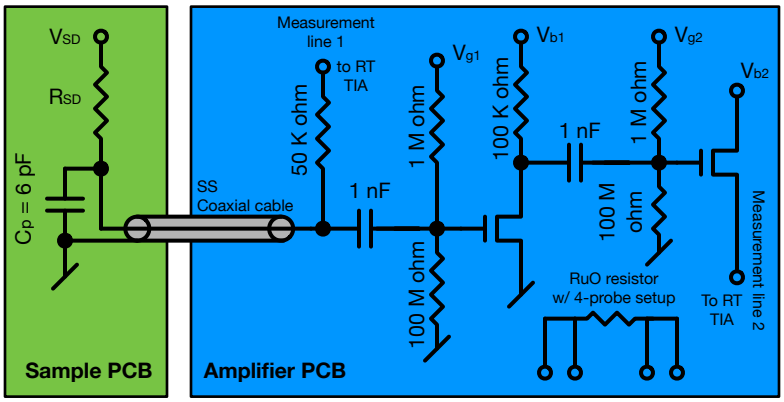

Figure 5.3: Circuit diagram for the two-stage cryogenic HEMT amplifier characterized in this paper. The most notable change from previous iterations of the two-stage HEMT amplifier [73] is that the input resistance of the amplifier was reduced by a factor of 2 in order to compensate for the parasitic capacitance introduced by the coaxial cable. While decreasing the input resistance of the amplifier allowed for a rise time of ∼650 ns, it also reduced the ultimate signal-to-noise ratio of which the amplifier was capable by roughly a factor of 2. A room temperature TIA attached to measurement line 1 can be used to measure the current passing through the charge sensor without cryogenic amplification. Simultaneously, a room temperature TIA attached to measurement line 2 can be used to measure the charge-sensing current after cryogenic amplification.

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amplifier PCB.

The amplifier PCB and the sample PCB were electrically connected using a 2 cm length of flexible ultra-miniature stainless steel coax produced by Lakeshore Cryotronics. The coax was chosen to be stainless steel for its high thermal impedance, though future work could use superconducting coax as an alternative.

Figure 5.3 depicts the circuit diagram for the amplifier that was used with the enhanced heat sinking technique. The most notable change from previous iterations of the two-stage HEMT amplifier [73] is that the input resistance of the amplifier was reduced by a factor of 2 in order to compensate for the parasitic capacitance introduced by the coaxial cable. While decreasing the input resistance of the amplifier allowed for a rise time of ∼650 ns, it also reduced the ultimate signal-to-noise ratio of which the amplifier was capable by roughly a factor of 2. As depicted in Figure 5.3, a room temperature TIA attached to measurement line 1 can be used to measure the current passing through the charge sensor without cryogenic

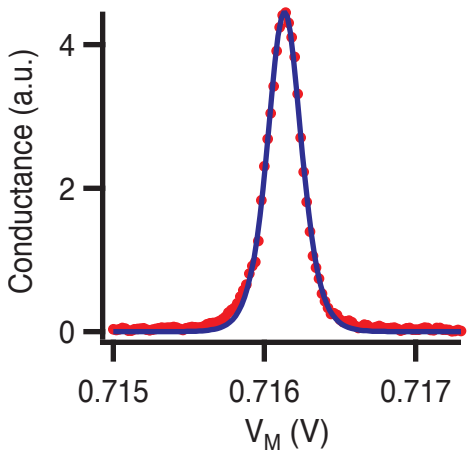

Figure 5.4: An example of a Coulomb blockade peak that was fit in order to extract the electron temperature in the triple-quantum-dot device. The conductance of a quantum dot formed under gate M was determined using a lockin measurement of the current with a 10 μV_{RMS} modulation of the source-drain bias at 87 Hz.; the width extracted from the fit was 0.148 mV, which corresponds to an electron temperature of ∼110 mK given the gate lever arm α_M=125 μeV/mV.

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amplification. Simultaneously, a room temperature TIA attached to measurement line 2 can be used to measure the charge-sensing current after cryogenic amplification.

At cryogenic temperatures, a quantum dot was formed under gate M of the triple-quantum-dot device. A bias voltage was applied to O1 and the current passing through the quantum dot was measured through O2. The conductance of the quantum dot was determined using a lockin measurement of the current with a 10 μV_{RMS} modulation of the source-drain bias at 87 Hz. Coulomb blockade peaks were demonstrated by variation of the voltage on gate M, V_M. The width of the Coulomb blockade peaks (defined below) was extracted by fitting the conductance with the function

$$G_{QD}(V_M) = G \cdot \cosh^{-2}\left(\frac{V_M - V_0}{W_e}\right),$$

where G is the size of the conductance peak, V_0 is the voltage on gate M at which the peak was centered, and W_e is the width of the peak. The width of the conductance peak, when defined as W_e, is approximately equal to 0.57 times the full-width-at-half-max of the

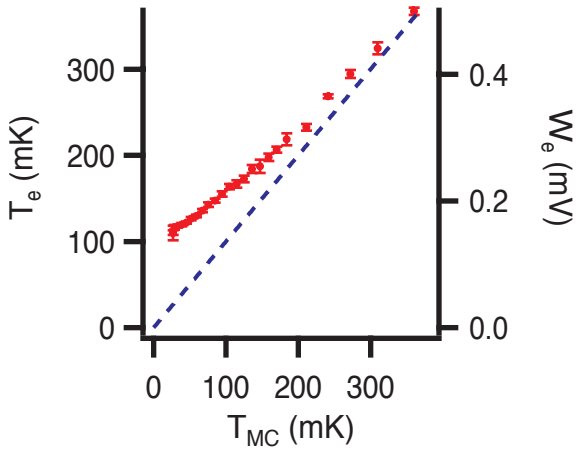

Figure 5.5: The results of Coulomb blockade thermometry, performed to measure the base electron temperature in the quantum dot sample. The red markers indicate the width of Coulomb blockade peaks (right axis), or alternatively the electron temperature (left axis), as a function of the equilibrium temperature of the mixing chamber. For T_{MC} >200 mK, the electron temperature in the triple-quantum-dot sample is very close to the temperature of the mixing chamber. However, as T_{MC} approaches the base temperature of ∼20 mK, T_e diverges from T_{MC} due to heating in the sample from external sources and imperfect heat sinking. The base electron temperature observed in the triple-quantum-dot sample is ∼100 mK. The blue dashed line in Figure 5.5 represents the electron temperature that would have been expected if the triple-quantum-dot were perfectly heat sunk, based on the gate lever arm α_{M}, extracted from bias spectroscopy.

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conductance peak, and is taken to be equal to $2k_{\mathrm{B}}T_e/\alpha_{\mathrm{M}}$ in accordance with reference [19], where k_{B} is the Boltzmann constant, T_e is the electron temperature, and α_{M} is the lever arm for gate M. The value $\alpha_{\mathrm{M}} = 125$ μeV/mV was extracted by performing bias spectroscopy on the quantum dot, which allowed the Coulomb blockade peak widths to be converted to an electron temperature. Figure 5.4 shows an example of a Coulomb blockade peak used to extract an electron temperature and its corresponding fit; the width extracted was 0.148 mV, which corresponds to an electron temperature of ∼110 mK.

Figure 5.5 shows the results of Coulomb blockade thermometry, which was performed to measure the base electron temperature in the quantum dot sample. The red markers indicate the width of Coulomb blockade peaks (right axis), or alternatively the electron temperature (left axis), as a function of the equilibrium temperature of the mixing chamber.

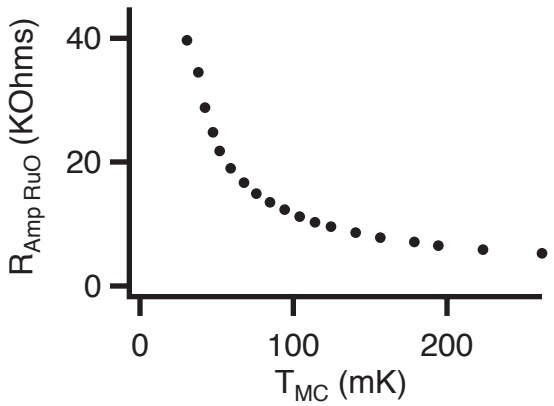

Figure 5.6: Calibration of the RuO thermometer that was heat sunk to the amplifier PCB; this thermometer needed calibration because it was subjected to thermally induced strain as part of being mounted on the amplifier PCB. All subsequent measurements of the RuO thermometer on the amplifier PCB rely on a linear interpolation of this data.

The equilibrium temperature of the mixing chamber was varied by heating a resistor heat sunk to the mixing chamber plate, and the equilibrium temperature was measured through a RuO thermometer heat sunk to the mixing chamber, as indicated in Figure 5.2. For $T_{\mathrm{MC}} >$ 200 mK, the electron temperature in the triple-quantum-dot sample is very close to the temperature of the mixing chamber. However, as T_{MC} approaches the base temperature of ∼20 mK, T_e diverges from T_{MC} due to heating in the sample from external sources and imperfect heat sinking. The base electron temperature observed in the triple-quantum-dot sample is ∼100 mK. The blue dashed line in Figure 5.5 represents the electron temperature that would have been expected if the triple-quantum-dot sample were perfectly heat sunk.

Figure 5.6 shows the temperature calibration of the ruthenium oxide thermometer that was heat sunk to the amplifier PCB; it was calibrated through variation of the equilibrium temperature of the MC in the same way as for Coulomb blockade thermometry. The RuO thermometer on the amplifier board needed calibration because it was subjected to thermally induced strain as part of being mounted on the amplifier PCB. All subsequent measurements of the RuO thermometer on the amplifier PCB rely on a linear interpolation of the calibration data presented in Figure 5.6.

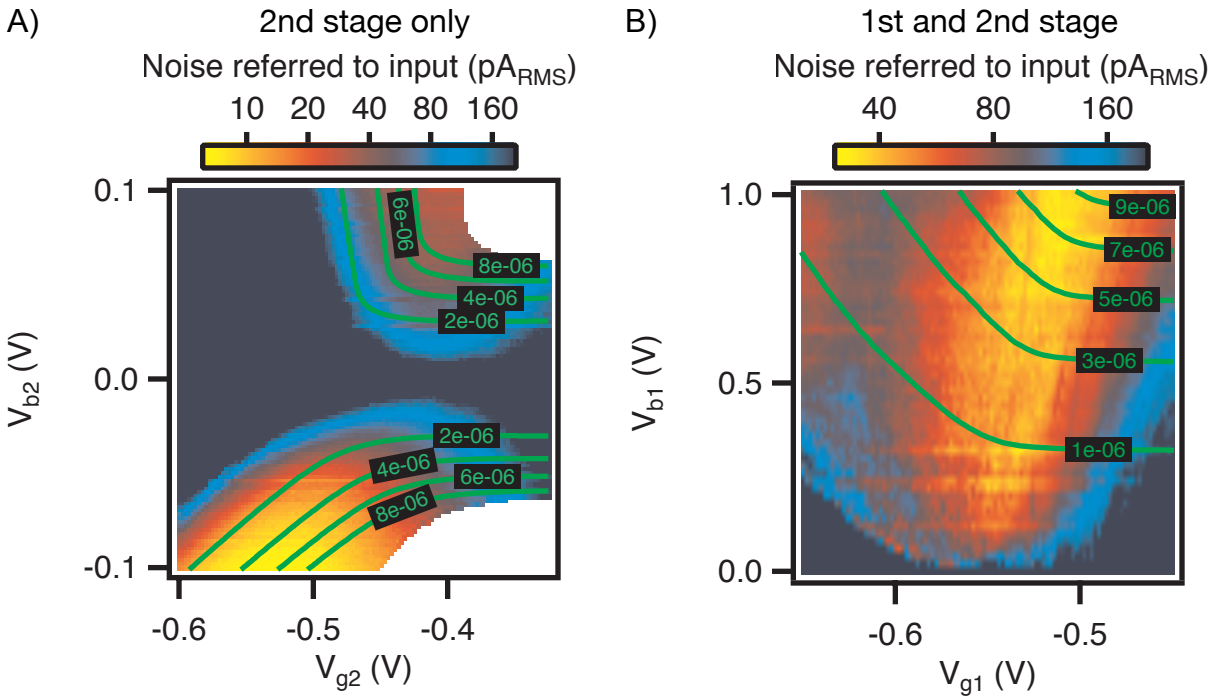

Figure 5.7: Input-referred noise of the cryogenic amplifier with a sample rate of 2 MSa/s as a function of amplifier tuning, with overlaid contours depicting the power consumption of the appropriate stage of the amplifier. For a fixed power expenditure on each stage, the best amplifier settings can be found by following the appropriate contour to minimize the noise referred to input. Panel A (B) depicts the RMS noise at the output of the amplifier as a function of the amplifier's first (second) stage tuning, divided by the gain of the amplifier with the same settings for the first (second) stage of the amplifier. The sample rate of the noise measurement was chosen to match the amplifier's 540 KHz bandwidth (650 ns rise time). The input-referred noise used for panel A was measured with the 1st stage of the amplifier off ($V_{b1} = 0$), which means that all of the noise that was measured at the output of the amplifier must have been generated by the second stage of the amplifier alone. The input-referred noise used for panel B was measured with the 2nd stage of the amplifier on, so the measurement includes noise generated by both the first and second stage of the amplifier.

The cryogenic amplifier was characterized by variation of its tuning parameters V_{b1}, V_{g1}, V_{b2} and V_{g2}, as labeled in the circuit diagram depicted in Figure 5.3. Figure 5.7 displays the RMS noise referred-to-input of the cryogenic amplifier with a sample rate of 2 MSa/s as a function of amplifier tuning, with overlaid contours depicting the power consumption of the appropriate stage of the amplifier. For a fixed power expenditure on each stage, the best amplifier settings can be found by following the appropriate contour to minimize the noise referred-to-input. The noise referred-to-input is depicted without contours in Figure 5.12 of

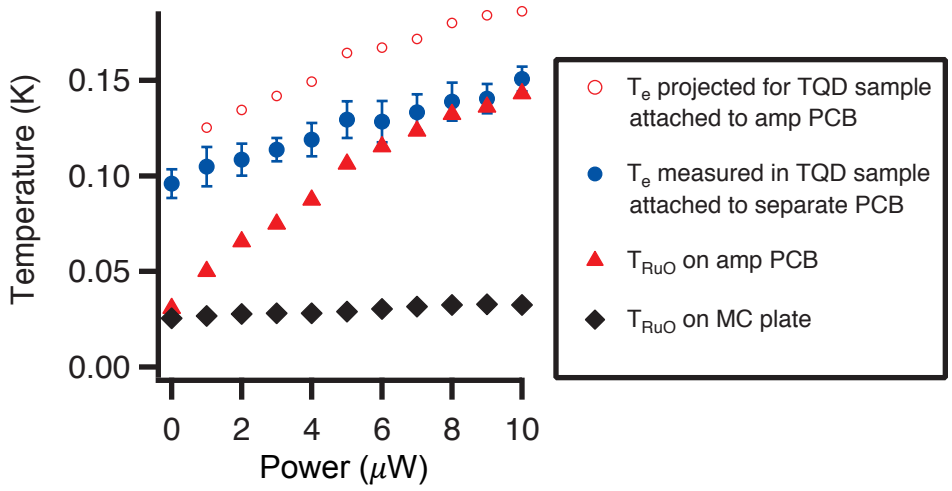

Figure 5.8: Local measurements of temperature made at various locations, all heat sunk to the mixing chamber of a dilution refrigerator, as a function of the power expenditure of the cryogenic amplifier. The filled blue circles represent the electron temperature T_e (measured through Coulomb blockade thermometry) in the triple-quantum-dot sample that was attached to a separate PCB from the amplifier. The red triangles represent the local temperature on the PCB of the cryogenic amplifier, as measured by a RuO resistor mounted on the amplifier's PCB. The black diamonds represent the local temperature on the mixing chamber plate, as measured by a RuO resistor heat sunk directly to the mixing chamber plate. The open red circles represent the electron temperature in the triple-quantum-dot sample when the equilibrium temperature of the mixing chamber was equal to the temperature measured at the amplifier PCB's RuO thermometer for the appropriate power level, based on a linear fit of the data presented in Figure 5.5; thus the open red circles are an estimate for what the electron temperature of the sample would have been if it were heat sunk to the amplifier's PCB.

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the appendix. Figure 5.7 panel A (B) depicts the RMS noise at the output of the amplifier as a function of the amplifier's first (second) stage tuning, divided by the gain of the amplifier with the same settings for the first (second) stage of the amplifier. The RMS noise at the output of the amplifier (Figure 5.13 of the appendix) was measured with a sample rate of 2 MSa/s with a 1 KHz high pass filter. The sample rate of the noise measurement was chosen to match the amplifier's 540 KHz bandwidth (650 ns rise time). The RMS noise used in panel A (B) was measured with fixed second (first) stage settings V_{g2}=-0.5 V and V_{b2}=-0.1 V (V_{g1}=-0.5 V and V_{b1}=0 V). The input-referred noise used for panel A was measured with the 1st stage of the amplifier off ($V_{b1} = 0$), which means that all of the noise that was

measured at the output of the amplifier was generated by the second stage of the amplifier alone. The input-referred noise used for panel B was measured with the 2nd stage of the amplifier on, so the measurement includes noise generated by both the first and second stage of the amplifier. The gain of the amplifier (Figure 5.14 of the appendix) was measured by examining the amplifier's response to a fixed current signal (generated by modulating V_{P2} on the quantum dot sample) as a function of the amplifier's first (second) stage setting. The gain of the amplifier used in panel A (B) was measured relative to fixed second (first) stage settings V_{g2}=-0.525 V and V_{b2}=-0.1 V (V_{g1}=-0.55 V and V_{b1}=1 V). The green contours represent the power expended by the first (second) stage of the amplifier as a function of the amplifier's first (second) stage settings (Figure 5.15 of the appendix). The power expended by the amplifier was measured by multiplying the current passing through each stage of the amplifier by the applied voltage. The current passing through each stage of the amplifier was measured using a Keithley 2400 source meter; however, during normal operation of the amplifier, the source-drain voltages for the first and second stage were applied using a SIM 928 module from SRS in order to reduce noise.

5.4 Results and Discussion

Figure 5.8 shows the results of the enhanced heat sinking technique. A measurement of local temperature as a function of amplifier power was made at various locations, all of which were nominally heat sunk to the mixing chamber of the dilution refrigerator. Blue circles represent the electron temperature T_e in the triple-quantum-dot sample, measured through Coulomb blockade thermometry. The red triangles represent the local temperature on the PCB of the cryogenic amplifier, as measured by the RuO thermometer mounted there. The black diamonds represent the local temperature on the mixing chamber plate, as measured by a RuO thermometer heat sunk directly to the mixing chamber plate. We observe that the temperature on the amplifier PCB rises much faster than the temperature in

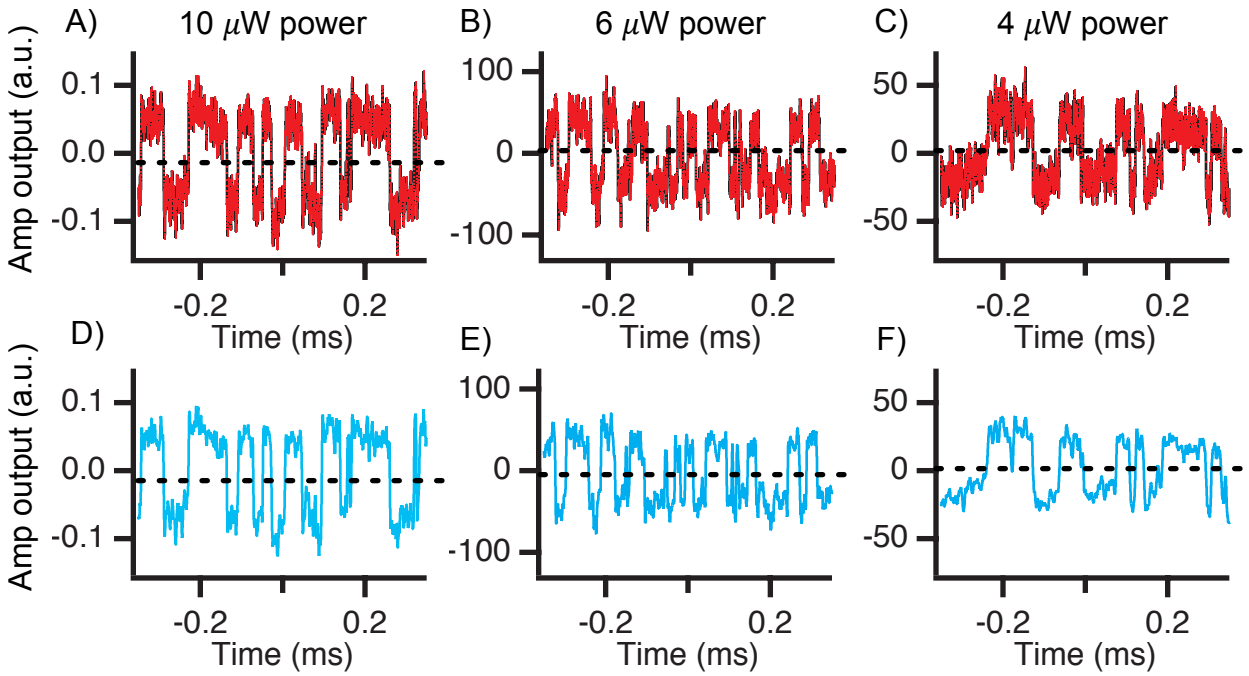

Figure 5.9: Single shot charge transitions between a quantum dot and electron reservoir, measured using a cryogenic amplifier with various amounts of power dissipation. A quantum dot was formed on the bottom half of the triple-quantum-dot sample and was tuned such that its electro-chemical potential lined up with that of a nearby electron reservoir; in this configuration, thermal fluctuations cause an electron to intermittently tunnel into and out of the reservoir, resulting in a random telegraph signal as measured by the quantum dot charge sensor on the top half of the device. The dashed line in each plot shows the threshold voltage; voltages below the threshold voltage indicate the n electron charge configuration, whereas voltages above indicate the n+1 electron charge configuration. Panels A-C depict the output of the cryogenic amplifier with a 1 KHz high pass filter and measured with a sample rate of 20 MSa/s. The amplifier's rise time is 650 ns, which corresponds to a 540 KHz bandwidth. The gain and noise of the amplifier vary with the amplifier's power expenditure. Panels D-F show the same time traces depicted in A-C respectively, but with a 2.5 μs boxcar filter. After the boxcar filter, the rise time is $\sim$2 μs, which corresponds with a 170 KHz bandwidth.

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the triple-quantum-dot as a function of the amplifier's power, suggesting that the enhanced heat sinking method provides some measure of thermal isolation between the amplifier and quantum dot sample. The electron temperature measured with 10 μW power dissipation in the cryogenic amplifier was 151 $\pm$ 6 mK, which is significantly better than >200 mK electron temperatures reported elsewhere with a similar amount of power dissipation [72,73]. Further evidence that the enhanced heat sinking technique provides an improvement can be

seen by comparing the electron temperature measured in the triple-quantum-dot sample with the open red circles depicted in Figure 5.8, which are an estimate for what the electron temperature of the sample would have been if it were attached to the amplifier's PCB (the open red circles show the electron temperature in the triple-quantum-dot sample when the equilibrium temperature of the mixing chamber was equal to the temperature measured at the amplifier PCB's RuO thermometer for the appropriate power dissipation, based on a linear fit of the data presented in Figure 5.5). The electron temperature that was estimated for a sample attached to the amplifier PCB with 10 μW power dissipation (186 mK) is slightly better than the electron temperatures reported in other work that did not employ the enhanced heat sinking technique, but is still significantly worse than the electron temperature attained with the enhanced heat sinking technique. Having an elevated electron temperature can be detrimental to spin qubits in two ways: charge transitions can be broadened with elevated temperature, making qubit states difficult to distinguish; further, charge noise is expected to increase linearly with temperature [98–100], which could reduce the fidelity of qubit operations. Accordingly, limiting the electron temperature to 150 mK is a valuable improvement over the >200 mK electron temperature observed in previous work [72, 73]. Last, it may be observed that the temperature of the mixing chamber plate rises slower than the temperature of the quantum dot sample, even with the enhanced heat sinking technique; this suggests that there is still room for improvement with regards to heat sinking of the cryogenic amplifier and quantum dot sample. Future work may be able to drastically reduce the effects of the amplifier's power dissipation.

The input-referred noise indicated in Figure 5.7 shows that the cryogenic amplifier provides a significant improvement over measurement without the cryogenic amplifier for comparable bandwidths. The cryogenic amplifier showed roughly $\sim$40 $\mathrm{pA_{RMS}}$ noise with a 540 KHz bandwidth; the DLPCA-200 transimpedance amplifier from Femto can achieve a similar bandwidth on its 10^4 V/A sensitivity setting, but would have a minimum of 2.4 $\mathrm{nA_{RMS}}$ of input-referred noise. If the sensitivity were increased to 10^7 V/A, the minimum input-

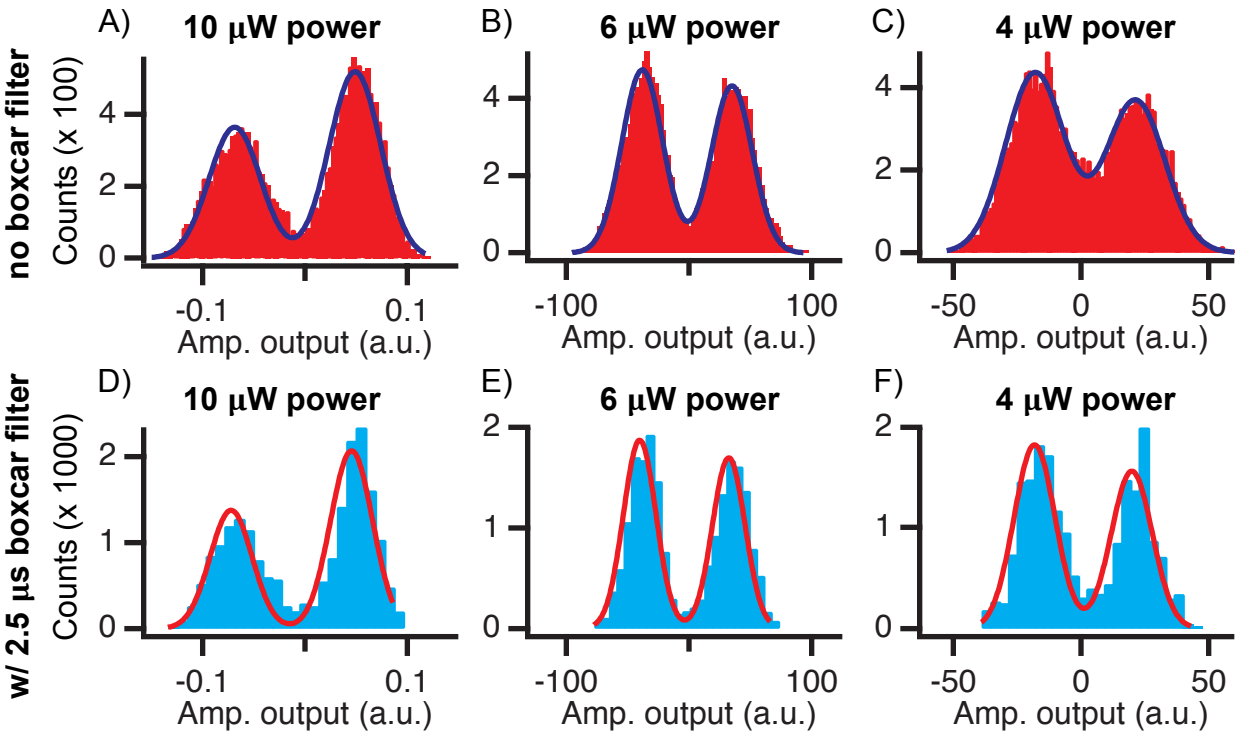

Figure 5.10: Panels A-F show histograms of the time traces depicted in Figure 5.9 panels A-F respectively. The histograms are fitted with a double gaussian, which allows a signal-to-noise ratio to be extracted. Before the boxcar filter is applied (panels A-C), the 10 μW setting has an SNR of 2.3:1, the 6 μW setting has an SNR of 2.2:1, and the 4 μW setting has an SNR of 1.7:1. Given a rise time of 650 ns, the charge sensitivity is 350 $\mu e/\sqrt{Hz}$ for the 10 μW power setting, 370 $\mu e/\sqrt{Hz}$ for the 6 μW power setting, and 470 $\mu e/\sqrt{Hz}$ for the 4 μW power setting. After the boxcar filter is applied (panels D-F), the 10 μW setting has an SNR of 2.9:1, the 6 μW setting has an SNR of 2.7:1, and the 4 μW setting has an SNR of 2.4:1. Given a rise time of 2 μs, the charge sensitivity is 500 $\mu e/\sqrt{Hz}$ for the boxcar filtered 10 μW power setting, 520 $\mu e/\sqrt{Hz}$ for the boxcar filtered 6 μW power setting, and 600 $\mu e/\sqrt{Hz}$ for the boxcar filtered 4 μW power setting.

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referred noise of the DLPCA-200 falls below 50 pA_{RMS}, but then the bandwidth would be limited to 50 KHz.

A quantum dot was formed near gate P2 on the bottom half of the triple-quantum-dot sample and was tuned such that its electro-chemical potential lined up with that of a nearby electron reservoir; in this configuration, thermal fluctuations cause an electron to intermittently tunnel into and out of the reservoir, resulting in a random telegraph signal as measured by the quantum dot charge sensor on the top half of the device. Figure 5.9 displays

single-shot measurements of these charge transitions, measured using the cryogenic amplifier with various amounts of power dissipation. The dashed line in each plot shows the threshold voltage; voltages below the threshold voltage indicate the n electron charge configuration, whereas voltages above indicate the n+1 electron charge configuration. Panels A-C depict the output of the cryogenic amplifier with a 1 KHz high pass filter and measured with a sample rate of 20 MSa/s. The amplifier's rise time is 650 ns, which corresponds to a 540 KHz bandwidth. Panels D-F show the same time traces depicted in A-C respectively but with a 2.5 μs boxcar filter. After the boxcar filter, the rise time is $\sim$2 μs, which corresponds with a 170 KHz bandwidth.

Figure 5.10 panels A-F show histograms of the time traces from Figure 5.9 panels A-F. The histograms are fit with the function

$$N(A) = N_1 e^{-\frac{1}{2}\left(\frac{A-A_1}{\sigma_A}\right)^2} + N_2 e^{-\frac{1}{2}\left(\frac{A-A_2}{\sigma_A}\right)^2},$$

where A is the output value of the amplifier, N_1 and N_2 scale with the number of counts measured in each charge state, and σ_A represents the RMS noise of the amplifier. Fitting each histogram with this double gaussian allows the signal-to-noise ratio to be extracted as $(A_1 - A_2)/(2\sigma_A)$. Before the boxcar filter is applied (panels A-C), the 10 μW setting has an SNR of 2.3:1, the 6 μW setting has an SNR of 2.2:1, and the 4 μW setting has an SNR of 1.7:1. Given a rise time of 650 ns, the charge sensitivity is 350 $\mu e/\sqrt{Hz}$ for the 10 μW power setting, 370 $\mu e/\sqrt{Hz}$ for the 6 μW power setting, and 470 $\mu e/\sqrt{Hz}$ for the 4 μW power setting. After the boxcar filter is applied (panels D-F), the 10 μW setting has an SNR of 2.9:1, the 6 μW setting has an SNR of 2.7:1, and the 4 μW setting has an SNR of 2.4:1. Given a rise time of 2 μs, the charge sensitivity is 500 $\mu e/\sqrt{Hz}$ for the boxcar filtered 10 μW power setting, 520 $\mu e/\sqrt{Hz}$ for the boxcar filtered 6 μW power setting, and 600 $\mu e/\sqrt{Hz}$ for the boxcar filtered 4 μW power setting.

The 2.3:1 SNR observed with the 10 μW setting for the amplifier indicates that a mea-

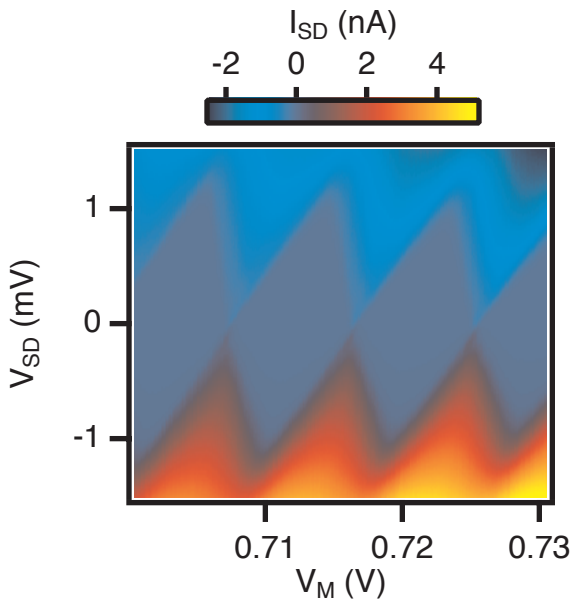

Figure 5.11: Bias spectroscopy performed by measuring the current through a quantum dot while varying the source-drain bias V_{SD} and the voltage on gate M, V_{M}. The value $\alpha_{\mathrm{M}} = 125$ μeV/mV was extracted from the slopes of the Coulomb diamonds.

surement infidelity of $\left(1 - \mathrm{erf}\left(\frac{2.3}{\sqrt{2}}\right)\right)/2 \approx 1\%$ in a 500 KHz bandwidth (650 ns rise time) could be possible with this amplifier, which is competitive with other approaches [84].

5.5 Conclusion

Cryogenic amplification is a powerful tool for increasing the signal-to-noise ratio of high bandwidth charge detection. We provided a study of the heating effect that cryogenic amplifiers have on a nearby charge sensor when both are heat sunk to the mixing chamber of a dilution refrigerator. While the power consumption of a cryogenic amplifier can cause a significant increase in the electron temperature of a nearby quantum dot sample, we presented evidence that these detrimental effects can be mitigated through an enhanced heat sinking technique where the cryogenic amplifier is situated on its own PCB, which is directly heat sunk to the mixing chamber, and thermally isolated from the sample's PCB. Using this heat sinking technique, we showed that the cryogenic amplifier could dissipate 10 μW of power

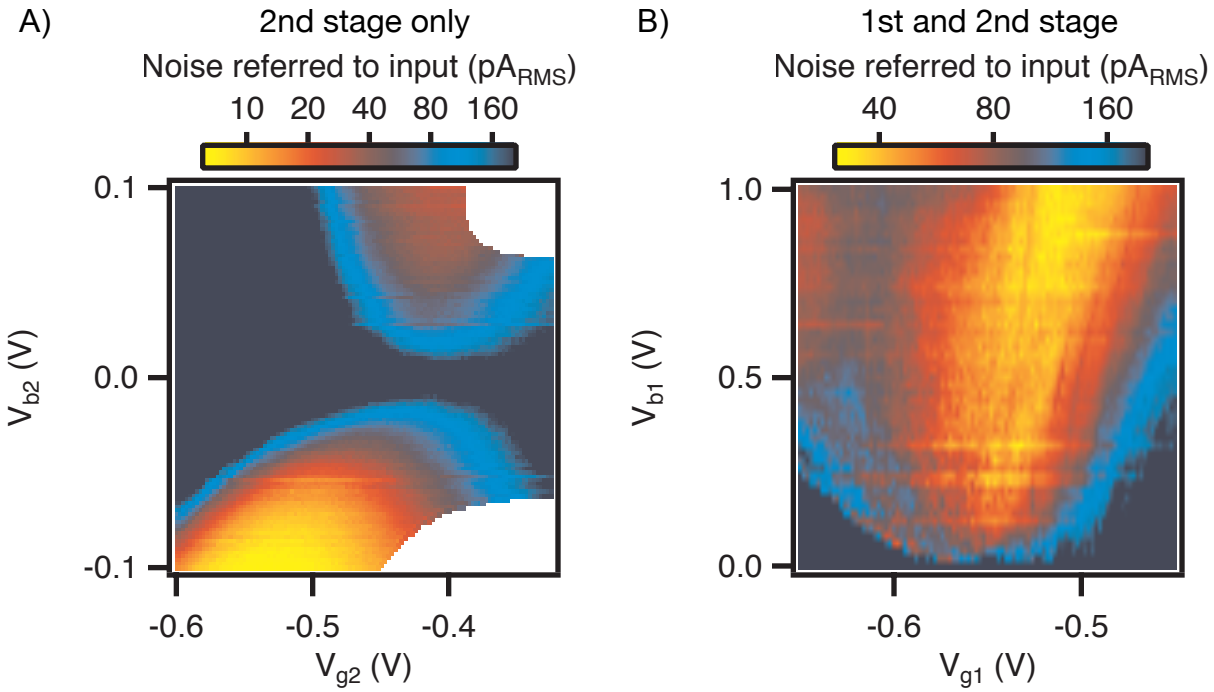

Figure 5.12: Noise referred-to-input of the cryogenic amplifier with a sample rate of 2 MSa/s as a function of amplifier tuning. A (B) depicts the RMS noise at the output of the amplifier as a function of the amplifier's first (second) stage tuning, divided by the gain of the amplifier with the same settings for the first (second) stage of the amplifier.

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while a nearby quantum dot sample maintained an electron temperature of ∼150 mK; this is a significant improvement over previous attempts to heat sink a cryogenic amplifier to the mixing chamber of a dilution refrigerator. Using the cryogenic amplifier, we demonstrated charge state readout of a quantum dot with a rise time of 650 μs and a SNR of 2.3:1.

5.6 Appendix

Figure 5.11 presents the results of bias spectroscopy performed on the charge sensing quantum dot formed in the triple-quantum-dot sample. Bias spectroscopy was performed by measuring the current through the quantum dot while varying the source-drain bias V_{SD} and the voltage on gate M, V_{M}. The value $\alpha_{\mathrm{M}} = 125$ μeV/mV was extracted from the slopes of the Coulomb diamonds.

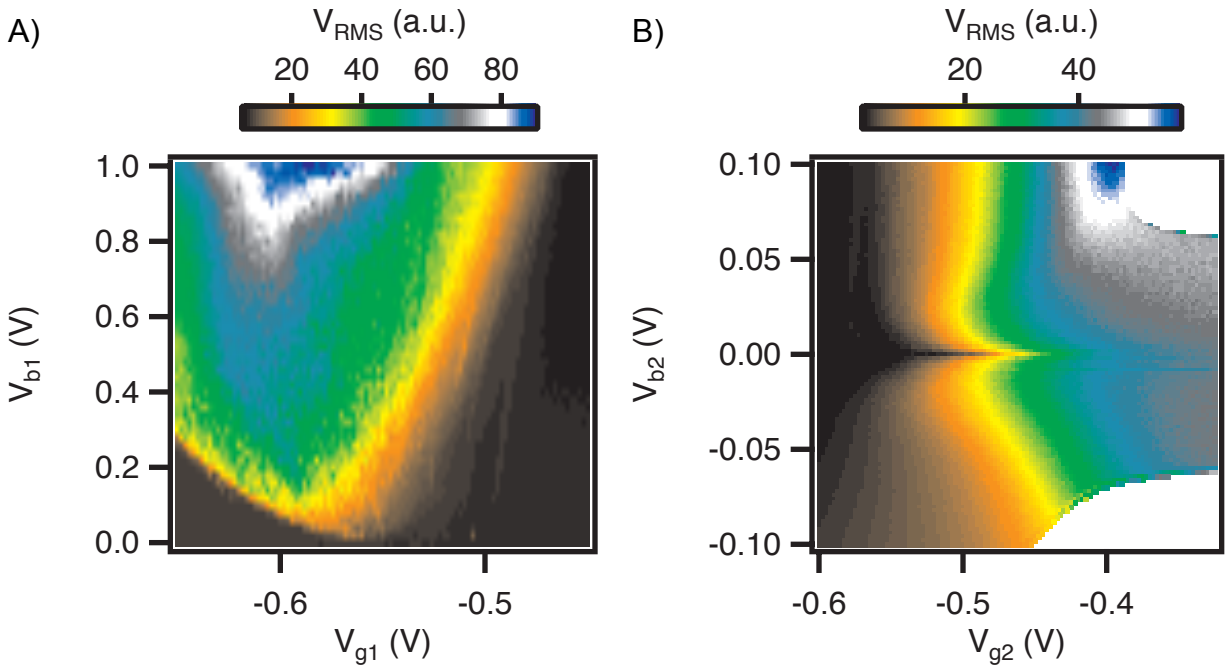

Figure 5.13: The RMS noise at the output of the amplifier, measured with a sample rate of 2 MSa/s with a 1 KHz high pass filter, as a function of the amplifier's first and second stage settings. The sample rate of the noise measurement was chosen to match the amplifier's 540 KHz bandwidth (650 ns rise time). The RMS noise used in panel A (B) was measured with fixed second (first) stage settings V_{g2}=-0.5 V and V_{b2}=-0.1 V (V_{g1}=-0.5 V and V_{b1}=0 V). The noise presented in panel A was measured with the 1st stage of the amplifier off ($V_{b1} = 0$), which means that all of the noise that was measured at the output of the amplifier was generated by the second stage of the amplifier alone. The noise presented in panel B was measured with the 2nd stage of the amplifier on, so the measurement includes noise generated by both the first and second stage of the amplifier.

The input-referred noise of the amplifier as a function of its first and second stage tuning parameters is presented without power contours in Figure 5.12; it was calculated by dividing the noise at the output of the amplifier by the gain of the amplifier for similar settings. Figure 5.13 presents the RMS noise measured at the output of the amplifier that was used to calculate the input-referred noise; it was measured with a sample rate of 2 MSa/s with a 1 KHz high pass filter. The RMS noise presented in Figure 5.13 panel A was measured with fixed second stage settings V_{g2}=-0.5 V and V_{b2}=-0.1 V; the RMS noise presented in Figure 5.13 panel B was measured with fixed first stage settings V_{g1}=-0.5 V and V_{b1}=0 V. The noise at the output of the amplifier presented in Figure 5.13 panel A was measured with

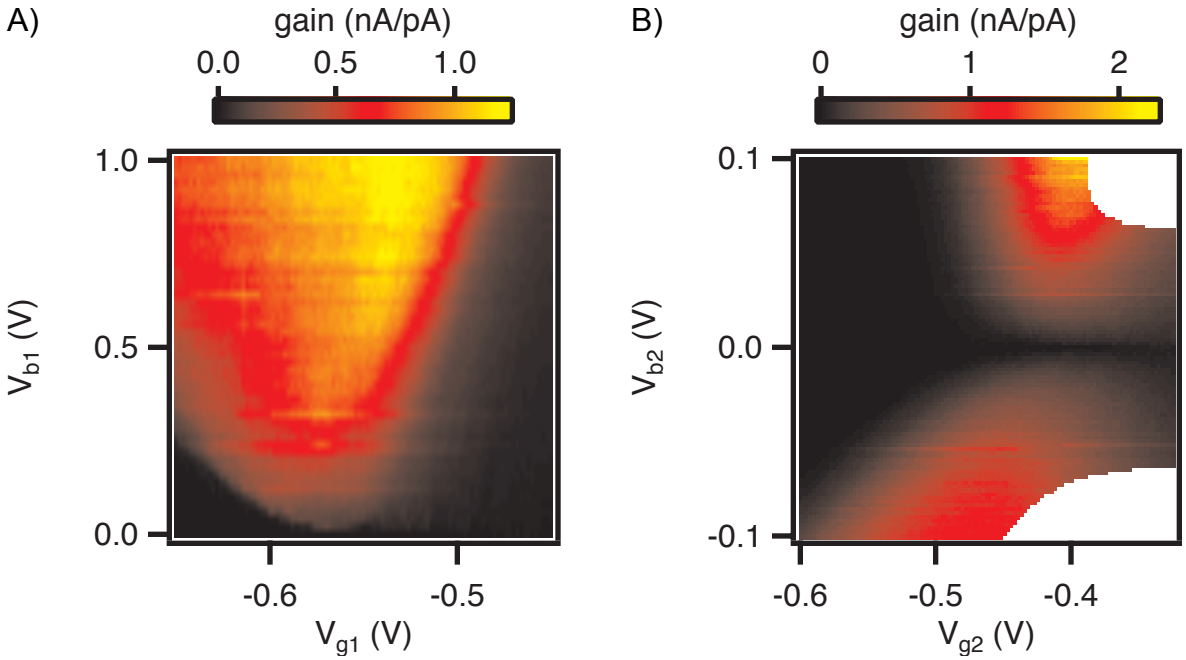

Figure 5.14: The gain of the amplifier as a function of the first and second stage settings of the amplifier. The gain of the amplifier was measured by examining the amplifier's response to a fixed current signal (generated by modulating V_{P2} on the quantum dot sample) as a function of the amplifier's first (second) stage settings. The gain depicted in panel A (B) is relative to fixed second (first) stage settings V_{g2}=-0.525 V and V_{b2}=-0.1 V (V_{g1}=-0.55 V and V_{b1}=1 V).

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the 1st stage of the amplifier off ($V_{b1} = 0$), which means that all of the noise was generated by the second stage of the amplifier alone. The noise at the output of the amplifier presented in Figure 5.13 panel B was measured with the 2nd stage of the amplifier on, so the measurement includes noise generated by both the first and second stage of the amplifier.

Figure 5.14 presents the gain of the amplifier that was used to calculate the noise referred-to-input; it was measured by examining the amplifier's response to a fixed current signal (generated by modulating V_{P2} on the quantum dot sample) as a function of the amplifier's first (second) stage setting. The gain of the amplifier presented in Figure 5.14 panel A was measured relative to fixed second stage settings V_{g2}=-0.525 V and V_{b2}=-0.1 V; the gain of the amplifier presented in Figure 5.14 panel B was measured relative to fixed first stage settings V_{g1}=-0.55 V and V_{b1}=1 V.

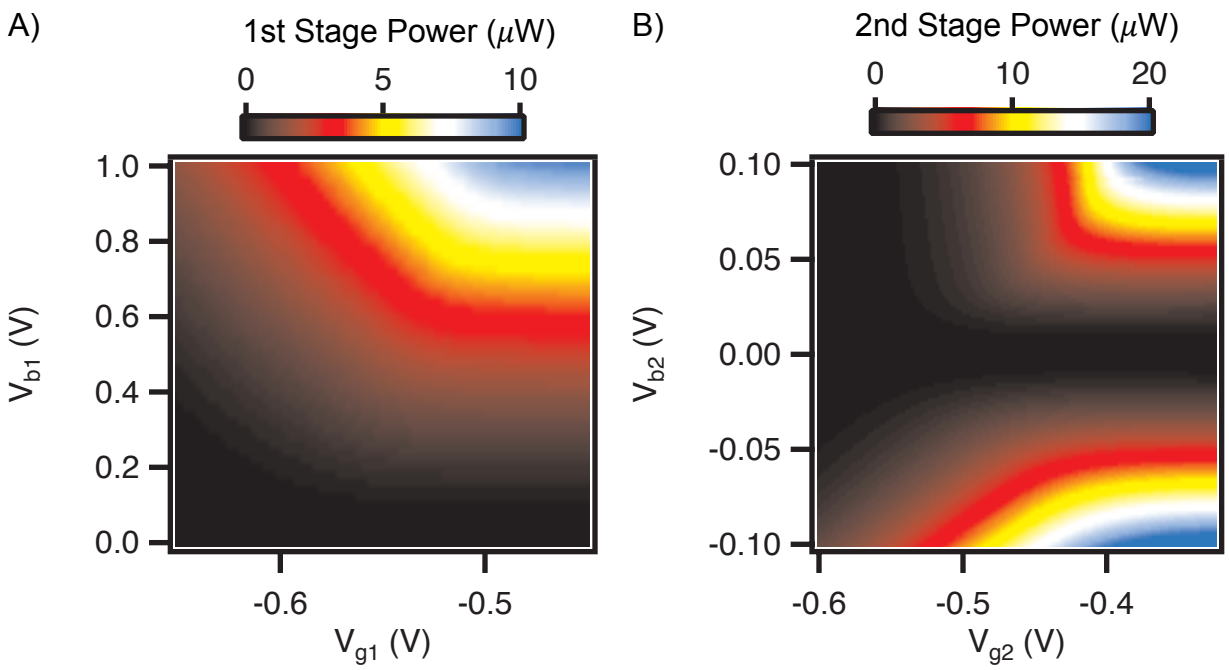

Figure 5.15: The power dissipation for each stage of the amplifier as a function of the amplifier's first and second stage settings. The power expended by the amplifier was measured by multiplying the current passing through each stage of the amplifier by the applied voltage.

Figure 5.15 displays the power expended by each stage of the amplifier as a function of the first and second stage settings, which was calculated by multiplying the current passing through each stage of the amplifier by the applied voltage. The current passing through each stage of the amplifier was measured using a Keithley 2400 source meter; however, during normal operation of the amplifier, the source-drain voltages for the first and second stage were applied using a SIM 928 module from SRS in order to reduce noise.

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