Thermal resistance of interfaces created by mechanical transfer of silicon nanomembranes

by

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Abstract

Nanoscale thermal management is of fundamental importance in modern electronics [1, 2]. As electronic device dimensions continue to shrink, thermal transport becomes increasingly dominated by structural interfaces and materials inhomogeneities [3]. Thermal resistances are most useful in either of the extremes; for example, low thermal resistance is required to manage on-chip hotspots in electronics [4], while high thermal resistance is required in thermoelectric energy conversion applications [5, 6]. With the advent of transferable and flexible electronics based on semiconductor nanomembranes, and frequently involving composites of quite disparate materials, the question of thermal transport across interfaces is becoming increasingly important [7, 8, 9].

The interfacial thermal resistance (ITR) of many interfaces have previously been measured, with most ITR values falling between 5 m^2K/GW and 100 m^2K/GW [1]. In order to better understand the properties that determine ITR, it would be very useful to study the thermal resistance between two well-aligned, identical, single crystals. In such a system, the nature of the interface itself is paramount in determining ITR.

In this thesis, we present measurements of the interfacial thermal resistance of single vdW-bonded interfaces between single-crystal silicon regions. We show that these transferred Si-Si interfaces can have an ITR as low as 2.8 m^2K/GW, up to five times lower than any previously reported thermal resistances of mechanically created interfaces. Further, we demonstrate that the surface condition is critical in determining and controlling the thermal resistance across the interface. Interfaces formed between Si surfaces that are hydrogen-terminated have an ITR of 9.2 m^2K/GW, more than three times higher than that observed when one of the surfaces is terminated by a thin oxide layer. Both values are lower than any previously reported ITR of

mechanically joined interfaces.

We support the thermal measurements with characterization of the interfaces by high-resolution scanning transmission electron microscopy (STEM) and atomic force microscopy (AFM). We present theoretical calculations of the ITR using a modification of the acoustic mismatch model [10] and a theoretical framework for van der Waals (vdW) bonded interfaces [11]. Together the theoretical calculations and interface characterization allow us to understand the ITR results in terms of bonded vdW interfaces, and they confirm the importance of the thin oxide layer in decreasing the ITR by increasing the interfacial bonding energy.

First, in Chapter 1, we describe the materials and techniques used to create van der Waals bonded interfaces by mechanically transferring nanomembranes.

In Chapter 2 we focus on the motivation for studying the thermal resistance of materials interfaces as it relates to modern applications.

In Chapter 3 we review the previous work, both theoretical and experimental, in the field of interfacial thermal measurements.

In Chapter 4 we describe the differential 3ω measurement technique we use to determine the interfacial thermal resistance of nanomembrane interfaces, and review the experimental setup used to take the required measurements.

In Chapter 5 we discuss the interface created by mechanically joining two single crystals of silicon, and show results of measurements done on two bonding configurations: between a pair of hydrogen-terminated surfaces, and between a hydrogen-terminated and an oxide-terminated surface.

Finally, in Chapter 6 we offer concluding remarks and suggest future research directions.

Appendix C gives preliminary ITR results through a third Si-Si interface type, one formed with an interfacial termination of hexamethyldisilazane.

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Chapter 1

Introduction to nanomembranes

1.1 From bulk to nanoscale

Silicon nanomembranes (Si NMs) are extremely thin sheets of crystalline silicon. While two dimensions of these silicon sheets can be quite large (we'll think of them as the lateral dimensions), the third dimension (vertical) is constrained to being hundreds of nanometers thick or less.

The nanoscale thinness of nanomembranes leads to novel properties and applications [8]. One of the most obvious properties is that what is usually a rigid solid material, silicon, becomes bendable, meaning it will readily deform to comply with the shape of another object. It may be helpful to draw an analogy with a more familiar material—think of the difference between a hunk of aluminum and aluminum foil. You could never imagine being able to wrap a piece of solid metal around your leftover pizza, but if that single piece of metal is very thin, it becomes no problem at all to bend it and form it around whatever shape you like.

Figure 1.1(a-c) schematically demonstrates the importance of the flexibility of nanomembranes. A block of bulk silicon, when bonded to an imperfect substrate,

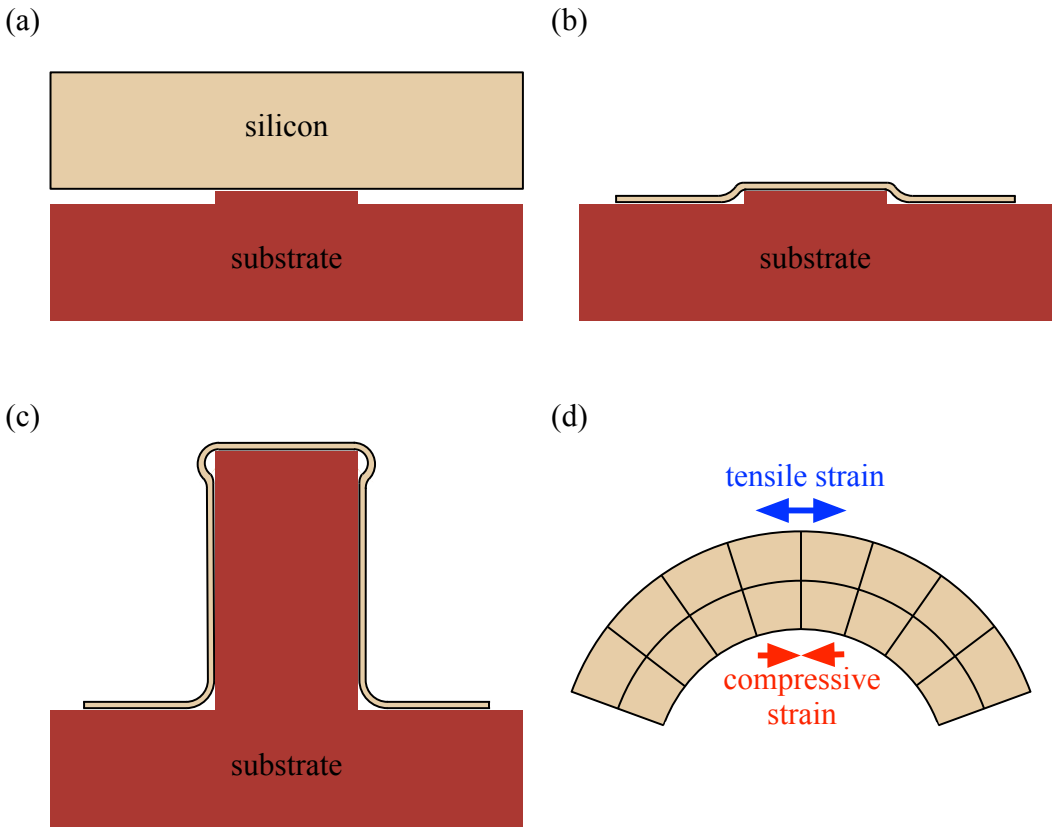

Figure 1.1: Schematic cross sectional views demonstrating the flexible nature of silicon nanomembranes. (a) A thick block of silicon, when placed on an imperfect substrate, results in large areas of unbonded interface. (b) A silicon nanomembrane is thin enough that it conforms to an imperfect substrate and increases the interface area. (c) Silicon nanomembranes can also conform to substrates that are purposefully textured or shaped. (d) The flexibility of silicon nanomembranes leads to stretching and compressing of the material, called tensile strain and compressive strain.

will leave large areas of interface unbonded. A thin, flexible nanomembrane, however, is able to deform across an imperfection in the substrate to create a better interface between the two materials. The flexibility of nanomembranes not only works to help ameliorate the effects of imperfections, but can also be used to purposefully engineer new structures.

A corollary to this flexibility is stretchability. To stretch your hamstrings, you flex at the waist and bend forward. The muscles on the outside of that bend, the

hamstrings and back, are lengthened and stretched. Meanwhile, the flesh on the inside of that bend, maybe your belly, is compressed. So to bend, there must be some stretch and some compression. The same is true of silicon nanomembranes. When bent the material on the outside of the bend is stretched—we call this tensile strain—while the material on the inside of the bend is compressed—we call this compressive strain. This dynamic is illustrated in Fig. 1.1(d). It is not necessary, however, to bend nanomembranes to achieve tensile or compressive strain. Because nanomembranes are so thin, they are stretchable just by pulling. In the same way that it is (in general) easier to stretch thinner rubber bands than thicker rubber bands, it is also easier to strain thin silicon.

Another important property is that the total area of the outer surface of the nanomembrane is greatly increased compared to the volume. In general, surface area changes like the square of the dimension of the object, while volume changes like the cube (note that even the language we use to describe these powers are related to exactly this: squares have area, cubes have volume!). Because nanomembranes are only shrunk in a single dimension, the vertical, this concept must be slightly altered. Both volume and surface area decrease linearly with the shrinking height. Unlike the volume, however, because the top and bottom surfaces of the block remain unchanged, the surface area does not disappear to zero even as the height becomes infinitesimally small. The effect is that what happens at the top and bottom surfaces becomes increasingly important as the nanomembranes become more and more thin. Both electronic and thermal transport effects of increasing the surface-to-volume ratio in silicon structures have been studied is some detail [14, 15, 16].

A third property directly related to the thinness of nanomembranes, and one that we take advantage of in this work, is that the bottom surface is not far from the top surface, making it easier to make measurements from the top down. If we

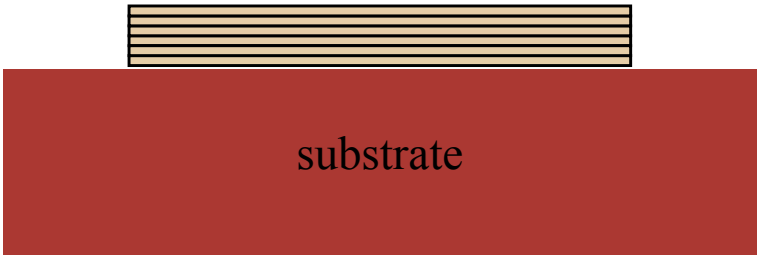

Figure 1.2: Cross sectional schematic view of a stack of silicon nanomembranes. Stacking nanomembranes leads to a high density of interfaces in a small volume. Because the surface and interface properties are of extreme importance in nanomembranes, stacking is an exciting tool for engineering the overall properties of the material.

consider placing a nanomembrane on some substrate, we create an interface between the nanomembrane and the substrate. That interface, when probed from above, is obscured by a relatively small amount of material. This means that measurements of the interface are easier to make, as the effects of the interface are more pronounced compared to the bulk material effects.

Lastly, imagine placing many nanomembranes on top of each other. Because the vertical dimension of each nanomembrane layer is so small, we end up with many wide-area interfaces stacked very close to each other. In these very small structures the surfaces and interfaces have an outsized effect on the overall properties of the material, and by stacking we can further increase the number interfaces in a still very small volume. In this way we can imagine creating layered materials in which the interfacial properties between layers are a dominant effect. Fig. 1.2 shows schematically a stack of nanomembranes, which results in a high density of interfaces in a small volume. The ability to stack nanomembranes will be used in this thesis.

1.2 Fabrication of silicon nanomembranes

Silicon nanomembranes can be made from silicon-on-insulator (SOI), which consists of two layers of silicon separated by a layer of silicon dioxide. The bottom layer of silicon, often referred to as the handle wafer, has thickness typical of a bulk silicon wafer. The thickness of the top layer of silicon, referred to as the device or template layer, can vary widely, but is much thinner than the handle wafer. The oxide layer, commonly called the buried oxide layer (BOX), can also have a wide range of thicknesses, but is again much thinner than the handle wafer. Template and BOX layers commonly vary from 5 nanometers to several micrometers thick [17].

There are two main methods to produce SOI: the separation by implantation of oxygen (SIMOX) process, and processes using wafer bonding, most notably including the Smart Cut^{TM} process [17]. The SIMOX process uses oxygen implantation to create a layer of SiO_2 below the surface of a bulk silicon wafer. One drawback of this process is that it is very difficult to create the buried oxide layer without compromising the perfection of the template layer crystal during the oxygen implantation process.

In the Smart Cut^{TM} process two wafers are bonded together. Before bonding, one wafer is thermally oxidized and then implanted with hydrogen. The hydrogen implantation creates a layer of imperfections in the bulk silicon substrate just below the silicon surface. This wafer is then wafer-bonded to a hydrophilic bulk silicon wafer. By annealing, the wafers are bonded and the first wafer is cracked off at the perforated layer, leaving the thermal oxide buried between the second bulk wafer and a thin silicon layer of the first wafer. The top surface, where the silicon was cracked off, is polished, and the SOI is ready for use. One of the major benefits of this process is that the original wafer can be re-oxidized and used again and again, thereby significantly reducing the amount of wasted material compared to our expectations

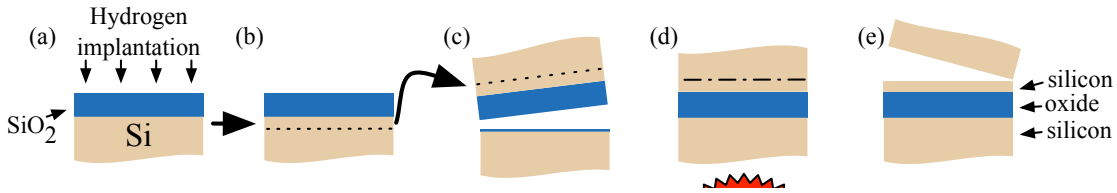

Figure 1.3: Processing steps required to make SOI by Smart Cut™. (a) The process starts with a silicon wafer that has been thermally oxidized. Hydrogen implantation creates a thin layer of imperfections in the silicon crystal. (b) This plane of imperfections is made up of tiny voids in the crystal structure. (c) The hydrogen-implanted oxidized wafer is bonded to a bulk silicon wafer that has a very thin oxide layer at the surface. (d) Annealing the wafers serves to strengthen the bond between them, as well as further aggravate the imperfections in the crystal, which has the effect of creating a perforation. (e) The bulk of the original silicon wafer is separated from the thin layer at the hydrogen-implanted plane. After polishing, the SOI is ready for use.

of waste in the SIMOX process. The Smart Cut™ process steps are illustrated in Fig. 1.3.

We fabricate silicon nanomembranes from SOI made by Soitec using the Smart Cut™ process. The basis of our method is that we eliminate the BOX, thereby releasing the silicon template layer from the handle wafer substrate. In practice, this is done by fabricating holes in the template layer and submerging the entire piece of SOI in hydrofluoric acid (HF), which selectively etches the SiO_2 BOX and releases the nanomembrane. Depending on specifics of the process, which we will cover in chapter 5, the nanomembrane will then either float to the surface of the HF solution or settle down onto the handle wafer. In the case that the nanomembrane floats, it can than be transferred to a new receiver substrate by a wet transfer process. If the nanomembrane adheres to the handle wafer, it can be rinsed and dried and then relocated using a dry transfer process to a new receiver substrate. These steps, necessary for creating and transfer of silicon nanomembranes, are shown in Fig. 1.4.

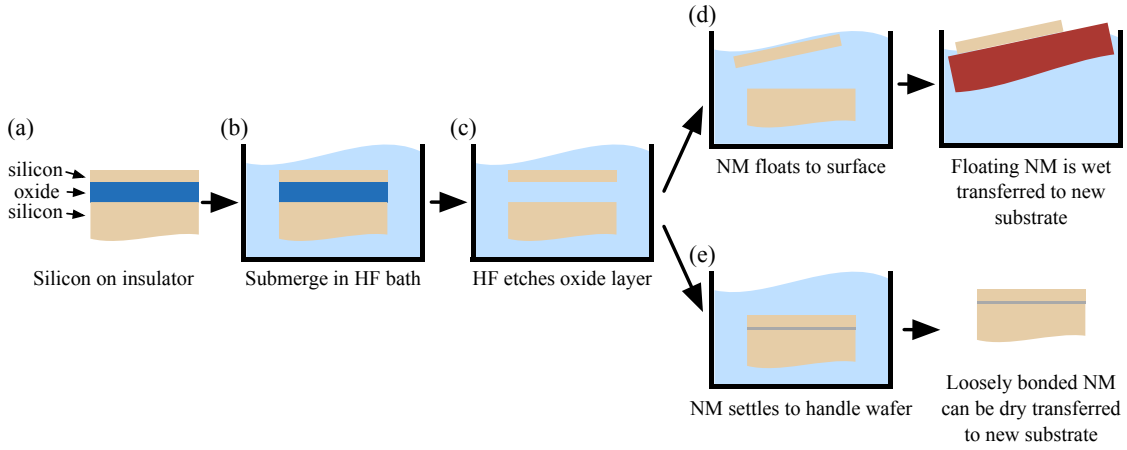

Figure 1.4: Schematic process flow of silicon nanomembrane release. (a) We start with a piece of SOI. (b) The SOI is submerged in an HF bath. (c) The HF etches the buried oxide layer. Depending on the specifics of the process, the released nanomembrane either floats and can then be scooped out onto a new receiver substrate, as in (d), or the nanomembrane settles and loosely bonds to the handle wafer, which can then be removed and used for dry transfer, as in (e).

1.3 Applications

Nanomembranes have properties that make them an exciting platform for many potential applications [7, 18]. Huang *et al.* have used strained nanomembrane to create curled nano mechanical architectures such as nanorings, nanodrills, and nanocoils (Fig. 1.5(a)) [19]. Flexible electronics applications abound. Yuan *et al.* transferred both unstrained and strained nanomembranes onto flexible polymer substrates to make thin-film transistors [20]. Kim *et al.* used transfer-printed silicon nanomembranes to create stretchable, bendable, and even foldable complementary metal-oxide-semiconductor (CMOS) circuits (Fig. 1.5(b)) [21]. Stacking of multiple nanomembranes, each with integrated active electronics, can yield complex three-dimensional circuits [22, 23].

The ability of thin electronics to bend means that incorporating nanomembrane electronics into mechanically dynamic biological systems is possible. Someya *et al.*

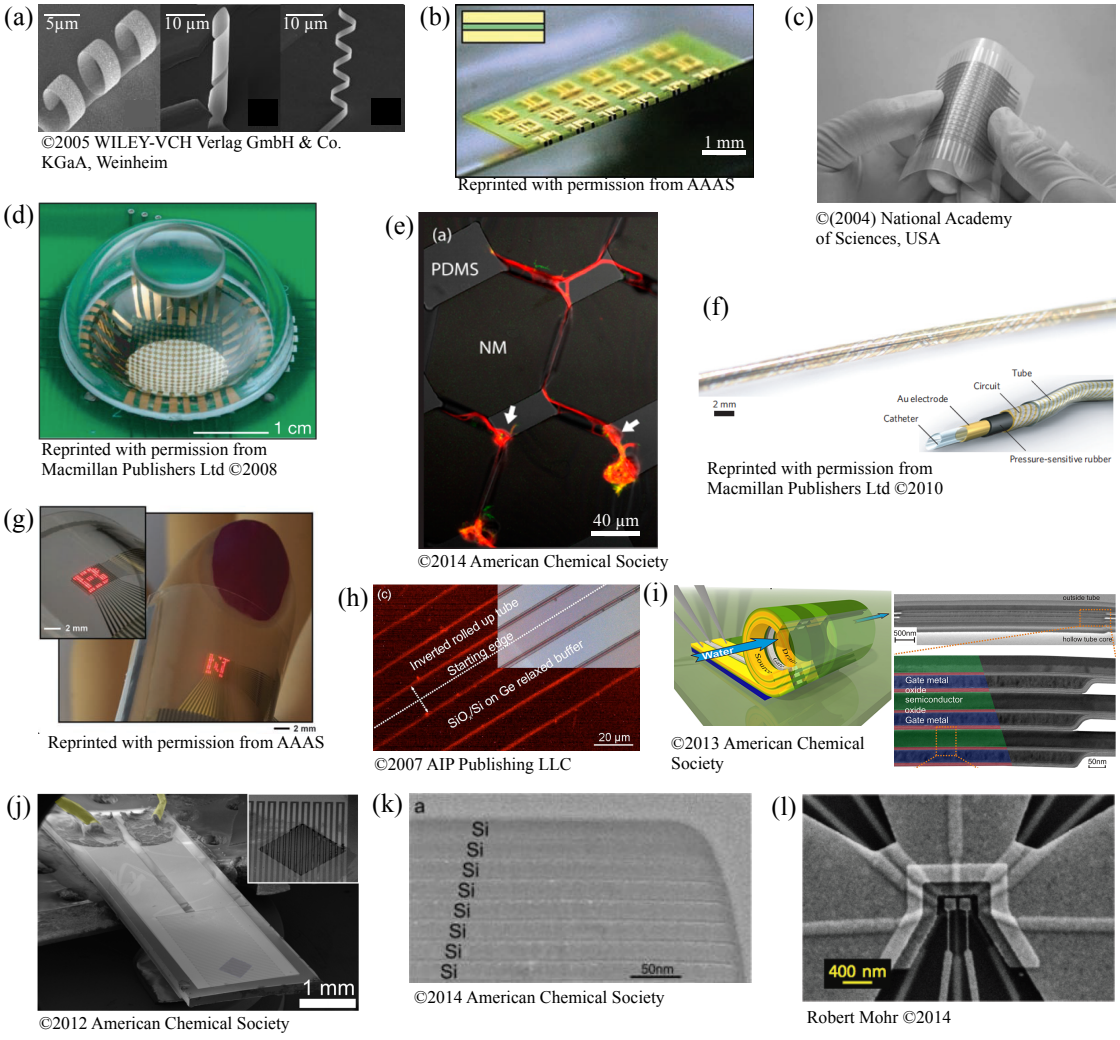

Figure 1.5: Examples of current and future nanomembrane technologies. (a) SEM images of nanorings, a nanodrill, and a nanocoil made with curled nanomembranes. (b) Flexible Si-CMOS technology folded over the edge of a glass microscope slide. (c) Bendable, flexible, pressure sensitive artificial electronic skin. (d) Eyeball camera using curved array of silicon photodetectors. (e) Confocal fluorescence microscope image of neuron growth through buckled NM channels. (f) Thin catheter capable of measuring pressure along it's length and circumference. (g) Flexible LED array wrapped around a fingertip. (h) Fluorescence spectroscopy at room temp of SiO_x/Si tubes rolled on substrate. Inset is light microscopy image. (i) Nanomembrane transistors for microfluidic flow sensors, with cross sectional TEM of rolled tube wall showing multi-material superlattice. (j) SEM of nanomembrane acid sensor device. (k) Cross sectional TEM of mechanically fabricated all-Si superlattice. (l) SEM of double quantum dot on relaxed SiGe nanomembrane.

have demonstrated flexible, pressure-sensitive artificial electronic skin (Fig. 1.5(c)) [24]. Ko *et al.* used silicon nanomembranes to create an electronic eyeball camera (Fig. 1.5(d)) [25]. Cavallo *et al.* used bended nanomembrane microchannels to guide the growth of neurons *in vitro* (Fig. 1.5(e)) [26]. Sekitani *et al.* show how highly bendable circuitry can be useful in the future of medical devices, such as catheters that measure the pressure along their length using an electrically active tubing (Fig. 1.5(f)) [27].

Consumer electronics are also within the scope of nanomembrane applications. Park *et al.* have demonstrating working flexible light-emitting diode (LED) displays (Fig. 1.5(g)) [28], which one can imagine being developed into flexible credit card displays and television screens. Songmuang *et al.* showed that rolled nanomembrane tubes can emit visible light at room temperature (Fig. 1.5(h)) [29]. Other optical applications have also been shown, including using nanomembranes to create Bragg reflectors [30] and Fano filters [31, 32]. A variety of sensor types have also been explored. Grimm *et al.* use rolled nanomembranes to sense fluid flow (Fig. 1.5(i)) [33]. Vervacke *et al.* use nanomembranes to detect dilute acids(Fig. 1.5(j)) [34].

While many of these technologies are exciting, two possible uses for nanomembranes have the potential to revolutionize how we harvest energy and redefine our computational processing abilities. Many-layer stacked nanomembrane superlattices have been suggested as platforms for thermoelectric energy conversion (Fig. 1.5(k)) [35], which enables the conversion of heat energy into electrical energy. Also, single strain-relaxed SiGe nanomembranes have been explored as growth substrates for scaleable condensed matter quantum computers (Fig. 1.5(l)) [8, 36].

All of these applications create thermal management challenges, which we will discuss in the next chapter.

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Chapter 2

The challenge of thermal control in modern electronics

When two materials are brought into contact, there is a natural thermal resistance that arises at the interface. This phenomenon was first observed between solids and liquid helium by Kapitza [37], who showed that there was a discontinuity in the temperature across the boundary. This thermal resistance is in series with the thermal resistances through the materials themselves, and therefore becomes more important as the constituent materials shrink in dimension. Figure 2.1 shows that as the dimension of material between the interfaces decreases, so does the thermal resistance of those materials' regions, even as the materials' thermal resistivities remains the same. The interfacial thermal resistance (ITR), however, stays the same. As the dimension of the materials decreases, then, it is the ITRs that can become the dominant resistances in the overall structure.

As in many physical systems, ITR is most useful in an extreme. When designing new devices with materials interfaces, the interfacial thermal resistance will either be seen as an asset, something to be maximized and taken advantage of, or as a problem,

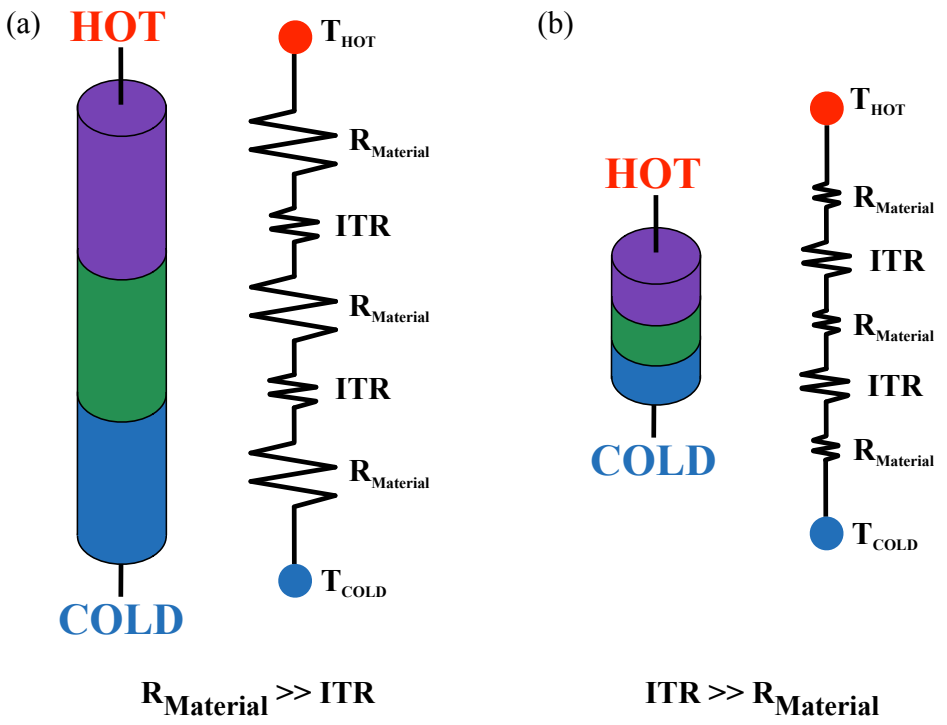

Figure 2.1: Diagram of interfacial thermal resistances in series with materials thermal resistances. (a) When materials are large-scale, the thermal resistance through a structure is dominated by the bulk thermal resistances of the materials. (b) As the dimension of the materials shrink, so do their associated thermal resistances. The ITRs are unchanged, however, and may dominate the overall structural thermal resistance.

something to be minimized and avoided.

For most electronics applications it is necessary to dissipate heat away from areas with high power usage so that devices don't overheat. Because nanomembranes are extremely thin, the interfaces they create with their substrates introduce thermal resistances very close to the heat source. Thus, the interfaces created between nanomembranes and their host substrates become very important factors in heat dissipation.

Conversely, in some applications, such as thermoelectric energy conversion, structures with high thermal resistance are necessary. In order to efficiently convert heat

to electrical power, it is necessary to separate the heat source from it's environment with a material that is thermally insulating.

2.1 Heat dissipation—hotspots

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the building block of the complementary metal-oxide-semiconductor (CMOS) technology used in microelectronic devices. Billions of MOSFETs are used to create microprocessors, random-access memory, and other digital logic devices [38, 39, 40].

A single MOSFET is composed of a gate separated from a semiconducting substrate by an insulating layer, as illustrated in Fig. 2.2(a). The gate is traditionally made of metal, the insulator of silicon dioxide, and the substrate of silicon. Under the edges of the gate are areas called the source and drain, which are doped with electrical carriers to make them conducting. With opposite doping in the region under the middle of the gate, however, there is no electrical path between source and drain. Changing the gate voltage accumulates carriers at the semiconductor-oxide interface, which can result in a conducting path between source and drain. If a voltage bias is applied between the source and drain, a current will flow [41]. Figure 2.2(b-c) shows the schematic operation of such a transistor. For purposes of illustration we show an n-channel MOSFET—that is, the source and drain are negatively doped with electrons while the rest of the substrate is positively doped. A p-channel MOSFET would have opposite doping in all regions.

The electric field generated by the voltage bias between source and drain accelerates electrons toward the drain, where they scatter with the silicon lattice. This scattering, at the drain edge, creates heat within the structure, and leads to what is called a hotspot. Ballistic phonons traveling away from the drain edge create a nonequilib-

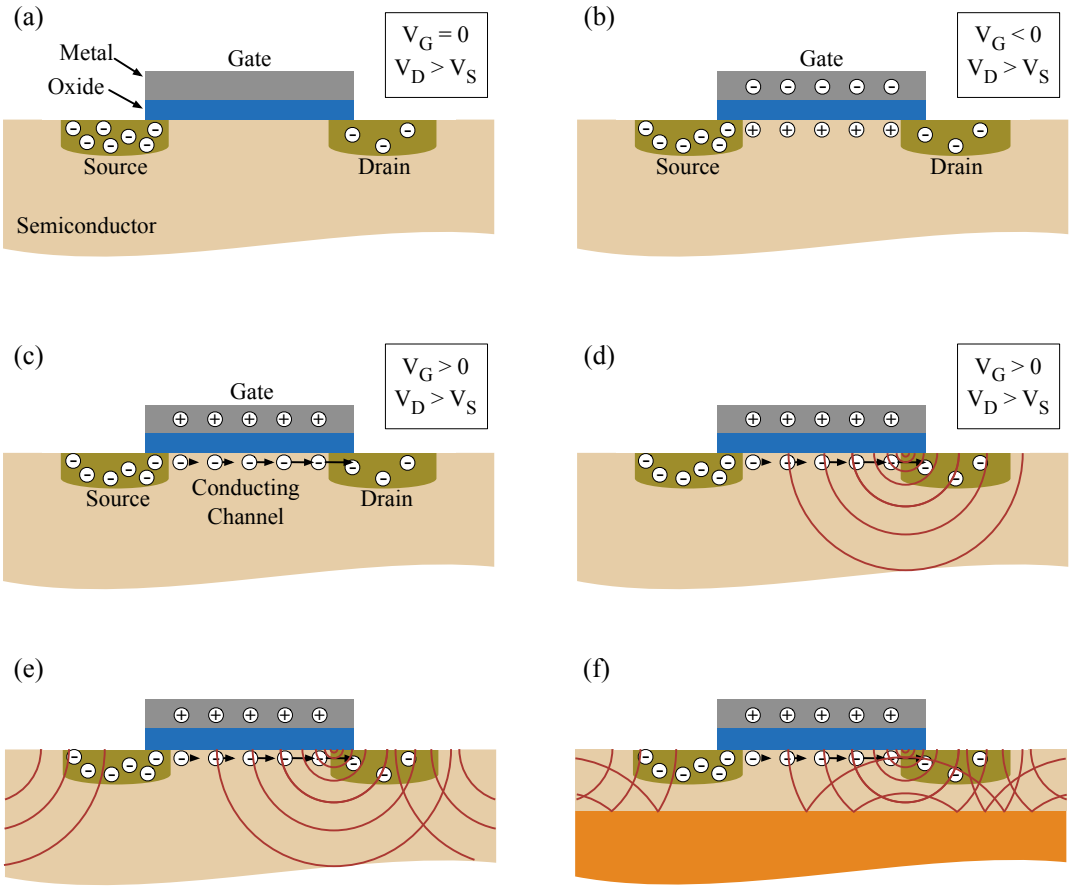

Figure 2.2: Schematic cross sectional views demonstrating the operation of and thermal management issues in n-channel MOSFETs. (a) Schematic diagram of a MOSFET, showing the gate, source, and drain. When the gate is grounded (V_G=0), there is no conduction between source and drain even when a bias is applied between source and drain (V_D>V_S). (b) When V_G<0, holes accumulate at the semiconductor-oxide interface, forming back-to-back p-n junctions, and restricting conduction between source and drain. (c) When V_G>0 electrons accumulate at the semiconductor-oxide interface and a conducting channel between source and drain is created. Because V_D>V_S, electrons accelerate toward the drain. (d) At the drain edge, electrons scatter with the semiconductor lattice, creating phonons which heat the device and raise the operating temperature. (e) Increased density of MOSFETs means that neighboring devices will heat each other, raising the operating temperature further. (f) Fabricating MOSFETs on nanomembranes means that there will be an interface between the silicon environment of the transistor and the underlying substrate. If this interface has high thermal resistance, phonons will not be able to travel away from the device, leading to still higher operating temperatures.

rium system in which the temperature of the hotspot can rise drastically [42, 43], as schematically represented in Fig. 2.2(d). This increases the operating temperature of the device, which leads to performance degradation, high power consumption, and poor device lifetime [44, 9].

Ongoing developments in microelectronics exacerbate the issue of thermal management even further. First, the continued decrease in transistor size and increase in transistor density means that neighboring MOSFETS raise the overall operating temperature further, as illustrated in Fig. 2.2(e). This scaling trend has led to on-chip power densities of over 100 W/cm^2, which is higher than a typical hotplate, and similar to the power density of a nuclear reactor [45]. The accumulated effect leads to localized temperatures that can be raised by hundreds of degrees.

Second, heat produced in CMOS circuits built on nanomembranes encounters additional interfacial thermal resistances that inhibit dissipation into the substrate. Even if the bulk semiconductor substrate is replaced by a material with high thermal conductivity, such as another silicon membrane, there is an added interfacial thermal resistance created at the boundary of the transferred membrane and the substrate. This ITR is in series with the substrate thermal resistivity, and the effect is that scattered phonons remain in the thin nanomembrane region, as shown in Fig. 2.2(f), raising temperatures even further. In fact, the lateral dissipation of heat is affected as well, since boundary scattering reduces the phonon mean free path (MFP) [45]. We can see, then, that interface resistances present a challenge to the thermal management of future nanomembrane electronics technologies. Interfaces must be engineered to have low thermal resistance for technologies to be viable.

Moore's law famously predicts the continued increase in density of components for computing processes, and his prediction that for minimal cost component complexity will double roughly every year has proven to be amazingly accurate in the 50 years

since it was first published [46]. In the same paper there is a section titled "Heat problem," in which Moore wonders, *"Will it be possible to remove the heat generated by tens of thousands of components in a single silicon chip?"* He goes on to state that it should not be a limiting factor, as each component has a three-dimensional solid into which it can dissipate heat. But what if it were billions of components, as there are in modern electronic devices, and we take the bulk of that solid away, as we do in nanomembrane-based electronics? This question threatens the future scaling of CMOS technologies, and Moore's law itself.

One solution to the self-heating problem, particularly for large-scale data centers, is to actively cool the entire apparatus, including non-hotspot areas which don't actually require cooling. This is inefficient, and requires large amounts of energy. Cooling is now a limiting factor in data center performance, and cooling can require as much as half of the overall power budget of such a facility [1]. Not only is a huge amount of power being lost in the form of waste heat, but we are then using even more power to counteract that effect by cooling entire data centers. One partial solution to this huge power sap is to reduce the the temperature escalation and thereby reduce the need for cooling. Fundamental understanding and engineering of the thermal properties of materials interfaces will play a key role. Another solution is to reduce the need for macroscopic cooling by focussing on cooling only the hotspots. This on-chip cooling strategy is potentially more efficient, as it neglects cooling of parts of the apparatus which don't need it anyway. Thermoelectric coolers, which we discuss in the next section, have the ability to integrate into current silicon-based micro and nanoelectronic systems and provide this hotspot-specific microscopic cooling.

2.2 Thermal insulation—thermoelectrics

Energy production is a highly inefficient process. Internal combustion engines, like those used in most cars, only convert about 25% of the total energy available in the gas they burn into useful energy. Diesel engines do better, converting energy with up to 50% efficiency. Electric motors are still better, but require remote energy sources, typically power plants, to charge and run. Coal, petroleum and nuclear power plants are all less than 35% efficient, and natural gas is less than 45% efficient [47]. The majority of the wasted energy in all of these cases is lost to the environment as heat. This huge amount of waste heat, currently unused for any useful purpose, provides ample supply for and motivation to develop efficient thermoelectric energy convertors.

The thermoelectric effect is used to convert thermal energy to electrical energy by the Seebeck effect, or electrical energy to thermal energy through the Peltier effect. Devices that take advantage of the Seebeck effect are used for converting waste heat into electrical power, and producing electronics that don't need batteries. The Peltier effect is used in devices for exact temperature control and on-chip cooling of microelectronics. Advantages of both types of devices include that they have no moving parts, and are therefore very robust and reliable, they are silent, and can be very compact. The major disadvantage is that they are currently prohibitively expensive to produce on a mass scale.

Thermoelectric materials are judged by their dimensionless figure of merit ZT, given as

$$ZT = (S^2\sigma/\kappa)T \tag{2.1}$$

where S is the Seebeck coefficient, σ is the electrical conductivity, κ is the thermal conductivity, and T is the temperature. The benchmark for materials to be considered good candidates for thermoelectric devices is that they have $ZT \geq 3$ [6]. From

Eq. 2.1 we can see that good thermoelectric materials require low thermal conductivity and high electrical conductivity. The problem is that most materials do not fulfill this requirement—metals have high electrical conductivity as well as high thermal conductivity, and insulators have the opposite, low electrical and thermal conductivity. This makes semiconductors, which generally have high Seebeck coefficients, a prime candidate for better thermoelectric materials, because electrical and thermal conductivities can be largely decoupled. Silicon in particular is an appealing candidate because it is abundant, knowledge of silicon processing already exists, and there is already a massive industry devoted to the production of Si devices.

Unfortunately, ZT of bulk Si is about 0.01, not nearly high enough to constitute a good thermoelectric material. Silicon can be doped, which can lead to high electrical conductivity, but the high thermal conductivity of bulk silicon prevents ZT from reaching high enough values to allow for Si to be used in bulk form [48]. Several strategies have been explored to reduce the thermal conductivity in semiconductors, all with the goal of reducing phonon transport. An ideal thermoelectric material would be what is often referred to as an 'electron crystal, phonon glass' [49], meaning the electrical charge carrying electrons are free to move through the material as if it were a crystal, while the heat carrying phonons are impeded as if in a highly disordered glass. Because the electron MFP in silicon is about ten nanometers [50] and the phonon MFP is hundreds of nanometers [51], the ideal 'electron crystal, phonon glass' would introduce scattering centers at an appropriate length scale to greatly reduce the phonon MFP while leaving the electron MFP relatively unchanged. Conceptually, this idea is illustrated in Figure 2.3.

Attempts to increase ZT by decreasing thermal conductivity have focussed on alloying, incorporating nanonstructures such as point defects and nanodots, and increasing interface boundary scattering by introducing nanograins or superlattic-

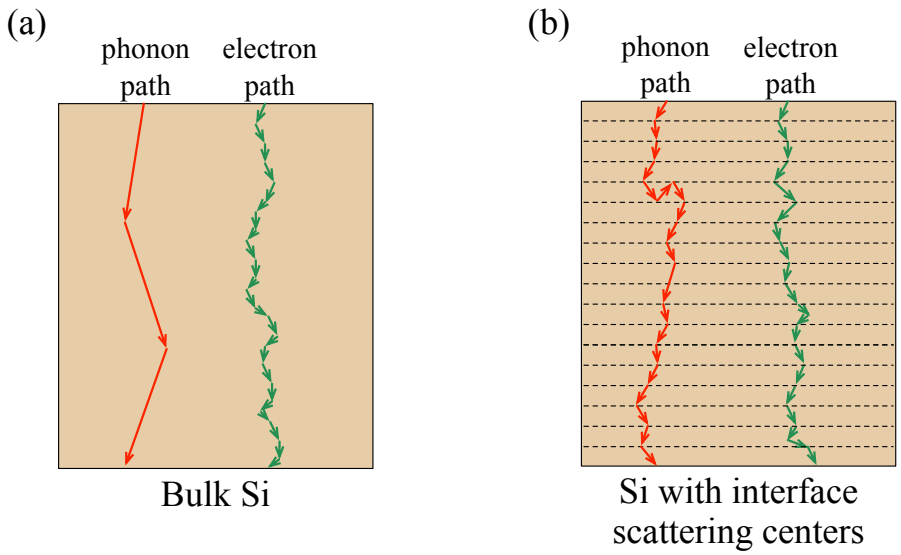

Figure 2.3: Cross sectional view of the effect of scattering centers on mean free path of phonons in silicon. (a) In bulk Si, the MFP of phonons is significantly greater than the MFP of electrons, meaning the electrons follow a more highly scattered path through the crystal. (b) By introducing scattering centers, in this example 2D interfaces, the phonon MFP is greatly reduced. The electron MFP is less effected overall. Because the electrons were scattering much more anyway, adding scattering centers does not have a large impact on their MFP.

ing. Many of the most successful increases in ZT have combined more than one of these strategies [52, 53, 54, 55, 56, 57, 58, 10]. It has also been shown that thermal conductivity can be greatly reduced in low-dimensional single-crystal silicon structures [59, 15, 60, 61], even to as low as the the silicon dioxide amorphous limit [62, 63].

Transfer printing silicon nanomembranes creates a van der Waals bonded interface [64]. Repeated transfers create an all-Si superlattice with many vdW-bonded interfaces in series. Because vdW bonds are weaker than covalent bonds, these vdW interfaces, if properly engineered, may have higher thermal resistance than other, more intimate interface types, and are therefore a potential candidate for further enhancement of ZT in a simple all-Si system [35].

As we have seen, the ability to tune thermal resistance, either to be as high or

low as possible, is of extreme importance. In this work we use silicon nanomembrane transfer to create two-dimensional van der Waals bonded interfaces. The two-dimensionality of the interfaces means that Si NM devices can be useful as a cover or barrier between hot and cold regions in thermoelectric applications, or as substrate environment for future electrical devices. In either case, it is important to be able to control the interfacial thermal resistance created by the membrane transfer process.

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Chapter 3

Interface thermal resistance background

Most applications of nanomembrane electronics, many of which are briefly described in Ch. 1, require the NM to be transferred and bonded to a host substrate. In some cases this material may be a flexible polymer, in others a solid block of semiconductor, and in others a multistack of more nanomembranes. Whatever the case, an interface is created between the nanomembrane and the material that it has been bonded to. While most integrated circuits are built on relatively thick silicon chips, typically hundreds of micrometers thick, nanomembrane electronics are built in sheets of silicon roughly one thousand times thinner. Because nanomembranes are so thin, the interfaces created between nanomembranes and their host substrates become very important factors in thermal management.

Heat flow perpendicularly through the an interface is described by

$$J_Q = \frac{\Delta T}{R_{th}} \tag{3.1}$$

where ΔT is the temperature difference from one side of the interface to the other, and R_{th} is the thermal resistance through the interface [3]. In this work we will refer to R_{th}

across such a boundary as the interfacial thermal resistance, or ITR. What Eq. 3.1 tells us is that, given a boundary between two regions of constant temperature, the amount of heat carried from one side of an interface to another is solely determined by the thermal resistance of the interface. In a sense, this makes the problem very simple, as there are no other factors besides ITR to be considered. On the other hand, because ITR is the only factor controlling heat flow through the interface, we are compelled to understand what specific characteristics of the interface effect the ITR.

3.1 Theoretical concepts

Until recently, there have been two main models that have been relied upon to help understand interfacial thermal resistance: the acoustic mismatch model (AMM) and the diffuse mismatch model (DMM).

The AMM considers a perfect interface between two materials—zero separation between the materials, no roughness at the interface, strong bonding. The ITR, then, arises from the intrinsic differences in the materials on either side of the interface. If the modes of thermal conduction are not perfectly matched, there will be an inability to pass heat across the interface with 100% efficiency. Hence, the rise of a thermal resistance. The theory was originally tailored for insulating materials, in which the heat is predominantly carried by acoustic vibrations of the crystal structure [65], called phonons, but was later expanded to include the role of electrons in heat conduction in non-insulating materials [66].

The AMM assumes that the materials on either side of the interface need not be treated as lattices, but instead can be treated as continua. That is, it assumes the phonon wavelength is much greater than the spacing between neighboring atoms.

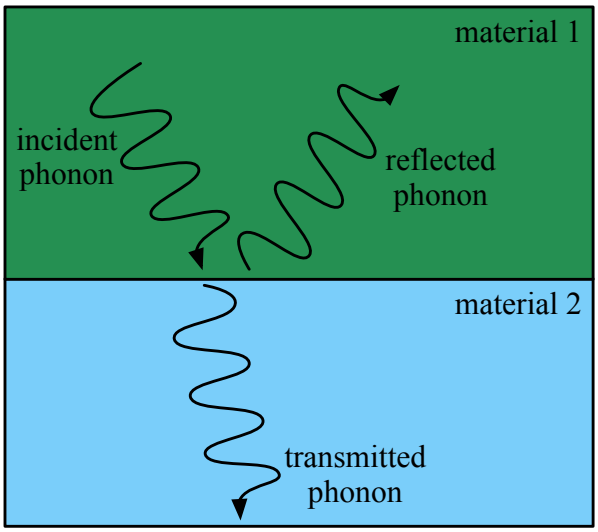

Figure 3.1: Diagram of the phonon transmission and reflection possibilities according to the acoustic mismatch model. The materials on either side of the interface are assumed to be continua, and phonons can be treated as plane waves. Incident phonons can either be reflected or refracted. There is no scattering at the interface.

This means that phonons can be treated as plane waves. Any phonon incident on the interface then has some statistical probability of being either transmitted and refracted, or reflected (Fig. 3.1) [67]. ITR arises from the fact that some statistical portion of phonons will be reflected back into the first material, thereby raising the temperature in that material and creating a temperature difference across the interface.

It should be noted that diffuse scattering of phonons at the interface does not exist in this model, as the reflection and refraction are determined by a generalized analogue of Snell's law of the reflection and refraction of light. As expected, the AMM describes that a perfect interface between two identical materials, which we can think of as no interface at all, would result in zero ITR.

A convenient way to quickly determine the magnitude of the acoustic mismatch between two materials, and therefore the hypothetical ITR arising from that mismatch,

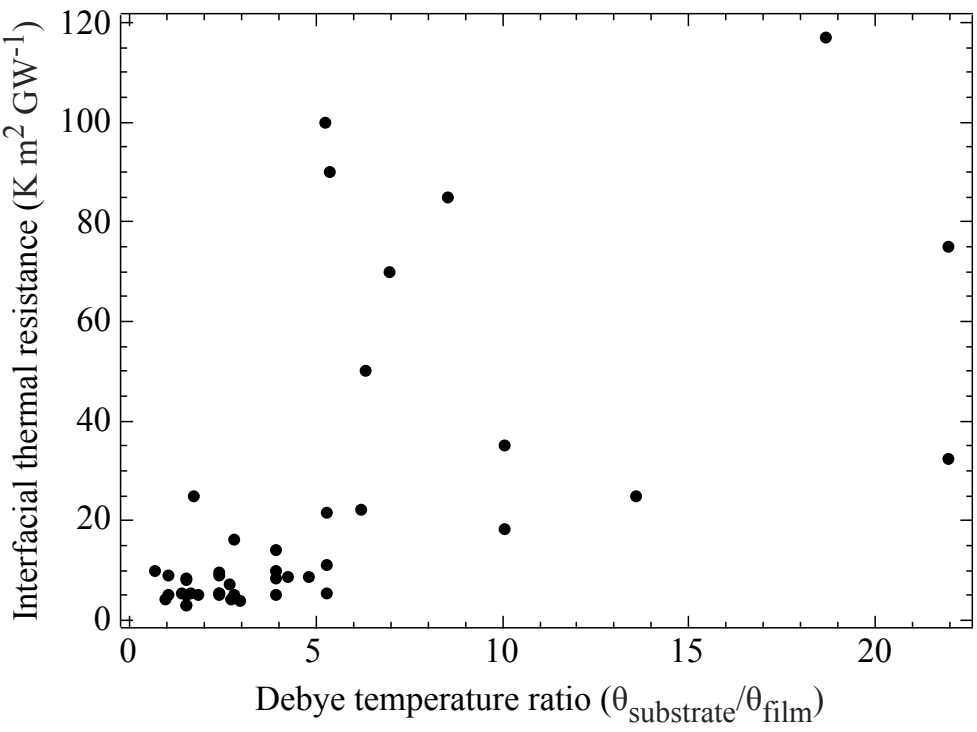

Figure 3.2: Interfacial thermal resistances of metal-nonmetal interfaces vs Debye temperature ratio of the materials forming the interface. While we may see a general trend, it is certain that the Debye temperature ratio, representing the acoustic mismatch between the materials, does not account for the entirety of the variation in ITR. Reference and numerical details of this collection of data can be found in Appendix A

is to refer to their Debye temperatures Θ [68]. Figure 3.2 shows ITR measurement results from several sources [69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 68, 82, 66] plotted against the ratio of Debye temperatures of the materials forming the interface [68, 66, 83, 84, 85, 86]. The interfaces considered here are the subset of interfaces created by a metallic thin film deposited on the surface of a nonmetal substrate. If more than one ITR was reported in a single source for an interface between the same two materials, we only plot the lowest value under the assumption that this value represents the interface that most closely resembles the perfect interface assumed by the AMM. While we can see that there may be some general trend between the

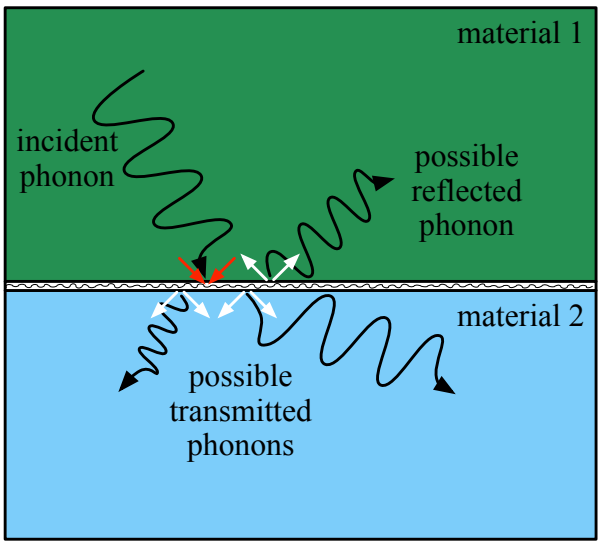

Figure 3.3: Diagram of the phonon transmission possibilities according to the diffuse mismatch model. Incident phonons are destroyed at the interface (as represented by inward red arrows), and new randomized phonons are created (as represented by outward white arrows). All phonons are scattered this way, and there is no correlation between the wave vectors of incident and outgoing phonons.

high mismatch in acoustic modes, represented by a Debye temperature ratios much greater than unity, and high interfacial thermal resistances, we can also see that this alone does not account for all the variation. It has been suggested that the AMM prediction provides a lower limit to the ITR in the case of very good interfaces [3]. However, there are clearly more factors at play.

The diffuse mismatch model presents a different view of the origins of ITR. In the DMM, the interface between two materials is assumed to be perfectly diffuse [87], meaning any incident phonon is destroyed and a new random phonon is created to replace it. The newly generated phonon can either be on the reflected or transmitted side of the interface, and the probability of either case is dependent on the density of the available phonon modes on both side of the interface [67]. This model of interfacial phonon scattering is schematically illustrated in Fig. 3.3. A direct result of the DMM is that at an imperfect interface between identical materials the probability

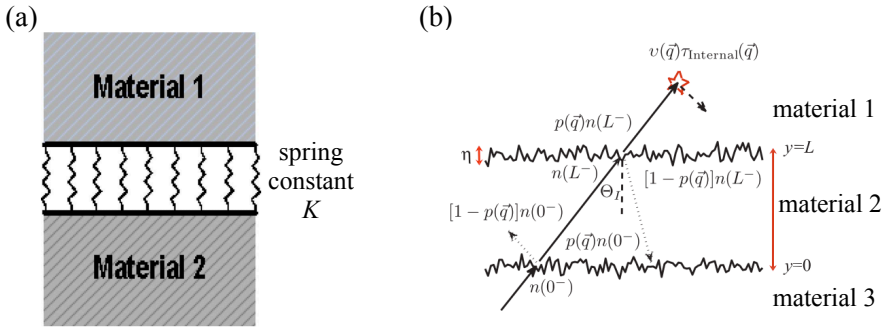

Figure 3.4: Schematic interpretations of modified theoretical models of interfacial thermal resistance. (a) From Prasher, two materials are separated by an effective spring constant, which is dependent on interfacial adhesion energy and separation distance. Reprinted with permission from [11]. ©2009 AIP Publishing LLC. (b) From Aksamija and Knezevic, phonons incident on rough interfaces have probability $p(\vec{q})$ of transmission unscattered, and probability 1 - $p(\vec{q})$ of scattering diffusely. Reprinted with permission from [10]. ©2013 by the American Physical Society.

of transmission is exactly 50%, which would result in the presence of an ITR. This is in opposition to the AMM interpretation of the same interface, where there would be none.

More recently, there has been work toward incorporating the important concepts of both the AMM and DMM into a single model. Prasher modified the AMM to include a non-perfect interface, and instead uses an effective spring constant joining the two materials [11]. The schematic diagram of his theoretical system is shown in Fig. 3.4(a). In this system, the original AMM is recovered as the spring constant $K \to \infty$. K is dependent on the interfacial adhesion energy, and we see in Fig. 3.5 that for adhesion energies less than 1000 mJ/m^2, which correspond to the range of energies attributed to van der Waals bonding, the modified AMM model diverges significantly from the original AMM predictions.

Aksamija and Knezevic have developed a model which treats scattering at the interface separately from the effects of acoustic mismatch [10]. They consider an interface with non-zero roughness, and identify that the DMM assumption of diffuse

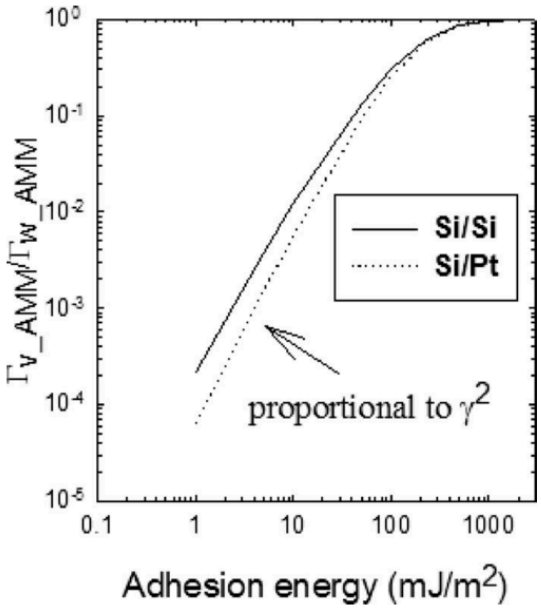

Figure 3.5: Ratio of modified AMM ($\Gamma_{v\text{-}AMM}$) to original perfect-interface AMM ($\Gamma_{w\text{-}AMM}$) versus interfacial adhesion energy. We see that allowing for non-perfect, non-infinite bonding significantly effects the theoretical ITR. Reprinted with permission from [11]. ©2009 AIP Publishing LLC.

scattering may hold for short-wavelength phonons, but that long-wavelength phonons will see the interface as smooth. Conversely, the specular nature of the AMM interface holds for long-wavelength phonons, but the assumption of a perfect interface fails for short-wavelength phonons which scatter from atomic-scale roughness at the interface. They therefore create a phonon momentum dependent factor which describes the probability for a phonon with a specific wave vector to pass through an interface without scattering. A diagram of such a system is seen in Fig. 3.4(b).

Molecular dynamics (MD) calculations have also been used to study heat flow and thermal resistance across materials interfaces [3]. One of the major challenges facing such MD studies, however, is that the computational power necessary to simulate three-dimensional systems of many atoms is prohibitive. This does, however, remain an exciting area of research.

3.2 Measurement techniques

Recently, thermoreflectance has become a widely used method to measure the thermal resistances of thin films and materials interfaces. The technique uses ultrashort pump laser pulses to heat the sample surface, and a probe laser to track the changing reflectance of the sample as it cools. Although the technique was originally presented in 1986 as transient thermoreflectance (TTR) [88], it has been reborn more recently as time-domain thermoreflectance (TDTR) by an advance in the analysis to include information gleaned from the out-of-phase probe signal [89]. More recently still, a tweak to the TDTR setup has resulted in the use of frequency-domain thermoreflectance (FDTR), where the modulation frequency of the pump beam is the independent experimental parameter instead of the probe beam delay [90].

The major advantages of thermoreflectance measurements is that they are a non-contact method of directly measuring thermal transport on the nanometer length scale, and can differentiate between the thermal resistance produced by a thin film and the interface of that thin film at the substrate. A major drawback, however, is that the technique is generally confined to samples with metallic thin film transducers, necessary to allow heating of the surface by laser. Aluminum is commonly chosen due to its large change in optical reflectivity with changes in temperature and strain. Another limiting factor is that the heat diffusion depth, dependent on thermal diffusivity of the material and the frequency of the pump pulses, is generally between 10 and 140 nm, effectively limiting the depth to which the technique can probe [3].

The other common technique for measuring ITR is the 3ω method [91], which we use in this work. This technique uses a single metal 4-probe wire deposited on the surface of the substrate as both the heater and thermometer. An AC current provides periodic heating of the wire, and the fluctuation in temperature is measured by the

change in resistance of the same wire.

The 3ω method also has limitations. First, the top surface must be insulating, in order to prevent the metallic 4-probe devices from leaking current into the sample. Second, the 3ω signal does not differentiate between any thermal resistances in the sample structure. Third, the depths to which the technique can probe are also limited by the AC current frequency and the geometry of the 4-probe devices. These limits can all be accounted for, however. We deposit an insulating aluminum oxide layer by atomic layer deposition to cap all our samples. By carefully designing our sample structures and measurement technique, we can use a differential method to isolate the interface effect on the measured thermal resistance [92]. With careful consideration of the measurement device geometry and the frequency domain used, the depth of measurement also can be controlled.

3.3 Previous solid-solid interface results

A majority of previously measured thermal boundary resistances are of interfaces between non-metal substrates (primarily silicon, sapphire, and diamond) and metal thin films (primarily aluminum and gold) that have been evaporated or sputtered onto those substrates. These metal-substrate interfaces have two major advantages—the constituent materials have highly dissimilar acoustic properties, often characterized by their dissimilar Debye temperatures, which leads to a large thermal resistance at the interface; and the metal surface can serve as the electromagnetic-to-thermal energy transducer necessary for thermoreflectance measurements. Almost all of the reported thermal resistances of these interfaces span only one order of magnitude, between 2.3 and 20 m^2K/GW [69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 68, 82, 66, 87, 93]. The studies which report thermal resistances out of that range for

metal-nonmetal interfaces all aimed to specifically increase ITR by some mechanism, either by choosing materials with particularly significant differences in Debye temperature [13], changing the microstructure at the interface [94, 95], or manipulating the surface chemistry of the substrate material [78].

Several studies have focussed on semiconductor interfaces, motivated by the necessity of thermal management in transistors. Kuzmik *et al.* have studied gallium nitride grown by chemical vapor deposition (CVD) on silicon, silicon carbide, and sapphire substrates and found the resistance at the GaN-Si interface to be 70 m^2K/GW, and at the GaN-SiC interface to be 120 m^2K/GW. They were unable to provide a confident value of the resistance at the GaN-sapphire [96]. In an earlier study, Kuzmik reported the thermal resistance at the interface between aluminum nitride, again grown by CVD, and silicon to be 70 m^2K/GW [97]. Zhao *et al.* report the thermal resistance of AlN sputtered onto Si to be between 55 and 85 m^2K/GW across several samples [94].

The interface of silicon dioxide with silicon is a common and important structure in many applications. The ITR of such SiO_2-Si interfaces has been consistently measured between 18 and 34 m^2K/GW [98, 99, 100, 101, 102]. Yamane *et al.* [101] and Chien *et al.* [102] find that interfaces created by thermal oxidation of silicon produce higher ITRs than those created by plasma-enhanced CVD, electron-beam evaporation or sputtering of SiO_2 onto Si substrates. It is worth noting, however, that the studies of Griffin *et al.* [98] and Kim *et al.* [100] use thermal oxides and find ITRs at the lowest end of all the reported thermal resistance values.

Interfaces created by mechanical transfer have been used to study many factors in thermal interface resistance. Wang *et al.* measured self-assembled monolayers (SAMs) covalently bonded between GaAs and Si, and showed that varying the length of the SAM (n=8, n=9, and n=10) has little effect on the thermal con-

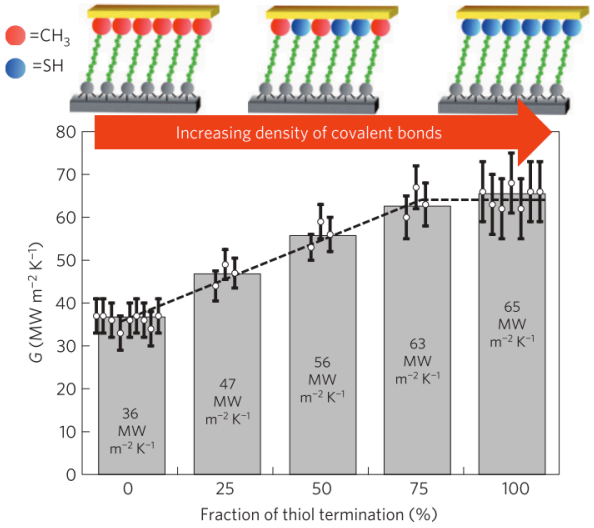

Figure 3.6: Results from Ref. [12] that demonstrate the effects of bonding strength on interfacial thermal conductivity. As the fraction of end-groups which bond covalently with the transferred gold film increases, the effective interfacial thermal conductivity also increases. Reprinted with permission from Macmillan Publishers Ltd: NATURE MATERIALS, ©2012.

ductance through the GaAs/SAM/Si interface, with all interfaces measuring about 37 m^2K/GW [103]. Oh *et al.* show that transfer printing metal films onto substrates produce interfaces with higher thermal resistances than interfaces between the same materials that have been created by sputtering the films directly onto the substrates. High temperature annealing (1100°C for 1 hour), however, decreases thermal resistance in at least one transfer-printed sample to a value equal to the sputtered interface. The difference between transfer-printed and sputtered interface is attributed to the difference in "area of intimate contact" [75]. Losego *et al.* use gold transferred onto SAMs to vary the bonding chemistry of the interface between purely vdW bonded CH_3 end-groups and purely covalent SH end-groups. Their results show a decrease in interface thermal resistance, from 28 m^2K/GW in the purely vdW case to 15 m^2K/GW in the purely covalent case (Fig. 3.6) [12].

Two studies have considered mechanically contacted Si-Si interfaces. In the first,

Huxtable *et al.* measure the thermal resistance through the interface created when polysilicon cantilevers relax onto polysilicon substrates. The samples are baked on a hotplate at 110°C, sputtered with aluminum, and measured with thermoreflectance. They report the polysilicon-polysilicon interface to have a thermal resistance of 110 m^2K/GW[104]. Grimm *et al.* measure the thermal resistance through a Si-Si interface by growing a highly strain-graded and dislocated silicon nanomembrane on a relaxed germanium substrate, releasing the nanomembrane from the Ge substrate, which leads to the thin silicon sheet rolling into a tube, and then finally compressing the rolled nanomembrane tube to form a mechanical superlattice. Because the rolling is performed in hydrogen peroxide, both surfaces at each of the interface are oxidized. They report the thermal resistance across each interface to be 33 m^2K/GW [35].

3.4 H-terminated vs oxide-terminated substrate

Several studies have investigated the difference in ITR between interfaces created with either hydrogen-terminated or oxide-terminated substrates, but that are otherwise identical.

Collins *et al.* sputtered aluminum onto diamond substrates functionalized with either hydrogen (by hydrogen plasma) or oxygen groups (annealed in air) and measured with TTR. They found that hydrogen-terminated diamond interfaces had a five-fold increase in ITR, 50 m^2K/GW, over those that were oxygenated, 11 m^2K/GW [78]. Monachon and Weber find a similar effect by depositing aluminum on diamond that has undergone various surface treatments. They find that H-terminated substrates (by hydrogen plasma) produce interfaces with higher ITR than oxygen-rich substrates (by acid treatment and by Ar:O_2 plasma), ranging from 15.4 to 18.5 m^2K/GW in the former and from 5.5 to 10.5 m^2K/GW in the latter [72]. Lyeo and Cahill measure

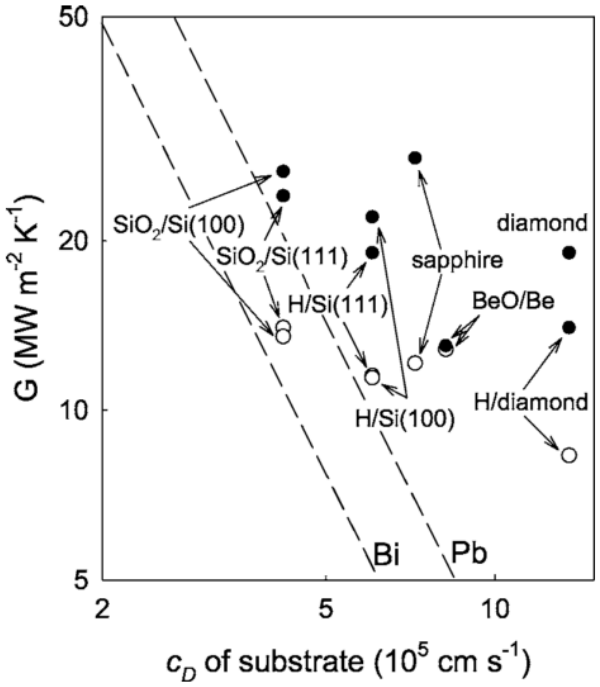

Figure 3.7: Results from Ref. [13] that shows thermal conductance of Pb (filled circles) and Bi (open circles) interfaces measured at 298 K as a function of Debye velocity of the substrates. The dashed lines represent the radiation limits of the thermal conductance for interfaces with the respective films. In all cases, the presence of an oxide layer increases conductance (decreases resistance) through the interface. Reprinted figure with permission. ©2006 by the American Physical Society.

the interfacial thermal resistance of lead and bismuth thin films evaporated onto silicon(100), silicon(111) and diamond. They prepare both silicon substrates by either HF rinse or thermal oxidation resulting in about 6 nm SiO_2. Even with such a large oxide layer they find decreased ITR across the metal-silicon interfaces that include a thermal oxide when compared to the ITR through the hydrogen terminated substrates (Fig. 3.7). They also find that ITR into diamond substrates is reduced by acid treatment of the substrate versus hydrogen plasma treatment [13].

Conversely, others find the opposite relationship between hydrogen and oxygen functionalization. Hopkins *et al.* evaporate aluminum onto silicon substrates (single crystal (100), n-type with resistivity 1 ohm cm) that are all etched in BOE, roughened

for various times in TMAH, and then allowed to regrow a native oxide. Half of the samples are then re-etched in BOE just before aluminum evaporation. For all sets of samples, ITR is smaller in the samples with H-terminated interfaces when compared to those with native oxide present [79]. Hsieh *et al.* also find that oxidized surfaces, in this case of SiC substrates, lead to higher thermal resistance. Aluminum is sputtered onto SiC substrates that have a native oxide as well as substrates that have been heated to 1300 K to remove the oxide layer, and then measured with TDTR. They find that the ITR is increased from 5 to 18 m^2K/GW with the inclusion of a native oxide termination, which they speculate is due to the native oxide being weakly bound to the SiC substrate, creating a weaker interface. They also show, by transferring graphene onto substrates with various thicknesses of native oxide, that additional oxide thickness slightly increases ITR [74].

We will show in this thesis that mechanically transferred Si-Si interfaces fabricated on oxide-terminated substrates exhibit lower ITR than those fabricated on hydrogen-terminated substrates. We attribute this effect to the increased bonding strength of the oxide interface.

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Chapter 4

Measurement

We use the 3ω technique to measure the thermal resistance through the plane of very thin silicon-silicon interfaces. The original technique, used to measure thermal conductivities of bulk materials, was first described by Cahill and Pohl [91], and was later extended to measure thermal conductivities through thin films [92]. The technique uses a single metal wire to both heat the sample and measure the temperature change in the sample. An alternating current is used to heat the wire, and the temperature can be measured by monitoring the third harmonic of the voltage fluctuations in the wire. It is important to also carefully measure the amount of current used in each wire, the exact resistance of each wire, and how that resistance changes with changes in temperature.

4.1 Theory of the 3ω method

Thermal conductivity into the surface of a substrate can be directly measured using the 3ω method. We deposit a wire on the surface of our sample that will act as both a heater and thermometer. Applying a current through the wire with frequency ω

produces Joule heating at 2ω. If the heating oscillates at a period that is less than the thermal time constant of the system, the heating produces temperature oscillation and changing electrical resistance within the wire at 2ω. As $V = IR$, by measuring the voltage along the line, we can observe a voltage component at 3ω. This $V_{3\omega}$ is related to the temperature of the wire, and therefore the dissipation of heat into the substrate. Figure 4.1(a) shows a top-down view of a gold 4-probe wire used as a 3ω measurement device on a bulk silicon substrate. The AC current is applied through the outer contacts, and the voltage is measured by the inner two contacts.

To understand the technique [105], begin with an oscillating current through a wire deposited on the surface of a sample

$$I(t) = I_0 \sin \omega t, \tag{4.1}$$

and the Taylor expansion of resistance as a function of temperature T in the wire

$$R(T) = R_0 + \frac{dR}{dT}\Delta T + \cdots . \tag{4.2}$$

We can see that small changes in the temperature of the wire will affect the resistance of the wire.

The power dissipated by the wire is given by

$$P = I^2 R \tag{4.3}$$

and inserting our fluctuating current and expansion for resistance gives

$$P(t) = I_0^2 R_0 \sin^2(\omega t) + \cdots \tag{4.4}$$

The change in temperature in the wire ΔT will follow the power, and be dependent on some proportionality constant which we'll call α.

$$\Delta T = \alpha P \tag{4.5}$$

$$= I_0^2 R_0 \alpha \sin^2(\omega t), \tag{4.6}$$

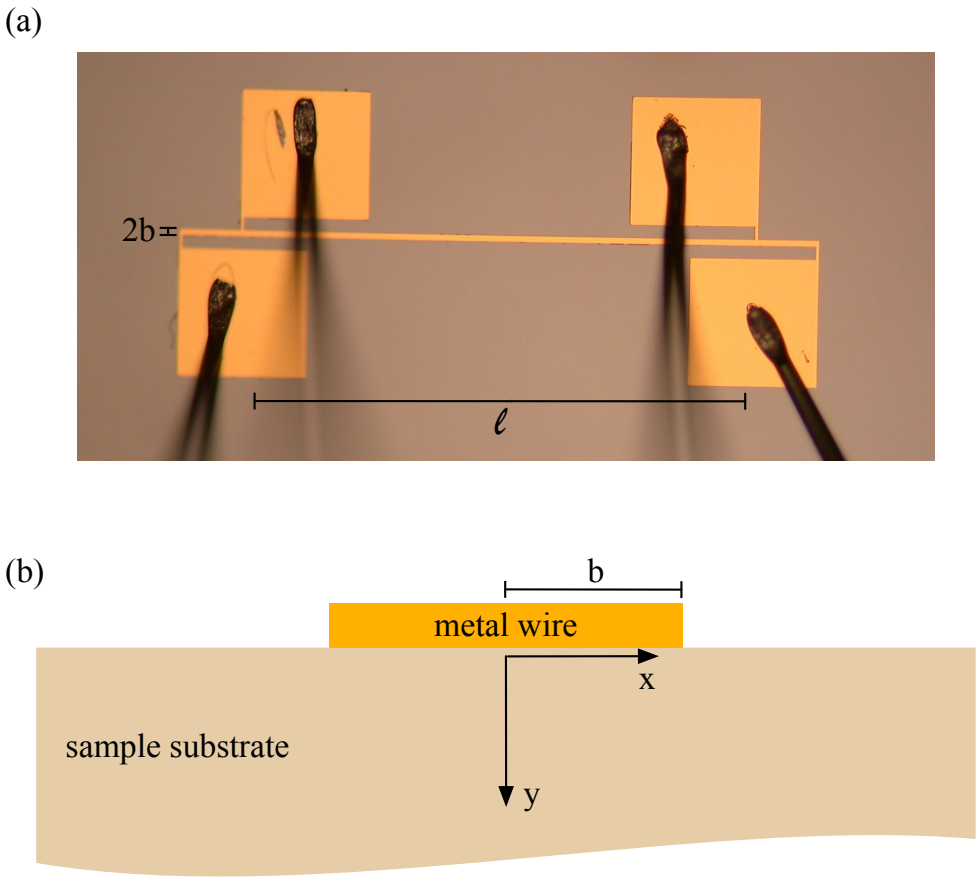

Figure 4.1: Geometry of the 3ω heater/thermometer device. (a) A top-down optical image of a gold 3ω measurement device on a bulk silicon substrate. The device is wire-bonded for measurement. The length of the wire is ℓ, the width is $2b$. (b) Cross sectional schematic diagram of the heater/thermometer. The halfwidth of the wire is b, and the coordinate axis within the sample is shown.

and by a simple trigonometric substitution

$$\Delta T = \frac{1}{2} I_0^2 R_0 \alpha (1 - \cos(2\omega t)) \tag{4.7}$$

We can see there is an effective temperature shift by a constant, and oscillations at 2ω around that point. We define the amplitude of the oscillating temperature to be

$$T' = \frac{1}{2} I_0^2 R_0 \alpha. \tag{4.8}$$

Next, insert the expression for ΔT from Eq. 4.6 into the resistance from Eq. 4.2,

giving

$$R(t) = R_0 + \frac{dR}{dT} I_0^2 R_0 \alpha \sin^2(\omega t) + \cdots . \tag{4.9}$$

We can then write

$$\begin{aligned} V(t) &= I(t)R(t) && (4.10)\\ &= I_0 \sin(\omega t)\left(R_0 + \frac{dR}{dT} I_0^2 R_0 \alpha \sin^2(\omega t)\right) && (4.11)\\ &= I_0 R_0 \sin(\omega t) + I_0^3 R_0 \frac{dR}{dT} \alpha \sin^3(\omega t) && (4.12)\\ &= I_0 R_0 \sin(\omega t) + I_0^3 R_0 \frac{dR}{dT} \alpha \left[\frac{3}{4}\sin(\omega t) - \frac{1}{4}\sin(3\omega t)\right] && (4.13)\\ &= \left[\frac{3}{4} I_0^3 R_0 \frac{dR}{dT}\alpha + I_0 R_0\right] \sin(\omega t) - \frac{1}{4} I_0^3 R_0 \frac{dR}{dT}\alpha \sin(3\omega t). && (4.14) \end{aligned}$$

The voltage will have a component that oscillates at 3ω with amplitude

$$V_{3\omega} = \frac{1}{4} I_0^3 R_0 \frac{dR}{dT}\alpha, \tag{4.15}$$

and relating that to the temperature oscillation T' from Eq. 4.8, we find that

$$\begin{aligned} V_{3\omega} &= \frac{1}{2} I_0 \frac{dR}{dT}\left(\frac{1}{2} I_0^2 R_0 \alpha\right) && (4.16)\\ &= \frac{1}{2} I_0 \frac{dR}{dT} T'. && (4.17) \end{aligned}$$

The remaining piece of the puzzle is to solve explicitly for T' by eliminating α.

Assuming the wire is infinitely long and infinitely narrow, it dissipates heat into the semi-infinite sample substrate two-dimensionally and semi-cylindrically. We know that the temperature within the sample obeys the heat equation

$$\frac{\partial T}{\partial t} - A\nabla^2 T = 0, \tag{4.18}$$

which can be solved for a long thin wire in cylindrical coordinates as [106]

$$T'(r) = \frac{I_0^2 R_0}{\ell \pi \kappa} K_0(qr) \tag{4.19}$$

where T' is the magnitude of the temperature change, $(I_0^2 R_0)$ is the amplitude of the power, ℓ is the length of the wire, κ is the thermal conductivity of the substrate, K_0 is the zeroth order modified Bessel function, q^{-1} is the thermal penetration depth, and r is the distance from an infinitely narrow heat source such that $r^2 = x^2 + y^2$. Because we are solving for the temperature in the wire, at the surface of the sample, we set $y = 0$. A cross sectional view of the setup is shown in Fig. 4.1(b).

The Fourier transform of Eq. 4.19 with respect to x gives

$$T'(k) = \int_0^\infty T'(x)\cos(kx)dx \tag{4.20}$$

$$= \frac{I_0^2 R_0}{2\ell\kappa}\frac{1}{\sqrt{k^2+q^2}}. \tag{4.21}$$

In reality, the heater has finite width, and we need to account for this. Assuming that there is even heating over the entire width of the source, we multiply in Fourier space by the width of the heater in real space. Call the center of the heater $x = 0$, and the width $2b$. Then, still in Fourier space, we have

$$T'(k) = \frac{I_0^2 R_0}{2\ell\kappa}\frac{\sin(kb)}{kb\sqrt{k^2+q^2}}, \tag{4.22}$$

and transforming back into real space gives

$$T'(x) = \frac{I_0^2 R_0}{\ell\pi\kappa}\int_0^\infty \frac{\cos(kx)\sin(kb)}{kb\sqrt{k^2+q^2}}dk. \tag{4.23}$$

Because we are interested specifically in the temperature of the heater/thermometer, we take the average of the temperature over the range $-b \le x \le b$. This yields

$$T'(x) = \frac{I_0^2 R_0}{\ell\pi\kappa}\int_0^\infty \frac{\sin^2(kb)}{(kb)^2\sqrt{k^2+q^2}}dk. \tag{4.24}$$

In the limit that the width of the wire b is much smaller than the thermal penetration depth q^{-1}, values for the integrand outside of $q < k < \frac{1}{b}$ are negligible. In this case we let

$$\frac{\sin(kb)}{kb} = 1, \tag{4.25}$$

and using the fact that

$$q^2 = \frac{i2\omega}{D} \tag{4.26}$$

where D is the thermal diffusivity, we solve the integral numerically as [105]

$$\int_0^\infty \frac{\sin^2(kb)}{(kb)^2\sqrt{k^2 + \frac{i\omega C_p}{\kappa}}}dk = -\frac{1}{2}\ln(\omega) + C_0 \tag{4.27}$$

where

$$C_0 = -\frac{1}{2}\ln\left(\frac{ib^2}{D}\right) + \ln(2) - 0.5772 - \frac{i\pi}{\kappa}. \tag{4.28}$$

Finally, we have

$$T'(x) = \frac{I_0^2 R_0}{\ell\pi\kappa}\left(-\frac{1}{2}\ln\omega\right) + C, \tag{4.29}$$

and

$$\begin{aligned} V_{3\omega} &= \frac{1}{2}I_0\frac{dR}{dT}T' && (4.30)\\ &= \frac{1}{2}I_0\frac{dR}{dT}\left(\frac{I_0^2 R_0}{\ell\pi\kappa}\left(-\frac{1}{2}\ln\omega\right) + C\right) && (4.31)\\ &= -\frac{I_0^3 R_0\frac{dR}{dT}}{4\ell\pi\kappa}\ln(\omega) + C. && (4.32)\end{aligned}$$

Differentiating Eq. 4.32 with respect to $\ln(\omega)$ [91] we have

$$\frac{dV_{3\omega}}{d\ln\omega} = -\frac{I_0^3 R_0\frac{dR}{dT}}{4\ell\pi\kappa}. \tag{4.33}$$

Solving for κ, we are finally left with

$$\kappa = -\frac{I_0^3 R_0\frac{dR}{dT}}{4\ell\pi\kappa}\frac{d\ln(\omega)}{dV_{3\omega}}. \tag{4.34}$$

By plotting the 3ω voltage against the log of the frequency ω, and carefully measuring the constants I_0, R_0, and $\frac{dR}{dT}$, we can easily calculate the thermal conductivity of the sample substrate.

Figure 4.2 shows the generalized expected relationship between $V_{3\omega}$ and $\ln(\omega)$, a negatively sloped linear curve. The negative slope results in a positive value derived for κ.

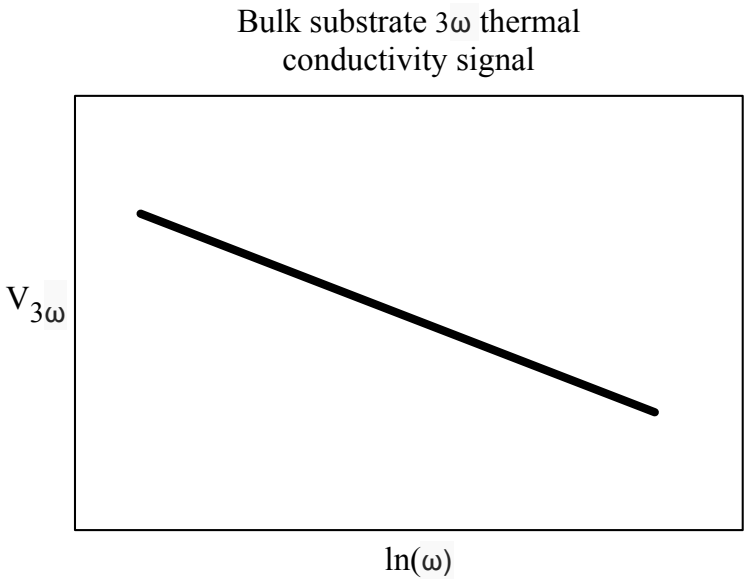

Figure 4.2: The graph shows the generalized expected relationship of the third harmonic voltage measured through a wire being heated by an AC current at frequency ω.

4.2 3ω method applied to thin films and membranes

Thin films and membranes, which generally produce a small thermal resistance compared to that of the bulk sample substrate, can be treated as one-dimensional conductors of heat so long as the width of the heater/thermometer wire is much larger than the thickness of the surface structure, as illustrated in Fig. 4.3. In that case, the effect is a frequency independent temperature oscillation in addition to the temperature change we've already derived for the substrate. The total change in temperature in the wire will be [92]

$$T'_{total} = T'_{substrate} + T'_{membrane}. \tag{4.35}$$

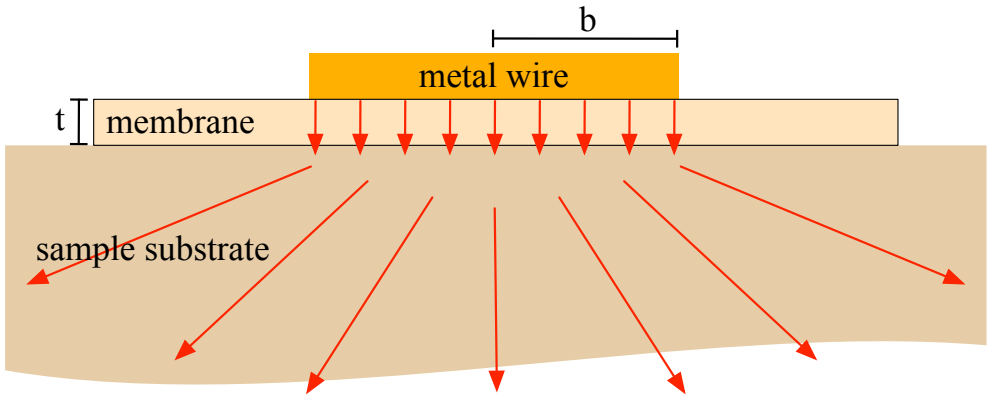

Figure 4.3: Cross sectional geometry of the 3ω device on a nanomembrane sample. The membrane thickness is t. Heat flow, as illustrated by the red arrows, is one dimensional through the thin membrane structure, and two dimensional into the semi-infinite bulk substrate.

The heat equation, given by Eq. 4.18, can be solved in the one dimensional case of heat flow through the membrane as

$$T'_{membrane} = \frac{I_0^2 R_0}{\ell \kappa_m} \frac{t}{2b} \tag{4.36}$$

where κ_m is the effective thermal conductivity of the nanomembrane, and t is the membrane thickness, as shown in Fig. 4.3.

Note, however, that the geometric factors in Eq. 4.36, along with the effective membrane thermal conductivity κ_m, yield the thermal conductance G of the membrane:

$$T'_{membrane} = \frac{I_0^2 R_0}{\ell \kappa_m} \frac{t}{2b} = \frac{I_0^2 R_0}{G}. \tag{4.37}$$

We then recall from Eq. 4.17, applied to just the effect of the membrane now, that

$$V_{3\omega} = \frac{1}{2} I_0 \frac{dR}{dT} T'_{membrane} \tag{4.38}$$

$$= \frac{1}{2} I_0 \frac{dR}{dT} \frac{I_0^2 R_0}{G} \tag{4.39}$$

$$2 \frac{V_{3\omega}}{I_0^3 R_0 \frac{dR}{dT}} = \frac{1}{G}. \tag{4.40}$$

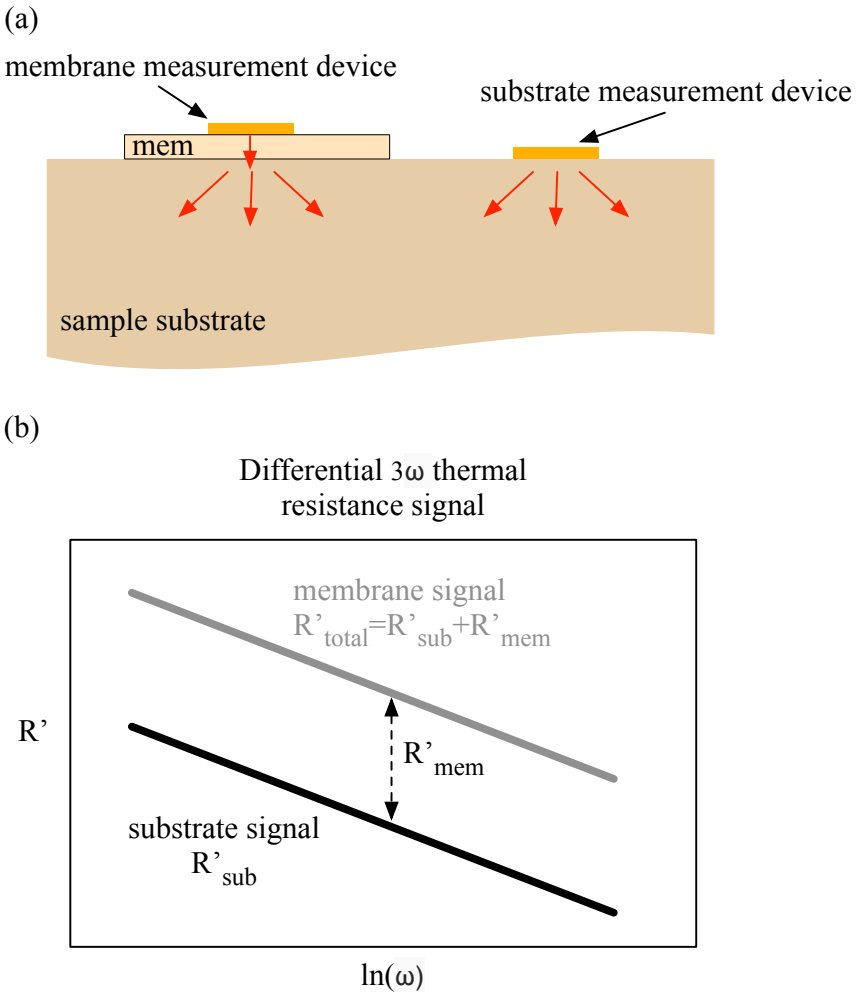

Figure 4.4: Schematic experimental setup and generalized measurement results from the differential 3ω technique. (a) Cross section of two measurement devices, one measuring directly into the substrate and the other measuring through the membrane structure in series with the substrate. (b) Because the membrane device sees the thermal resistance of the membrane structure in series with the substrate resistance, the difference in the two signals yields these thermal resistance due solely to the membrane structure.

We can see that the thermal resistance of a membrane, the reciprocal of the conductance, can be measured by inspecting the added $V_{3\omega}$ signal due to the membrane,

$$R_{thermal} = 2\frac{V_{3\omega}}{I_0^3 R_0 \frac{dR}{dT}}, \tag{4.41}$$

and importantly, that the added temperature rise due to this thermal resistance is independent of ω.

This frequency independent component of $V_{3\omega}$ measured through a thin membrane or film means that we can experimentally deduct the thermal resistance of the thin surface structure by using a differential method. Measuring the 3ω voltage directly into the substrate, as well as through the membrane in series with the substrate, allows us to take the difference of the signals and attribute it directly to the membrane structure. In effect, we are measuring and then subtracting $T'_{substrate}$ from Eq. 4.35, resulting in $T'_{membrane}$.

Figure 4.4 illustrates the experimental setup necessary to conduct this measurement, as well as what the expected results will look like. Note that in Fig. 4.4 we plot R', which is the $V_{3\omega}$ signal normalized for the specific properties of each measurement device, defined as

$$R' = \frac{V_{3\omega}}{I_0^3 R_0 \frac{dR}{dT}}. \tag{4.42}$$

4.3 Notes about the application of the differential 3ω method

There are several experimental considerations that need to be satisfied when applying the 3ω method to nanomembrane samples. All of them relate to making sure we are measuring accurately the intended domain within the sample.

First, as mentioned previously, the measurement device needs to have appropriate dimensions. The width of the heater/thermometer wire, $2b$ in the previous derivation and figures, has to be large compared to the thickness of the nanomembrane structure t to ensure that the one-dimensional heat flow assumption is valid. The length ℓ of the wire must be long compared to the width to ensure that the wire looks like an infinitely narrow line to the semi-infinite substrate, which results in two-dimensional heating.

Table 4.1: Thermal penetration depths q^{-1} for various frequencies ω. The thermal penetration depth must be much larger than the thickness of any surface structure, as well as less than the overall thickness of the substrate.

frequency ω (Hz)	$\ln(\omega)$	penetration depth q^{-1} (μm)
2.7	1	1530
7.4	2	928
20.1	3	562
54.6	4	341
148	5	207
403	6	125
1097	7	76
2981	8	46
8103	9	28
22,027	10	17
59,874	11	10.3

The range of the frequency ω used also requires careful consideration. The thermal penetration depth q must be much larger than the thickness of the membrane structure t in order to ensure the measurement probes well into the substrate. As described in Eq. 4.26, the thermal penetration depth is dependent on the material being probed, but also the frequency being used. The depth of q^{-1} should also be less than the overall thickness of the sample being measured, so that all components of the signal are attributable to the well-controlled sample. If q^{-1} is too large, the measurement will probe all the way through the sample substrate, breaking the as-

sumption that the substrate is semi-infinite. Table 4.1 shows the thermal penetration depths in silicon as a function of ω.

4.4 Experimental setup

The 3ω method, at it's core, is a delicate temperature control experiment. As such, careful control must be used to manage and measure small temperature variations throughout the experiment.

A previous 3ω setup, used the Physical Properties Measurement System (PPMS) by Quantum Design to control sample temperature and measure dR/dT of the measurement device. The PPMS is a cryostat, good at controlling low temperatures, but not designed to carefully manipulate temperatures around room temperature. Also, the sample space within the PPMS is under vacuum during measurements, meaning all thermal sinking of the sample was done by physical contact through the sample mount and electrical leads. We determined that within this system, the temperature control of our sample was ineffective. By bringing the sample and accompanying staging and wiring out of the cryostat dewar of the PPMS we were able to markedly improve the experimental setup.

The 3ω experimental sample space is now housed in a Tenney Junior Compact Temperature Test Chamber, rated for use from -75°C to +200°C with a control tolerance of $\pm$0.3°C. The Tenney Junior can be seen in Fig. 4.5. The chamber is useful as a bench top system that permits straightforward electrical access to a temperature controlled environment.

Compared to the vacuum space of the PPMS, the Tenney Junior offers three main benefits. First, besides housing a large sample space with ample access, the Tenney Junior is designed to carefully control temperatures in the range we use in

Figure 4.5: Picture of the 3ω experimental setup. The large box on the right, labeled SPX, is the Tenney Junior Compact Temperature Test Chamber. On the left, an instrument rack houses an Agilent 33250A waveform generator, an HP infinium oscilloscope, and four Signal Recovery 7265 lock-in amplifiers. The three homemade electrical boxes between the instruments and sample chamber allow for electrical breakout, switching, and house a series of unity gain operational amplifier circuits.

this experiment, around room temperature.

Second, the temperature in the chamber is controlled by heating and cooling elements which monitor and adjust air temperature. In the PPMS the sample was in a vacuum chamber and relied on physical contact for heat sinking. Our setup in the Tenney Junior uses a copper sample stage with commercially available copper heat sink fins, as seen in Fig. 4.6 in order to establish a thermal mass with well defined temperature. To this we attach the sample mount, which is a printed circuit board (PCB). By running the electrical connections to the sample back and forth across the PCB before they reach the sample, as seen in Fig. 4.7, we guarantee that the thermal connections made through these traces are properly heat sunk to the inside of the

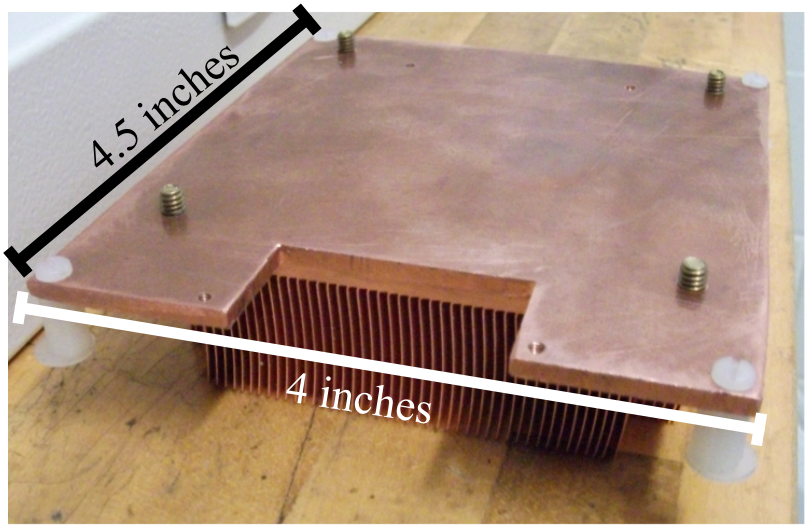

Figure 4.6: Side-on view of the copper sample stage. A CPU heat sink is attached to the bottom of a copper plate to provide the fins. Teflon posts ensure the stage is isolated electrically and thermally from the chamber walls.

chamber. We are not drawing heat from the sample out of the chamber through the leads.

Third, we can now conduct the entire measurement *in situ*. The previous setup required that we did the frequency dependent portion of the measurement, determining $\frac{d\ln(\omega)}{dV_{3\omega}}$, in a bench top setup, which was susceptible to variations in the room temperature. Then the temperature calibration of $\frac{dR}{dT}$ was done in the vacuum chamber of the PPMS, meaning the sample had to be moved and re-mounted to complete the measurement. Using the Tenney Junior we can now do both of these necessary components of the measurement without disturbing the sample.

Within the Tenney Junior sample chamber we constructed a suspended shelf, which can be seen in Fig. 4.8. The sample stage sits on the shelf on Teflon risers, keeping the sample stage in thermal and electrical isolation from the chamber walls.

The measurement setup has 4 identical measurement channels in parallel, as shown in Fig. 4.9. Each channel has an op-amp current source, which regulates the current

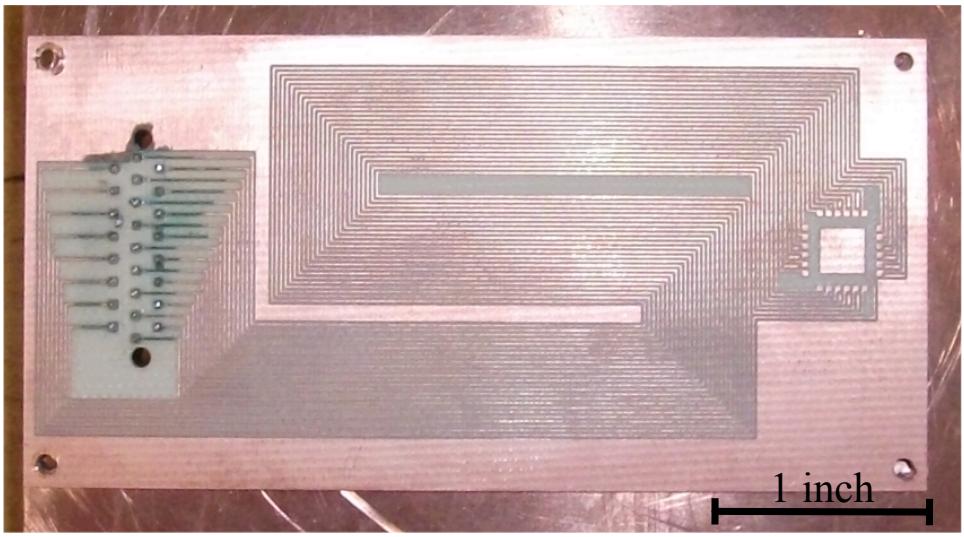

Figure 4.7: Top view of the sample mount PCB. The traces, which provide electrically access from the pins on the left to the sample space on the right, run back and forth in order to allow for good heat sinking to the environment.

Figure 4.8: Interior of the Tenney Junior chamber, including the shelf and sample stage, both made in house. There are two sets of mounting brackets, upper and lower. In this picture the shelf is mounted in the upper brackets.

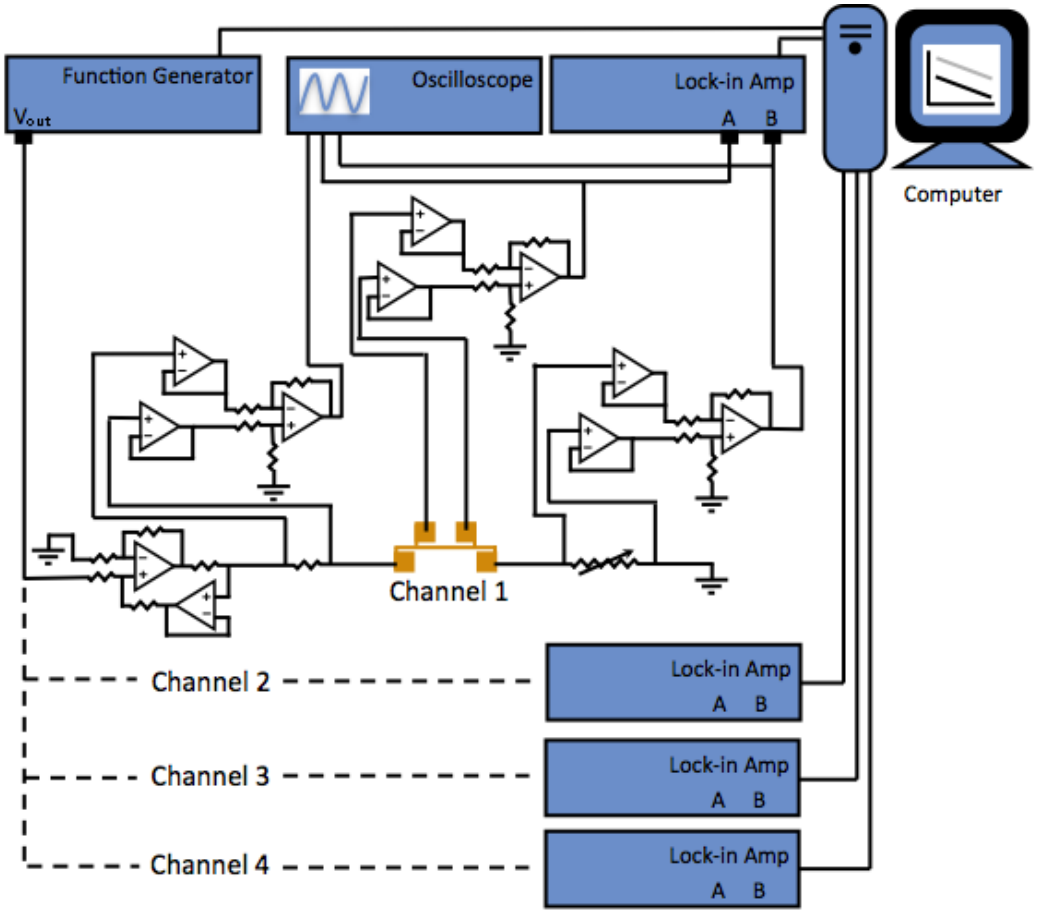

Figure 4.9: Experimental instrument setup diagram. The setup has four identical channels in parallel. Each channel consists of an op-amp current source, followed by three unity gain differential amplifiers. The differential amplifiers measure the voltage across a thin-film resistor, the 3ω device, and a potentiometer, all in series.

regardless of the exact load. Next is a 20 Ω resistor R_{ser}, used to monitor the current in each channel. The voltage across this series resistor is measured by a unity gain differential amplifier, with current buffers on each input to ensure no leakage of current. The output voltage of this amplifier can be viewed and analyzed on the oscilloscope. The 4-probe device used for the measurement, also with a unity gain differential amplifier, is next. The voltage across the device V_0 can be viewed and analyzed on the oscilloscope, but is also used as the A input of the lock-in amplifier. Lastly, another unity gain amplifier measures the voltage V_{pot} over a potentiometer

(variable resistor), which we balance with the 1ω signal over the measurement device and use as the B input to the lock-in amplifier, to cancel the A-B signal at the fundamental frequency. The output voltage of the function generator is also fed to the reference input of each lock-in amplifier.

The 4 lock-in amplifiers and the function generator are controlled and read by a LabVIEW program running on an adjacent computer.

4.5 Testing the temperature control

We conducted extensive testing to verify the control of the temperature of the sample. We used two resistance temperature detectors (RTDs), thin film resistors with known temperature dependancies, both in 4-probe configurations. First, we placed both RTDs directly next to each other on the copper stage so that they would have the same temperature. The positioning of the RTDs is visible in Fig. 4.10(a), as labelled by the primary RTD position and 2nd RTD, together on stage. We then swept the operating current of both RTDs to find a point where they were in agreement. After setting the appropriate current for each, we swept the temperature in the chamber. The measurements for both RTDs were in good agreement over the entire range. The results are seen in Fig. 4.10(b). The 2nd RTD is significantly less massive than the primary RTD, so we can see that it reacts more quickly to temperature variations, but that is expected. We then moved one of the RTDs to the far side of the stage, so that the temperature sensor were now on across the stage from each other. Again, as seen in Fig. 4.10(c), the measurements were in good agreement and almost identical to the initial sweep, indicating that there is no thermal gradient across the stage.

Next we attached the 2nd RTD to the sample space while leaving the primary RTD mounted directly to the stage. In Fig. 4.10(d) we can see that the sample space

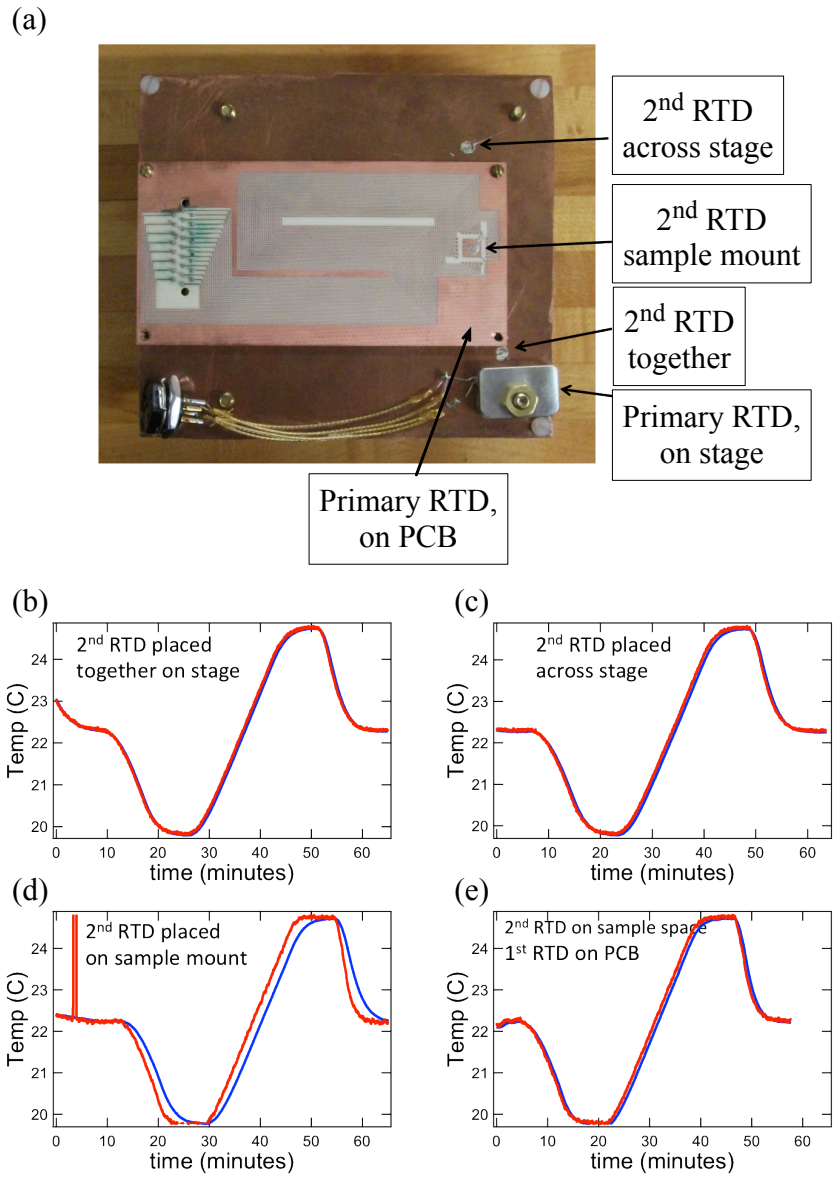

Figure 4.10: Diagram of temperature control measurement positions and results. (a) The sample mount PCB is attached to the sample stage, and the primary and 2nd RTD were placed at various points on both the stage and PCB, as indicated. (b) Temperature sweeps of the primary RTD, in blue, and 2nd RTD, in red, when both RTDs were placed together on the sample stage. (c) Temperature sweeps of the primary (blue) and 2nd (red) RTDs when they were placed across the stage from each other. (d) Temperature sweeps with the 2nd RTD placed on the sample mount at the sample space. (e) Temperature sweeps with the primary RTD placed on the PCB, and 2nd RTD on the sample mount.

and the stage are not in equilibrium. The 2nd sensor displays two characteristics worth noting—it reacts significantly faster and has sharper features than the RTD on the stage, showing that the thermal mass of the copper stage slows and dampens the reaction to temperature changes. This, however, is not a negative trait. The large thermal mass that is the copper sample stage acts to dampen any quick temperature changes that the sample might experience, stabilizing the steady state and ramping temperatures.

We next moved the primary RTD to an adjacent position on the PCB sample mount, and the readings come back into good agreement, as seen in Fig. 4.10(e). The metal top of the PCB is isolated from the thermal mass that is the copper stage by the PCB dielectric, and we can see that in that isolated position the reaction to temperature changes of the air is faster than if in direct thermal contact with the stage.

The Tenney Junior has two sets of mounting bracket within the sample space. The shelf is mounted in the upper brackets in Fig. 4.8, and the lower brackets are also visible. We moved the stage to a vertically lower position in the Tenney Junior chamber and again ran a temperature sweep. The results of this sweep, compared to the analogous sweep in the upper position, are seen in Fig. 4.11. We observed that in the lower position the RTDs were slower to react to programmed changes in the temperature than in the upper position, as can be seen by the more rounded curves in the results and a longer time to reach a steady state at the maximum temperature. We will use the upper brackets for our experiments.

Last, we ran several sweeps at varying temperature ramp rates to determine how closely the RTDs mirror the intended sweeps as controlled by the chamber. All results are visible in Fig. 4.12. We see that for sweeps of 1.0°C/min or greater the chamber has trouble regulating the ramp speed, and the RTDs don't maintain a consistent

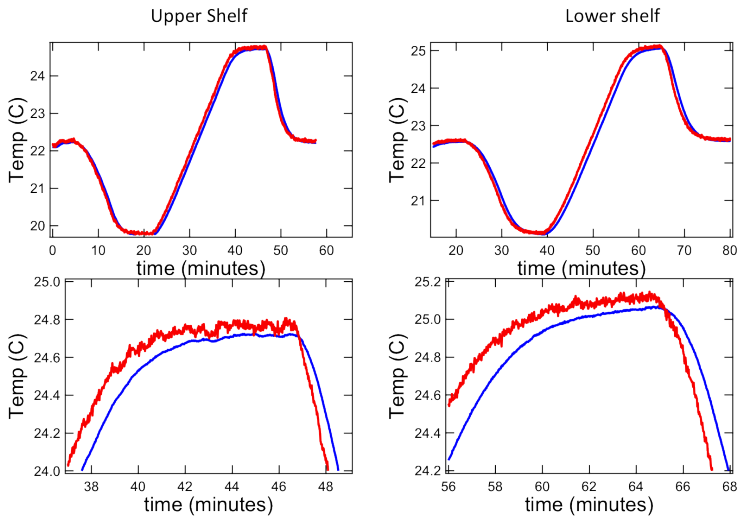

Figure 4.11: Temperature control measurements in upper versus lower positions within the sample chamber. The primary RTD (blue) and 2nd RTD (red) are both mounted on the PCB. The second scans for both shelf positions are zoomed views of the ramp towards the upper temperature limit.

rate of change. A sweep at 0.7°C/min shows agreement to the programmed ramp rate within 1%, and at 0.5°C/min within 0.2%.

4.6 Measurement procedure

Each sample prepared for testing contains many 4-probe 3ω devices, as can be seen in the next chapter in Fig. 5.4. For measurement, the sample is attached to the PCB sample mount using a small dab of silver paste. A short amount of time is necessary for the silver paste to dry and harden, and then multiple devices are electrically connected to the sample mount by wire bonding. The sample mount is attached to the stage, the stage is placed on the shelf, and the PCB is connected to the instrument setup through the breakout box.

Each lock-in is set to measure the 1ω signal of the A-B input, the difference of the measurement device and the potentiometer in each channel. By zeroing each 1ω

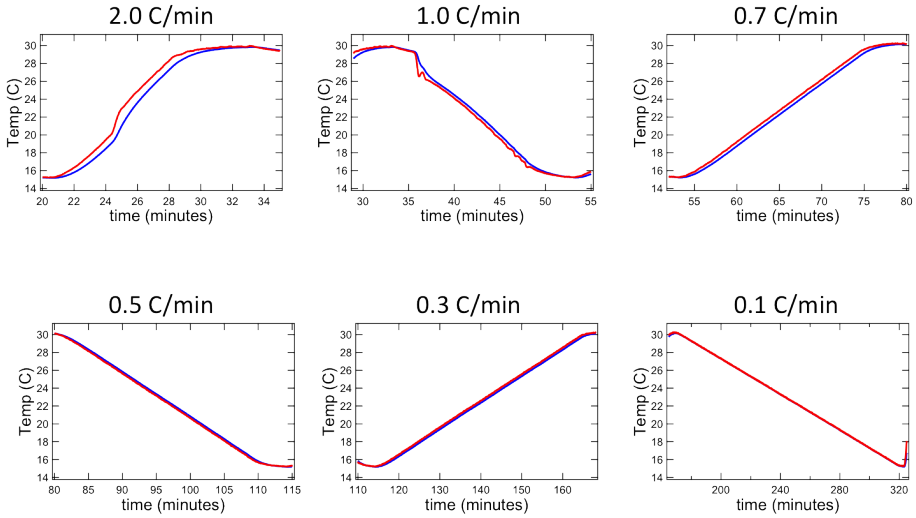

Figure 4.12: Temperature readings from the primary (blue) and 2nd (red) RTDs for varying ramp rates. For rates greater than 1°/sec, the Tenney Junior has trouble maintaining a steady ramp. For ramp rates slower than that, however, the RTDs show linear ramps and there is negligible difference between the results.

signal, we match the potentiometer resistance to R_0 of each device.

After each device is balanced, the lock-ins are reconfigured to measure the third harmonic of the A-B signal. To reduce noise in this measurement by increasing averaging, we use a long time constant of 5 seconds.

Once each device is balanced and configured to measure the 3ω signal, the function generator is set to sweep from $e^{6.5}$ Hz ($\approx$ 665 Hz) to $e^{8.0}$ Hz ($\approx$ 2980 Hz) and back. Sweeping frequency both directions is done to ensure stability and reproducibility. While the frequency is swept, the lock-ins record the third harmonic of the voltage, $V_{3\omega}$, and the phase shift θ of the third harmonic of the voltage.

Following the frequency sweeps, each channel is monitored using the oscilloscope to measure the voltage across the device V_0, the potentiometer in series V_{pot}, and the 20 Ω resistor in series V_{ser}, along with the standard deviations of each voltage. The series resistor is used as a means of measuring exactly the current across each device.

Finally, each device is reconnected to the lock-in across the A-B input, bypassing

the rest of the measurement setup. The internal oscillator of each lock-in is set to 5V and a 1 MΩ resistor is used in series to measure the resistance of each device as the Tenney Junior chamber temperature is stepped from 10°C to 50°C in 10°C increments.

Using this process, we measure all the parameters necessary to compute the thermal conductivity of the sample substrate, as well as the thermal resistance through any membrane and thin film structure.

4.7 Computing the results

We first compute $V_{3\omega}^{real} = V_{3\omega}\cos(\frac{\pi}{180}\theta)$. Then $\frac{dV_{3\omega}^{real}}{d\ln(\omega)}$ is computed in Igor Pro.

$I_0 = V_{ser}/R_{ser}$ and $R_0 = V_0/I_0$ are computed.

The temperature dependence of the wire, $\frac{dR}{dT}$, is calculated by averaging the resistance of the measurement device, $R_0 = \frac{V_0}{5\mu A}$, for 100 seconds at each temperature step, after the resistance has equilibrated to the temperature of the chamber. Igor Pro is used to fit the slope $\frac{dR}{dT}$ to the six resultant data points.

To ensure that each device is thermally sunk to the chamber environment, and that all devices are acting appropriately, we compute the resistance ratio $\frac{1}{R_0}\frac{dR}{dT}$ for each device.

The thermal conductivity of the silicon substrate, κ, can be computed for each device.

$$\kappa_{sub} = \frac{I_0^3 R_0 \frac{dR}{dT}}{4\pi\ell\left(\frac{dV_{3\omega}^{real}}{d\ln(\omega)}\right)} \tag{4.43}$$

Next, define $R' = \frac{V_{3\omega}^{real}}{I_0^3 R_0 \frac{dR}{dT}}$ for each device, which varies linearly with $ln(\omega)$. Then define $\bar{R}$ as the mean of each R' over the frequency range. We use $\bar{R}$ as the magnitude of the total signal from each device.

Until now each device on each sample has been treated separately. Next, we average the signal from the devices in each measurement scan that lay directly on the substrate, and also the devices that lay on top of the membrane stack.

For a single measurement, we compute

$$R'_{sub} = \frac{1}{N_{sub}} \sum_{N_{sub}} \bar{R}_{sub} \tag{4.44}$$

$$R'_{total} = \frac{1}{N_{mem}} \sum_{N_{mem}} \bar{R}_{mem} \tag{4.45}$$

where N_{sub} and N_{mem} are the number of substrate and membrane devices in a single measurement scan, typically two each.

We can then find thermal resistance of the membrane structure R'_{mem} between membrane and substrate by considering the difference between R'_{total} and R'_{sub}. Thermal resistances are commonly reported in units of [m^2K/GW] for ease of comparing resistances between samples of different geometries, and so the differential thermal resistance between substrate devices and membrane devices is given as

$$R_{mem} = 2(R'_{total} - R'_{sub})(\ell \cdot 2b). \tag{4.46}$$

Finally, in the case that we have multiple measurements of a single sample type, we compute the mean and standard deviation of the results of those measurements.

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Chapter 5

Si-Si interfaces

Individual materials interfaces are both the real and the conceptual building blocks of larger systems, yet in spite of their critical importance, the majority of previous ITR measurements have focused on metal-nonmetal interfaces, which lend themselves to measurement by thermoreflectance [3]. Such metal-nonmetal interfaces typically have low ITR, with almost all values reported between 2.3 and 20 m^2K/GW [87, 66, 94, 104, 82, 68, 13, 81, 78, 79, 80, 95, 77, 76, 75, 74, 73, 93, 72, 71, 69, 70]. Recently, transfer printing of thin films and membranes has been used to create mechanically-joined interfaces, and measurements of such interfaces have yielded larger ITR values, from 15 to 50 m^2K/GW [103, 75, 12]. The membrane transfer process also enables the formation of interfaces between like materials, and mechanically-joined silicon regions have been shown to have similarly large ITRs, in the range from 30 to 110 m^2K/GW. One reason these interfaces may be as resistive as they are is that they have been between polysilicon regions in one case [104], and highly dislocated silicon regions in the other [35]. To date it is unclear whether van der Waals coupled interfaces, like those formed from membrane transfer, can exhibit low ITR.

In order to better understand the properties that determine ITR, it would be

very useful to study the thermal resistance two well-aligned, identical, single crystals. There are several key factors that partially determine the thermal resistance across an interface, including the acoustic mismatch of materials across the interface, the temperature of the interface, the bonding strength, pressure, and roughness of the interface, any interdiffusion of materials at the interface, and interfacial defects [107]. The Si-Si interface we create is a model system because it controls for so many of these factors. The interface is between two vdW-bonded crystals that have no acoustic mismatch, the temperature and pressure is well controlled, and the interface is abrupt. This leaves us with two key characteristics to consider, which we will discuss—bonding strength and roughness.

5.1 Fabrication

We create well-controlled interfaces between regions of single-crystal Si(100) by transfer printing Si NMs onto bulk Si substrates using the thermal-release tape method [108]. Bonding two identical, well-aligned Si crystals means there is no acoustic mismatch across the interface. Repeating the transfer process, we can stack two membranes on top of each other, producing two Si-Si vdW-bonded interfaces in series, and enabling a check for consistency with the results obtained from single interfaces. Because the NMs are only 300 nm thick, the interfaces are close to the surface, enabling high resolution measurement of the ITR.

Figure 5.1 shows the two interface configurations we study here: in the upper two diagrams, interfaces are formed between a pair of H-terminated Si surfaces (H-H), and in the lower two diagrams, interfaces are formed between an H-terminated surface and an oxide-terminated surface (H-ox). Hydrogen terminated surfaces are achieved in a hydrofluoric acid (HF) bath, while oxide terminated surfaces are created

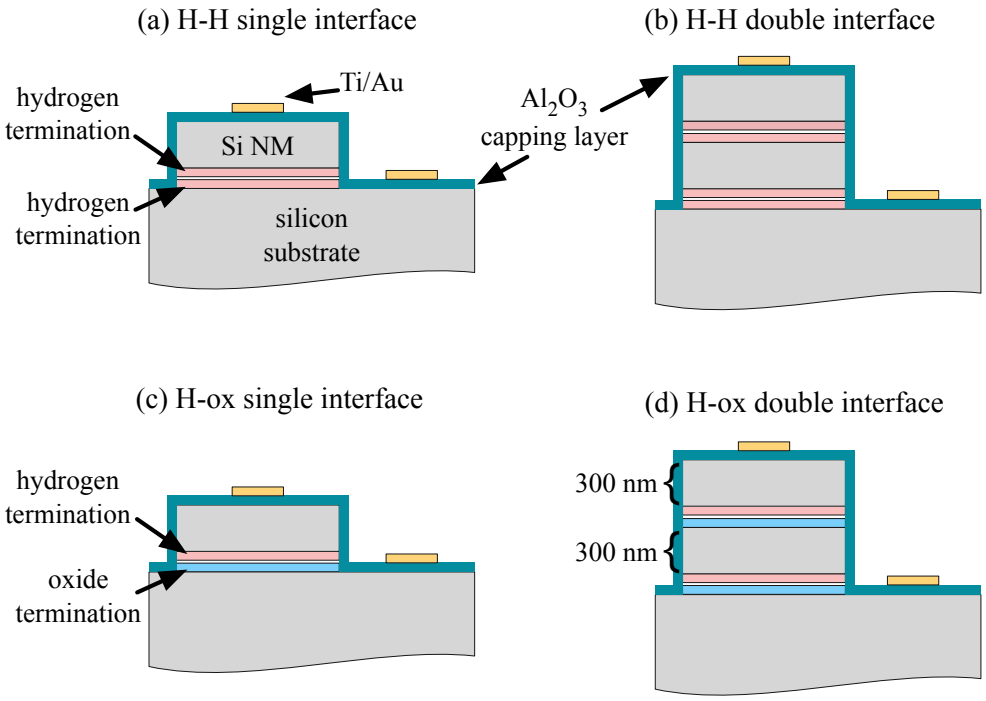

Figure 5.1: Schematic sample cross sections, not to scale. Silicon nanomembranes are mechanically transferred onto bulk silicon receiver substrates. After transfer, the samples are capped with a layer of Al_2O_3, and Ti/Au microstructures are fabricated on top. We create two types of samples—those in which the receiving surface is hydrogen terminated, and those in which the receiving surface is oxide terminated. In all cases the underside of the NMs are hydrogen terminated. (a) Cross section of a single interface H-H sample. (b) Cross section of a double interface H-H sample. (c) Cross section of a single interface H-ox sample. (d) Cross section of a double interface H-ox sample.

in piranha solution [109].

Si NMs are created from the template layer of commercially available silicon-on-insulator (SOI) (Soitec Unibond, 300nm (100) membrane layer on 400nm buried oxide, P-type 8.5-11.5 Ωcm), shown schematically in Fig. 5.2(a). Standard optical lithography techniques and reactive ion etching are used to define both the membrane area and a pattern of access holes through the template layer to the buried oxide layer. The patterned SOI is submerged in 49% hydrofluoric acid (HF) solution for 2 hours to allow diffusion of HF through the access holes and complete etching of the buried

oxide, releasing the membrane onto the donor substrate, as shown in Fig. 5.2(b). After rinsing and drying, thermal release tape (Nitto Denko, REVALPHA) is adhered to the nanomembrane surface, Fig. 5.2(c). Peeling the tape removes the membrane from the donor substrate (Fig. 5.2(d)). The membrane is then positioned and aligned over a new receiver substrate, Fig. 5.2(e), pressed into contact, and allowed to bond, Fig. 5.2(f). Heating the entire structure reduces the adhesive strength of the tape, which releases the membrane to the receiver substrate, Fig. 5.2(g). The residual adhesive left by the tape is removed by wet cleaning, Fig. 5.2(h). The process can be iterated to add more than one membrane to a stack, creating interfaces vertically in series.

Because all Si NMs come out of an HF bath shortly before transfer, the underside of the membrane is hydrogen terminated, and therefore hydrophobic, for all samples.

Receiver substrates were prepared from bulk silicon wafers from University Wafers ((100), P-type, 0-100 Ωcm). All substrates are cleaned by sonication in acetone and isopropanol, followed by piranha clean (2:1 H_2SO_4:H_2O_2, 10 minutes), and HF dip (49%, 5 seconds).

Samples with hydrophobic receiver substrates (H-H samples) are made by transferring membranes to H-terminated substrates immediately following (within 5 minutes of) the HF clean. After transfer, the samples are cleaned in piranha and HF. If only one interface is desired, the sample is piranha cleaned again to passivate the top surface. If fabricating a multiple interface sample, another membrane is transferred immediately following the HF clean.

For samples with hydrophilic receiver substrates (H-ox samples), the bare substrates are further cleaned in AZ 300T stripper, and then again piranha cleaned to produce a chemical oxide termination, after which the membranes are transferred. After transfer the samples are cleaned in AZ 300T and piranha, at which point either

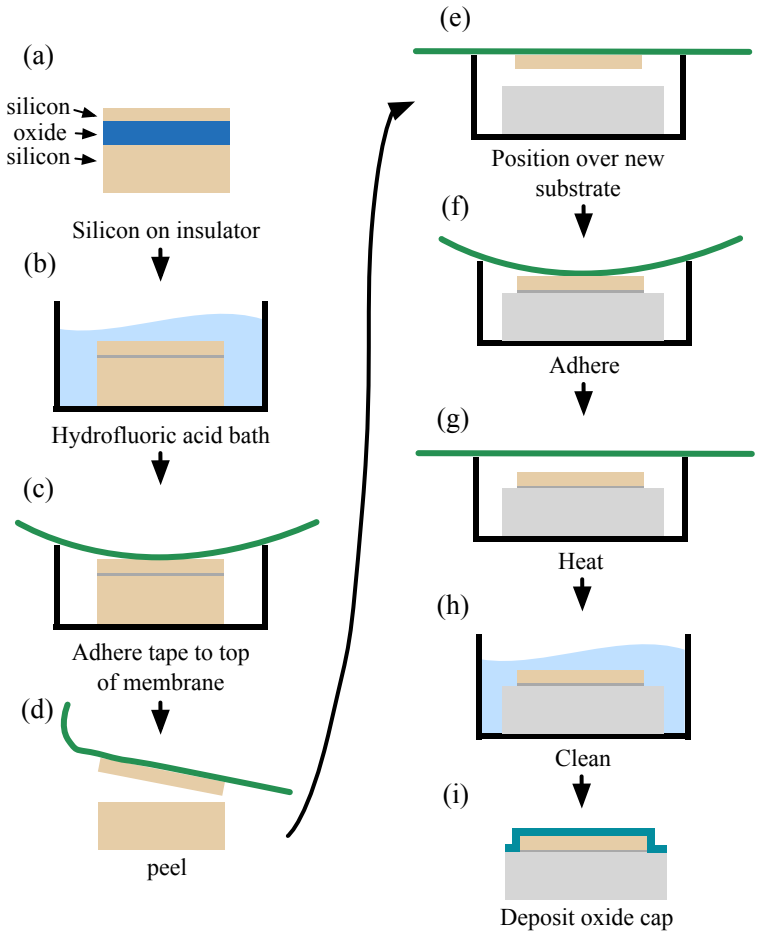

Figure 5.2: Illustration of the sample fabrication process using the thermal release tape transfer technique. (a) Silicon on insulator is patterned and (b) placed in hydrofluoric acid to etch the buried oxide layer. (c) A piece of thermal release tape is adhered to the released single crystal nanomembrane (d) and both are removed from the substrate. (e) The membrane is positioned over a new substrate and (f) brought into contact and allowed to adhere naturally. (g) Heating the entire assembly releases the tape from the surface. (h) After cleaning, another membrane can be added to the stacked by the same process. (i) When all transfer and stacking is complete, a thin layer of aluminum oxide is deposited by atomic layer deposition.

another membrane can be transferred or the stacking can be complete.

After stacking, all samples are capped with 10 nm of Al_2O_3 by atomic layer deposition (ALD), as shown in Fig. 5.2(i). During the ALD process all samples are annealed at 300°C.

All membranes in this study are transferred using thermal release tape. This technique has many benefits—it is a deterministic assembly method that allows for dry transfer, maintains the relative position of Si NMs during transfer, enables accurate control of alignment and position of transferred Si NMs by hand and eye without the need for expensive and elaborate machinery, and has a high success rate. The results of the transfer process is illustrated in Fig. 5.4(a-b), which shows that the membranes are transferred to the receiver substrate in the same alignment and positioning as they were created in the SOI.

In this work we focus on samples with one and two membranes stacked onto bulk substrates, but the thermal release tape transfer method has been used to successfully stack up to five silicon nanomembranes, creating samples with 5 interfaces in series. Figure 5.3 shows top-down dark-field optical images of the HF release hole patterns made by stacking membranes. For single membrane samples, an grid of single release holes is visible, where the area inside the small squares are the holes through the membrane, as seen in Fig. 5.3(a). Stacks of two, three, and five membranes on top of each other are shown in Fig. 5.3(b-d). The number of membranes in the sample is equal to the number of release holes visible in a single unit of the release hole grid, as shown by the dotted squares on the figure. The good alignment of release holes between membranes shows good control of rotational placement by the thermal release tape transfer method.

The thinness of the NMs mean that they are compliant over length scales larger than their thickness, but rigid on length scales much smaller than their thickness.

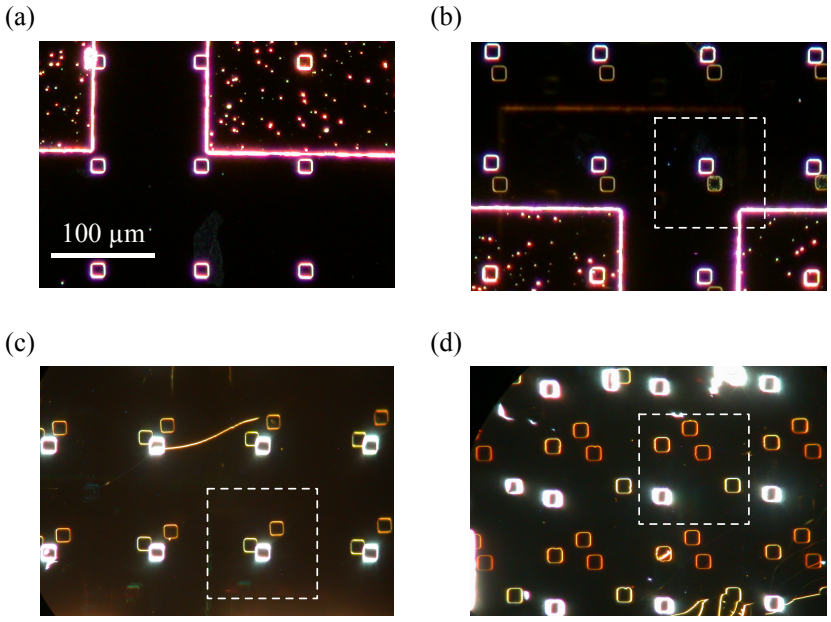

Figure 5.3: Top-down dark-field optical images of multi-membrane stacks. The small squares are HF release holes in the membrane. The number of holes per unit of the grid indicates the number of membranes stacked on top of each other. The good alignment of release holes between membranes shows good control of rotational placement by the thermal release tape transfer method. (a) A single membrane on a bulk substrate. Edges of gold wire bonding pads are also visible. (b) Two membranes, with dashed square showing the two layers of HF release holes. Again, gold wire bonding pads are visible. (c) Three membranes. (d) Five membranes.

Therefore any imperfection in the fabrication process, such as a speck of dust at the substrate-NM interface, becomes only a localized problem while the rest of the interface is unaffected.

Ti(5nm)/Au(150nm) 4-probe wires, 5 μm wide and 400 μm long, are deposited on both the oxide-covered Si substrate and the oxide-covered membrane surface using standard optical lithography and electron-beam evaporation. The result of this metallization is shown schematically in Fig. 5.4(c). Bubbling occurs in the H-ox samples during the ALD/annealing process. The metal wires are positions such that they do not lie over any bubbles. Electrical contacts are then deposited such that the wire-bonding pads lie off of the membrane, as shown in Fig. 5.4(d). Figure 5.4(h) shows a

top down atomic force microscope (AFM) image of a 4-probe device on a transferred nanomembrane.

Figure 5.5, which is the same AFM image as in Fig. 5.4(h), shows in detail the final structure of the sample, including a 3ω measurement device, the HF etch access holes, the membrane edge, and the electrical contacts. The lower inset shows the uncolored version of the same image. The upper inset shows an illustration of a double interface sample.

These devices measure the thermal resistance from the surface of the sample into the substrate. Measurements of what we call substrate devices provide a baseline, but in reality include not only the thermal conductivity of the bulk substrate, but also the resistance of several interfaces. The heating is produced in the metal wire, which has an interface with the oxide capping layer. The oxide cap, in turn, has an interface with the silicon underneath it. The important point is that the devices which measure through a single or double interface structure include each of these thermal resistances also, as well as the resistance of the interface or interfaces in series. The difference in these measurements gives us the effective thermal resistance of the single or double interface, while all other parts of the sample structure are negated.

5.2 Interfacial thermal resistance results

We determine the ITR by subtracting the results of 3ω measurements made with and without the interface of interest, enabling the isolation of the thermal resistance arising from the interface under study [92]. Because the interface is in a region of the sample where the heat flow can be assumed to be one-dimensional, the thermal resistance of the interface is added in series to the bulk Si resistivity. Since the interface

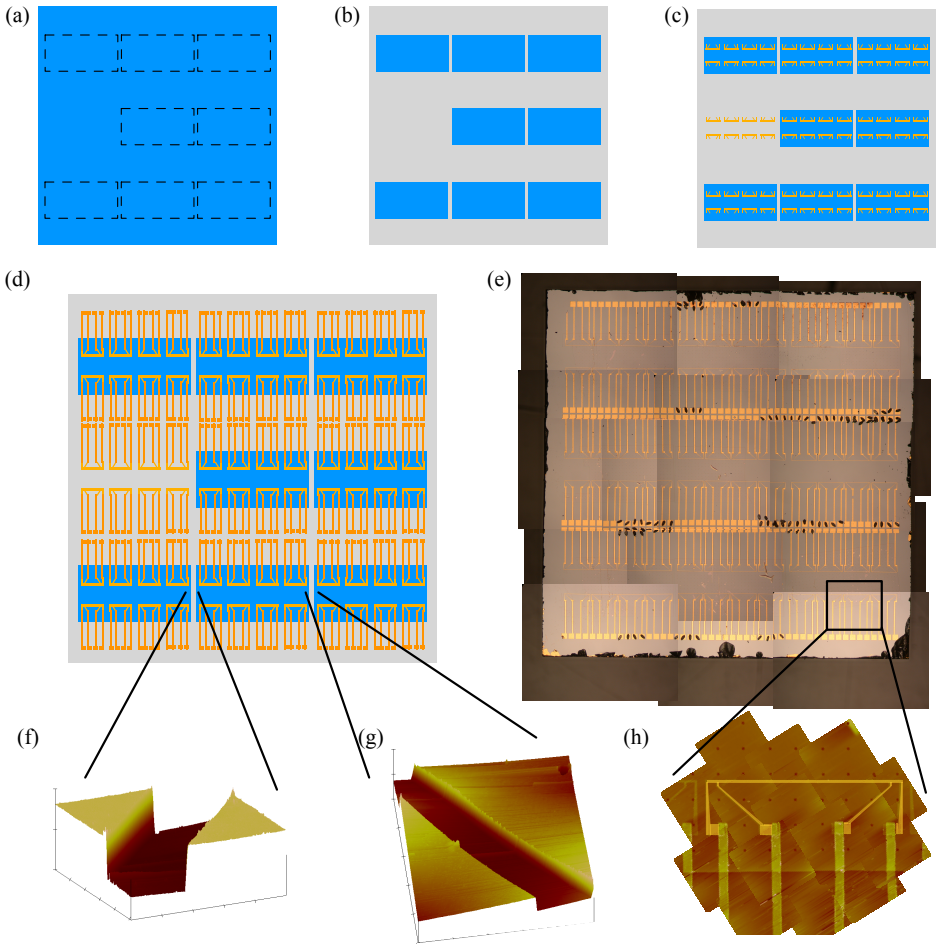

Figure 5.4: Schematic top view diagram of the membrane 3ω device fabrication, and optical and AFM images of the resultant sample. (a) Si NMs start as the template layer of a 7x7 mm piece of SOI. Here we use blue to represent the template layer, for ease of viewing. (b) Membranes are dry transferred using the thermal release tape transfer technique as illustrated by Fig. 5.2. (c) 3ω devices are fabricated by standard optical lithography and metal evaporation. (d) Electrical contacts and bond pads are fabricated in a second metallization step, also by optical lithography. (e) A finished sample. Because the NMs and substrate are both composed of Si, and because the NMs are so thin, it is very difficult to see the membranes optically. Black marks are wire bonding footprints on used devices. (f-g) 3D AFM of the region between two membranes shows clearly the alignment of the membranes and the channel created between them to the substrate. The NMs are 300 nm tall. An etch hole visible in the back corner of the second image. (h) A stitched picture of many AFM images showing a single 3ω device, which has been false colored to highlight the 4-probe measurement device.

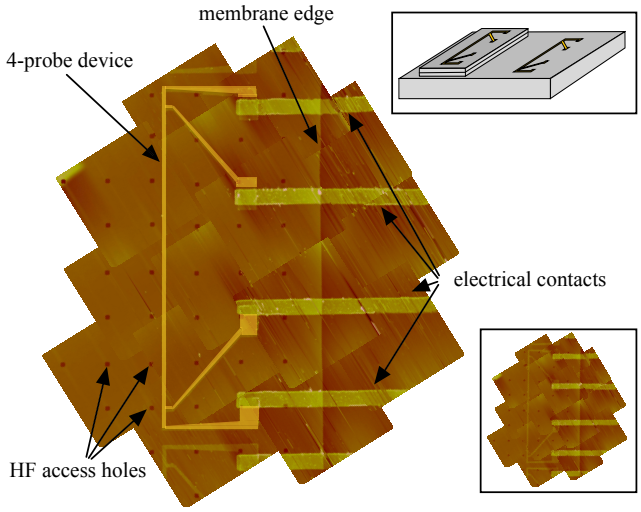

Figure 5.5: False-color AFM of a four-prove device (vertically aligned) on top of a single Si membrane. A grid of lithographically patterned release holes is visible in the image, as well as the edge of the membrane to the right (vertical), and four large electrical contacts (horizontal). The full image is made up of 17 individual scans stitched together, each separately flattened using the native NanoScope SPM 4.43r6 software. Only the 4-probe device has been false-colored. Original coloring is visible in the adjacent devices at the extreme top and bottom of the image. Lower Inset—the same image, uncolored. Upper Inset—Schematic of a two membrane, two interface sample. Analogous geometries are used for samples with a single transferred membrane. Four-probe measurements are made using the 3ω method. In order to determine the thermal resistance of the Si-Si interfaces created by mechanical transfer, measurements are made both directly on the host substrate as well as on top of the membrane stack.

is sandwiched between identical silicon crystals, the thermal resistance we measure through the membrane structure arises out of the weak van der Waals bonding at the interface.

Geometric and frequency-dependent limitations are considered when designing the wires and measurement procedure. Care is taken that the frequency regime used does not probe through the bottom of the substrate at low frequencies, but also probes well past the depth of the NM structure at high frequencies. We use the frequency range from 665 Hz to 2980 Hz. Also important is that the width of the wires used is

much larger than the thickness of the SiNM stack. We use wires 5 μm wide and 400 μm long.

For each 4-probe device, an AC current is applied through the wire with amplitude I_0 and a swept frequency ω. The frequency dependence of the third harmonic of the voltage along the device $V_{3\omega}$ is measured, as well as the electrical resistance of the device R_0. $V_{3\omega}$ and R_0 are measured with the temperature held carefully at 295°K. The temperature dependence of the resistance in the wire $\frac{dR}{dT}$ is measured in the linear regime between 283°K and 323°K.

Our setup is capable of measuring up to four 4-probe devices at a time. In any measurement scan we measure at minimum one device directly on the substrate and one device that probes the membrane stack. $R' = V_{3\omega}/\left(I_0^3 R_0 \frac{dR}{dT}\right)$ is computed for each device. If there are multiple devices of the same type in a single measurement run their values at each frequency point are averaged, and the difference between the two types of devices (R'_{total}-R'_{sub}), on the membrane stack and on the substrate, is then found by taking the difference of the mean signals. Finally, the differential thermal resistance is determined as $R_{mem} = 2(R'_{total}\text{-}R'_{sub})(\ell \cdot 2b)$, where ℓ is the length of the wire and $2b$ is the width.

Figure 5.6 shows the differential thermal resistance results for many single- and double-interface H-H and H-ox samples. Each marker represents a single measurement, and measurements for each type come from at least three distinct samples. The mean value of the resistance for each type of sample is given by the solid line: brown for the H-H samples, and blue for H-ox. The shading represents one standard deviation for each sample type. The measured thermal resistance in H-H samples is 8.8±4.4 m^{2}K/GW for a single interface, and 19.0±2.9 m^{2}K/GW for two interfaces in series. The thermal resistance for H-ox is 2.3±1.5 m^{2}K/GW for a single interface, and 6.6±1.7 m^{2}K/GW for two interfaces in series.

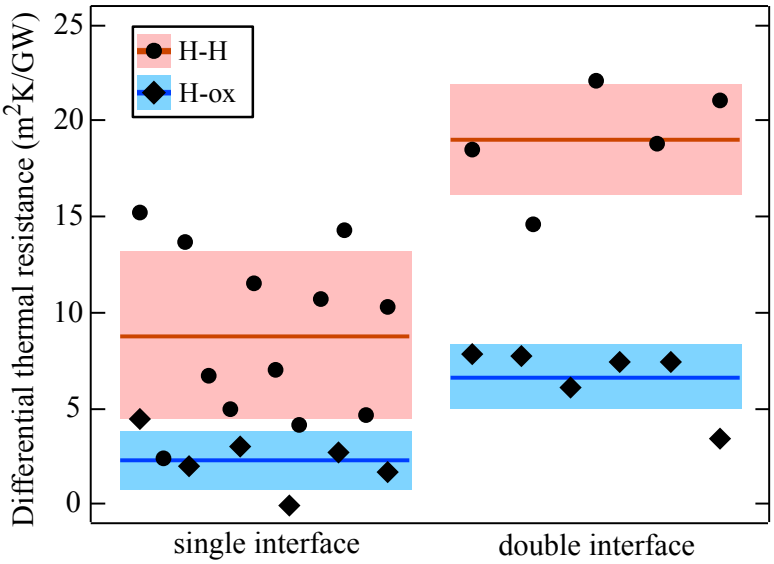

Figure 5.6: Differential thermal resistance values of single and double interface nanomembrane sample structures. H-H interface values are given by circles, H-ox values by diamonds. Each marker represents a single independent measurement run. The mean value of each type of sample is given by the solid line, the standard deviation is given by the shaded region. For both interface types, the samples with two interfaces are twice as resistive as the samples with a single interface.

The double interface samples produce a differential thermal resistance signal arising from two identical interfaces in series. We can divide each individual double interface measurement by two, which yields the ITR of a single interface. From the values of thermal resistance through single- and double-interface structures, we determine the ITR of a single H-H interface between two well-aligned Si(100) regions to be 9.2±2.3 m^2K/GW, and of a single H-ox interface between the same two regions to be 2.8±0.9 m^2K/GW.

Experimental ITR values for each measurement point represented in Fig. 5.6 are given in Table 5.1. Every value comes from a differential measurement of multiple devices on a single sample. For example, H2C(S5,S6,M7,M8) comes from an H-H interface sample (H), double interface (2), third sample of it's kind (C). On that sample

Table 5.1: Differential thermal resistance values for each measurement represented in Figs. 5.6. Each data point in Fig. 5.6 corresponds to a single value given here. Every value comes from a differential measurement of multiple devices on a single sample. For example, H2C(S5,S6,M7,M8) comes from an H-H interface sample (H), double interface (2), third sample of it's kind (C). On that sample 3ω measurements were performed on devices measuring directly into the substrate (S5 and S6) as well as devices measuring through the membrane structure (M7 and M8), all in parallel. The value given for this measurement is the mean membrane signal less the mean substrate signal.

Differential thermal resistance values (m^2K/GW)

H-H single interface		H-H double interface	
Sample(devices)	DTR	Sample(devices)	DTR
H1A(S1,S2,M4)	15.26	H2A(S1,S2,M3,M4)	18.51
H1A(S5,S6, M7)	13.72	H2B(S1,S2,M3,M4)	14.65
H1B(S1,S2,M3,M4)	2.38	H2B(S5,M7,M8)	22.06
H1B(S5,S6,M8)	6.65	H2C(S1,S2,M3,M4)	18.85
H1C(S5,S6,M8)	5.00	H2C(S5,S6,M7,M8)	21.10
H1C(S5,M7)	11.49		
H1D(S1,S2,M3,M4)	7.00		
H1D(S6,M8)	4.08		
H1E(S1,S2,M3)	10.74		
H1E(S5,M7,M8)	14.31		
H1E(S14,M16)	4.68		
H1E(S17,M18)	10.32		

H-ox single interface		H-ox double interface	
Sample(devices)	DTR	Sample(devices)	DTR
ox1A(S1,M4)	4.41	ox2A(S1,S2,M3)	7.84
ox1A(S5,M8)	1.94	ox2B(S2,M3)	7.73
ox1A(S9,M11,M12)	3.04	ox2B(S5,S6,M7,M8)	6.04
ox1B(S5,M7,M8)	-0.11	ox2B(S9,S10,M11,M12)	7.47
ox1C(S1,S2,M3,M4)	2.69	ox2C(S1,S2,S3,M8)	7.40
ox1C(S5,S6,M7,M8)	1.62	ox2C(S5,S6,M9)	3.37

3ω measurements were performed on devices measuring directly into the substrate (S5 and S6) as well as devices measuring through the membrane structure (M7 and M8), all in parallel. The value given for this measurement is the mean membrane signal less the mean substrate signal. A complete table of measured and computed values for each measurement device used in this work is available in Appendix B.

5.3 Structural characterization

In order to understand phonon transport through H-H and H-ox interfaces, it is important to characterize the thickness, roughness, and bonding energy of the interface [107].

To measure the total thickness of the interfacial region, scanning transmission electron microscopy was performed on both H-H and H-ox type samples. The samples of each type used for STEM imaging are typical double-interface samples. Electron transparent cross-sectional TEM samples are prepared by an *in situ* lift-out technique using focused ion beam (FIB) etching. The FIB cut is made directly under a previously measured 4-probe measurement device.

Figure 5.7 shows TEM images of both H-H and H-ox sample types. From the wide angle TEM, we cannot see any large interfacial defects or voids. Although the TEM gives us only a small snapshot of each interface, the consistently good interfaces shown in both samples suggests high quality and consistent fabrication. The figure also includes high-resolution STEM images of the interface regions for both sample types. Note that these high-resolution images may not have actually come from the areas suggested in the figure, but that they do come from the appropriate interface type, either H-H or H-ox, and either substrate-NM or NM-NM. The substrate-NM interface thickness for H-H interface sample, in Fig. 5.7(a), is measured as 1.4 ± 0.2 nm, and the

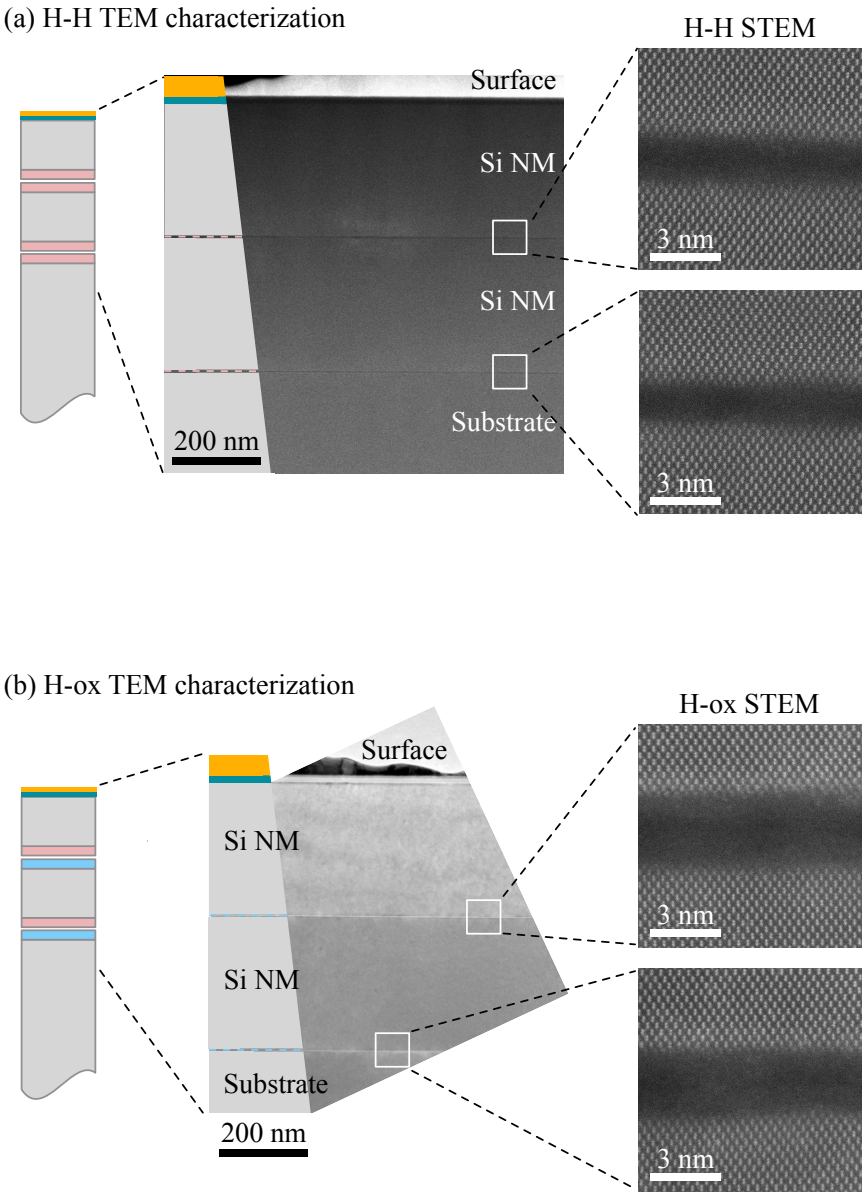

Figure 5.7: Schematic of H-H and H-ox samples, with wide angle TEM and high resolution z-contrast STEM images of both sample types taken along the [110] zone axis of Si, used for interface characterization. (a) The H-H interfaces have an interfacial thickness of 1.5 nm. (b) The presence of an additional oxide layer at the H-ox interfaces increases the thickness to 2.9 nm. All TEM and STEM images courtesy of Dr. Ashutosh Rath.

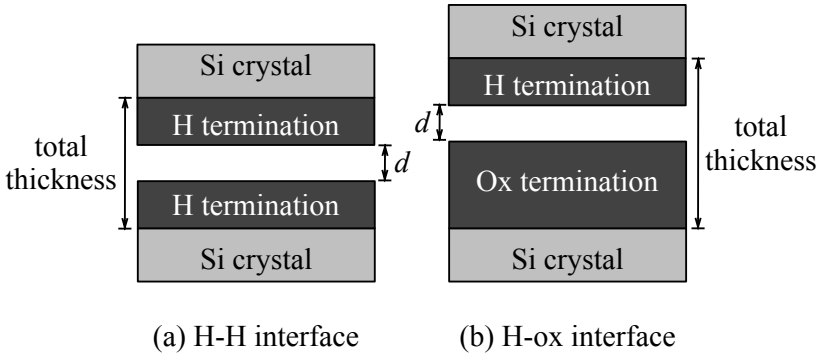

Figure 5.8: Schematic diagram of the interface termination structure for both H-H and H-ox type samples. The total interface thickness, as measured by STEM, is greater than the interfacial separation distance d between vdW-bonded planes. The terminations of each surface are amorphous, and not visible by STEM.

NM-NM interface thickness as 1.6± 0.2 nm. Figure 5.7(b) shows the high-resolution STEM results from the H-ox sample, where substrate-NM interface thickness is 2.8 ± 0.3 nm, and the NM-NM interface thickness is 3.0±0.2 nm. The average H-H interface thickness is therefore 1.5 nm, while the average H-ox interface thickness is 2.9 nm. These thicknesses represent the total distance between Si crystals, which is larger than the separation distance of the vdW-bonded interface, as schematically illustrated in Fig. 5.8. Each Si surface has a covalently-bonded termination, which is not visible by STEM. It is the distance of these surface terminations from each other that defines the thickness of the vdW-bonded interface separation, for which the STEM results provide a definitive upper bound.

The determination of interface thickness from the STEM measurements was done by measuring the width between top and bottom crystal patterns along several hundred nanometers of the interface. Each interface was measured 80 times. The mean and standard deviation of these measurements is reported for each of the 4 interfaces inspected.

The rotational alignment of the membrane transfer, also important to our un-

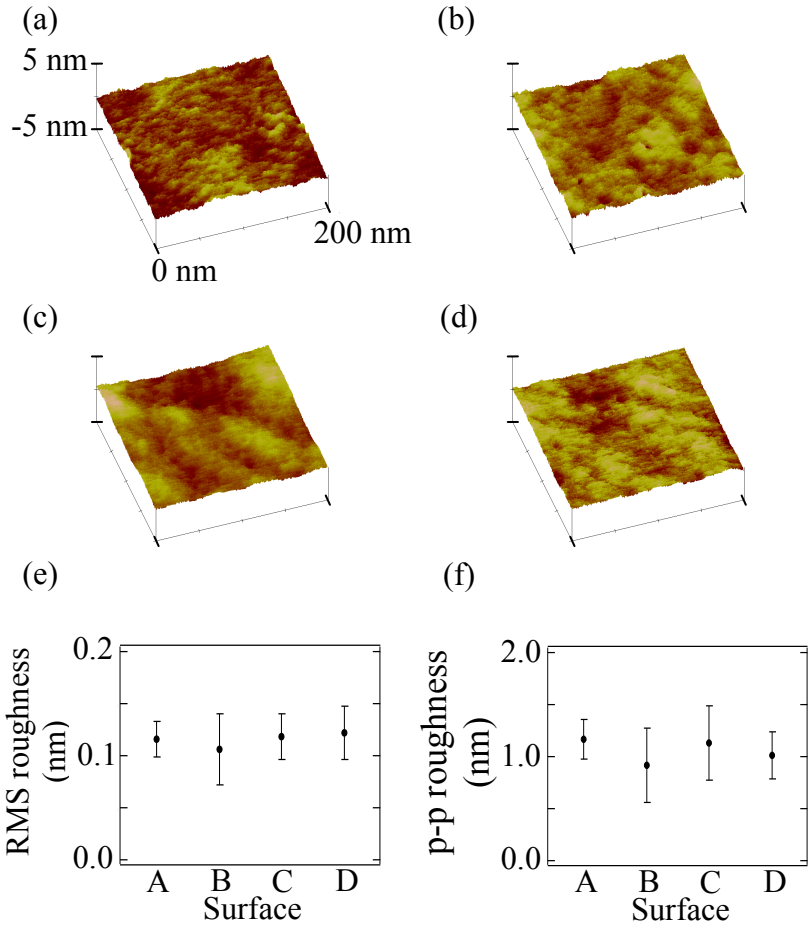

Figure 5.9: AFM surface roughness measurement results. (a-d) Typical AFM scans on four different surface types, all with the same vertical and lateral dimensions. (a) Typical AFM scan of an oxide-terminated substrate as prepared for transfer. (b) H-terminated substrate as prepared for transfer. (c) H-terminated substrate in an area adjacent to a membrane after transfer. (d) H-terminated nanomembrane surface after transfer. (e-f) AFM measurements on A-hydrophilic substrates pre-transfer, B-hydrophobic substrates pre-transfer, C-hydrophobic substrates adjacent to membranes post-transfer, and D-top membrane surface post-transfer. RMS roughness is given in (e), peak-to-peak roughness is given in (f).

derstanding of phonon transport through the interface, is very good in all samples measured by STEM. As can be seen by the well-aligned Si dumbbells in the silicon regions on either side of the interfaces in Fig. 5.7, the rotational alignment is within 1° [110].

To determine the interface roughness, which is difficult to estimate by STEM, AFM measurements were conducted. Measurements were taken on four surfaces: H-terminated and oxide-terminated receiver substrates as prepared for NM transfer, the exposed top NM surface directly after transfer, and the exposed substrate adjacent to that membrane after transfer. Figure 5.9 shows typical AFM scans on each surface used for this measurement. All AFM analysis was done on 200 nm x 200 nm scans, with a minimum of 5 scans per surface type spread across an area of order 1 mm^2. Each scan is flattened using the native NanoScope 4.43r6 software, and then analyzed for root mean square (RMS) and peak-to-peak roughness. Plots of the root-mean-square (RMS) and peak-to-peak roughness for each surface are given in Fig. 5.9(e) and (f). The roughness is consistent across all measured surfaces, with average RMS roughness of 0.12 nm and average peak-to-peak roughness of 1.1 nm. Because all measured roughnesses were consistent, regardless of what processing steps each surface had been exposed to, we assume that the bottom surface of the NM, at the interface, is also consistent.

Also key to modeling the ITR is the bonding energy of each interface, which we take from previous wafer bonding results. The H-H interface bonding energy has previously been measured in wafer bonded samples as 30 mJ/m^2 at room temperature, and 100 mJ/m^2 after annealing to 300°C [111]. H-ox bonding has been measured as 60-80 mJ/m^2 at room temperature with no anneal [112]. We have not been able to find a value after the anneal.

Dehydration at interfaces with H-terminated surfaces is not expected to occur unless the samples are annealed above about 400°C, which they are not, and so the H-H interface remains vdW bonded[113].

5.4 Theoretical modeling

Here we discuss a model proposed by Dr. Zlatan Aksamija and its application to the experiments discussed above. The model relates the observed interfacial thermal resistance to three variables: (i) interface separation distance, (ii) interfacial bonding energy, and (iii) acoustic impedance mismatch (which we may ignore here, because phonons are crossing a boundary between like materials). Calculations based on this model show that the physical interpretation presented above can be made quantitative with a reasonable choice for the interface separation and the bonding energy, both of which are consistent with the STEM measurements (in the case of the interface separation) and expectations from the literature (for the case of the bonding energy).

Given an understanding of the interface characteristics as described in the previous section, it is possible to model the ITR through a vdW-bonded interface [64]. The perturbation to the thermal transport at the vdW contact must be taken into account in the thermal-conductivity calculations. Our model, which we call vdW-AMM, is based on the Acoustic Mismatch Model (AMM) [10], and includes the theory of thermal conduction through van der Waals bonded interfaces [11]. To model thermal transport through an interface, it is important to know the transmission coefficient τ for each phonon mode $\vec{q}$. Within the vdW-AMM model, the phonon transmission coefficient $\tau_{\mathrm{b}}^{\mathrm{vdW}}(\vec{q})$ due to the vdW contact between identical materials is

$$\tau_{\mathrm{b}}^{\mathrm{vdW}}(\vec{q}) = \frac{1}{1 + \frac{\omega_{\mathrm{b}}^2(\vec{q})}{K_A} Z_{\mathrm{b}}^2(\vec{q}) \cos^2 \Theta}, \tag{5.1}$$

where $\omega_{\mathrm{b}}(\vec{q})$ is the phonon angular frequency of mode $\vec{q}$ on phonon branch b making angle Θ with the interface normal, and $Z_{\mathrm{b}}(\vec{q})$ is the acoustic impedance. K_A is the spring constant per unit area, and is dependent on the interfacial separation distance d and the interfacial adhesion energy γ.

We relate the spring constant K_A in the vdW-AMM model to the adhesion energy

via the Hamaker constant. The spring constant per unit area is given by $K_A = nK$, with $K = 72\epsilon(2^{1/3}d^2)$ and n being the number of surface atoms per unit area. ϵ and d are the depth of the potential well and the length scale parameter of the Lennard-Jones potential, respectively. These two parameters are key in describing the interface as d is related to the equilibrium distance between the two surface planes z_0 by $d = (2/15)^{1/6}z_0$ while ϵ can be related to the bonding strength γ through the Hamaker constant $H = 4\pi^2\epsilon N^2 d^6$, which is then related to the bonding strength as $H = 16\pi z_0^2\gamma$.

The full phonon dispersion is calculated from the Adiabatic Bond Charge model for Si [114], as described in more detail in Ref. [57]. $Z_{\rm b}(\vec{q})$ is given by $Z_{\rm b}(\vec{q}) = \nu_{\rm b}(\vec{q})\rho$, where $\nu_{\rm b}(\vec{q})$ is the phonon velocity of mode $\vec{q}$ obtained from the gradient of the dispersion $\nu_{\rm b}(\vec{q}) = \nabla_{\vec{q}}\omega_{\rm b}(\vec{q})$ and ρ is the density.

Phonon transmission through interfaces generally does not get interrupted at low phonon frequencies, because of the long wavelength of the phonons. Phonons with higher frequencies experience more scattering, because their wavelength becomes comparable to the nanoscale size of the interfacial imperfections. The result is an overall reduction of the phonon transmission through the interface. This feature can be observed directly in Eq. 5.1, where the phonon transmission through the vdW interface reaches unity as the phonon angular frequency ω goes to zero, corresponding to the acoustic or long wavelength limit. In the opposite limit, as ω increases, the transmission decays as ω^{-2}.

The interface conductance σ^{vdW} is obtained from the transmission coefficient by summing over all phonon branches b that contribute to transport in each layer i and all the modes $\vec{q}$ [115, 67]:

$$\sigma_{i,T}^{\rm vdW} = \frac{1}{2}\sum_{{\rm b},\vec{q}} \frac{C_{{\rm b},T}(\vec{q})\upsilon_{\rm b}(\vec{q})\cos\Theta\tau_{\rm b}^{\rm vdW}(\vec{q})}{1-\langle\tau_{\rm b}^{vdW}(\vec{q})\rangle}, \tag{5.2}$$

where $C_{\mathrm{b},T}(\vec{q})$ is the modal heat capacity given by

$$C_{\mathrm{b},T}(\vec{q}) = \frac{\left[\hbar\omega_{\mathrm{b}}(\vec{q})\right]^2}{k_B T^2} \frac{e^{(\hbar\omega_{\mathrm{b}}(\vec{q})/k_B T)}}{\left[e^{(\hbar\omega_{\mathrm{b}}(\vec{q})/k_B T)} - 1\right]^2} \tag{5.3}$$

and T is the temperature. The correction factor in the denominator of Eq. 5.2 ensures that the interface resistance goes to zero in the limit of a fictitious ideal interface between two identical materials, where τ^{vdW} becomes unity and interface resistance must vanish [116].

Using the previously measured bonding strength for H-H interfaces annealed at 300°C of γ=100 mJ/m^2 [111] and our measured value for the H-H ITR of 9.2 m^{2}K/GW, the vdW-AMM model gives an interfacial separation distance of d=0.38 nm. This value describes the distance between vdW-bonded planes at the H-H interface, and is rightfully smaller than the total separation distance between Si crystals, as illustrated in Fig. 5.8. This value of d is also consistent with the roughness measurements performed on membrane and substrate surfaces.

Because oxide-terminated and H-terminated surfaces have equal roughness, we assume that the H-ox interfaces have equal interfacial separation to the H-H interfaces. The H-ox interfaces do however have additional structure, which must be accounted for by adding a thermal resistance in series. The additional 1.4 nm of amorphous oxide termination at the H-ox interface contributes a thermal resistance in series with the vdW bonded interface. By using the minimum thermal conductivity calculation for amorphous SiO_2 of κ_{ox}=1.05 W m^{-1} K^{-1} [117], we find that the additional oxide at the H-ox interface yields a resistance of R_{ox}=1.5 m^{2}K/GW. Given the total interfacial thermal resistance ITR=R_{ox}+R_{vdW}, we determine R_{vdW}=1.3 m^{2}K/GW at the H-ox interface. The vdW-AMM model then gives the bonding strength to be γ=300 mJ/m^2. This result is consistent with the expectation of increasing the bonding strength through annealing, and maintains the relative strength of the bonding of

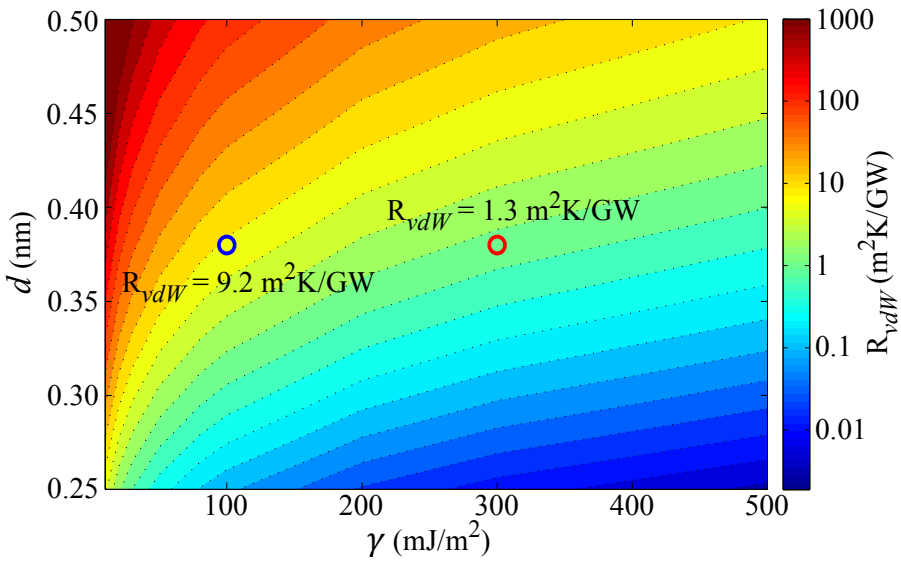

Figure 5.10: Contribution to the ITR due to vdW bonding as a function of the interfacial separation distance d and bonding strength γ, calculated from the vdW-AMM model. Thermal resistivity decreases with γ, and increases with d. The experimental thermal resistance results are shown by symbols with the H-H (red) and H-ox (blue) interfaces both consistent with calculations at interface separation d=0.38 nm and γ=100 mJ/m^2 and 300 mJ/m^2, respectively.

H-H and H-ox interfaces pre- and post-anneal.

The results of the vdW-AMM calculations are displayed in Fig. 5.10. The vdW-AMM components of the total ITR are plotted for both interface types as a function of both interface separation distance d, on the vertical axis, and interfacial bonding strength γ, on the horizontal axis.

The vdW-AMM model also explains well the thermal resistance observed by Grimm *et al.* through unannealed Si-Si interfaces in which both surfaces were oxide terminated. Assuming twice the R_{ox} of our H-ox interfaces and bonding energy of 200 mJ/m^2 [111], the value of R_{vdW}=30 m^{2}K/GW is achievable with sub-nanometer interfacial separation, in agreement with the original observations and results [35].

Previous studies have suggested that the presence of an oxide at a mechanically created Si-Si interface has a negligible effect on interfacial thermal resistance [35]. We

see here, however, that the oxide contribution to the thermal resistance is only negligible for interfaces with high overall thermal resistance, such as unannealed samples. More importantly, however, we see that even if the resistance of the oxide itself is negligible, the role the oxide plays in the bonding strength of the interface is vital.

Further, past studies have compared ITR between interfaces fabricated on H-terminated substrates to interfaces fabricated on oxide-terminated substrates, although not in Si-Si structures. The results of these studies have not been conclusive, with multiple reports of increased ITR at the oxide interface [74, 79], as well as multiple reports of the opposite effect, decreased ITR at the oxide interface [72, 78, 13]. Here we find clear evidence that oxide-terminated substrates lead to lower ITR between mechanically-join single-crystal silicon regions due to the increased interfacial bonding energy when compared to interfaces with hydrogen-terminated substrates.

In conclusion, we show that vdW bonded interfaces of transferred nanomembranes can have very low interfacial thermal resistance. Further, the surface condition of vdW-bonded interfaces between like materials can affect the ITR by over 300%: interfaces created by transfer printing hydrogen-terminated silicon nanomembranes onto oxide-terminated silicon receiver substrates show a significantly lower interfacial thermal resistance than those formed by transferring to hydrogen-terminated substrates. The vdW-AMM model, which we propose here, accurately captures and describes the interface-specific properties critical to ITR and confirms our understanding of the experimental ITR values, characterization measurements, and theoretical modeling methods. We show the direct relationship between ITR and bonding energy. The results are important for the future of thermal management in electronic devices built on flexible, stretchable, and transferable nanomembranes.

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Chapter 6

Conclusion

In this work we use silicon nanomembrane transfer to create mechanically-joined silicon-silicon interfaces. Two well-aligned regions of single crystal silicon are van der Waals bonded together across a narrow interfacial region using a thermal-release tape transfer technique. These model interfaces are useful as they control for several of the factors that contribute to interfacial thermal resistance, including importantly the acoustic mismatch of materials across the interface. The result is that the ITR is highly dependent on the bonding strength of the interface.

Mechanically-joined, vdW-bonded interfaces have lower bonding strength than those formed by more intimate covalent bonds, created by thermal oxidation or thin film deposition. Previous measurements had shown that the ITR of vdW-bonded interfaces was generally greater than for most covalent interfaces. We have shown here, however, that under the right conditions, the lower bonding strength across an interface formed by vdW bonds need not limit thermal transport across that interface. This result has large implications for the development of stackable, multilayer, stretchable, flexible, and transferable electronics based on nanomembrane technology.

We have provided characterization measurements using TEM and AFM, as well

as the vdW-AMM model which describes the critical properties critical to interfacial thermal resistance. Both the characterization and modeling confirm our understanding of the experimental ITR results.

6.1 Future work

The techniques described in this thesis, both in sample fabrication and measurement, provide a means to continue the study of thermal transport across nanomembrane interfaces. As described in Chapter 2, interfaces are of greatest use in application when they have thermal resistances in one of the two extremes, either very high or very low. Moving forward, studies of nanomembrane interfaces could either focus on optimizing towards either of these extremes, or investigating how very specific characteristics of the interface affect ITR.

One of the main ways to vary the interface is by manipulating the substrate. Using different surface terminations on the substrate will affect bonding strength and interfacial separation. Changing the rotational alignment of the Si substrate with respect to the Si NM will change, however slightly, the way phonons can transfer from one crystal to the other. Likewise, changing the material of the substrate all together will introduce an acoustic mismatch which we expect to raise the ITR. Germanium, for example, has a lattice that is 4% larger than silicon. Careful control over such variables will lead to better understanding of the physics of ITR.

Interfaces that incorporate 2D materials, such as graphene or transition metal dichalcogenide (TMDC) monolayers, are also of interest. The introduction of an interfacial layer may increase the interfacial bonding strength, as the oxide layer did in this work, or it may reduce phonon transport through increased scattering and mode mismatch. Understanding what characteristics effect these results will be

important to the future of technologies which incorporate these 2D materials.

Lastly, it would be a huge step forward in this work to incorporate an electrical measurement capable of measuring the electrical resistance across interfaces. Interfaces with high electrical resistivity are useful in nanoelectronics applications as electrically insulating layers. Interfaces with low electrical resistivity are necessary in thermoelectric applications. The trick is to decouple electrical and thermal resistivity, as it is low thermal resistivity that is necessary in electronics, and high thermal resistivity in thermoelectrics. The ability to measure both parameters independently will significantly increase the scope of possible work.

Appendix A

Details of the AMM results displayed in Fig. 3.2

Table A.1: Details of the AMM results displayed in Fig. 3.2

Reference	Material 1	Material 2	Θ_1 (K)	Θ_2 (K)	DTR (Θ_2/Θ_1)	ITR (m^2K/GW)
[66]	Pb	BaF_2	102	287	2.8	16.1
[66]	Au	BaF_2	165	287	1.7	25
[66]	Al	BaF_2	423	287	0.68	10
[66]	Pb	sapphire	102	1024	10.0	18.2
[66]	Au	sapphire	165	1024	6.2	22.2
[66]	Al	sapphire	423	1024	2.4	9.5
[66]	Ti	sapphire	426	1024	2.4	8.9
[66]	Pb	diamond	102	2240	22.0	32.3
[66]	Au	diamond	165	2240	13.6	25
[66]	Al	diamond	423	2240	5.3	21.7
[66]	Ti	diamond	426	2240	5.3	100
[94]	Au	AlN	165	1150	7.0	70
[82]	Cu	sapphire	344	1024	3.0	4

Table A.2: Details of the AMM results displayed in Fig. 3.2, continued

Reference	Material 1	Material 2	Θ_1 (K)	Θ_2 (K)	DTR (Θ_2/Θ_1)	ITR (m^2K/GW)
[68]	Al	GaN	423	600	1.4	5.3
[68]	Cr	GaN	630	600	0.95	4.3
[68]	Au	Si	165	645	3.9	14.1
[68]	Pt	Si	240	645	2.7	7.1
[68]	Al	Si	423	645	1.5	8.3
[68]	Cr	Si	630	645	1.0	5
[68]	Al	sapphire	423	1024	2.4	5
[68]	Cr	sapphire	630	1024	1.6	5.3
[68]	Al	AlN	423	1150	2.7	4.3
[68]	Cr	AlN	630	1150	1.8	5
[13]	Pb	Si	102	645	6.3	50
[13]	Pb	sapphire	102	1024	10.0	35
[13]	Pb	diamond	102	2240	22.0	75
[13]	Bi	Si	120	645	5.4	90
[13]	Bi	sapphire	120	1024	8.5	85
[13]	Bi	diamond	120	2240	18.7	117
[81]	Al	sapphire	423	1024	2.4	5.4
[81]	Pt	sapphire	240	1024	4.3	8.6
[81]	Cr	Si	630	645	1.0	9
[81]	Pt	AlN	240	1150	4.8	8.7
[78]	Al	diamond	423	2240	5.3	11
[80]	Al	TiN	423	580	1.4	5
[79]	Al	Si	423	645	1.5	5
[77]	Al	Si	423	645	1.5	2.9
[74]	Al	SiC	423	1194.8	2.8	5
[75]	Au	Si	165	645	3.9	8.5
[76]	Al	Si	423	645	1.5	5
[71]	Au	Si	165	645	3.9	5
[72]	Al	diamond	423	2240	5.3	5.5
[72]	Al	Si	423	645	1.5	2.9
[72]	Al	sapphire	423	1024	2.4	5.3
[69]	Au	Si	165	645	3.9	10
[70]	Al	Si	423	645	1.5	8
[118]	Al	Si	3	423	645	1.5
[118]	Al	Ge	4.3	423	374	0.88
[119]	Al	MgO	2.2	423	750	1.8
[120]	Au	Si	20	165	645	3.9
[120]	Pt	Si	6.7	240	645	2.7
[120]	Pd	Si	8	275	645	2.3
[120]	Al	Si	4.5	423	645	1.5
[120]	Ni	Si	5	450	645	1.4
[120]	Ru	Si	5.7	600	645	1.1
[120]	Mo	Si	6.25	450	645	1.4

Appendix B

Detailed results of Si-Si interface measurements

Table B.1: Detailed results of thermal resistance measurements

Device	R_0 (Ω)	I_0 (mA)	dR/dT (mΩ/K)	$\frac{1}{R_0} \cdot \frac{dR}{dT}$ (10^{-3}/K)	$dV_{3\omega}/d\ln(\omega)$ (μV/ln(ω))	Substrate κ (W/(m K))	$\bar{R}$ (K/W)
H1AS1	7.57357	15.0594	8.97	2.50476	-0.495739	196.908	13.0647
H1AS2	7.49395	15.0516	18.684	2.49321	-0.439014	216.362	12.2959
H1AM4	7.50758	15.0944	17.78	2.36827	-0.517195	176.584	16.4964
H1AS5	7.53925	15.0629	18.853	2.50065	-0.682938	141.509	12.8153
H1AS6	7.46977	15.0384	18.6334	2.49451	-0.560202	168.107	12.2536
H1AM7	7.66616	15.0486	19.026	2.48182	-0.488037	202.624	15.9655
H1BS1	7.63496	15.1046	19.0478	2.49481	-0.529848	188.173	13.0119
H1BS2	7.50506	15.1042	18.6324	2.48264	-0.412994	232.115	12.7617
H1BM3	7.36933	15.0811	18.1954	2.46907	-0.527254	173.542	13.5714
H1BM4	7.30579	15.1176	18.5234	2.53544	-0.619265	150.207	13.3927
H1BS5	7.59018	15.0775	19.0672	2.51209	-0.592625	166.524	13.0447
H1BS6	7.35311	15.0626	18.3262	2.49231	-0.532839	171.94	12.5519
H1BM8	7.46797	15.1021	18.877	2.52773	-0.662084	145.903	14.4608
H1CS1	7.48115	15.0595	18.9216	2.52924	-0.513821	187.185	12.8216
H1CS2	7.4136	15.046	18.4448	2.48797	-0.562164	164.829	12.6605
H1CM3	7.50668	15.0256	18.4788	2.46165	-0.470818	198.834	14.0444
H1CM4	7.40111	15.0718	18.4756	2.49633	-0.522094	178.391	13.94
H1CS5	7.45258	15.039	18.57	2.49175	-0.497188	188.357	12.8745
H1CM7	7.35127	15.0529	18.0838	2.45995	-0.421029	214.255	15.748

Table B.2: Detailed results of thermal resistance measurements, continued

Device	R_0 (Ω)	I_0 (mA)	dR/dT (mΩ/K)	$\frac{1}{R_0} \cdot \frac{dR}{dT}$ (10^{-3}/K)	$dV_{3\omega}/d\ln(\omega)$ (μV/ln(ω))	Substrate κ (W/(m K))	$\bar{R}$ (K/W)
H1DS1	13.2807	15.2855	35.0378	2.63824	-1.84338	179.353	13.1564
H1DS2	13.1584	15.3784	34.282	2.60534	-1.8181	179.519	13.0821
H1DM3	12.0692	15.3865	31.4066	2.6022	-1.54329	177.995	15.346
H1DM4	12.0334	15.4408	31.5068	2.61828	-1.5388	180.449	14.3911
H1DS6	13.4217	15.0088	35.825	2.66919	-1.94027	166.685	14.9119
H1DM8	12.3227	15.0592	32.9406	2.67316	-1.83555	150.247	15.9327
H1ES1	16.5626	15.9494	41.6692	2.51586	-3.11066	179.083	12.8952
H1ES2	17.1484	15.9638	43.482	2.53563	-3.42005	176.459	12.973
H1EM3	16.5782	15.9971	42.0333	2.53546	-3.54142	160.253	15.6186
H1ES5	16.8194	16.6899	41.993	2.4967	-4.40898	148.162	8.30858
H1EM7	18.2713	16.7274	46.8982	2.56677	-5.41564	147.329	10.7627
H1EM8	17.5849	16.7853	44.8328	2.5495	-3.68342	201.374	13.0117
H1ES14	18.1238	18.4907	45.8428	2.52943	-8.03665	130.027	7.70799
H1EM16	17.9157	18.5828	45.3844	2.53322	-9.10289	114.032	8.87786
H1ES17	17.4571	18.4407	43.2474	2.47735	-3.80319	247.657	5.56644
H1EM18	18.5811	18.5507	47.6468	2.56426	-2.43726	195.674	8.1456
H2AS1	14.1144	15.6428	36.8184	2.60858	-2.22633	177.75	14.0931
H2AS2	14.5573	15.6361	37.9408	2.60631	-2.37853	176.601	13.6761
H2AM3	15.0141	15.6315	39.6816	2.64296	-2.65178	170.718	19.7407
H2AM4	13.6075	15.6556	35.5978	2.61605	-2.09227	176.735	17.2857
H2BS1	12.5035	14.8541	33.4715	2.67697	-1.78929	152.511	14.8602
H2BS2	12.3359	14.8429	32.9309	2.66952	-1.82914	144.481	14.2087
H2BM3	12.4628	14.8433	33.3726	2.67778	-1.86238	145.298	19.9107
H2BM4	15.2971	14.8661	32.9175	2.15188	-2.13311	154.292	16.4851
H2BS5	12.6244	15.5174	32.5991	2.58223	-1.66253	184.007	11.6372
H2BM7	11.9148	15.6092	30.1594	2.53125	-1.43921	188.912	17.1693
H2BM8	12.2859	15.6807	31.9166	2.59782	-1.87891	160.083	17.1326
H2CS1	18.2905	15.5048	49.9062	2.72853	-3.99936	169.246	14.883
H2CS2	18.1524	15.4609	49.166	2.70852	-3.86498	169.778	14.8469
H2CM3	18.3812	15.4802	50.3908	2.74143	-4.0359	169.374	19.9875
H2CM4	16.1213	15.5102	43.6162	2.7055	-3.21866	162.164	19.168
H2CS5	18.3592	15.2911	50.2642	2.73782	-4.02668	163.007	15.1742
H2CS6	18.3877	15.3675	50.3228	2.73676	-3.98649	167.587	15.1634
H2CM7	18.7131	15.3838	51.5028	2.75223	-4.39908	158.684	22.3225
H2CM8	16.1973	15.4409	44.1638	2.72661	-2.98396	175.575	18.5628
ox1AS1	18.7867	15.6798	49.0563	2.61123	-5.12825	137.825	14.655
ox1AM4	18.8594	15.7143	49.6648	2.63342	-5.12342	141.134	15.757
ox1AS5	18.1346	15.791	47.5885	2.62418	-4.73303	142.835	11.4779
ox1AM8	18.404	16.7925	47.5606	2.58426	-4.67587	176.347	11.9637

Table B.3: Detailed results of thermal resistance measurements, continued

Device	R_0 (Ω)	I_0 (mA)	dR/dT (mΩ/K)	$\frac{1}{R_0} \cdot \frac{dR}{dT}$ (10^{-3}/K)	$dV_{3\omega}/d\ln(\omega)$ (μV/ln(ω))	Substrate κ (W/(m K))	$\bar{R}$ (K/W)
ox1BS5	19.7493	16.7076	51.69	2.6173	-6.09474	155.409	12.079
ox1AS9	17.0188	16.9215	43.7754	2.57218	-3.98349	180.278	11.8899
ox1AM11	17.0458	16.6951	43.8816	2.57434	-4.07155	170.074	12.6534
ox1AM12	16.7671	16.7892	43.2898	2.58182	-3.7917	180.232	12.6464
ox1BM7	17.5649	16.7309	45.726	2.60325	-3.91142	191.321	12.1259
ox1BM8	18.1781	16.8112	47.7704	2.62791	-4.76838	172.134	11.9748
ox1CS1	17.0124	20.6305	40.462	2.37838	-3.46571	346.964	5.38251
ox1CS2	17.1609	20.6343	41.3608	2.41018	-3.63891	340.924	5.42095
ox1CM3	17.542	20.6604	43.0168	2.45222	-3.77792	350.436	6.04587
ox1CM4	17.1005	20.7069	41.4618	2.42459	-3.62658	345.334	6.10078
ox1CS5	16.8625	18.1394	41.682	2.47187	-3.85401	216.549	8.32084
ox1CS6	17.0137	18.1371	42.196	2.48011	-3.80006	224.241	8.27654
ox1CM7	17.4184	18.1626	43.86	2.51803	-4.11244	221.432	9.91775
ox1CM8	16.6838	18.2169	41.42	2.48265	-3.6942	224.977	7.49008
ox2AS1	18.4194	15.949	47.9719	2.60442	-4.39294	162.346	13.7575
ox2AS2	18.259	15.9843	47.564	2.60497	-8.98324	78.5477	11.162
ox2AM3	17.1837	16.0122	44.5448	2.59227	-5.6452	110.745	14.4203
ox2BS2	19.1148	18.5683	49.4711	2.5881	-4.89098	246.246	8.61534
ox2BM3	19.6917	18.5795	51.9322	2.63727	-5.19014	251.404	10.5479
ox2BS5	18.9927	20.8631	48.048	2.52981	-5.2032	316.852	6.04187
ox2BS6	18.9094	20.8876	47.909	2.53361	-4.84527	338.978	5.91774
ox2BM7	19.5916	20.9191	50.8428	2.59513	-5.68396	319.16	7.69445
ox2BM8	18.4325	20.9609	46.3486	2.51451	-4.73672	330.45	7.28618
ox2BS9	19.3453	20.9386	49.4976	2.55863	-5.38788	324.575	6.05898
ox2BS10	19.0563	20.9292	48.5676	2.54863	-4.91062	343.743	5.79089
ox2BM11	18.6415	20.9896	47.073	2.52518	-4.76098	339.077	7.66663
ox2BM12	19.8339	21.0549	51.9076	2.61711	-5.89652	324.215	7.91743
ox2CS1	17.3528	20.6305	42.0108	2.42098	-3.90193	326.373	5.61161
ox2CS2	16.749	20.6518	39.6684	2.3684	-3.28746	354.142	5.4056
ox2CS3	17.5749	20.6627	43.1268	2.45388	-4.12839	322.217	5.15421
ox2CM8	17.287	20.7293	42.0106	2.43019	-3.89976	330.008	7.24112
ox2CS5	17.1764	20.7576	41.2116	2.39932	-3.59895	349.972	5.43198
ox2CS6	17.3513	20.7615	41.917	2.41579	-3.7423	346.013	5.52625
ox2CM9	17.6671	20.8401	43.7312	2.47529	-4.28998	324.287	6.32135

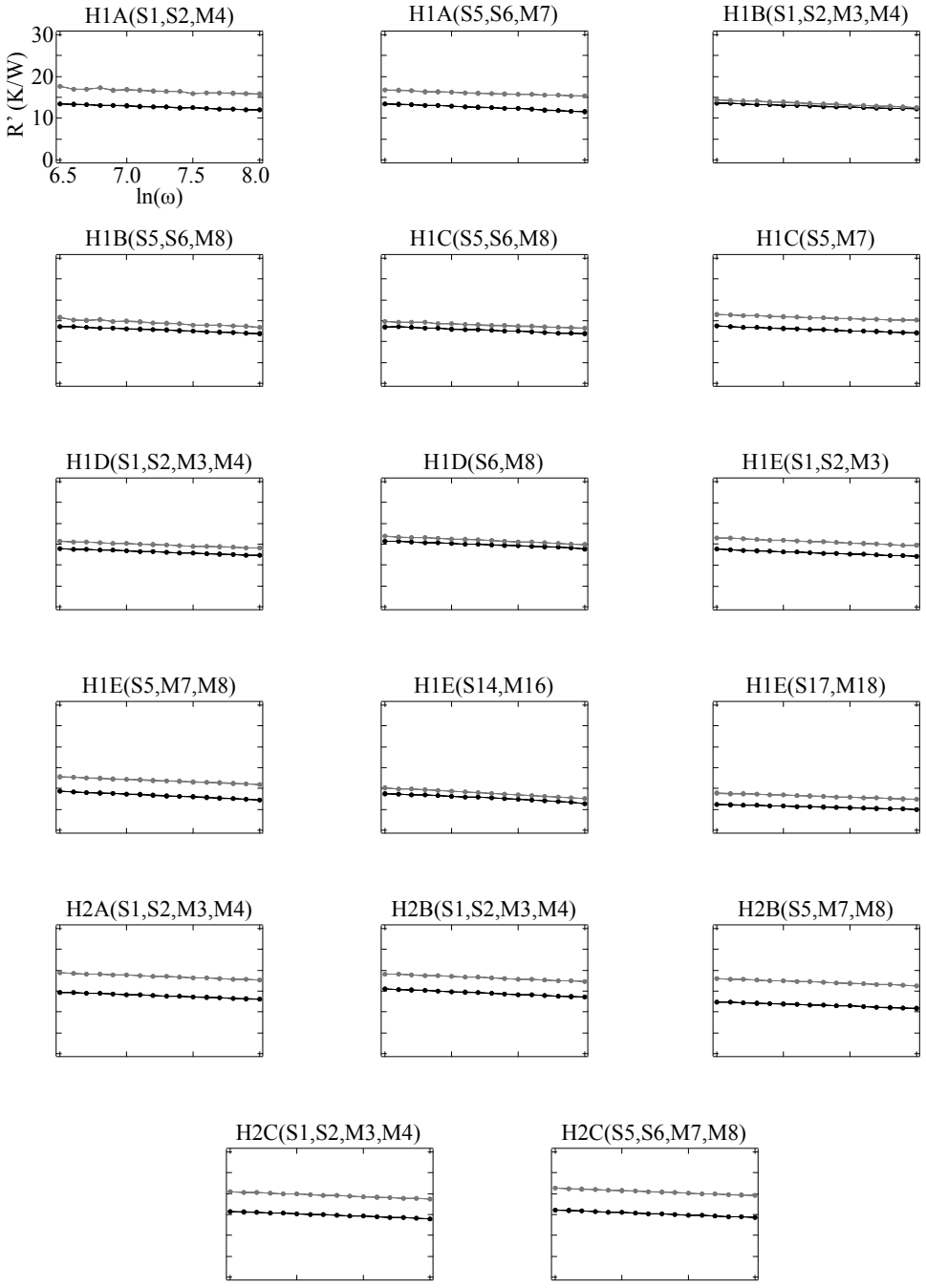

Figure B.1: Individual measurement data for all H-H interface data points. Each panel shows the mean signal of devices that measure directly into the substrate (black) and of devices that measure through the membrane interface structure (gray). Interfacial thermal resistances are proportional to the vertical shift between the two signals. All graphs have the same axes, as labeled in the first panel.

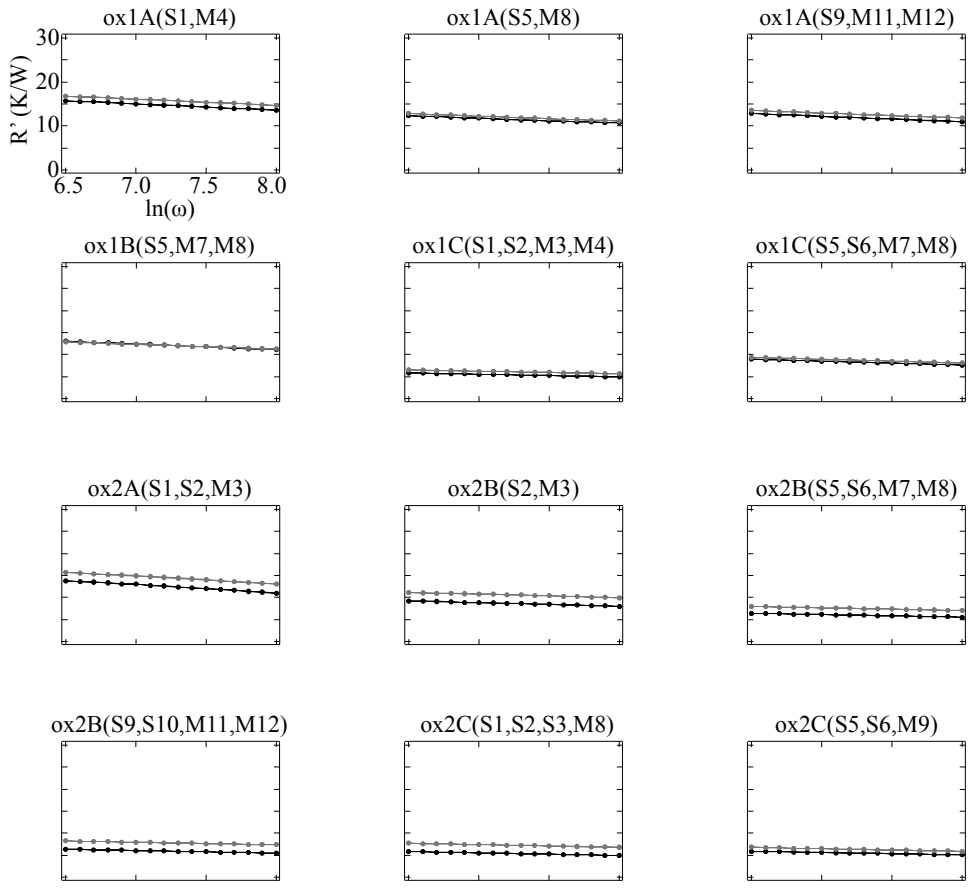

Figure B.2: Individual measurement data for all H-ox interface data points. Each panel shows the mean signal of devices that measure directly into the substrate (black) and of devices that measure through the membrane interface structure (gray). Interfacial thermal resistances are proportional to the vertical shift between the two signals. All graphs have the same axes, as labeled in the first panel.

Appendix C

Preliminary results on HMDS-terminated interfaces

As shown in Ch. 5, the bonding energy of mechanically formed Si-Si interfaces is a crucial parameter in determining interfacial thermal resistance. One way to manipulate the adhesion strength is through the silicon surface terminations present at the interface. We showed in Ch. 5 that receiver substrates terminated with a thin oxide layer resulted in a more strongly bonded interface than when H-terminated receiver substrates were used due to the increased bonding energy of the oxide termination.

Here, we show preliminary ITR results of interfaces formed by transferring H-terminated membranes onto receiver substrates that have been treated with hexamethyldisilazane (HMDS). HMDS is commonly used as a photo resist adhesion promoter during optical lithography processing.

We fabricate H-HMDS interfaces in much the same way as both the H-H and H-ox interfaces discussed in Ch. 5. The receiver substrates are cleaned and then terminated with a chemical oxide layer. Before membrane transfer, however, the substrates are subjected to the additional step of HMDS termination. This is accomplished in a

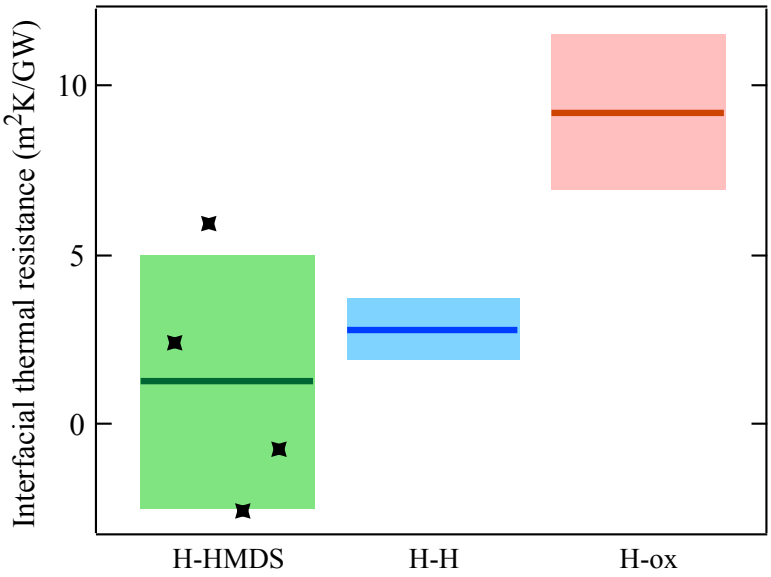

Figure C.1: Preliminary results of the ITR through interfaces formed by transferring H-terminated Si nanomembranes onto HMDS terminated Si substrates. Also shown are the measured ITRs for H-H and H-ox interfaces as previously discussed, for comparison. H-HMDS interfaces have ITR consistent with the that of H-ox interfaces.

Solitec VBS200 HMDS Prime Oven, which bakes and exposes the Si samples to HMDS vapor in a vacuum chamber. After termination, membranes are transferred to the substrate surface as described previously, and cleaned and oxide capped accordingly. We have only made single interface H-HMDS samples.

Differential thermal resistance measurements were taken as previously described. Because only single interface samples were measured, we take the measured values to be the single interface ITR. We find the ITR of H-HMDS to be 1.2±3.7 m^2K/GW. The results of these measurements are shown in Fig. C.1 in green, along with the H-H and H-ox ITRs, as measured in Ch. 5, for reference. Solid dark lines give the mean value, while shading gives one standard deviation. The data points represented on the graph are enumerated in Table C.1.

Table C.1: Interfacial thermal resistance values for each measurement represented in Figs. C.1. Each data point in Fig. C.1 corresponds to a single value given here. Every value comes from a differential measurement of multiple devices on a single sample. For example, HMDS1A(S1,S2,M4) comes from an H-HMDS interface sample (HMDS), single interface (1), first sample of it's kind (A). On that sample 3ω measurements were performed on devices measuring directly into the substrate (S1 and S2) as well as a devices measuring through the membrane structure (M4), all in parallel. The value given for this measurement is the mean membrane signal less the mean substrate signal.

Interfacial thermal resistance values (m^2K/GW)

H-HMDS interface	
Sample(devices)	ITR
HMDS1A(S1,S2,M4)	2.37
HMDS1A(S5,S6, M7)	5.92
HMDS1B(S1,S2,M3,M4)	-2.57
HMDS1B(S5,S6,M7,M8)	-0.72

As we can see, these preliminary results suggest that the ITR of H-HMDS interfaces are consistent with the previously measured H-ox interfaces. This is a reasonable observation, as it suggests the H-HMDS interface is strongly bonded. We consider these results preliminary because we have relatively few data points, and those that we do have display a large spread. Additionally, we have not performed any characterization measurements to confirm the structure of the H-HMDS interface.

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