Modeling and Mitigation of Simultaneous Switching Events in Power Converters

by

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Abstract

In multi-phase inverter systems where phase legs share a common DC bus, simultaneous switching in two or more legs can result coupling between the two transients caused by shared commutation loop inductance. This coupling effect can cause an undesirable increase in transient voltage stresses and switching losses. This effect has received little attention in the literature. In this work, the potential simultaneous switching events that can occur within a three-phase inverter are evaluated across a range of conditions using a two-phase test circuit. The knowledge gained from this work can then be used to inform the design of simultaneous switching avoidance algorithms.

In the literature, some hardware-based solutions have been proposed to mitigate this issue, through active gate drive control or switching lockout circuitry. Previously, an asymmetric PWM method was proposed to avoid simultaneous switching between phases of a three-phase inverter. In this method, avoidance is performed by the PWM scheme without introducing any error into the inverter's output voltage. Thus, no further control modifications are required. However, this approach imposes limitations on both the control bandwidth and implementation of simultaneous switching avoidance between additional three-phase inverters sharing the same DC link. To overcome these limitations, an error vector approach is proposed that modifies the voltage command to avoid regions of simultaneous switching. In doing so, compensation must be performed to avoid control degradation due to the injected voltage errors. The result of this work is a pair of methods for avoiding intra-inverter simultaneous switching with differing pros and cons regarding implementation and their impacts on inverter output distortion.

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Nomenclature

Symbol	Description
C_{OSS}	Output capacitance of a power switching device
C_{dec}	Decoupling capacitance
I_d, I_c	MOSFET drain current and IGBT collector current
I_{expon}	Switching transient current modeled as an exponential decay input
I_L	Converter load current
I_{RR}	Diode reverse-recovery current
I_{ramp}	Switching transient current modeled as a ramp input
I_{qd}	Complex current space vector
L_p	Parasitic commutation loop inductance
L_{CC}, L_{Phase}	Common and phase parasitic commutation loop inductance
$L_{Virtual}$	Virtual inductance modeling simultaneous switching voltage coupling
m^*	Modulation index
$t_{d(on)}$, $t_{d(off)}$	Delay times during active device turn-on and turn-off
T_e	Electromagnetic torque
T_{PWM}	PWM switching frequency
t_{rise}, t_{fall}	Rise and fall time durations for semiconductor switching transients
T_s	Controller sampling time
τ_x	Time constant
V_{abc}	Phase voltages for a three-phase system
V_{DC}	DC bus voltage
V_{DS}, V_{CE}, V_{CA}	Drain-to-source, collector-emitter, and cathode-anode terminal voltages for the MOSFET, IGBT and diode, respectively.
V_g	Gate terminal voltage
V_{qd}	Complex voltage space vector
ΔV	Change in voltage
ΔT	Change in switching instant timing

T_{Dead}	Inverter deadtime
T_{Sep}	Separation time enforced between switching instances
V_{Sep}	Separation voltage enforced inverter voltage commands
V_{Min}, V_{Mid}, V_{Max}	Sorted minimum, middle, and maximum phase voltages for a set of three phase voltages
λ_{qd}	Complex flux space vector
θ_e, ω_e	Electrical angular position and velocity
ω_n	Natural frequency

Superscripts

$( )^*$	Commanded quantity
$( )^e$	Synchronous frame
$( )^s$	Stationary frame

Subscripts

$( )_e$	Synchronous frame electrical angle
$( )_{qd}$	Vector form of a complex variable, $( )_q - j( )_d$
$( )_{RMS}$	Root mean square value of a signal
$( )_{x\text{-}1}$	Signal value for the first-half of a PWM period
$( )_{x\text{-}2}$	Signal value for the second-half of a PWM period

Abbreviatioms

AC	Alternating current
APWM	Asymmetric PWM
DB-DTFC	Deadbeat-Direct Torque and Flux Control
DC	Direct Current
DPWM	Discontinuous Pulsewidth Modulation
DTC	Direct Torque Control
DSP	Digital Signal Processor

EMF	Electromotive Force
ESL	Equivalent Series Inductance
EV	Error Vector
FOC	Field-Oriented Control
FPGA	Field Programmable Gate Array
IGBT	Integrated Gate Bipolar Transistor
IM	Induction Machine
MOSFET	Metal-Oxide-Silicon Field Effect Transistor
PWM	Pulsewidth Modulation
SSA	Simultaneous Switching Avoidance
SPMW	Sinusoidal Pulsewidth Modulation
SVPWM	Space-Vector Pulsewidth Modulation
WEMPEC	Wisconsin Electric Machines and Power Electronics Consortium

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Introduction

In this section, the background and motivation for this research is presented together with a summary of the research contributions made and a chapter-by-chapter list of the content included in this thesis.

Background and Motivation

Switching transient modeling and measurement is a well-established area of research in the power electronics field. Understanding the nature of switching transient voltage and current waveforms in hard-switching power electronic circuits is necessary to ensure operating conditions remain within a device's rated limits. As voltage or thermal stresses approach or exceed the devices limits, fatigue and failure of the device will occur.

In the current literature, this research has primarily focused on single-device, or single-phase, switching transients. However, in the broad range of power converter systems utilized in industry, multiple converter outputs are frequently placed on a common-or shared-DC bus. A primary example of this is the three-phase voltage source inverter where all three inverter phase legs source and sink power to a common DC bus. Going further, drive systems are frequently designed with additional three-phase inverters, DC-DC converters, or active rectifiers on a common DC bus. This is often done in traction drive and industrial automation systems, and a clear example of this is the inverter drive topologies used in hybrid vehicles.

In any of these converter topologies, parasitic inductance present in the shared DC commutation loop circuit paths can result in voltage stress coupling between converter phases when multiple devices turn on or off simultaneously. This effect is not captured when simply analyzing a single-phase switching transient. The limited research to date into simultaneous switching has shown that it can cause increases in switching transient voltage stresses as well as power losses, due to this voltage coupling effect. In addition, some solutions have been proposed

using active gate drive control techniques which mitigate the severity of simultaneous switching events.

The two main thrusts of this research are to more clearly understand the impact of simultaneous switching on switching transient waveforms and to develop software-based solutions for completely avoiding simultaneous switching in three-phase inverter drives. An experimental test circuit is constructed to evaluate the effects of simultaneous switching on switching transient waveforms as a function of load current and switching transient separation in an IGBT-based inverter circuit. Simplified modeling techniques for estimating the impact of simultaneous switching on voltage stress are then developed to more clearly identify the design trade-off in selecting a given switching speed and the resulting requirement for parasitic inductance minimization and decoupling capacitor sizing. A voltage-error-based simultaneous switching avoidance technique is developed in contrast to the previously developed PWM-based approach. These two methods are then implemented on a current-regulated induction motor drive and the impact on inverter output distortion is evaluated. Finally, potential solutions for performing simultaneous switching avoidance in arbitrary n-phase converter systems are identified and compared with a focus on implementation complexity.

Research Overview

This work focuses on the development of control techniques to avoid simultaneous or overlapping switching instances from occurring in three-phase motor drives.

To date, there has been some investigation of the effects of simultaneous switching [13], [14] for a general multi-output converter. This work showed how switching transients become coupled due to parasitic inductance resulting in increased voltage stresses and switching losses as the number of overlapping phases increases. To address this, researchers proposed active gate drive control techniques to keep di/dt and voltage stresses below specified limits. In addition, [20] presents a patent for digital gate drive hardware that blocks switching events from occurring to closely in time. As such, previous work has focused on hardware-based solutions.

In this research, techniques for avoiding simultaneous switching through control software are developed for application in three-phase motor drives specifically. To inform the design of these methods, switching transient measurements are performed for the potential simultaneous switching events that can occur between phases of a three-phase inverter (intra-inverter simultaneous switching). Using this knowledge, two approaches are developed to perform simultaneous switching avoidance in software, a PWM-based solution and an voltage-error-based solution. These two approaches are compared with respect to their impact on inverter output harmonics as well as the restrictions they impose on controller performance and inter-inverter simultaneous switching avoidance algorithm design.

Research Contributions

The key contribution of this work is the development of methods for performing intra-inverter simultaneous switching avoidance in real-time. Taking two different approaches, one implemented in the PWM modulator and another in the closed-loop control scheme itself, simultaneous switching avoidance algorithms are developed with differing pros and cons with respect to implementation as well as the resulting additional harmonic content introduced to the inverter's output.

To inform the design and analysis of these algorithms, a comprehensive evaluation of simultaneous switching events and their impacts on DC link di/dt, transient voltage stress, and power losses is presented. This evaluation shows that minimal separation is required in order to effectively null any coupling effects between switching transients.

In addition, a method for properly compensating for deadtime effects in the context of simultaneous switching avoidance is proposed and evaluation. Using this approach commutation timing uncertainty introduced by deadtime insertion can be properly handled and the amount of enforced switching separation provided by the avoidance methods can be decreased.

Finally, this work shows that, while additional harmonic distortion is necessarily introduced by both simultaneous switching avoidance methods there is no significant impact on current regulator bandwidth and stability under the cases tested.

Summary of Chapters

In Chapter 1, a state-of-the-art review is given for power electronic switching transients, coupling effects during simultaneous switching transient effects and existing mitigation and avoidance methods. In addition, existing current and torque control schemes for three-phase machines are reviewed as well as three-phase pulsewidth modulation schemes.

In Chapter 2, a comprehensive analysis of the potential simultaneous or overlapping switching transients within a multi-phase inverter is performed. The impact on DC link di/dt and the resulting voltage stress coupling and switching losses are presented.

In Chapter 3, simplified switching transient models are developed to enable estimation of simultaneous switching effects in a particular converter design at the early stages of the design process. These models can serve to provide engineers with a clearer understanding of the design trade-offs in selecting a particular switching speed and the resulting impact of parasitic inductance and decoupling capacitor sizing under the possibility of simultaneous switching.

In Chapter 4, the probability of switching overlaps occurring for single and two, three-phase inverter systems are analyzed using geometric and simulation-based methods across one electrical cycle of a steady-state, rotating command vector.

In Chapter 5, an error-vector-based SSA method is developed as an alternative approach to the previously developed APWM-SSA method. A compensation scheme is also developed to decouple the effect of voltage errors on closed-loop performance. Simulations are used to identify and compare the impacts of the APWM and EV-SSA methods on inverter output current.

In Chapter 6, a method for properly handling deadtime effects in the context of SSA is proposed. This is then evaluated experimentally to show the reduction in necessary enforced switching separation that can be achieved.

In Chapter 7, the proposed intra-inverter SSA methods are implemented in an IFOC-CVCR induction machine drive. Experimental evaluation of the SSA methods is presented to identify their impact on current regulator bandwidth and stability, as well as to verify simulation results of the current waveform distortion and harmonic spectral content.

In Chapter 8, potential methods for performing simultaneous switching avoidance in n-phase converter systems are explored. This is done first using the specific example of a two, three-phase inverter system. The resulting approaches are then extended to arbitrary n-phase systems and the design trade-offs of each solution approach are compared with respect to their implementation complexity.

In Chapter 9, the key conclusions and contributions of this work are presented, followed by recommendations for future work.

Chapter 1 State-of-the-Art Review

This chapter discusses the state-of-the-art for a collection of topics that pertain to simultaneous switching transient effects and control methods for avoiding these events. This begins by reviewing switching transient modelling used for piecewise single-phase transient waveform modelling. Then, existing research regarding simultaneous switching events is presented as well as hardware-based techniques for controlling switching transients. Next, PWM methods used in three-phase, voltage-source inverters is presented followed by PWM techniques for avoiding simultaneous switching events. Finally, existing torque and current control techniques for controlling power conversion in the electric machine are reviewed and opportunities for performing simultaneous switching avoidance in the closed-loop control architecture are identified.

1.1 Semiconductor Switching Transient Modeling and Control

The methods used in previous research to model semiconductor terminal voltage and current waveforms during switching transients were reviewed as follows. They are presented first for the ideal case and then extended to the case where parasitic inductance is present in a converter's commutation loop. Further, modelling approaches for including output and decoupling capacitance effects are identified. Next, research documenting the effects of simultaneous switching on voltage stress and power losses is presented. Active and passive methods for shaping switching transient waveforms through gate drive circuit design are presented. Finally, the current state-of-the-art in DC link busbar and power electronic module design is outlined to better understand realistic ranges of parasitic inductance in modern power converters.

1.1.1 Power Diode

Beginning with the passive diode, switching events are controlled by the voltage polarity appearing across the anode and cathode terminals. When the diode's terminal voltage is negative it is said to be reverse-biased and the diode is blocking current. When the terminal voltage is positive, the diode is forward-biased and allows for continuous conduction of forward current [1].

Time-domain current and voltage waveforms for the diode's transients are shown in Fig. 1-1, where t_1 and t_2 mark the transition from reverse to forward-biased and t_3 through t_5 denote the reverse to forward-biased transition.

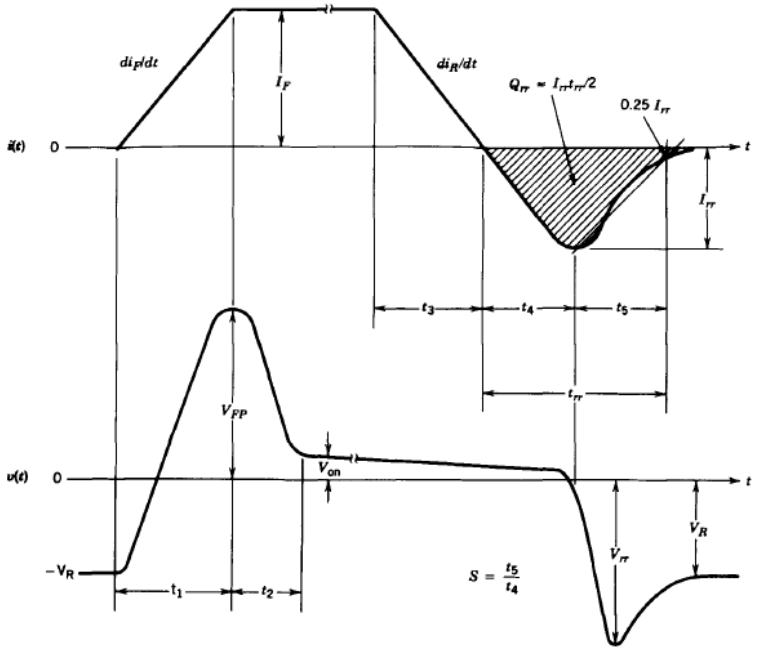


Figure 1-1: Time-domain current and voltage waveforms for a power diode during turn-on and turn-off transients [1].

During the diode's turn-off transient, the terminal voltage overshoots the steady-state blocking voltage. This overshoot is shown in t_5. As the diode's terminal voltage polarity changes sign, carriers are removed at a finite rate from the device's drift region. Because current is required to remove completely these carriers, a negative reverse-recovery current flows through the device. Current reaches a peak value (I_{rr}) before rapidly falling back to zero as the drift-region carrier-concentration returns its off-state value. As the current decreases to zero, any parasitic inductance in the device leads and/or between the device and input power source will result in an observed voltage overshoot as measured across the device leads.

1.1.2 MOSFET and IGBT

In contrast to the passive diode, active power devices present a second form of switching transient that will be present in inverter commutation events. In the scope of this thesis, active devices take the form of either the MOSFET or IGBT. They are capable of current and voltage

levels sufficient for low and medium power drive applications. In both devices, an external gating voltage is applied to the gate terminal which is used to control their electrical states. At each rising or falling edge of the gate voltage (V_g) the MOSFET or IGBT will undergo a switching transient from on-state to off-state, or vice-versa. These gate-controlled turn-on properties can be modelled as capacitive in nature for both devices. Qualitatively, the switching transient waveforms are largely similar for both MOSFET and IGBT. These similarities and differences will be addressed here.

To understand the properties of a MOSFET's switching transient, equivalent circuit models have been developed, based on its physical structure. A MOSFET is formed with three external terminals: a source, drain, and gate. When a positive voltage of sufficient magnitude is applied between the gate and source, electrons are injected into the depletion region. Once the concentration of injected electrons is sufficient current can flow from drain to source, and the device is in its "on" state. For the device to turn off and block current again, the injected electrons must be removed from the depletion region by shorting, or applying a negative voltage to, the gate and source terminals. Once a sufficient quantity of electrons has been removed, the electric potential barrier blocking current flow is reestablished. (This overview is a simplification of those found in the literature. For an in-depth description of power semiconductor device physics, see [1].) Due to this capacitive nature of the MOSFET (charging and discharging of the depletion region through the gate terminal), most lumped-parameter MOSFET equivalent circuit models are formed using capacitances to model the charge between the drain and source, drain and gate, and drain and source. These capacitances are termed C_{ds}, C_{gd} and C_{ds}, respectively.

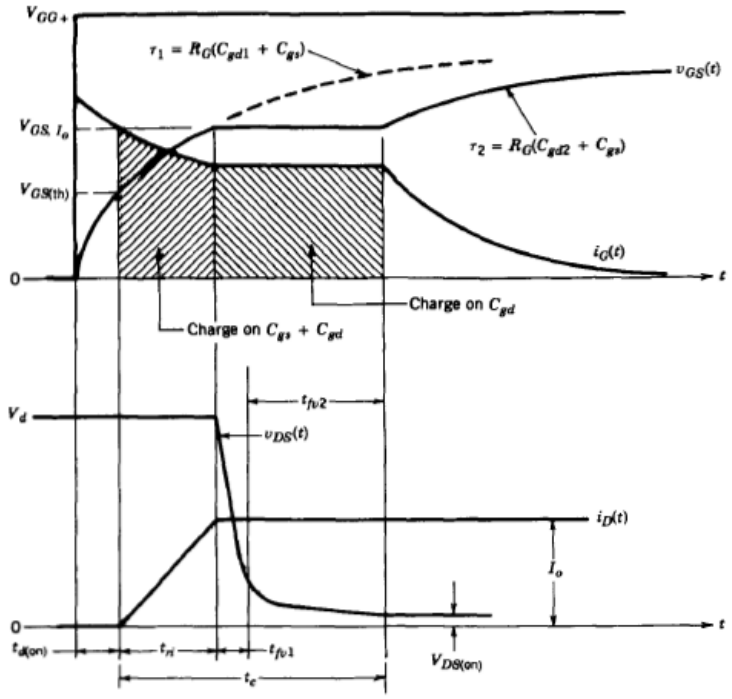


Figure 1-2: Gate-to-source current and voltage waveforms (top) and drain-to-source voltage and current waveforms (bottom) for a MOSFET during turn-on [1].

To initiate a turn-on transient, a positive gate voltage is applied externally to the device terminals. This leads to a positive gate current which begins to charge the MOSFET's input capacitance, C_{gs} and C_{gd}. This charging behavior is a result of majority carriers building up in the depletion layer to form a conducting channel. During this process, V_{gs} increases at a rate governed by the circuit time constant defined by C_{gs}, C_{gd} and R_g, where R_g is the total resistance between the positive and negative terminals of the applied V_{gs}. Once V_{gs} reaches the device's threshold voltage (V_t), I_d begins to increase. Due to I_d beginning to flow before V_{ds} falls from its blocking-state value, there is measurable power loss during this transient. This loss is referred to as switching loss [1]. This is shown in Fig, 1-2.

The MOSFET's turn-off transient can be understood by reversing the turn-on transient sequence. The turn-off transient is initiated when the externally-applied gate-to-source voltage goes below V_t. At this point, V_{gs} begins to decrease. Once V_{ds} reaches V_{DC}, I_d falls rapidly to zero from its on-state value. This rapid fall in I_d results in a large rate-of-change in current on the DC bus supplying the device. Once I_d is extinguished, the MOSFET is in its off-state.

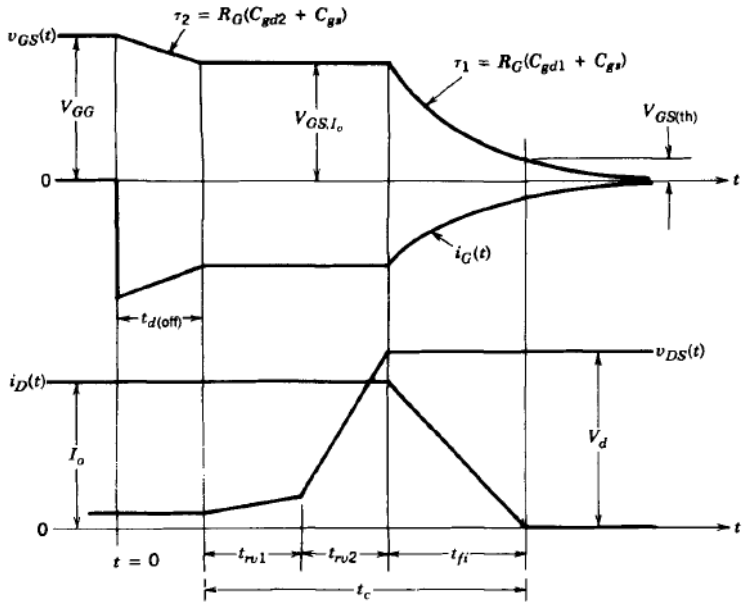


Figure 1-3: Gate-to-source current and voltage waveforms (top) and drain-to-source voltage and current waveforms (bottom) for a MOSFET during turn-off [1].

The structure of an IGBT is like the MOSFET and is also formed with three terminals: a gate, source, and emitter. However, in the IGBT, a BJT structure is inserted between the emitter terminal and the MOSFET structure. The addition of this BJT structure allows for higher off-state blocking voltages in the IGBT without forcing excessive on-state losses. The conductivity of the BJT structure is controlled by current flowing through the MOSFET structure. Consequently, once current begins to flow through the MOSFET structure the BJT structure also becomes forward-biased. The IGBT is made suitable for higher power levels. However, it does also result in slower switching transients, particularly during turn-off [1].

The beginning of the IGBT's turn-off transient sequence is once again identical to that of the MOSFET (input capacitance discharging through V_{ge}, V_{ce} rise to V_{DC}). I_c begins to fall as the current supported by the MOSFET structure is shut off. This occurs rather quickly, since the MOSFET is a majority carrier device. Moreover, IGBT's are often designed to maximize the amount of current flowing through the MOSFET structure. So, this initial current drop makes up most the on-state value (Fig. 1-4). The current flowing through the BJT structure is supported through stored charge in its drift region. (This is analogous to the diode's turn-off.) Since there is

no path for this stored charge to be removed back through the MOSFET, this charge decays in the form a "tail current" as shown in Fig. 1-4. During this tail-current decay period, the conductivity of the BJT's drift region is reduced, and it can be simplistically modeled as a non-linear resistor. The extended tail current decay property leads to an increase in both turn-off losses and turn-off transient duration [1].

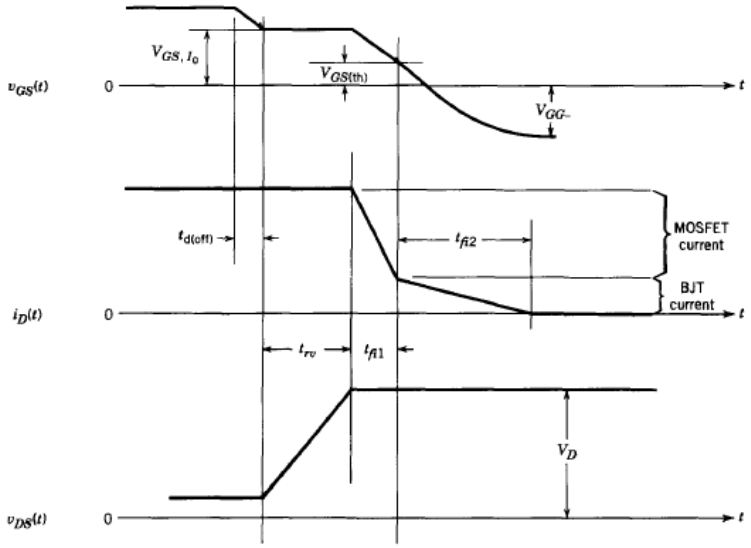


Figure 1-4: Turn-off transient waveforms for an IGBT highlighting the current separation between an IGBT's internal MOSFET and BJT structures [1].

1.1.3 Converter Commutation with Parasitic Commutation Loop Inductance

The previous piecewise waveform models using lumped-parameter equivalent circuits were used to describe switching transient waveforms for diodes, MOSFETs and IGBTs under ideal conditions. However, due to the relatively fast switching transients of modern power electronics (on the order of 10's to 100's of [ns]) even a small amount of parasitic inductance in the commutation loop path will result in unwanted voltage spikes as measured across the switching device terminals. Researchers have proposed methods using similar piecewise analysis approaches to approximate the effects of parasitic inductance on commutation events [2-7]. Using these tools, researchers have primarily sought to quantify the effects of parasitic inductance on voltage stresses, switching losses, and EMI. In this section, a piecewise, lumped-parameter model is presented which models current commutation between an IGBT and diode under parasitic

inductance effects. While models can differ slightly based on the actual devices used, they reach similar conclusions regarding parasitic inductance effects [2-7].

Forming the basis for this analysis, an equivalent circuit model as shown in Fig 1-5 is typically used. In this figure, a lumped inductance, L_s, is placed in the path of the DC bus to model any parasitic inductances in the DC link circuit. Thus, as the IGBT turns on and off, there will be changes in the current flowing through this inductance and a resulting change in voltage across it. Using this model, effects of parasitic inductance on switching transient waveforms can be derived.

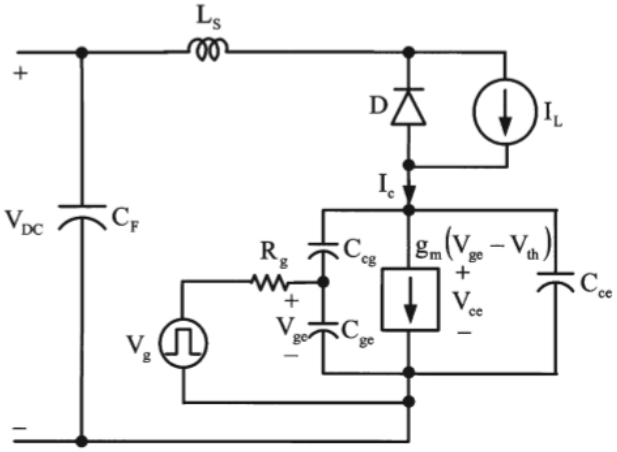


Figure 1-5: Equivalent circuit used to model an IGBT switching transient under the effect of parasitic commutation loop inductance [2].

IGBT Turn-on Transient

Starting with the IGBT turn-on transient, the circuit begins in a state where the diode is forward-biased and conducting the converter's load current. Meanwhile, the IGBT is blocking the full DC bus voltage, V_{DC}. The general form of the transient remains the same as before. As current begins to flow through the IGBT, L_s will cause an inductive voltage drop proportional to $\frac{dI_c}{dt}$ as shown in (1.1-2). Due to the polarity of this current rate-of-change, this inductive voltage drop will lower the total DC bus voltage, as seen by blocking devices downstream of L_s. This can be seen in the time segment τ_1 in Fig 1-6 [2].

Once the diode has reached its maximum reverse-recovery current and its stored charge has been sufficiently removed, the reverse-recovery current quickly decays away. The rate at which this occurs depends upon can be represented as an exponential time constant as shown in (1.1-4). At this point $\frac{dI_c}{dt}$ has changed polarity and thus the inductive voltage drop across L_s increases the voltage measured across blocking devices downstream. The magnitude of this inductive voltage drop can be estimated as shown in (1.1-5).

$$\frac{dI_c}{dt}(\tau_1) = \frac{g_m(V_{gc} - V_{th})}{R_g C_{ies} + g_m L_s} \tag{1.1-1}$$

$$\Delta V_{ce}(\tau_1) = L_s \frac{dI_c}{dt}(\tau_1) \tag{1.1-2}$$

$$I_{rr} = \sqrt{2\tau_{LT} I_L \frac{dI_c}{dt}(\tau_1)} \tag{1.1-3}$$

$$\frac{dI_c}{dt}(\tau_2) = \frac{I_{rr}}{\tau_2} \tag{1.1-4}$$

$$\Delta V_s(\tau_2) = L_s \frac{dI_c}{dt}(\tau_2) \tag{1.1-5}$$

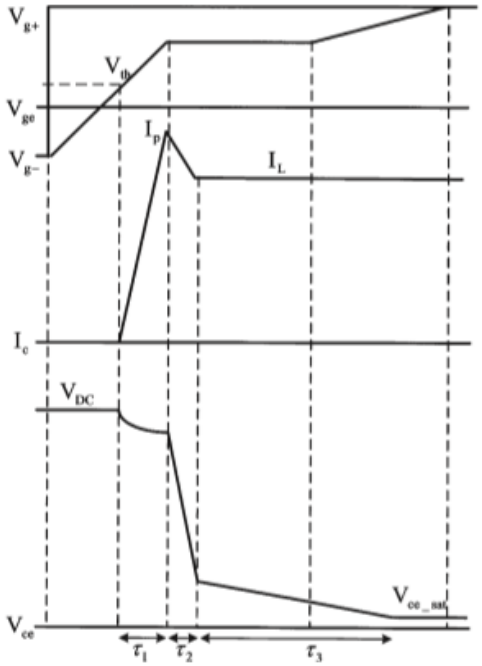


Figure 1-6: IGBT voltage and current waveforms during turn-on, as current is commutated from diode to IGBT [2].

IGBT Turn-off Transient

Moving on to the IGBT turn-off transient case, once V_{ce} reaches V_{DC}, I_c begins to fall rapidly as the IGBT's current supported by the MOSFET structure extinguishes and the diode's current increases to provide the necessary load current. The current rate-of-change during this segment can be approximated using the expression shown in (1.1-8). Because of this $\frac{dI_c}{dt}$, there is an inductive voltage drop across L_s that increases the total DC voltage experienced by downstream blocking devices. This can be seen in the plot of V_{ce} during τ_6 [2].

$$\frac{dV_{ce}}{dt}(\tau_5) = \frac{V_{th} - V_g + I_L/g_m}{R_g C_{cg}} \tag{1.1-6}$$

$$\Delta I_c(\tau_5) = -C_d \frac{dV_{ce}}{dt}(\tau_5) \tag{1.1-7}$$

$$\frac{dI_c}{dt}(\tau_6) = \frac{g_m V_g - V_{th} - I_L/g_m}{R_g C_{ies} + g_m L_s} \tag{1.1-8}$$

$$\Delta V_{ce}(\tau_6) = L_s \frac{dI_c}{dt}(\tau_6) \tag{1.1-9}$$

$$\frac{dI_c}{dt}(\tau_7) = \frac{I_{BJT}}{\tau_7} \tag{1.1-10}$$

Once the MOSFET-supported current is extinguished, the current supported by the IGBT's BJT structure decays away. While it is very difficult to accurately model this BJT tail current effect, it's decay can be simplistically modelled as an exponential decay with a time constant, τ_7, expressed in (1.1-10) and shown in Fig 1-7. Since there is a finite $\frac{dI_c}{dt}$ during this period, there will also be some voltage drop across L_s. However, the rate of this tail current decay is usually much slower than that of the MOSFET structure during τ_6.

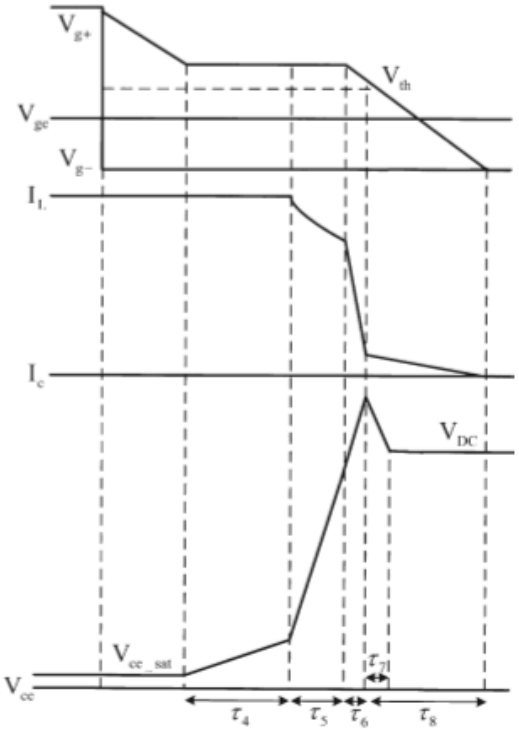


Figure 1-7: IGBT voltage and current waveforms during turn-off, as current is commutated from IGBT to Diode [2].

1.1.4 Simultaneous Switching Transients

There is relatively little published research addressing the impacts of simultaneous switching between inverter phases sharing a common DC link. However, researchers at Siemens have presented some analysis and experimental measurement of these simultaneous switching conditions. The primary focus of this work was analyzing voltage-stress and peak switching losses during diode turn-off transients [12, 13]. Some test measurements were presented for simultaneous IGBT turn-off transients as well.

An equivalent circuit model of the distributed parasitic inductances in a multi-phase inverter was formed as shown in Fig. 1-8 [12]. The model differentiates between the individual phase inductances as well as their common (or shared) parasitic inductance. The equations governing this model are presented to describe the voltage stress experienced by a diode during a simultaneous switching event (1.1-11). Applying the assumption that all devices are identical and switch simultaneously (1.1-12), a virtual inductance is defined to describe the coupling of

switching voltage stress between converter phases (1.1-14). The switching simultaneity assumption is critical for this model. If this is not true, $\frac{dI_c}{dt}$ will no longer be identical and this virtual inductance model is no longer valid.

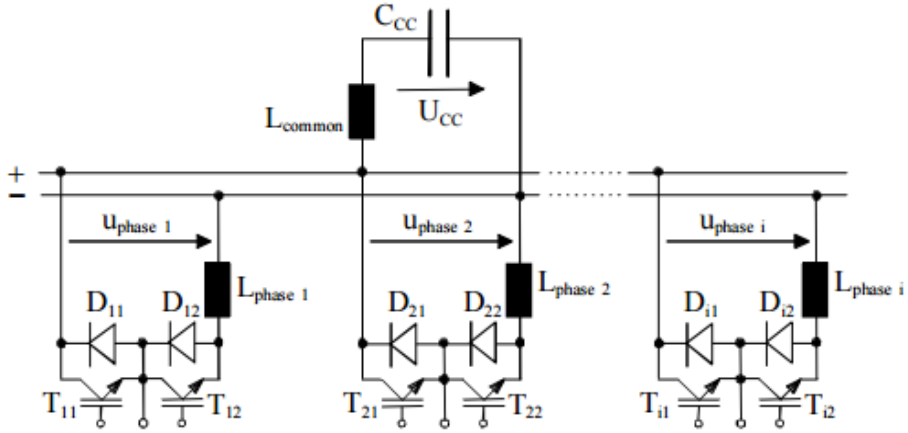


Figure 1-8: Modeling of distributed parasitic inductances in a multi-phase power converter with a common DC link [12].

$$V_{D\_i1}(t) = V_{CC}(t) - L_{Common}\sum_{j=1}^{n}\frac{dI_{c\_j2}}{dt} - L_{phase\_i}\frac{dI_{c\_j2}}{dt} \quad (1.1\text{-}11)$$

$$\frac{dI_{c\_1}}{dt} = \frac{dI_{c\_2}}{dt} = \frac{dI_{c\_n}}{dt} = \frac{dI_c}{dt} \quad (1.1\text{-}12)$$

$$V_D(t) = V_{CC}(t) - \left(nL_{Common} + L_{phase}\right)\frac{dI_c}{dt} \quad (1.1\text{-}13)$$

$$L_{Virtual} = nL_{Common} + L_{phase} \quad (1.1\text{-}14)$$

The authors constructed a high-voltage, megawatt-rated test circuit with four inverter phases sharing a common DC link. With this circuit, measurements of voltage stress, current, and switching power loss were recorded for different combinations of diode turn-off commutations (Fig 1-9) [13]. Here, it was found that the diodes' peak reverse-recovery current, power loss, as well as phase voltage stresses all increase as the number of phases increases (Fig 1-10). For the IGBT turn-off case, experimental waveforms were presented for single-IGBT and four-IGBT turn off transients (Fig 1-11) [12]. An active gate control technique was shown to reduce the peak voltage stress during both switching cases.

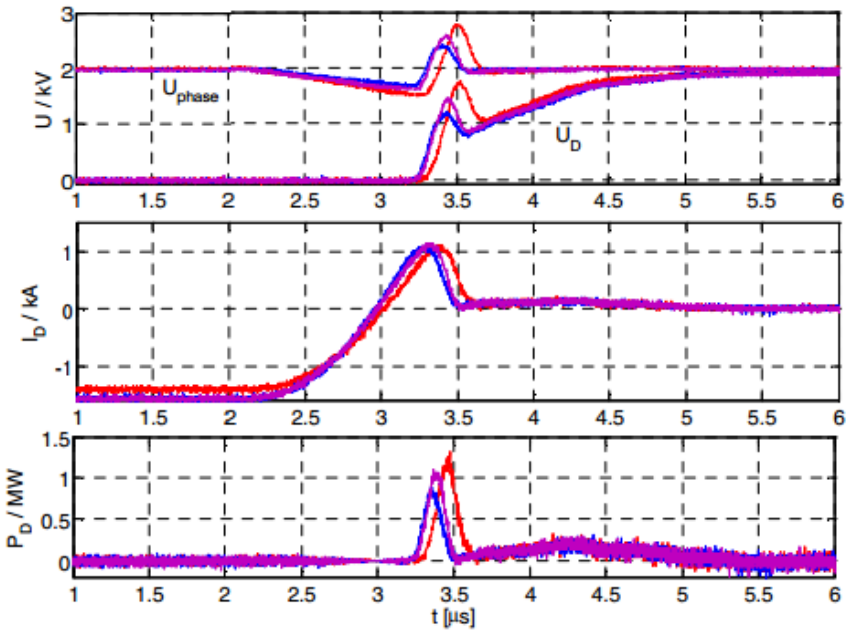


Figure 1-9: Voltage stress, diode current, and power loss waveforms during simultaneous turn-off of freewheeling diodes [13].

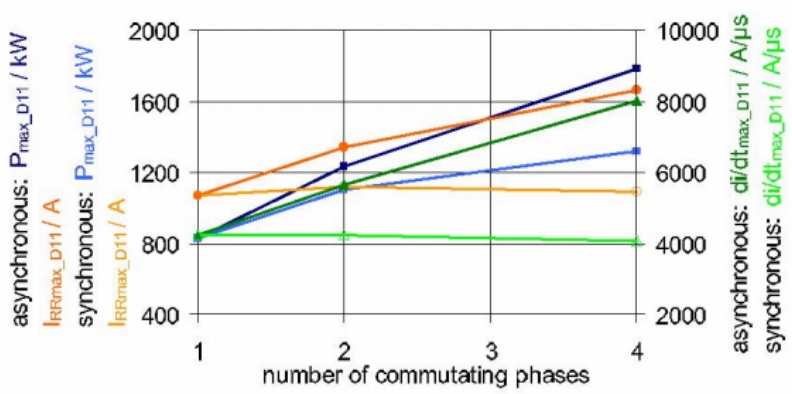


Figure 1-10: Peak rates-of-change and reverse-recovery currents and power losses during simultaneous diode turn off transients [13].

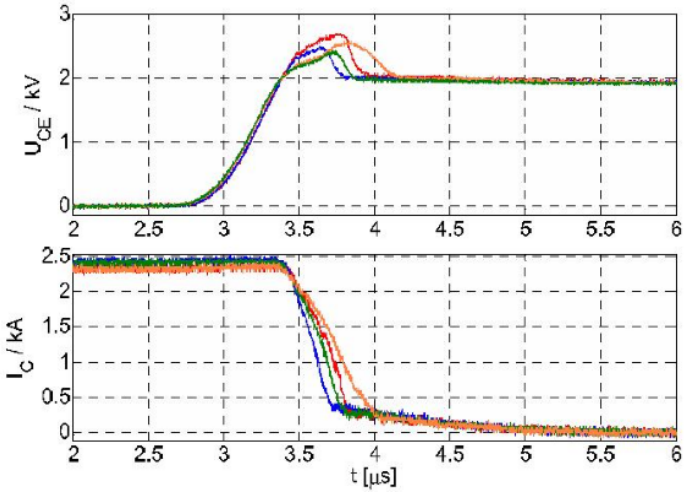
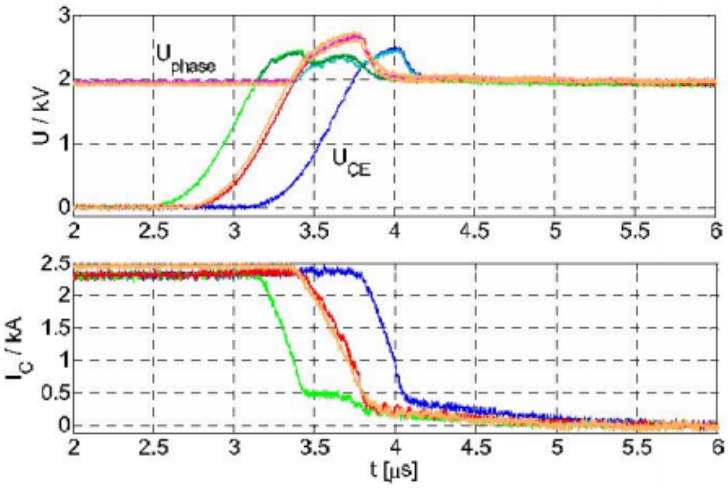


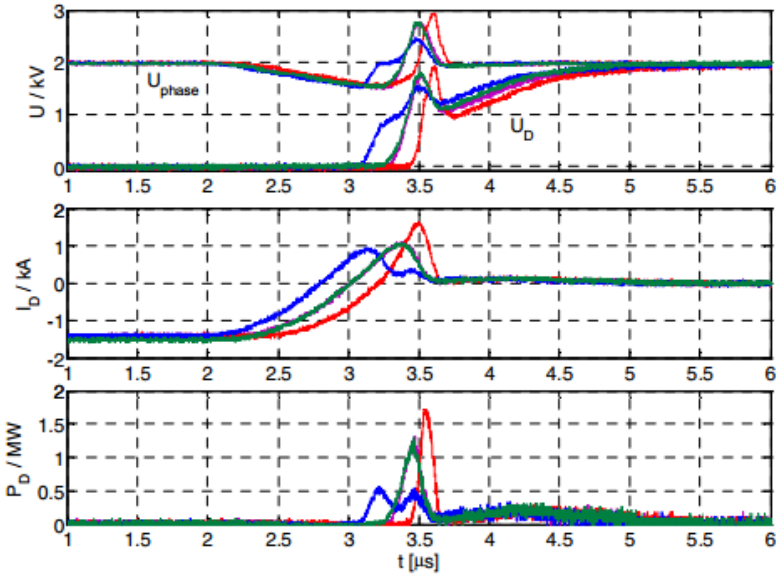
Figure 1-11: Voltage stress and current waveforms during individual and simultaneous IGBT turn-off events with passive and active gate control techniques [12].

These researchers also carried out tests for cases when the devices turned off with asynchronous, but overlapping, transients. This is shown for IGBTs in Fig 1-12 and for diodes in Fig 1-13. In both cases, a phase simultaneous transient is compared to the case when one phase switches slightly before or after. For the simultaneous IGBT turn-off case, the addition delay between switching events will decrease peak voltage stress [12]. However, in the diodes, it was found that peak reverse-recovery current and peak voltage stress increases in the case where one transient is slightly delayed [13]. This effect was credited to an acceleration of diode turn-off due to an increase in phase voltage. Peak power loss was also shown to also be a function of delay time in asynchronous diode turn-off transients (Fig 1-14)



Legend
1 IGBT Delayed
No Separation
1 IGBT Advanced

Figure 1-12: Voltage stress and current waveforms during a simultaneous 4-IGBT turn-off event as well as with some small time delay in each direction in one of the phases [12].



Legend
1 Diode Delayed
No Separation
1 Diode Advanced

Figure 1-13: Voltage stress and current waveforms during a simultaneous 4-diode turn-off event as well as with some small time delay in each direction in one of the phases [13].

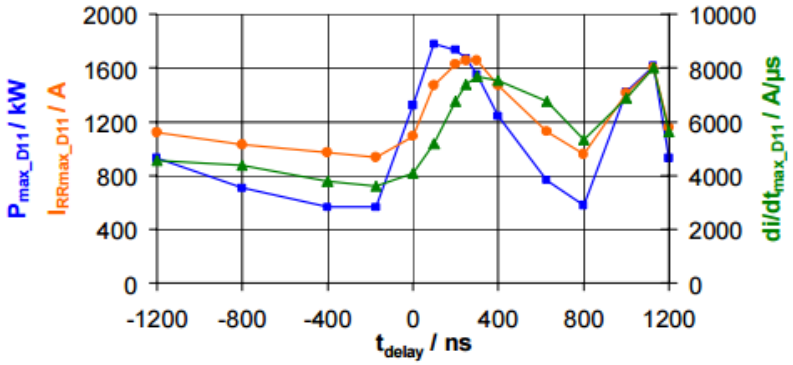


Figure 1-14: Peak diode currents and power loss during 4 diode turn-off event as delay is introduced to one of the diode's turn-off [13].

Moving on to work conducted at WEMPEC, [14] presents an evaluation of simultaneous switching voltage stresses for a low power test case. Here the total output of each phase was on the order of 100W with a 20V DC bus. In this work, the effect of load current and switching transient separation was the primary focus. In addition, These effects were investigated using both MOSFETs and IGBTs as active devices.

In [14], simultaneous switching of MOSFETs, IGBTs or diodes all resulted in increased voltage stresses. Moreover, this effect increased as the load current being commutated increased in magnitude (Fig 1-16). Simultaneous switching also caused increased ringing during turn-off, particularly for the MOSFET (Figure 1-17).

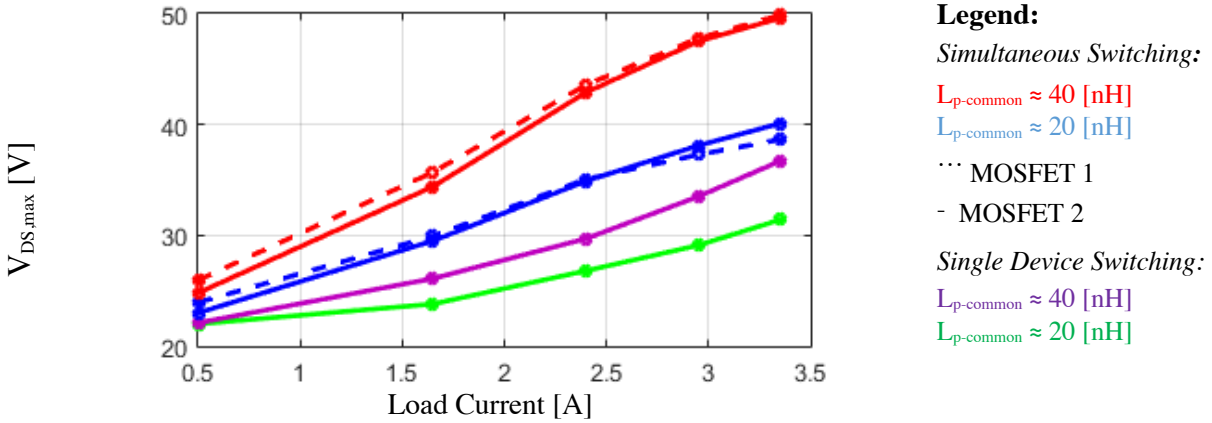


Figure 1-15: Peak MOSFET voltage stress during single and simultaneous turn-off transients [14].

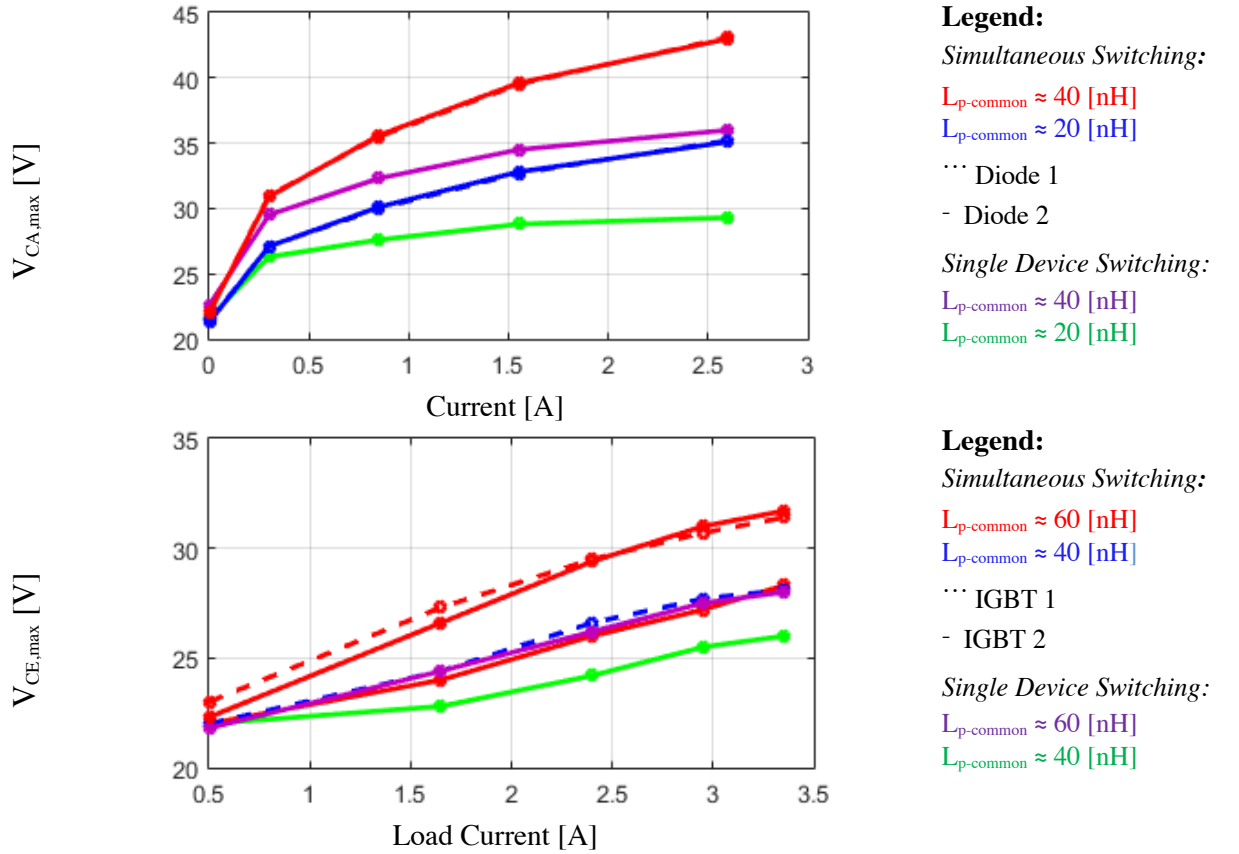


Figure 1-16: Peak voltage stress during simultaneous diode turn-off transients (top) and IGBT turn-offs (bottom)[14].

Finally, for developing SSA algorithms, [14] shows that the addition of small separations in switching instances effectively eliminates this increase in voltage stress. This holds true for the MOSFET, IGBT, and diode transients and is shown in fig 1-18.

While the work in [14] helps to broaden the understanding of simultaneous switching effects beyond those shown in [12] and [13], It does have some limitations. First, the operating power output of this circuit was in the 100's of W, which is quite small considering the range of power levels used in real-world applications. Moreover, the DC bus voltage was well below the rated blocking voltage of the devices. Second, current measurements were not taken, so understanding the impact of di/dt in the DC bus structure was not provided. Finally, due to duty cycle resolution limits in the controller used for these tests, separation time could only be added in increments of

20 ns. This is fairly large compared to the transient duration time, so it doesn't allow for in-depth understanding of separation effects on switching transients.

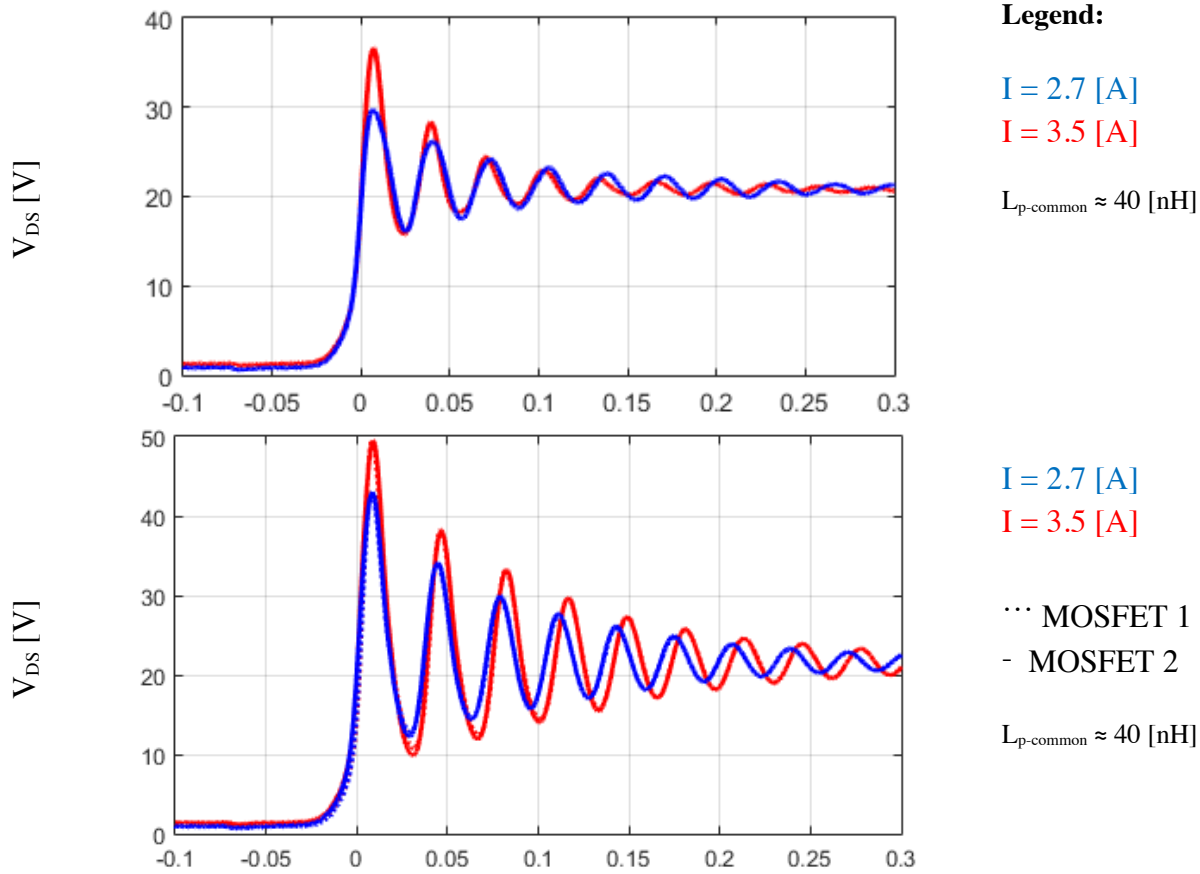


Figure 1-17: Single-MOSFET (top) and simultaneous-MOSFET turn-off voltage transient waveforms (bottom) at two different load current levels with added parasitic inductance [14].

While the amount of previous research into simultaneous switching transient is limited, the results presented based in [12], [13], and [14] show the impact of this simultaneous switching of power electronics on switching transient voltage stress and power loss. In the next section, methods for controlling switching transient waveforms through both passive and active gate drives, particularly power loss and voltage stress, will be presented.

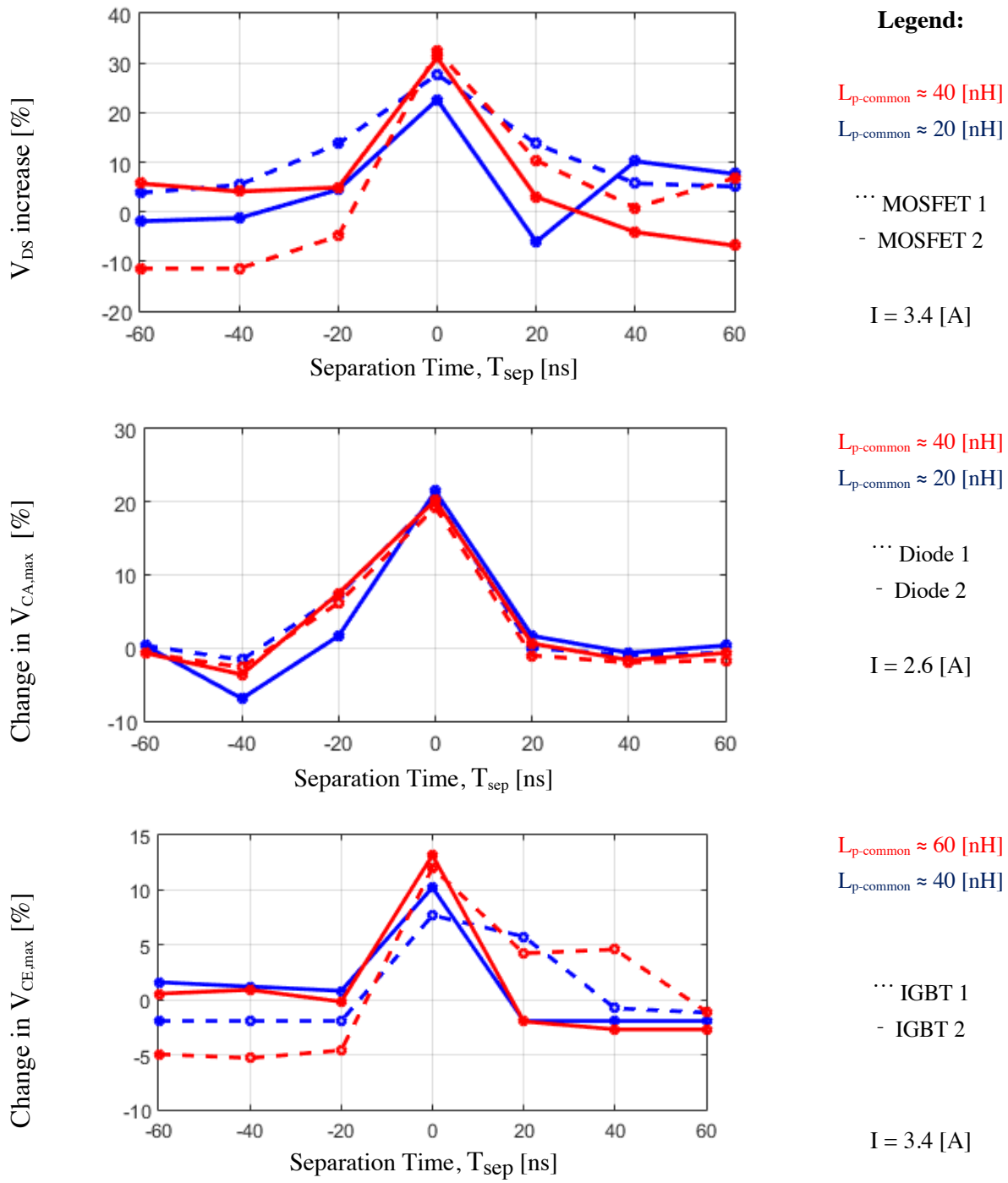


Figure 1-18: Impact of switching separation on peak voltage stresses for overlapping MOSFET (top) diode (middle) and IGBT (bottom) turn-off waveforms.

1.1.5 Switching Transient Modeling Including Device Output and Decoupling Capacitances Using Current Source Excitation

The switching models reviewed thus far assume that the commutation loop parasitic inductances are the only energy storage element impacting a circuit's switching transient dynamics. This is a useful assumption for simple approximations of voltage overshoot, it fails to consider the capacitances that are present in the circuit and impact transient behavior.

The first source of capacitance that should be considered is the output capacitance, C_{oss}, of the switching device [58]. This parameter represents the capacitance seen by the commutation loop circuit. While this capacitance is a nonlinear function of the voltage seen by the device, it does flatten at high voltages when the device is in its blocking state. This output capacitance is readily available from device datasheets and can be modeled in series with the parasitic inductance used to model the commutation loop. This capacitance value will have a strong impact on voltage overshoot estimates, particularly for MOSFET devices where the damping of the LC resonance is relatively small.

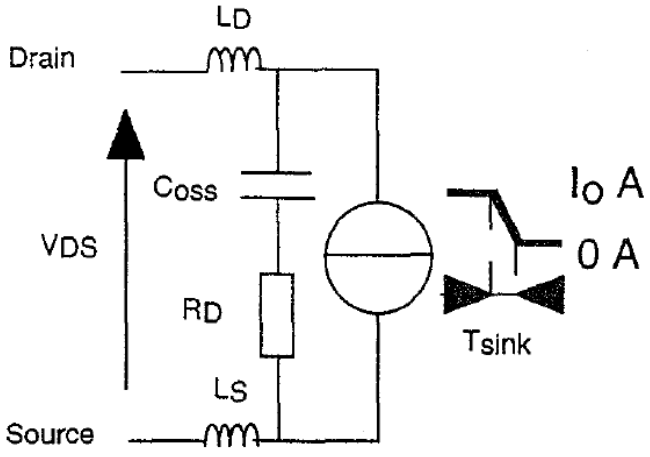


Figure 1-19: Commutation loop model including the switching device's output capacitance [58].

The second relevant capacitance to consider is decoupling capacitance that designers may place near the switching device to physically shrink the effective commutation loop and thus reduce the parasitic inductance influencing the voltage overshoot [59]. These are generally

separate from the bulk energy storage capacitance (Fig 1-20). This separation is done to enable placement of relatively small capacitors as close as possible to the switching devices. Moreover, while film or electrolytic capacitors are often used for bulk energy storage, the relatively small capacitance needed for decoupling enables to use of ceramic capacitors, which provide lower equivalent series inductance.

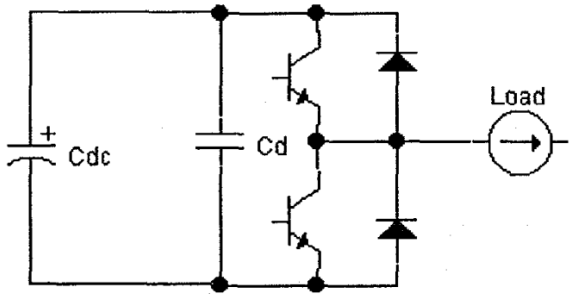


Figure 1-20: Example of the separation of bulk DC capacitance and high-frequency decoupling capacitance [59] in a power converter circuit.

Beginning simply modeling the MOSFET's turn-off under the influence of C_{oss}, [58, 63] demonstrate that voltage overshoot and oscillation can be estimated using a ramped current source model placed in parallel with the MOSFET's C_{oss} (Fig. 1-19). This model requires only three parameters, the commutation loop parasitic inductance, the device's output capacitance, and an approximation of the turn-off time used to define the ramp duration. Estimates of these values are easily obtained from approximations or FEA, device datasheets, and gate drive designs, respectively. Laplace transforms are then used to obtain a time-domain response from which a peak voltage value can be obtained.

Taking this modeling a step further, [2,60] use device parameters to define the device's di/dt as a function of gate drive parameters, trans-conductance, parasitic device capacitances and commutation loop inductance. While published work suggests this modeling approach is effective, it does require more detailed knowledge about the device's parameters as well as the converter's gate-drive design.

Moving on to the modeling of decoupling capacitors, researchers have used both time and frequency-domain analysis methods to analyze their impact on voltage stresses and to understand

their impact on DC link impedance resonances. The same time domain techniques with current source excitation to estimate voltage overshoot and oscillation profiles. [59] performed this working using simple step input models of the current transient while [61, 63] use a ramp model of the current transient. This research demonstrates that adding decoupling capacitance will lead to voltage stress reduction, but also that there is a diminishing return on voltage stress reduction by adding increasingly larger decoupling capacitance [61, 63, 64, 65].

With this diminishing return in mind, researchers have proposed a simple rule-of-thumb that C_{dec} should be at least ten times larger than C_{oss} while ratios from twenty to one hundred times larger are suggested [61, 63, 64, 65]. In doing so, the resonance caused by C_{oss} will be effectively separated from the resonance of C_{dec} and the ringing observed at the switching device terminals will be dominated by C_{oss} [64, 65].

Finally, it should be noted that the inclusion of decoupling capacitors will necessarily have an impact on electromagnetic noise spectrum of a converter. These effects are generally positive, as the decrease in peak overshoot voltage at the switching device will reduce the magnitude of high-frequency noise generated by switching events [63]. However, the addition of these decoupling capacitors introduces new resonance modes at lower frequencies that must be considered. From a system design perspective, these can certainly be addressed by properly designed EMI filtering, never-the-less it must be taken into consideration.

In addition to the change in noise spectrum, the addition of decoupling capacitors creates new paths for the converter to create radiated emissions [62]. Once again, there are some straight forward design guidelines that have been proposed by researchers [62, 66].

1.1.6 Control of Switching Transient Waveforms

The area of gate drive design is a well-established research area in the field of power electronics which allows designers to influence voltage stress during switching transients, as well as switching losses and EMI [15]. Beginning with passive methods, it has been shown that the appropriate selection of external gate resistors optimize passive gate drives for either turn-on or turn-off

transients. This can be combined with additional capacitors to form snubber circuits to mitigate the negative effects of hard-switching transients [16]. For active methods, researchers have presented both open and closed-loop methods for controlling turn-on and turn-off waveform properties. A useful block diagram summary of research in this field is shown in Fig 1-21 [15].

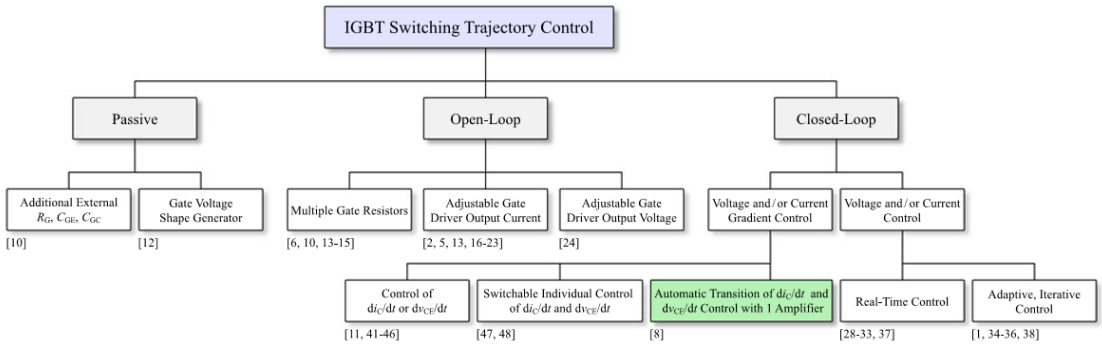


Figure 1-21: Classification of techniques for shaping IGBT switching transient trajectories through gate drive design [15].

The selection of external gate driver resistance allows for tuning of switching delays and rates-of-change by limiting the current sourced by the gate drive. This can be combined with push-pull gate drive topologies (Fig 1-22) to allow for the selection of different gate resistances for turn-off and turn-on. In [17], variations in gate resistance were shown to have a significant impact on IGBT collector current trajectories in both switching cases (Fig 1-23). Designers are able to optimize turn-on and turn-off transients through passive design by appropriate selection of gate resistance. Snubber circuits composed of passive circuit elements may also be employed to mitigate switching transient voltage stress. An example of such a circuit is shown in Fig. 1-24. A sketch of the resulting switching transients with the addition of this snubber design is shown in Fig 1-25 [1].

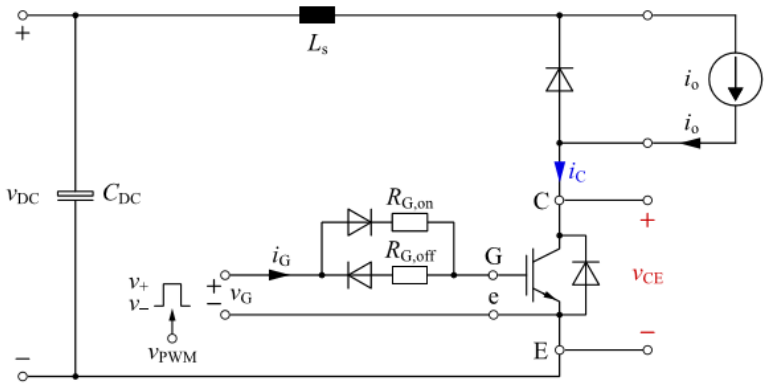


Figure 1-22: Push-pull gate driver allowing for the selection of separate turn-on and turn-off gate resistors [17].

Open-loop control techniques that control either gate current [18] or voltage [19] to optimize switching transient waveforms have also been presented in literature. In an example of open-loop current control, [18] presented a gate drive circuit that allowed for open-loop control of gate current based on a 3-stage strategy. Using this design (Fig. 1-26), charging and discharging of the gate capacitances is controlled to minimize switching delays, losses, and voltage stress. The impacts of this active gate drive design are shown in Fig. 1-27 where switching delays, losses, and voltage stress all improved compared to the conventional design. One drawback of this approach is the time-intensive calibration process for choosing voltage levels and time durations for this open-loop strategy. This calibration will inherently be unique to the particular switching device being used and the parasitic inductance it is subjected to during turn-off. Moreover, open-loop control approaches are not robust to switching device parameter variations at different load current levels and junction temperatures. So, additional control parameters must be added to handle these variations or their tuning must be carried out to address worst-case operating conditions only.

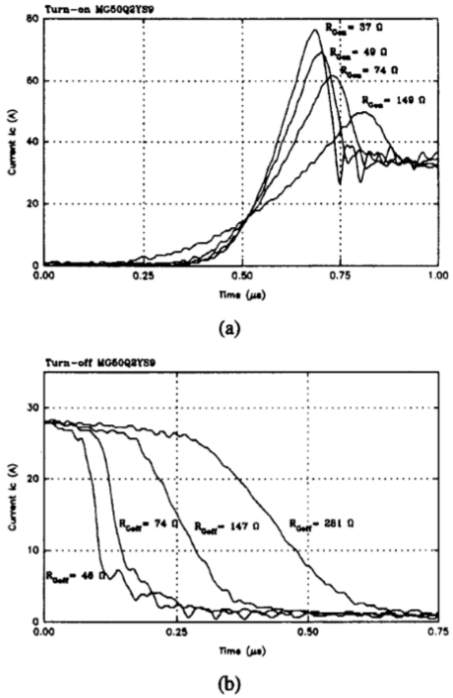


Figure 1-23: Effect of external gate resistance on IGBT turn-on (a) and turn-off (b) current waveforms [17].

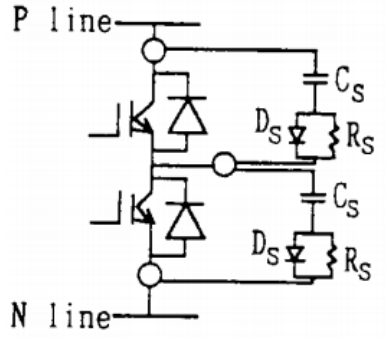


Figure 1-24: Example of a snubber circuit used to mitigate overvoltage effects during switching transients due to parasitic inductances [1].

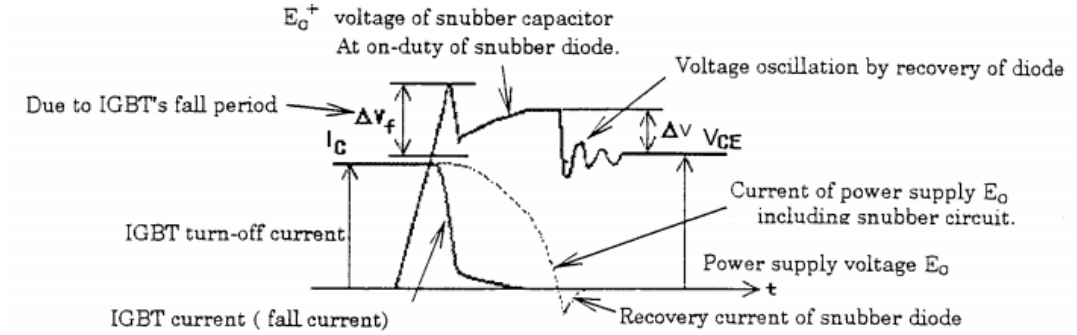


Figure 1-25: Modeling of IGBT turn-off waveforms with the incorporation of snubber circuits [1].

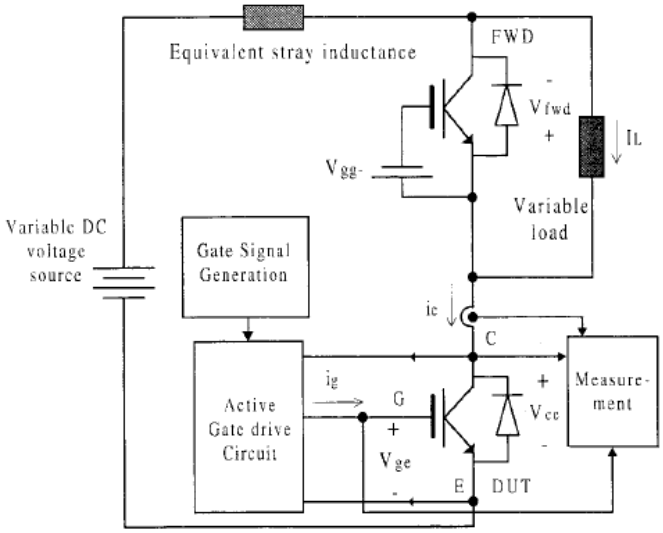


Figure 1-26: Schematic for an open-loop gate current control circuit presented in [18].

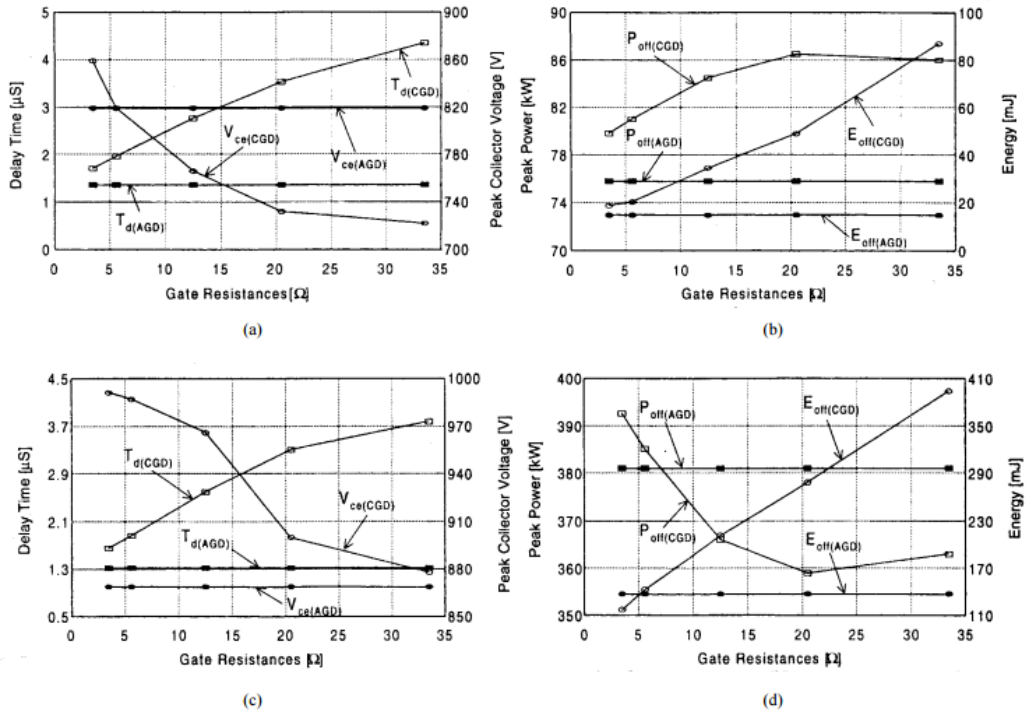


Figure 1-27: Plots of switching delays, losses and voltage stress for the conventional gate drive (CGD) and proposed active gate drive (AGD) at 150 [A] in (a) and (b), and 620 [A] in (c) and (d) [18].

Researchers have also presented methods to control collector-emitter voltage, collector current, or the rates-of-change of these states in a closed-loop fashion. These control techniques have been implemented using analog circuits and digital controllers. Analog circuitry allows for the

implementation of simple, high-bandwidth control circuits [15] while digital control methods allow for much more complex control design. Schematics of these analog and digital control methods are shown in Fig. 1-28. Both methods utilize existing or specially-placed circuit parasitics to sense the controlled states. These measurements can then be compared to waveform reference commands or simple limits and a controller can be formed to manipulate gate voltage to meet the control objectives. Fig 1-29 shows experimental waveforms for both di/dt and dv/dt control during turn-on and turn-off switching waveforms.

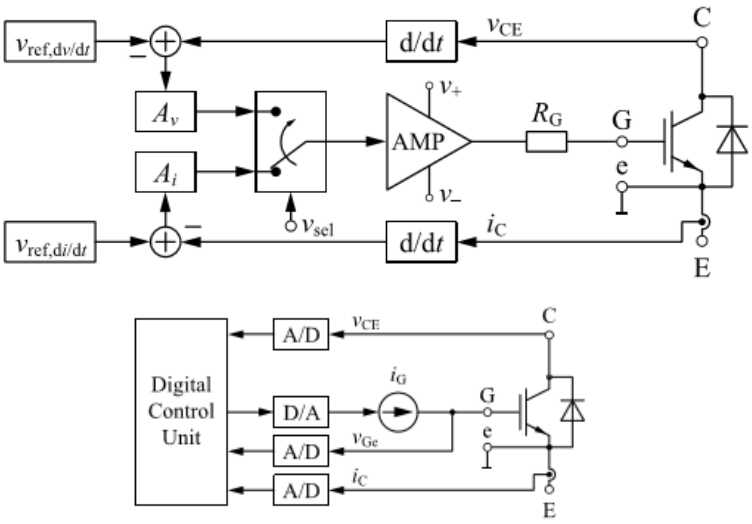


Figure 1-28: Schematic of a proposed dual active dv/dt and di/dt control gate drive in [15] using analog (top) and digital (bottom) implementations.

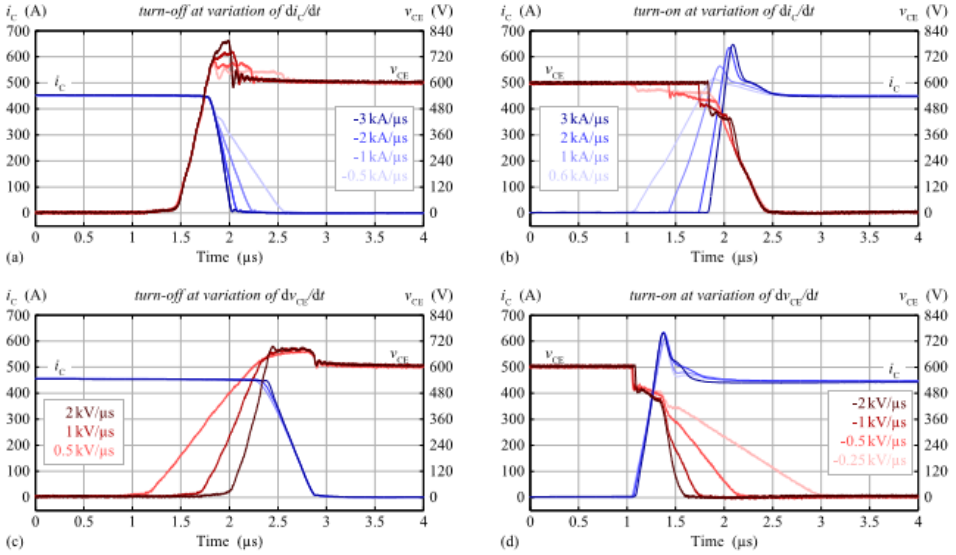


Figure 1-29: Experimental switching waveforms for active di/dt and dv/dt control in both turn-off and turn-on switching transients using the design proposed in Fig. 1-27 [15].

Both digital and analog closed-loop control approaches are subject to bandwidth requirements dictated by the power device's switching speed. Digital control approaches are inherently limited by the delays introduced by digital-to-analog conversion and vise-versa [15]. Closed-loop control does lend some forgiveness to the inevitable parameter variation that will occur between devices as well as at different junction temperatures and load current levels.

The authors of [12] and [13] proposed active gate drive control methods for mitigating the impact of these simultaneous switching events on voltage stress and switching losses. In their research, both active voltage control and active current control techniques were investigated. Schematics for these active gate drive designs are shown in Fig 1-30. Beginning with active voltage control, IGBT turn-off transient tests were carried out showing that this active collector-emitter voltage control can reduce transient voltage stress in both the single and simultaneous IGBT turn-off cases. In [13] it was shown that active control of collector current could reduce peak power losses during simultaneous diode turn-off transients compared to passive resistive gate control (Fig 1-31).

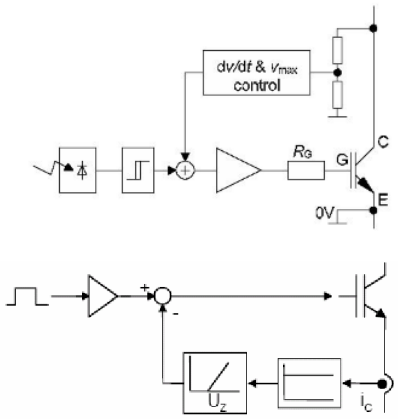


Figure 1-30: Proposed active gate control of collector-emitter voltage (top) and collector current (bottom) techniques used to mitigate simultaneous switching effects in [12] and [13].

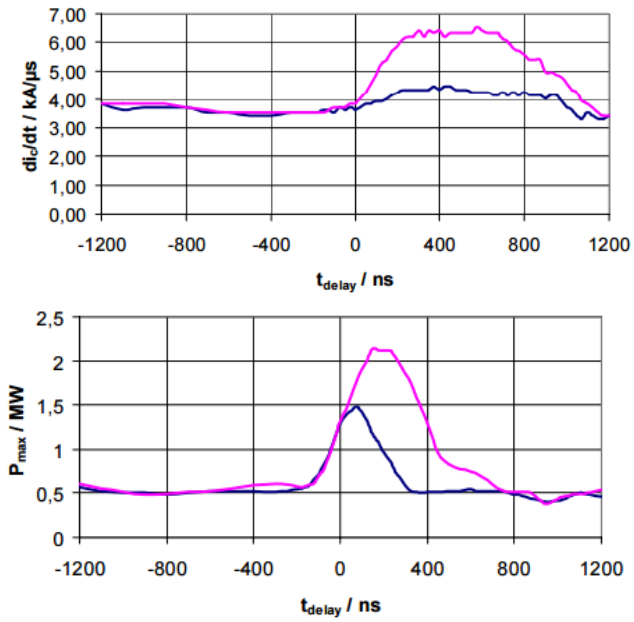


Figure 1-31: Peak collector current rate-of-change and switching power loss during simultaneous diode turn-off as a function of delay time for active and passive gate driver designs [13].

1.1.7 Parasitic Inductance Minimization in Power Converters

The sources of parasitic inductance in commutation loop circuits can be separated into two parts: busbar (or DC bus) inductance and module inductance. Busbar inductance constitutes the parasitic inductance introduced by the DC link structure used to electrically connect the DC voltage source and bulk capacitance to the power electronic module's input terminals. Module inductance consists of the parasitic inductances internal to the module itself.

Busbar design will necessarily be unique to a specific converter design, depending on the application and geometric packaging constraints. However, researchers have identified useful design rules that can be applied to any voltage source converter to minimize parasitic inductance for improved voltage overshoot and EMI performance [67-72]. This work has identified that laminated, or planar, busbar structures – with sufficiently large width-to-length ratios, are best for minimizing the self-inductance of the busbar. Further, placing the positive and negative bus rails directly on top of one another with minimal spacing between them minimizes the effective commutation loop area. In addition, minimizing the number of holes in these planes (i.e. for

placing through-hole circuit components) further reduces the effective inductance. Finally, these conductive planes can also serve to provide some shielding for reducing radiated noise. In [68-72], the effective busbar inductance using this approach are on the order of 10 to 25 [nH] depending on the physical size of the busbar structure.

As mentioned in Section 1.1.5, the parasitic inductance introduced by the DC link structure (e.g. bulk capacitance, interconnects, busbar) can be decoupled-to a certain degree-through the placement of high-frequency capacitors as close as possible to the switching devices. These decoupling capacitors can be significantly smaller than the primary DC bus capacitors and simply serve to provide a high frequency current path that minimizes the physical size, and therefore inductance, of the commutation loop. If this performed, the primary source of commutation loop inductance will come from those introduced by the power electronic module or discrete device leads.

Half-bridge or "six-pack" modules are commonly used to the single-pole, double-throw converter phase legs in industrial and automotive applications due to their design simplicity. Application notes from various suppliers and published research indicate that the inductance internal to these modules can range from 15 to 50 [nH] for conventional designs, depending on the power rating and form factor [73-76]. If discrete devices are used to construct the converter phase legs the total commutation loop inductance will be a combination of the device leads as well as the PCB traces between the device leads and the DC link structure or decoupling capacitors. Taking the range provided by [77], the device leads themselves can introduce between 5 to 15 [nH] depending on the packaging form.

In response to the continued drive for faster switching speeds, researchers have put effort into developing new module designs that optimize parasitic inductances. In [78-81], the layout of module substrates is optimized to minimize commutation loop area, achieving module inductances on the order of 5 to 10 [nH]. In [81-84], either the module substrates, DC terminal connections, or both, are stacked on top of one-another to further minimize loop areas and to bring DC link

terminal connections as close as possible to one another. Researchers taking this approach report loop inductances on the order of 2 to 5 [nH]. In [78, 80-82], decoupling capacitors are embedded within the module to help decouple inductances due to module terminals and interconnections.

1.2 Pulsewidth Modulation Methods

The design and analysis techniques used in three-phase voltage-source inverters up to the current state-of-the-art. Carrier-based Sinusoidal PWM is first presented, which can be used form a basis for further PWM development. Next, the concept of zero-sate partitioning, together with the dual approach of zero-sequence voltage injection, is identified as a key degree-of-freedom used in modern PWM techniques. Finally, modern space vector PWM methods are presented along with established techniques for analyzing the performance of these methods.

1.2.1 Sinusoidal PWM

All carrier-based PWM methods utilize a per-carrier cycle volt-second balancing principle to generate the desired voltage output over a given switching period. These be implemented using analog circuits or in digital hardware [21]. Fig 1-32 shows an example of this PWM method for the analog case. Here, an output voltage command waveform is compared to the triangular carrier waveform. At any point where the carrier waveform is greater than the command waveform, the corresponding switch is turned off. Conversely, the output is on whenever the command exceeds the carrier waveform. In this way, SPWM generates a new gating signal at each intersection point.

The existing literature presents well established theory for understanding the properties of SPWM. Assuming a sufficiently large ratio of the carrier frequency to the fundamental frequency, the fundamental component magnitude of the inverter's output voltage is linearly proportional to the command waveform's fundamental component [21]. This relationship holds true, if the command waveform magnitude does not exceed that of the carrier waveform. In the linear range, the switching frequency is fixed and is equal to the frequency of the carrier. Further, the output harmonics produced by an inverter using SPWM are well defined. Harmonic content below the switching frequency is small, and the harmonic spectrum is concentrated at integer multiples of

the switching frequency as well as their sidebands [21]. An example of this harmonic spectrum is shown in Fig 1-32.

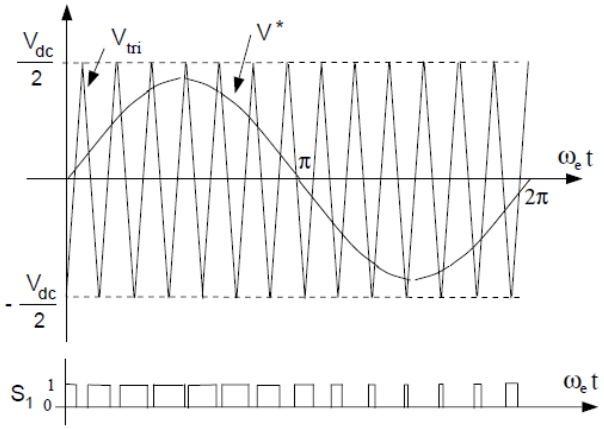


Figure 1-32: Example of the SPWM method where a sinusoidal command waveform is compared to a triangular carrier waveform. Each intersection point, corresponds to a rising or falling edge in the switch waveform [21].

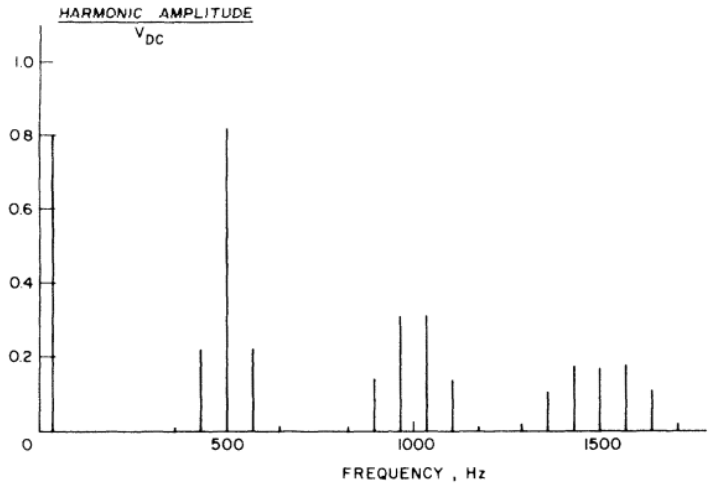


Figure 1-33: Example of an inverters output voltage harmonic spectrum using SPWM with a carrier frequency of 500 [Hz] [21].

For the case when the command waveform magnitude exceeds that of the carrier waveform, the two waveforms no longer intersect, which results in a loss of linearity between the commanded and output waveform fundamental component. This operating space is termed overmodulation and the point at which SPWM crosses into the overmodulation region is referred to as the modulator's linearity limit. For SPWM, this occurs when the commanded output is only 78.5% of the potential fundamental component of six-step operation [22]. To improve this linearity limitation in SPWM,

zero-sequence voltage injection techniques have been developed to increase the PWM linearity range for three-phase, isolated-neutral loads.

1.2.2 Zero-State Partitioning and Zero-Sequence Voltage Injection

Zero-state partitioning refers to the redistribution of time durations in which all three phases of the inverter's load are shorted together. This idea is clearly illustrated using the space vector representation of the inverter's discrete switching states. In a corollary to this concept, zero-sequence voltage injection provides a way to leverage this degree-of-freedom in carrier-based PWM. A survey of the literature shows that zero-state partitioning has become a popular and effective method to increase the linear operating range of three-phase PWM, as well as to manipulate the harmonic content produced at an inverters output.

A Three-phase VSI contains only eight discrete switching states. Taking this into account, the distribution of available output voltage vectors can be mapped onto the d-q plane [23,24]. This mapping is shown in Fig 1-34(b) and the corresponding inverter switching states are shown in Fig 1-34(a). Six of these states, called the active states, are produced when at least one phase is tied to each terminal of the DC bus. These vectors are labelled as V_1 through V_6 and connecting their vertices forms the inverter's voltage hexagon. The remaining states, V_0 and V_7, are created when all three phases are tied to either terminal of the DC bus. Since all three phases are shorted together, these show up at the origin of the dq-plane. Thus, they are called zero states. Combining all this together, the inverter can synthesize any vector within the voltage hexagon by switching between the two nearest active vectors together with the two zero-states. Taking a command vector in Sector I an example, trigonometric expressions can be derived for the active vector dwell times, T_1 and T_2 which will produce the desired output [25]. The remainder of the switching period, T_s can be distributed in any way between T_0 and T_7.

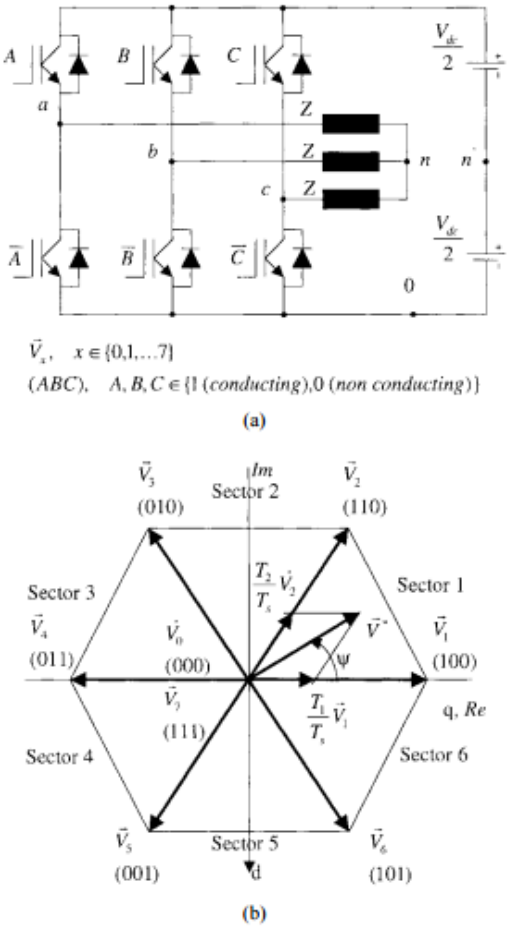


Figure 1-34: (a) Shows a circuit schematic of a three-phase inverter for which the available switching states map to the voltage hexagon shown in (b) [25].

The PWM switching waveforms that correspond to these states can be shown in the time domain for a given switching period. To minimize the effective switching frequency, transitions between states are made so that only one inverter phase switches whenever possible. In doing so, the degree-of-freedom created by the zero-state partitioning presents itself. This time domain representation is shown in Fig 1-35(a), where the degree-of-freedom in zero-state partitioning is denoted k_0. By adjusting k_0 between 0 and 1, all switching instances can be shifted symmetrically about the midpoint of the PWM period. Taking this one step further, Fig 1-35(b) shows that a set of three phase-to-neutral voltage commands can be produced, which will result in the same distribution of zero states when a carrier-based PWM implementation is used [25].

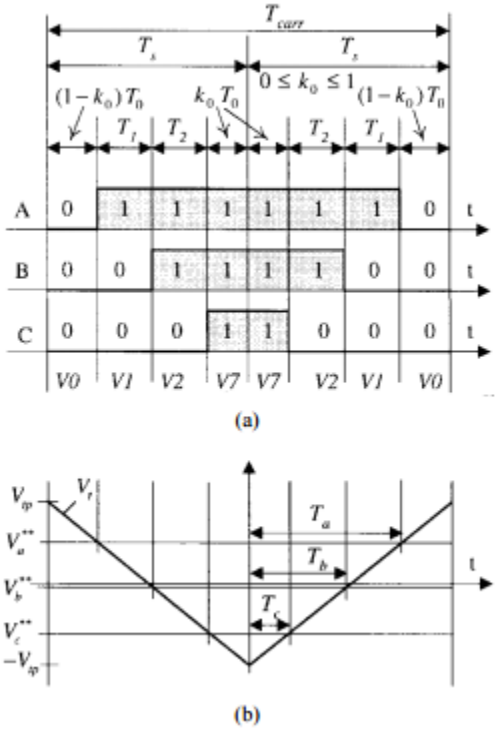


Figure 1-35: Time domain plot of the switching sequence between inverter states for a given switching period [25].

A zero-sequence voltage component can be added into all three phase-voltage commands to reproduce this degree-of-freedom. Referring again to Fig 1-34, the load's neutral is free to float with respect to the DC bus. Because of this, the addition of a zero-sequence voltage does not affect the fundamental component of the inverter output, if the phase voltage commands remain within the inverter's voltage limits [1]. Using Fig 1-35, the addition of a common component to all three voltage commands shifts the resulting carrier-wave intersections symmetrically about the midpoint of the PWM period.

1.2.3 Modern Three-Phase PWM Methods

Most modern PWM methods present in the literature can be related to one another through their use of zero-sequence voltage. This group includes methods such as Triplen Harmonic Injection PWM (THIPWM), Space Vector PWM (SVPWM), and various forms of Discontinuous PWM (DPWM). Researchers have performed comparisons of these different PWM methods with respect to output voltage linearity, output current distortion, torque and flux ripple, as well as

switching losses. Some researchers have presented hybrid PWM techniques, which transition between different PWM methods depending upon conditions.

THIPWM techniques, first introduced by King [26], are formed by injecting certain amounts of triplen harmonics into the commanded phase voltages. A similar concept was presented in [27]. The effect of this additional component is an increase in the linear range of the modulator in addition to a reduction in total switching harmonics. In [27], a method was presented for calculating an optimum magnitude of the injected third-harmonic that maximized the linear modulation region. An example of a single phase-voltage waveform with superimposed harmonics is shown in Fig 1-36. However, due to its simpler implementation, SVPWM has become the most common method for achieving this increase in output voltage [21].

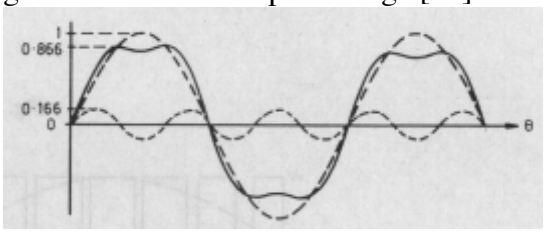


Figure 1-36: Single phase voltage waveform plotted together with the injected third harmonic zero-sequence voltage for optimal output voltage linearity range [9].

SVPWM, first presented in by Van der Broeck using the space vector switching representation [23], is formed so that the zero-state dwell times are partition equally between the two zero-states. Through this, the upper limit of the modulator's linear region is maximized. An example of a phase voltage command for SVPWM is shown in Fig 1-37. In addition to this benefit, it was also shown that SVPWM provides a significant reduction in both RMS currents and torque ripple at high modulation indices as compared to SPWM (Fig 1-38). This method can also be very easily implemented through zero-sequence voltage injection [21, 23, 25]. This value can be easily calculated each switching period in a digital controller.

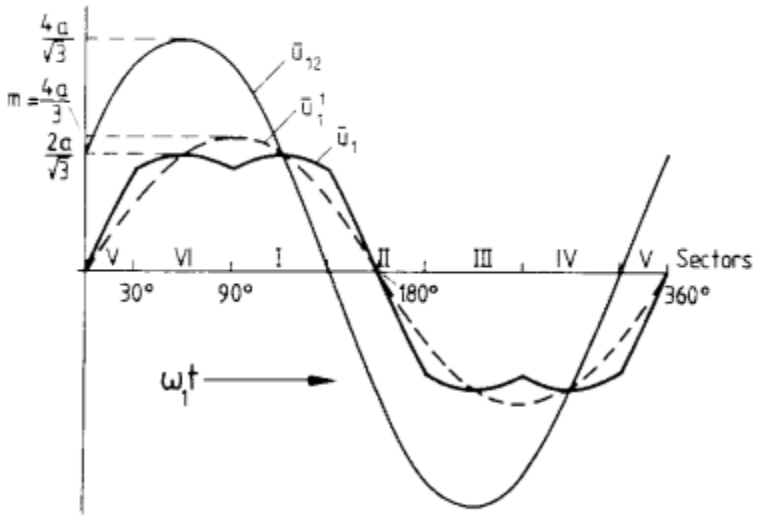


Figure 1-37: Single phase voltage waveform for SVPWM plotted together fundamental phase-to-neutral and phase-to-phase voltage components [23].

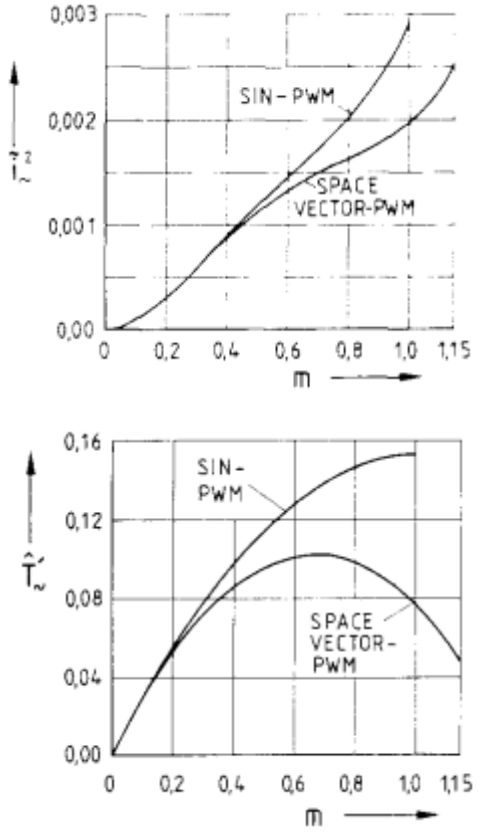


Figure 1-38: Overlaid analytical comparisons between SPWM and SVPWM with respect to output RMS Current (left) and torque ripple (right) for and induction machine operating at varied modulation indices [23].

The next advancement in PWM methods came with the development of various DPWM techniques, which are named due to the discontinuities created in the phase voltage command waveforms. For all DPWM techniques presented in the literature, these discontinuities are formed by the addition of either the maximum or minimum possible zero-sequence voltage component. This has the effect of clamping one of the three phases to either the positive or negative DC bus over an entire switching cycle. As a result, these methods are also commonly referred to as Bus Clamping PWM. Different DPWM techniques are usually differentiated based upon how DC bus clamping sequence is divided across sectors of the inverter hexagon. An extensive list of DPWM methods can be found in [21] and an example of various phase voltage waveforms for DPWM is shown in Fig 1-39. One consequence of this bus clamping approach is the effective reduction in switching frequency by one-third that takes place [21]. This has the effect of repositioning harmonic content in the frequency spectrum [28, 29]. Because this switching frequency reduction only occurs across a certain range of Θ_e, different DPWM methods produce differing switching and conduction loss variations. Using knowledge of the load's power factor, the inverter phase leg experiencing the largest current can be clamped to the DC Bus. Thus, switching losses can be reduced [21, 30].

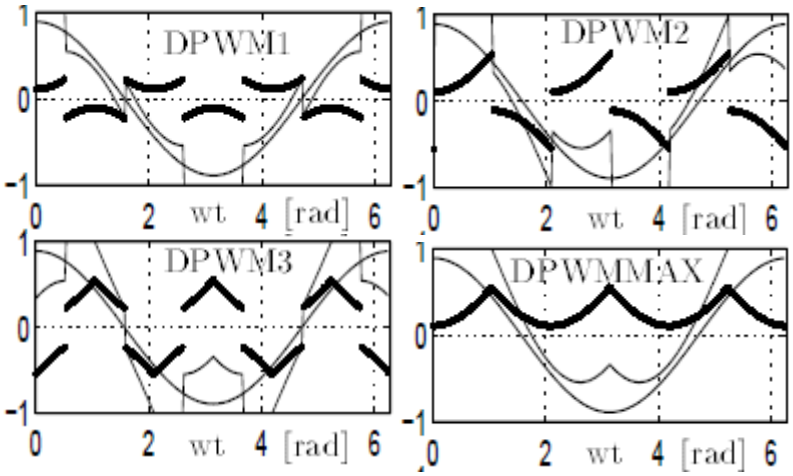


Figure 1-39: Examples of DPWM phase voltage command waveforms for different bus clamping sequences [21].

In summary, three-phase VSI PMW techniques can be implemented by comparing each phase voltage command to a common carrier waveform operating at the desired switching frequency. This results in well-defined linear operating space and resulting harmonic content. To improve both PWM linearity and harmonic distortion as well as to impact switching losses, methods to manipulate zero-sequence voltage or inverter zero-state partitioning have been introduced and their effects well documented in the literature. However, there is no evidence in the literature of research into using this available degree-of-freedom in three-phase systems for avoiding inter-inverter simultaneous switching events. Further, an additional degree-of-freedom which has not been documented in the literature is the introduction of asymmetries in PWM waveforms. This degree-of-freedom provides an opportunity to avoid intra-inverter simultaneous switching. Implementation of asymmetric PWM waveforms in hardware requires modifications to be made to existing, commonly-used, PWM architectures. In the next section, existing PWM architectures for three-phase systems will be reviewed.

1.2.3 PWM Duty Cycle Update and Current Sampling

In the previous section, the development of modern three-phase PWM techniques documented in the literature has been reviewed. In this review, a focus was placed on zero-sequence voltage injection as an available degree-of-freedom for researchers to optimize PWM techniques with respect to certain design goals. However, in the research presented so far, the impact of PWM command update timing and current sampling on inverter drive performance was ignored. In this section, research pertaining to these effects will be reviewed.

There are up to three commonly avialable interrupt sequences for updating the PWM duty cycle command and sampling the measured load currenst in commercially available DSPs for motor control applications. These can be described with respect to the triangular carrier waveform used in the PWM unit. As was covered previously, a center-aligned carrier waveform that begins and ends each switching period at the same value is used. With this, there are two convenient points for generating controller interrupts: at the beginning of a switching period or in the middle.

For the examples shown in Fig. 1-40, these correlate to the carrier waveform's valleys and peaks, respectively [31].

In the first commonly available interrupt timing, shown in Fig. 1-40(a), both duty cycle command updating and current sampling can be performed at the beginning of each switching period. This can be refered to as Single Update Mode 1. Current sensors are sampled at the k^{th} sampling instant. These measurements are then used to calculate the appropriate duty cycle commands based on the given control laws used. This calculated duty cycle is then output to the PWM generation unit and applied to the load at the k+1 sampling instant. Thus, there is a delay equal to T_s between current sampling and the controller's response to these measurements [32].

In the second available implementation, updates of duty-cycle and current sampling are staggered between the peak and valley of the carrier waveform. This can be refered to as Single Update Mode 2. As with Mode 1, the switching and control periods are equal. Using the example in Fig 1-40(b), current is sampled at the carrier's peak, defined as the k^{th} sampling instant. If this current measurement is used to calculate the control output M(k), the delay bewteen current sampling and controller response is reduced to $0.5T_s$. This form was used in [32] and resulted in improved current control bandwidth. However, if this current measurement is not used to calculate a control output until the beginning of the next switching period, the controller does not respond to the k^{th} current measurement until M(k+1) is output. As a result, there is a delay equal to $1.5T_s$ between current sampling and the controller's response to these measurements. This will necessarily cause a decrease in controller bandwidth due to the increased delay time. This was shown in [31].

The third commonly available interrupt structure, commonly referred to as double-update mode, performs duty cycle command updates and current sampling twice each switching period, at the beginning and midpoints of the switching period. This is shown in Fig. 1-40(c). In this case, the control period is reduced to half the switching period. Current sensors are sampled at the k^{th} sampling instant at the beginning of a switching period. This current measurement is then used to

calculate a new duty cycle command that is output to the PWM unit at the k+1 sampling instant at the midpoint of the same switching period. Thus, the delay between current sampling and the controller's response is reduced to $0.5T_s$ and the controller's bandwidth can be increased.

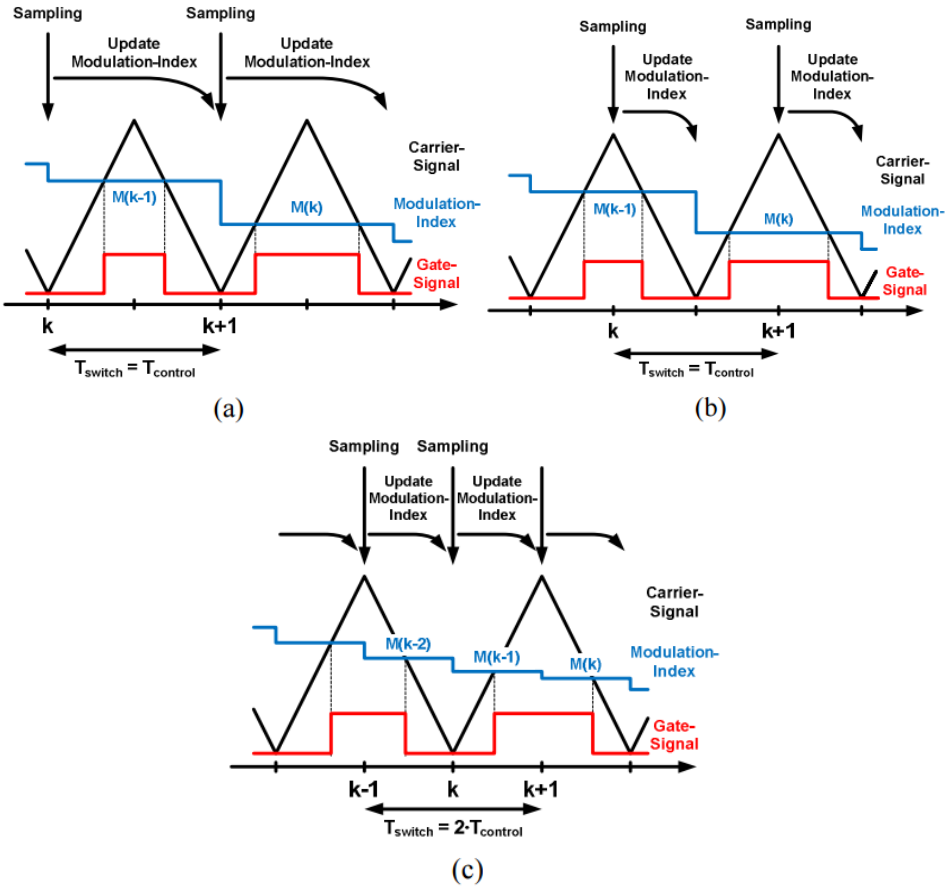


Figure 1-40: Three common forms of modulation index command and current sampling used in PWM with a center-aligned carrier waveform: single-update sampled at start (a), single-update sampled at the middle (b), and double-update double-sampled (c) [30].

single-update PWM (sampling at beginning, $f_{switch} = f_{control} = 3.5$ kHz)		
Gain	Theoretical derived	Measured
$K_{crit.}$	2.56	2.45
$f_{crit.}$	583 Hz	583 Hz
single-update PWM (sampling at middle, $f_{switch} = f_{control} = 3.5$ kHz)		
Gain	Theoretical derived	Measured
$K_{crit.}$	3.45	3.55
$f_{crit.}$	876 Hz	847 Hz
double-update PWM ($f_{switch} = 3.5$ kHz, $f_{control} = 7$ kHz)		
Gain	Theoretical derived	Measured
$K_{crit.}$	2.56	2.55
$f_{crit.}$	1166 Hz	1107 Hz

Figure 1-41: Theoretical and experimental current control bandwidths achieved in [30] using three different PWM and current sampling update schemes.

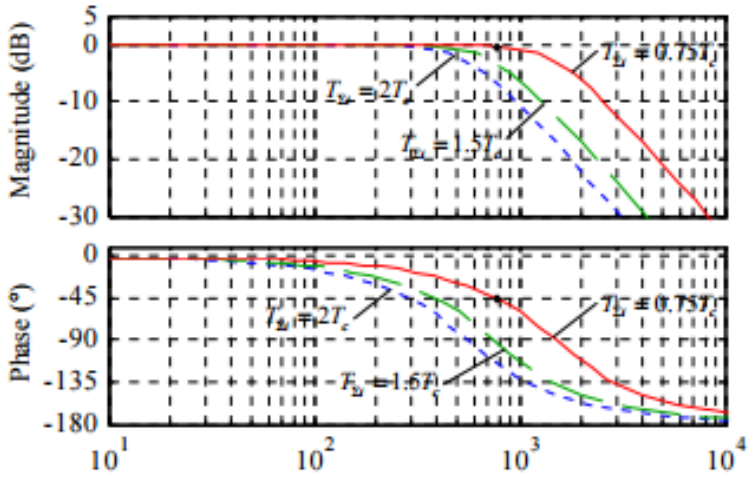


Figure 1-42: Theoretical current control frequency response plots in [31] using three different PWM and current sampling update schemes.

For the two papers cited in this section, both sets of researchers carried out theoretical controller tuning using the controller delay assumptions made previously. In [31], they showed that Double-Update PWM improved the current control bandwidth for their system by nearly a factor of two as compared to the Single-Update Mode 1 PWM. In addition Single-Update Mode 2 increased the achieved bandwidth by a factor of about 1.5. In their research, Single-Update Mode 2 was implemented so that the delay between current sampling and controller response was only $0.5T_S$. In [32], they showed similar results between Single-Update Mode 1 and Double-Update PWM where current control bandwidth was doubled. However, in this research, Single-Update Mode 2 as implemented in way that resulted in a sampling delay equal to $1.5T_S$. Thus, the

acheivable current regulator bandwidth in this case was reduced to two-thirds of that achieved using Single-Update Mode 1.

In summary, a variety of available duty cycle command and current sampling update interrupt sequences have been used by researchers to improve the available current regulator performance at a given switching frequency. Appropriately sequencing the current sampling and duty cycle update interrupts, controller delays can be reduced leading to an increase in achievable controller bandwidth. One area that has not been investigated in the literature is the use of double-update PWM to introduce asymmetries into the PWM waveform. This would provide additional degrees-of-freedom for avoiding simultaneous switching in power converters.

1.2.4 Avoidance of Simultaneous Switching Transients Using PWM Techniques

A single patent [20] was found which attempts to address the issue of simultaneous switching by avoiding it altogether. The proposed circuit does this by preventing any inverter phases from switching at the same time as others. In this proposed solution, gating signals for each phase are passed to a simultaneous-switching prevention circuit (Fig. 1-43) which introduces delays in each phase's gating signals as shown in (Fig. 1-44). While there are no published experimental results for this solution, this approach will eliminate simultaneous switching voltage stresses by avoiding the situation. However, this patent does not address the impact of these switching delays on the volt-seconds sourced by the inverter and closed-loop control of the load.

Building off this idea of avoiding any simultaneous switching events, an asymmetric PWM simultaneous switching avoidance (APWM-SSA) method was proposed in [14]. This method introduces asymmetries into the three-phase PWM waveform so that simultaneous switching is avoided without changing the average voltage applied to the load each switching period (Fig. 1-45).

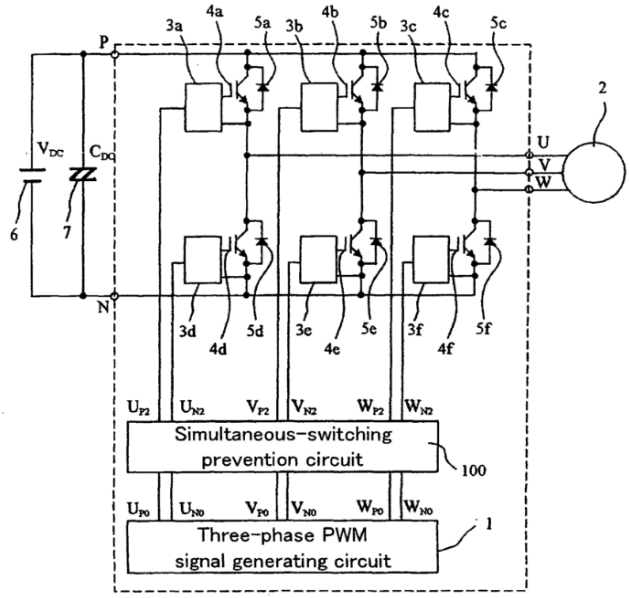


Figure 1-43: Schematic of the proposed hardware-based simultaneous switching prevention circuit presented in [20].

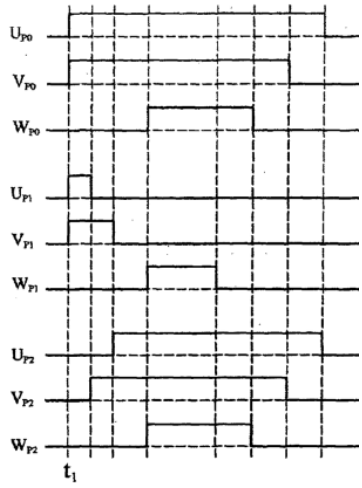


Figure 1-44: Waveforms of the simultaneous switching[20].

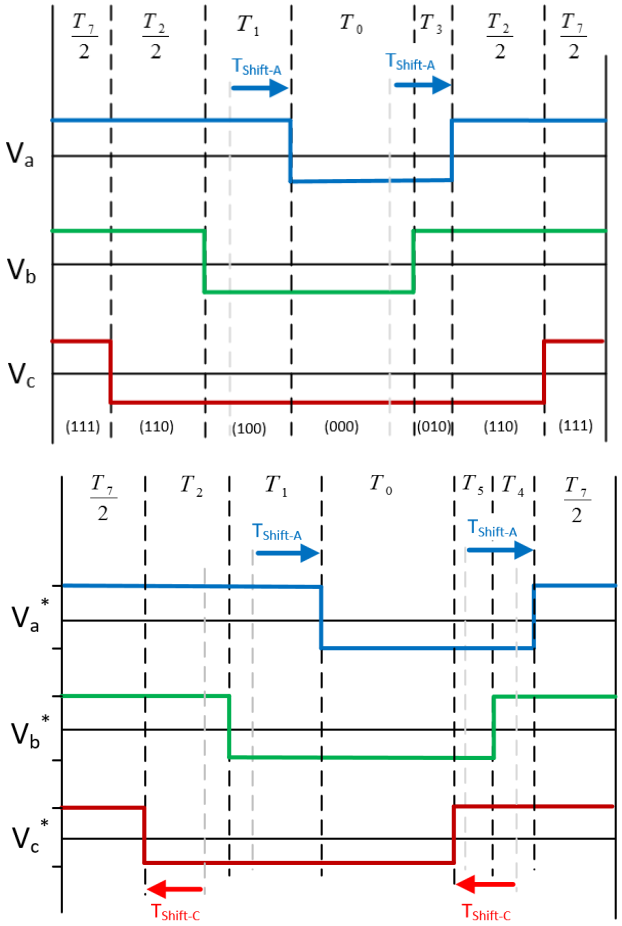


Figure 1-45: Introduction of an asymmetries for the three-active-vector and four-active-vector modes of the APWM-SSA Method [14].

To implement this APWM-SSA approach in hardware, a double-update PWM structure was used. However, rather than running the motor control loop twice each switching period, as is normally done with double-update PWM, it is only run once per switching cycle. The APWM-SSA algorithm generates two voltage commands for each phase, one for the first and second halves of the PWM period. An example of the resulting asymmetric PWM waveform generated using this approach is shown in Fig. 1-46. The relationship between the shift in switching instant timing, T_{Shift}, and the change in shift in voltage command, V_{Shift}, is shown in (1.2-1).

$$V_{Shift} = \frac{T_{Shift}}{T_{PWM}} 2V_{DC} \tag{1.2-1}$$

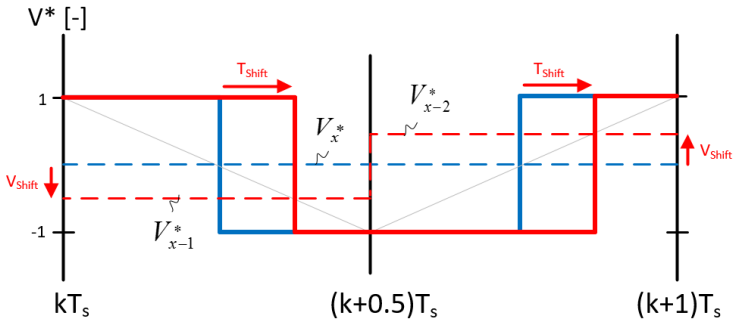


Figure 1-46: Using a double-update PWM method to introduce asymmetries into a symmetrical PWM waveform [14].

Mapping the new switching sequences from Fig 1-43 onto the inverter output hexagon and taking note of T_{Sep} defined to enforce the necessary switching separation, the operating space of the APWM-SSA is shown in Fig. 1-47. Most of the inverter's operating space can be utilized using symmetrical SVPWM combined with the three and four-active vector methods produced by the switching sequences in Fig. 1-43. The only unavailable region is at the voltage limits, where the degree-of-freedom to introduce asymmetries within the PWM period goes to zero. However, this region also coincides with the minimum-pulsewidth limit region often imposed in commercial drives to avoid device damage.

Legend:

Symmetric PWM
3 Active Vectors
4 Active Vectors
Unavailable

Figure 1-47: Areas of a sector of the inverter hexagon (in purple) where V_{qd}^* can be synthesized without simultaneous switching using the addition of new active voltage vectors [14].

This APWM-SSA method was the implemented and evaluated on an induction machine drive under open-loop, volts-per-hertz control to evaluate the impact of this method on output current harmonics at different amounts of enforced switching separation, T_{Sep}. The output current trajectories (Fig 1-48) clearly show the regions where APWM-SSA is active (every 60° of rotation). This produces an increase in current ripple, but the fundamental current component remains unchanged. The added current ripple results in increased harmonic content below the

switching frequency (Fig 1-49). These effects increase as the required switching separation increases.

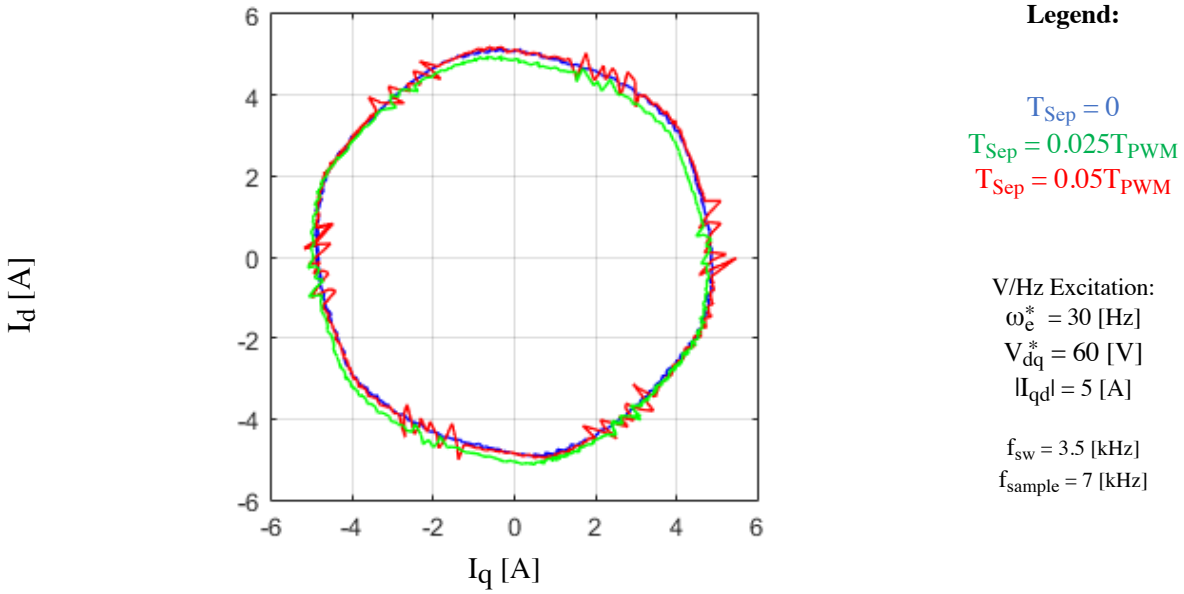


Figure 1-48: Test machine stator current trajectory for different amounts of enforced switching time separation using the three-active-vector PWM method [14].

While the work in [14] presented a working method for performing SSA without impacting the average inverter output voltage each switching period, implementation of APWM-SSA was not performed with closed-loop current control. This is identified as a research opportunity for this preliminary document.

In addition, the APWM-SSA has some limitations which beg for further development of other intra-inverter SSA methods. First, APWM-SSA is fundamentally incompatible with conventional double-update control methods, because the approach requires the control update rate to remain equal to the PWM frequency. Moreover, once asymmetries are introduced into the three-phase PWM waveform, the introduction of zero-sequence voltages will impact the relationship between switching instants within an inverter. Adding zero-sequence voltages after asymmetries have been introduced can cause intra-inverter SSA to occur, if care is not taken. This leads to additional complexity when trying to implement inter-inverter SSA

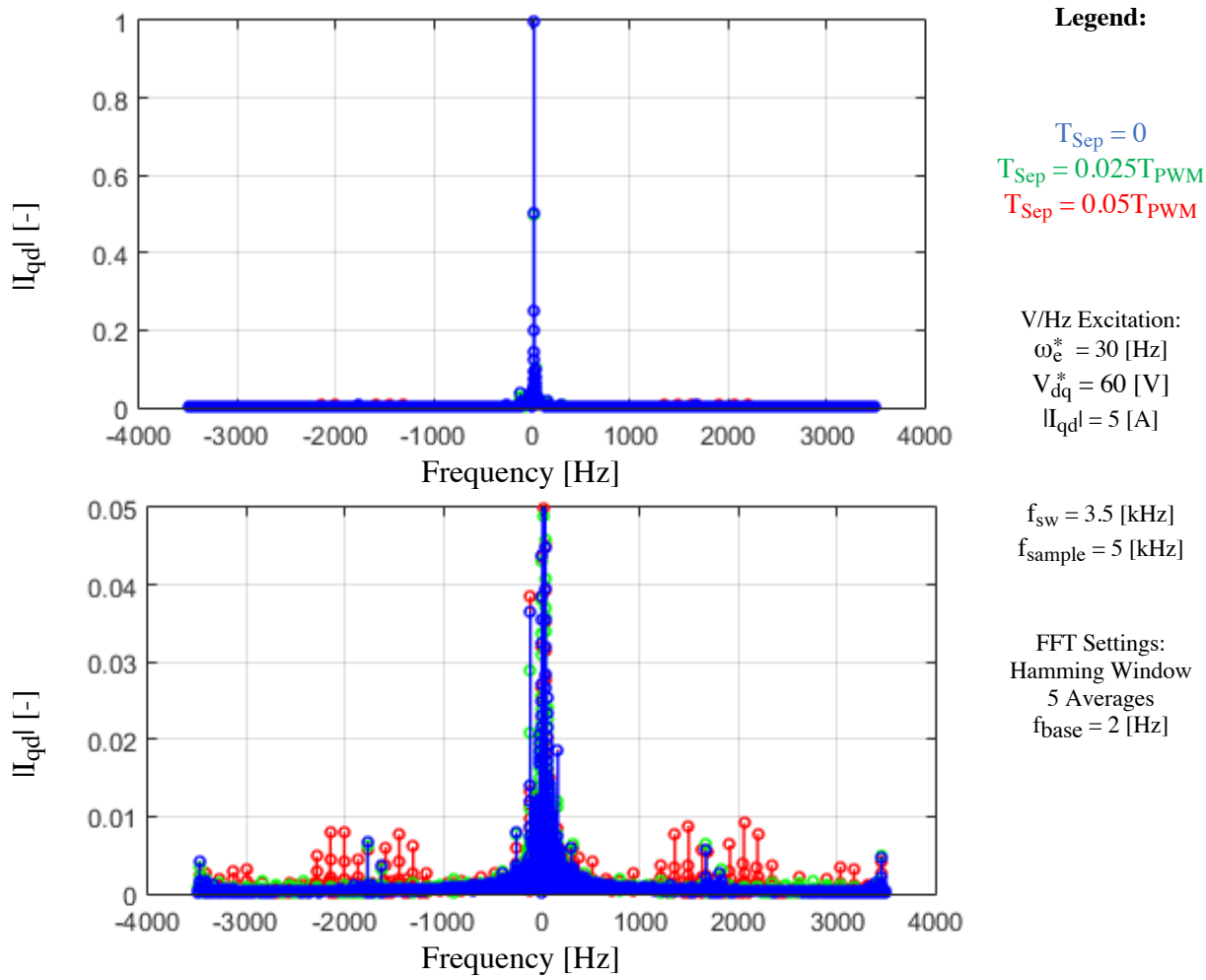


Figure 1-49: Harmonic content of I_{qd} for different amounts of enforced switching time separation using the three-active-vector PWM method, normalized by the fundamental magnitude [14].

Look at inter-inverter simultaneous switching avoidance more closely, it is possible to use PWM asymmetries as a degree-of-freedom to carry it out. However, forming an algorithm in a way that doesn't introduce new simultaneous switching events, intra or inter-inverter, becomes a difficult task, because the avoidance algorithms must monitor and manipulate the rising and falling edges of the PWM waveforms simultaneously. This is illustrated in Fig 1-50 and Fig-52.

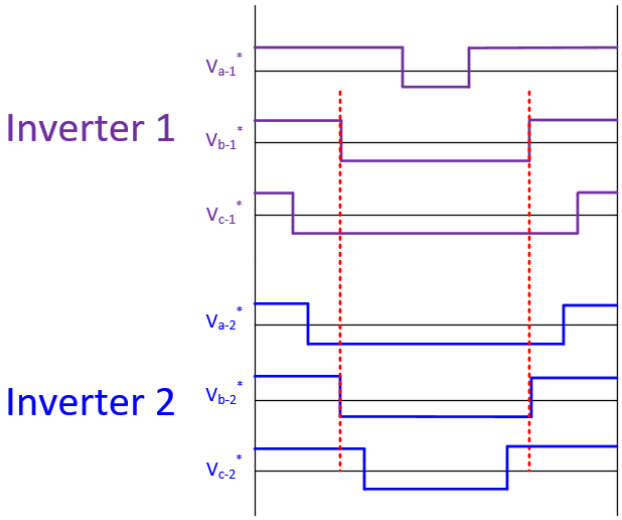


Figure 1-50: Example of two sets of three-phase PWM waveforms where the switching instances in phase B-1 and B-2 overlap [14].

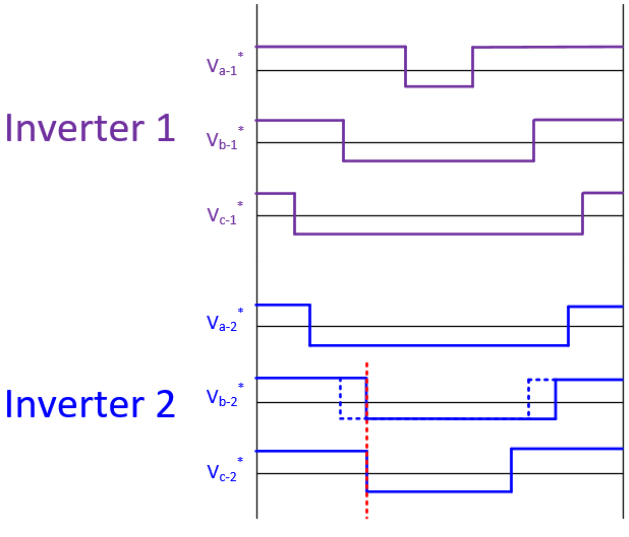


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Figure 1-51: Example of two sets of three-phase PWM waveforms after introducing asymmetry to phase B-2. Here an a new overlap condition is created between phase B2 and C-2 [14].

However, if asymmetric PWM methods are abandoned for the intra-inverter SSA problem and PWM symmetries are maintained, then zero-sequence voltage injection becomes a potentially more workable solution [14]. To perform inter-inverter SSA using this degree-of-freedom, All possible combinations of overlapping phase voltages must be checked, as demonstrated by (1.2-2)-(1.2-9) for the two-inverter case. If any of these inequalities are true, a relative zero-sequence

voltage can be injected to shift the two inverters' zero-sequence command relative to one another (1.2-10). Here, an appropriate $\Delta V_{z\text{-}rel}^{*}$ must be selected so that all phase voltage inequalities become false (example for (1.2-2) shown in (1.2-11)).

$$|V_{a\text{-}1}^{*} - V_{a\text{-}2}^{*}| < V_{Sep} \quad (1.2\text{-}2)$$

$$|V_{a\text{-}1}^{*} - V_{b\text{-}2}^{*}| < V_{Sep} \quad (1.2\text{-}3)$$

$$|V_{a\text{-}1}^{*} - V_{c\text{-}2}^{*}| < V_{Sep} \quad (1.2\text{-}4)$$

$$|V_{b\text{-}1}^{*} - V_{a\text{-}2}^{*}| < V_{Sep} \quad (1.2\text{-}5)$$

$$|V_{b\text{-}1}^{*} - V_{b\text{-}2}^{*}| < V_{Sep} \quad (1.2\text{-}6)$$

$$|V_{b\text{-}1}^{*} - V_{c\text{-}2}^{*}| < V_{Sep} \quad (1.1\text{-}6)$$

$$|V_{c\text{-}1}^{*} - V_{a\text{-}2}^{*}| < V_{Sep} \quad (1.1\text{-}7)$$

$$|V_{c\text{-}1}^{*} - V_{b\text{-}2}^{*}| < V_{Sep} \quad (1.1\text{-}8)$$

$$|V_{c\text{-}1}^{*} - V_{c\text{-}2}^{*}| < V_{Sep} \quad (1.1\text{-}9)$$

$$\Delta V_{z\text{-}rel}^{*} = \Delta V_{z\text{-}1}^{*} - \Delta V_{z\text{-}2}^{*} \quad (1.2\text{-}10)$$

$$|V_{a\text{-}1}^{*} - V_{a\text{-}2}^{*} + \Delta V_{z\text{-}rel}^{*}| > V_{Sep} \quad (1.2\text{-}11)$$

As shown, addressing inter-inverter simultaneous switching through zero-sequence voltage injection on symmetric PWM waveforms is the simplest approach to take. If asymmetries are used to perform intra-inverter SSA, than the equations listed in (1.2-2)-(1.2-9) would need to double to account for the first and second halves of the PWM period. If asymmetries are used for both intra and inter-inverter SSA, there are a total of six degrees-of-freedom that must be manipulated (degree of asymmetry introduced to each phase's PWM waveform).

To simplify the implementation of inter-inverter SSA methods, a technique to implement intra-inverter SSA without the need for PWM asymmetries should be developed. This means that the voltage command of the inverter must necessarily be altered so that regions of simultaneous switching on the voltage hexagon must not be used. With these approaches in hand, zero-sequence-voltage-based inter-inverter SSA can be developed based on the concept of $\Delta V_{z\text{-}rel}^{*}$ injection.

1.3 Existing Motor Control Techniques

Closed-loop control of electro-mechanical power conversion in an AC motor drive requires some form of torque and flux control. Regardless of the outer control loop objectives-be it motion control, DC link voltage control, or torque control-there must be a torque modulator in place regulate the drive's torque production. There are many different methods that have been developed in the literature for forming these torque modulators for AC motor drives. This section will present three common forms of torque modulator that have been studied in the literature and examine the opportunities they present for forming simultaneous switching avoidance algorithms.

1.3.1 Current Regulators and Field Orientation Control

Current-regulated FOC is a widely used method of forming torque modulators in AC motor drives. These can be structured in two different ways: Indirect Field Oriented Control (IFOC) and Direct Field Oriented Control (DFOC) (Fig 1-50) [37].

Comparing these two FOC techniques, both are formed using commands for electromagnetic torque (T_{em}^*) and d-axis rotor flux,(λ_{dr}^*) as inputs. Using these torque and flux references, commands for stator current, i_{qs}^* and i_{ds}^*, are calculated and then passed to a current regulator for closed-loop control. In the case of IFOC, there is no direct measurement of flux inside the machine. Instead the only sensors available for closed-loop control are current and position. Thus, estimates of machine parameters are used together with T_{em}^* and λ_{dr}^* to calculate i_{qs}^* and i_{ds}^* as shown in Fig 1-52 [37]. In the case of DFOC, measurements (or potentially observer-based estimates) are made of the machine's rotor flux using phase current measurements. Thus, a control loop can be closed for rotor flux using i_{ds}^* as the manipulated input. In addition, an estimate of T_{em} is made. Using this signal, a second control loop can be closed on T_{em} using i_{qs}^* as the manipulated input [37]. Finally, the measured rotor flux is used to determine the position of the synchronous frame for current regulation. In these ways IFOC and DFOC use T_{em}^* and λ_{dr}^* to calculate i_{qs}^*, i_{ds}^*, and θ_{rf}^* which are then used as inputs to the current regulator.

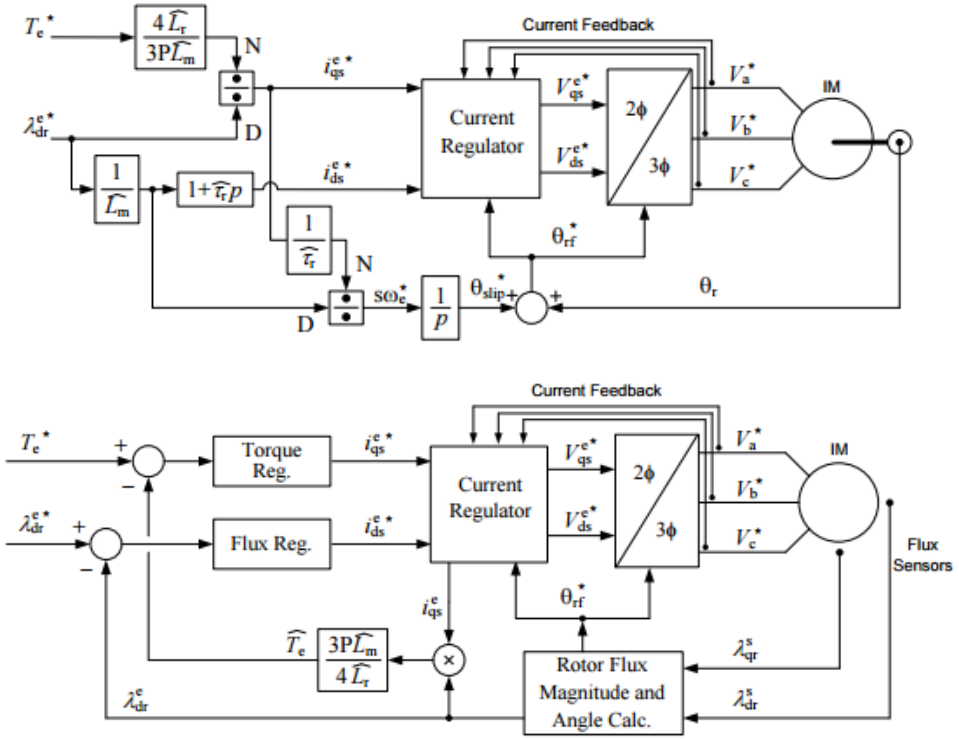


Figure 1-52: State block diagrams of the traditional IFOC (top) and DFOC (bottom) for induction machines [37].

Much like the design of FOC structures, current regulators can also be implemented in a variety of ways, such as stationary frame or synchronous frame PI and deadbeat regulators [38-40]. The most common form used in FOC are variations on the synchronous frame PI regulator like those shown in Fig 1-53. In the top figure, a classical Synchronous Frame PI Regulator is shown together with a synchronous frame model of the induction machine assuming a perfectly decoupled back-emf. A similar controller, called a Complex Vector PI Regulator, is shown in the lower figure. These block diagrams show that the commanded voltage vector output by the current regulator is determined by the current and previous values of error between commanded and measured current as well as the tuned controller gains, K_p and K_i. Thus, there is no control handle to directly manipulate V^*_{qds} independent of i^*_{qs} and i^*_{ds}.

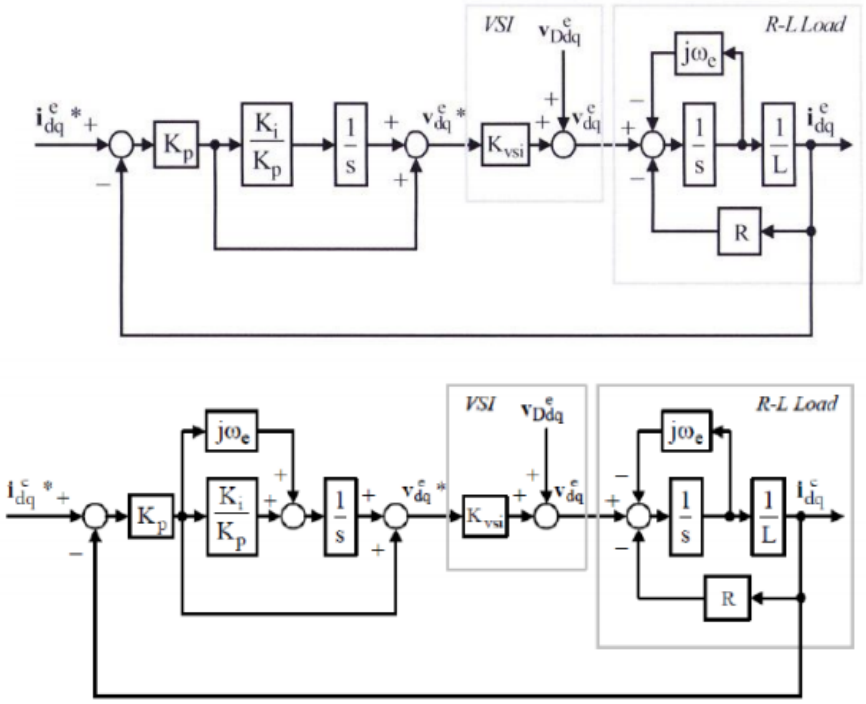


Figure 1-53: State block diagrams of the traditional synchronous frame PI (top) and the complex vector PI (bottom) current regulators.[38].

As has been shown, the generation of V_{qds}^{*} in current regulated FOC torque modulators is determined by the torque and flux commands together with current and previous measurements of current, flux and/or position. Thus, the commanded voltage vector passed to the inverter's PWM cannot be directly manipulated independent of these control inputs. So, there is no way manipulate switching instances within an inverter by selecting a favorable V_{qds}^{*} without impacting control objectives. That said, assuming torque control is of primary concern for control of the motor's mechanical position or power output, selection of λ_{dr}^{*} does provide an indirect method of influencing the resulting V_{qds}^{*} vector determined by the controller.

Field weakening control in electric drives is a commonly used technique to control the magnitude of V_{qds}^{*} by way of adjusting λ_{dr}^{*}. This can be used to optimize efficiency at different operating torque and speed levels [48, 49]. In addition, this technique is often used in high speed operating conditions to extend the available speed range of a drive system [41]. While this method only impacts $|V_{qds}^{*}|$, it could potentially be used to avoid regions of the inverter voltage hexagon which result in simultaneous switching of inverter phases.

1.3.2 Direct Torque Control

Direct Torque Control (DTC) is another form of closed-loop control for AC machines and was first presented in [42]. Rather than forming the controller around regulation of the machine's stator current vector, these control techniques are designed by directly controlling electromagnetic torque together with a rotor flux magnitude command. The first implementation of DTC was formed using hysteresis control methods without the need for PWM methods to control inverter switches [42, 43]. Later DTC was reformed using PI control loops to regulate torque and flux through a voltage command vector which is then applied to the controlled machine through PWM [44].

Beginning with the first implementation presented in [42], DTC was formed using hysteresis band controllers which work to keep T_{em} and $|\lambda_{qds}|$ within specified error bounds of T_{em}^{*} and $|\lambda_{qds}^{*}|$. This form is shown in Fig 1-54. Here measurements are made of the machine's phase currents which are then used to compute estimates of T_{em} and $|\lambda_{qds}|$. These estimates are then compared to their commanded values. Whenever either quantity exceeds there error limits, a new inverter switching state is selected from a lookup table in order to keep T_{em} and $|\lambda_{qds}|$ within the desired limits. Thus, no PWM techniques are required since the inverter's switching states are controlled directly though the controller's hysteresis bands. This control approach leads to machine stator flux trajectories like the one shown in Fig 1-54. One downside of this method is the variable switching frequency which results from this hysteresis control. As can be seen in Fig 1-55, switching frequency will increase and decrease as the stator flux vector rotates around the complex plane [48].

With respect to simultaneous switching avoidance, this control approach allows the timing of switching events to be directly manipulated by adjusting the set error bounds. This enables the separation of switching instances between two inverters (inter-inverter simultaneous switching). In addition, switching states could be selected so that only one inverter phase switches at any given inverter state transition. This would avoid simultaneous switching between phases of a single

inverter (intra-inverter simultaneous switching). However, these approaches would have the unavoidable effect of momentarily degrading torque and flux control performance in favor of simultaneous switching avoidance.

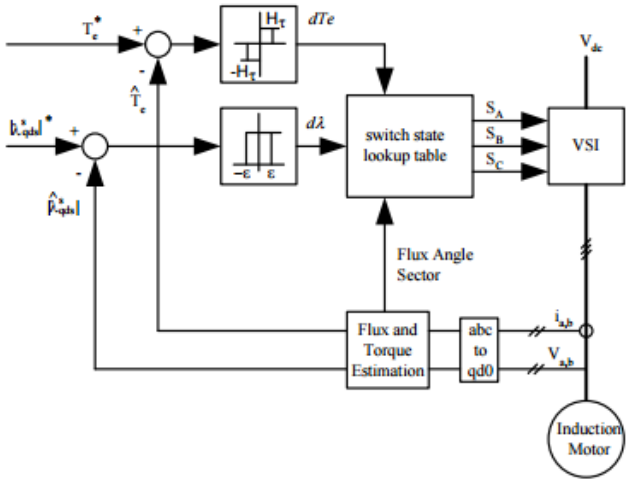


Figure 1-54: System block diagrams of DTC implemented using a hysteresis band controller [42].

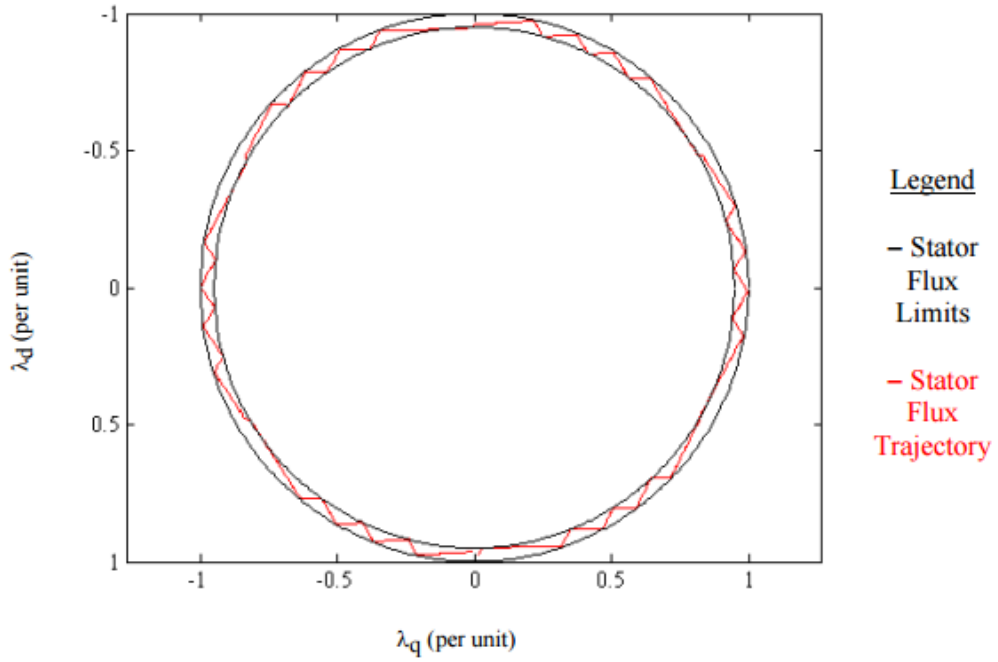


Figure 1-55: DTC implemented using a hysteresis band controller [42].

Moving on to the PI-regulator implementation of DTC, this form has been presented in [44] as a fixed switching frequency alternative to the hysteresis-based DTC. In this form, shown in Fig 1-

56, PI regulators are formed for both T_{em} and $|\lambda_{qds}|$. Like the previous case, current measurements are used to estimate current values of both T_{em} and $|\lambda_{qds}|$. These are then compared to their commanded values to calculate errors that are then fed into their respective PI regulators. These PI regulators then output V_{qs}^{*} and V_{ds}^{*} commands, which are then applied to the inverter using PWM.

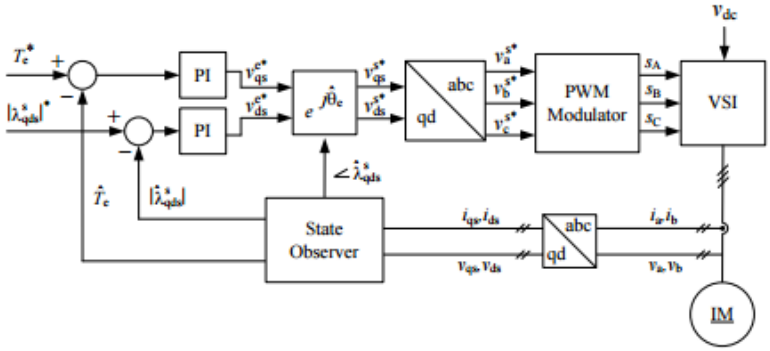


Figure 1-56: System block diagrams of DTC implemented using a PI regulator and PWM [44].

With respect to simultaneous switching avoidance, this control technique has similar properties as the current regulated FOC torque modulators. Because the inverter's voltage vector is determined by command inputs to the PI regulator, the only way to influence the voltage vector command is indirectly through selection of $|\lambda_{qds}^{*}|$.

1.3.3 Deadbeat-Direct Torque and Flux Control

The final torque modulator to be covered in this review is Deadbeat-Direct Torque and Flux Control (DB-DTFC). DB-DTFC was first presented in [45] and is an improvement upon the previously presented DTC control methods. In this torque modulator control of T_{em} and λ_{qds} are decoupled through properly formed discrete-time models of the machine which accurately capture the cross-coupling between the two machine states. Further, as the name states, this control technique can be easily formed as a deadbeat controller, meaning feasible commands for torque and flux values can be achieved at the end of the next switching period [45-49]. Finally, the decoupling of torque and flux control allows for a degree-of-freedom in selecting the stator flux linkage independent of torque each switching period to minimize machine and/or inverter losses [46-48]. To form this deadbeat controller, current, flux, and motion observers are used to estimate

machine states one sampling period ahead. These machine state estimates are then used to solve an inverse machine model which forms the DB-DTFC control law. This implementation and the resulting independent control of torque and flux are shown in Fig 1-57. The equation which defines the available flux linkage commands for a given torque command is shown in (1.3-1) using coefficients defined in (1.3-2)-(1.3-5). In depth derivations of this model can be found in [45-49].

$$Y = MX + B \tag{1.3-1}$$

$$Y = V_{qs}^{*}(k)t_s \tag{1.3-2}$$

$$X = V_{ds}^{*}(k)t_s \tag{1.3-3}$$

$$M = \frac{\lambda_{qr}^{*}(k)}{\lambda_{dr}^{*}(k)} \tag{1.3-4}$$

$$B = \frac{4\sigma L_s L_r}{3PL_m\lambda_{dr}(k)}\left(\left(\frac{R_s}{\sigma L_s} + \frac{R_r}{\sigma L_r}\right)T_e(k)t_s + \Delta T_e(k)\right) + \frac{\lambda_{ds}(k)\lambda_{dr}(k) + \lambda_{qs}(k)\lambda_{qr}(k)}{\lambda_{dr}(k)} \tag{1.3-5}$$

To obtain the form the necessary current and flux observers, two type of observer structures are used, shown in Fig. 1-58. Form the current observer, a Luenberger style structure is used, where $V_{dq}^{*}(k)$ is used together with a synchronous frame current model to create an open-loop observer model. To provide a reference for the model to track measured current is then used together with a PI controller structure. Moving to the Gopinath style flux observer, observed current is used as an input to a current-based flux model. This provides accurate low frequency tracking of actual machine flux. This open-loop flux estimate is then used as a reference to close the loop voltage-based flux model, which provides accurate high-frequency estimates of flux. Once again, a PI controller is used to close the loop on this voltage model. So, the tuning of this controller sets the cross-over frequency at which the flux observer estimate transitions between the two models [49].

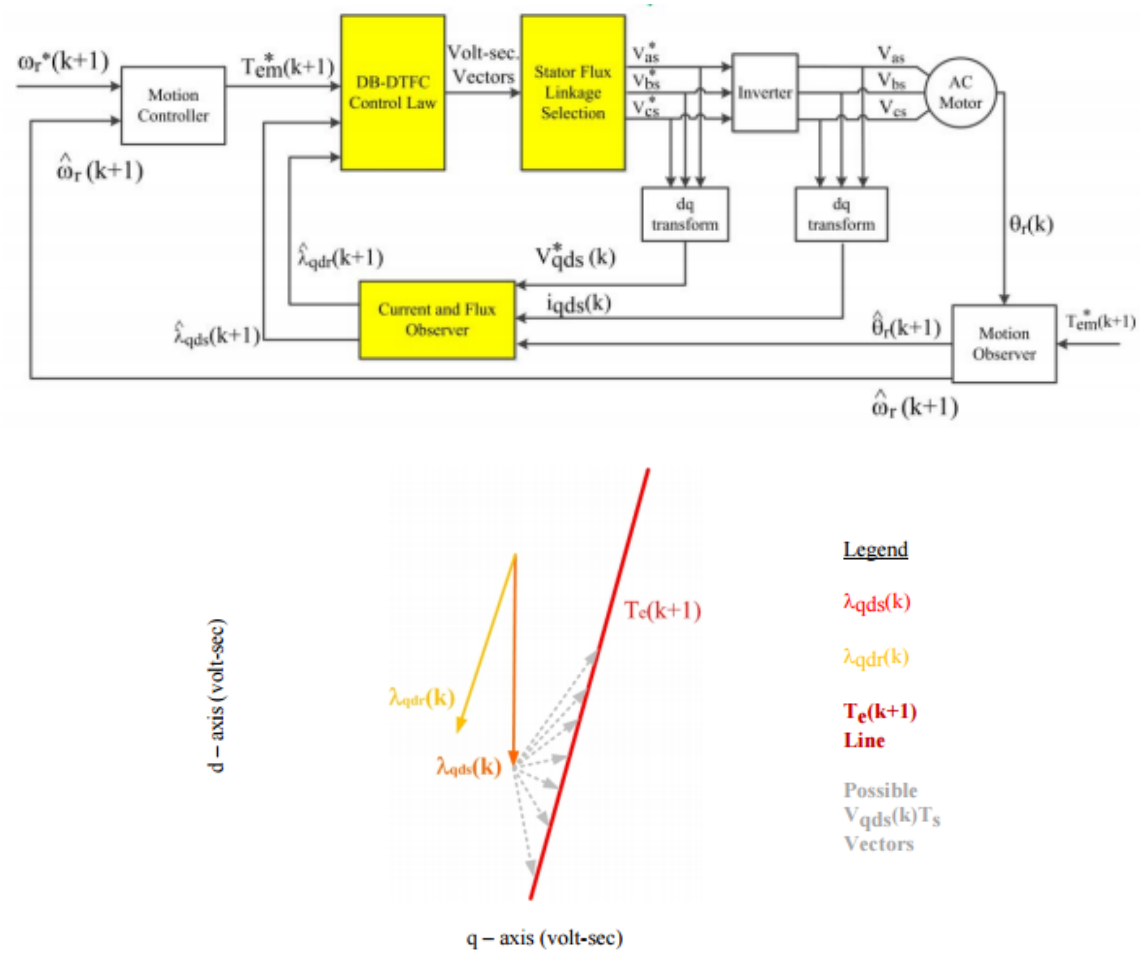


Figure 1-57: Graphical solution for DB-DTFC showing the torque line and the corresponding range of inverter volt-second command vectors [45].

With respect to simultaneous switching, DB-DTFC offers a unique advantage compared to other torque modulators through its ability to directly select the command voltage vector to be applied during the next switching period. Using this available degree-of-freedom in control, volt-sec vector commands can be selected to avoid unfavorable regions of the inverter's volt-sec hexagon. Going further, it would be technically feasible to coordinate this selection of inverter volt-sec command between two or more drives sharing a common DC bus. This could provide another useful degree-of-freedom outside those available in PWM techniques to achieve simultaneous switching avoidance.

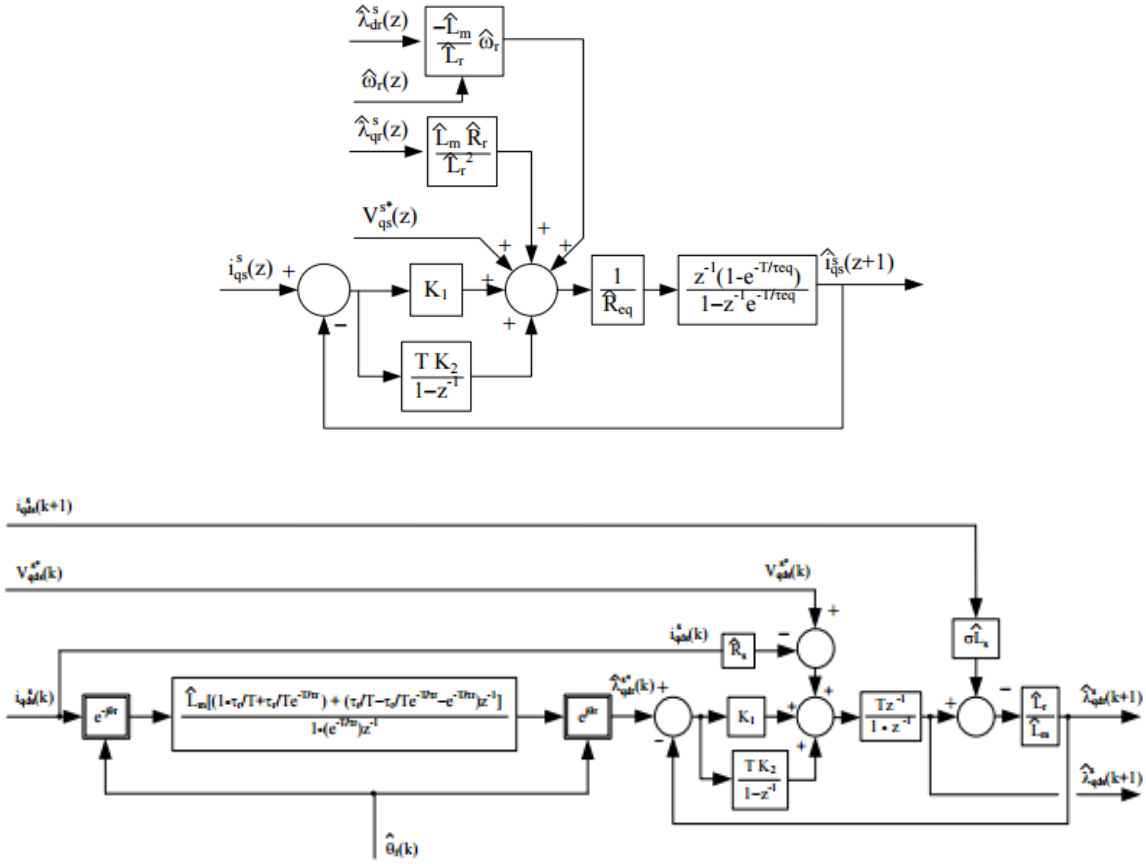


Figure 1-58: Discrete-time implementations of the Luenberger style current observer for the q-axis (top) and Gopinath style flux linkage observer (bottom) [49].

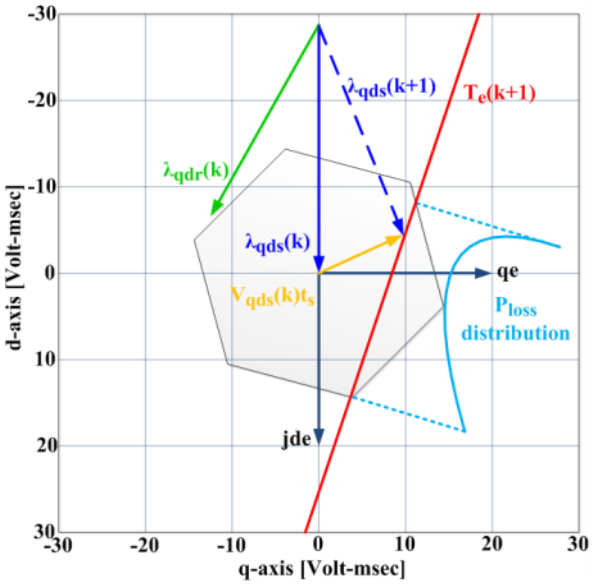


Figure 1-59: Graphical solution for DB-DTFC showing the distribution of loss along the torque line as a function of stator flux.[48].

1.4 Summary of Research Opportunities Identified

The following is a list of conclusions reached based on the review of literature related to simultaneous switching transients, intra-inverter simultaneous switching, and its integration with closed-loop current/torque control for electric machines.

- **Simultaneous Switching Transients in Power Converters**

Evaluation of simultaneous switching events and their related effects is relatively limited in existing literature. Currently published work provides documentation of simultaneous switching in a narrow range of operating conditions. To further understand the impacts of simultaneous switching events, an evaluation of simultaneous switching transients should be performed with detailed measurement of switching transient voltages and currents, as well as with improved resolution in switching transient separation, to paint a clearer picture of simultaneous switching and its impact on DC link di/dt, device voltage stresses, and switching losses.

- **Contextualization of the Severity of Simultaneous Switching Events for different Switching Speeds and parasitic Inductance Distributions**

Both the existing literature and this research work provide example data of simultaneous switching effects for specific test circuits operating under specific conditions. To better understand the implications of simultaneous switching on power converters in general, simple switching transient models should be developed and facilitate a comparison of the implications of switching speed selection on parasitic inductance, voltage margin, and decoupling capacitor requirements across a broad range of converter designs.

- **Error Vector-Based Simultaneous Switching Avoidance**

Previous work in developing SSA algorithms was limited in scope to modifying PWM schemes alone. Using this approach, no modifications to current or torque control loop structures need to

be made, and SSA can be integrated seamlessly into a drive's control. However, in order to perform intra-inverter SSA using PWM methods, a novel asymmetric PWM technique is required. This approach inherently limits control bandwidth by being incompatible with classical double-update control structure. Moreover, the introduction of PWM asymmetries means that zero-sequence voltage injection no longer manipulates switching instances symmetrically about the midpoint of the PWM period and can now cause new intra-inverter switching overlaps if applied incorrectly after intra-inverter SSA is performed. To overcome both of these limitations, methods for performing SSA in the inverter's control loop structure should be developed. SSA can be performed this way by introducing some voltage error and selecting a voltage command vector that does not fall in a region of simultaneous switching. In taking this approach compensation will need to be performed, so that the introduced voltage errors and resulting current errors are handled properly.

- **Compensation of Deadtime Effects for Simultaneous Switching Avoidance**

Deadtime insertion is required for safe operation of voltage source inverters. However, this deadtime results in commutation timing errors driven by load current polarity. Because the developed SSA algorithms assume an ideal inverter model without deadtime, this real uncertainty means that the amount of switching separation enforced by SSA must be large enough to cover this. However, if these commutation timing effects are properly handled, enforced switching separation can be reduced, causing a reduction in inverter output distortion caused by SSA. However, this timing compensation must be performed in such a way so that it cannot cause new switching transient overlaps to occur, thus defeating the purpose of SSA.

- **Intra-Inverter SSA Operation under Closed-Loop Current Control**

Previous work developing the APWM-SSA algorithm was experimentally analyzed using open-loop, voltz-per-hertz operation. However, a goal in developing this method was to eliminate

any impact on closed-loop control performance. So, experiments should be carried out to evaluate the degree to which this has been achieved. Namely, that the current regulator does not see any voltage disturbances and resulting current errors, as a result of SSA manipulations. Moreover, the EV-SSA method proposed in this current work must be evaluated in the same vein. Finally, a comparative analysis of the two SSA approaches must be performed to document the pros and cons of each.

- **SSA Algorithm Development for Converters with an Arbitrary number of Phases**

To date, SSA algorithm development been focused on the specific case of a single three-phase voltage source inverter. In theory, an arbitrary number of converter output phases can be combined on a single DC bus. In practice, a common system topology industrial and traction applications is multiple three-phase converters sharing a common DC bus. To address this, approaches for extending EV-SSA and APWM-SSA to these multi-phase converter systems are proposed and compared with respect to their implementation complexity. This is then compared to the hardware-based active-gate-drive solution as a second avenue for mitigating simultaneous switching effects.

Chapter 2 Simultaneous Switching Transient Waveform Measurement

In this chapter, switching transient waveforms are evaluated to understand how different types of simultaneous switching events impact their characteristics. To do this, a multi-phase inverter circuit is constructed with a large common DC link inductance. In addition, design provisions were included to allow measurement of currents through the DC link, as well as through individual devices. Combining this with appropriate voltage measurements, a clearer picture of simultaneous switching and its impact on DC link di/dt, device voltage stresses, and switching losses at different load current levels and switching separations is obtained.

2.1 Experimental Setup

In this chapter, a multi-phase inverter circuit constructed with discrete IGBTs with anti-parallel diodes and designed to enable measurement of both switching transient voltages and currents. IGBT and diode ratings from the datasheet of the Infineon IKA15N60T devices used are shown in Table 2.1.

Table 2.1. Datasheet parameters for the Infineon IKA15N60T IGBT & anti-parallel diode discrete devices used.

Parameter	**Value**
Max collector-emitter voltage, V_{CE}	600 [V]
Max collector current, I_C (T_C = 100° [C])	10.6 [A]
Max diode forward current, I_F (T_C = 100° [C])	10.8 [A]
Turn-off fall time, t_f (T_C = 100° [C])	80 [ns]
Turn-on rise time, t_r (T_C = 100° [C])	15 [ns]
Diode reverse-recovery time, t_{rr} (T_C = 100° [C])	140 [ns]

A schematic of the inverter and accompaning probing points is shown in Fig. 2-1. To measure the transient voltage waveforms, passive voltage probes (Agilent 10074c) were used. To minimize the introduction of parasitic effects on the circuit, probe clips were removed and a shared piece of

copper foil was soldered to their ground sheaths. This single foil was then soldered to a pad on the power ground plane. This was done to minimize the possibility for parasitic ground loops to influence measurement results. Single strand wire was then used to connect the probe tips to the desired measurement points on the discrete device terminals. This is shown in Fig. 2-1.

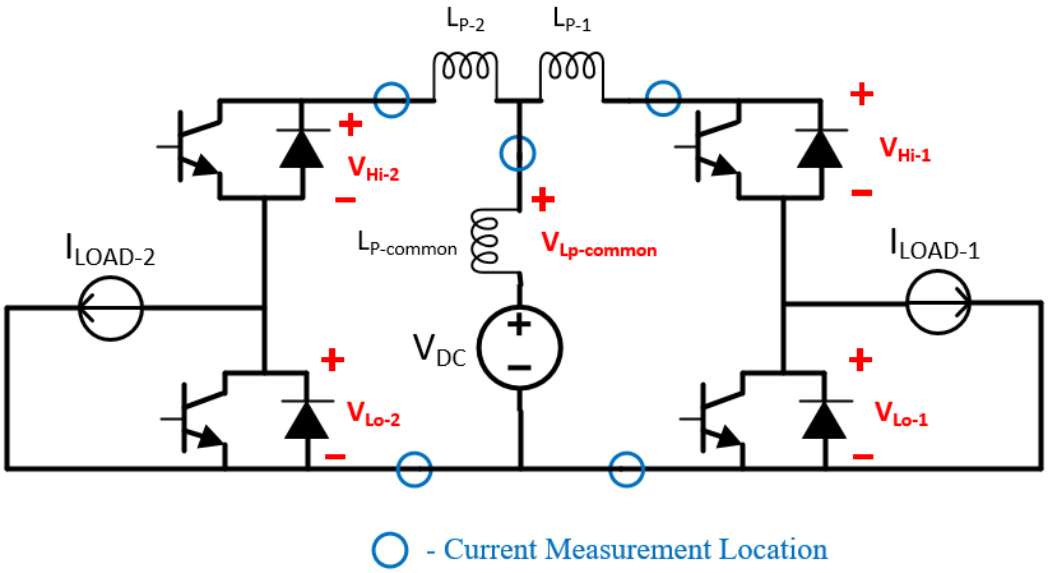


Figure 2-1: Schematic of the two-phase inverter together with voltage and current probe locations.

Figure 2-2: Image of voltage probing setup.

Two different current measurements were performed for these switching transient tests. First, a Lecroy CP031 current probe was used to measure the total current flowing from the DC bus to the inverter phases. This was placed around a copper wire used connect the inverter phases to the DC bus. In addition, PEM MiniHF rogowski coils were used to measure currents flowing in individual devices. These were inserted around jumpers constructed of copper foil and soldered to the surface of the PCB (Fig. 2-3).

Figure 2-3: Image of rogwoski coil probing setup.

For the purpose of understanding voltage stresses during switching transients, impedance measurements were performed using a Keysight E4990A Impedance Analyzer. Figure 2-4 shows impedance measurements taken at four locations: DC link capacitors, the common or shared portion of the commutation loop, and across individual phases. (These locations are identified in Fig. 2-4). Based on these measurements, the common loop inductance, $L_{p\text{-}common}$, was around 90 [nH] while the total inductance seen by each phase, $L_{p\text{-}phase}$, was approximately 180 [nH].

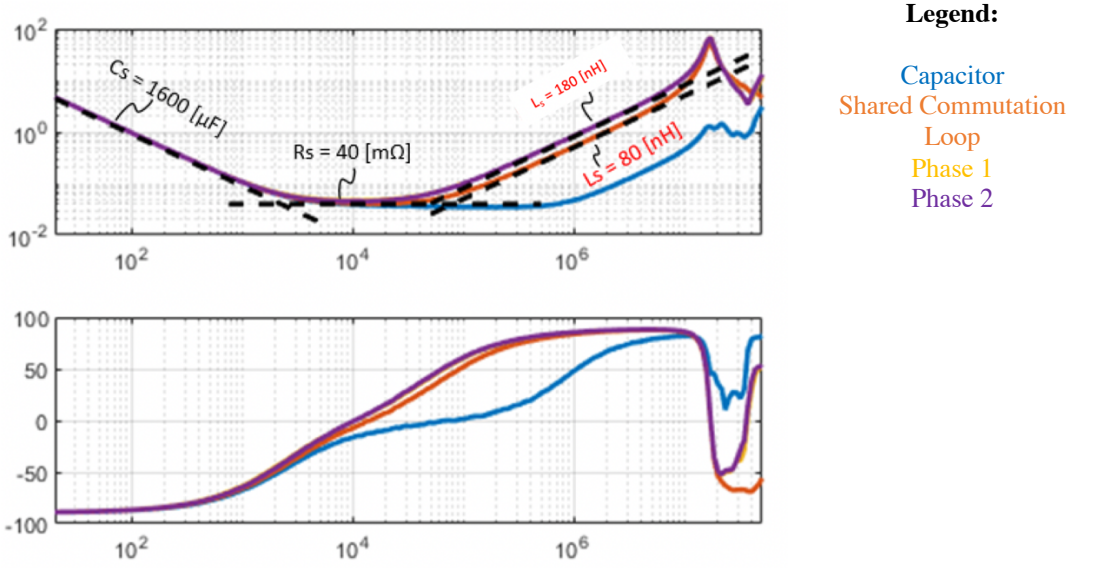


Figure 2-4: Measurement of the DC link impendence experienced by each inverter phase, as well as across the shared commutation path and DC link capacitance.

2.2 Voltage Stresses during Simultaneous Switching

The impacts of simultaneous switching on transient waveforms were evaluated for both the IGBT turn-off and turn-on (or diode turn-off) transients. First, measurements were taken with only one phase operating to provide a baseline of comparison. Then, measurements were repeated with two phases commutating simultaneously.

2.2.1 Simultaneous IGBT Turn-off

Beginning first with a time-domain comparison Fig. 2-5 shows the impact of simultaneous IGBT turn-off on voltage stresses as compared to the single IGBT turn-off case. Examining the voltage waveforms, the simultaneous turn-off results in higher peak voltages at both across the individual devices as well as across the shared commutation loop. This is due to the increased di/dt through $L_{p\text{-}common}$ that can be seen in the calculated di/dt waveform included in Fig. 2-5.

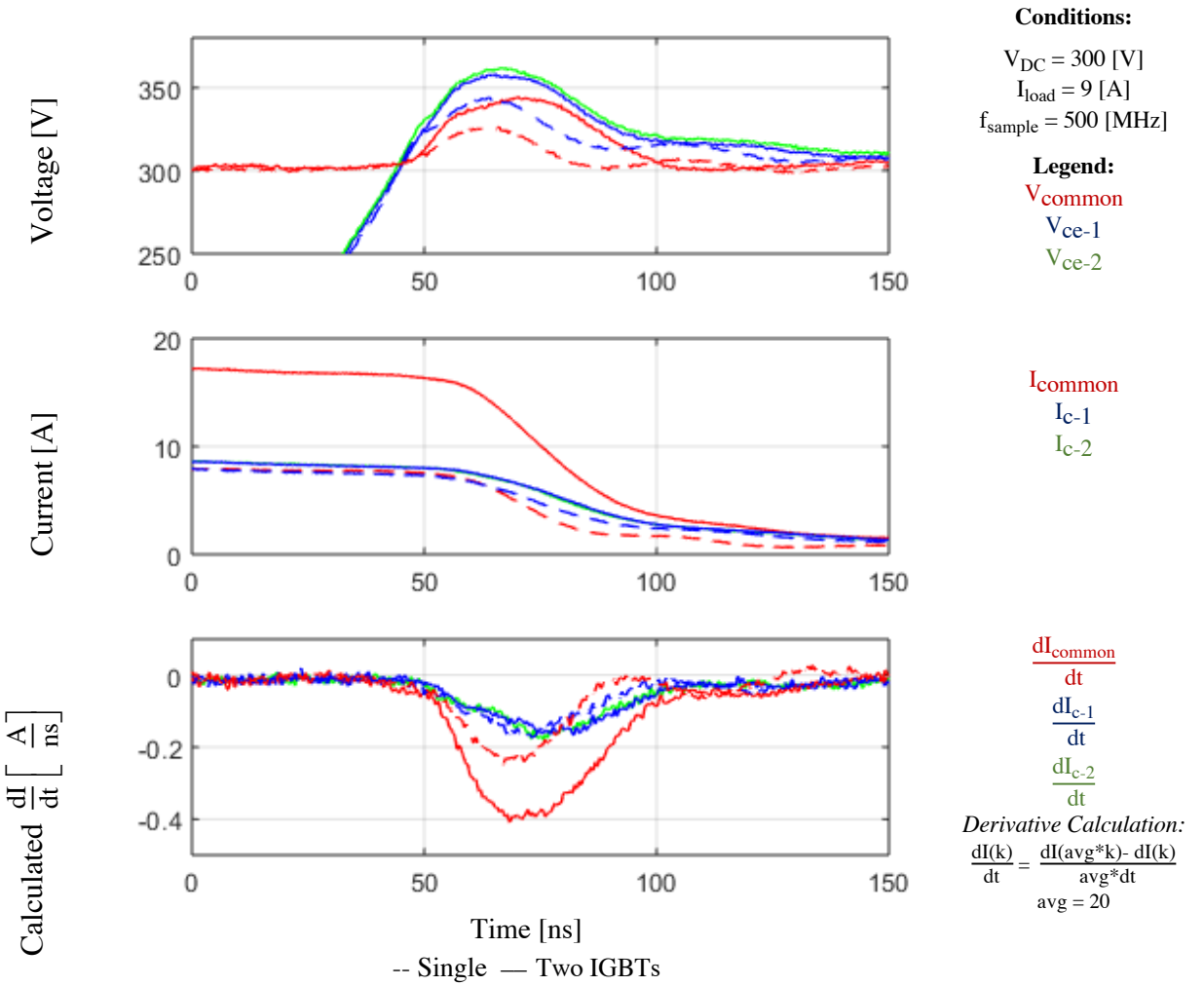


Figure 2-5: Overlaid comparison of time domain waveforms during a single IGBT and simultaneous IGBT transient.

Fig 2-6 shows a summary of peak voltage stresses experienced for both the single IGBT and simultaneous IGBT turn-off transients at different load current levels. For both the single and simultaneous cases, the voltage difference between $V_{common,peak}$ and $V_{ce,peak}$ remains the same, as expected from (1.1-11). However, the overshoot as measured by $V_{common,peak}$ increases by a factor of nearly 2. This is due to the near doubling of di/dt in the common inductance (Fig. 2-6).

$$V_{D\_i1}(t) = V_{CC}(t) - L_{Common}\sum_{j=1}^{n}\frac{dI_{c\_j2}}{dt} - L_{phase\_i}\frac{dI_{c\_j2}}{dt} \qquad (1.1\text{-}11)$$

$$V_D(t) = V_{CC}(t) - \left(nL_{Common} + L_{phase}\right)\frac{dI_c}{dt} \quad (1.1\text{-}13)$$

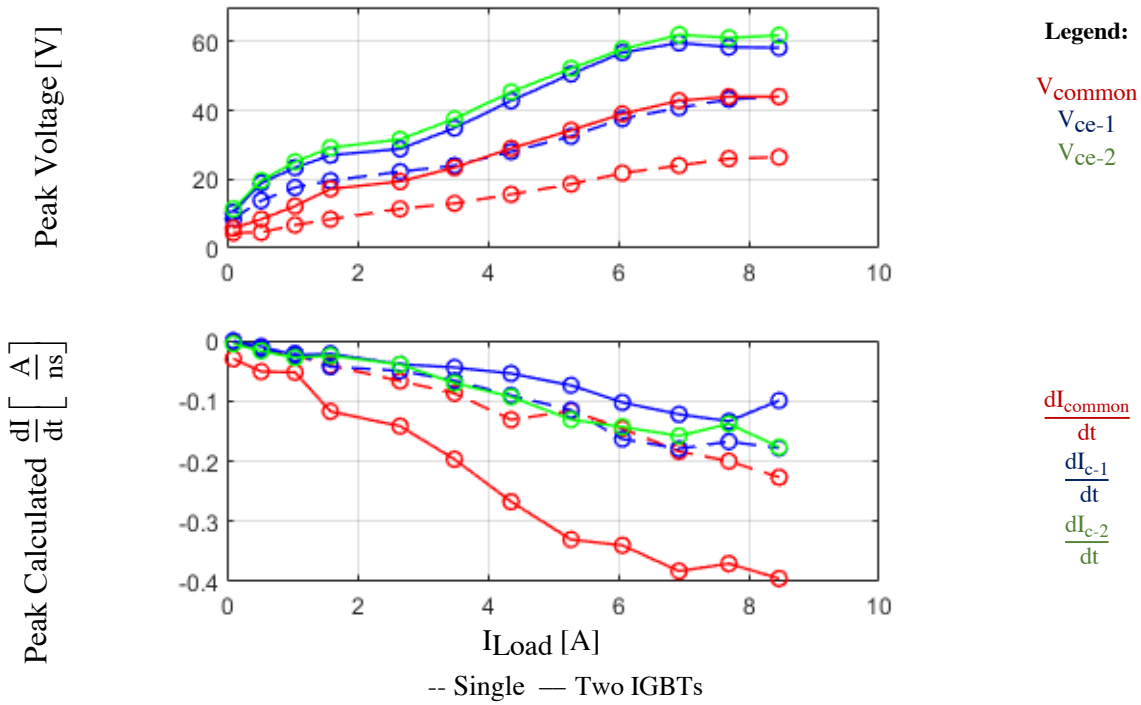


Figure 2-6: Peak voltage and di/dt values for both the single IGBT and simultaneous IGBT turn-off transient.

Finally, Fig. 2-7 shows a comparison of simultaneous switching events occuring between two low-side IGBTs and occuring between two high-side IGBTs. As one would expect, The results are similar because the result in the same trend in voltage stresses.

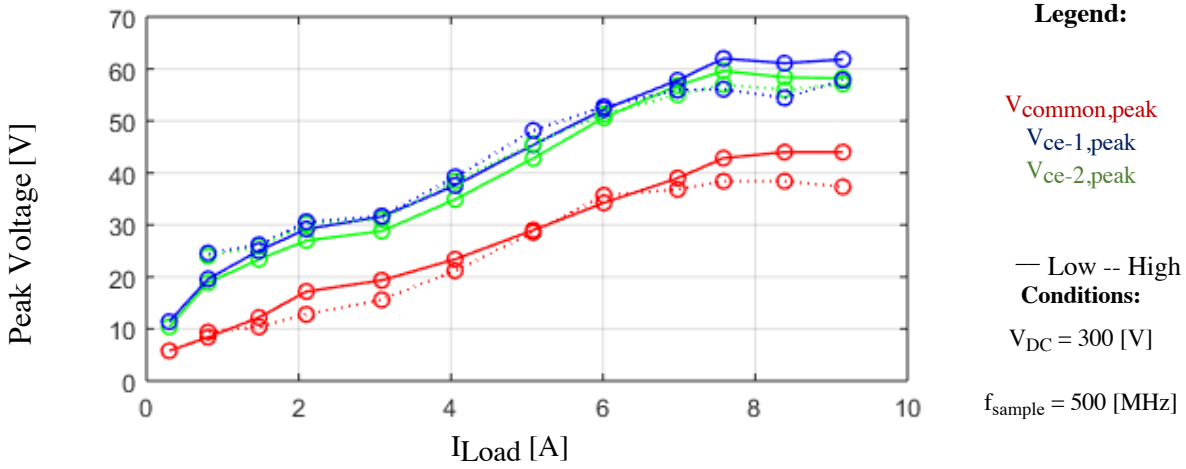


Figure 2-7: Comparison of peak voltages during high-side and low-side simultaneous IGBT turn-off transients.

Fig. 2-8 compares calculated power losses during single phase and simultaneous switching for the 9 [A] load case. Here, simultaneous switching results in a 15% increase in peak power losses during the transient. This effect on peak power losses is summarized as a function of load current in Fig. 2-9. This increased power loss results in an increase in total switching energy losses of up to 20%, as shown in Fig 2-10.

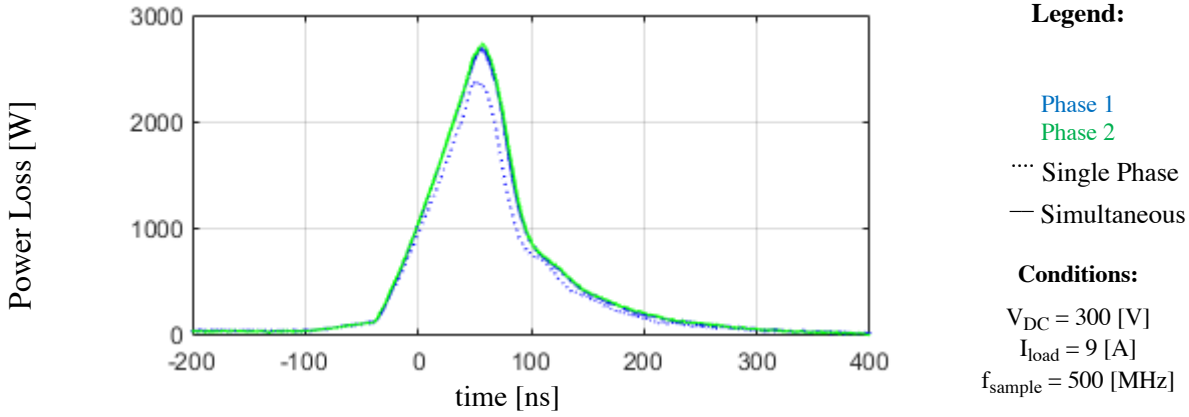


Figure 2-8: Comparison of calculated power losses during single-phase and simultaneous IGBT turn-off transients.

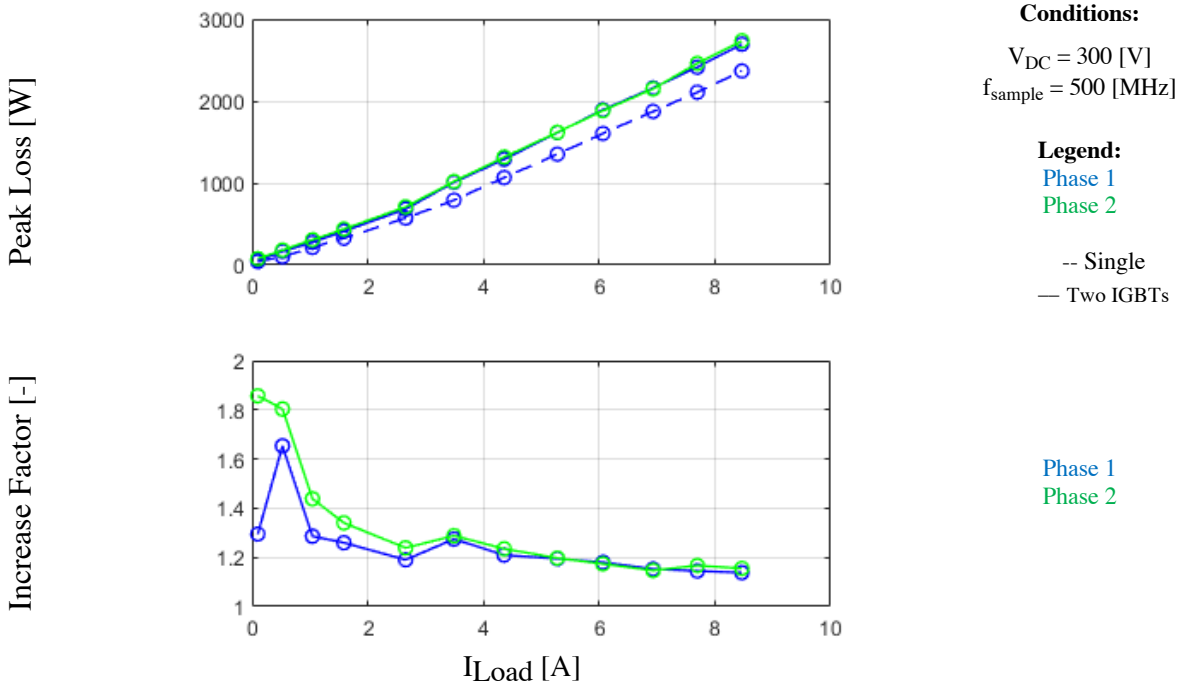


Figure 2-9: Comparison of calculated peak power losses during single-phase and simultaneous IGBT turn-off transients as a function of load current.

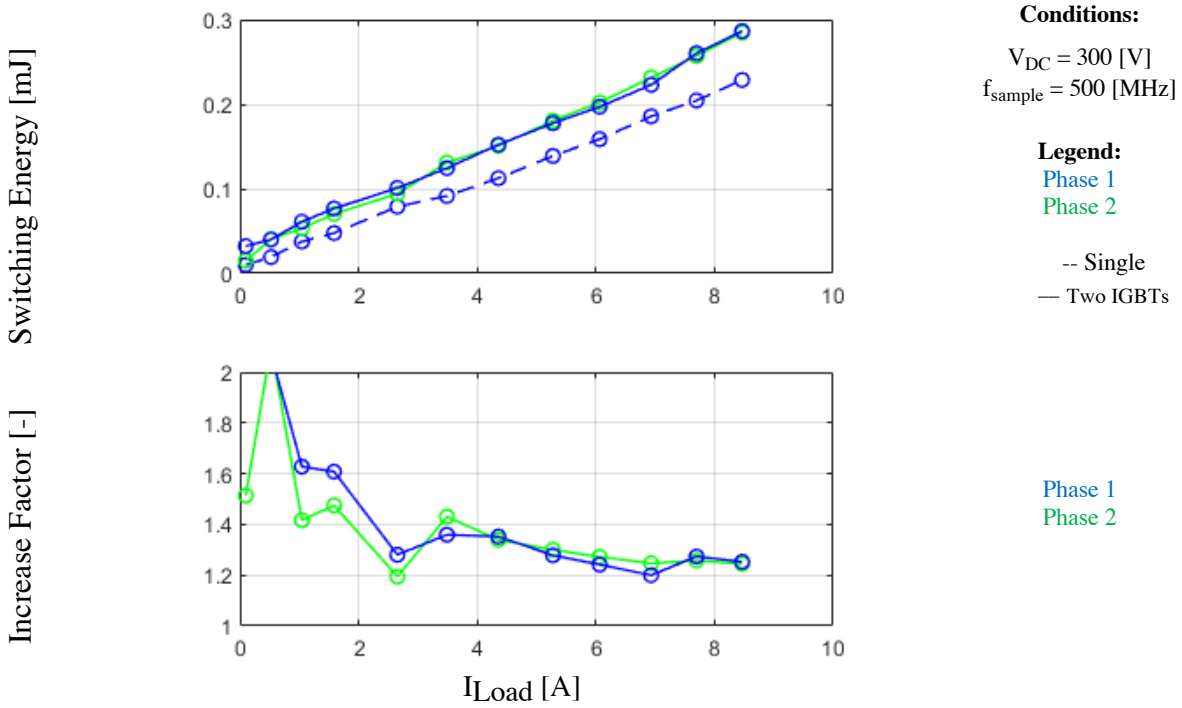


Figure 2-10: Overlaid comparison of time domain waveforms during a single IGBT and simultaneous IGBT transient.

2.2.2 Simultaneous Diode Turn-off

Beginning first with a time-domain comparison Fig. 2-11 shows the impact of simultaneous diode turn-off on voltage stresses as compared to the single IGBT turn-off case. Examining the voltage and current waveforms, the simultaneous turn-off results in slower turn-off combined with a slightly faster extinguishing of the reverse-recovery current. Due to the doubling of the di/dt through the DC link, there is a larger peak-to-peak swing in voltage across the inverter phase. There is a noticeable increase in oscillation after turn-off, however, the di/dt waveforms suggest this is largely due to parasitic capacitive coupling in the DC link structure after the common inductance wire.

Fig 2-12 shows a summary of peak voltage stresses experienced for both the single diode and simultaneous diode turn-off transients at different load current levels. Unlike the IGBT, peak voltage stresses stop increasing with current after 2 or 3 [A]. This result is supported by the corresponding peak calculated di/dt values. The same is true for the minimum voltages and peak di/dt rates during initial turn-off. Once again, comparing high-side and low-side simultaneous diode turn-off transients, the results are very similar. This is shown in Fig 2-13.

Unlike the simultaneous IGBT turn-off, Fig. 2-14 shows there was not a noticeable increase in peak power losses during the simultaneous diode turn-off. This holds true for a range of load current values (Fig. 2-15). Moreover, Fig 2-16 shows that total switching energy loss decreased slightly. These results are likely due to the slightly lower peak reverse-recovery current seen during the simultaneous diode turn-off. This result doesn't quite follow those presented in the state-of-the-art, where simultaneous diode turn-off resulted in increased losses. However, these differences could simply be due to the significant difference in power levels and switching devices being used.

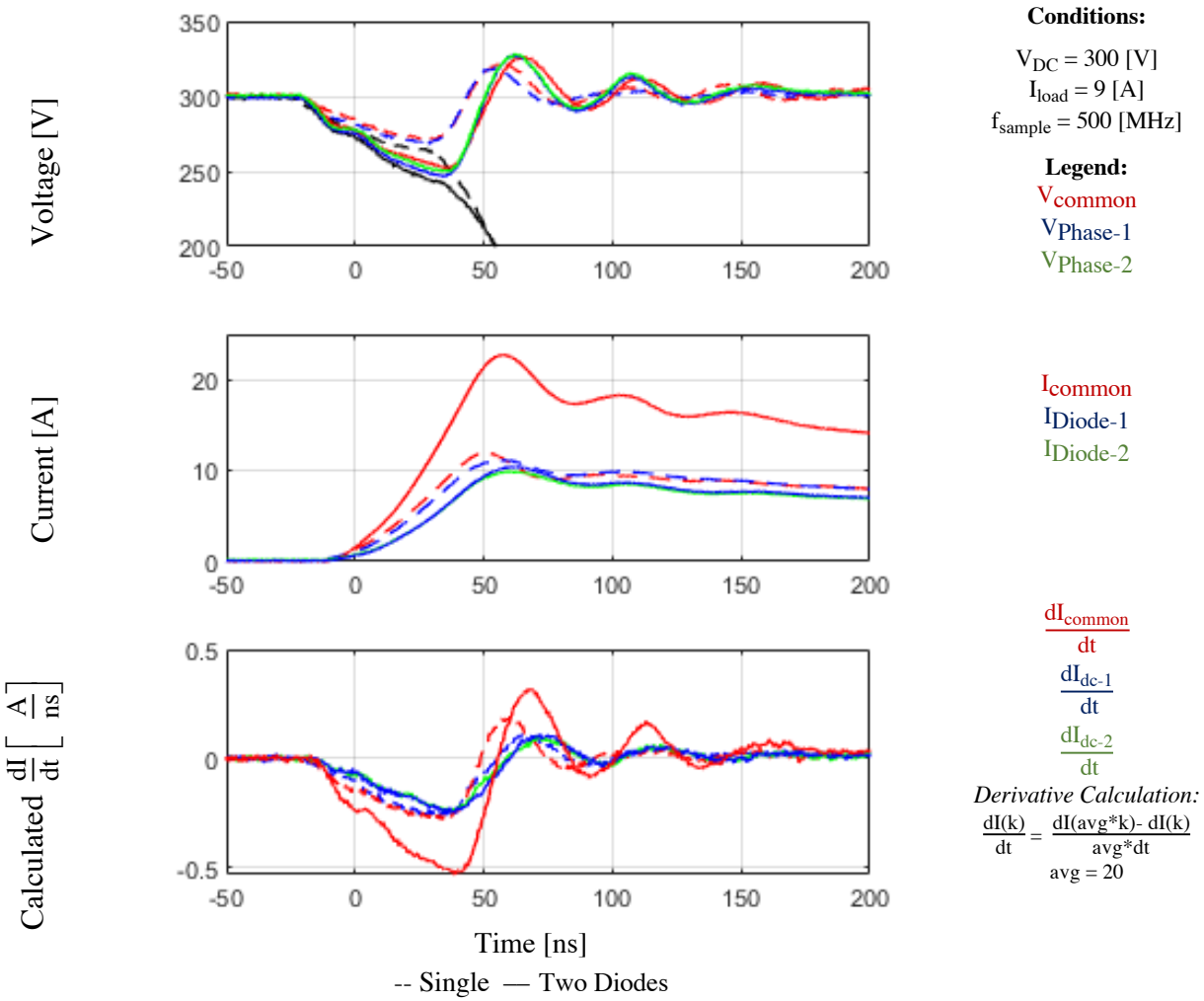


Figure 2-11: Overlaid comparison of time domain waveforms during a single diode and simultaneous diode transient.

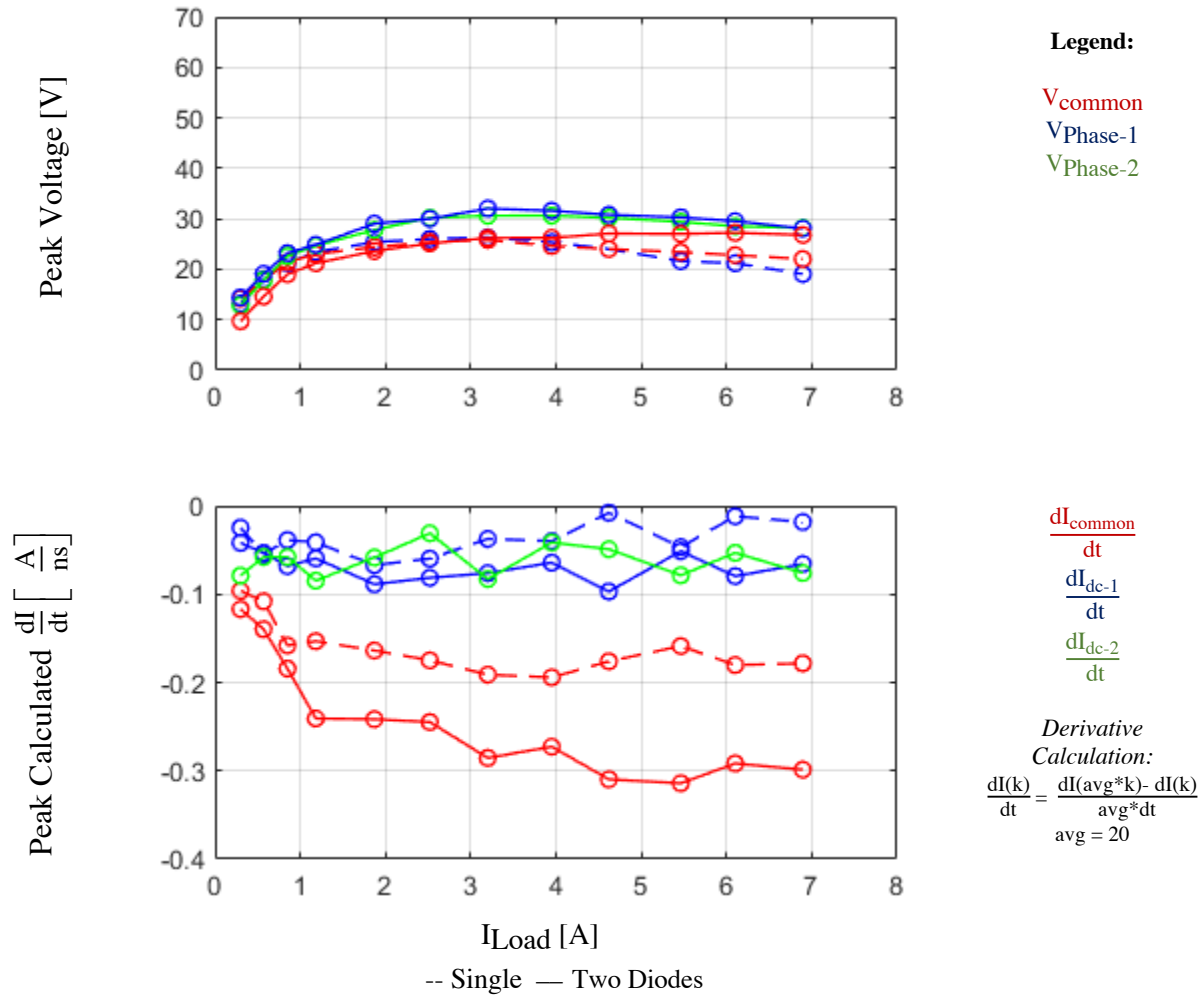


Figure 2-12: Peak voltage and di/dt values for both the single diode and simultaneous diode turn-off transient.

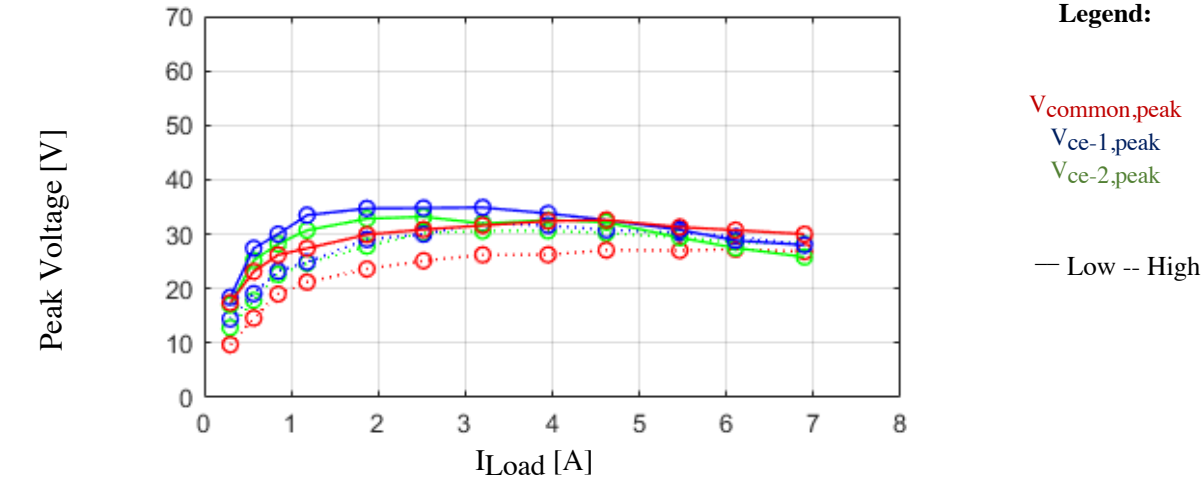


Figure 2-13: Comparison of peak voltages during high-side and low-side simultaneous diode turn-off transients.

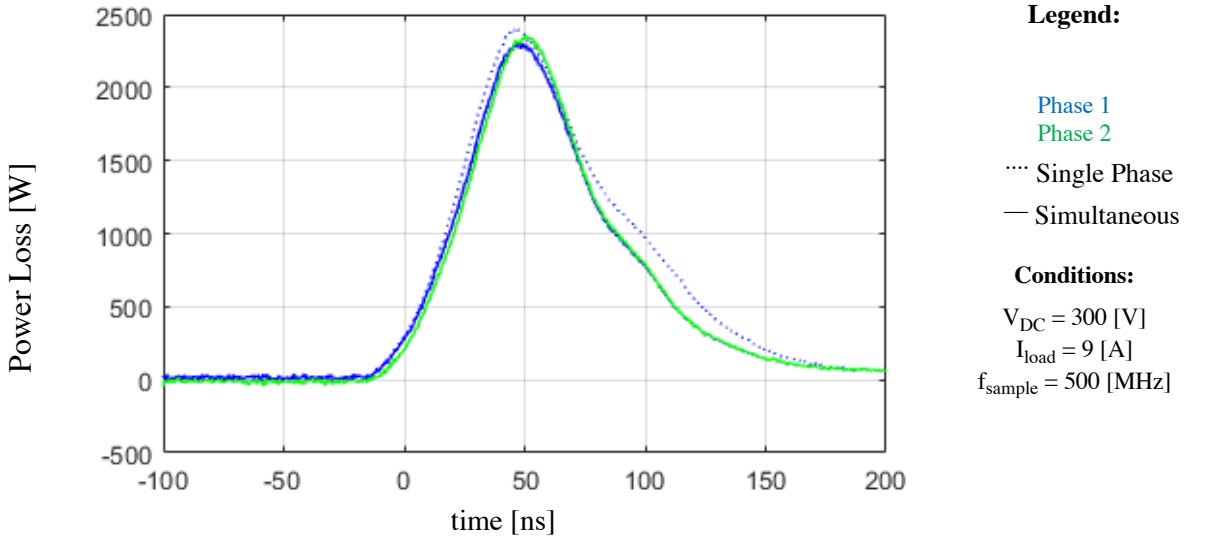


Figure 2-14: Comparison of calculated power losses during single-phase and simultaneous diode turn-off transients.

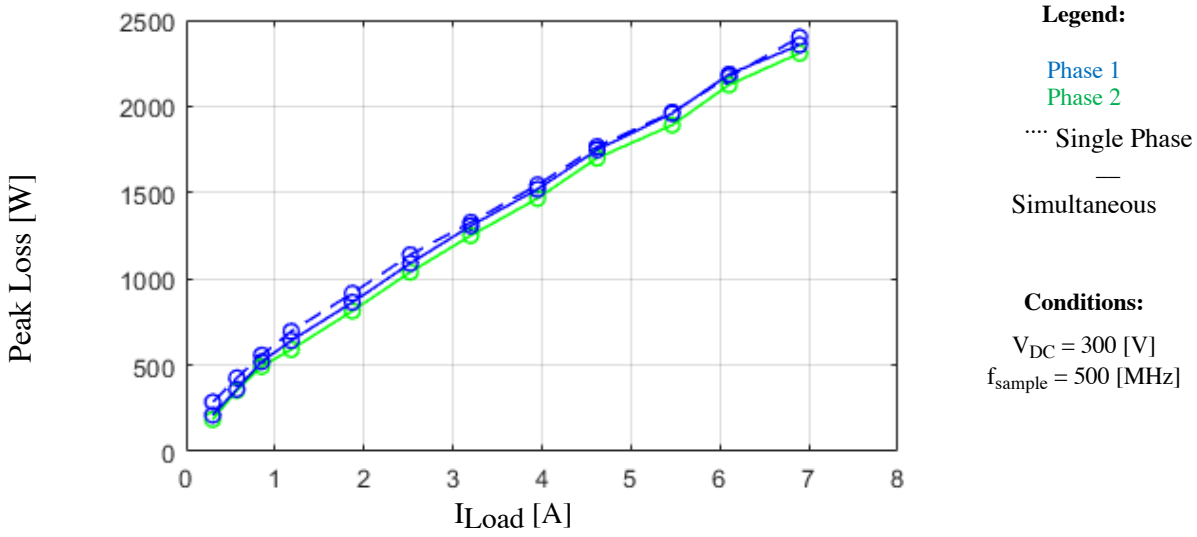


Figure 2-15: Comparison of peak power losses during single-phase and simultaneous diode turn-off transients.

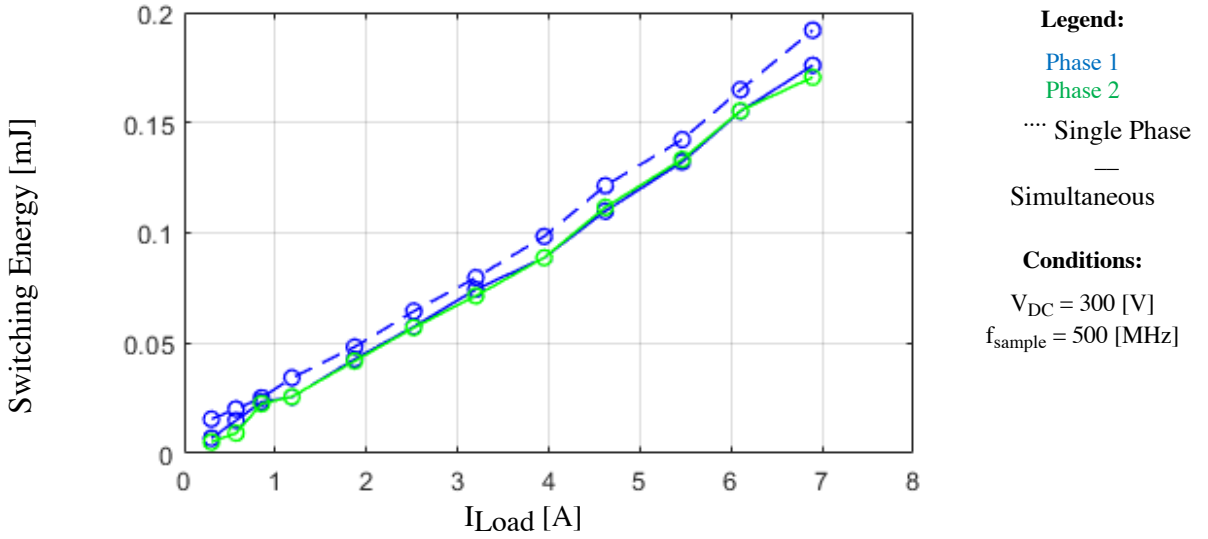


Figure 2-16: Comparison of energy losses during single-phase and simultaneous diode turn-off transients.

2.3 Voltage Stresses During Asynchronous Switching

To further inform the design of simultaneous switching avoidance algorithms, it is useful to understand the relationship between separations in switching events and the resulting transient waveforms. To this end, tests were carried out for both IGBTs and diodes where the switching events occur asynchronously with differing amounts of switching separation, T_{Sep}.

2.3.1 Asynchronous IGBT Turn-off

For the case of two IGBTs turning-off asynchronously, Fig. 2-17 shows a time-domain comparison for the case of simultaneous turn-off and asynchronous turn-off where the switching separation time, T_{Sep}, equals 20 [ns]. This demonstrates how sufficiently separating these transients, so that their regions of peak di/dt no longer overlap, significantly limits any voltage stress coupling between the two phases.

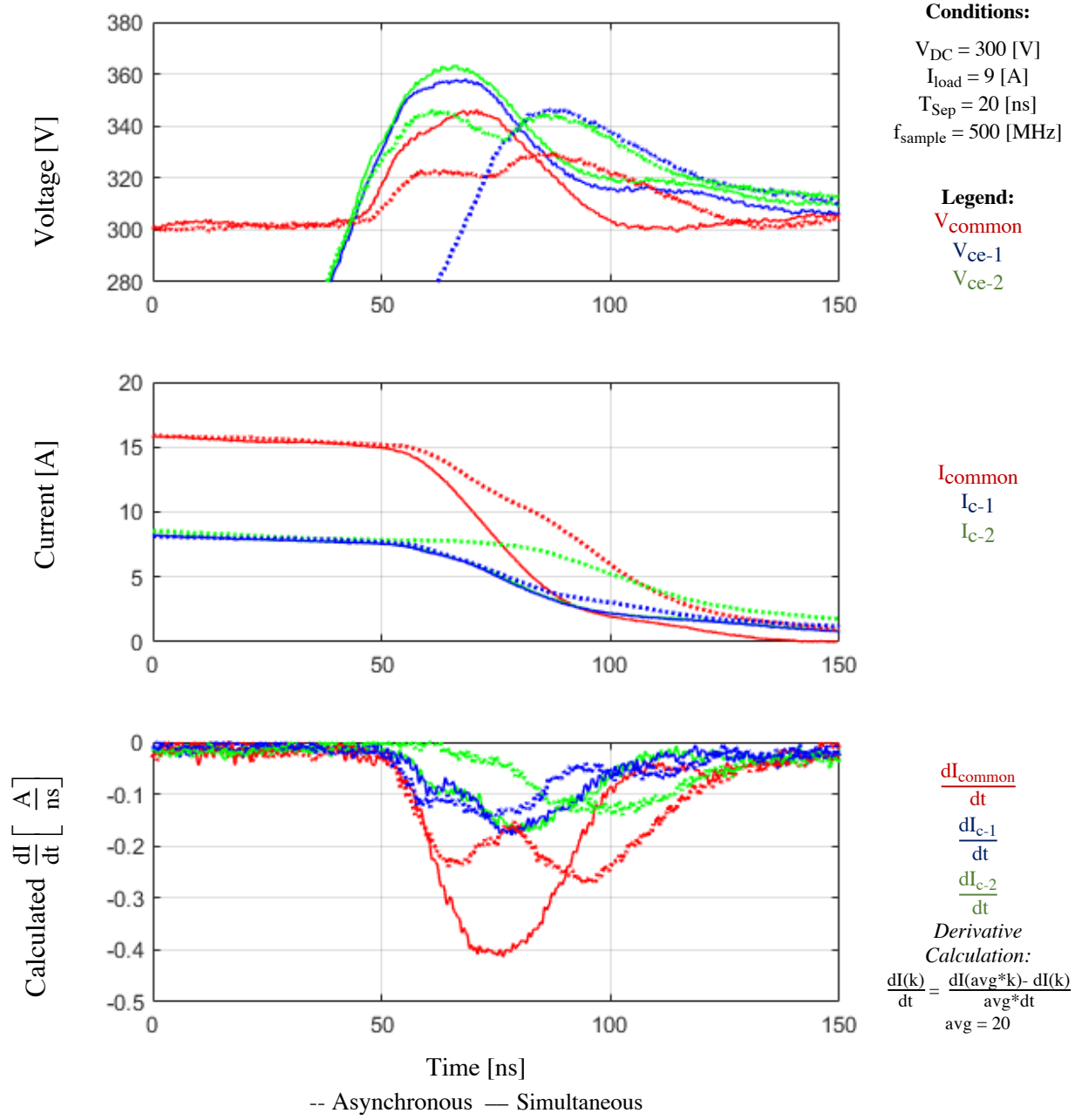


Figure 2-17: Overlaid comparison of time domain waveforms during a simultaneous IGBT and asynchronous IGBT transients.

Fig. 2-18 clearly summarizes the effect of T_{Sep} on voltage stresses during asynchronous IGBT turn-off. This further underscores the limited amount of separation needed to effectively mitigate the voltage stress coupling effect.

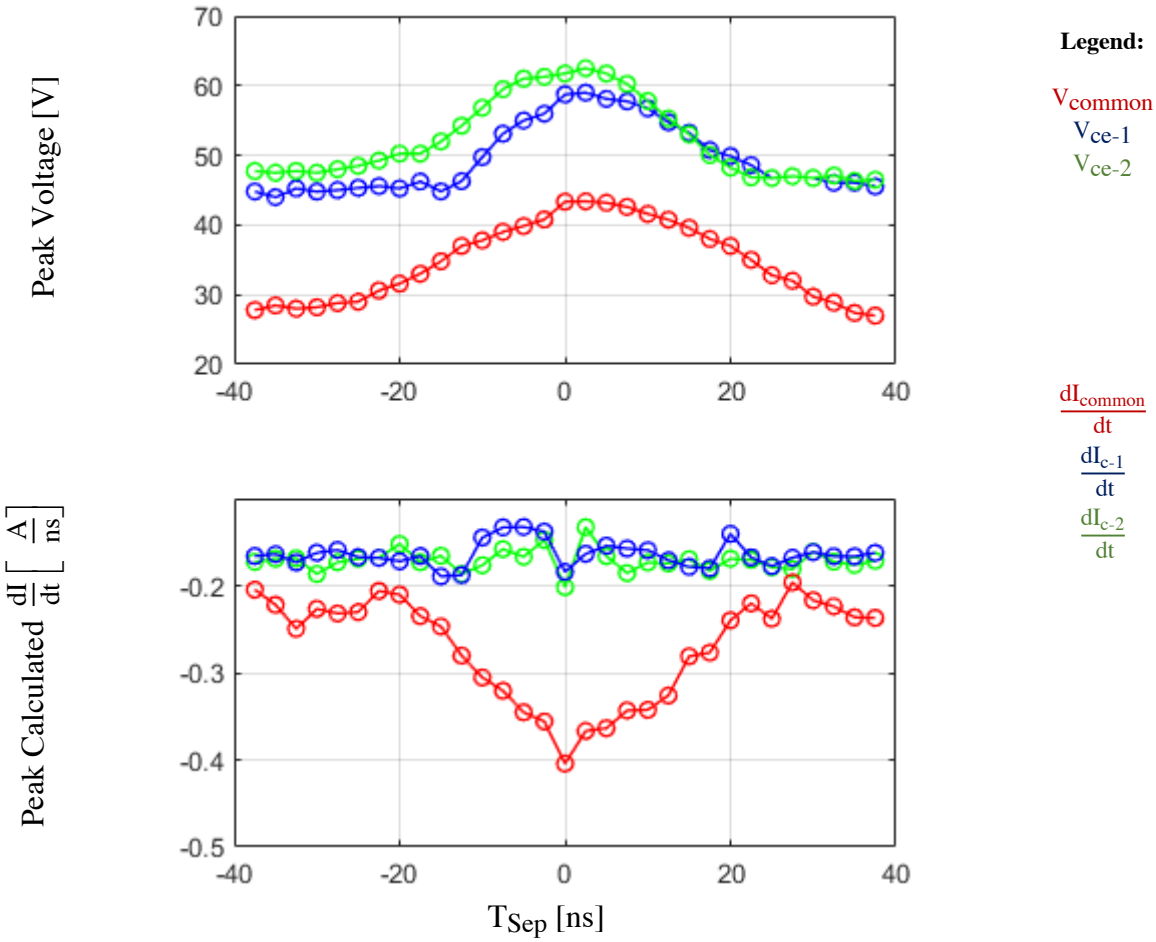


Figure 2-18: Peak voltage and di/dt values for asynchronous IGBT turn-offs with varying separation time.

Fig. 2-19 shows the increases in peak power losses experienced during simultaneous switching are also quickly eliminated as separation is introduced between the switching transients. Once again, this is because the voltage stress coupling diminishes once regions of peak di/dt in each phase are given sufficient temporal separation.

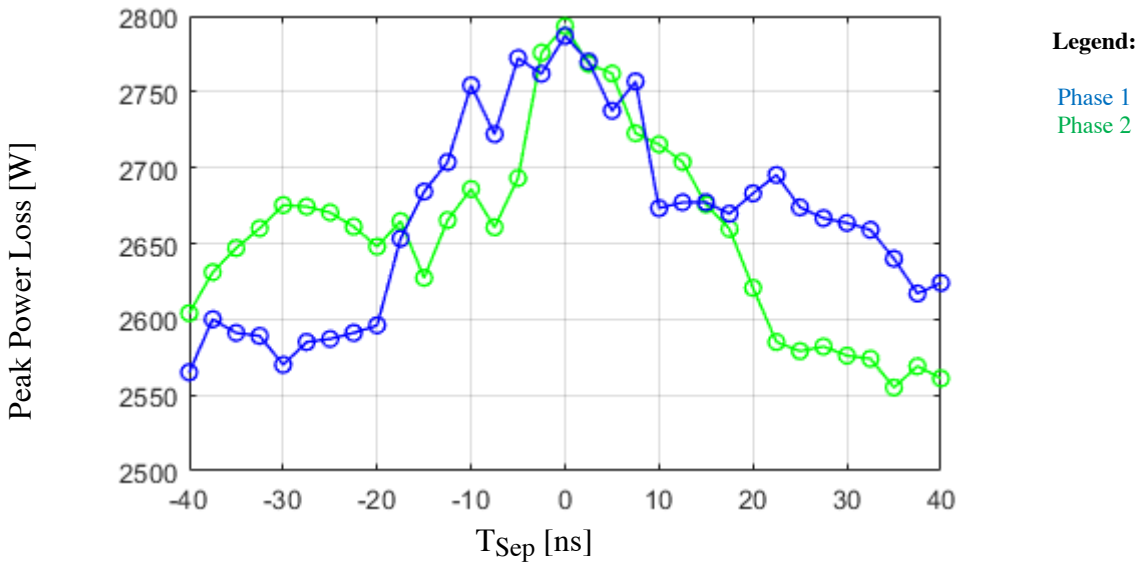


Figure 2-19: Peak calculated power losses for asynchronous IGBT turn-offs with varying separation time.

2.3.2 Asynchronous Diode Turn-off

For the case of two diodes turning-off asynchronously, Fig. 2-20 shows a time-domain comparison for the case of simultaneous turn-off and asynchronous turn-off where the switching separation time, T_{Sep}, equals 30 [ns]. In the latter case, the reverse-recovery currents are no longer overlapping. Instead the delayed diode's initial turn-off di/dt cancels out the reverse-recovery di/dt flowing through the common inductance. This causes a reduction in voltage stresses.

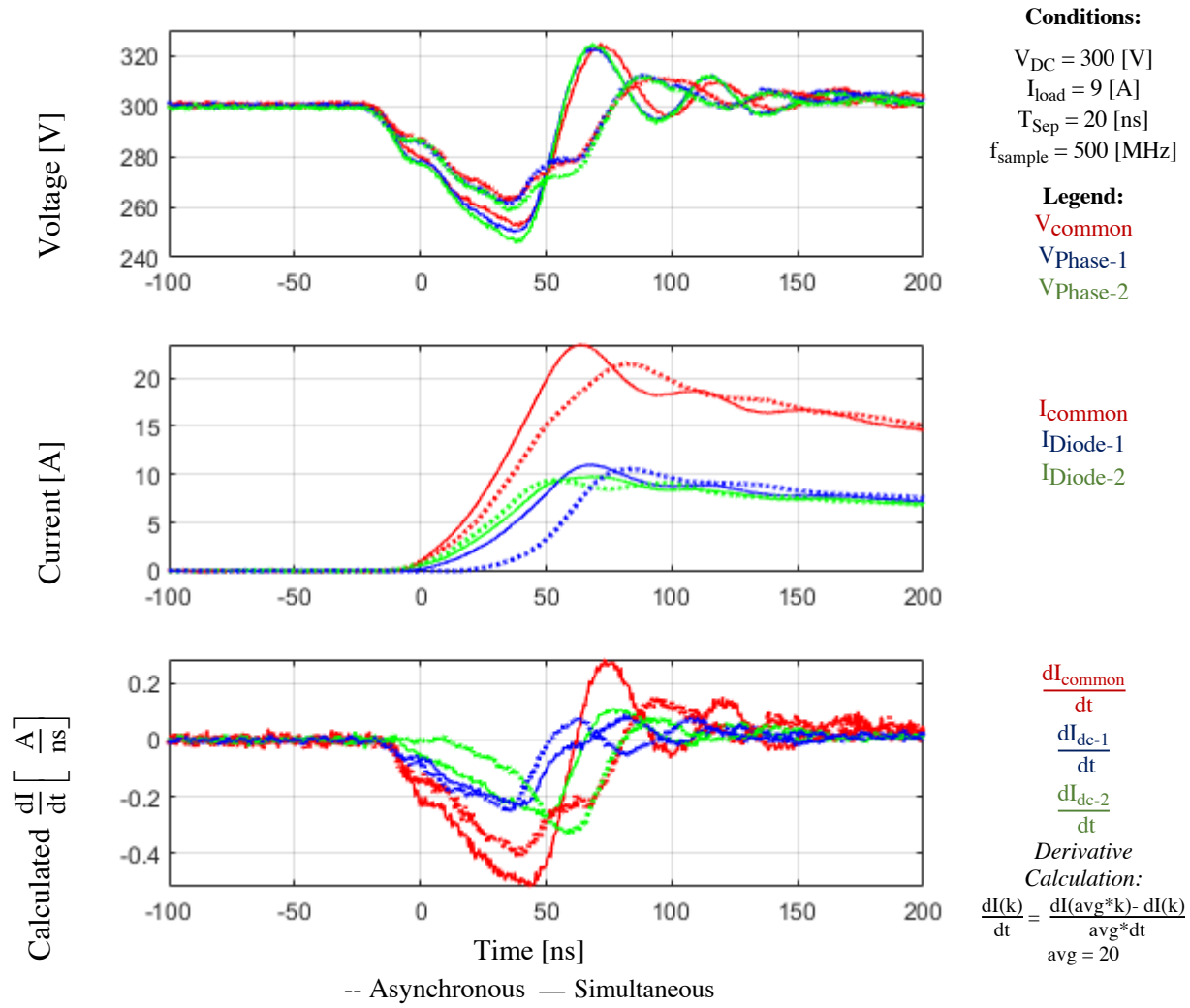


Figure 2-20: Overlaid comparison of time domain waveforms during a simultaneous Diode and asynchronous Diode transients.

Fig. 2-21 clearly summarizes the effect of T_{Sep} on voltage stresses during asynchronous IGBT turn-off. Here the cancelling effect of opposing-polarity di/dt is seen when T_{Sep} is roughly 30 [ns]. As T_{Sep} increases further, there is some coupling with the oscillations from the leading turn-off. However, after roughly 80 [ns] coupling between the two transients is nulled.

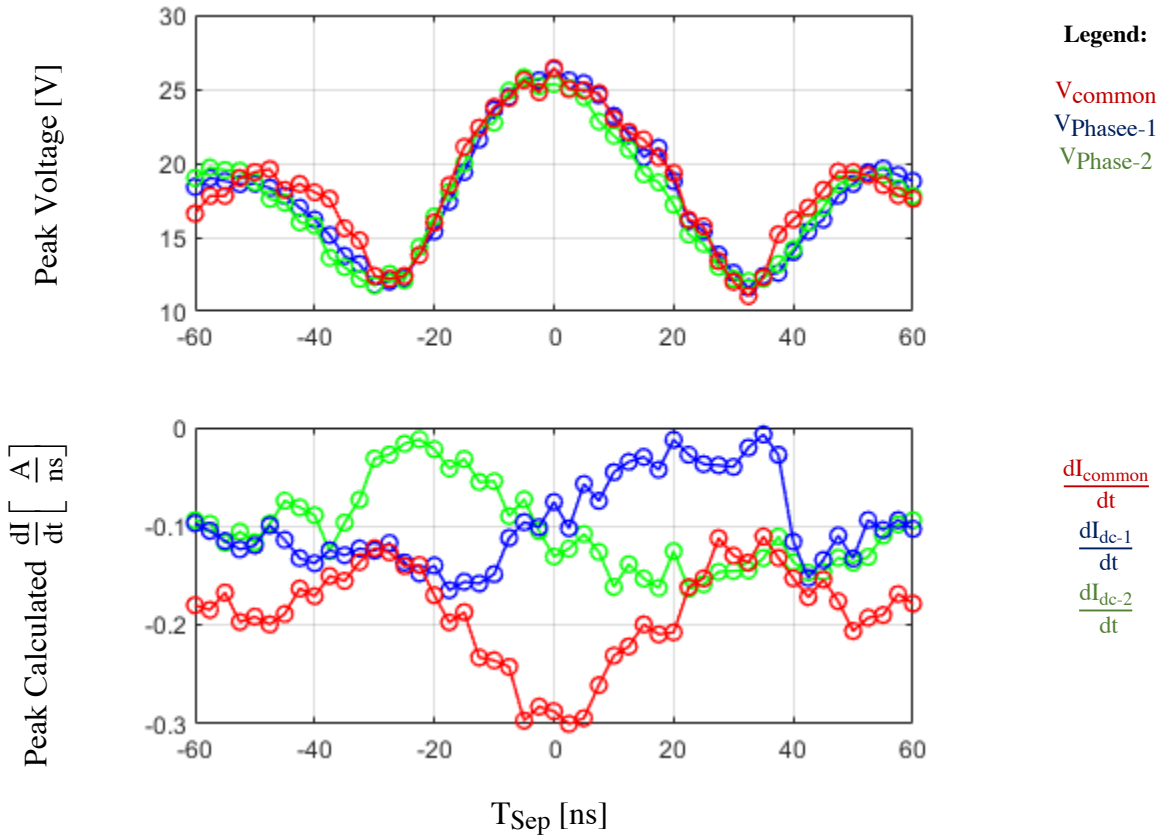


Figure 2-21: Peak voltage and di/dt values for asynchronous diode turn-offs with varying separation time.

Fig 2-22 shows that, unlike the simultaneous switching diode case, the asynchronous diode turn-off does result in increases in peak power loss for the diode being turned off second, when its initial turn-off overlaps with the first diode's reverse-recovery. However, this does correspond to a decrease in power losses experienced by the first diode. Once again, both diodes' peak losses return to their nominal values when their di/dt profiles are sufficiently separated.

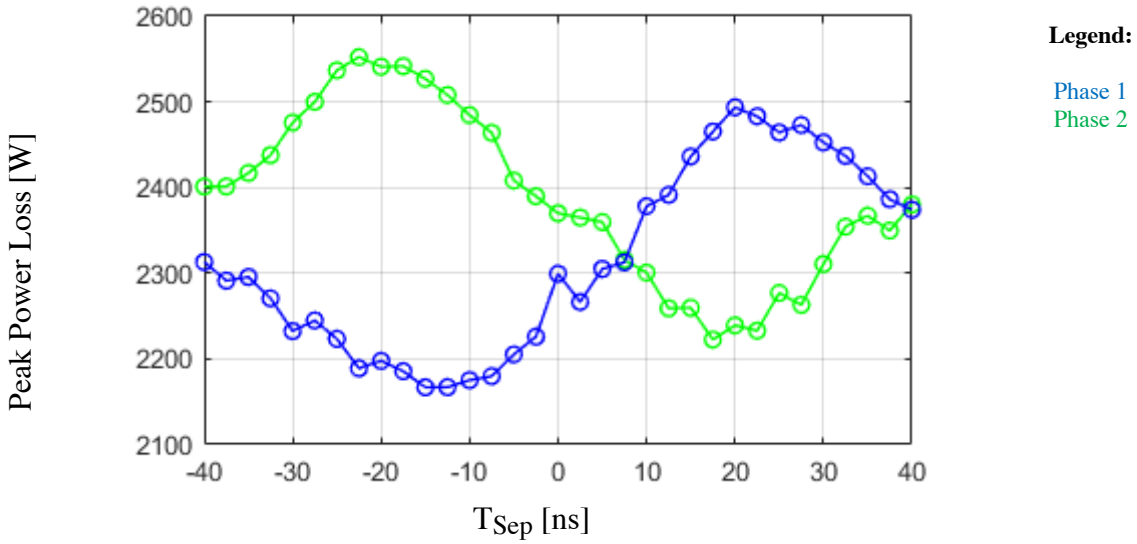


Figure 2-22: Peak voltage and di/dt values for asynchronous IGBT turn-offs with varying separation time.

2.3.3 Asynchronous IGBT-Diode Turn-off

The final possible Asynchronous turn-off case is that of an IGBT and diode. Taking what was learned from the previous asynchronous turn-off cases, the results are straight-forward. Fig. 2-23 shows time-domain waveforms for two test cases, one where the IGBTs turn-off overlaps with the diode's initial turn-off and one where it overlaps with the diode's reverse-recovery. The former case is shown with dotted lines where the opposing di/dt polarities in each device largely cancel out. This results in a small current transient measured through the common inductance and reduced peak voltage stress, particularly for the IGBT. For the case where the IGBT's turn-off overlaps with the diode's reverse-recovery, the di/dt profiles share the same polarity as they are overlapping. This increases voltage stresses, again particularly true for the IGBT. This coupling between the two devices is summarized as a function of T_{Sep} in Fig. 2-24.

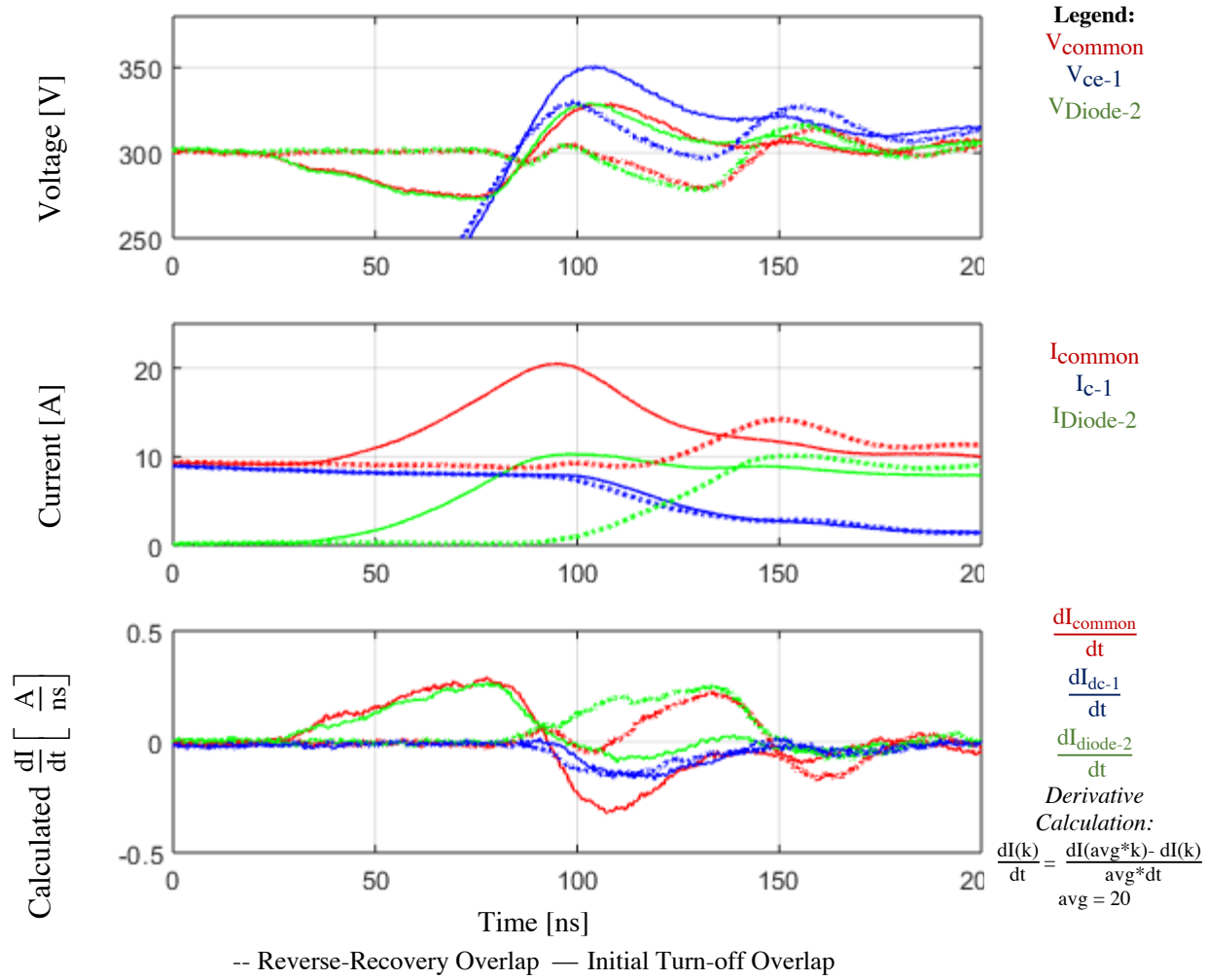


Figure 2-23: Overlaid comparison of time domain waveforms during a simultaneous Diode and asynchronous Diode transients.

Fig 2-24 shows how coupling between the IGBT and diode impacts peak power losses during switching. When the di/dt profiles overlap with negative polarity, voltage stresses increase on the IGBT and its switching power loss increases. When their opposing polarities overlap, the IGBTs peak losses decrease together with peak voltage stress. However, the diode's losses increase because the voltage stresses caused by the IGBT still increase the voltage being blocked by the diode during its reverse-recovery.

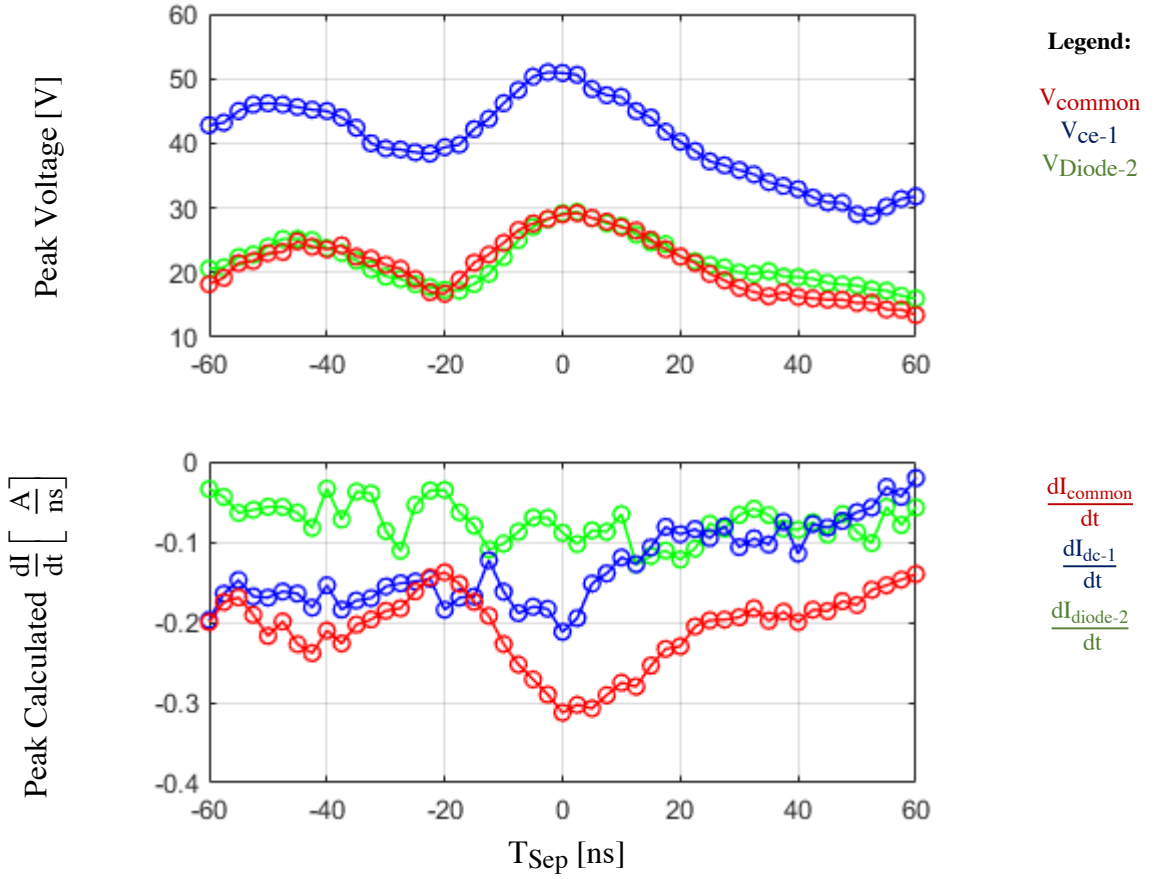


Figure 2-24: Peak voltage and di/dt values for asynchronous turn-off of an IGBT and diode with varying separation time.

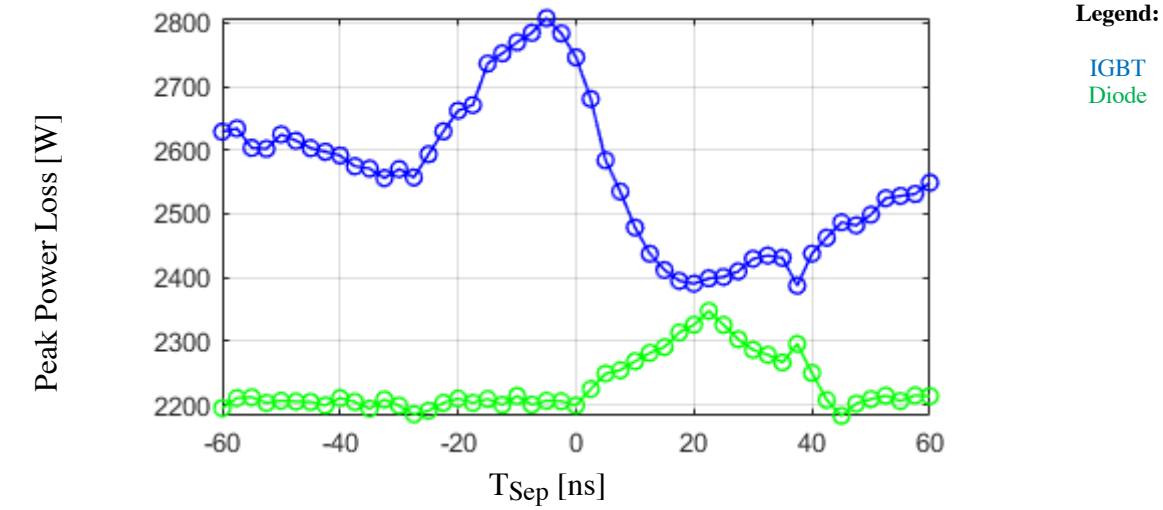


Figure 2-25: Peak power loss values for asynchronous IGBT turn-offs with varying separation time.

2.4 Summary

In this chapter, the effects of simultaneous switching, and overlapping switching in general were discussed. In contrast to the state-of-the-art, detailed measurements of switching transient voltages and currents, as well as calculations of di/dt and switching losses were performed across a range of load current conditions. Thus, a clearer picture of the conditions under which simultaneous switching is significant is drawn.

In all cases, effects are most significant when the load current being commutated is largest. This results in the largest magnitude di/dt, causing larger voltage stress coupling. Simultaneous IGBT turn-off, producing the highest di/dt magnitudes, resulted in the most significant voltage stress coupling and increased losses. Simultaneous diode turn-off did not produce voltage stresses as large as the IGBT case, due to its quick saturation of di/dt rates as load current increases. For all asynchronous switching transient test cases, regions of high di/dt must be sufficiently separated to mitigate any coupling between transients. The overlapping IGBT turn-off case is the simplest, resulting in rapidly decaying coupling between transients as the regions of peak di/dt are separated. Given the more complicated di/dt profile of a diode turn-off, asynchronous diode turn-off produces more complex effects, depending on how the falling forward current and reverse-recovery currents overlap. Similar effects can also be seen for the asynchronous IGBT-diode turn-off as the IGBT's di/dt profile overlaps with the positive and negative di/dt portions of the diodes turn-off.

Keeping these results in mind, it should be remembered that the absolute or relative severity of any simultaneous switching condition will be determined by the specific hardware used to construct the converter; including power electronic devices, gate drivers, as well as DC link layout and placement of decoupling capacitors. So, the true value of SSA on improving transient waveforms will be highly dependent on the converter design it is applied to.

Chapter 3 Current Source Modeling for Estimation of Voltage Overshoot

In this chapter, simple analytical models for estimating peak transient voltage overshoot are explored and compared to experimental and simulation results. The purpose of this modeling effort is not to reproduce precise time-domain responses of turn-off transients. Rather, it is on providing simple methods to estimate peak voltage overshoot while minimizing the need for detailed circuit parameter information. In doing so, one can apply these methods at the beginning stage of a design process to understand design trade-offs and establish benchmarks for commutation loop inductance minimization in conjunction with a desired switching speed. This can then be used to understand their implications on the required voltage margin (i.e. the difference between the converters DC bus voltage and the maximum blocking voltage of the switching devices used to construct the converter).

These are then extended to the case of simultaneous switching to identify trends, as a function of shared commutation loop inductance, on required voltage margin in a particular design. Similar modeling techniques are then applied to simulated commutation loop circuits utilizing decoupling capacitors. Finally, a per-unit analysis approach to switching transient modeling is proposed to facilitate comparison of switching speed and parasitic inductance across different device types and power levels is proposed. Through this work, a clearer understanding of simultaneous switching impacts on parasitic inductance, decoupling capacitor sizing, and voltage margin requirements is achieved.

3.1 Modeling Scope for Voltage Overshoot Estimation

To provide voltage overshoot estimates from the standpoint of an initial design concept, it is useful to start with a simple commutation model that is divorced from as many circuit design details as possible. To do this, the model shown in Fig 3-1 is proposed.

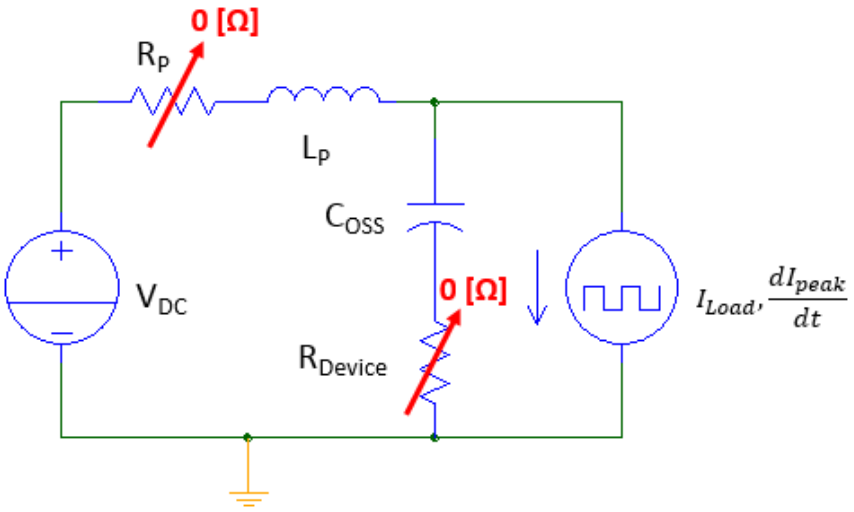


Figure 3-1: Commutation model to be used for voltage overshoot estimation

Beginning with the current source model that takes the place of the switching device, it can simply be defined based on the peak load current. In addition, dI_{peak}/dt can be defined based upon a combination of design consideration: the desired switching frequency and switching transient duration. These two quantities will define the noise envelope generated during operation and will drive EMI filtering requirements in conjunction with the application's relevant regulatory requirements. Taking this approach to defining the current source model parameters removes the need for modeling the behavior of the gate drive circuitry in combination with the specific switching device selected for a final design. As the design process progresses, one can then design the gate drive such that dI_{peak}/dt is not exceeded.

The inclusion of the switching device's output capacitance in parallel with the current source model is not inherently necessary for these approximate models. As was covered in the State-of-the-art review, simple inductive models of commutation loop impedance ($V = L*dI_{peak}/dt$) are often used to obtain rough estimates of overshoot voltage, or to estimate commutation loop inductance based on experimentally measured overshoot. However, the resonance introduced by this capacitance can lead to underestimation of voltage overshoot. So, for the purpose of completeness, both models will be utilized and compared in this section. While the inclusion of C_{OSS} is inherently tied to the device being used, rough estimates can be obtained from supplier datasheets. While

these capacitance values vary the rated power level of a specific device, they do remain well within an order of magnitude for a given device technology and power rating (Table 3.1). This is useful to note, as the impact of C_{OSS} on natural frequency and resonance peaks scale by the square root of C_{OSS}.

Table 3.1: Summary of reported output capacitance for a variety of Si IGBTs and SiC MOSFETs from different suppliers and for different rated voltage and current levels.

Si IGBTs					**SiC MOSFETs**				
Supplier	**Product**	**Voltage [V]**	**Current [A]**	**Output Capacitance [pF]**	**Supplier**	**Product**	**Voltage [V]**	**Current [A]**	**Output Capacitance [pF]**
Infineon	IKW40N60H3	600	40	80	Cree	C3M0065090D	900	36	70
Infineon	IKW40N120H3	1200	40	150	Cree	C2M0080120D	1200	36	90
Infineon	IKW75N60H3	600	75	200	Cree	C2M0080170D	1700	36	105
Infineon	IKY75N120CH3	1200	75	300	Cree	C3M0021120D	1200	100	180
Semikron	SK25NEB066T	600	30	190	Rohm	SCT3080AR	650	30	40
Semikron	SK100GD066T	600	100	380	Rohm	SCT3080KLHR	1200	30	70
Mitsubishi	CM100MXUB	650	100	500	Rohm	SCT3022ALHR	650	90	118
Mitsubishi	CM100MXUC	1200	100	500	Rohm	SCT3022KLHR	1200	90	240

Finally, with the inclusion of this LC resonance, the damping introduced by resistances in the DC bus structure and the switching device itself will certainly play a role in reducing the resonance peak and determining the severity of voltage ringing after turn-off. However, neglecting these resistance terms does help to provide a worst-case estimate of voltage overshoot. Moreover, these damping sources will be dependent on the DC bus design and its AC resistance characteristics. So, for the sake of simplicity, damping is neglected in the modeling presented in this chapter. If desired, one can add these effects into the model later in the design process through one of two methods: simply multiplying the resonance term by an exponential decay factor ($e^{-\zeta\omega_n t}$) or by altering the commutation loop impedance to include these effects and carrying out the inverse Laplace Transform with the desired current source input model.

3.2 Current Waveform Approximations During IGBT or MOSFET Turn-Off

The next step in this process is to define a current transient model to be used as the model's input excitation. As shown in the state-of-the-art review, the most common model used is a ramp model defined by the rated load current being commutated and an approximate turn-off time, τ_{off} (3.2-1). One can go about defining τ_{off} in different ways, such as manually or algorithmically fitting the ramp to experimental measurements, one can simply define it based on I_{load} and dI_{peak}/dt as shown in (3.2-2). Defining τ_{off} based on dI_{peak}/dt is beneficial as it is both straight-forward and helps to facilitate a worst-case overshoot estimate, particularly for a purely-inductive impedance model.

Another simple model that can be employed to describe the turn-off transient is an exponential decay function. Once again, this can be defined using only I_{load} and τ_{off} (3.2-3). This approach has its own advantage, particularly for IGBT modeling, in more accurately capturing the tail current effect introduced by its BJT structure. Fig 3-2 shows comparisons of the two current transient models for experimentally measured current transients for an IGBT and SiC MOSFET. A summary of test conditions and estimated circuit parameters for each case is given in Table 3.2.

Table 3.2: Summary of estimated circuit parameters and operating conditions for the two example converter circuits constructed using Si IGBTs and SiC MOSFETs.

Si IGBTs (IKA50N60T)					**SiC MOSFETs** (C3M0065090J)				
Bus Voltage V_{DC} [V]	**Current I_C [A]**	**Loop Inductance L_p [nH]**	**Output Capacitance C_{OSS} [nF]**	**Peak dI/dt [A/ns]**	**Bus Voltage V_{DC} [V]**	**Current I_C [A]**	**Loop Inductance L_p [nH]**	**Output Capacitance C_{OSS} [nF]**	**Peak dI/dt [A/ns]**
300	8.4	180	0.1	0.17	300	14.5	40	0.1	1.45

$$I_{Ramp}(t) = \begin{cases} I_{Load} & t < 0 \\ I_{Load}\left(1 - \frac{t}{\tau_{off}}\right) & 0 < t < \tau_{off} \\ 0 & \tau_{off} < t \end{cases} \quad (3.2\text{-}1)$$

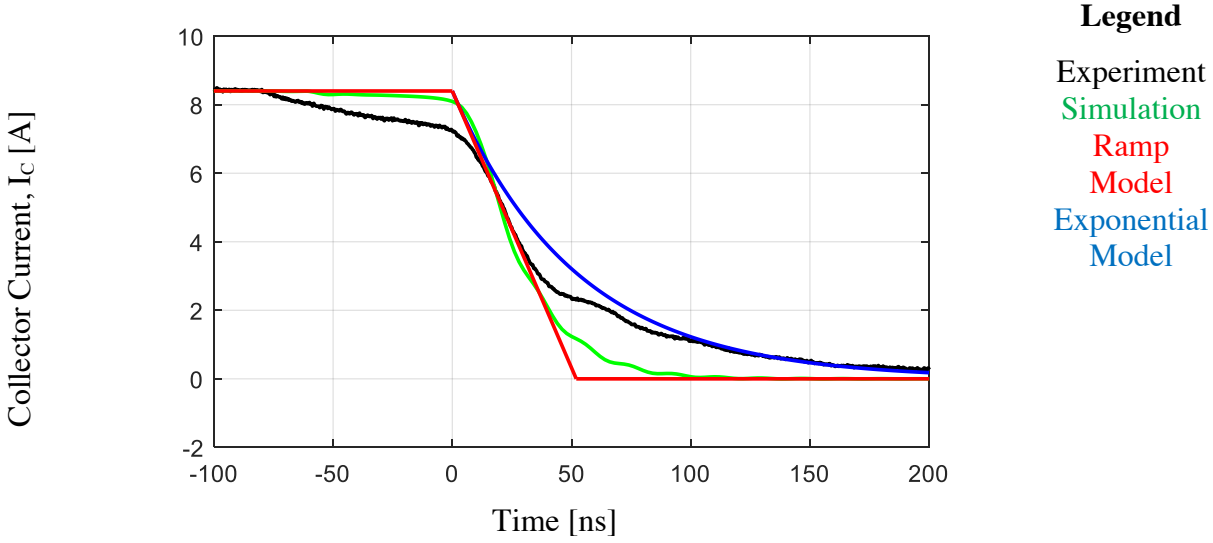
$$\tau_{off} = I_{Load} \div \frac{I_{peak}}{dt} \quad (3.2\text{-}2)$$

$$I_{expon}(t) = I_{Load} \times \exp\left(\frac{-t}{\tau_{off}}\right) \quad (3.2\text{-}3)$$

Both of the proposed turn-off current models can be easily described in the Laplace domain. This is shown in (3.2-4) and (3.2-5) for the ramp exponential decay model, respectively.

$$I_{ramp}(s) = \frac{I_{Load}}{\tau_{off}}\left[\frac{1 - \exp(-s\tau_{off})}{s^2}\right] \quad (3.2\text{-}3)$$

$$I_{expon}(s) = I_{Load}\frac{1}{s(\tau_{off}\, s + 1)} \quad (3.2\text{-}4)$$



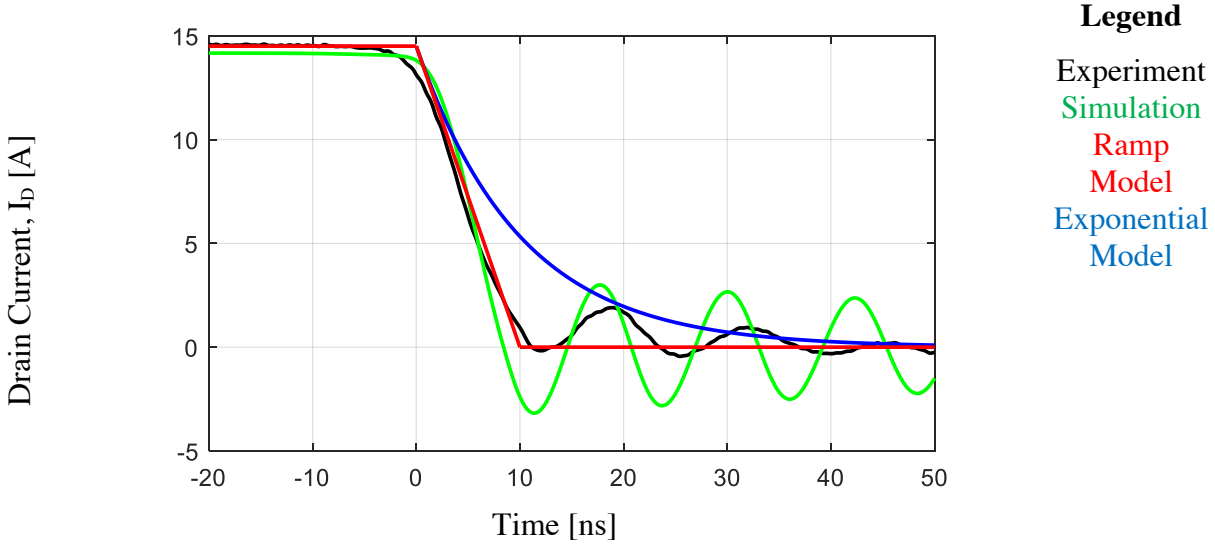


Figure 3-2: Current transient models overlaid with both simulation and experimentally measured IGBT (top) and SiC MOSFET (bottom) turn-off transients.

3.3 Commutation Loop Impedance Model Approximations

For this modeling work, both the purely-inductive and LC resonant impedance models will be compared. The Laplace domain impedances for these two models is given in (3.3-1) and (3.3-2) for the inductive and LC resonant model cases, respectively. The natural frequency of the LC resonant circuit is defined in (3.3-3).

$$Z_L(s) = -L_p s \tag{3.3-1}$$

$$Z_{LC}(s) = \left(\frac{1}{C_{OSS}}\right)\frac{s}{(s^2 + \omega_n)} \tag{3.3-2}$$

$$\omega_n = \frac{1}{\sqrt{L_p C_{OSS}}} \tag{3.3-3}$$

3.4 Single-Phase Turn-off Overshoot Approximations

The final step to obtaining a time-domain response is to combine the current transient input model and the impedance models in the Laplace domain (3.4-1) and perform the inverse Laplace Transform (3.4-2). Taking all possible model combinations for the sake of completeness, this results in four different time-domain voltage overshoot estimates given in (3.4-3) through (3.4-10).

$$\Delta V(s) = Z(s)I(s) \tag{3.4-1}$$

$$\Delta V(t) = L^{-1}\{\Delta V(s)\} \tag{3.4-2}$$

$$\Delta V_{L-Ramp}(t) = \begin{cases} 0 & t < 0 \\ L_p \dfrac{I_{Load}}{\tau_{off}} & 0 < t < \tau_{off} \\ 0 & \tau_{off} < t \end{cases} \tag{3.4-3}$$

$$\Delta V_{LC-Ramp}(t) = \begin{cases} 0 & t < 0 \\ L_p \dfrac{I_{Load}}{\tau_{off}}[1 - \cos(\omega_n t)] & 0 < t < \tau_{off} \\ L_p A \dfrac{I_{Load}}{\tau_{off}} \cos(\omega_n t + \Phi) & \tau_{off} < t \end{cases} \tag{3.4-4}$$

$$A_{ramp} = \sqrt{2 - 2\cos(-\omega_n \tau_{off})} \tag{3.4-5}$$

$$\Phi_{ramp} = \tan^{-1}\left[\frac{\sin(-\omega_n \tau_{off})}{\cos(-\omega_n \tau_{off}) - 1}\right] \tag{3.4-6}$$

$$\Delta V_{L\text{-}expon}(t) = \left(\frac{I_{Load}}{\tau_{off}}\right)\exp\left(\frac{-t}{\tau_{off}}\right) \tag{3.4-7}$$

$$\Delta V_{LC\text{-}expon}(t) = \frac{I_{Load}\sqrt{L_p}}{\tau_{off}\left(\omega_n^2 + \dfrac{1}{\tau_{off}^2}\right)\sqrt{C_{OSS}}}\left[\omega_n \exp\left(\frac{-t}{\tau_{off}}\right) + A_{expon}\sin(\omega_n t + \Phi_{expon})\right] \tag{3.4-8}$$

$$A_{expon} = \sqrt{\omega_n^2 + \frac{1}{\tau_{off}^2}} \tag{3.4-9}$$

$$\Phi_{expon} = \tan^{-1}(-\omega_n \tau_{off}) \tag{3.4-10}$$

Fig 3-3 shows a comparison of these different undamped overshoot models with both experimental and simulation results for both an IGBT and SiC MOSFET circuit. Beginning with the inductive models in the IGBT case, the differences between a ramp and exponential excitation are trivial from a peak overshoot perspective. The peak voltage stress will simply be given by the inductance scaled by modelled dI/dt. However, one can see that the exponential response more closely resembles the experimental and simulated response due to its more accurate representation of the IGBT's tail current. Finally, one can see that these inductive models do underestimate the peak voltage stress. A summary of peak voltage overshoot values for each model is given in Table 3.3

Moving to the responses of the undamped LC resonant impedance model, both models overestimate both the peak voltage stress and the oscillation frequency. This is of course due to

resistances being neglected. The experimentally measured overshoot waveform, in comparison with the analytical responses, highlight the relatively large amount of damping introduced by both the IGBT's BJT structure in conjunction with resistances in the commutation loop. This relatively overdamped response is characteristic of IGBT turn-off transients in general. So, one can expect undamped models of the commutation loop to overestimate overshoot.

Moving to the SiC MOSFET circuit example, Similar trends can be observed for the relative under and overestimation of voltage overshoot for the inductive and LC impedance models, respectively. However, as is characteristic of MOSFET turn-off transients, experimental results indicate significantly less damping than the IGBT case. This leads to much better agreement for the exponential response model. Conversely, the ramp model's overshoot estimation error actually increases going from the IGBT to MOSFET case. The reason for this effect is due to the ratio of ω_n to τ_{off} in the commutation loop model (This relationship is explored further in Section 3.6).

Finally, for both the MOSFET and IGBT examples, simulated models that include detailed nonlinear models of the switching devices do result in the closest agreement of all the analysis techniques. However, it is worth highlighting that constructing these models to faithfully reproduce experimental measurements requires more time and effort than using the simple analytical methods presented here and accepting that a larger degree of error is inevitable. This is particularly true for IGBT circuits, where the relatively complex device structure introduces a significant modeling challenge. In the following sections of this chapter, simulation models will be used as a stand-in for experimental results to explore the impact of parasitic inductance and decoupling capacitor variations on voltage overshoot during simultaneous switching events.

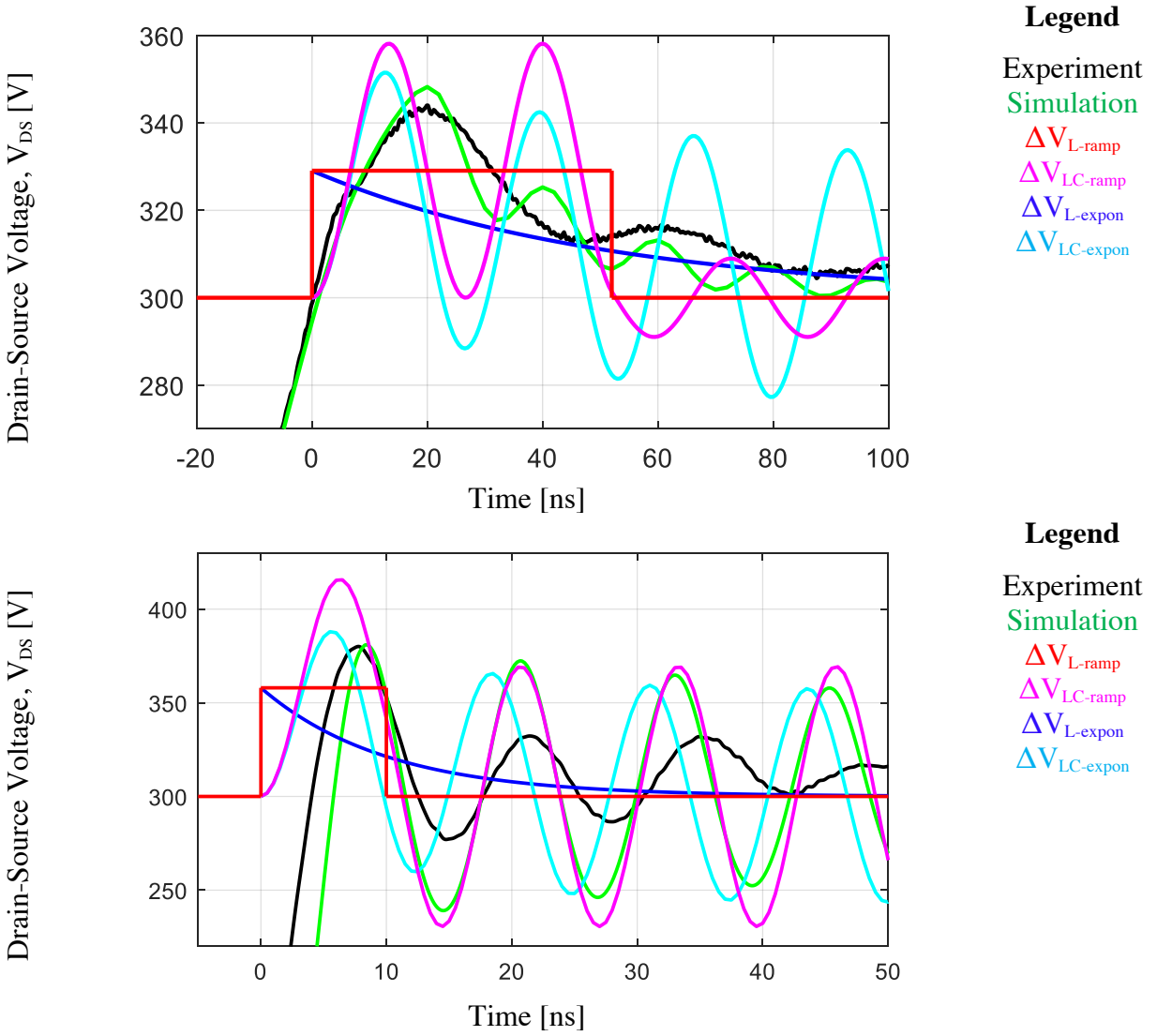


Figure 3-3: Undamped voltage overshoot models overlaid with both simulated and experimentally measured IGBT (top) and SiC MOSFET (bottom) turn-off transients.

Table 3.3: Summary of peak voltage overshoot values for each model approach compared to experimental and simulative results.

		Experiment	Simulation	LC Expon.	LC Ramp	Inductive
IGBT	Overshoot Voltage [V]	44 [V]	48 [V]	52 [V]	58 [V]	29 [V]
	Error [%]	-	9 %	18 %	32 %	- 34%
SiC	Overshoot Voltage [V]	80	81	88	116	58
	Error [%]	-	1%	10 %	45 %	- 28%

In summary, the analytical models presented here provide a relatively quick method for estimating peak voltage overshoot in power converter commutation loops. While there is an

unavoidable degree of error introduced by these modeling approaches, the inductive and LC-exponential response models help provide reasonable upper and lower bounds on voltage overshoot that can be used to define commutation loop design requirements.

3.5 Two-Phase Simultaneous Turn-off Overshoot Approximations

Moving from the single-phase to two-phase simultaneous switching case, the same modeling approaches can be applied. To enable this, some model simplifications can be applied to the two-phase circuit to reduce it to a single-phase equivalent model. This simplification is shown in Fig 3-4 and described in equations (3.5-1) through (3.5-4). Here, it is assumed that the parasitic inductance distribution is symmetrical and that each phase is operating at the same load current condition. This is the same simplification approach used by previous researchers as shown in Section 1.1-4.

Using this simplified circuit, the same voltage overshoot comparisons can be made for the different impedance and excitation models as was done in Section 3.4. Once again the same trends can be observed. The inductive commutation loop model underestimates voltage overshoot as it doesn't take into account the resonance introduced by the device's output capacitance. However, the error of this inductive estimate actually decreases slightly, from 34% to 29%. Moving to the LC resonant circuits, both excitation models lead to overestimation of voltage overshoot for the IGBT example due to relatively large amount of damping that exists in the actual commutation loop. However, the exponential excitation does perform noticeably better than the ramp model due to its more accurate modeling of the IGBT tail current. It is worth noting that peak di/dt actually decreases slightly when the effective inductance increases during a simultaneous switching event. This effect was observed in the experimental results presented in Chapter 2 and is once again shown in simulation results presented in Fig 3.6.

For the SiC MOSFET example, no simultaneous switching measurements were taken as the circuit used was designed for single-phase double-pulse tests only. In the absence of experimental data, simulation results will be used as a stand in. Here, the inductive model once again leads to

an underestimate of voltage overshoot while the LC resonant impedance model with ramp excitation overestimates overshoot. However, the percent error decreased from 45% to 29% as shown in the peak overshoot summary given in Table 3.4. Moreover, the exponential excitation with an LC resonant impedance model actually underestimates voltage overshoot with 7% error while it overestimated overshoot by 10% in the single phase case. The reason for this change in estimation accuracy can be seen by observing the impact of simultaneous switching on peak di/dt. Simulation results presented in Fig 3.6 show that peak di/dt actually increases as the effective parasitic inductance imposed on the transient increases.

It is worth highlighting that this characteristic difference between the IGBT and MOSFET examples can be observed in previous experimental simultaneous switching results presented in Section 1.4. In these tests, it was observed that the IGBT overshoot increased by 30% during simultaneous switching while the MOSFET overshoot increased by 80% when the devices were placed in identical converter circuits.

$$I_{cc\text{-}tot} = I_{cc\text{-}1} + I_{cc\text{-}2};\ \frac{dI_{cc\text{-}tot}}{dt} = \frac{dI_{cc\text{-}1}}{dt} + \frac{dI_{cc\text{-}2}}{dt} \tag{3.5-1}$$

$$Z_{L\text{-}simult}(s) = (2L_{cc} + L_1)s \tag{3.5-2}$$

$$R_{cc} = \frac{L_{cc}}{L_p};\ L_p = L_{cc} + L_1 \tag{3.5-3}$$

$$Z_{L\text{-}simult}(s) = L_p(1 + R_{cc})s \tag{3.5-4}$$

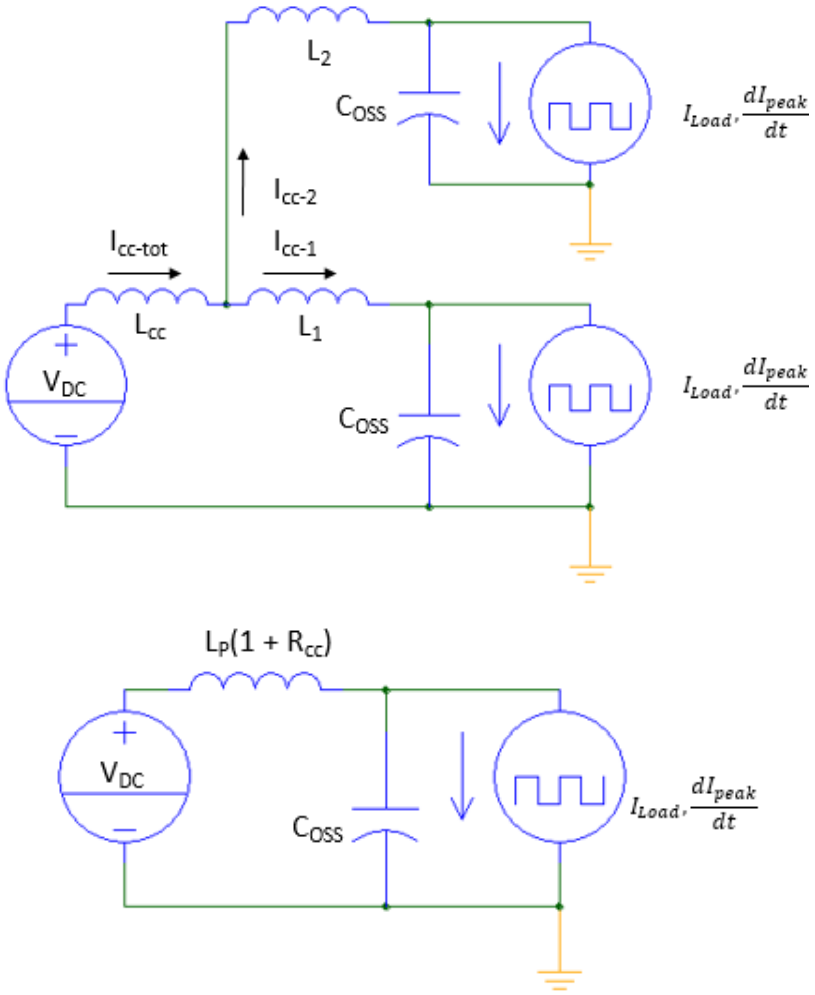


Figure 3-4: Model simplification (bottom) for evaluating simultaneous switching voltage stress in a symmetrical two-phase circuit (top).

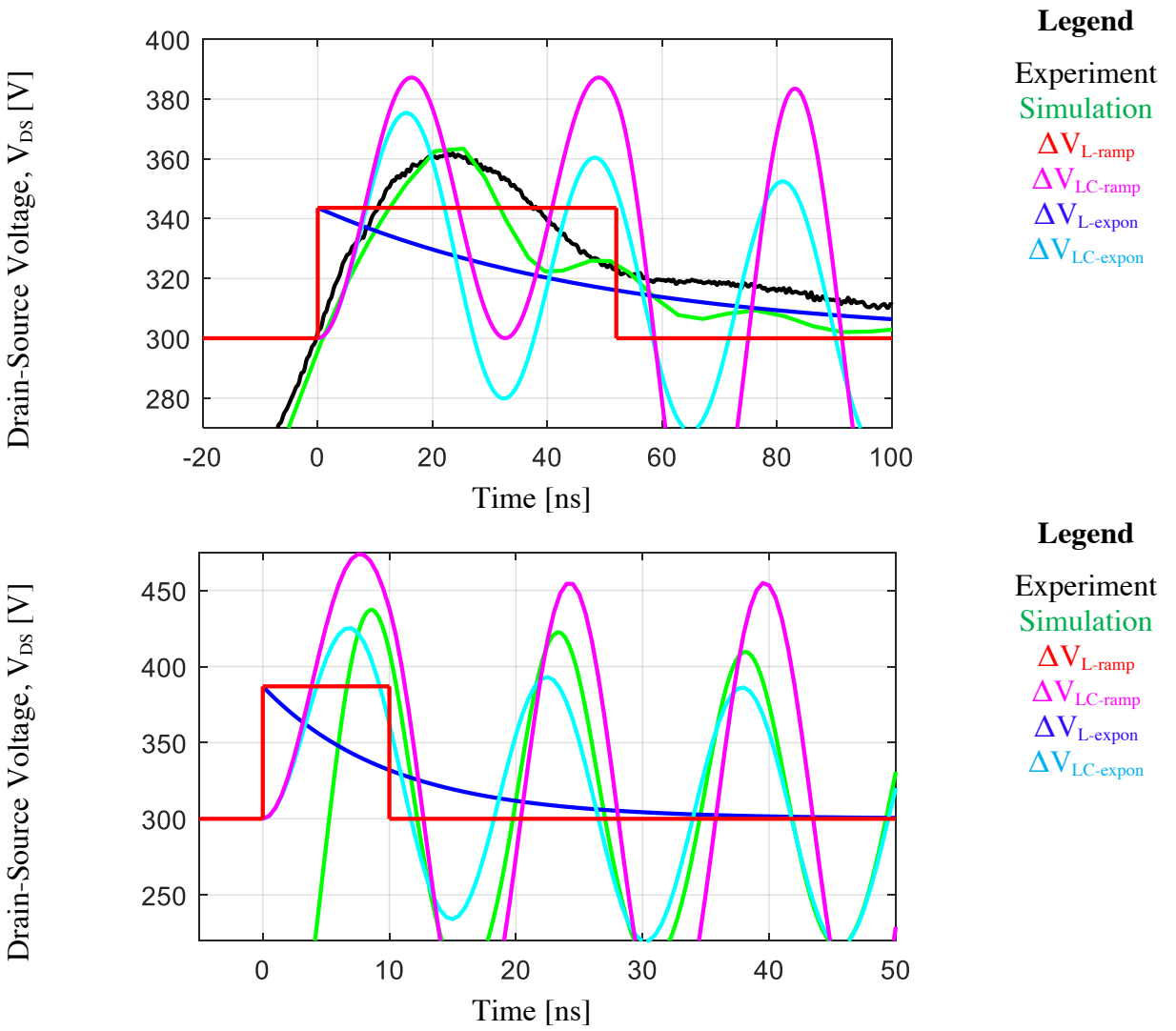


Figure 3-5: Undamped voltage overshoot models overlaid with both simulated and experimentally measured IGBT (top) and simulated SiC MOSFET (bottom) turn-off transients for the case when $R_{cc} = 0.5$.

Table 3.4: Summary of peak voltage overshoot values for each model approach compared to experimental and simulative results for the two-phase simultaneous switching case.

		Experiment	Simulation	LC Expon.	LC Ramp	Inductive
IGBT	Overshoot Voltage [V]	62 [V]	63 [V]	75 [V]	87 [V]	44 [V]
	Error [%]	-	2 %	21 %	40 %	- 29 %
SiC	Overshoot Voltage [V]	n/a	135	125	174	87
	Error [%]	n/a	-	-7 %	29 %	- 36 %

It is no doubt useful to compare absolute values of peak voltage overshoot values between single and simultaneous switching events in a specific converter circuit under specific operating conditions for the purpose of insuring adequate voltage margin. However, from the standpoint of better understanding di/dt coupling effects on voltage overshoot in general, it is more useful to look at the relative increase in overshoot as a function of the common coupling ratio, R_{cc}. This can better inform a circuit designer on the implications of commutation loop design before any hardware is constructed.

This ratio describing the increase in voltage overshoot during a simultaneous switching event can be determined quite easily for the inductive commutation loop model and is given in (3.5-5). This analytical model suggest that voltage overshoot will increase linearly with R_{cc}. However, one should note that this approximation assumes peak di/dt remains unchanged during a simultaneous switching event. LC resonant circuit model does not lend itself to such a simple expression, because the peak voltage stress depends on a trigonometric function of ω_n which changes as the common coupling inductance, L_{cc}, changes. Taking the exponential response as an example, the voltage stress increase (3.5-7) can be calculated by varying the common coupling ratio, R_{cc}, and evaluating (3.4-8) at the instance in time given in (3.5-8) for different values of R_{cc}. In addition to the need for numerically evaluating this expression for different values of R_{cc}, (3.5-7) will also vary for different values of ω_n and τ_{off} (That is, the relative values of C_{OSS}, L_p, and switching speed) as these both play a role in determining the peak value of $\Delta V_{LC\text{-}Expon}$.

$$\frac{\Delta V_{L\text{-}simult}}{\Delta V_L} = (1 + R_{cc}) \tag{3.5-5}$$

$$R_{cc} = \frac{L_{cc}}{L_p} \tag{3.5-6}$$

$$\frac{\Delta V_{LC\text{-}Expon\text{-}simult}}{\Delta V_{LC\text{-}Expon}} \tag{3.5-7}$$

$$t_{max} = \frac{\pi/2 - \tan^{-1}(-\omega_n \tau_{off})}{\omega_n} \tag{3.5-8}$$

To evaluate the efficacy of these voltage overshoot ratio models, a set of simulations was carried out for both the IGBT and MOSFET examples where R_{cc} was varied from 0.1 to 0.9 while holding L_p constant. A summary of voltage and current waveforms for each is given in Fig 3-6. Unsurprisingly, voltage overshoot increases for both examples as the effecting commutation loop inductance increases. However, looking at the current waveforms, one can see that di/dt does not remain constant under different R_{cc} conditions. For the IGBT case, the initial fall in collector current slows down as R_{cc} increases leading to a decrease in peak di/dt. Conversely, peak di/dt in the MOSFET, which occurs approximately when the drain current initially crosses zero, actually increases. These changes in di/dt are not captured in the simplified turn-off transient models and should be considered when comparing analytical estimates to simulated or experimental data.

With that said, Fig 3-7 gives a summary of peak voltage overshoot values for different values of R_{cc}. As was seen previously for the inductive model underestimates voltage overshoot for all test conditions while the LC resonant model overestimates, as compared to simulation results. On the whole, all three models do provide similar rates of increase in peak voltage overshoot. However, the increase in simulated peak overshoot does begin to taper off as R_{cc} approaches 1 because the effective near-doubling of commutation loop inductance slows the turn-off transient to a certain degree.

Moving to the MOSFET example, both analytical models underestimate voltage overshoot for the simultaneous switching case. The LC resonant model does provide significantly closer estimates than does the inductive model. However, while both analytical models provide consistent rates of increase in voltage overshoot, simulation results indicate a higher rate of increase. This results from the increase in peak di/dt seen in the simulated current transient as the effective commutation loop inductance increases.

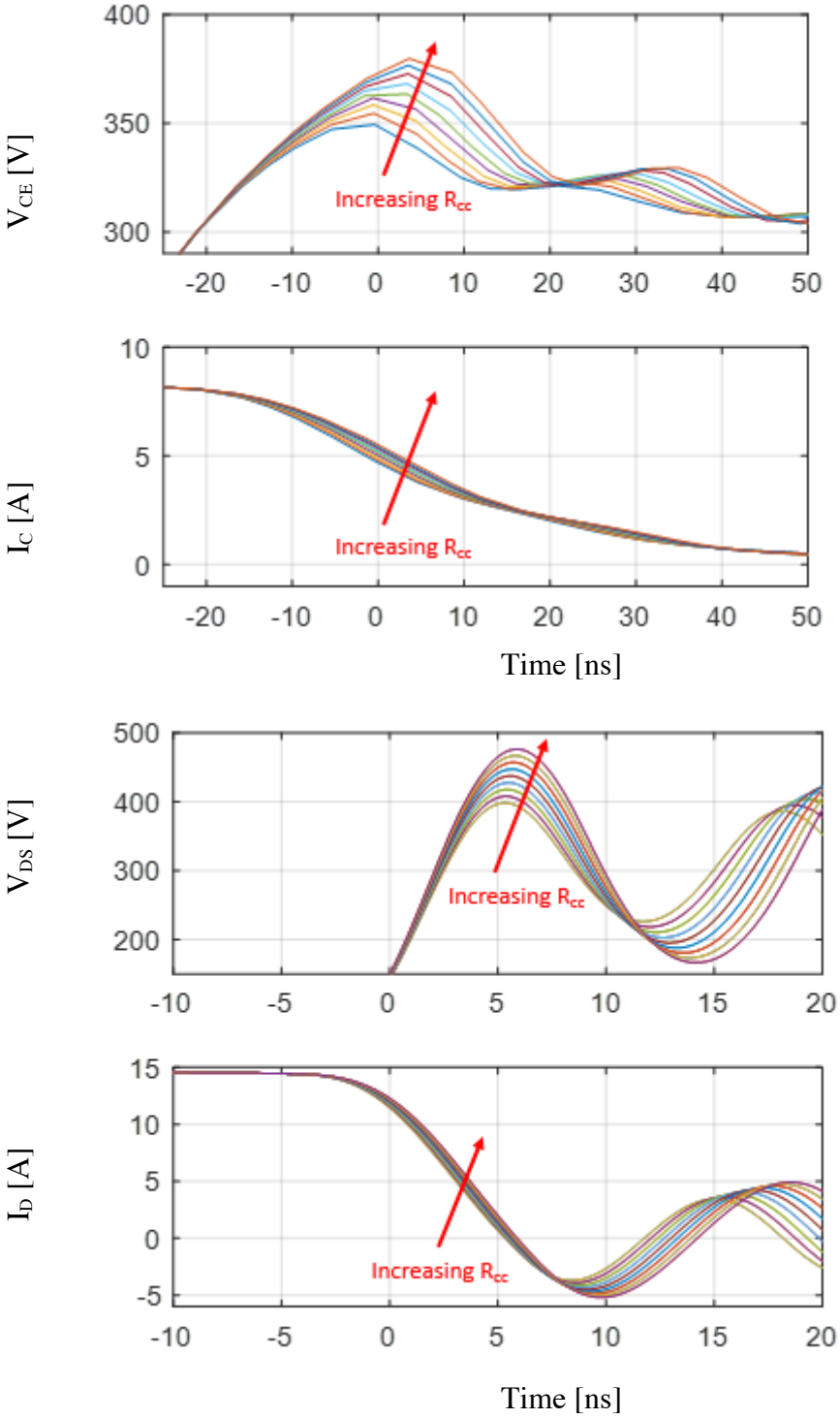


Figure 3-6: Simulated time-domain waveforms of simultaneous switching events for different values of R_{cc}, holding L_p constant.

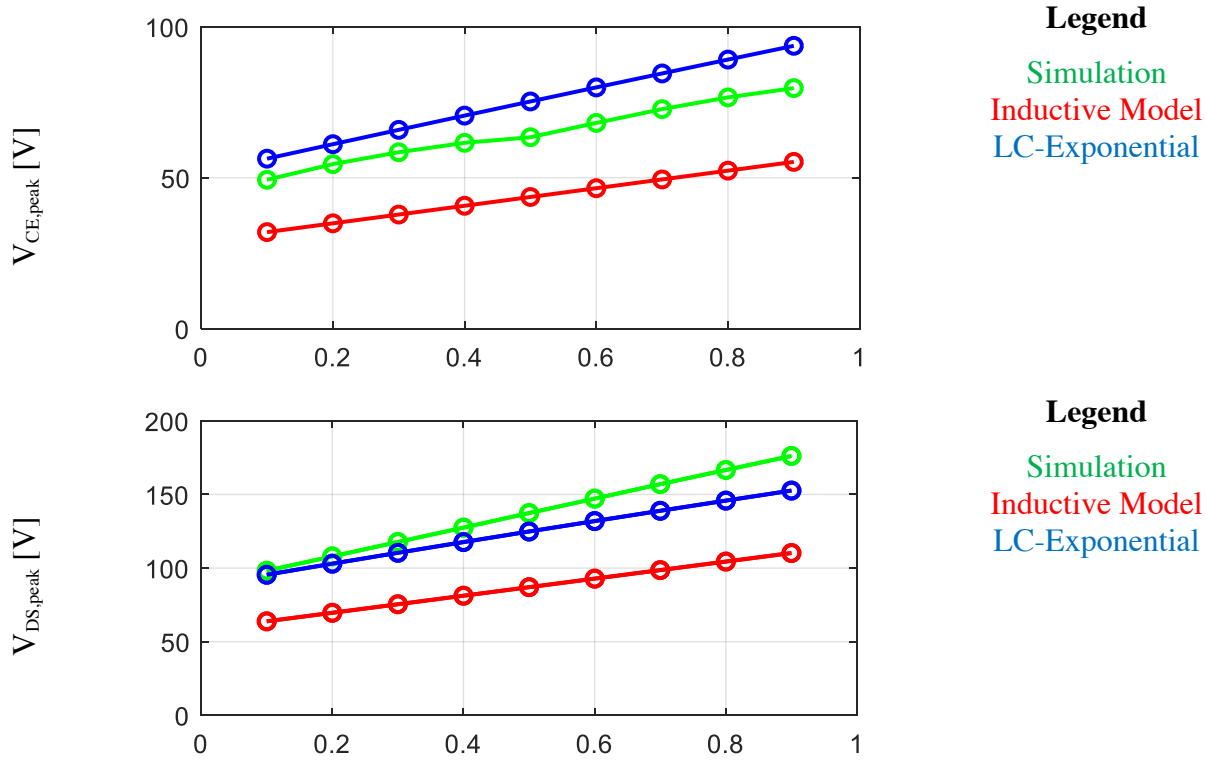


Figure 3-7: Simulated peak simultaneous switching overshoot values for the IGBT and MOSFET examples, compared to estimates produced by the inductive and LC impedance model with exponential current excitation.

Moving on to the relative increase in peak voltage overshoot going from the single-phase to simultaneous switching event, a summary of these ratios is provided in Fig 3-8. In the IGBT example, both analytical models provide overestimates of this overshoot magnification effect. An examination of the relative estimation errors of each method given previously provides an explanation. That is, the estimation error moves in the positive direction going from the single-phase to simultaneous switching events. So, when taking the ratio of these estimates, it leads to an overestimation of the voltage overshoot magnification during simultaneous switching. Moreover, one can observe the effect of decreasing peak di/dt as R_{cc} increases, as the overshoot magnification tapers off as R_{cc} approaches 1.

Conversely, in the MOSFET example, estimation error for the two analytical models moves in the negative direction. This leads to an underestimation of voltage overshoot magnification during

simultaneous switching. Moreover, because peak di/dt increases in the MOSFET as R_{cc} increases, the difference between analytical estimates and simulation results grows as R_{cc} increases.

Finally, comparing the trends in voltage stress magnification during simultaneous switching, both analytical models provide similar estimates regarding the impact of R_{cc}. That is, this increase in voltage stress trends linearly with R_{cc}. Granted, the impact of R_{cc} on peak di/dt will necessarily drive deviations away from this simplistic modeling approach, the underlining trend remains the same.

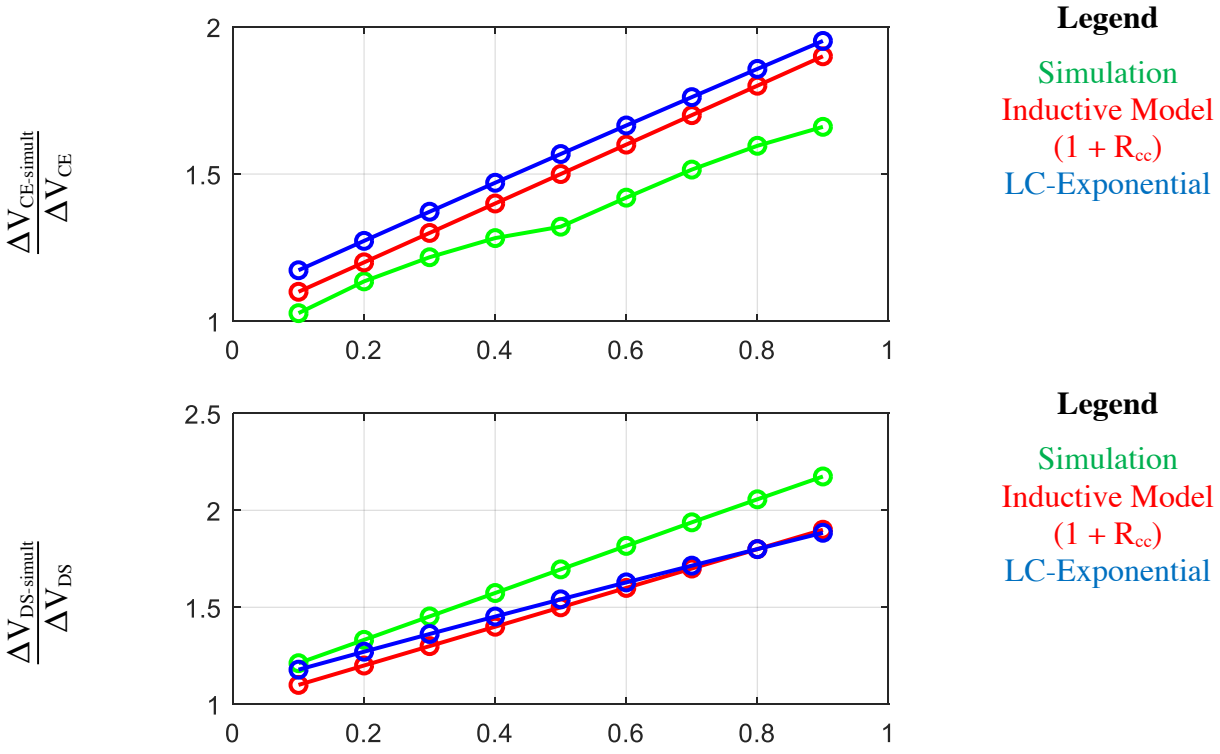


Figure 3-8: Relative increase in peak voltage overshoot between the single-phase and simultaneous switching events in the IGBT and MOSFET example cases.

In summary, there is underlying error in these simplified analytical approaches that do not account for the nonlinear effects that impact peak voltage overshoot during turn-off transients. These errors propagate through the analysis carried out here and lead to imperfect approximations of voltage overshoot magnification during simultaneous switching events. However, recalling that the purpose of this work is to provide simple methods for estimating these effects from a high-

level design standpoint, these do provide insight into the underlining trends of the di/dt coupling effects created by shared commutation loop inductance during simultaneous switching. This can provide insight into commutation loop design impacts on voltage margin required in a multi-phase converter where simultaneous switching is a possibility.

3.6 Turn-off Overshoot Approximations with Decoupling Capacitors

As highlighted in Section 1.1.5, a common method for reducing the effective parasitic inductance in a commutation loop is the addition of high-frequency decoupling capacitors as close as possible to switching devices. As such, it is useful to explore how simultaneous switching will impact the efficacy of these capacitors in suppressing overshoot.

One key takeaway shown by research presented in Section 1.1.5 is that decoupling capacitors should be sized so that the effective capacitance is at least 10 times larger (and anywhere from 20 to 100 times larger in practice) than the output capacitance of the switching devices. In doing so, one ensures that the resonance frequency of the decoupled commutation loop is sufficiently separated from the new resonance mode introduced between the decoupling capacitor and the parasitic inductance being decoupled. In doing so voltage overshoot can be approximated as a simple sum of these two resonant circuits as expressed in (3.6-1). Further, if the decoupled commutation loop has a resonance that is significantly faster than that of the decoupling capacitor, it is assumed that any ringing within the commutation loop will decay before the decoupling capacitor reaches its peak overshoot value. Thus, one can analyze each loop independently and verify that neither will produce a peak voltage value that exceeds the switching device's rated blocking voltage.

$$\Delta V(t) = \Delta V_{dec}(t) + \Delta V_{OSS}(t) \tag{3.6-1}$$

However, most existing research assumes that the bulk capacitance, C_{bulk}, is sufficiently large that it behaves effectively like a stiff voltage source from the perspective of the decoupling capacitor, C_{dec}. Given that the trend in converter design is to minimize C_{bulk} for the sake of cost and space saving, it is useful to first identify when this assumption holds true. To do so, two circuit models will be compared as shown in Fig 3-9. On one extreme, the DC bus can be modelled without any voltage source where C_{bulk} and C_{dec} are the only energy sources in the circuit. On the other extreme C_{bulk} can be replaced by a stiff voltage source were it is assumed that the energy stored in C_{bulk} is sufficiently large so that it's voltage does not change during a switching transient. For the sake of completeness, the equivalent series inductance of the decoupling capacitor is included and its impact on these two models is evaluated.

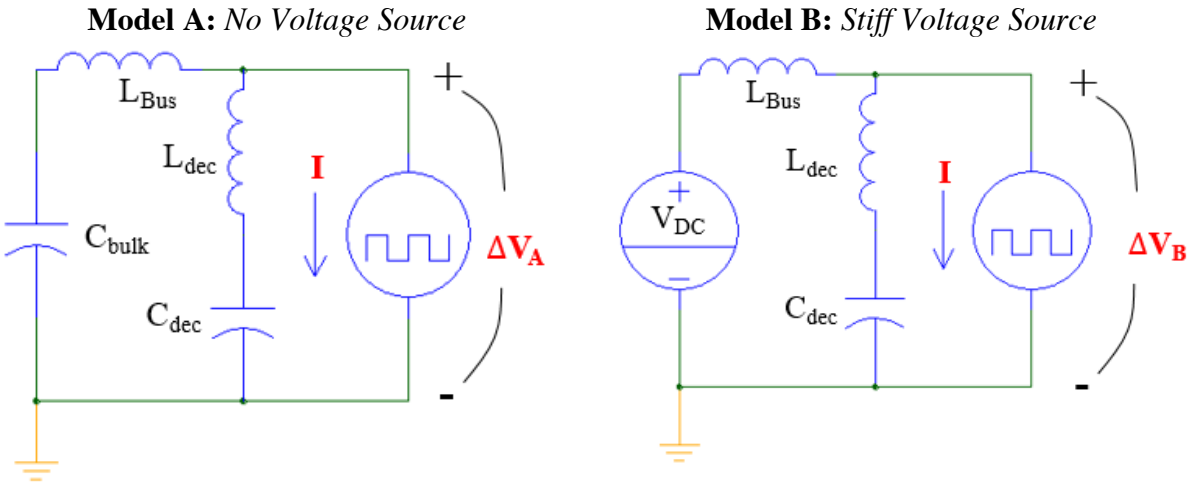


Figure 3-9: DC bus circuit models assuming that there is no external voltage source (Model A) and where the bulk capacitance can be modelled as a stiff voltage source (Model B).

Beginning with a comparison of natural frequencies, (3.6-2) and (3.6-3) provide expressions for the natural frequencies of Model A and Model B, respectively. Comparing the ratio of these two values, one arrives at the expression given in (3.6-4) where one can define a capacitance ratio, ε_c. evaluating (3.6-4) for a range of ε_c, values, Fig. 3-10. This shows that, for example, if ε_c is less than 0.1, these natural frequencies will only deviate by 5%. Similar to the sizing of $C_{dec}$with respect

to C_{OSS}, C_{bulk} should realistically be more than 10 times bigger than C_{dec} to ensure that Model B is a good approximation of the DC bus structure.

$$\omega_{n\text{-}A} = \sqrt{\frac{C_{bulk} + C_{dec}}{C_{bulk}C_{dec}(L_{bus} + L_{dec})}} \tag{3.6-2}$$

$$\omega_{n\text{-}B} = \sqrt{\frac{1}{C_{dec}(L_{bus} + L_{dec})}} \tag{3.6-3}$$

$$\frac{\omega_{n\text{-}A}}{\omega_{n\text{-}B}} = \sqrt{\frac{C_{bulk} + C_{dec}}{C_{bulk}}} = \sqrt{1 + \varepsilon_c} \tag{3.6-4}$$

$$\varepsilon_c = \frac{C_{dec}}{C_{bulk}} \tag{3.6-5}$$

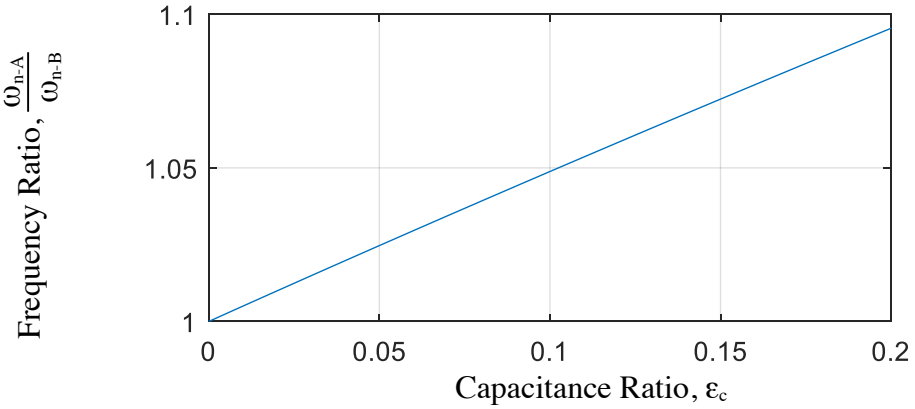


Figure 3-10: Natural frequency ratio between Model A and Model B as a function of ε_c.

Taking this approximation one step further, one can compare the response of these two models to a step change in load current flowing to the converter output, as an approximation of the turn-off transient. This can be done by taking the Laplace domain impedance models given in (3.6-1) through (3.6-5) and applying an inverse Laplace transform for a step input. These time domain responses are given in (3.6-6) and (3.6-7) for Model A and Model B, respectively. One can observe that Model A contains a term describing the discharge of C_{bulk} over time. This term must necessarily be negligible on the time scale of a switching transient in voltage source converters if the DC bus voltage is to remain relatively stable across a switching period. In addition, each model contains a delta function describing the effective inductance seen by the converter output in the decoupled portion of the DC bus. If (3.6-5) is small, as it should be to ensure the decoupling capacitors placed

in the circuit are actually decreasing the effective inductance of the commutation loop, this term can be ignored as well. This leaves the resonance term described by the sinusoidal portion of each response. Comparing the ratio of the resonance terms in each model, a surface plot such as the one shown in Fig 3-10. To do so, one must first define another ratio, ε_L, describing the ratio of L_{dec} to L_{Bus} (3.6-8). To ensure that Model B is a good approximation of the DC bus structure, the system should fall in the dark blue region of the plot Here, one can see that ε_C should remain less than 0.05 (C_{bulk} is 20 times greater than C_{dec}). At these values of ε_c, the model is relatively insensitive to ε_L up to even 0.5. At such an extreme the parasitic inductance of the decoupling capacitor is already half that of the bus inductance being decoupled and the effectiveness of this decoupling on removing the influence of L_{bus} has decreased by 33% as described by (3.6-5). Moving forward in this section, it will be assumed that a converter has been designed so that Model B is an acceptable approximation for the DC bus structure. Further, assuming that L_{dec} is negligible compared to L_{bus}, L_{dec} will be disregarded for the sake of simplicity as its impact on capacitor overshoot voltage is small compared to that of L_{bus}.

$$\frac{V_A(s)}{I(s)} = \frac{kL_{bus}\left(s^2 + \omega_{dec}^2\right)\left(s^2 + \omega_{Bus}^2\right)}{\left(s^2 + \omega_{n\text{-}B}^2\right)} \tag{3.6-1}$$

$$\frac{V_B(s)}{I(s)} = \frac{kL_{bus}\left(s^2 + \omega_{dec}^2\right)}{\left(s^2 + \omega_{n\text{-}B}^2\right)} \tag{3.6-2}$$

$$\omega_{Bus} = \sqrt{\frac{1}{C_{bulk}L_{bus}}} \tag{3.6-3}$$

$$\omega_{dec} = \sqrt{\frac{1}{C_{dec}L_{dec}}} \tag{3.6-4}$$

$$k = \frac{L_{dec}}{L_{Bus} + L_{dec}} \tag{3.6-5}$$

$$\Delta V_A(t) = kL_{bus}I_{Load}\left(\frac{\omega_{n\text{-}A}^2\omega_{Bus}^2 + \omega_{n\text{-}A}^2\omega_{dec}^2 - \omega_{Bus}^2\omega_{dec}^2 - \omega_{n\text{-}A}^4}{\omega_{n\text{-}A}^3}\right)\sin\left(\omega_{n\text{-}A}t\right) + \left(\frac{I_{Load}}{C_{dec} + C_{bulk}}\right)t + kL_{bus}I_{Load}\delta(t) \tag{3.6-6}$$

$$\Delta V_B(t) = kL_{bus}I_{Load}\left(\frac{\omega_{dec}^2 - \omega_{n\text{-}B}^2}{\omega_{n\text{-}B}}\right)\sin\left(\omega_{n\text{-}B}t\right) + kL_{bus}I_{Load}\delta(t) \tag{3.6-7}$$

$$\varepsilon_L = \frac{L_{dec}}{L_{bus}} \tag{3.6-8}$$

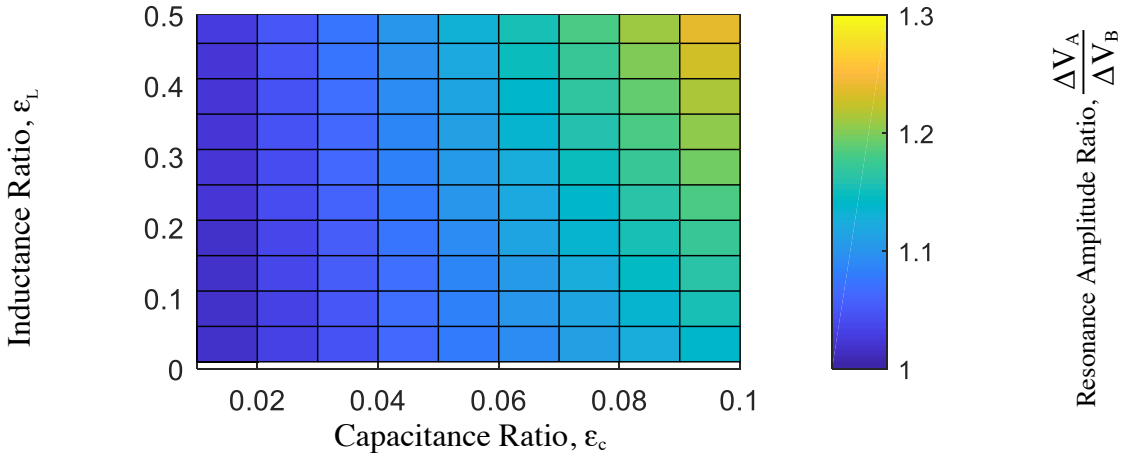


Figure 3-11: Resonance amplitude ratio between Models A and B as a function of ε_c and ε_L.

With the exclusion of C_{bulk} and L_{dec} from the decoupling capacitor model, one is left with the same circuit model as was used in sections 3.4 and 3.5. Here, L_p is replaced with L_{bus} and C_{OSS} is replaced with C_{dec}. These means that the same analytical models for overshoot can be used to (3.4-1) through (3.4-10) can be used, after making the appropriate parameter substitutions. An additional analytical model can be included, that uses a step response approximation of the turn-off transient, as has been done by previous researchers. This model is expressed in (3.6-9) and (3.6-10). To better facilitate comparison of these analytical models, the IGBT simulation model used previously is once again employed with the decoupling capacitance placed across the entire commutation loop inductance introduced by the DC Bus. This would represent the best-possible case for performing decoupling. The impact of any remaining parasitic inductance can be modeled using (3.6-1).

$$\Delta V_{dec}(t) = I_{Load}\sqrt{\frac{L_{Bus}}{C_{dec}}}\sin(\omega_n t) \tag{3.6-9}$$

$$\omega_n = \sqrt{\frac{1}{C_{dec}L_{Bus}}} \tag{3.6-10}$$

Examples of these simulated decoupling capacitor voltage waveforms are given in Fig 3-10. As expected, increasing the decoupling capacitance will lead to a decrease in voltage overshoot together with a decrease in the resonant frequency observed. These simulated results for varied C_{dec} can be compared to results obtained by utilizing the proposed analytical models. A summary of these peak voltage overshoot values is given in Fig 3-11. In this plot a pair of trends can be observed. First, increasing C_{dec} will of course decrease peak overshoot values. However, the return on decreasing overshoot with increasing C_{dec} diminishes as C_{dec} grows ever larger. This agrees with trends identified in Section 1.1-4. additionally, for small values of C_{dec}, there is noticeable deviation between the various analytical models. The ramp and step input models significantly overestimate voltage overshoot. exponential input model remains closer to the simulated results, but does begin to underestimate slightly for small values of C_{dec}. However, all models converge once C_{dec} is sufficiently large.

The reason for this is tied to the ratio of the resonance period ($2\pi/\omega_n$) to τ_{off}. As this ratio shrinks, the step approximation is the first to suffer inaccuracy, as its assumption of an infinitely fast turn-off time with respect to ω_n breaks down. The ramp model soon follows suit as the impact of the IGBT's tail current on slowing down the end of the turn-off transient is not captured. The exponential model remains the closest to simulated results as it does better capture the tail current effects. However, as the resonance period approaches that of τ_{off}, it begins to underestimate overshoot. The relative performance of these estimates can be altered by redefining τ_{off} for each model. However, for the sake of a straight forward comparison τ_{off} was left defined by the peak di/dt value as described in Section 3.2. These relative modeling errors are also directly responsible for the relative modeling errors in MOSFET turn-off seen in Section 3.4 and 3.5. Here the ratio of resonance period to τ_{off} was roughly 1.3.

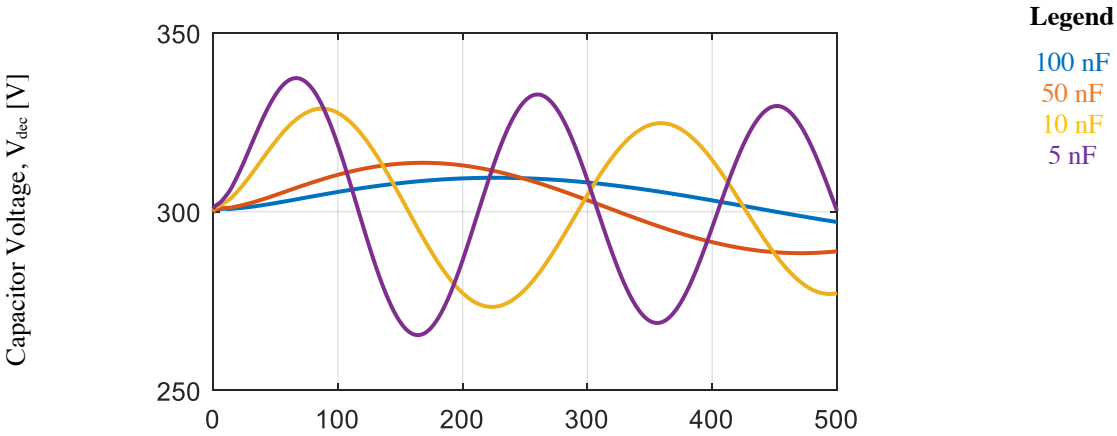


Figure 3-12: Simulated decoupling capacitor voltage waveforms placed in the simulated single-phase IGBT example circuit used in Section 3.4.

Recalling the proposed rule that C_{dec} should be at least 20 times larger than C_{OSS}, it suggests that C_{dec} should be at least 2 [nF] for the IGBT circuit to ensure that resonances are sufficiently separated. However, from a peak voltage overshoot perspective, one can determine a different approximation of minimum decoupling capacitance using the analytical models. Taking the worst-case overshoot estimate provided by the step response model, its magnitude can be compared to the voltage overshoot that would occur assuming no decoupling capacitor was used (i.e. the purely inductive commutation loop model). This leads to the ratio given in (3.6-11). If this expression is set equal to 1 and one solves for the value of C_{dec} that achieves this unity ratio, (3.6-12) is obtained. This provides an estimate of the minimum decoupling capacitance needed to ensure that the voltage stress seen at the point of decoupling is no greater than what would be seen without any decoupling at all. This value is indicated with the vertical dashed line in Fig 3-13 and indicates the point where the step response model intersects with the purely inductive model.

So, an additional decoupling capacitor sizing rule is obtained that can be used in conjunction with the resonance separation rules proposed by previous researchers. This is of course a conservative estimate for two reasons. First, the step response model will overestimate overshoot. Second, the inductive commutation loop model underestimates overshoot. For this IGBT example case $C_{dec\text{-}min}$ is roughly 100 times greater than C_{OSS}. This actually corresponds well with the most conservative sizing estimates proposed by previous researchers. However, this estimate is tied to

L_{bus}, τ_{off} and voltage stress reduction-rather than C_{OSS} and resonance separation-so the correlation between these sizing estimates are not tied to each other by any underlying physical properties.

$$\frac{\Delta V_{dec\text{-}Peak}}{\Delta V_{L\text{-}Peak}} = \frac{\tau_{off}}{\sqrt{C_{dec} L_{Bus}}} \tag{3.6-11}$$

$$C_{dec\text{-}min} = \frac{\tau_{off}^2}{L_{Bus}} \tag{3.6-12}$$

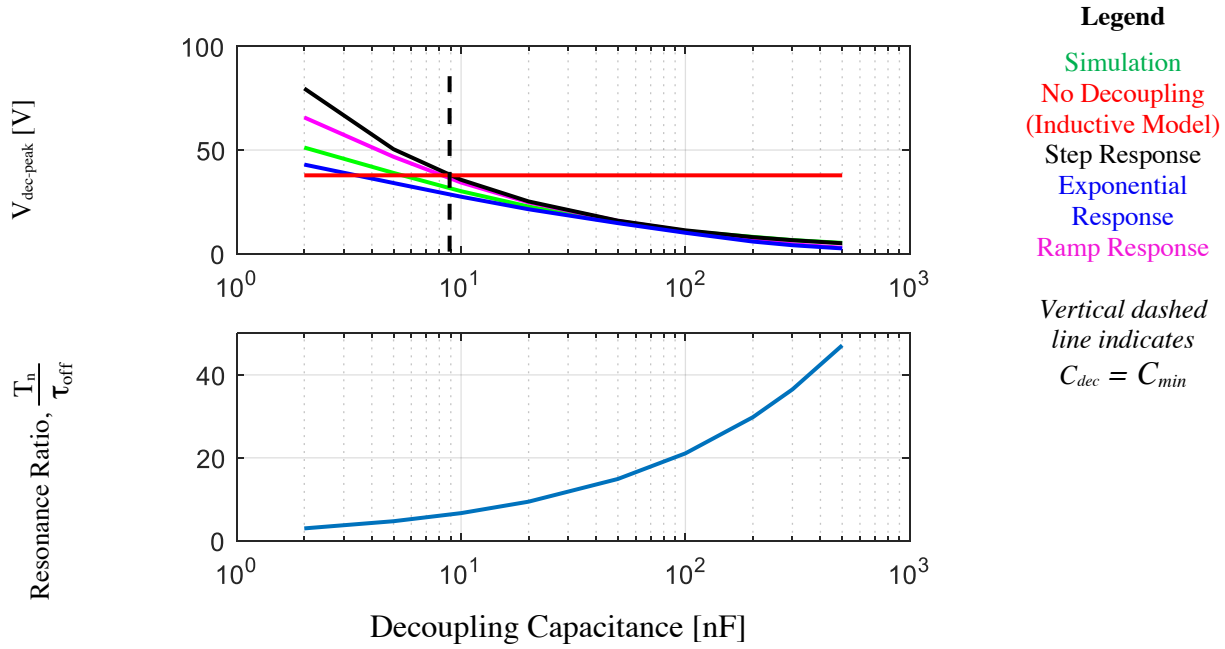


Figure 3-13: Analytical estimates of peak voltage overshoot seen at the decoupling capacitor compared to simulated results for different values of C_{dec} (top) as well as the ratio of the modeled resonance period to τ_{off}.

Staying with the most conservative overshoot estimate provided by the step response model, it can easily be expanded to simultaneous switching to observe how this more severe switching transient case may impact decoupling capacitor sizing. Once again, the same circuit simplification technique used in Section 3.5. That is, the effective inductance increases by a factor of $(1 + R_{cc})$. Plugging in this effective inductance yields a time-domain response given by (3.6-11). Taking the ratio of this new resonance amplitude to that of the single-phase decoupling case gives (3.6-12). This indicates that, at the extreme case where R_{cc} equals 1, voltage overshoot seen at decoupling capacitor will increase by 40%. Framing this another way, if one desired to keep capacitor

overshoot voltage constant going from a single-phase transient to that of a two-phase simultaneous switching transient, decoupling capacitance would need to increase by 40% at the most extreme case of R_{cc}.

$$\Delta V_{dec\text{-}simult}(t) = I_{Load}\sqrt{\frac{(1+R_{CC})L_{Bus}}{C_{dec}}}\sin(\omega_n t) \tag{3.6-11}$$

$$\frac{\Delta V_{dec\text{-}simult\text{-}Peak}}{\Delta V_{dec\text{-}Peak}} = \sqrt{1+R_{CC}} \tag{3.6-12}$$

$$\frac{\Delta V_{dec\text{-}simult\text{-}Peak}}{\Delta V_{L\text{-}single\text{-}Peak}} < 1 \tag{3.6-13}$$

$$C_{dec\text{-}min\text{-}simult} = \frac{\tau_{off}^2}{L_{Bus}}\sqrt{1+R_{CC}} \tag{3.6-14}$$

In summary, simultaneous events will degrade the effectiveness of decoupling capacitors in minimizing voltage stresses compared to a single-phase transient case. However, this effect scales with the square root of R_{cc} rather than being directly proportional to R_{cc}. Never-the-less, these impacts should be considered.

3.7 Per-Unit Switching Transient Analysis for Comparing Parasitic Inductance Requirements at Different Switching Speeds and Power Levels in Voltage Source Converters

To more clearly identify the trade-offs inherent in switching speed on parasitic inductance and voltage margin requirements in general-and simultaneous switching more specifically-across the broad range of converter power levels and available switching devices, it is useful to develop a per-unit analysis approach that normalizes the analysis across the board. The idea behind this is similar to the per-unit analysis applied to electric machine analysis in that it facilitates these comparisons. While electric machine per-unit analysis is built upon rated machine parameters provided by motor manufacturers, the per-unit analysis presented here will be developed from a converter design standpoint, where base parameters are defined by the targeted rated operating conditions and desired switching speed. This is then applied to the simple inductive commutation loop model to identify how per-unit voltage margin scales with per-unit inductance.

For the purpose of this analysis, a minimum of two base parameters are needed. First, one can begin by defining a base voltage, V_{base}. A useful value to use here is simply the desired peak DC Bus voltage (3.7-1). Next, one must obtain a base value for the peak rate-of-change in current experienced by the commutation loop, dI_{base}/dt (3.7-2). This can be defined one of two ways: defining it directly from a desired maximum di/dt (as was done in Section 3.2), or by defining a base current, I_{base}, and a base time t_{base}. If the later approach is used, I_{base} and t_{base} can be defined by the desired peak load current and a desired turn-off transient time. Regardless of the method chosen, the end result will be approximately the same. Finally, using V_{base} and dI_{base}/dt, a base value of inductance, $L_{base,}$ is defined (3.7-4). The per-unit value of any of the relevant physical quantities is then given by (3.7-5).

$$V_{base} = V_{DC\text{-}peak} \tag{3.7-1}$$

$$\frac{dI_{base}}{dt} = \frac{dI_{peak}}{dt} \tag{3.7-2}$$

$$\frac{dI_{base}}{dt} = \frac{I_{base}}{t_{base}} = \frac{I_{peak}}{t_{off}} \tag{3.7-3}$$

$$L_{base} = V_{base} \div \frac{dI_{base}}{dt} \tag{3.7-4}$$

$$X_{PU} = \frac{X_{physical}}{X_{base}} \tag{3.7-5}$$

This set of base parameters could be applied to any of the overshoot models presented previously. However, due to its relative simplicity and close agreement to other models in estimating the impact of simultaneous switching, the inductive model of voltage overshoot will be used here. As such the per-unit overshoot is given by (3.7-6). For the case when dI_{PU}/dt and $V_{DC\text{-}PU}$ equal 1, the peak voltage stress experienced by a switching device during a single phase and two-phase simultaneous switching transient are given by (3.7-7) and (3.7-8), respectively. These expressions provide estimates of the minimum required voltage margin needed to ensure a device's maximum blocking voltage is not exceeded during a transient.

$$\Delta V_{PU} = L_{PU} \frac{dI_{PU}}{dt} \quad (3.7\text{-}6)$$

$$V_{Peak\text{-}PU} = 1 + L_{PU} \quad (3.7\text{-}7)$$

$$V_{Peak\text{-}simult\text{-}PU} = 1 + (1+R_{cc})L_{PU} \quad (3.7\text{-}8)$$

To give this analysis a grounding in realistic parameter values, Table 3.5 provides a summary of di/dt estimates obtained from manufacturer datasheets. Here, di/dt values are estimated by dividing the rated current value by the reported t_{fall} time which is derived from double-pulse tests carried out by individual manufacturers. These di/dt values are not necessarily precise estimations of peak di/dt that would be generated in an actual converter circuit as this will depend on the specific gate drive design and operating conditions of a specific design.

Table 3.5: Summary of di/dt estimates for a variety of Si IGBTs and SiC MOSFETs from different suppliers and for different rated voltage and current levels estimated from reported t_{fall} values.

Si IGBTs					**SiC MOSFETs**				
Supplier	**Product**	**Voltage [V]**	**Current [A]**	**di/dt [A/ns]**	**Supplier**	**Product**	**Voltage [V]**	**Current [A]**	**di/dt [A/ns]**
Infineon	IKW40N60H3	600	40	2	Cree	C3M0065090D	900	36	3.6
Infineon	IKW40N120H3	1200	40	2.5	Cree	C2M0080120D	1200	36	2.4
Infineon	IKW75N60H3	600	75	2.7	Cree	C2M0080170D	1700	36	2
Infineon	IKY75N120CH3	1200	75	2.3	Cree	C3M0021120D	1200	100	4
Semikron	25NEB066T	600	30	0.66	Rohm	SCT3080AR	650	30	2.5
Semikron	100GD066T	600	100	1.1	Rohm	SCT3080KLHR	1200	30	1.6
Mitsubishi	CM100MXUB	650	100	0.167	Rohm	SCT3022ALHR	650	90	2.6
Mitsubishi	CM100MXUC	1200	100	0.25	Rohm	SCT3022KLHR	1200	90	3.2

Using this example range of di/dt values, a range of base inductance values can be generated across the design space of low voltage drives. This is shown in Fig 3-14. To better understand this space, a couple of example points are provided. Point 1 provides an example of a fairly low peak di/dt value of 0.5 [A/ns] that may be typical in IGBT-based drives currently in use today combined

with a bus voltage of 400 [V] which falls in the middle range of bus voltages used in electric vehicle architectures and in low voltage industrial drives. This yields a base inductance value of 800 [nH]. Holding DC bus voltage constant and increasing the switching speed by a factor of four, this base inductance decreases by a factor of four (point 2).

If this is plot is extended with an eye on the industry trend of pushing devices to ever faster switching speeds, points 3 and 4 indicate how low these base inductance values fall as peak di/dt is pushed to 10 [A/ns]. This produces base inductance ranges between 10 and 100 [nH] as bus voltage ranges from 100 to 1000 [V].

On the whole, one can understand this base inductance value to indicate the amount of parasitic inductance that can be tolerated while holding peak voltage overshoot (as a percent of the DC bus voltage) constant. As base inductance decreases, allowable parasitic inductance decreases proportionally.

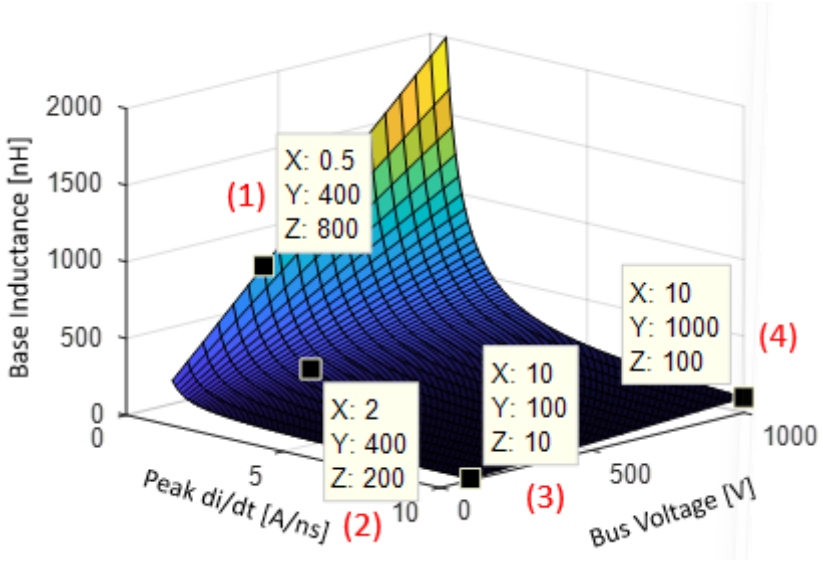


Figure 3-14: Base inductance (z-axis) as a function of peak di/dt (x-axis) and bus voltage (y-axis).

Recalling equation (3.7-7), one must examine per-unit inductance to understand the impact on per-unit peak voltage stress and therefore voltage margin requirements during a switching transient. Taking the parasitic inductance ranges provided in Section 1.1.6 (5-50 [nH]), the range of base inductances provided by Fig. 3-14 can be used to convert this range of physical inductances to per-unit quantities. This is given in Fig 3-15.

Fig 3.15 once again includes a collection of example points to provide some context. Points A and B indicate how per-unit inductance changes for the relatively high base inductance value (Fig 3-14: Point 1, 800 [nH]) of a converter one might find on the market today. If one manages to push the limits of parasitic inductance minimization in this application (Fig 3-15: Point A: 5 [nH]), per-unit inductance is only 0.625%. Increasing parasitic inductance to the high-end of the range provided in 1.1.6, per-unit inductance is still only 6.25% (Fig 3-15: Point B, 50 [nH]). This suggests that, with conventional design techniques that don't require special layout techniques, voltage overshoot should not exceed 6.25% of the bus voltage. For added precaution, one can factor in that the inductive model was shown to underestimate measured overshoot by 30-40%, this overshoot estimation increases up to 8.75%.

Taking Point 2 from Fig 3.14, where switching speed has been increased by a factor of 4, and using a middling parasitic inductance value of 20 [nH], per-unit inductance increases to 10%. This can be shifted up to 14% if one considers the underestimate provided by the inductive commutation loop model.

Finally, if one takes the extreme example from Fig 3.14, where peak di/dt increases to 10 [A/ns] in point 3 and combine it with very good parasitic inductance design of 5 [nH], per unit inductance increases to 50%

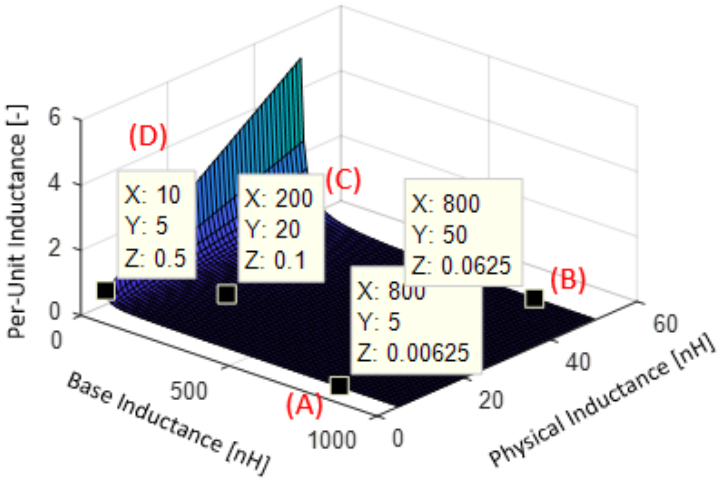


Figure 3-15: Per-unit inductance (z-axis) as a function of base inductance (x-axis) and physical inductance (y-axis).

What this design space mapping highlights is that the bare minimum voltage margin requirements, without even including design safety factors, will rapidly increase as engineers push switching devices to ever faster speeds. In addition, these estimated margin requirements will increase by a factor of roughly $(1 + R_{cc})$ for a two-phase simultaneous switching case.

Considering the benefits of simultaneous switching avoidance, the improvement in voltage margin will be highly dependent on the per-unit inductance of a particular converter and its inductive coupling ratio, R_{cc}. For the relatively mundane example given by point B in Fig 3-15, simultaneous switching avoidance will, at best ($R_{cc} = 2$), improve voltage margin by roughly 9%. For a 400 [V] system with a peak di/dt of 0.5 [A/ns] and 50 [nH], this reduces peak voltage stresses from approximately 472 [V] to 436 [V]. This will certainly have the benefit of modestly reducing switching losses or slightly increasing the peak bus voltage in a variable-bus system, but it will come at the cost of increased control architecture complexity.

However, as switching speeds increase, the benefit of simultaneous switching avoidance will become greater. When per-unit inductance is on the order of 20 or 30%, the option to implement simultaneous switching avoidance may provide cost reduction benefits by eliminating the need to move to switching devices with a higher voltage rating.

Power devices available on the market are provided at discrete intervals of maximum blocking voltages. These vary by supplier and device type, but commonly available voltage ratings are 600 [V], 650 [V], 700 [V], 900 [V], and 1200 [V] for low voltage drives. A reduction in peak overshoot of 10% the DC bus voltage could begin to provide the benefit of reducing the required voltage blocking capability. Table 3.6 gives an example cost comparison for Si-IGBT and SiC MOSFETs from different suppliers at different voltage ratings.

Taking an example from one of Infineon's IGBT product families that provide roughly 400 [A] current capability, the impact of simply moving from a 650 [V] device to a 705 [V] device is an increase in cost of 18%. Moving from a 705 [V] device to a 1200 [V] device leads to a 50%

increase in cost. Similar cost jumps can be seen from other suppliers and for SiC MOSFETs as well.

Table 3.6: Cost comparison of power devices with similar current ratings at different voltage blocking capabilities within a given manufacturer's product families for Si IGBTs and SiC MOSFETs. Prices were obtained from 3rd party distributor websites (Digikey, Mouser)

Si IGBTs					**SiC MOSFETs**				
Supplier	**Product**	**Voltage [V]**	**Current [A]**	**Cost [$]**	**Supplier**	**Product**	**Voltage [V]**	**Current [A]**	**Cost [$]**
Infineon	FS400R07A1E3S7BOMA1	650	400	340	Cree	C3M0030090K	900	63	28
Infineon	FS380R12A6T4BBPSA1	705	400	400	Cree	C30021120K	1200	63	37
Infineon	FS380R12A6T4BBPSA1	1200	380	600	Rohm	SCT3030AR	650	70	32
Semikron	28AC066V1	600	100	66	Rohm	SCT3030KLGC11	1200	72	56
Semikron	38AC12T4V1	1200	100	89	-	-	-	-	-

3.8 Summary

The simplified modeling approaches presented here provide a way to obtain rough estimates of peak voltage overshoot for a particular target application at the beginning of the design process, before significant design decisions have been made. While these methods do not provide precise estimates, due to their simplistic representation of the nonlinear dynamics at play, the do provide a reasonable bound on the peak voltage overshoot that can be expected.

Applying these simple models to the case of a two-phase simultaneous switching event, the impact of coupled commutation loop inductance, as expressed by R_{cc}, can be found. In general, peak overshoot will increase linearly with R_{cc}, However, the impact of unmodeled changes in effective commutation loop inductance on peak di/dt must also be considered when using these models.

Extending this same modeling approach to decoupling capacitor sizing, the impact of simultaneous switching on required decoupling capacitance can also be estimated. Here,

mathematical modeling and simulation indicate the decoupling capacitance needed to hold peak voltage overshoot constant increases with the square root of R_{cc}.

Finally, using the proposed per-unit analysis method, the impact of simultaneous switching avoidance on power converter design requirements can be compared across a broad range of switching speeds and parasitic inductance values. Here, the benefit of simultaneous switching avoidance in conventional drives operating in the range of 0.1 to 2 [A/ns] is relatively small, as long as it meets a relatively simple standard of keeping parasitic inductance at or below the 50 [nH] range. However, as the industry pushes to faster switching speeds approaching the 5 to 10 [A/ns] range, simultaneous switching may begin to provide the opportunity of either increasing the maximum DC bus voltage or eliminating the need to move to switching devices with higher blocking potential. These do provide the design benefits of increasing system performance or decreasing system cost, respectively.

Chapter 4 Probability of Simultaneous Switching Occurrence in Three-Phase Inverter Systems

The impact of simultaneous switching in power converters has been shown in both the literature review as well as through experimental evaluation performed for this thesis. However, there has been no evaluation of how common it is for simultaneous switching to occur during normal operation of a three-phase inverter. Clearly, if this is an event that never-or almost never-occurs, then performing simultaneous switching avoidance may not be worth the trouble to implement. Having said that, if even one occurrence of simultaneous switching-under adequate load current conditions-will damage a device, then any non-zero probability will be sufficient cause to implement simultaneous switching avoidance algorithms. This analysis shows that, for any non-zero value of T_{sep}, there will be a non-zero probability of simultaneous switching occurring. Moreover, this probability increases as T_{sep} increases.

It is worth mentioning that more detailed and application specific probability maps can be generated for specific applications where specific operating condition distributions are well known. However, this analysis is done assuming that all steady-state operating conditions in the inverter's linear range are equally likely. In addition, V_{dc} and T_{pwm} have been normalized to 1 to further simply the results.

4.1 Defining Simultaneous Switching Probability

There are several ways one could define the "probability" of simultaneous switching occurring. The simplest would be to say, if one picks a command vector on the voltage hexagon at random, what is the probability that it will cause overlapping switching transients. While this is maybe the most general possible definition and is explored briefly here, it doesn't correlate well to how an inverter is used in actual operation.

In this work, probability is primarily evaluated as a function of steady-state operating conditions. That is, for a given $|V_{qd}|$ and ω_e, what is the probability that a simultaneous switching event will occur? Now, this could be analyzed across a fixed time period or a fixed electrical angular rotation. Since doing so for a fixed time period will inherently make probability a function of ω_e, it was chosen to analyze simultaneous switching probability across one electrical cycle. Having said that, to reduce numerical effects, such as non-integer ratios of switching-to-fundamental frequencies, all simulations were performed for 20 complete electrical cycles.

4.2 Intra-Inverter Simultaneous Switching Probability

The evaluation of intra-inverter simultaneous switching probability was carried out in three steps. First, the effect of T_{sep} on the areas of the inverter hexagon that will cause simultaneous switching was evaluated. This corresponds directly evaluating simultaneous switching probability by choosing command vectors at random. Next, an arc-length-based method is used, where probability of evaluated based on the arc lengths of a circle corresponding to constant $|V_{qd}|$ that fall in regions of simultaneous switching are compared to the total circle circumference. This allows one to remove the effects of discrete command vector sampling from the analysis. Finally, these results are compared to a direct simulation of the three-phase inverter system under steady-state operating conditions. Here, all analysis is carried out assuming that SVPWM is used, where T_0 equals T_7.

4.2.1 Inverter Hexagon Area Ratios

As presented in Chapter 1, regions of simultaneous switching can be directly mapped onto the inverter hexagon, as a function of T_{sep}. This is shown in Fig. 4-1 for one sector of the inverter hexagon. Taking the random-command-vector definition of probability, one simply needs to calculate the ratio of areas where simultaneous switching will and will not occur. The equations for this are given in (4.2-1) through (4.2-3). (4.2-2) is plotted in Fig 4-2.

In addition, Fig 4.1 and (4.2-4) define what is labeled the “intra-phase overlap limit”. This corresponds to the case when the zero state dwell times become small enough that, as defined by

T_{sep}, the inverter phases corresponding to minimum and maximum will have switching transients that overlap within a single phase. Not only is this not really a concern for simultaneous switching – as there is no di/dt coupling that can occur when only one phase is involved – but it also corresponds to a minimum pulsewidth limitation; where dwell times that are too short can cause damage due to prolonged, incomplete switching transients. This has not yet been parsed out and should be done in future work.

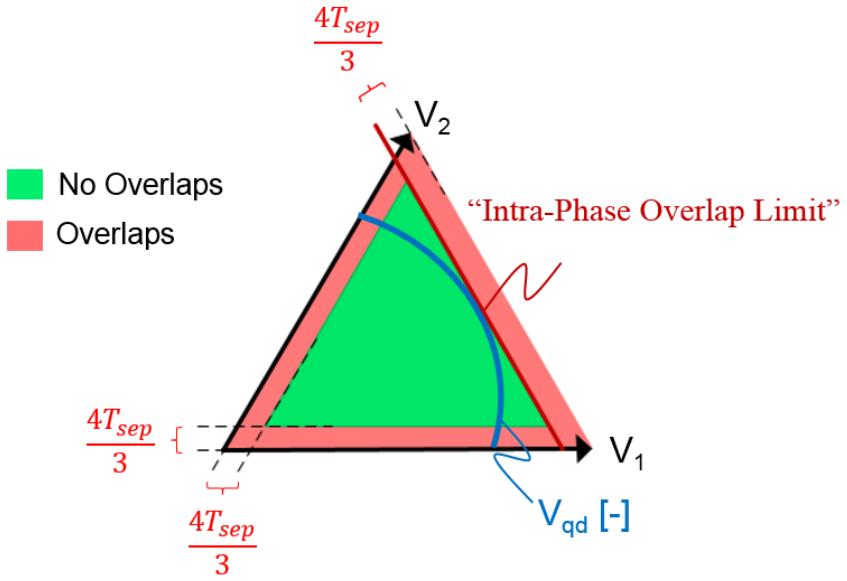


Figure 4-1: Mapping regions of simultaneous switching (overlaps) onto one sector of the inverter hexagon

$$\text{Sector Area} = \frac{\sqrt{3}}{9} \tag{4.2-1}$$

$$\text{Available Area} = \frac{\sqrt{3}(1-6T_{sep})^2}{9} \tag{4.2-2}$$

$$\text{Randomized Overlap Probability} = 1 - (1-6T_{sep})^2 \tag{4.2-3}$$

$$\text{Intra-Phase Overlap Limit} = \frac{\sqrt{3}(1-2T_{sep})}{3} \tag{4.2-4}$$

Using (4.2-3) and Fig. 4-2, the probability of a random voltage command vector causing switching overlaps for the motor drive testbench used in later chapters (where T_{sep} must equal roughly 2% to ensure proper switching separation) the probability of switching transient overlaps is roughly 6%. That is, the ratio of unavailable-to-total-hexagon-area is roughly 6%.

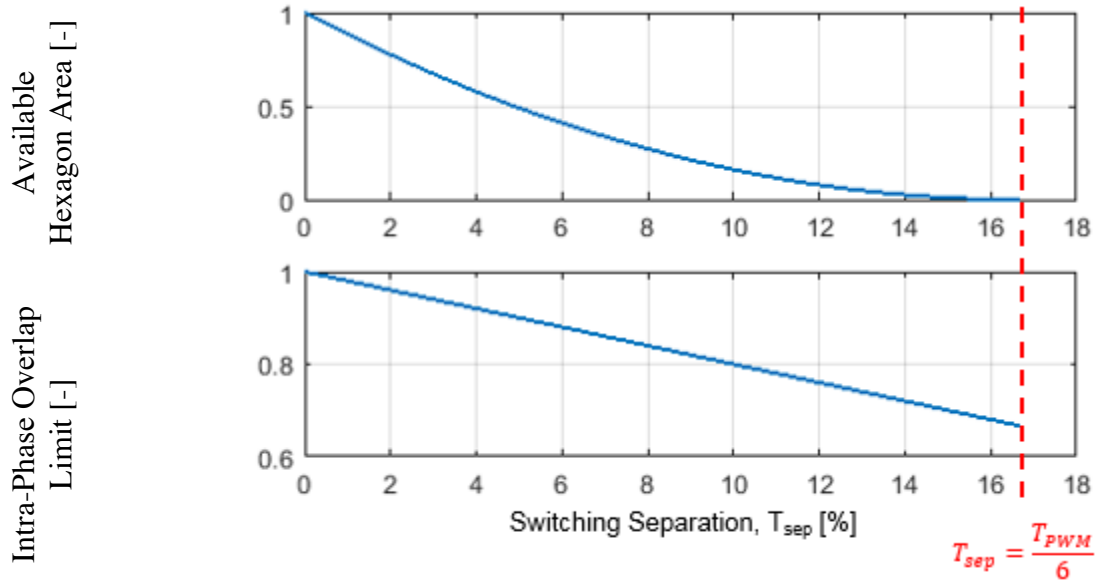


Figure 4-2: Available hexagon area that will not cause simultaneous switching (top) and the voltage command magnitude that will begin to cause intra-phase switching transient overlaps as defined by T_{sep} (bottom).

4.2.2 Arc Length Method

One approach to determining intra-inverter simultaneous switching based on steady-state operating conditions is to use an arc-length-based approach. To do this one can simply compare the arc lengths of a constant $|V_{qd}|$ command circle that cross regions of simultaneous switching on the voltage hexagon. This inherently removes any effect of ω_e and f_{pwm} on the analysis. The result of this analysis is shown in Figure 4-3 for all $|V_{qd}|$ that fall within an inverter's linear range using SVPWM.

Fig. 4-3 shows that, for any non-zero value of T_{sep}, the probability of simultaneous switching is non-zero. This is somewhat difficult to discern for T_{sep} values near zero, but the probability contours never reach zero. Taking an example where T_{sep} equals 2%, there is a 100% probability

that switching overlaps will occur when $|V_{qd}|$ is less than 0.1 [-]. This is because there is a region near the voltage hexagon origin where active-vector dwell times are to small to exceed the T_{sep} requirement. Increasing $|V_{qd}|$ out of this region causes the overlap probability to decrease. But, again, it never goes to zero, because the command must still cross regions of simultaneous switching at hexagon boundaries. As $|V_{qd}|$ approaches 1, the command begins to cause intra-phase overlaps causing the probability to increase again. As T_{sep} increases, these regions of high overlap probability increase until there is no longer any usable operating space left.

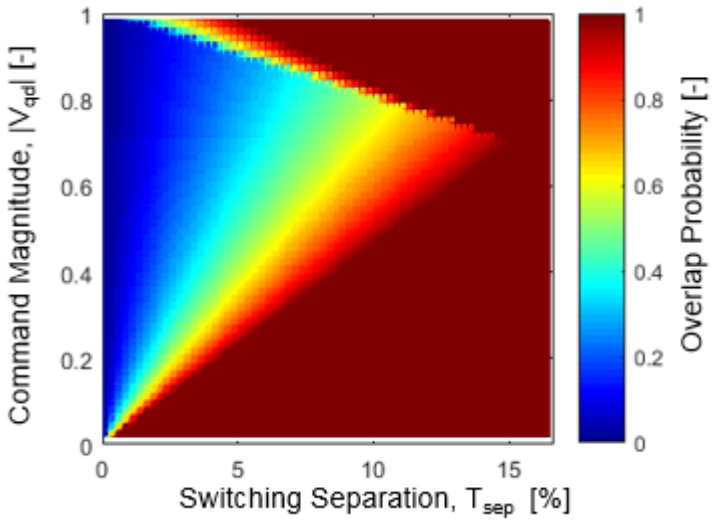


Figure 4-3: Calculated intra-inverter simultaneous switching probability for a three-phase inverter as a function of command magnitude and switching separation.

These results can be summarized as solely a function of T_{sep} by summing probability values for each value of T_{sep} and then divided by the number of $|V_{qd}|$ values used in the analysis. This is shown in Fig 3-4. Once again, for any non-zero value of T_{sep}, there is as non-zero value of switching overlap probability. Using the 2% separation example, intra-inverter overlaps will occur roughly 30% of the time under steady-state operation (Assuming all $|V_{qd}|$ values are equally likely).

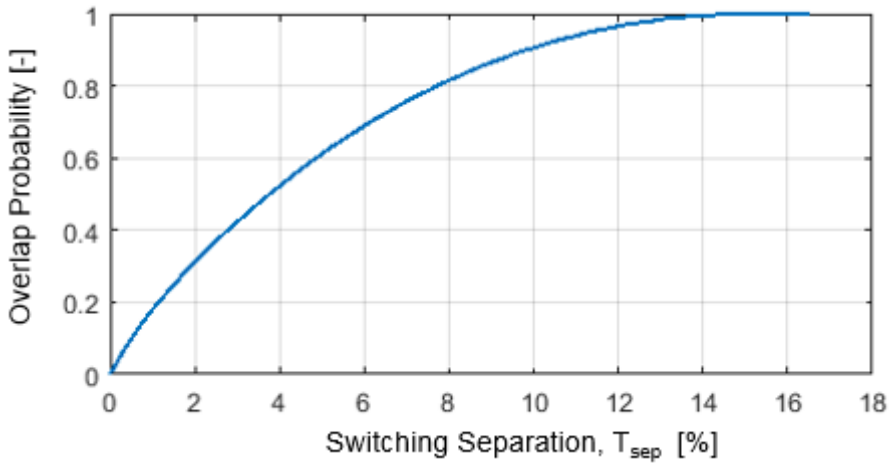


Figure 4-4: Average switching overlap probability as a function of T_{sep} assuming all values of $|V_{qd}|$ are equally likely.

4.2.3 Simulation-Based Intra-Inverter Simultaneous Switching Probability

A second approach to determining intra-inverter simultaneous switching probability is throught direct simulation of the system. A block diagram for this type of simulation is shown in Fig 4-5. Here, simulation may a be misnomer, as no system states are being integrated. Rather, a steady-state, rotating command vector is sampled and SVPWM is applied to produce switching instances. Using these switching instances, switching overlap occurance can be determined using the T_{sep} constraint. These simulation were carried out for 20 complete electrical cycles for each value of ω_e tested. To determine the overlap probability, the number of overlap occurances are divided by the number of PWM switching cycles included in each simulation.

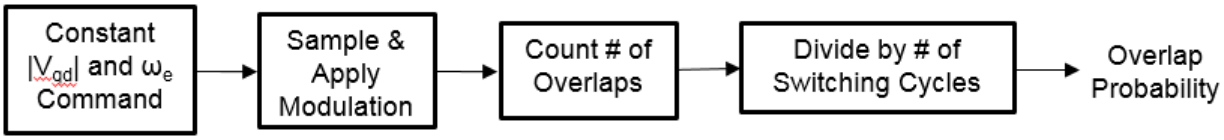


Figure 4-5: Block diagram of the simulation model used to determine intra-inverter switching overlap probability under steady-state operation.

Using this approach, Fig 4-6 shows that overlap probability is not a function of ω_e. This makes sense as, while the number of switching cycles in on fundamental period decreases at higher ω_e, so does the number of switching cycles that fall in a region of simultaneous switching. In addition, Fig 4-6 includes a plot where ω_e is held constant and T_{sep} is varied. Here, a result similar to Fig 4-3 using the arc length method is obtained.

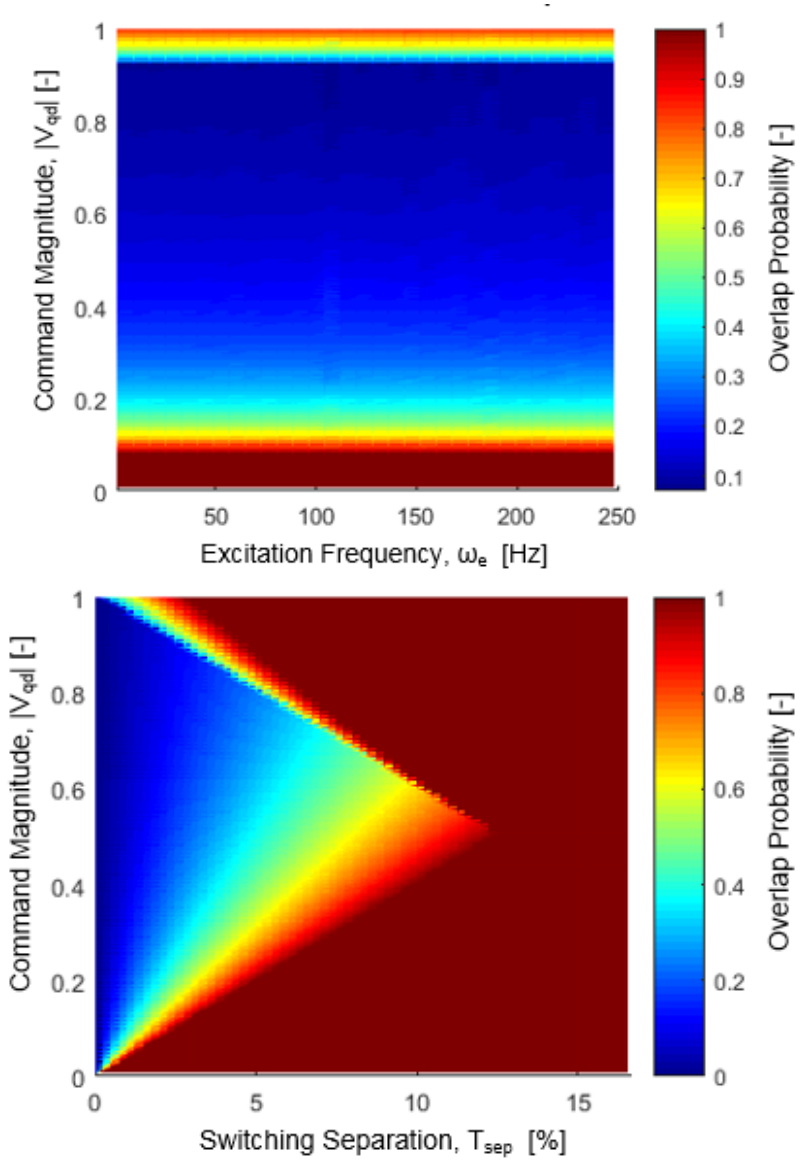


Figure 4-6: Simulation based intra-inverter switching overlap probability as a function of $|V_{qd}|$ and ω_e (top), and as a function of $|V_{qd}|$ and T_{sep} (bottom).

Taking a similar approach as before, and averaging the simulated overlap probability for each value of T_{sep}, the simulation-based and arc-length-based methods can be compared as shown in Fig 4-7. Here, the two results agree quite well, particularly for low values of T_{sep} where numerical simulation effects have less impact. Once again, at 2% separation, the probability of simultaneous switching occuring is roughly 30% under steady-state conditions.

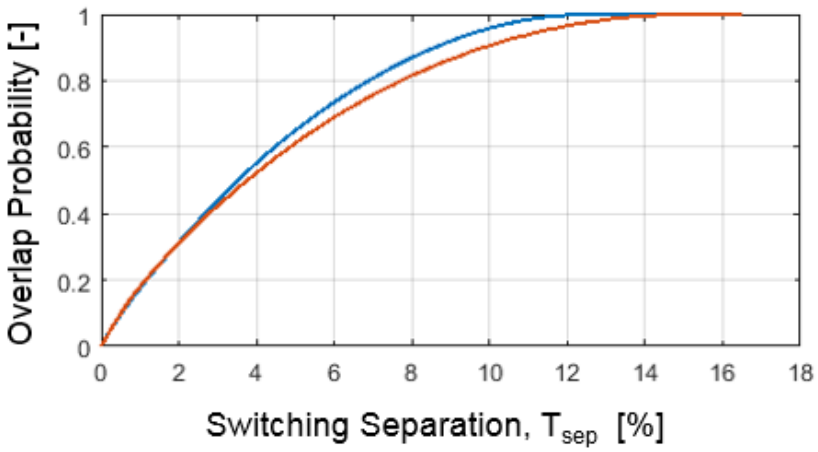


Figure 4-7: Comparison of average switching overlap probability from the arc-length and simulation methods, assuming all $|V_{qd}|$ values are equally likely.

From this analysis it is clearly shown that the probability of unwanted simultaneous switching events will be non-zero under steady-state conditions within a three-phase inverter. For a practical value of 2% separation, the probability is roughly 30%. While it is possible to come up with an arbitrary command trajectory that always skips over regions of simultaneous switching, this is not at all applicable to practical applications. This shows that simultaneous switching is indeed necessary if one wishes to operate switching devices near voltage limits where unwanted commutation coupling could cause overvoltage failures.

4.3 Inter-Inverter Simultaneous Switching Probability

Move to the inter-inverter simultaneous switching problem, a two, three-phase inverter system was analyzed using a similar simulation-based approach. This is shown in Fig 4-8. To isolate inter-inverter switching overlaps, intra-inverter overlaps in either inverter are ignored and only overlaps between two inverters are detected.

In this analysis, $|V_{qd}|$, ω_e, and T_{sep} are once again variables of concern. In addition, because zero-sequence-voltage, or zero-state-partitioning, does influence the relative switching instant timing between two three-phase inverters, it is useful to include this in the analysis in some way. Here, this was done by evaluating inter-inverter simultaneous switching probability for two cases: using sinusoidal PWM (SPWM) and Space-Vector PWM (SVPWM). In both cases, the two inverters use identical modulation schemes.

Because of the number of variables included in this analysis problem have been doubled, simulations were performed in iterations where Inverter 1's parameters ($|V_{qd\text{-}1}|$ and $\omega_{e\text{-}1}$) were held constant while sweeping $|V_{qd\text{-}2}|$ and $\omega_{e\text{-}2}$. Also, a constant value of T_{sep} was used, based on the 2% separation threshold needed in the experimental motor drive test setup used in Chapter 6.

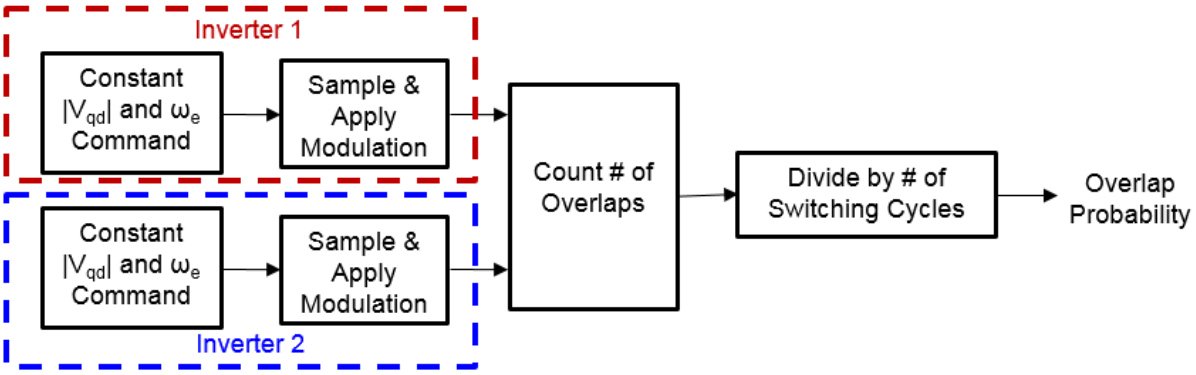


Figure 4-8: Block diagram of the simulation model used to determine inter-inverter simultaneous switching events for a two, three-phase inverter system.

To give the reader a clear example of what is happening in each iteration of this simulation, example time-domain waveforms are shown in Fig 4-9. Here, anytime there is an intersection between the voltage commands of Inverter 1 and Inverter 2, an inter-inverter switching overlap will occur.

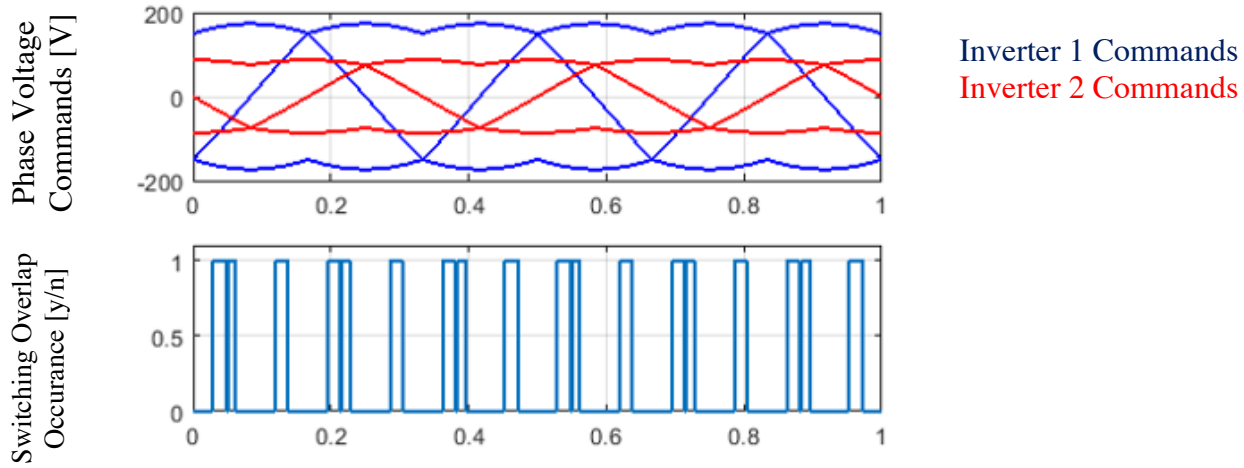


Figure 4-9: Time domain waveforms for one iteration of the inter-inverter overlap probability simulation shown voltage command waveforms (top) and binary (1 or 0 = yes or no) overlap conditions (bottom).

Fig 4-10 shows a side-by-side comparison of inter-inverter switching overlap probability for the SVPWM and SPWM test cases. This was iterated for four different values of $|V_{qd\text{-}1}|$, corresponding to the 4 rows of contour plots, while $\omega_{e\text{-}1}$ remained at 50 [hz] in each case.

By sweeping $|V_{qd\text{-}2}|$ and $\omega_{e\text{-}1}$ in each case, two interesting trends are revealed. First, inter-inverter simultaneous switching probability is not a function of ω_e for the cases tested. This is further explained later in this section. Also, the switching overlap probability distribution is noticeable different for the SVPWM and SPWM cases.

SVPWM produces high overlap probabilities when the two inverters' $|V_{qd}|$ values are similar. When they are the same, the inter-inverter overlap probability approaches 100%. This quickly falls to 20-30% as the two command magnitudes separate. However, using SPWM, the probability map is more distributed. While probability doesn't reach as high of peaks, it remains at or above 50% across a wide region of $|V_{qd\text{-}2}|$ values.

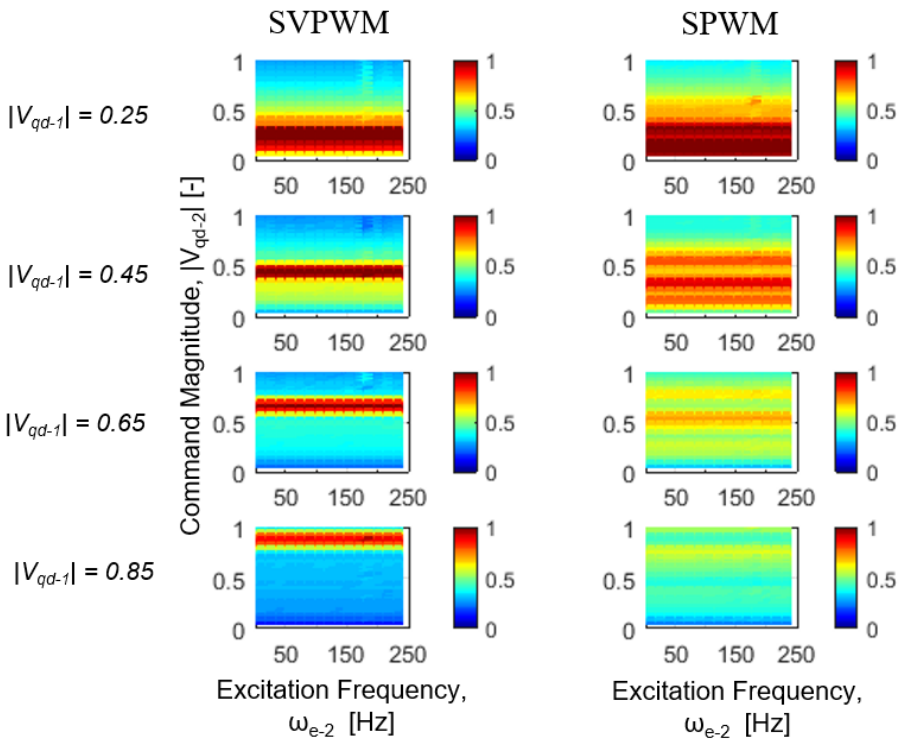


Figure 4-10: Inter-inverter simultaneous switching overlap probability contours for different command voltage magnitudes and electrical frequencies using SVPWM (left column) and SPWM (right column). Here $\omega_{e\text{-}1}$ is held constant at 50 [Hz]. f_{pwm} = 5000 [Hz]

Most importantly of all, in the context of this entire research work, is the fact that the inter-inverter overlap probability never goes to zero. This means that, assuming steady-state operating conditions, one cannot say that simultaneous switching will never occur between two inverters. Thus, if this switching case could damage power devices, it must be addressed and avoided by properly formed simultaneous switching avoidance algorithms.

Showing this in a different way, the average overlap probability was found for each probability contour in Fig 4-10 and is plotted in Fig 4-11. This shows that SPWM produces a higher overlap probability when $|V_{qd\text{-}1}|$ is small. However, these two converge as $|V_{qd\text{-}1}|$ increases.

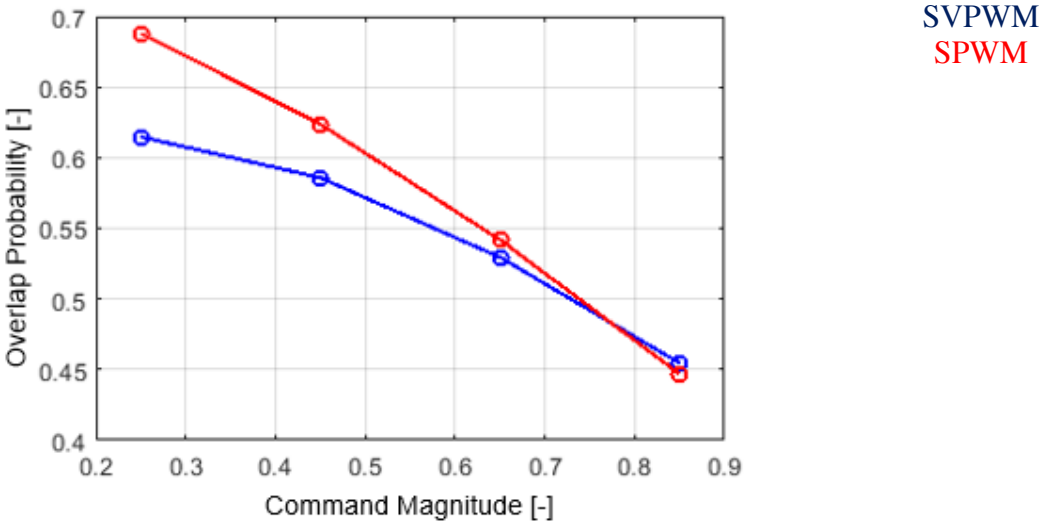


Figure 4-11: Comparison of average inter-inverter switching overlap probability for the SVPWM and SPWM modulation strategies as a function of command magnitude using a T_{sep} value of 2%. $\omega_{e\text{-}1}$ = 50 [Hz], f_{pwm} = 5000 [Hz]

The reason for the distinct difference in probability distribution for SVPWM and SPWM can be immediately identified by looking at time-domain phase voltage commands for each scheme, shown in Fig 4-12. Because SVPWM causes the maximum and minimum phase voltage commands to be equal and opposite, when $|V_{qd\text{-}1}|$ and $|V_{qd\text{-}2}|$ approach one another, these equal and opposite phase voltages are overlapping nearly continuously – as a function of the phase difference between the two command vectors. SPWM does not share this feature. Moreover, the phase voltages cross a wider range of voltages. This leads to a wider distribution of high overlap probability albeit with a lower peak value.

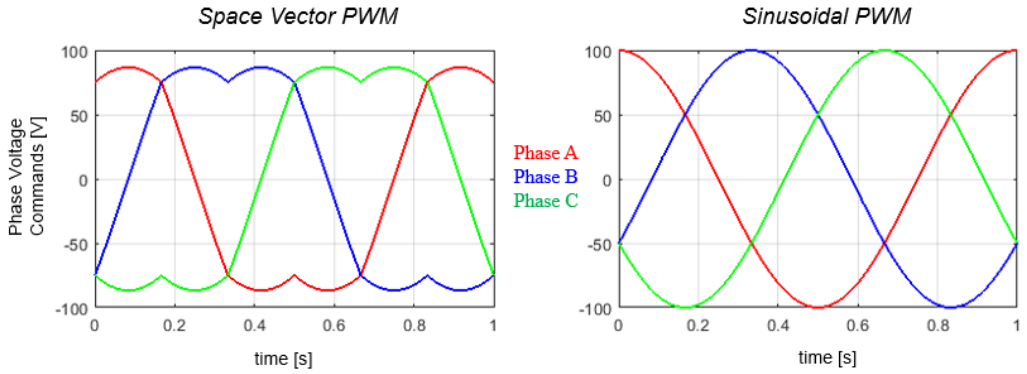


Figure 4-12: Comparison of time-domain phase voltage waveforms using the SVPWM (left) and SPWM (right) modulation schemes.

The reason there is no ω_e dependence in inter-inverter overlap probability is because there is 120° symmetries in the probability distribution when holding $\omega_{e\text{-}1}$ and $\omega_{e\text{-}2}$ constant and varying $\phi_{e\text{-}2}$ instead. This is shown in Fig 4-13. So, when averaged across a sufficient number of electrical cycles, probability differences due to phase differences caused by unequal $\omega_{e\text{-}1}$ and $\omega_{e\text{-}2}$ will be averaged out and the result is a probability distribution that is not a function of ω_e.

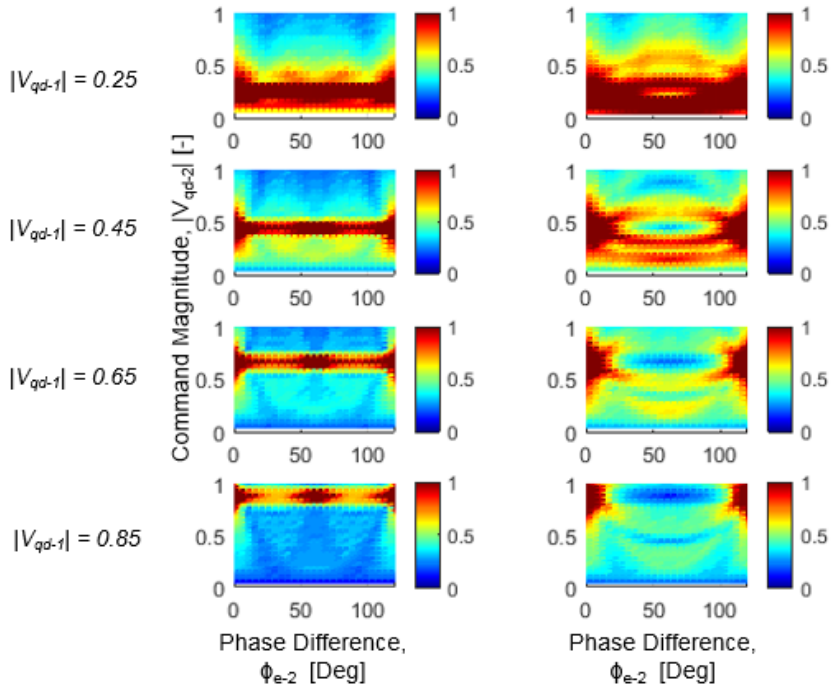


Figure 4-13: Inter-inverter simultaneous switching overlap probability contours for different command voltage magnitudes and phase differences using SVPWM (left column) and SPWM (right column). Here $\omega_{e\text{-}1}$ and $\omega_{e\text{-}2}$ are held constant at 50 [Hz]. f_{pwm} = 5000 [Hz] .

4.4 Summary

In this chapter the probability of simultaneous switching occurring was evaluated for the intra and inter-inverter cases assuming steady-state operating conditions. For the intra-inverter case, this was done using geometric and simulative analyses, while simulation was used exclusively for the inter-inverter case.

Using this analysis, it was shown that the probability of simultaneous switching never goes to zero for a non-zero value of T_{sep}. Using the 2% separation threshold example taken from the test setup used in Chapter 6, this produces an intra-inverter switching overlap probability of roughly 30%, assuming all steady-state operating conditions are equally likely. For the inter-inverter case, depending upon the modulation scheme used and the relative $|V_{qd}|$ magnitudes for each inverter, this can be anywhere from 40% to 70%. It is worth noting that not all of these overlaps may be damaging to devices, as it is dependent upon load current magnitude and polarity. But the chances that switching overlaps will occur is certainly high enough that it cannot be ignored.

Chapter 5 Error Vector Intra-Inverter SSA Algorithms

In this chapter, an alternative approach to APWM-SSA is developed for performing intra-inverter SSA. This is done through the introduction of an error voltage in the inverter's output to move the command vector out of a region of simultaneous switching. Using this approach, some limitations of APWM-SSA can be eliminated and harmonic content caused by SSA can be improved. However, this approach requires modification of the controller structure to compensate for introduced voltage errors.

5.1 Development of Error-Vector SSA (EV-PWM)

The APWM-SSA method developed previously, being implemented in the PWM scheme and sourcing the commanded average voltage V_{qds}^{s*} across each switching period (Fig. 5-1), has no impact on closed-loop control of the motor drive. As such, it can be integrated into a motor drive control structure by changing the PWM algorithm and no changes to the motion or torque/current control loops (Fig. 5-2).

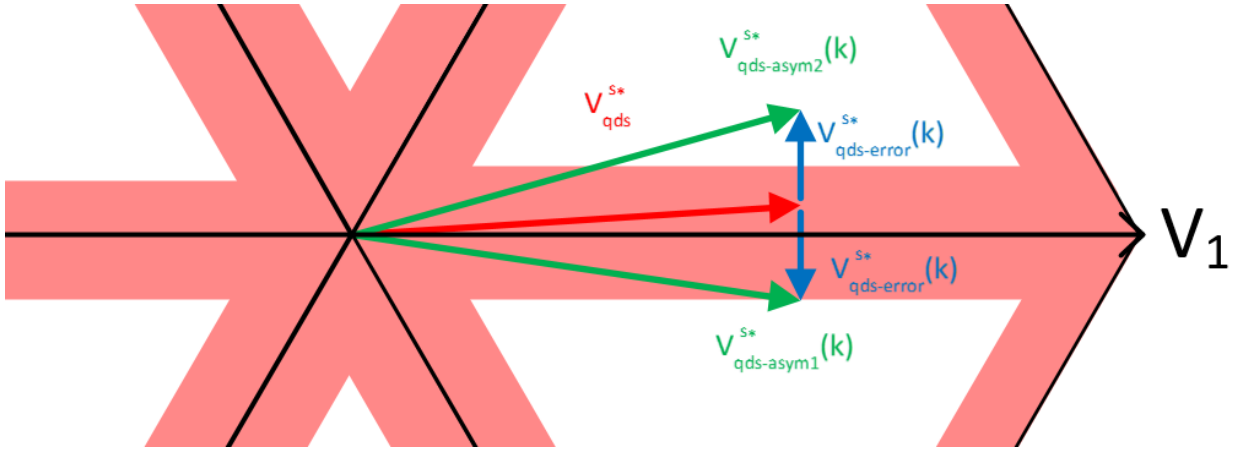


Figure 5-1: Diagram depicting output voltage vector selection for the APWM-SSA method.

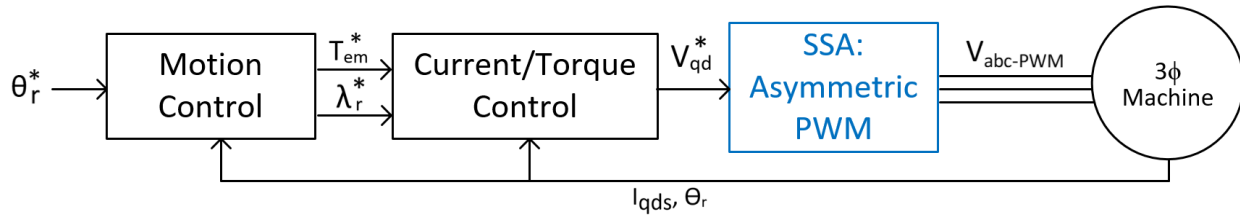


Figure 5-2: Simplified motor control structure showing the placement of APWM-SSA together with the pulsewidth modulation function of the controller.

Removing the restriction of maintaining V_{qds}^{s*}, SSA can be performed by selecting a new command $V_{qds\text{-}SSA}^{s*}$ that does not fall in a region of simultaneous switching. In doing so, an error, ΔV_{qds}^{s} will be introduced into the command (Fig. 5-3). Using this approach, the Error-Vector SSA (EV-SSA) algorithm is placed after the current/torque loop and can use SVPWM, as shown in Fig 5-4, or any other three-phase PWM method.

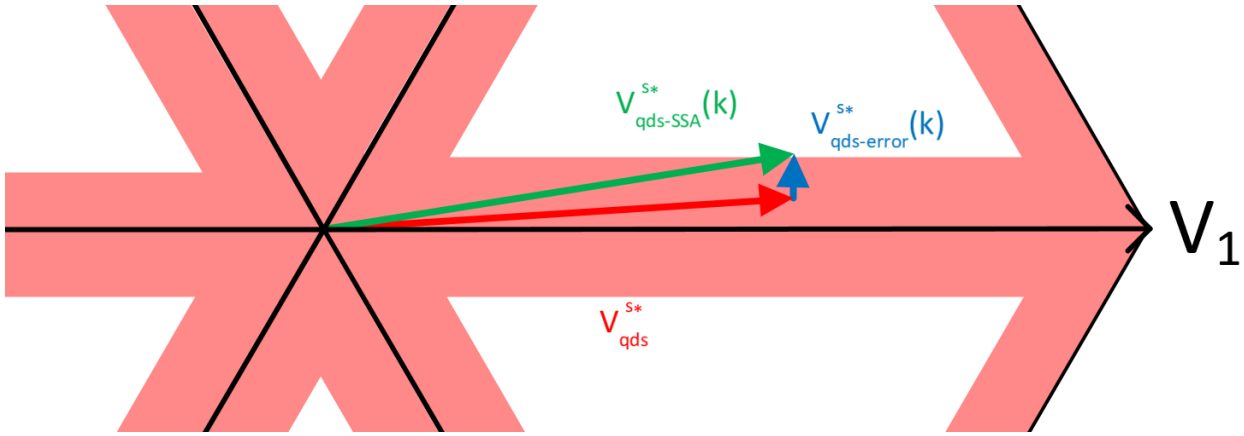


Figure 5-3: Diagram depicting output voltage vector selection for the EV-SSA method.

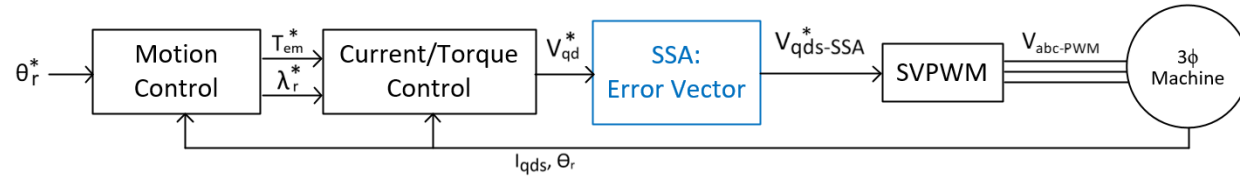


Figure 5-4: Simplified motor control structure showing the placement of EV-SSA after the current/torque control loop but prior to the PWM function.

Because EV-SSA introduces ΔV_{qds}^{s} into the inverter output, it is necessary to provide compensation in the control structure. If this is not done, ΔV_{qds}^{s} will appear as a disturbance to the

drive's control, causing unwanted interaction between current control and the SSA algorithm. So, the resulting current error, ΔI_{qds}^{s}, generated by ΔV_{qds}^{s} must be estimated and a compensation voltage, $\Delta V_{qds\text{-}null}^{s*}$, should be calculated and added to V_{qds}^{s*} in the next sample period.

Assuming the load is an AC machine with relatively slow (or no) rotor flux dynamics, and the current or torque control scheme compensates for back-emf voltage properly, superposition can be applied and ΔI_{qds}^{s} can be modeled separately using a simple resistive-inductive dq-frame model with ΔV_{qds}^{s} used as an input. The discrete-time model for this is shown in (5.1-1). $\Delta I_{qds}^{s}(k+1)$ (5.1-3) can then be subtracted from the measured current before using it in any current or torque control schemes in the next sampling period. To eliminate $\Delta I_{qds}^{s}(k+1)$ during the next sampling period, (5.1-3) can be re-arranged to solve for $\Delta I_{qds}^{s}(k+2)$. This can then be set equal to zero (5.1-4), and a $\Delta V_{qds\text{-}comp}^{s*}(k+1)$ can be calculated that will make $\Delta I_{qds}^{s}(k+2)$ zero (5.1-5).

$$\frac{\Delta I_{qds}^{s}}{\Delta V_{qds}^{s}} = \frac{[1-e^{(-T_s/\tau)}]z^{-1}}{R[1-e^{(-T_s/\tau)}z^{-1}]} \tag{5.1-1}$$

$$\tau = \frac{L_s}{R_s} \tag{5.1-2}$$

$$\Delta I_{qds}^{s}(k+1) = \frac{[1-e^{(-T_s/\tau)}]z^{-1}}{R[1-e^{(-T_s/\tau)}z^{-1}]}\,\Delta V_{qds}^{s}(k) \tag{5.1-3}$$

$$\Delta I_{qds}^{s}(k+2) = 0 = e^{(-T_s/\tau)}\Delta I_{qds}^{s}(k+1) + \frac{[1-e^{(-T_s/\tau)}]}{R}\,\Delta V_{qds\text{-}comp}^{s*}(k+1) \tag{5.1-4}$$

$$\Delta V_{qds\text{-}null}^{s*}(k+1) = -\frac{R\,e^{(-T_s/\tau)}}{[1-e^{(-T_s/\tau)}]}\,\Delta I_{qds}^{s}(k+1) \tag{5.1-5}$$

Putting this into block diagram form, Fig. 5-5 shows signal flow for the voltage error compensation scheme in detail. Fig 5-6 shows how this voltage error compensation should be combined with EV-SSA to provide open-loop compensation for induced current errors without interaction with other control loops.

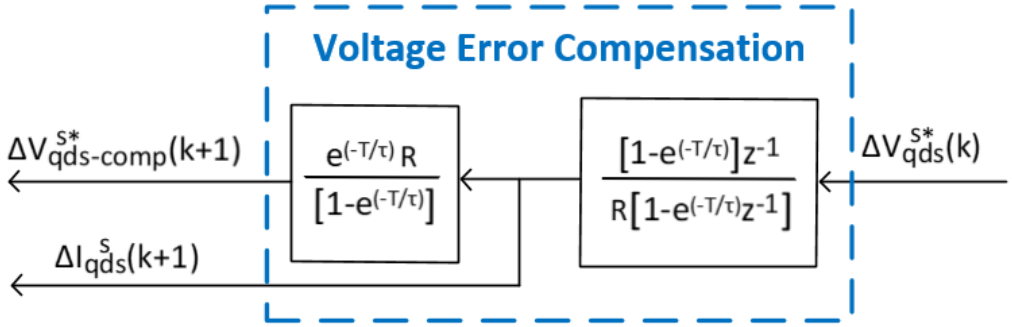


Figure 5-5: Discrete-time R-L models used in the Voltage Error Compensation scheme for estimating current error and generating a nulling voltage at the next sampling period.

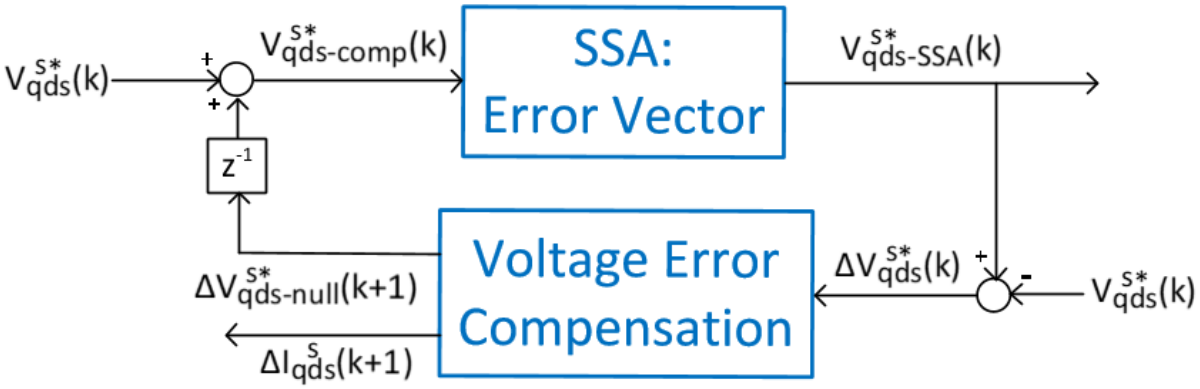


Figure 5-6: Integration of the EV-SSA approach together with voltage error compensation.

To more clearly understand how the EV-SSA method functions during normal operation, analyzing open-loop simulation results is most useful.

5.2 Open-Loop Operation of EV-SSA with Voltage Error Compensation

To demonstrate how the EV-SSA method operates in the ideal case, simulation results using an R-L load operating under constant volts-per-hertz were performed. A block-diagram model of the simulated system is shown in Fig 5-7. Fig. 5-8 shows the resulting output voltages, $V^{s*}_{qds\text{-}SSA}$, and currents, I^{s}_{qds}. Here, the impact of EV-SSA can be seen every 60 electrical degrees, where $V^{s*}_{qds\text{-}SSA}$ has a clear ripple component. This is oscillation is caused by the selected $V^{s*}_{qds\text{-}SSA}$ oscillating between limits of the simultaneous switching region in order to drive ΔI^{s}_{qds} to zero. This is more clearly shown in Fig. 5-9, where ΔV^{s}_{qds} and ΔI^{s}_{qds} are plotted.

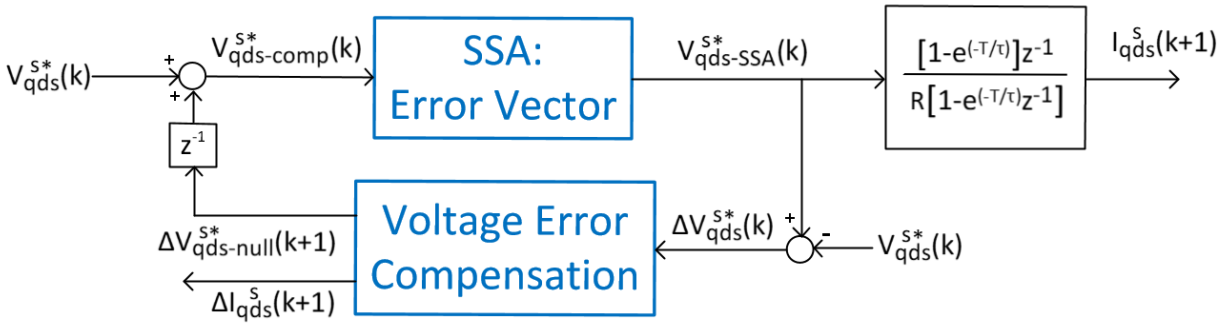


Figure 5-7: Open-loop simulation of EV-SSA using an R-L Load Model.

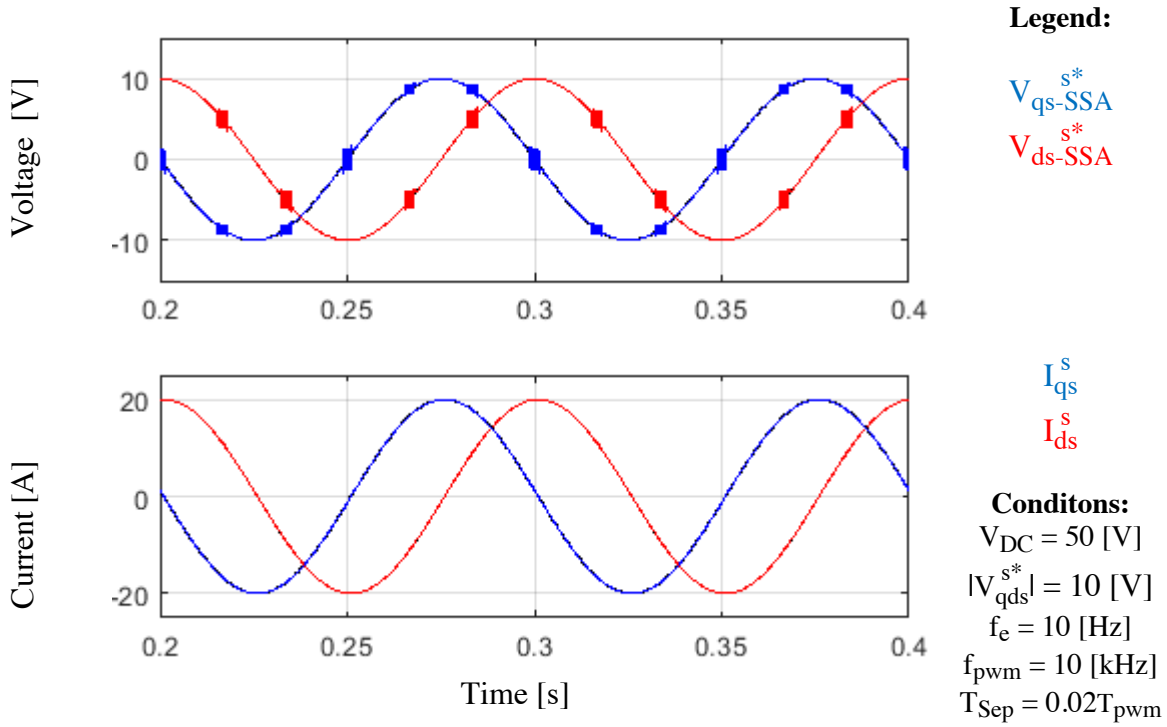


Figure 5-8: Stationary frame output voltages and currents during constant volts-per-hertz operation using the EV-SSA algorithm.

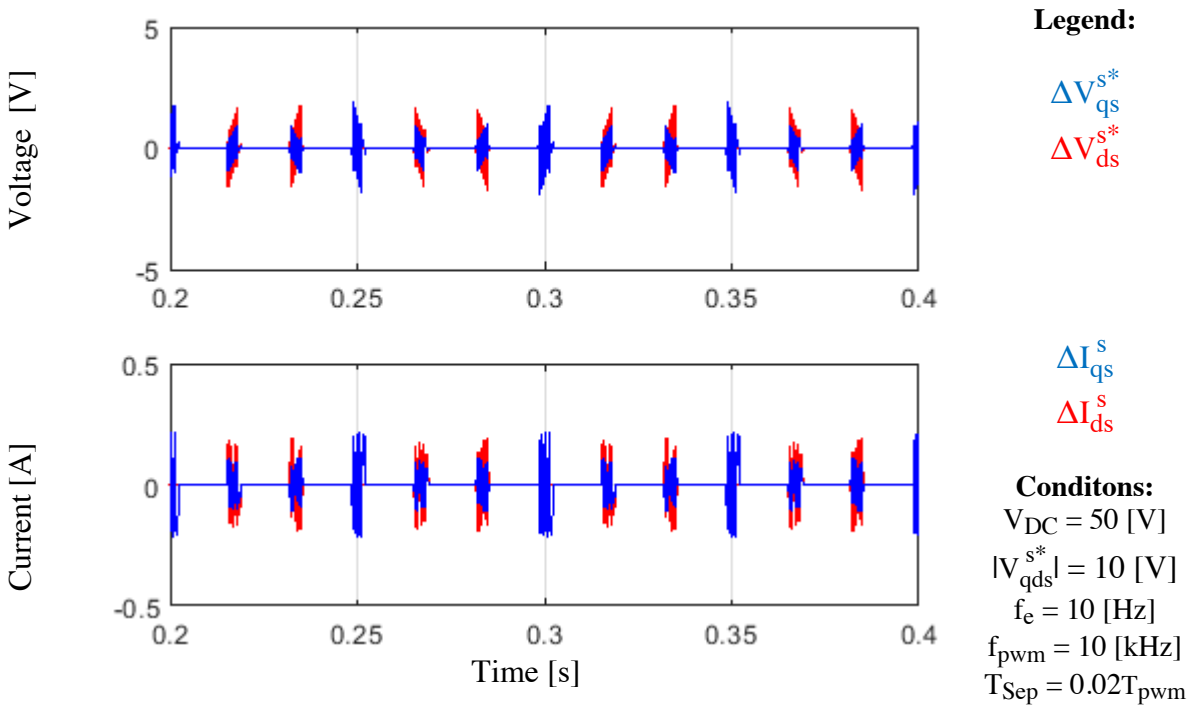


Figure 5-9: Stationary frame error voltages and error currents introduced by the EV-SSA algorithm during constant volts-per-hertz operation.

Fig. 5-10 shows a zoomed view of one region where EV-SSA is active. As V_{qds}^{s*} enters the region of simultaneous switching, a small, increasing voltage error is introduced in both the d and q-axes. The causes a proportional response in ΔI_{qds}^{s}. Once ΔI_{qds}^{s} gets large enough, $\Delta V_{qds\text{-}comp}^{s*}$ grows large enough to push $V_{qds\text{-}comp}^{s*}$ back into the previous inverter hexagon sector. This causes ΔI_{qds}^{s} to increase with opposing polarity. Once ΔI_{qds}^{s} gets large enough again, $V_{qds\text{-}comp}^{s*}$ gets pushed back to the neighboring hexagon sector and the process repeats. As V_{qds}^{s*} approaches the end of the simultaneous switching region it is currently in, $\Delta V_{qds\text{-}comp}^{s*}$ and ΔI_{qds}^{s} go to zero.

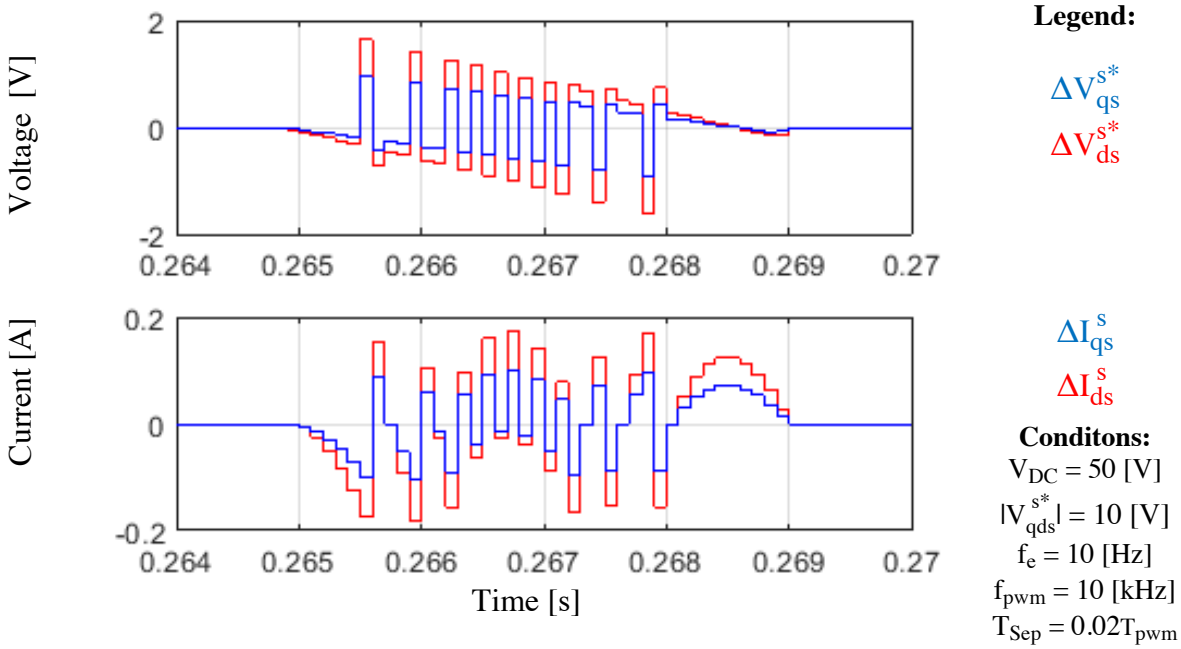


Figure 5-10: Zoomed view of error voltages and error currents introduced by the EV-SSA algorithm during constant volts-per-hertz operation.

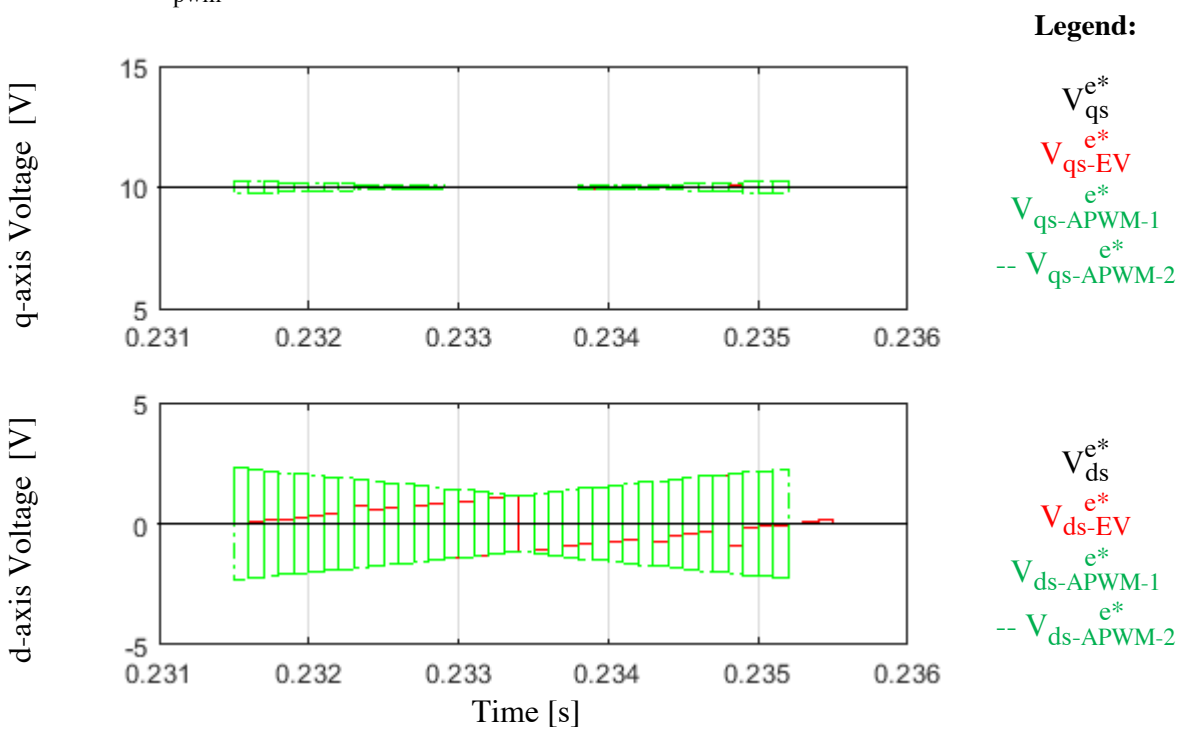
Having demonstrated how the EV-SSA operates using time-domain waveforms, it is useful to compare its performance to that of the APWM-SSA method.

5.3 Open-Loop Comparison of EV-SSA and APWM-SSA

Using the same volts-per-hertz excitation with an R-L load, simulations were performed using both EV-SSA and APWM-SSA, to compare their impact on current waveforms. Fig. 5-11 shows the output voltage waveforms compared with a case without any SSA. Waveforms are shown in the synchronous frame to eliminate the sinusoidal component for clarity. Clearly, the APWM-SSA method results in both a higher-frequency and higher-amplitude injection of harmonic content in the applied voltage.

Fig. 5-12 shows the resulting current waveforms from all three simulation cases with PWM switching harmonics included. Here, the impact of APWM-SSA versus EV-SSA on output current can be clearly seen. The APWM-SSA method produces current oscillations that repeat each switching period. However, at the end of each switching period, the current produced by APWM-SSA is the same as the case without any SSA. This confirms that no average voltage error is

introduced to the inverter output each switching period. On the other hand, the EV-SSA current waveforms slowly deviate away from those of the no SSA case.Once this devation is large enough, the $\Delta V_{qds\text{-}comp}^{s*}$ term causes the voltage command oscillating between boundaries of the simultaneous switching region. However, this oscillation, and the resulting current oscillations occur at half of f_{pwm}.

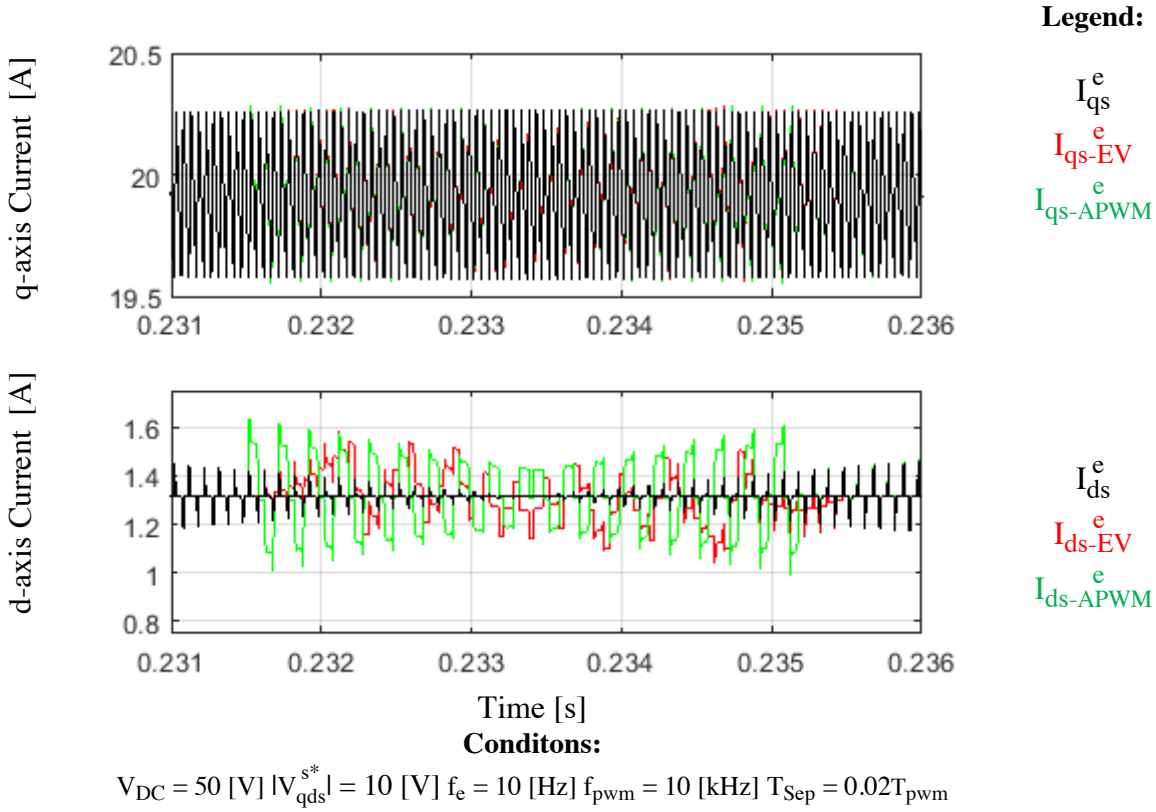


Conditons:

V_{DC} = 50 [V] $|V_{qds}^{s*}|$ = 10 [V] f_e = 10 [Hz] f_{pwm} = 10 [kHz] $T_{Sep} = 0.02T_{pwm}$

Figure 5-11: Synchronous frame q and d-axis voltages for the EV-SSA and APWM-SSA algorithms, compared with a case without any SSA.

Finally, the amplitude of the current deviation for EV-SSA approaches zero as V_{qds}^{s*} approaches the end of the simultaneous switching region, because the amount of necessary voltage error decreases. However, the PWM current ripple in the APWM-SSA approach increases in magnitude at the boundaries of the simultaneous switching region, due to its need to produce $V_{qds\text{-}APWM\text{-}1}^{*}$ and $V_{qds\text{-}APWM\text{-}2}^{*}$ that both fall outside of the simultaneous switching region while also averaging to V_{qds}^{s*}.

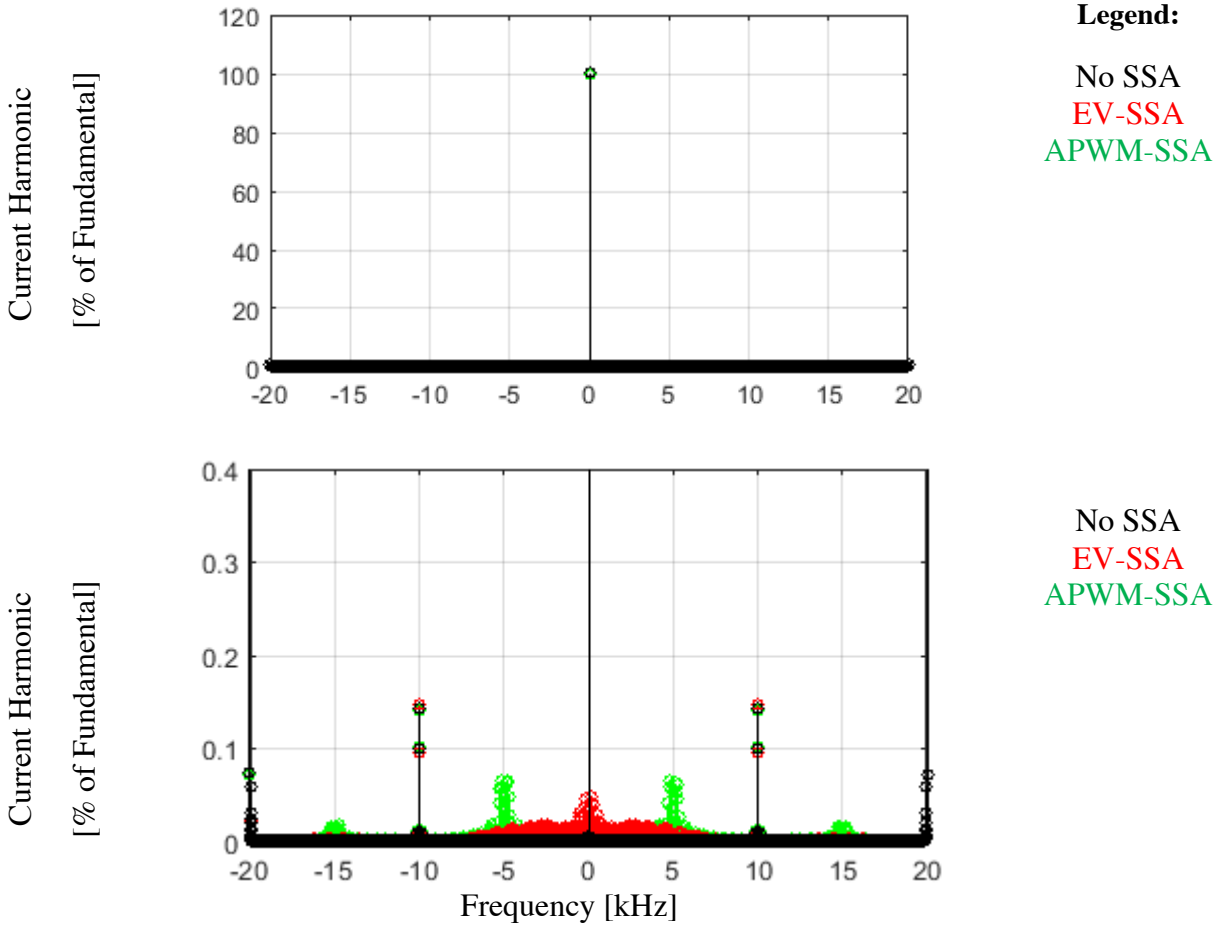


Conditons:

V_{DC} = 50 [V] $|V^{s*}_{qds}|$ = 10 [V] f_e = 10 [Hz] f_{pwm} = 10 [kHz] $T_{Sep} = 0.02T_{pwm}$

Figure 5-12: Synchronous frame q and d-axis currents for the EV-SSA and APWM-SSA algorithms, compared with a case without any SSA.

Performing FFT analysis on all three current waveforms, Fig. 5-13 compares the current harmonics produces in each case, where all harmonic components are normalized by the fundamental component magnitude. First, the un-zoomed plot shows that the fundamental current component produced by EV-SSA and APWM-SSA is nearly identical to the case without any SSA. Moving to the zoomed plot, the only significant current harmonics produced in the no SSA case are at integer multiples of f_{pwm}. For the APWM-SSA case, these are still present. However, new peaks in harmonic content are added at half-multiples of f_{pwm}. EV-SSA also maintains harmonic content peaks at switching frequency multiples. However, the additional harmonic content it produces is spread out across a range of frequencies between the zero and f_{pwm}.



Conditons:

$V_{DC} = 50$ [V] $|V_{qds}^{s*}| = 10$ [V] $f_e = 10$ [Hz] $f_{pwm} = 10$ [kHz] $T_{Sep} = 0.02T_{pwm}$

Figure 5-13: Synchronous frame q and d-axis current harmonics for the EV-SSA and APWM-SSA algorithms, compared with a case without any SSA.

Finally, Fig 5-14 depicts the percent change in current total harmonic distortion (THD), as defined in (5.3-2), caused by both SSA methods. This is done for a range of T_{Sep} values and at different excitation frequencies. In each case the volts-per-hertz ratio remained equal to 1 [-]. For both SSA methods THD increases exponentially as T_{Sep} increases. This is because the regions of the voltage hexagon where SSA is active increases. On the contrary THD decreases as f_e increases. This is because the number of sampling periods where V_{qds}^{s*} falls in a region of simultaneous switching decreases. Finally, for each case tested, EV-SSA produces slightly lower THD than APWM-SSA. This suggests that the induced ohmic losses in EV-SSA will be slightly lower than those caused by APWM-SSA.

$$\text{Change in THD} = \frac{\text{THD}_{SSA} - \text{THD}}{\text{THD}} \quad (4.3\text{-}1)$$

$$\text{THD} = \left[\sum |I^{e}_{qds}(n)|^2\right]^{1/2} \textit{ for } n = 1,2,3\ldots \quad (4.3\text{-}2)$$

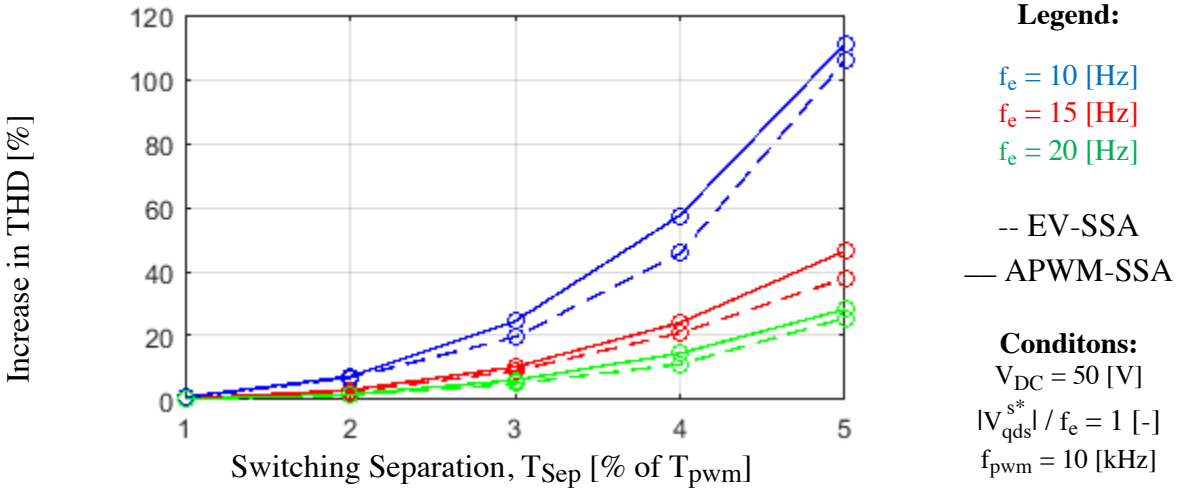


Figure 5-14: Synchronous frame q and d-axis current harmonics for the EV-SSA and APWM-SSA algorithms, compared with a case without any SSA.

As mentioned previously, EV-SSA is compatible with double-update control. So, it is beneficial to investigate how distortion caused by SSA can be further reduced using the increased controller update rate provided by double-update PWM.

5.4 EV-SSA Using True Double-Update Control

Using the same simulation and operating conditions, Fig 5-15 presents time-domain current waveforms for EV-SSA performed using single-update and double-update PWM compared to single-update operation without any SSA. Here, the key difference is that the magnitude of current ripple caused by EV-SSA is reduced by the increased controller sampling rate. In Fig 5-16, the harmonic specra comparison for the single-update and double-update cases shows that harmonic content is distributed across a wider range of frequencies with decreased amplitudes particularly at low frequencies.

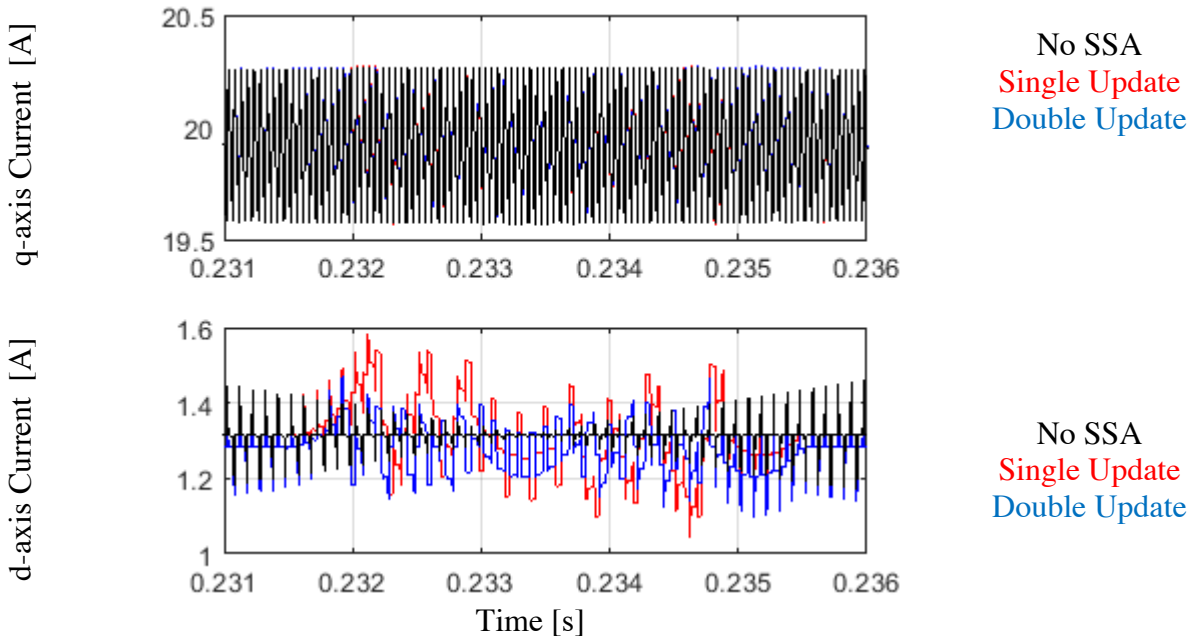


Figure 5-15: Synchronous frame q and d-axis currents for the EV-SSA algorithm with single-update and double-update control, compared with a case without any SSA.

Finally, the increase in THD caused by EV-SSA is significantly reduced for low f_e and T_{Sep} high. This reduction is present for all tested cases, but reduces as f_e and T_{Sep} increase.

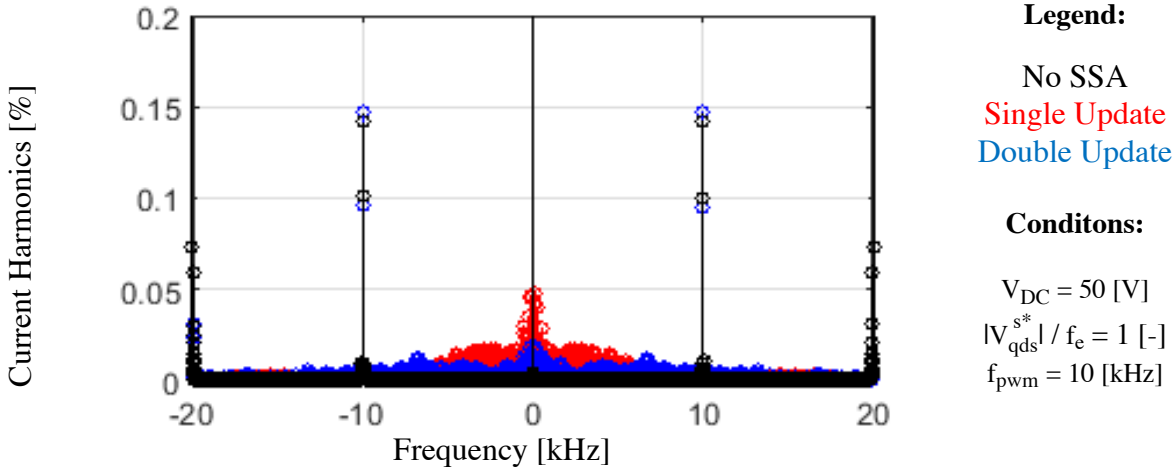


Figure 5-16: Synchronous frame q and d-axis current harmonics for the EV-SSA using single and double-update control rates.

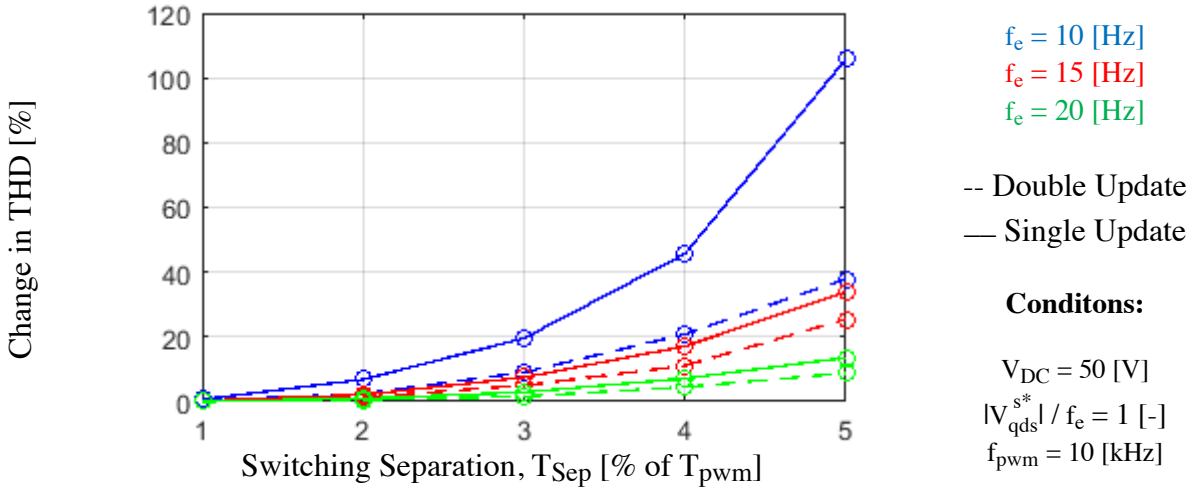


Figure 5-17: Synchronous frame q and d-axis current harmonics for the EV-SSA using single and double-update control rates.

5.5 Summary

By relaxing the requirement that the inverters average voltage output across one switching period is not altered, the EV-SSA approach is developed. This increases the flexibility of intra-inverter SSA by allowing for its operation with conventional double-update control structures as well as seamless integration with potential zero-sequence-voltage-based inter-inverter SSA. Because this method introduces voltage errors, resulting current errors must be estimated and properly compensated for so that closed-loop current control does not experience performance degradation. Comparing current waveforms produced by the APWM and EV-SSA, APWM-SSA produces significantly larger PWM ripple while EV-SSA causes lower frequency oscillations with slightly smaller peak magnitudes. A harmonic spectra comparison reflects this, with APWM-SSA producing large, concentrated peaks of harmonics content at half-multiples of the switching frequency while EV-SSA produces a more distributed harmonic spectrum with slightly smaller THD. Moreover, EV-SSAs harmonic distortion can be reduced further by implementing it in a double-update control structure, distributing harmonic content to higher frequencies while lowering THD.

Chapter 6 Compensation of Deadtime Effects for Simultaneous Switching Avoidance

The SSA algorithms developed in this research both infer when switching instances will occur based on the voltage commands produced by the controller. Using an ideal inverter model- with infinitely quick switching speeds, no delays due to signal propagation or gate-drive dynamics, and no deadtime insertion-this assumption works perfectly. However, all the aforementioned non-ideal effects introduce a measure of uncertainty between the assumed switching transient timing and what actually occurs in the inverter.

Drawing from Chapter 2, switching transients should be the sufficiently separated so that their regions of peak di/dt do not overlap. However, the introduction of excessive T_{Sep} will produce significant distortion in the inverter's output current waveforms. To balance this pair of competing objectives, the uncertainty in switching instant timing should be minimized so that T_{Sep} can be reduced as well. In this Chapter, a method to properly compensate for deadtime-induced commutation timing errors in the context of SSA is proposed.

6.1 Ideal Modeling of Voltage Compensation for Simultaneous Switching Avoidance

When analyzing the accuracy of the average output voltage each switching period, voltage drops across switching devices and commutation timing errors due to deadtime insertion are the two primary contributors to errors. These are shown in Fig. 6-1, with current and voltage drop polarities defined in Fig 6-2. While these load-current driven nonlinear effects are often addressed together in compensation schemes, it is necessary to separate the two for proper implementation of SSA. This separation is shown in Fig 6-3.

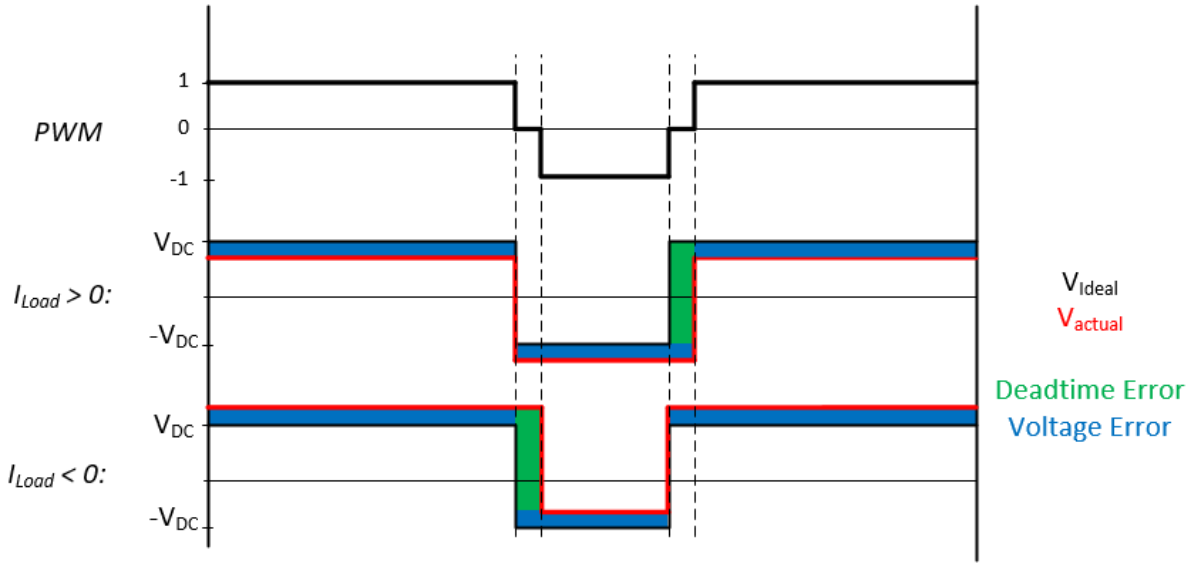


Figure 6-1: Non-ideal effect of voltage drop errors and deadtime-induced commutation timing errors on inverter output voltage.

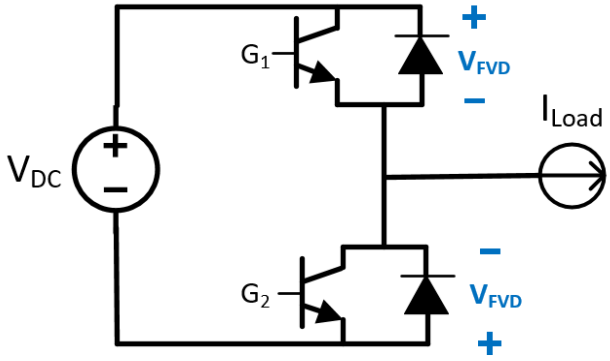


Figure 6-2: Definition of load current polarity and switching device voltage drops in an inverter phase

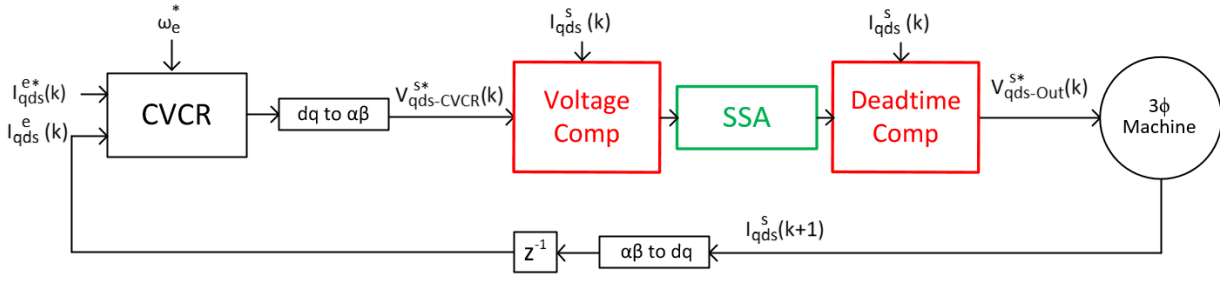


Figure 6-3: Integration of inverter voltage and deadtime error compensation together with SSA algorithms.

Intuitively, it would make sense to place the SSA algorithm as the last block before outputing the final voltage, $V_{qds\text{-}out}^{s}$. This is true for voltage compensation. Going from Fig. 6-1, when voltage compensation is properly applied the resulting PWM output becomes as shown in Fig.6-2, where the controller has an accurate estimate of the DC voltage that is actually applied to the load. Now, the only remaining error is due to deadtime.

Because deadtime error is intrinsicly tied to commutation timing it is of particular importance to SSA implementation. In order for SSA to work as desired, the desired switching instances must be accurately obtained. This can be done by adding a compensation voltage as described by (6.1-1). This results in the same output voltage waveform, regardless of current polarity, as shown in Fig. 6-5.

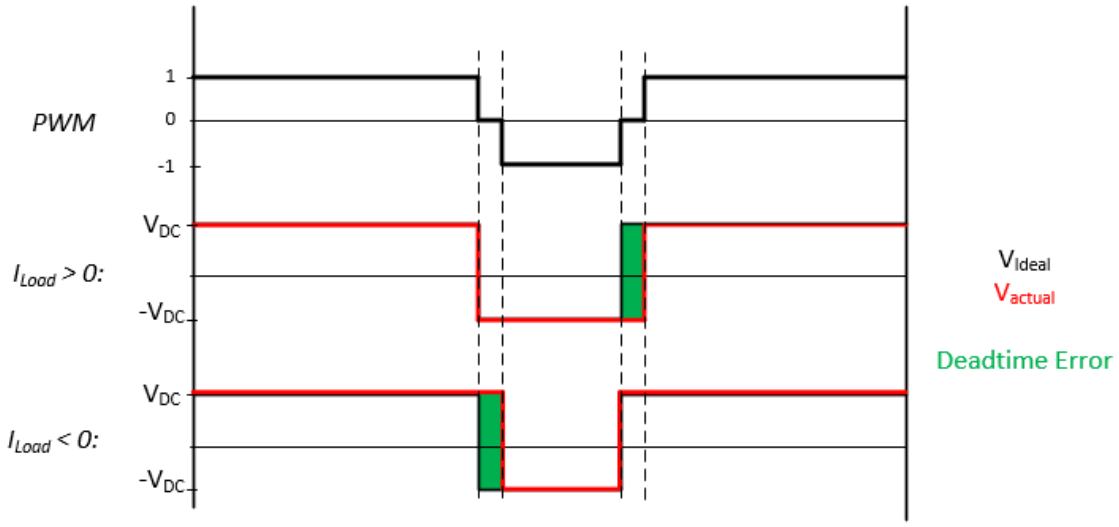


Figure 6-4: Remaining deadtime-induced commutation timing errors after voltage drops have been appropriately compensated for.

$$V_{Comp} = V_{Uncomp} + \frac{V_{DC}\, T_{dead}}{V_{PWM}} Sign(I) \qquad (6.1\text{-}1)$$

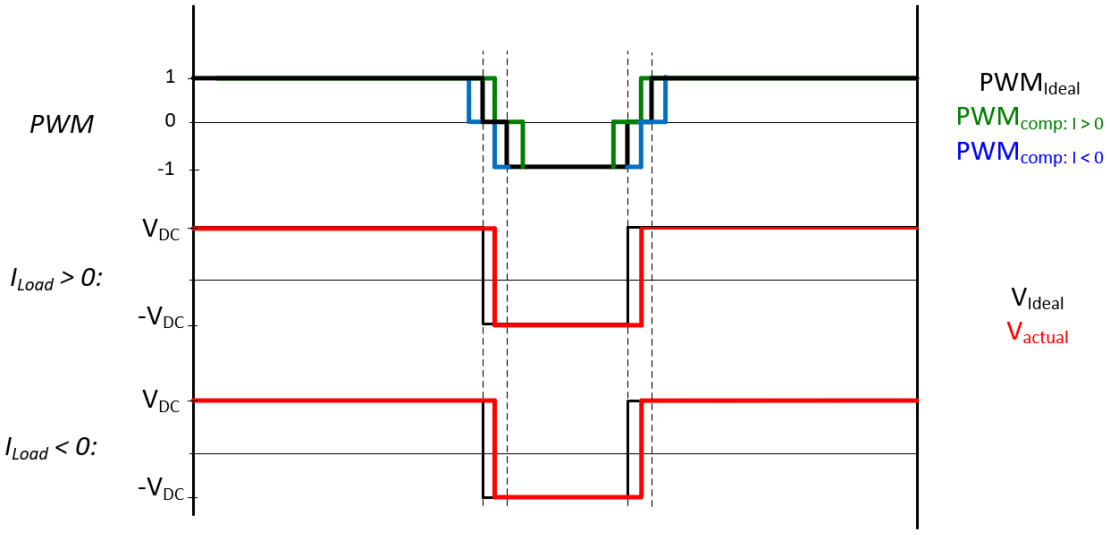


Figure 6-5: Elimination of deadtime-induced commutation timing errors by adding a constant current polarity-dependent term.

Framing this another way, a compensation voltage is added so that the desired switching instances are achieved after deadtime is inserted into the output PWM waveform. The developed SSA algorithms use the voltage command to estimate when switching instances will occur. However, they assume an ideal inverter without deadtime-effects. So, to ensure the switching instances enforced by SSA are achieved, the compensation must be added after SSA has been performed. This approach will be demonstrated and verified experimentally in the following section.

6.2 Experimental Compensation of Deadtime-Induced Commuatation Timing Effects

Fig. 6-6 shows one of the PWM gating signals produced by the AIX controller used in this research. This plotted is zoomed in to highlight the deadtime inserted by controller between transitions from high-to-low and vise-versa. In this case, the controller has been programed to provide 2.8 [μs] of deadtime, which is clearly seen in the waveform.

To measure the effect of this deadtime on the inverter's output voltage, a simple open-loop test was carried out where phase B and C were given constant voltage commands of 150 [V]. With the DC bus set at 300 [V], this corresponds to a constant 50% duty cycle command. Different voltage commands were then applied to Phase A to drive positive and negative load current through the

machine Fig. 6-7. The resulting voltage waveforms applied to Phase B were recorded for different load current values to measure the actual voltage output by the inverter.

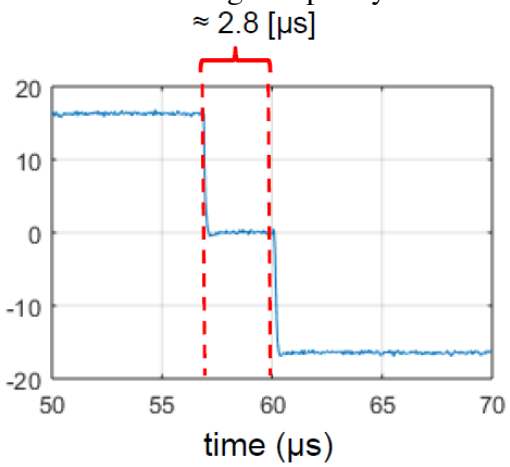


Figure 6-6: Measured deadtime insertion on the PWM output of the AIX controller used for experimental evaluation.

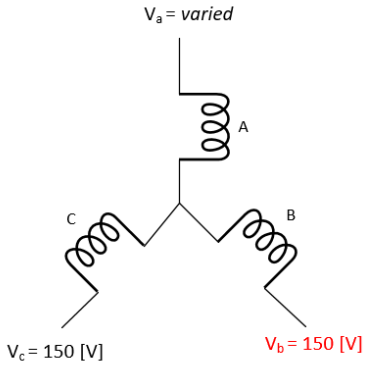


Figure 6-7: Constant voltage commands applied to each phase of the induction machine.

Time-domain results from this test are shown in Fig. 5-8. In these waveforms, the oscilloscope was set to trigger on the falling-edge of the voltage waveform so all timing variation appears on the rising-edge. Fig. 6-8(b) shows a zoomed view of these rising edges. Here commutation timing varies by roughly 5.5 [μs], which is as expected given a deadtime of 2.8 [μs]. Moreover, this plot shows the impact of load current magnitude and polarity on the timing effects. Looking particularly at the 0.5 [A] case, the switching transient takes significantly longer to occur and does not begin or end at the same times as the 2 [A] case. This highlights the particular difficulty in handling deadtime effects at low load current levels.

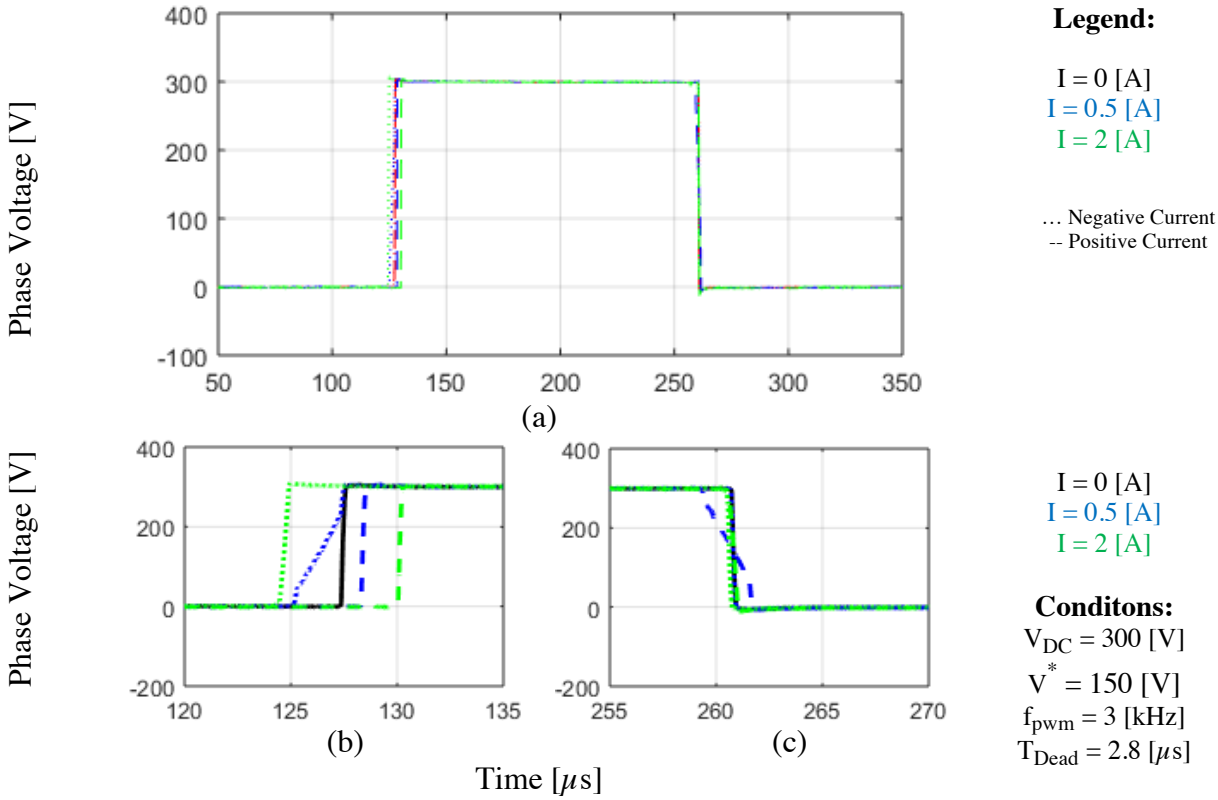


Figure 6-8: Measured voltages on Phase B across one switching period (a) for different phase current magnitudes. Zoomed-views are provided for the rising-edge (b) and falling-edge (c) of the voltage waveform (Oscilloscope triggered on the falling edge).

To address for this commutation timing variation, a sigmoid compensation function is used in this work. This is expressed in (6.2-1) and plotted in Fig 6-9. Here the variable "*a*" is a tunable parameter that determines how quickly the transition from -1 to 1 occurs. While deadtime commutation errors are ideally only a function of load current polarity, non-ideal effects near zero current are more properly handled using this sigmoid activation function for compensation. This activation function can then be multiplied by the effective voltage error due to deadtime, as described in (6.2-2).

$$f(I_{Load}) = \frac{2}{1+e^{-(a \times I_{Load})}} - 1 \tag{6.2-1}$$

$$V^{*}_{Comp} = V^{*}_{Uncomp} + \frac{V_{DC} T_{Dead}}{T_{PWM}} f(I_{Load}) \tag{6.2-2}$$

$$V_{Avg} = \frac{1}{T_{PWM}} \int_{0}^{T_{PWM}} V_{Phase}(t) \tag{6.2-3}$$

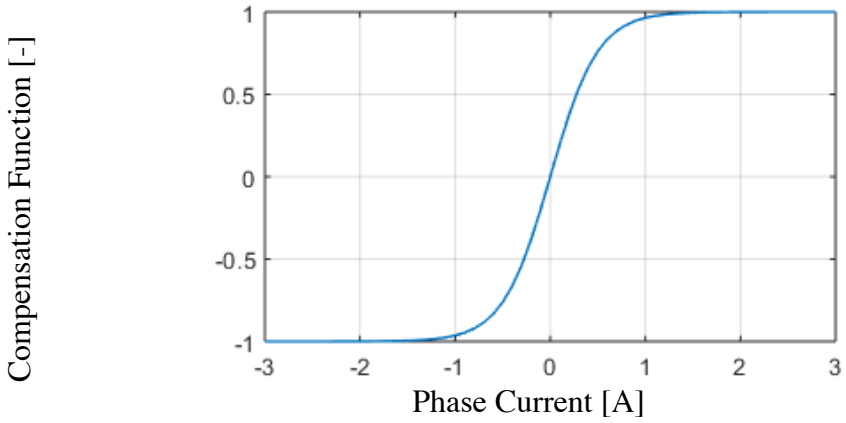


Figure 6-9: Sigmoid function used for providing compensation of deadtime effects.

To measure the effectiveness of this compensation scheme, average output voltages where calculated for phase B, with and without this compensation (6.2-3). Results for these calculations are plotted in Fig. 6-10 as a function of load current. Here, the average voltage produced by V^{*}_{Uncomp} clearly deviates from the desired value of 150 [V]. Moreover, its transition from positive to negative error near zero current occurs in a non-linear fashion as in the compensation function used to eliminate it. Applying this compensation, V^{*}_{Comp} produces an output voltage with significantly less error. Here, remaining error is primarily due to on-state voltage drops across the switching devices, as well as any lingering uncompensated deadtime effects.

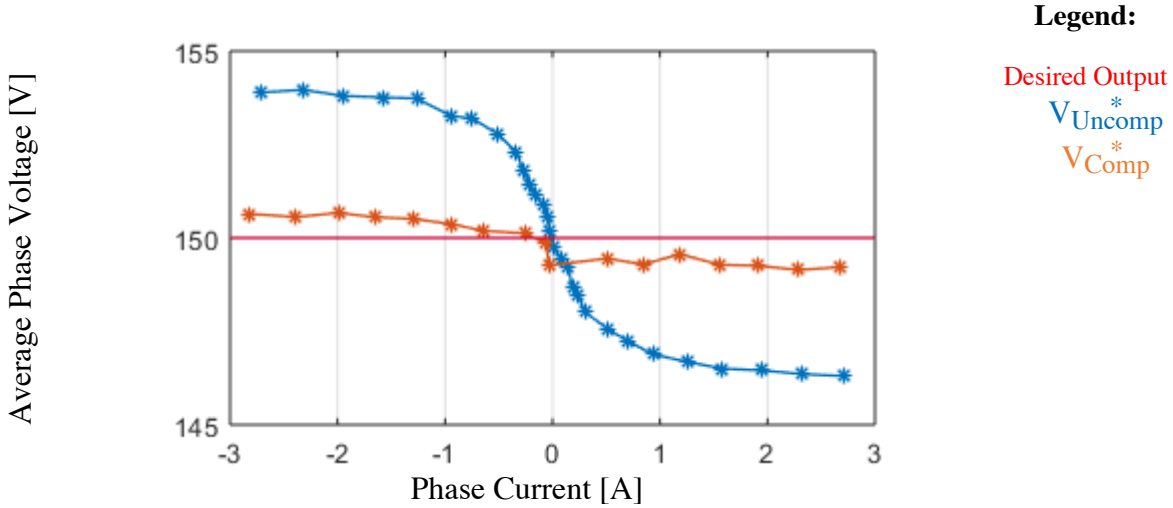


Figure 6-10: Calculated average voltages applied across Phase B of the inverter's output with and without deadtime compensation at different load current values

Returning to the time-domain analysis, voltage waveforms after compensation has been performed are shown in Fig 6-11. Focusing again on the rising-edge, commutation timing

deviation is reduced from about 5.5 [μs] to roughly 2 [μs]. Ignoring the low-current case, this deviation is further reduced to roughly 1 [μs].

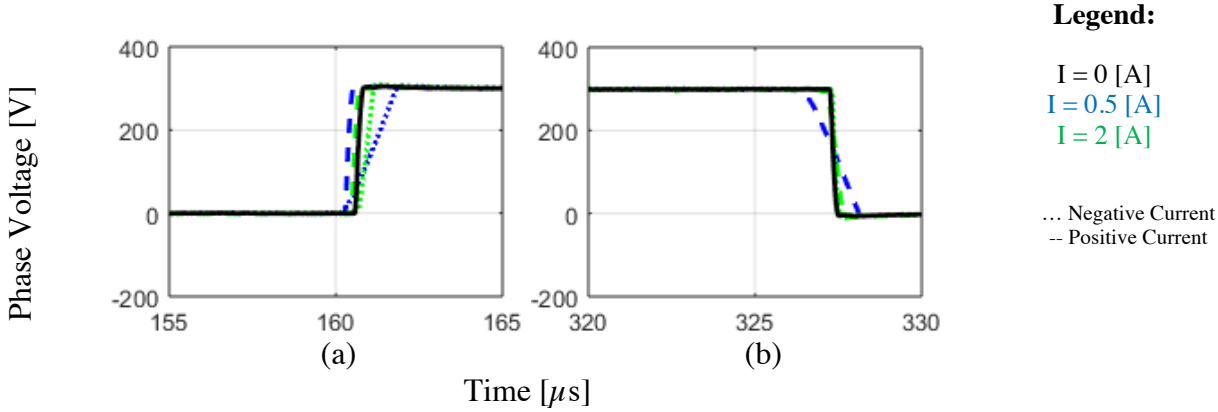


Figure 6-11: Measured voltages on Phase B across one switching period for different phase current magnitudes with deadtime compensation implemented. The rising and falling edges are shown in (a) and (b), respectively. (Oscilloscope triggered on the falling edge)

By significantly reducing the deviation in commutation timing caused by deadtime insertion, the amount of enforced switching separation that SSA algorithms must introduce can be reduced. The open-loop compensation scheme proposed in this chapter effectively performs this function. By specifically placing this compensation scheme after SSA in the control execution order, it will adjust the output voltage command so that the switching instances assumed by the SSA algorithm are actually achieved.

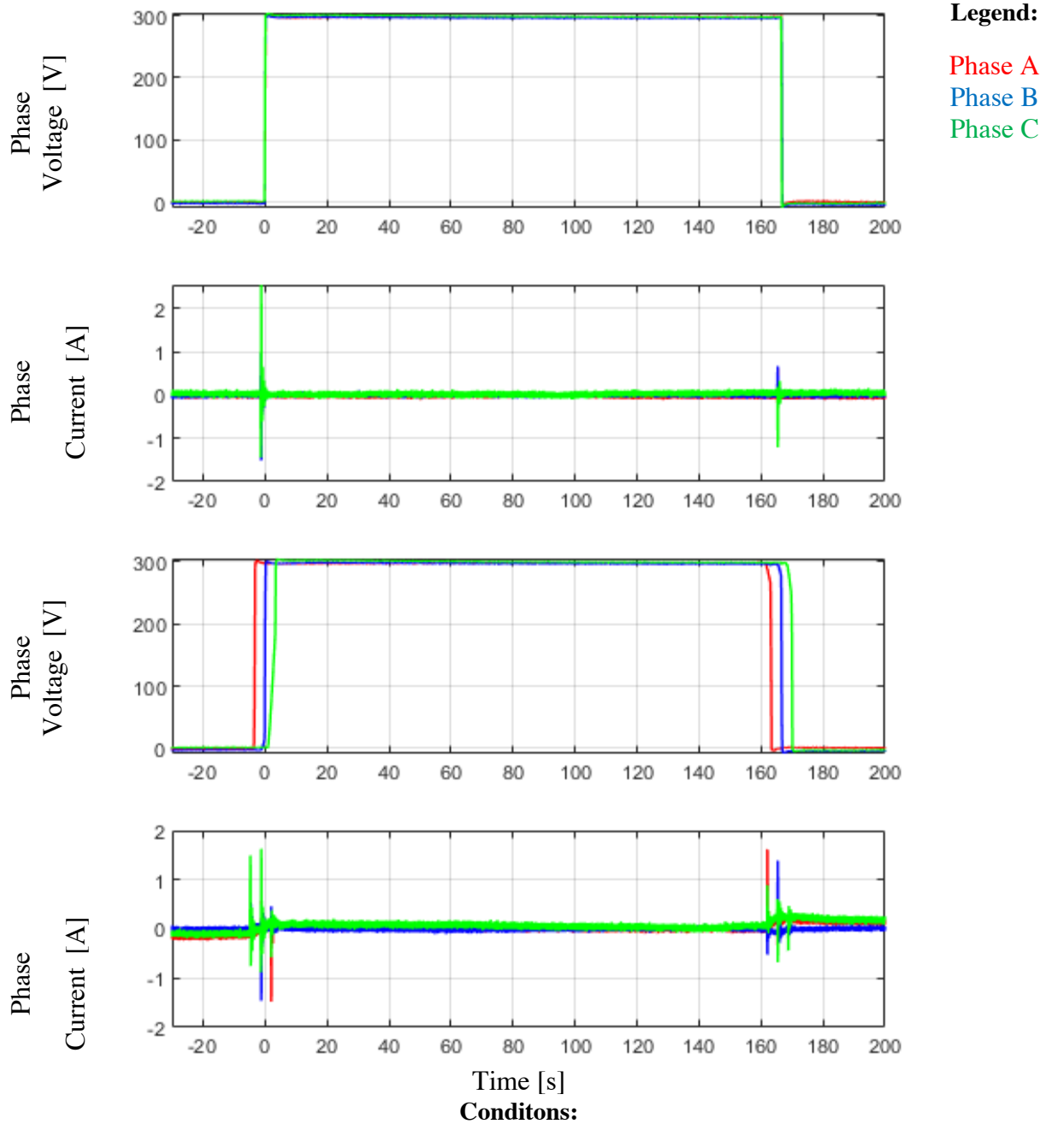
6.3 Verification of Enforced Switching Separation

With this deadtime compensation scheme implemented, tests were carried out to verify that the desired switching separation be each SSA algorithm. This was done by passing a constant voltage vector command to each SSA method and measuring the output phase voltages and currents.

The first set of tests were carried out where $|V_{qds}^{s*}| = 0$ [V]. In this case, all phases receive a 50% duty cycle without SSA active. When SSA is active, it requires using the 4-active vector method for the APWM-SSA technique. Fig 6-12 and Fig. 6-13 show operation of APWM-SSA and EV-SSA, respectively with $T_{Sep} = 0.01T_{pwm}$. With a 3 [kHz] pwm frequency, this equates to 3.3 [μs]. In each case, the algorithm achieves roughly this separation. This is the most difficult condition

for enforcing exact switching instances, due to the load currents near 0 [A]. So, the separation is less precise.

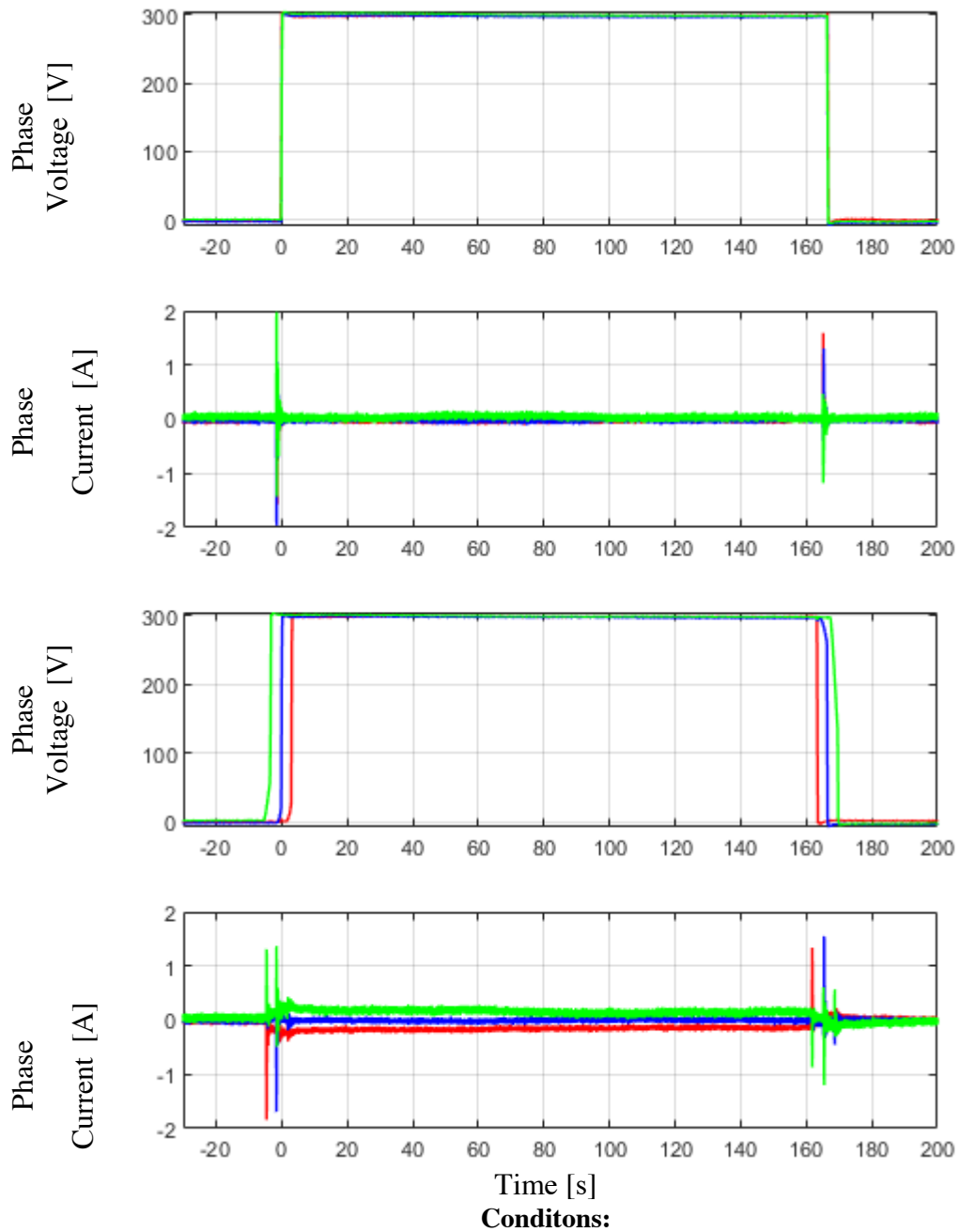
The second set of tests were carried out where $|V_{qds}^{s*}| = 15$ [V] along the V_1. In this case, phase B and C have identical duty cycle commands. Fig 6-14 and Fig. 6-15 show operation of APWM-SSA and EV-SSA, respectively with $T_{Sep} = 0.01T_{pwm}$. In each case, the algorithm achieves more precise separation because load current is sufficiently large to ensure rapid and predictable commutation.



Conditons:

$V_{DC} = 300$ [V] $|V_{qds}^{s*}| = 0$ [V] $f_e = 0$ [Hz] $f_{pwm} = 3$ [kHz] $T_{Sep} = 0.01T_{pwm}$

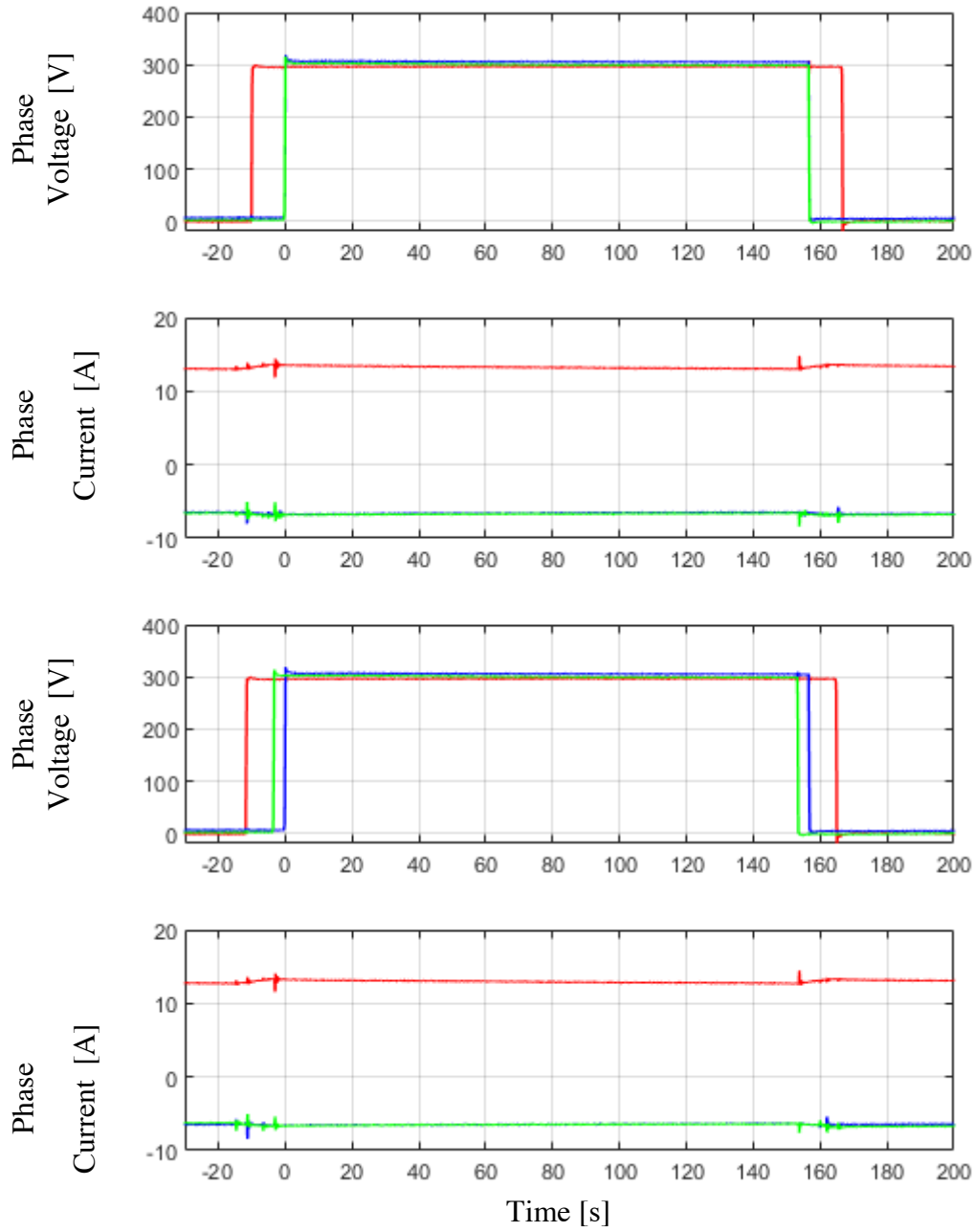
Figure 6-12: Verification of switching separation enforcement with the APWM-SSA algorithm operating at the inverter hexagon origin.



Conditons:

$V_{DC} = 300$ [V] $|V_{qds}^{s*}| = 0$ [V] $f_e = 0$ [Hz] $f_{pwm} = 3$ [kHz] $T_{Sep} = 0.01T_{pwm}$

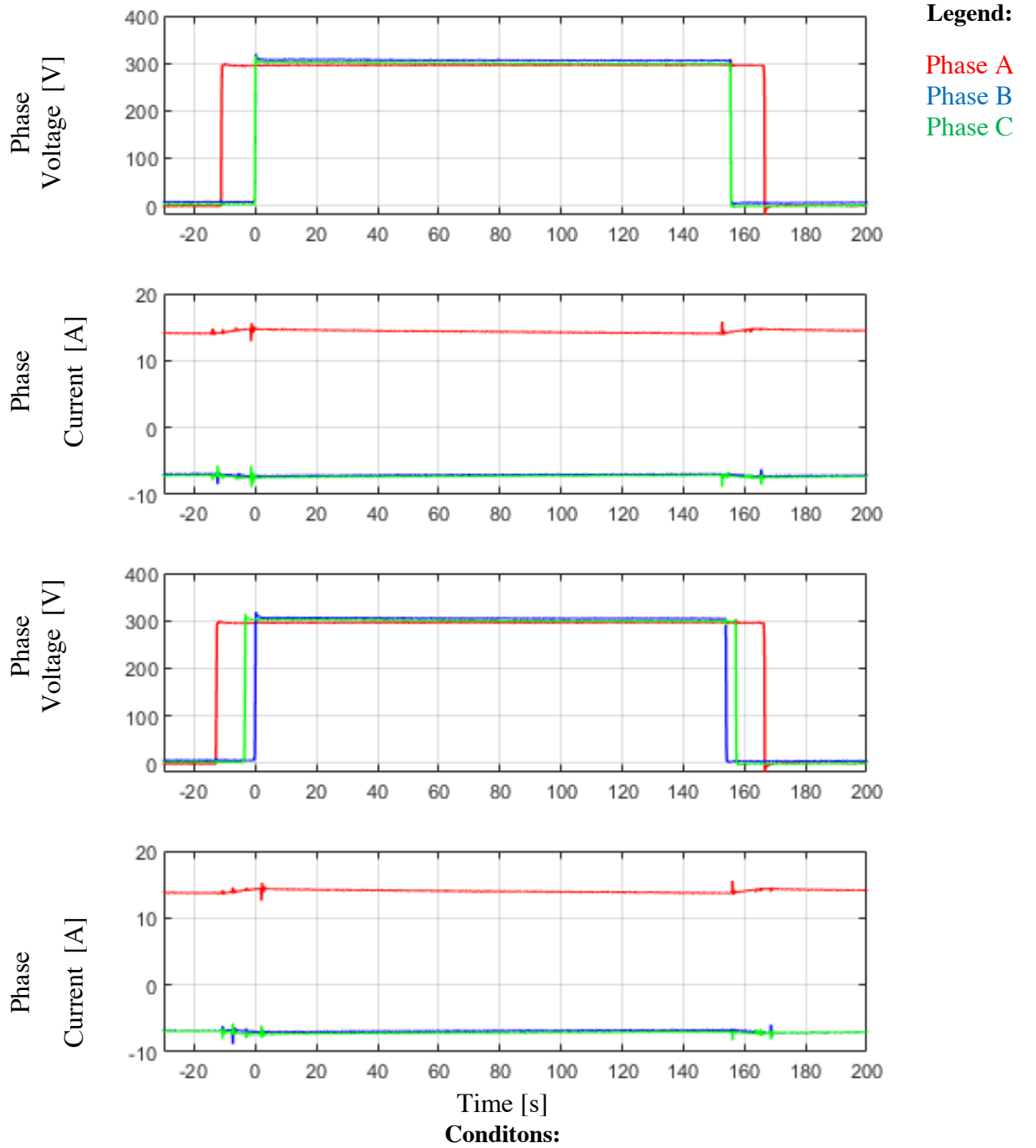
Figure 6-13: Verification of switching separation enforcement with the EV-SSA algorithm operating at the inverter hexagon origin.



Conditons:

$V_{DC} = 300$ [V] $|V_{qds}^{s*}| = 15$ [V] $f_e = 0$ [Hz] $f_{pwm} = 3$ [kHz] $T_{Sep} = 0.01T_{pwm}$

Figure 6-14: Verification of switching separation enforcement with the APWM-SSA algorithm operating at an inverter hexagon sector boundary.



Conditons:

$V_{DC} = 300$ [V] $|V_{qds}^{s*}| = 15$ [V] $f_e = 0$ [Hz] $f_{pwm} = 3$ [kHz] $T_{Sep} = 0.01T_{pwm}$

Figure 6-15: Verification of switching separation enforcement with the EV-SSA algorithm operating at an inverter hexagon sector boundary.

6.4 Summary

The SSA methods developed in this work assume an ideal inverter model to select output voltage vectors that avoid simultaneous switching. However, the necessary insertion of deadtime into the PWM gating signals produces commutation timing errors that are driven primarily by load current polarity and manifest voltage errors on the inverters output. Often times these voltage errors are compensated for together with other DC voltage drops inside the inverter. However, to handle these errors properly in the context of SSA, they must be separated. In this context, deadtime compensation is performed solely to ensure that the desired commutation instances are achieved. As such, it is performed after SSA. This has been shown experimentally to reduce commutation timing errors by roughly 60% in all cases and up to 80% when load current magnitude is sufficiently large. This significantly reduces the amount of switching separation that must be enforced by SSA algorithms, thus reducing the amount of distortion imposed on the inverter output. Finally, switching separation enforcement was verified for each SSA algorithm under different load current conditions.

Chapter 7 Current Regulation with Intra-Inverter SSA Algorithms

In this chapter, the proposed intra-inverter SSA algorithms are implemented on a three-phase induction machine drive. Using this test setup, the impact of the EV-SSA and APWM-SSA on machine current harmonics are evaluated and compared. This is done using a combination of steady-state and transient test cases.

7.1 Integration of Intra-Inverter SSA with a Current-Regulated Drive

For this chapter, the focus will be placed on how proposed SSA algorithms can be implemented within a current-regulated drive. For simplicities sake, it is assumed a field-oriented control scheme appropriate for the machine being controlled is selected. This generates synchronous frame current commands for the current regulator to track. Here, a complex-vector current regulator is assumed, as described in Chapter 1.3. This includes decoupling of the load machine's back-emf.

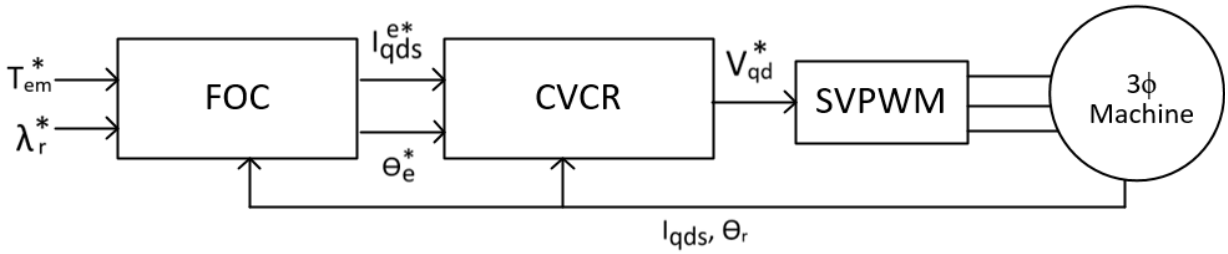


Figure 7-1: General field-oriented, current regulated control structure used in for SSA integration.

7.1.1 Simultaneous Switching Avoidance Using Asymmetric PWM (APWM-SSA)

To integrate it with the current regulator control structure, the APWM-SSA algorithm can simply be placed after the current regulator (Fig. 7-2). Because APWM-SSA is designed to produce the same average output voltage as the current regulator's commanded voltage, $V_{qds\text{-}CVCR}^{s*}$, no additional compensation schemes need to be added. The APWM-SSA algorithm takes $V_{qds\text{-}CVCR}^{s*}$ as an input, identifies whether simultaneous switching will occur, and takes the appropriate action. If the command vector falls in a region of simultaneous switching on the voltage hexagon, a pair of new command vectors are generated, $V_{qds\text{-}asym1}^{s*}$ and $V_{qds\text{-}asym2}^{s*}$, that

fall outside the simultaneous switching region and whose average equals the original commanded voltage.

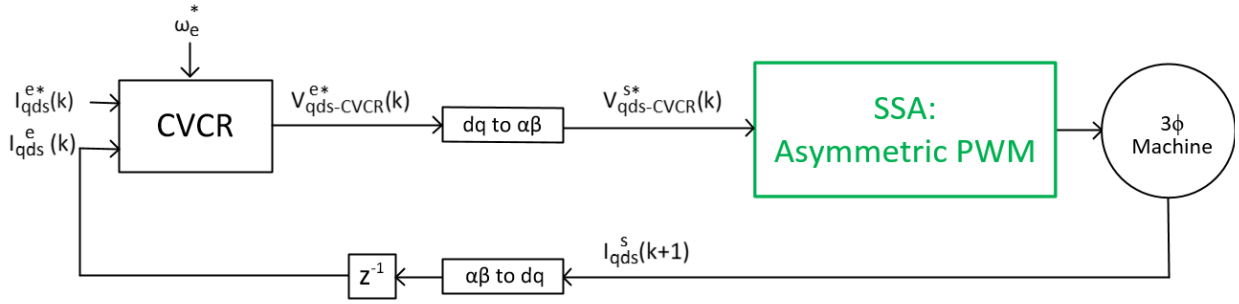


Figure 7-2: Current regulator control structure with APWM-SSA included.

To implement this dual command vector approach, a double-update PWM structure is used. Unlike conventional double-update operation, where current control's sample time is half the switching period, APWM-SSA requires current control to be performed at the same frequency as switching. This is so that the desired average output voltage value, $V_{qds\text{-}CVCR}^{s*}$, can be achieved. An example of this implementation is shown in Fig. 7-3.

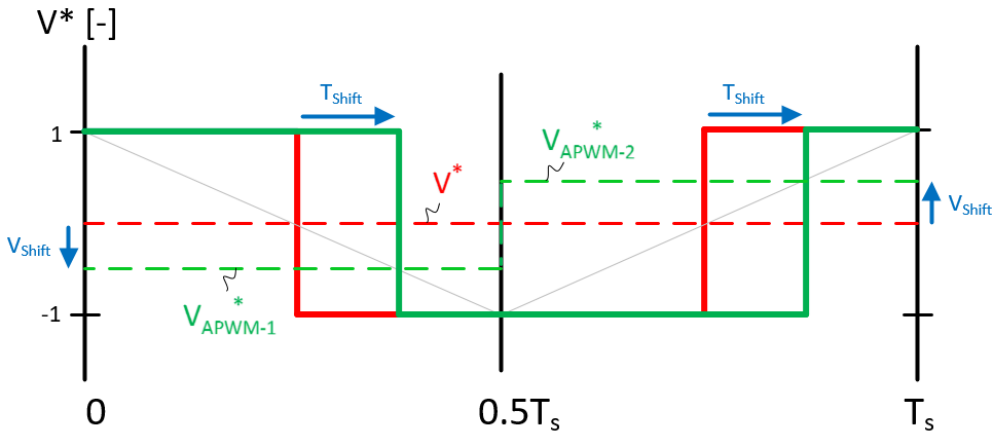


Figure 7-3: Implementation of the APWM-SSA algorithm using a double-update PWM structure.

7.1.2 Simultaneous Switching Avoidance Using Voltage Error Vectors (EV-SSA)

To implement the EV-SSA method with a current-regulated drive, the error vector selection and compensation blocks must be properly integrated into the system. This is shown in Fig 7-4. Here, the command from the CVCR, $V_{qds\text{-}CVCR}^{s*}$, is passed through the error vector selection

algorithm, choosing the closest possible vector, $V^{s*}_{qds\text{-}SSA}$, that will avoid simultaneous switching. Using the difference between $V^{s*}_{qds\text{-}CVCR}$ and $V^{s*}_{qds\text{-}SSA}$, ΔV^{s}_{qds} can be calculated. ΔV^{s}_{qds} is then used to estimate the resulting current error, ΔI^{s}_{qds} and a compensation voltage that will eliminate ΔI^{s}_{qds} during the next control cycle, $\Delta V^{s*}_{qds\text{-}null}$. ΔI^{s}_{qds} can be subtracted from the measured load current so that the CVCR does not see the effects of SSA on its feedback current, $I^{e}_{qds\text{-}fb}$.

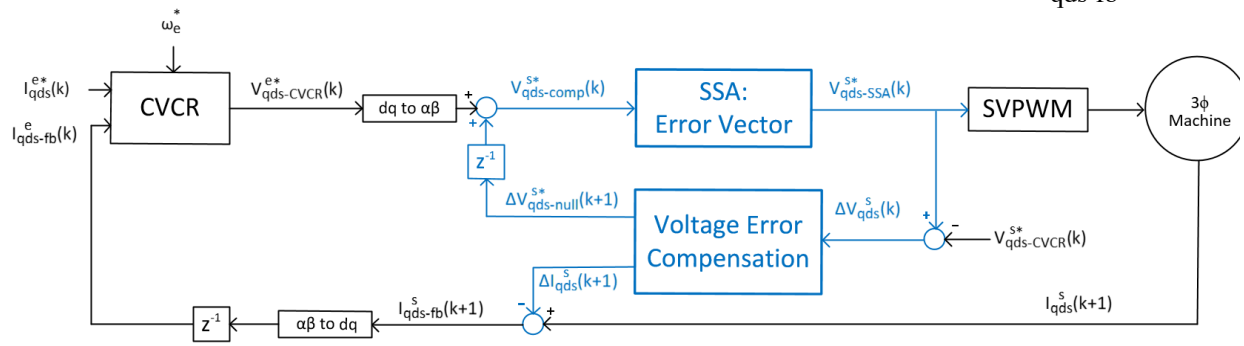


Figure 7-4: Modified current regulator control structure for EV-SSA with voltage error compensation.

7.2 Experimental Evaluation of Intra-Inverter SSA In a Current Regulated Drive

To understand how the proposed SSA algorithms impact current regulation performance in the induction machine motor drive, a series of steady-state and transient tests are performed. The impact of each SSA technique is evaluated first from the perspective of the CVCR using sampled current waveforms. Then, high-frequency current waveforms measured with external current probes (Lecroy CP031) are used to measure the impact on harmonic content with PWM effects included.

7.2.1 Experimental Setup

The test stand used in this evaluation consists of two identical induction machines connected back-to-back. These induction machines are driven by identical three-phase inverters which share a common DC bus. In this way, power can circulate between the load and test machines during testing. The DC bus is also fed by a Magna DC power supply. Current sensors in each inverter phase were used to provide current measurements. The AIX controller unit used previously was

once again used to run the necessary control schemes and provide gating signals to the two inverters. A block diagram of this system is shown in Fig 7-5.

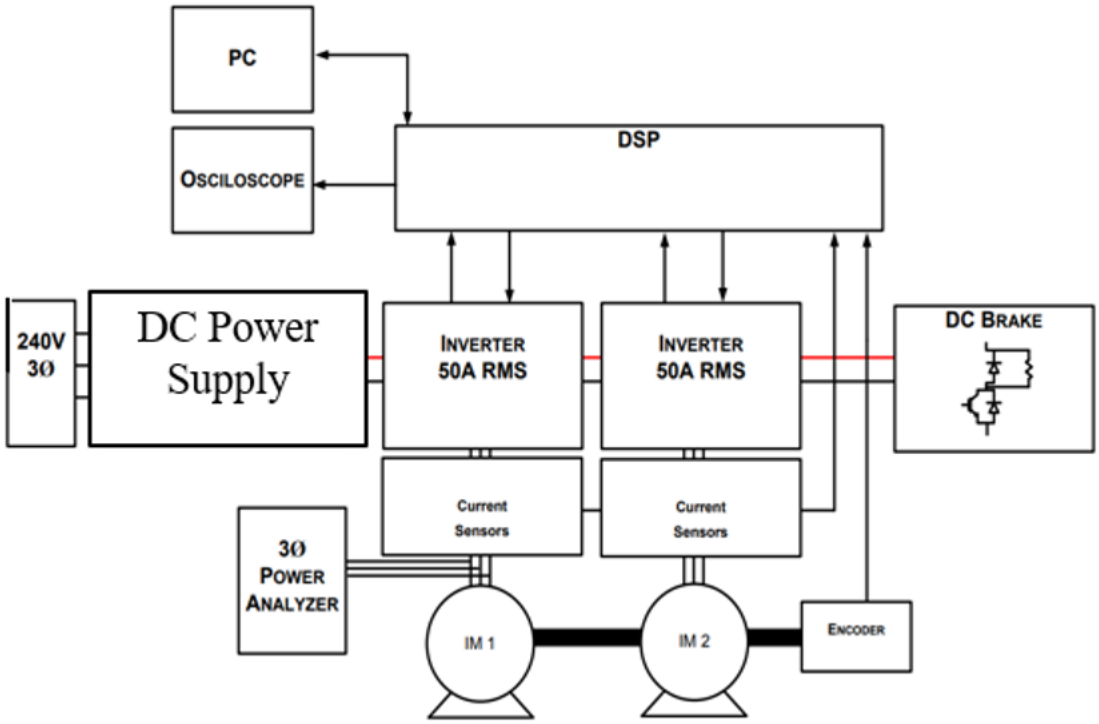


Figure 7-5: Block diagram of the experimental test setup used in this evaluation.

The two identical induction machines used in this test setup are General Electric 5K182BC18A models. Their nameplate and estimated parameters are shown in Table 7-1.

Table 7-1. GE Model 5K182BC218A Specifications and Parameters

Rated Voltage	240 [V_{RMS}] (line-to-line)
Rated Frequency	60 [Hz]
Rated Power	3 [hp]
Rated Torque	12 Nm
Rated Flux	0.5 [V-s]
Rated Slip	2.5%
Pole Pairs	2
Stator Resistance	0.8 [Ω]
Rotor Resistance	0.4 [Ω]
Magnetizing Inductance	99 [mH]
Stator Leakage Inductance	5.2 [mH]
Rotor Leakage Inductance	5.2 [mH]

Each induction machine is driven by a three-phase VSI. The power electronics used in these inverters is the Mini Skiip8 inverter module, which provides built-in protection with current and thermal sensing as well as a hardware dead time. Specifications for this power module are shown in Table 7-2.

Table 7-2. Inverter Hardware Specifications and Parameters.

DC Link Voltage	800 [V_{DC}]
DC link Capacitance	1.5 [mF]
Rated Output Current	50 [A_{RMS}]
Maximum Switching Frequency	20 [kHz]
Hardware Deadtime	2.2 [μs]

An AIX XCS2000 Controller was used to provide system control. The FPGA included in the XCS2000 is used to produce the PWM gating signals sent to the inverter modules. In addition, the AIX controller was also connected to a desktop computer via Ethernet. This was used to alter operating conditions during testing, as well as to retrieve current sensor measurements recorded with the DSP during testing.

Fig. 7-6 shows the control system structure used for testing SSA algorithms on the test machine. Conventional IFOC is used to generate synchronous frame current commands as well as the synchronous frame angle, based on the torque and rotor flux commands. These are passed to the CVCR which generates a voltage command. Here, the CVCR is tuned for a bandwidth of 100 [Hz]. These are then passed through voltage compensation, the SSA algorithm being tested, and then deadtime compensation, as described in Chapter 4. The final voltage command is then passed to the PWM modulator. The load machine is simply used for speed regulation, and uses a similar control structure, without the SSA algorithms and with a motion controller providing torque commands.

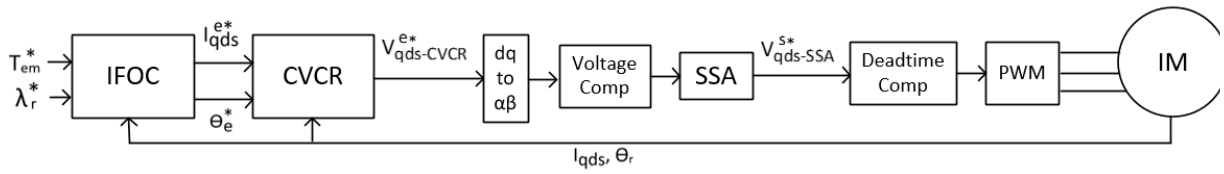
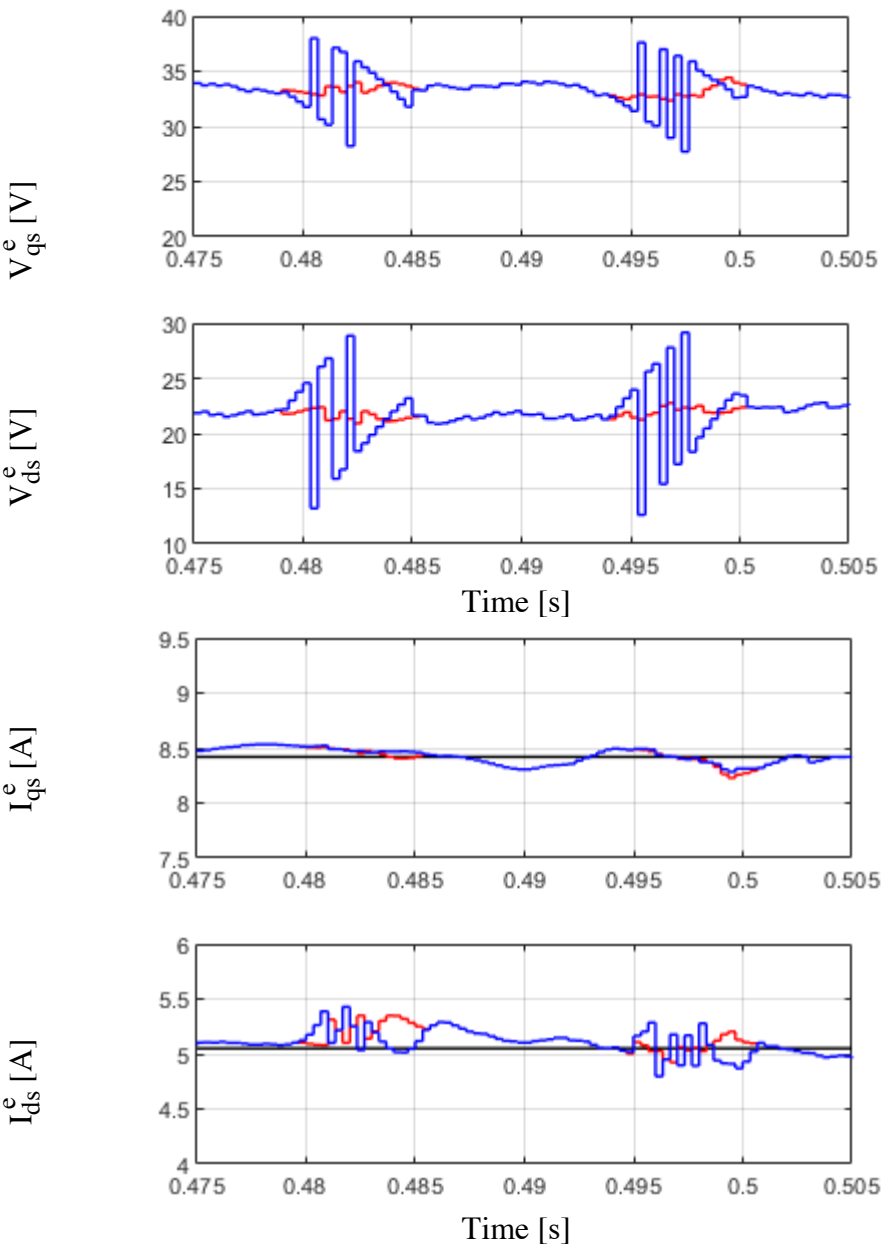


Figure 7-6: Control system block diagram for the IFOC induction machine drive used in this evaluation.

7.2.2 SSA Under Steady-State CVCR Operation

Fig. 7-7 and Fig 7-8 show the output voltage commands from the CVCR as well as the sampled current waveforms seen by the controller for the EV-SSA and APWM-SSA methods, respectively. Beginning with the voltage commands, the high-frequency voltage oscillations introduced by the SSA algorithms is clearly seen. In contrast, the $V_{qds\text{-}CVCR}^{e*}$ commands remain relatively unchanged. In both cases, there is some oscillation that appears in $V_{qds\text{-}CVCR}^{e*}$ due to harmonic content that appears in the sampled currents. This is likely due to modelling errors leading to incomplete or slightly inaccurate open-loop decoupling of the introduced current error. In addition, the relatively low switching frequency leads to more non-linear effects to appear in the system response. For the APWM-SSA case, these nonlinear effects introduce some current ripple, even though the average output voltage across the PWM period is not changed.

Stator phase currents were also measured using Lecroy CP031 current probes to observer the harmonic content on the current waveform with PWM switching harmonics included. A comparison of the EV-SSA and APWM-SSA waveforms is shown in Fig. 7-9. Here the impact of each is clearly seen in the d-axis waveform. As was found in simulation, EV-SSA causes smaller, lower frequency ripple content while APWM-SSA produces higher-amplitude ripple that oscillates at the PWM frequency.



Legend:

CVCR Voltage
Command
SSA Output

Conditions:

$\omega_e = 10$ [Hz]
$T_{em}^{*} = 12$ [n-m]
$\lambda_r^{*} = 0.5$ [V-s]
$f_{pwm} = 3$ [kHz]
$T_{sep} = 0.02T_{pwm}$

CVCR Bandwidth:
$\omega_{CVCR} = 100$ [Hz]

Figure 7-7: Synchronous frame sampled voltage and current waveforms during steady-state operation using the EV-SSA.

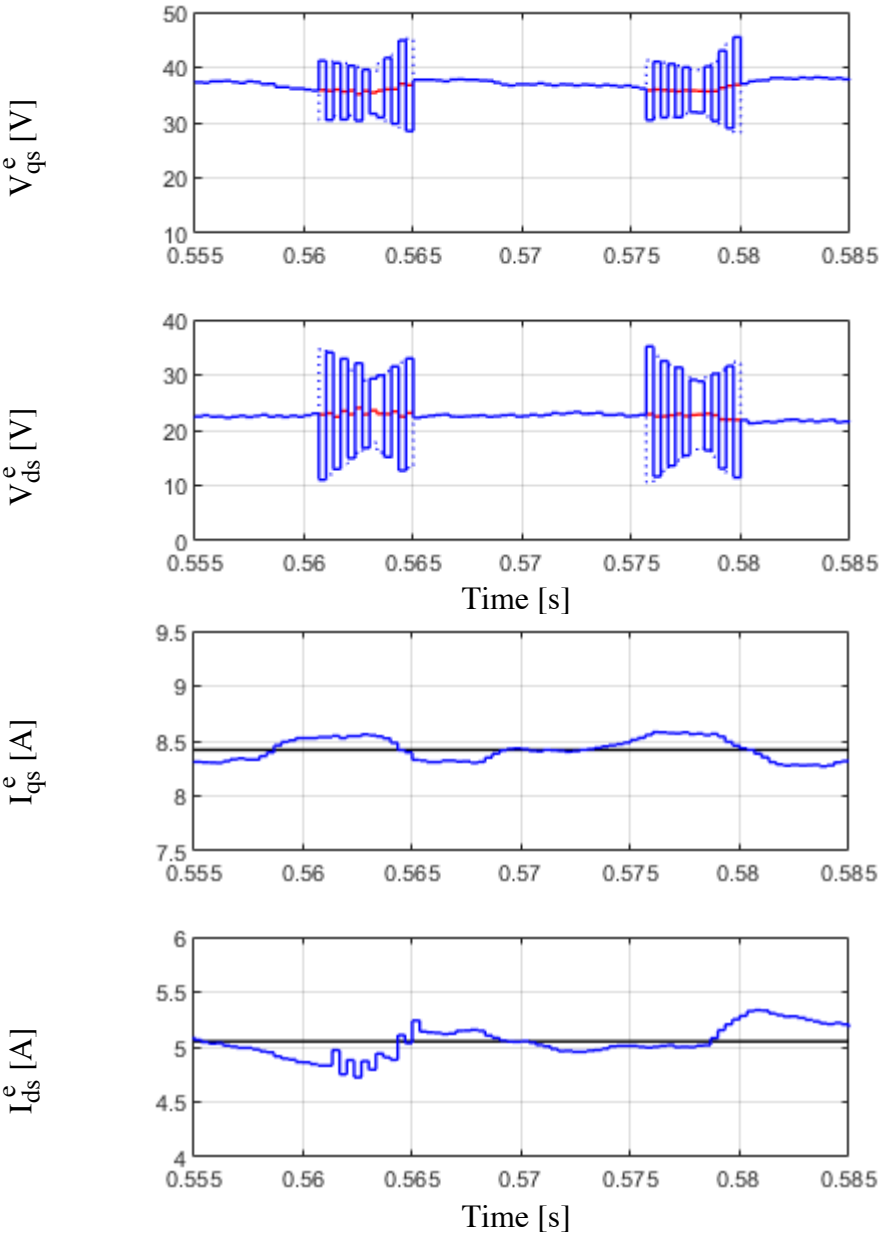


Figure 7-8: Synchronous frame sampled voltage and current waveforms during steady-state operation using the APWM-SSA.

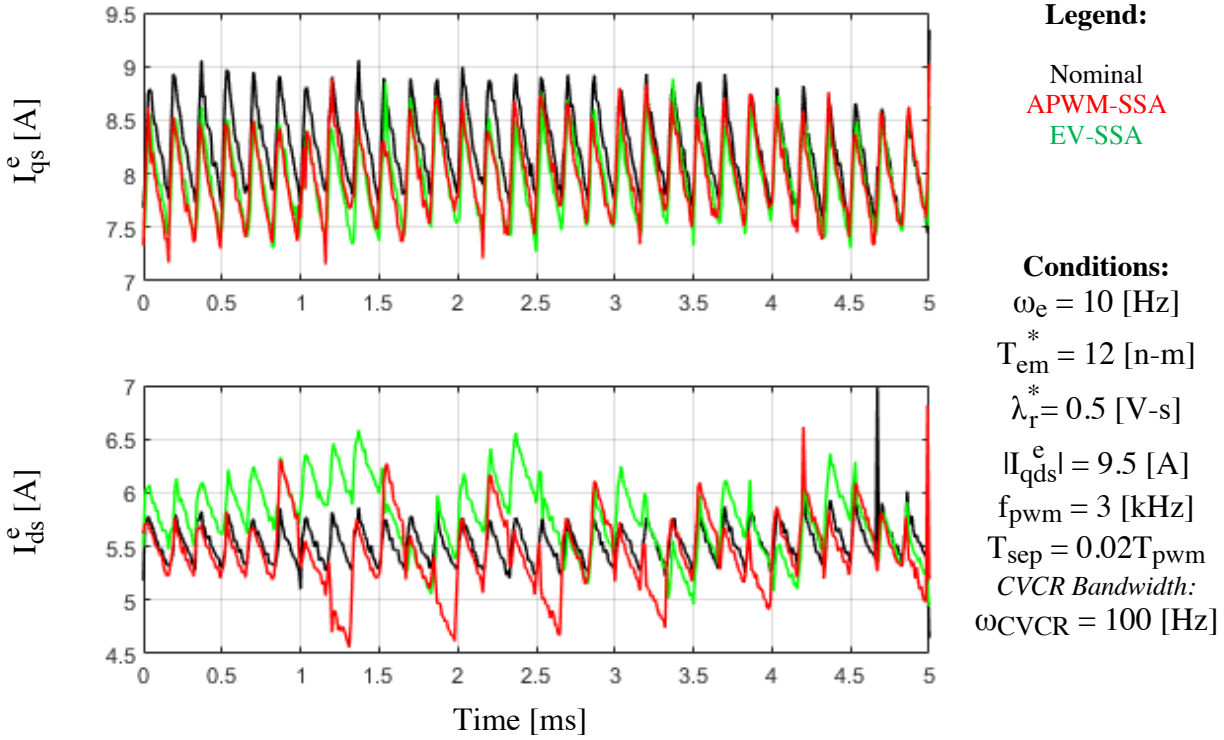
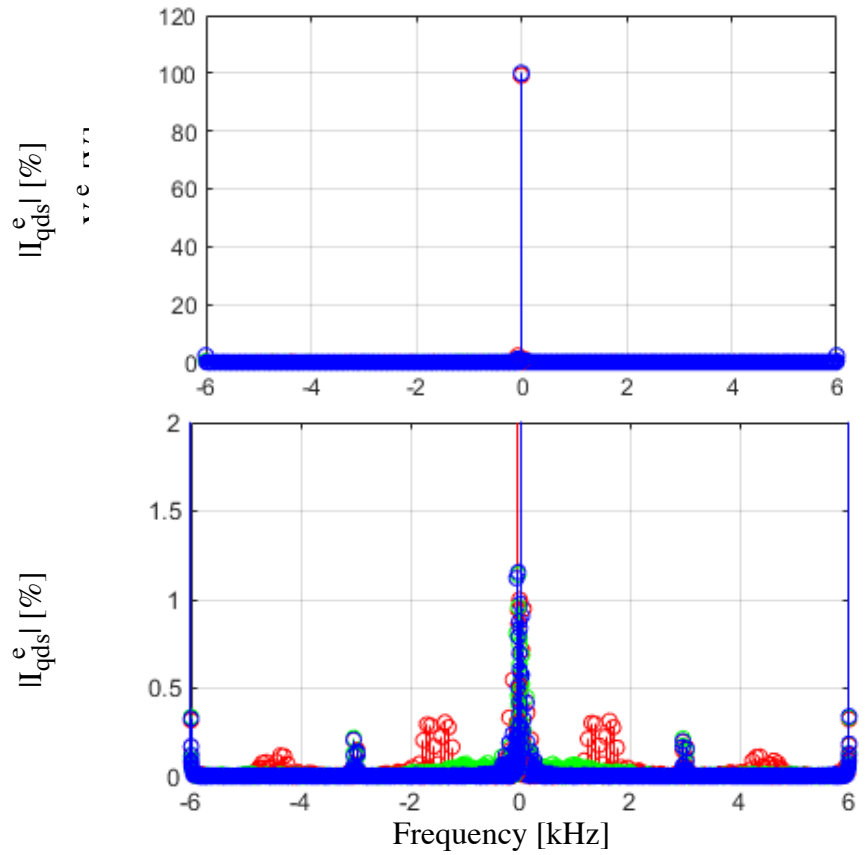


Figure 7-9: Measured current waveforms transferred into the synchronous frame from steady-state operation using the EV-SSA and APWM-SSA.

Fig 7-10 shows FFTs for the synchronous frame current waveforms in Fig. 7-9. Once again, the results agree well with simulation. The APWM-SSA method produces concentrated harmonic content at half-multiples of the PWM frequency. During experimental testing this actually produces a distinct tone that increases in volume as T_{sep} increases. On the other hand, EV-SSA produces a more distributed harmonic spectrum with smaller peak amplitudes.

Finally, Fig. 7-11 shows a summary of the change in RMS currents introduced by the two SSA algorithms. Here, the relative impact of each method is similar to simulation results. That is EV-SSA produces slightly less RMS content. Moreover, the effect decreases as the fundamental frequency increases.



Legend:

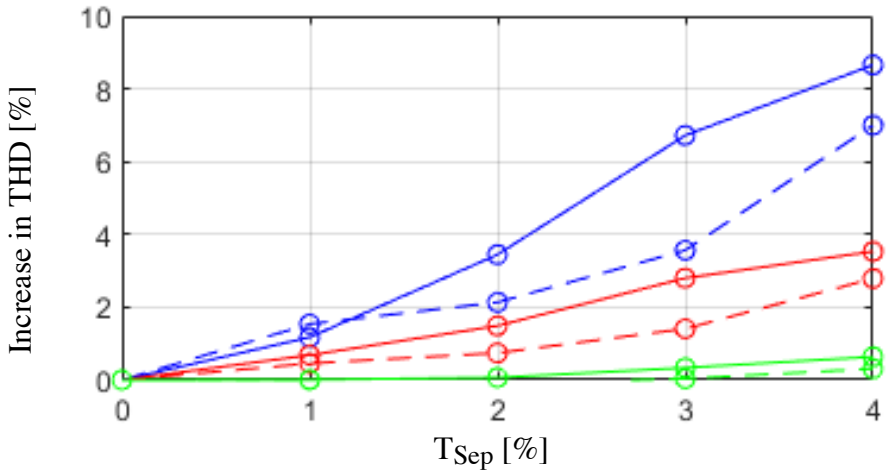
Nominal
APWM-SSA
EV-SSA

Conditions:

$\omega_e = 10$ [Hz]
$T^*_{em} = 12$ [n-m]
$\lambda^*_r = 0.5$ [V-s]
$|I^e_{qds}| = 9.5$ [A]
$f_{pwm} = 3$ [kHz]
$T_{sep} = 0.02T_{pwm}$
$f_{sample} = 100$ [kHz]
$f_{fft\text{-}res} = 2$ [Hz]

CVCR Bandwidth:
$\omega_{CVCR} = 100$ [Hz]

Figure 7-10: Synchronous frame harmonic content during steady-state operation using SSA. All magnitudes normalized to the fundamental component.



Legend:

$f_e = 5$ [Hz]
$f_e = 10$ [Hz]
$f_e = 15$ [Hz]

-- EV-SSA
— APWM-SSA

Conditions:

$|I^e_{qds}| = 9.5$ [A]
$f_{pwm} = 3$ [kHz]

Figure 7-11: Change in THD from steady-state operation using the EV-SSA and APWM-SSA.

Simulation results showed that double-update control allows for further improvement in the EV-SSA method regarding the induced distortion. This is verified experimentally in Fig. 7-12 and

7-13. Time domain currents show that error current ripple magnitude decrease while the harmonic spectra shows that harmonic content gets pushed to higher frequencies than in the single-update case.

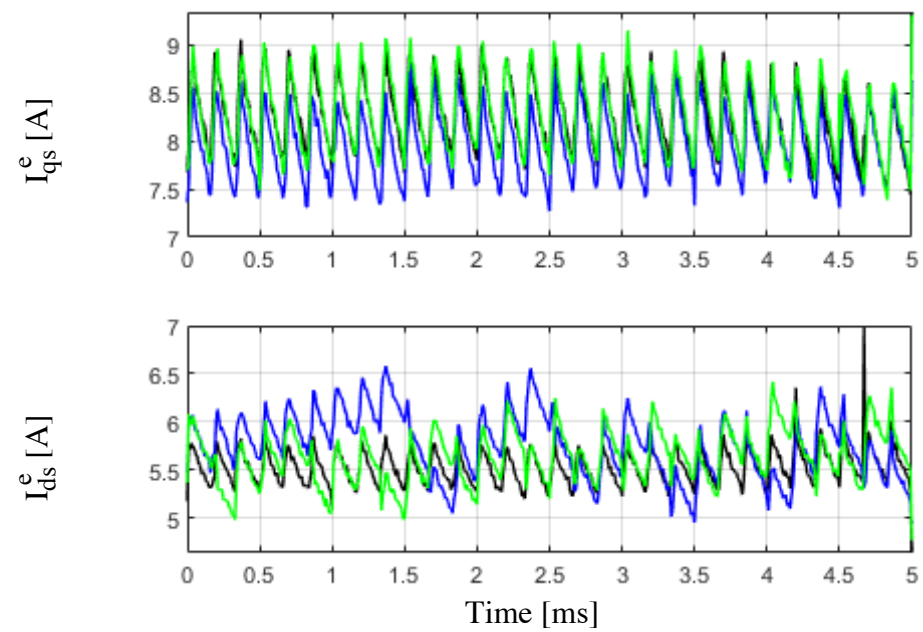


Figure 7-12: Measured current waveforms transferred into the synchronous frame from steady-state operation using the EV-SSA and APWM-SSA.

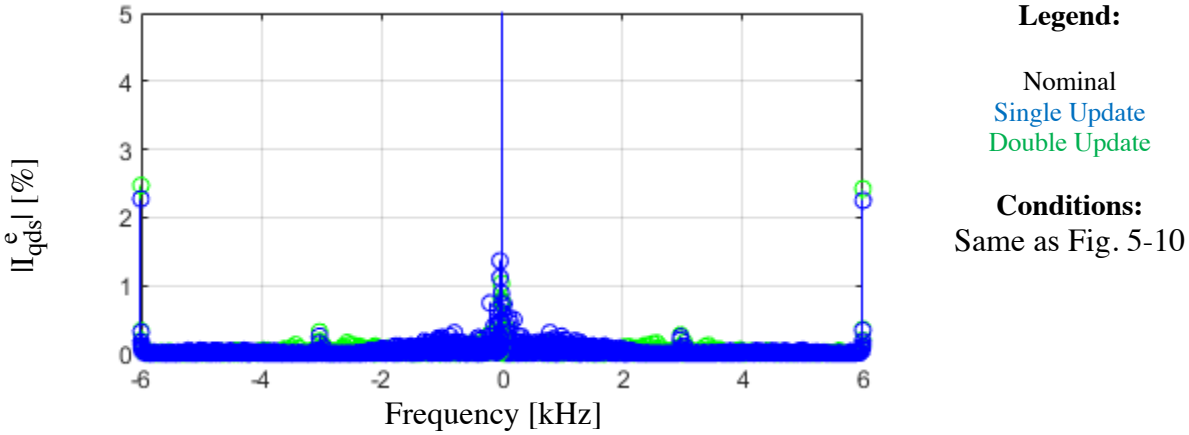


Figure 7-13: Synchronous frame harmonic content during steady-state operation EV-SSA with single-update and double-update control structures.

7.2.3 CVCR Command Tracking with SSA

Fig 7-14 shows command tracking frequency response plots for the CVCR with and without the SSA algorithms operating. This helps to demonstrate that the current regulator's bandwidth or command tracking ability is not impacted by the SSA algorithms. Here it should be noted that the

feedback current, with errors properly decoupled, was used for the EV-SSA case. Fig. 6-15 shows controller-sampled current waveforms during a rated torque step response from motoring to generating. Here, it can be seen that the transient response is left uneffected by the SSA algorithms.

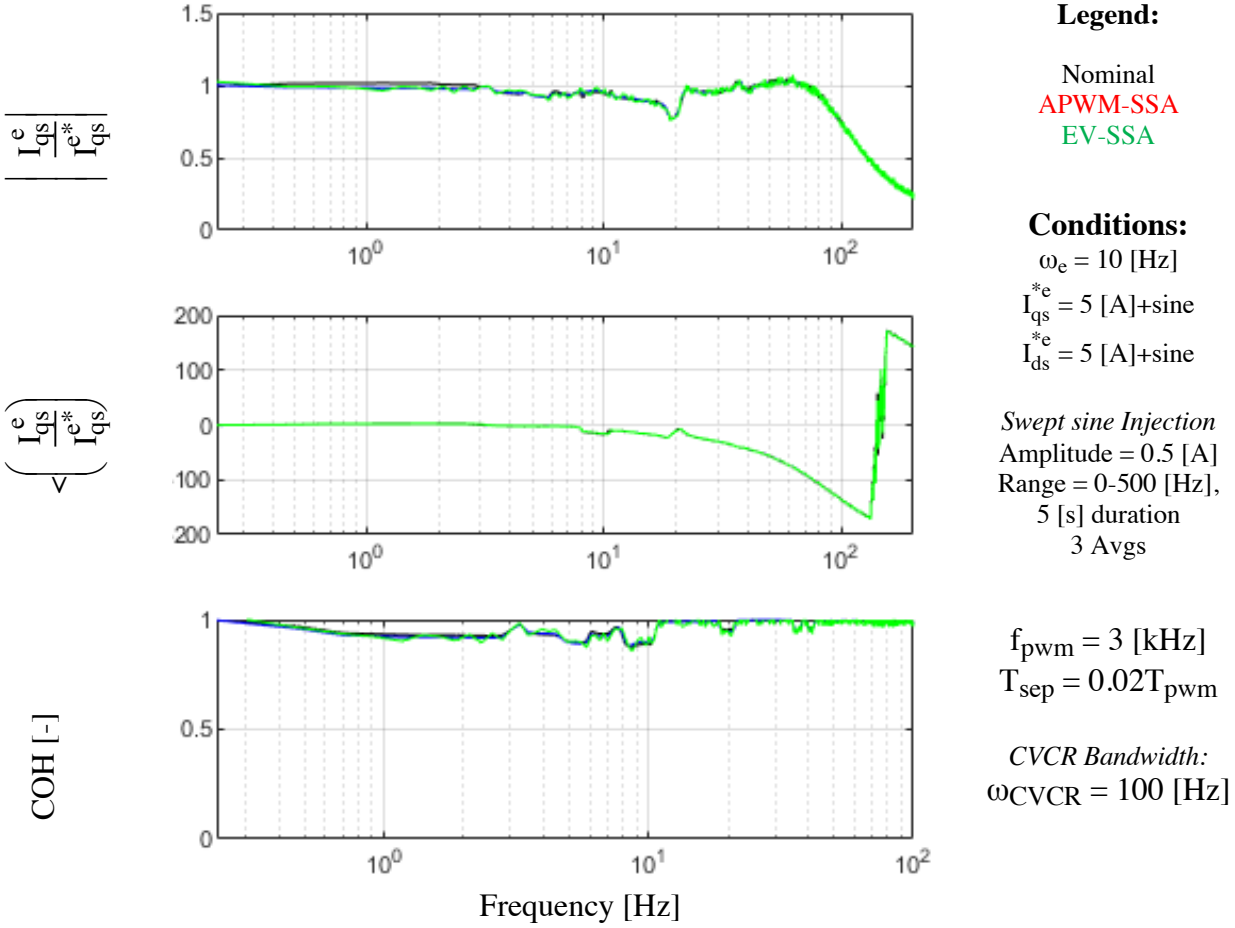


Figure 7-14: CVCR command tracking FRF comparison with and without the proposed SSA algorithms.

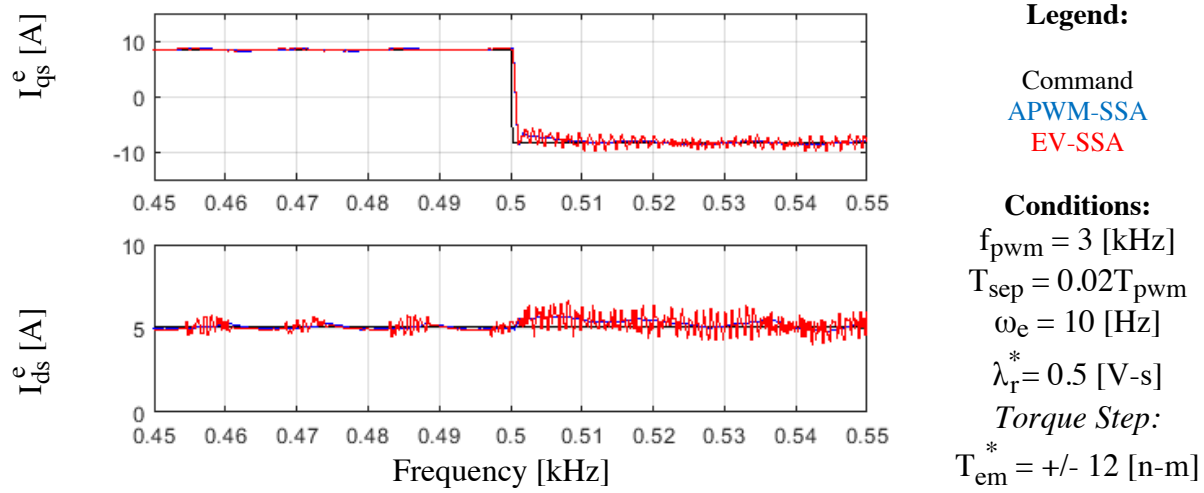


Figure 7-15: Synchronous frame during a rated torque step response using EV-SSA and APWM-SSA.

7.3 Summary

In this chapter, the proposed SSA techniques were implemented together with an IFOC CVCR induction machine drive. Steady-state, step-response, and command tracking tests were carried out to identify the impact of each SSA method on both inverter output distortion as well as current regulation performance.

Time-domain current waveforms during steady-state operation show that both methods perform similarly to results from simulation. The APWM-SSA method produces larger, higher-frequency ripple in the current waveforms. However, little deviation from the nominal case is seen at each sampling instant, since the inverter's voltage command is not altered. The EV-SSA method produces a lower-frequency current ripple and does error into the sampled-current waveform. However, the proposed open-loop compensation method effectively decouples this current error from the CVCR's feedback. The current harmonic spectra produced by each method also agree with results from simulation, where the APWM-SSA method produces concentrated peaks in harmonic content at half-multiples of the switching frequency while EV-SSA produces more distributed harmonic content. Moreover, APWM-SSA resulted in slightly higher THD in the measured output current. Finally, step-response and swept-sine command tracking tests show that

the SSA methods have little to no impact on the tuned bandwidth of the CVCR or torque command step responses.

Chapter 8 Simultaneous Switching Avoidance Considerations for n-Phase Converter Systems

In this chapter, the error-vector and asymmetric-PWM simultaneous switching avoidance methods are examined as possible solutions for creating simultaneous switching avoidance algorithms in n-phase converter systems. First, the specific example of a two, three-phase inverter system is used and the potential SSA algorithm approaches are compared and contrasted. This is then extended to an arbitrary, n-phase converter system. Finally, the implementation complexity of these simultaneous switching avoidance approaches are contrasted with that of a mitigation approach using active gate drive techniques.

8.1 Multiple Three-Phase Converters Sharing a DC Bus

Given its widespread use in the off and on-highway vehicle industries, as well as in industrial applications, the dual-inverter topology provides a relevant example case for examining how SSA methods can be extended to multi-phase converter systems. This also serves as an example of how SSA algorithms can be developed by taking into consideration the relevant operating space of each converter phase, or group of phases, and the available degrees-of-freedom for manipulating switching instances within the system's control schemes.

8.1.1 Error-Vector Inter-Inverter Simultaneous Switching Avoidance

To use the error-vector approach for performing inter-inverter SSA, regions of inter-inverter simultaneous switching must be defined so that they can be avoided. Unfortunately, unlike the intra-inverter case, these regions do not map statically onto the voltage hexagon of either inverter. Rather, they become a function of the respective voltage command vectors for each inverter. For the inter-inverter case, there are nine potential simultaneous switching conditions that can occur, as outlined in (8.1-1) to (8.1-3).

To illustrate how manifests on an inverter's operating space, Fig ? shows regions of inter-inverter simultaneous switching mapped onto Inverter 2's linear operating region for different Inverter 1 command vectors. Regardless of the hexagon sector it is operating in Inverter 2 will have three addition regions that must be avoided to ensure proper switching separation.

To implement an error-vector inter-inverter SSA algorithm in its simplest form, one can let Inverter 1's commands remain unchanged while potential error voltages, $\Delta V_{a\text{-}2}$, $\Delta V_{b\text{-}2}$, and $\Delta V_{c\text{-}2}$, are considered for each phase of Inverter 2. This three-dimensional error voltage vector, $\Delta V_{abc\text{-}2}$, must be chosen so that no overlaps occur between three phases in each inverter, defined by nine equalities of the form shown in (8.1-4). I addition, $\Delta V_{abc\text{-}2}$ must be chosen so that no new intra-inverter simultaneous switching events are created in Inverter 2. Thus (8.1-5) through (8.1-6) must be included in the selection process as well.

This results a set of twelve inequalities that must be satisfied based on three independent variables. Clearly there is no closed-form solution for choosing $\Delta V_{abc\text{-}2}$ as a function of $V_{abc\text{-}1}$ and $V_{abc\text{-}2}$. This problem can be posed as a constrained optimization problem by adding where the magnitude of $\Delta V_{abc\text{-}2}$ is to be minimized in order to minimize the resulting current error produced. A block diagram example of such an algorithm is shown in Fig ?.

Defining this optimization problem in a way that can be solved in real time by an embedded controller presents a significant challenge. Alternatively, one could solve this offline across the entire operating space of each inverter. However, this would require storing a six-dimensional array (one for each converter phase) of $\Delta V_{abc\text{-}2}$ with sufficient resolution ensure satisfactory behavior, presenting a high demand on available memory. Moreover, optimal values of $\Delta V_{abc\text{-}2}$ will be a discontinuous function of $V_{abc\text{-}1}$ and $V_{abc\text{-}2}$, so ensuring interpolation properly avoids simultaneous switching is an additional challenge that would require extensive testing and tuning, based on the desired separation requirements.

$$(V_{a\text{-}1} = V_{a\text{-}2}) \text{ or } (V_{a\text{-}1} = V_{b\text{-}2}) \text{ or } (V_{a\text{-}1} = V_{c\text{-}2}) \qquad (8.1\text{-}1)$$

$$(V_{b\text{-}1} = V_{a\text{-}2}) \text{ or } (V_{b\text{-}1} = V_{b\text{-}2}) \text{ or } (V_{b\text{-}1} = V_{c\text{-}2}) \quad (8.1\text{-}2)$$

$$(V_{c\text{-}1} = V_{a\text{-}2}) \text{ or } (V_{c\text{-}1} = V_{b\text{-}2}) \text{ or } (V_{c\text{-}1} = V_{c\text{-}2}) \quad (8.1\text{-}3)$$

$$\text{abs}(V_{x\text{-}1} - V_{y\text{-}2} + \Delta V_{x\text{-}2} - \Delta V_{y\text{-}2}) > V_{sep} \quad (8.1\text{-}4)$$

$$\text{abs}(V_{a\text{-}2} - V_{b\text{-}2} + \Delta V_{a\text{-}2} - \Delta V_{b\text{-}2}) > V_{sep} \quad (8.1\text{-}5)$$

$$\text{abs}(V_{a\text{-}2} - V_{c\text{-}2} + \Delta V_{a\text{-}2} - \Delta V_{c\text{-}2}) > V_{sep} \quad (8.1\text{-}6)$$

$$\text{abs}(V_{b\text{-}2} - V_{c\text{-}2} + \Delta V_{b\text{-}2} - \Delta V_{c\text{-}2}) > V_{sep} \quad (8.1\text{-}7)$$

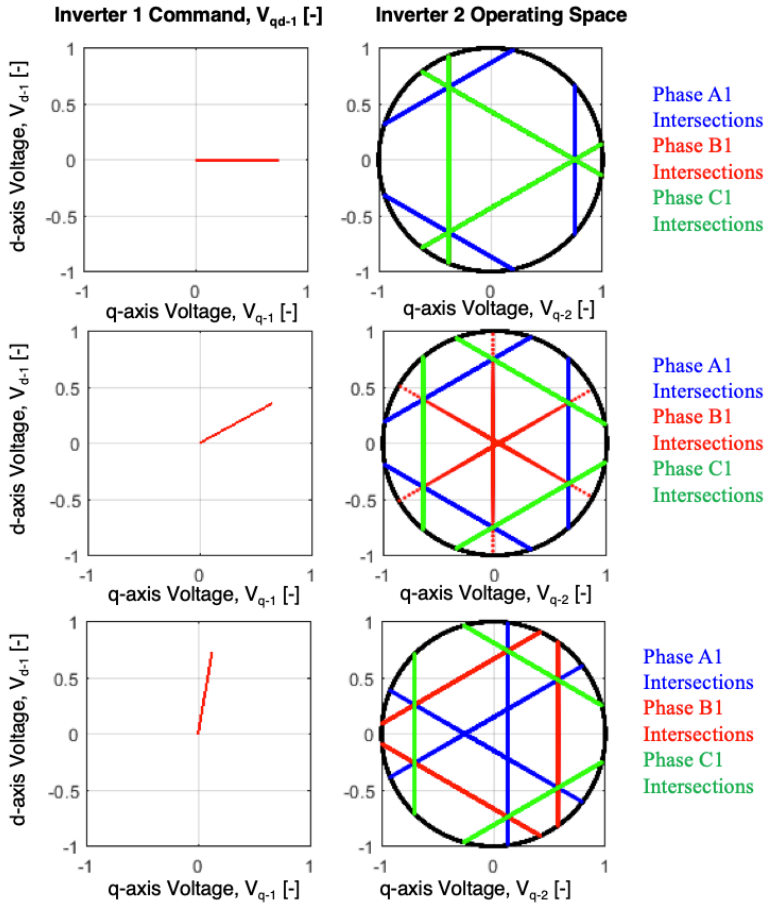


Figure 8-1: Example of inter-inverter switching on Inverter 2's linear operating space (right column) as a function of Inverter 1's command vector (left column)

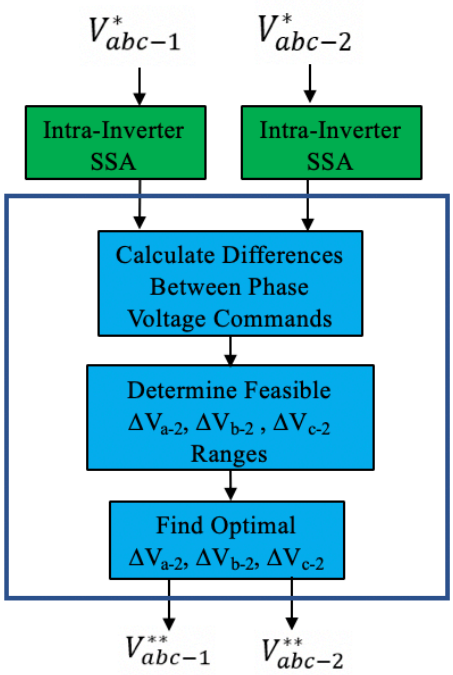


Figure 8-2: Example block diagram of an inter-inverter SSA algorithm using an error-vector-based approach.

8.1.2 Asymmetric-PWM-Based Inter-Inverter SSA

PWM asymmetries provides a second approach for performing inter-inverter SSA. Unlike the Error-vector-based approach, if this route is taken, then intra and inter-inverter SSA do not need to be performed separately. Rather, each phase can be adjusted independently and SSA for the entire converter system can be performed all at once (Fig ?). However, like in Section 8.1.1, regions of simultaneous switching will dynamically change as a function of each inverter's command vector and thus simple operating-space mapping cannot be easily used for selecting how asymmetries should be introduced.

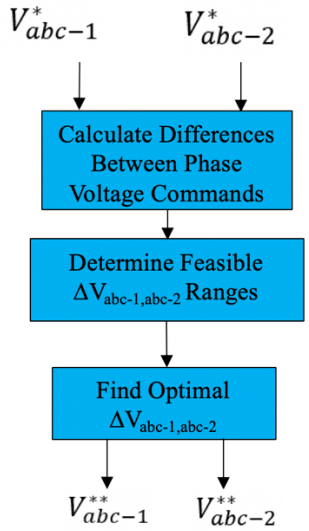


Figure 8-3: Example block diagram of an intra + inter-inverter SSA algorithm using an asymmetric-PWM-based approach.

One can use (8.1-1) through (8.1-3), defining inter-inverter simultaneous switching conditions, combined with (8.1-8) and (8.1-9) that define intra-inverter simultaneous switching to define the overall SSA problem. Because the asymmetric PWM approach works by balances voltage errors in the first and second halves of the PWM period, this set of equations must be doubled to accurately capture the potential for simultaneous switching events in both the first and second halves of the PWM period.

Generating the necessary constraints that define the acceptable solution space, one is left with thirty inequalities that must be satisfied. (8.1-10) and (8.1-11) provide generic example of the eighteen inter-inverter constraint inequalities for the first and second halves of the PWM period, respectively. In addition, the intra-inverter simultaneous switching constraints will provide six additional inequalities per inverter for a total of twelve intra-inverter constraints. These thirty equations in total should be satisfied in a way that minimizes the magnitude of the introduced asymmetries. All together this constrained optimization problem consists of thirty constraints and six independent variables that can be adjusted to achieve SSA. Clearly, the complexity of this proposed approach is worse than the error-vector approach and will suffer from the same implementation issues to an even greater degree.

$$(V_{a\text{-}1} = V_{b\text{-}1}) \text{ or } (V_{a\text{-}1} = V_{c\text{-}1}) \text{ or } (V_{b\text{-}1} = V_{c\text{-}1}) \quad (8.1\text{-}8)$$

$$(V_{a\text{-}2} = V_{b\text{-}2}) \text{ or } (V_{a\text{-}2} = V_{c\text{-}2}) \text{ or } (V_{b\text{-}2} = V_{c\text{-}2}) \quad (8.1\text{-}9)$$

$$\text{abs}(V_{x\text{-}1} + \Delta V_{x\text{-}1} - V_{y\text{-}2} + \Delta V_{y\text{-}2}) > V_{sep} \quad (8.1\text{-}10)$$

$$\text{abs}(V_{x\text{-}1} - \Delta V_{x\text{-}1} - V_{y\text{-}2} - \Delta V_{y\text{-}2}) > V_{sep} \quad (8.1\text{-}11)$$

It is possible to make some algorithm simplifications based on where the system is within the two-inverter operating space. First, one can observe that the only time all six inverter phases can have overlapping switching instances is if both inverters are operating at the origins of their voltage hexagons. In this space, all duty cycle commands will be close to 50% and one can generate a simple ad-hoc solution for this operating region. In a similar vein, when both inverters are operating near sector boundaries and their command magnitudes are similar, there will be a set of four overlapping phase commands and a set of two overlapping phase commands. Once again, an ad-hoc SSA solution can be developed to handle this particular case as well. Additional overlap cases exist and can be addressed in a similar manner. This can be extended to include as many cases as one chooses.

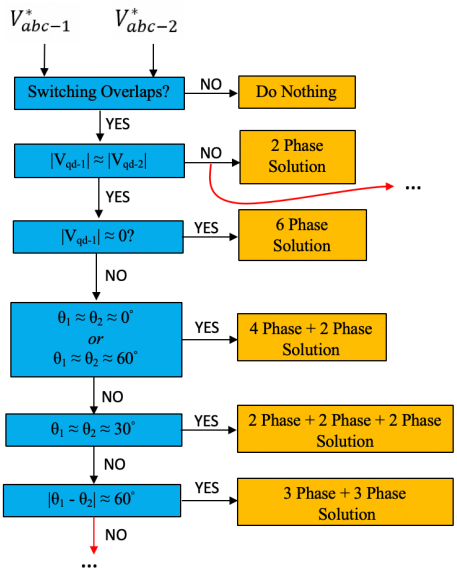


Figure 8-4: Example block diagram of an ad-hoc intra + inter-inverter SSA algorithm using an asymmetric-PWM-based approach.

The primary hurdle of this case-by-case approach, as compared to a mathematically-described optimization problem, is that the boundaries between different overlap cases within the system's operating space must be defined. If this is not done properly, the chosen ad-hoc solution may generate new overlapping switching instances or by introduce unnecessarily large asymmetries. The latter will cause undesirable increases in output distortion due to the inserted asymmetry. This can be mitigated to a certain extent by adding more cases to the algorithm.

At the limit of this exhaustive approach, one can include every single potential combination of phases in the six-phase system. At this point, the system can be treated as an arbitrary six-phase converter as addressed in Section 8.2.1.

8.1.3 Zero-Sequence-Based Inter-Inverter SSA

Zero-sequence voltage provides an additional degree-of-freedom for manipulating switching instances with a PWM period without impacting the average voltage output of a three-phase inverter. As covered in Section 1.2.2 and 1.2.3 and shown in Fig ?, injecting a zero-sequence voltage ΔV_{z1} in Inverter 1 will shift all its switching instances symmetrically towards or away from the midpoint of the PWM period. While this cannot be used to perform intra-inverter SSA, it can be leveraged to shift switching instances of Inverter 1 and 2 with respect to one another. Thus, one can define a relative zero-sequence voltage injection, $\Delta V_{z\text{-}rel}$, as a single degree-of-freedom for performing inter-inverter SSA (8.1-12). Moreover, variations in zero-sequence voltage have significantly less impact on inverter output distortion as compared to asymmetric PWM techniques [14, 85].

This zero-sequence-based Inter-Inverter SSA approach can be implemented together with either APWM-SSA or EV-SSA. For single-update EV-SSA it only needs to be performed once per switching period while APWM-SSA and double-update EV-SSA require that it be performed twice, once for each half of the switching period.

$$\Delta V_{z\text{-}rel} = \Delta V_{z1} - \Delta V_{z2} \tag{8.1-12}$$

Like in Section 8.1.1 and 8.1.2, a set of nine inter-inverter SSA inequalities can be used to constrain the selection of $\Delta V_{z\text{-}rel}$ so that inter-inverter switching overlaps are avoided. This given by (8.1.14) in a generic form. These constraints can be mapped onto a number line representing the range of possible $\Delta V_{z\text{-}rel}$ values. This is shown in Fig. ? where V_a, V_b, and V_c have been sorted into V_{max}, V_{mid}, and V_{min} to make the representation independent of the hexagon sector that each inverter is operating within. Each region shown in red is centered on a value of $\Delta V_{z\text{-}rel}$ that will cause simultaneous switching between one phase from Inverter 1 and one phase from inverter 2. The width of these red regions is simply $2V_{sep}$. Thus, all regions in green indicate acceptable values of $\Delta V_{z\text{-}rel}$ for inter-inverter SSA. The limit of $\Delta V_{z\text{-}rel}$, (+/-) $\Delta V_{z\text{-}rel,Max}$, is defined by (8.1.15).

$$\text{abs}(V_{x\text{-}1} - V_{y\text{-}2} + \Delta V_{z\text{-}rel}) > V_{sep} \tag{8.1-14}$$

$$\Delta V_{z\text{-}rel,Max} = V_{DC} - V_{max\text{-}1} - V_{max\text{-}2} - 2V_{sep} \tag{8.1-15}$$

With the solution space clearly defined, one simply needs to form an algorithm for selecting $\Delta V_{z\text{-}rel}$ from the range of possible values. This can be posed as a constrained optimization problem where the goal is minimizing $\Delta V_{z\text{-}rel}$. While not always true (see Section 1.2.3), minimizing the deviation in zero-sequence voltage will minimize the resulting impact on output distortion. This could potentially be performed in real-time using a guess-and-check approach where the magnitude of $\Delta V_{z\text{-}rel}$ is gradually increased and both positive and negative values are checked to see if proper inter-inverter SSA is achieved. No such selection algorithm has been developed in this work. Once again, this could be solved offline and a four-dimensional array of solutions could be stored in memory. This will present a pair of challenges in choosing the look-up table resolution and the method used for interpolating between points in a highly-discontinuous solution set.

An alternative approach would be to develop ad-hoc $\Delta V_{z\text{-}rel}$ selection methods depending on command vectors for each inverter. This approach is identical to the ad-hoc approach shown in 8.1.2 and will be subject to the same trade-offs. The number of calculations required of the controller can be reduced by reducing the number of solution cases added to the algorithm.

However, reducing the number of solution cases will reduce the optimality of the overall inter-inverter SSA algorithm. In addition, this approach will require extensive testing and tuning of the conditions used to transition between solution cases.

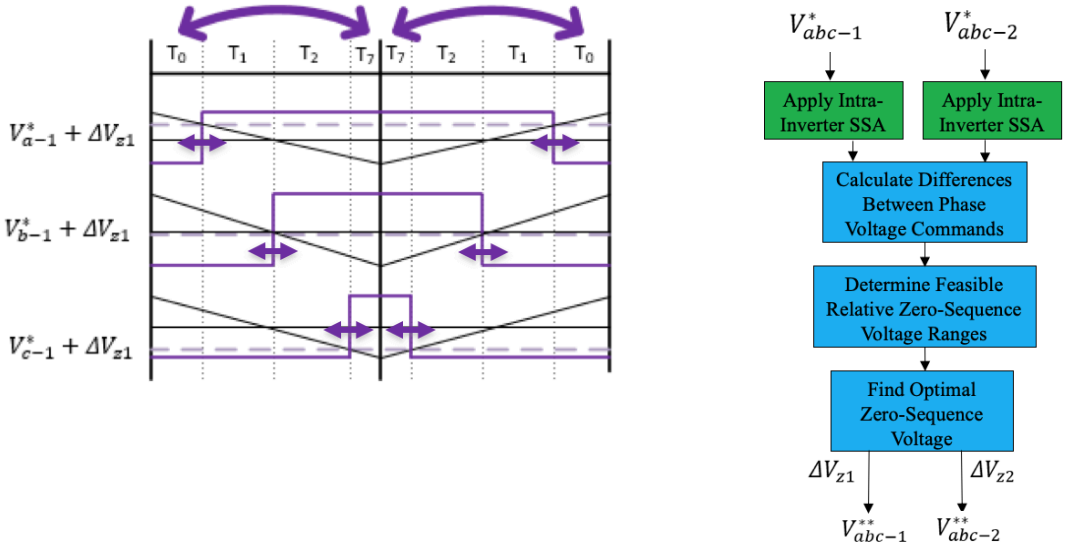


Figure 8-5: Example of switching transient timing adjustment through zero-sequence voltage injection into the three-phase voltage command vector (left) and an example block diagram for performing zero-sequence-based inter-inverter SSA .

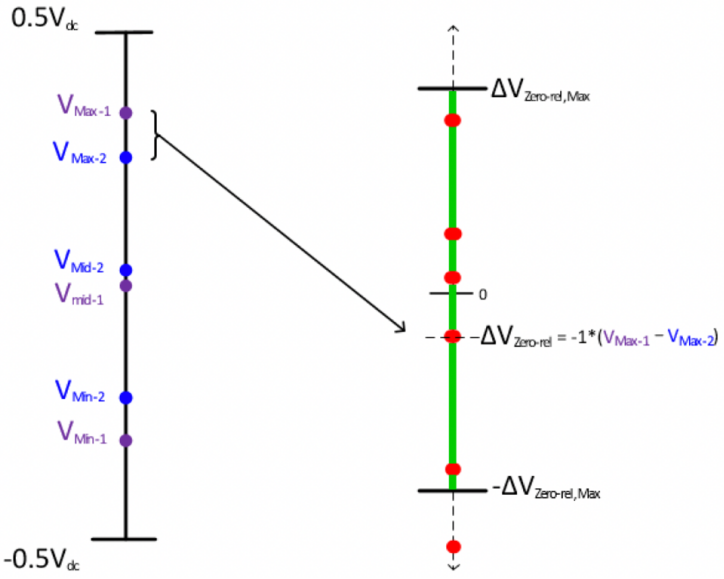


Figure 8-6: Defining the range of acceptable $\Delta V_{z\text{-}rel}$ values for performing zero-sequence-based Inter-Inverter SSA.

8.2 Simultaneous Switching Avoidance for n-Phase Converters

As demonstrated for the example case of a system consisting of two, three-phase inverters, both error-vector and asymmetric-PWM approaches can be used to design SSA solutions for a particular system. Further, both can be developed in one of two ways: constrained optimization or through ad-hoc algorithm development. Unlike the system used in Section 8.1, an arbitrary n-phase converter does not provide the option of using zero-sequence voltage injection as a solution approach. The exception to this general rule would be any system that contains a subsystem of converter phases that whose outputs share a common, floating, neutral point.

8.2.1 Error-Vector SSA

Extending the error-Vector SSA algorithm to the arbitrary converter case, constraint equations of the same generic form as shown in 8.1.1 can be used (8.2-2). Here, the number of constraint equations will grow with the number of converter phases, n (8.2-1). To satisfy these constraints, an n-by-1 array of independent variables can be manipulated (8.2-3). As discussed previously, this could be solved as a constrained optimization problem or using an ad-hoc case-by-case approach. These will have the same previously-discussed implementation issues as the number of converter phases increases.

If the ad-hoc approach is chosen, the number of unique simultaneous switching cases that the SSA algorithm will potentially need to address grows at an accelerating pace as the number of converter phases increases. (8-9). An example of all possible cases for a six-phase converter system is shown in Fig 8-8. All of these cases may not be necessary, depending on the operating space and parasitic inductance distribution of a given system. Never-the-less, one will need to define logic for properly distinguishing between these cases in a manner that ensures no new harmful simultaneous switching events are produced in the attempt to perform SSA.

Finally, the impact on EV-SSA on the converters available operating space is demonstrated in Fig 8-9 and expressed in (8.2-4). This equation expresses the maximum (or minimum) phase voltage commands that can be achieved before running into the converters DC bus voltage limits.

Here, it is assumed that the errors introduced in Fig 8-9 will be equal and opposite for each converter phase in the next switching cycle. If any of the phase voltage commands exceed $V_{limit,SSA}$, one could simply reduce all voltage commands until sufficient separation can be achieved. However, compensating for this error in the subsequent switching period may require exceeding this voltage limit once again, leading to a cycle where voltage error compensation cannot be adequately achieved.

$$\text{Constraints} = \frac{n!}{2(n-2)!} \tag{8.2-1}$$

$$\text{abs}(V_1 - V_2 + \Delta V_1 - \Delta V_2) > V_{sep} \tag{8.2-2}$$

$$\Delta V = \{\Delta V_1, \Delta V_2, \ldots, \Delta V_n\} \tag{8.2-3}$$

$$V_{limit,SSA} = 0.5V_{DC} - \left(\frac{n-1}{2} + 1\right)V_{sep} \tag{8.2-4}$$

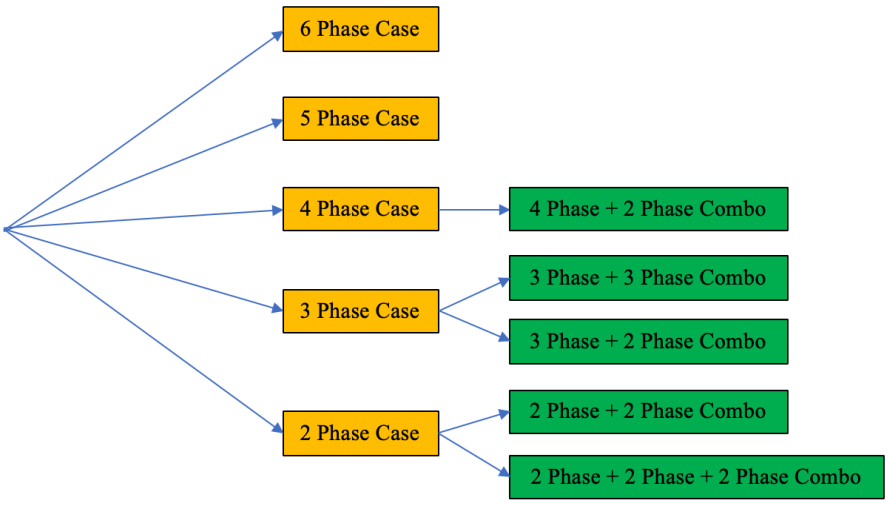


Figure 8-7: Example of all the possible switching overlap cases for a six-phase converter system

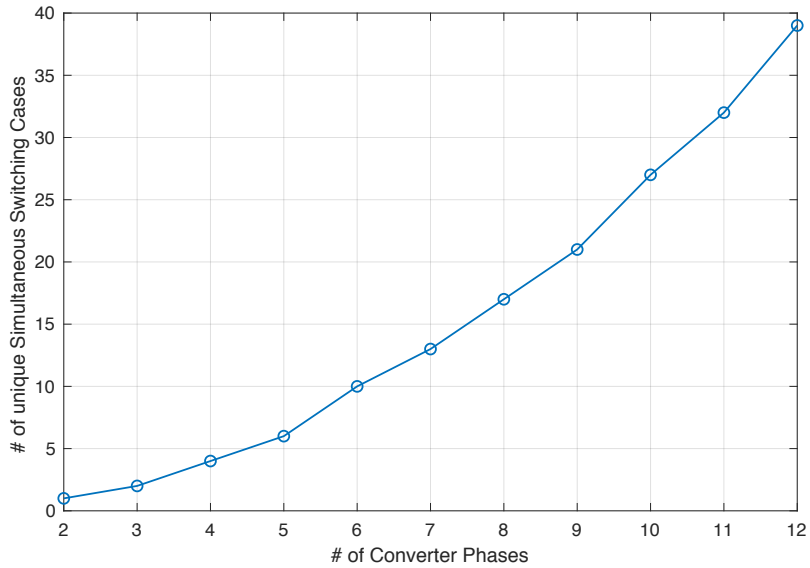


Figure 8-8: Number of distinct algorithm cases needed to handle all possible switching overlap combinations as a function of converter phases

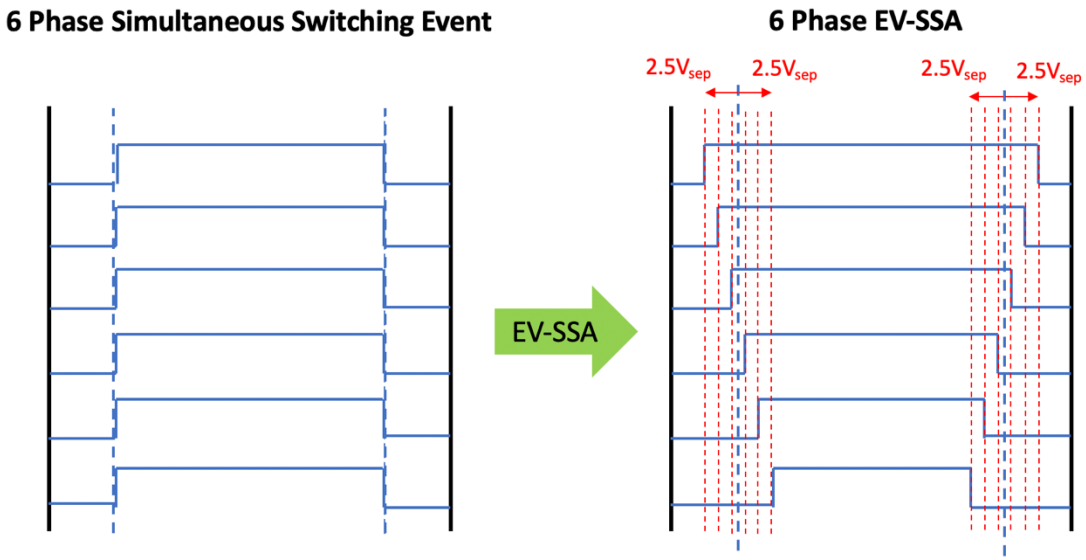


Figure 8-9: Example of all the required space needed to enforce switching separation in a five-phase converter system using the error-vector approach.

Finally, using the error-vector approach will require a voltage error compensation scheme that estimates the resulting load current error and adjusts voltage commands in subsequent switching periods to drive this error to zero. For the arbitrary n-phase converter, a separate compensation scheme will be needed for each converter phase.

8.2.2 Asymmetric-PWM SSA

Moving to the asymmetric PWM approach to SSA, a familiar set of constraint equations can be developed for the arbitrary n-phase converter. Here, the number of constraint equations doubles as compared to the EV-SSA approach because SSA must be enforced for both halves of the PWM period. So from an optimization approach, the problem becomes significantly more difficult to solve compared to the EV-SSA approach. However, using an ad-hoc case-by-case approach to algorithm development, the same number of cases will exist for a given n-phase converter. In addition, its impact on available converter operating space remains the same (Fig 8-10).

$$\text{Constraints} = \frac{n!}{(n-2)!} \tag{8.2-4}$$

$$\text{abs}(V_1 - V_2 + \Delta V_1 - \Delta V_2) > V_{sep} \tag{8.2-5}$$

$$\text{abs}(V_1 - V_2 - \Delta V_1 + \Delta V_2) > V_{sep} \tag{8.2-6}$$

$$\Delta V = \{\Delta V_1, \Delta V_2, \ldots, \Delta V_n\} \tag{8.2-3}$$

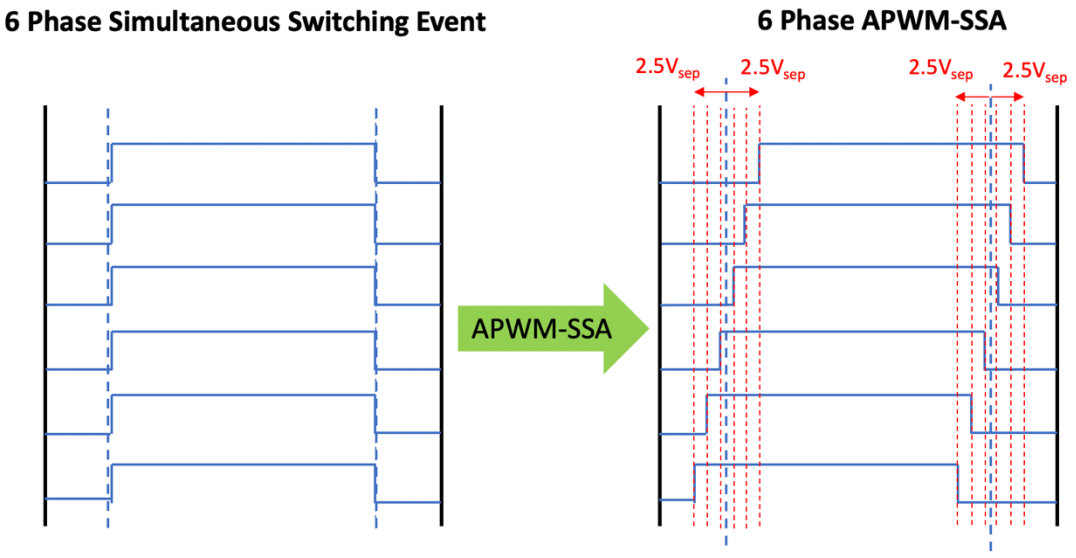


Figure 8-10: Example of all the required space needed to enforce switching separation in a three-phase converter system using the asymmetric PWM approach.

Finally, the APWM-SSA approach will not require any modification to the closed-loop control scheme as is needed in the EV-SSA approach because the average voltage sourced by the converter each switching period remains unchanged. This is a benefit of simplifying closed-loop control design of the converter's outputs. However, asymmetric PWM will inherently lead to larger converter output distortion as compared to EV-SSA. Moreover, it is inherently incompatible with double-update control architecture, placing a limit on the achievable control bandwidth for a given switching frequency.

8.3 Active Gate Drive Solutions for Mitigating Simultaneous Switching Effects

Section 1.1.6 shows that active gate drives can be employed to mitigate the impacts of simultaneous switching events on voltage stress and switching losses. While the experimental results shown in [12] and [13] indicate that switching stresses do not return to their single-phase transient levels, a significant reduction can be gained. With this in mind, it is beneficial to consider this hardware-based approach in contrast to the software-based SSA approach.

For the active gate drive circuitry to automatically respond to simultaneous switching events, it must be of the closed-loop variety. That is, device terminal voltages must be sensed and fed back to the gate drive circuit so that the switching transient speed can be adjusted accordingly. In [12] and [13], this was done in conjunction with di/dt feedback to form the active gate drive solution.

Given switching speeds on the order of 5 to 50 [ns] in modern power devices, closed-loop active gate drives require analog control circuitry to avoid timing delays introduced by A/D and D/A conversion in the control loop. This introduces a few new challenges into the design process.

First, the performance of these analog control circuits must be tested across the range of simultaneous switching conditions they are required to handle and control loops must be tuned to robustly handle this range of operating conditions. Second, closed loop gate drive circuitry drives up the complexity, cost, and physical size of the converter design. For example, [30] indicates that the required op-amps, multiplexers, reference generators, and passive components needed to form an analog closed-loop gate drive for di/dt and dv/dt control for a single phase leg occupied roughly

10 [in^2] of PCB space and significantly increased the part count of the gate drive design from a simple passive-resistive gate drive. Finally, these analog control circuits can be susceptible to noise and cross-talk due to switching transients in other converter phases. All these challenges can certainly be overcome, as shown by [12, 13, 30]. However, off-the-shelf solutions for this closed-loop gate drive control do not currently exist.

While open-loop active gate drives are inherently incapable of responding to simultaneous switching events autonomously and effectively, the emergence of open-loop active gate drive ICs [86, 87] present an opportunity for coordination between to address simultaneous switching events. In these off-the-shelf solutions, the motor control DSP or FPGA providing gate drive signals can also provide a command to select a desired switching speed level. These are then used by the gate drive IC to select between possible gate voltage levels to speed up or slow down the switching transient.

This ability to dynamically adjust the switching speed of an open-loop active gate drive provides the possibility of the motor controller to dynamically adjust switching speeds when it detects an upcoming simultaneous switching event. Tuning still needs to be carried out to adjust the timing of the gate voltage profiles and to select appropriate voltage levels for different switching overlap conditions. Further, the open-loop nature of this approach means the gate drive. will be less robust to load current and temperature variations. However, the possibility of leveraging off-the-shelf gate drive hardware simplifies the design process.

While implementing an active gate drive circuit may require extensive testing and tuning of the control loop hardware, this effort does not necessarily scale at the same rate as developing SSA algorithms for increasing numbers of converter output phases. For the case where multiple or all converter phases use the same switching devices, the gate drive control solution can simply be duplicated for each duplicate converter phase. For example, in a three-phase inverter, each phase leg will almost assuredly be constructed with identical switching devices. Thus, a gate drive solution developed for one converter phase should be sufficient for all the others. If a second,

identical three-phase converter is added, the gate drive solution can once again be duplicated to control this new set of converter phases. Conversely, an complexity of an SSA algorithm will continue to grow as the number of converter phases-and the number of possible simultaneous switching cases-increases.

Considering that the implementation complexity of software-based SSA methods increase at an accelerating rate with increasing degradation of the available converter operating space, there will likely exist a cross-over point where developing SSA algorithms is no longer worth the required design effort (Fig 8-9). It is difficult to quantify where this cross-over point is, as it will be dictated by the design requirements and available development resources for a specific application and design team. However, this inherent difference complexity scaling for the two solution approaches should be kept in mind when weighing the two potential design routes.

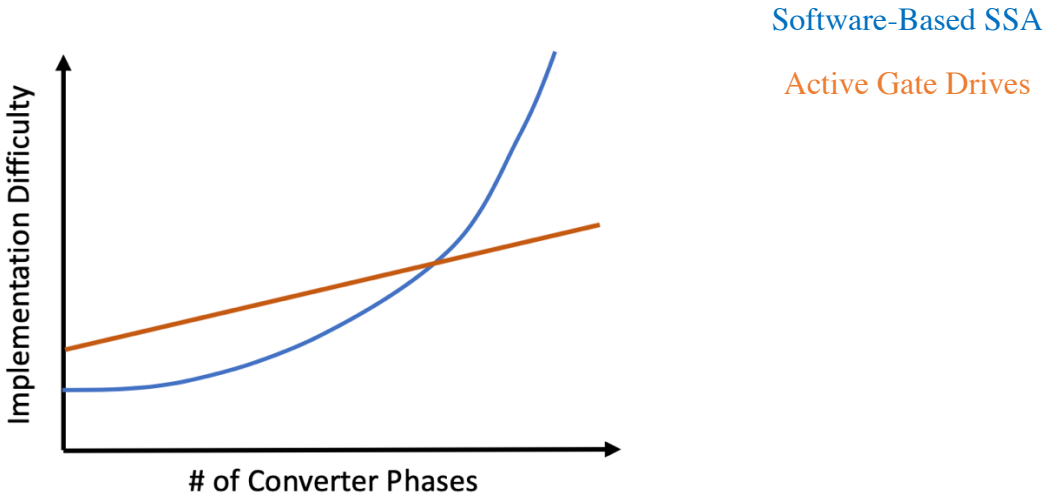


Figure 8-11: Cartoon depiction of the implementation complexity of software-based simultaneous switching avoidance compared to hardware-based active gate drive solutions as the number of converter phases increases

8.4 Commutation loop Design and Decoupling

Regardless of the specific converter topology, simultaneous switching avoidance should always be second to good commutation loop design practices. As shown in Chapter 3, if parasitic inductance is minimized so that the per-unit inductance of each commutation loop is small – say on the order of 5% - than simultaneous switching avoidance will only bring small benefits.

However, even for well-designed commutation loops, the impact of simultaneous switching on required voltage margin will increase as with the common-coupling ratio, R_{cc}, and the number of converter phases, n. So, the severity of simultaneous switching can be kept small by maximizing the amount of decoupling in the DC link commutation loops. In applications where space and cost are not at a premium, this is theoretically not an issue. However, if a compact design is required and the additional space and cost needed for providing adequate decoupling – either through design of busbar geometry or inclusion of decoupling capacitors – then a combined approach of commutation loop design and simultaneous switching avoidance could be leveraged.

As shown in this chapter, performing SSA within a single three-phase inverter is a relatively straight-forward task. Similarly, designing SSA algorithms for groups of two or three converter phases is a relatively simple undertaking. However, designing SSA algorithms for a five or six phase converter rapidly becomes a daunting task. So a circuit designer may choose to group the commutation loops of certain converter phases so that simultaneous switching avoidance only needs to be performed between a certain segment of the converter phases.

Using the two, three-phase converter system as an example, if R_{cc} for all inter-inverter simultaneous switching cases is small – less than 0.2 – than inter-inverter simultaneous switching will cause roughly a 20% increase in voltage overshoot at most. If R_{cc} for intra-inverter simultaneous switching cases is significantly larger, than the proposed intra-inverter SSA techniques can be employed to avoid these more severe simultaneous switching events. In this way commutation loop design and converter output group could provide some flexibility in removing the requirement to include all potential simultaneous switching cases in a SSA algorithm.

8.5 Summary

The methods for performing software-based simultaneous switching avoidance can be extended to arbitrary n-phase converter designs in general. However, the implementation complexity of any SSA algorithm will increase at an accelerating rate as the number of converter phases and required simultaneous switching avoidance cases increases.

One can take two possible approaches for developing the SSA algorithms: constrained optimization or ad-hoc algorithm design. The optimization problem poses a challenge for real-time control systems as the set of “n” or “2n” constraint inequalities are nonlinear functions of the “n” independent variables for manipulated switching instant timing. Further, the resulting solutions will be highly discontinuous across the operating space of a given converter. The ad-hoc design approach may provide a simpler way to implement SSA in software. However, the challenge of this approach will be in defining algorithm logic to ensure the proper avoidance case is selected and no new switching overlap conditions are created. Further, as the number of cases is reduced, the optimality of SSA solution decreases and the impact of SSA on converter output distortion will increase.

For the specific case of a two, three-phase converter system, a third algorithm option is provided through the use of relative zero-sequence voltage injection for inter-inverter simultaneous switching avoidance. This has four primary benefits. First, it is compatible with either intra-inverter SSA method and does not risk the chance of creating new intra-inverter simultaneous switching events regardless of how the algorithm is formed. Second, reduces the number of constraint inequalities to the nine that define inter-inverter switching overlaps. Third, the solution space is reduced to a single degree-of-freedom. Finally, the impact of zero-sequence voltage injection of inverter output distortion is less than that of either APWM-SSA or EV-SSA

Chapter 9 Conclusions, Contributions, and Recommended Future Work

9.1 Conclusions

The following is a summary of the key conclusions made in each chapter:

9.1.1 Simultaneous Switching Analysis and Avoidance in the State-of-the-Art Review

- Parasitic inductance in a DC link commutation loop will produce voltage stresses and increased switching losses in power electronic switching transients.
- When multiple converter outputs share a common DC link, mutual commutation loop inductance will cause di/dt and voltage stress coupling if switched simultaneously.
- This coupling can result in significant increases in peak voltage stresses as well as increases in peak power lost during switching.
- Some hardware-based solutions to this simultaneous switching problem have been proposed, including active gate control as well as gating signal delay circuitry.
- These approaches can increase material cost and could lead to control performance degradation in the case of delay circuitry.
- A previously proposed asymmetric PWM based SSA method, implemented using a modified double-update control structure can be used to perform intra-inverter SSA without altering V_{qd}^{*} from a current or torque controller.
- A variety of symmetrical three-phase PWM methods have been proposed and evaluated in the literature using zero-sequence voltage as the key degree-of-freedom.
- This offers an available degree-of-freedom for performing inter-inverter SSA without impacting V_{qd}^{*}

- Using either current-regulated FOC without any modifications, V_{qd}^{*} can only be indirectly manipulated through flux weakening techniques to alter switching instances independent of torque production.
- Using DB-DTFC, V_{qd}^{*} can be chosen independent of torque using the degree-of-freedom provided in selecting a flux command. In this way, the timing of switching instances could be manipulated independent of torque production.

9.1.2 Simultaneous Switching Transient Waveform Measurement

- Simultaneous turn-off of two IGBTs resulted in increased peak voltage stresses, as expected due increased di/dt through to shared commutation loop inductances.
- These effects are most prominent at high load currents, because the IGBT's turn-off speed, and the resulting di/dt, increases.
- Both peak power losses and total switching loss energy also increased during simultaneous switching transients.
- By introducing approximately 20 [ns], equal to the duration of peak di/dt, the impact of switching transient coupling is effectively nulled between IGBTs tested.
- Simultaneous diode turn-off does not result in comparable increases in either peak voltage stress or losses.
- Unlike the relatively linear effects in the IGBT turn-off case, peak di/dt and resulting voltage stresses quickly saturate as load current increases.
- Because the diode turn-off contains regions of both positive and negative di/dt, certain asynchronous switching transients can result in cancellation of di/dt through the shared commutation loop path.
- These asynchronous turn-off transients can produce increases in switching losses for the delayed diode, due to increased blocking voltage during the transient.

- Similarly, asynchronous turn-off of an IGBT and diode can produce either amplification or cancellation of di/dt in the DC link. This can cause increased losses in either the IGBT or diode, depending on the relative timing of each transient.
- For all cases, coupling between switching transients is eliminated once regions of high di/dt are sufficiently separated. This was only 20 [ns] for the IGBT and 40 [ns] for the diode.

9.1.3 Simplified Modeling of Simultaneous Switching Coupling Effects

- Simple, undamped inductive and inductive-capacitive commutation loop models can be used together with simple ramp or exponential current transient models to estimate peak voltage overshoot in single phase converter circuits.
- These modeling approaches, while only providing rough estimates of voltage overshoot, require little prior knowledge of circuit parameters and are thus easily applicable to the concept-phase of a design process.
- Extending these to simultaneous switching events the impact of common coupling inductance ratio, R_{CC}, will increase voltage overshoot by a factor of roughly $1 + R_{CC}$.
- These models are broadly applicable to both Si IGBT and SiC MOSFET circuits. However, care should be taken to consider the unmodelled impact of effective increases in commutation loop inductance during simultaneous switching on peak rates of di/dt.
- Extending these models to decoupling capacitor considerations, simultaneous switching events will increase the required decoupling capacitance by a factor of $\sqrt{1 + R_{CC}}$ if peak overshoot is to remain the same.
- Per-unit switching transient modeling can be used to compare the impact of switching speed and parasitic inductance distribution on required design voltage margin for withstanding simultaneous switching events. This margin will scale at a rate of $(1 + R_{CC})L_{PU}$.
- For small values L_{PU} (large base inductance or small physical inductance) simultaneous switching avoidance will provide little benefit in reducing voltage margin requirements.

- As L_{PU} and R_{CC} increase, SSA may reduce voltage margin requirements, allowing circuit designers to increase DC Bus voltage levels for increased system performance or to use devices with lower blocking voltage ratings leading to a reduced system cost.

9.1.4 Probability of Simultaneous Switching in Three-Phase Inverters

- For any non-zero value of T_{sep}, there will be a non-zero probability of simultaneous switching occurring, for both the intra and inter-inverter overlap cases.
- For both cases, this probability is a function of $|V_{qd}|$ and T_{sep} and is not a function of ω_e.
- For inter-inverter simultaneous switching, the probability is dependent upon the zero-sequence-voltage, or zero-state partition used in each inverter.

9.1.5 Error-Vector Intra-Inverter SSA Algorithms

- The APWM-SSA method developed previously presents control limitation due to its incompatibility with conventional double-update PWM and additional zero-sequence voltage injections after APWM-SSA has been performed.
- By relaxing the requirement that the inverter's average output voltage remains unchanged, an EV-SSA method is developed that eliminates the need for asymmetric PWM techniques.
- Because EV-SSA introduces $\Delta V_{qds\text{-}error}^{s}$ into the inverters output, compensation must be performed to decouple the effect of $\Delta I_{qds\text{-}error}^{s}$ on current regulator performance and to eliminate residual $\Delta I_{qds\text{-}error}^{s}$ when EV-SSA is not active.
- Open-loop, voltz-per-hertz simulations of the APWM-SSA and EV-SSA methods show that each method has different impacts on inverter output distortion.
- The APWM-SSA approach does not cause any current error at the end of each PWM period but results in large PWM current ripple caused by the necessary asymmetries for cancelling voltage error.
- The EV-SSA approach does cause current error at the end of certain PWM periods. However, PWM ripple is not increased because classical SVPWM can be used.

- APWM-SSA produces concentrated current harmonic content at half-multiples of the switching frequency whereas the EV-SSA approach produces a more distributed current harmonic spectrum, appearing mostly below the switching frequency.
- EV-SSA produces slightly lower increases in THD compared to APWM-SSA.
- Both methods produce exponentially increasing THD as T_{Sep} increases.
- The impact on THD decreases for both methods as f_e increases.
- Leveraging EV-SSA's ability to operate in a conventional double-update manner, THD can be reduced as compared to the single-update case and the harmonic content can be distributed across an even larger range of frequencies.

9.1.6 Compensation of Deadtime Effects for SSA

- When compensating for current-dependent inverter output non-linearities with SSA methods, compensation for voltage drops and deadtime-induced errors should be separated out.
- To ensure the switching instances enforced by SSA, which assumes ideal inverter switching, are achieved, deadtime compensation should be performed after SSA.
- Using this approach, current-polarity-dependent deviations in commutation timing can be systematically reduced when load current magnitude is sufficiently greater than 0 [A].
- This mitigation of commutation timing deviations reduces the required separation time that SSA must enforce to ensure switching transients do not overlap.

9.1.7 Evaluation of CVCR Performance with Intra-Inverter SSA Algorithms

- The proposed intra-inverter SSA algorithms enforce the desired switching separation under closed-loop control and utilizing proper deadtime effect compensation
- Proper switching separation was found to decrease both amplitude and duration of voltage oscillations during switching transients, as seen on the phase voltage outputs.
- Operating under steady-state conditions, the impact of both intra-inverter SSA methods on current harmonic content was qualitatively similar to simulation results.

- Step-response tests and command tracking FRFs show that current regulator bandwidth and/or stability are not noticeable impacted by either intra-Inverter SSA method.

9.1.8 Considerations for SSA Algorithms in n-Phase Converter Systems

- In general, either EV-SSA or APWM-SSA methods can be extended to n-phase converter systems.
- However, as the number of converter phases increases the complexity of a SSA algorithm increases at an accelerating pace due to the increase number of possible simultaneous switching combinations.
- Either EV-SSA or APWM-SSA can be posed as a constrained optimization problem. However, solving the required set of constraint inequalities is a challenging task for real-time control applications.
- These optimization problems could be solved offline and solutions stored in n-dimensional look-up tables. However, this introduces two design challenges: selecting adequate lookup-table resolution and developing interpolation algorithms for properly coping with the discontinuous solution space.
- SSA algorithms can also be developed in an ad-hoc, case-by case, basis. Each relevant simultaneous switching combination can be addressed in a manner that is unique to the particular case.
- Ad-hoc solutions can leverage knowledge of a particular converters' commutation loop design and operating space to address only the simultaneous switching events that are most significant.
- the number of possible required ad-hoc solution cases increases as the number of converter phases increases and the required logic for differentiating between cases increases in complexity.

- For the specific case of a two, three-phase converter system relative zero-sequence voltage injection provides a third route for performing inter-inverter SSA and is inherently compatible with any intra-inverter SSA algorithm.
- Relative zero-sequence voltage injection reduces the number of necessary contsraints to 9 while also requiring only one independent variable for choosing a solution.
- Zero-sequence voltage injection produces significantly will introduce significantly less distortion than either EV-SSA or APWM-SSA.

9.2 Contributions

This work offers a framework for developing control techniques that mitigate the impact of simultaneous switching transients by systematically avoiding their occurrence.

- Identification and evaluation of load and separation dependent switching transient effects on peak voltage stress, di/dt, and switching losses for a two-phase IGBT-based inverter that can be used to inform the design of SSA techniques.
- Methodologies for performing simplified switching transient modeling to identify switching speed, parasitic inductance, and voltage margin trade-offs including simultaneous switching effects for IGBT and MOSFET circuits.
- Methodologies for analyzing the probability of intra and inter-inverter simultaneous switching occurrence under steady-state operation.
- Methodologies for performing intra-inverter simultaneous switching avoidance by appropriately manipulating current regulator output voltage through EV-SSA.
- Methodologies for appropriately compensating for deadtime-induced commutation timing errors in the context of SSA.
- Integration and experimental evaluation of SSA algorithms into a current regulated induction machine drive.
- Identification of potential inter-inverter SSA algorithm design approaches and their implications on implementation complexity.

- Identification of the potential SSA algorithm design approaches for n-phase converter systems and their implications on implementation complexity.

9.3 Recommended Future Work

Based on the research completed to date, the following future work is proposed:

- **Intra-Inverter SSA using DTFC or other Model Predictive Control Techniques**

While EV-SSA does reduce the effect of SSA on the inverter's output current harmonics, it is unable to systematically decouple SSA from torque control. DTFC provides an available degree-of-freedom through flux command selection to introduce the required voltage error vectors for SSA along the torque line so that output torque remains unaffected by SSA. This also eliminates the need for current error estimation and compensation as there is no current regulator. An evaluation of this approach should be performed comparing output torque and current waveforms from DTFC-SSA to those obtained using EV-SSA.

- **Transitions to Six-Step Operation while enforcing Intra-Inverter Simultaneous Switching Avoidance**

When an inverter's command voltage magnitude approaches its voltage limits, the available degrees-of-freedom for performing simultaneous switching avoidance diminish. On the contrary, six-step operation inherently prevents simultaneous switching because it always transitions between adjacent active-voltage vectors. However, transitions between this "pulse-dropping region and normal linear operation must be performed in such a way that simultaneous switching events are not created. Methods to do so while minimizing the impact on inverter output distortion should be explored to extend the intra-inverter SSA methods' operating range to the inverter's voltage limits.

- **Zero-Sequence-Voltage-Based Inter-Inverter SSA Techniques**

Relative zero-sequence voltage injection between the three-phase voltage commands of two inverters enables manipulation of their switching instances relative to one another without impacting current or torque control. Further, zero-sequence voltage injection for Inter-Inverter

SSA can be combined with any Intra-Inverter SSA technique without worry of creating new Intra Inverter switching overlaps. Finally, of all the possible approaches for performing Inter-Inverter SSA explored in this work, zero-sequence voltage injection presents the simplest route for developing an SSA algorithm that can be implemented in real-time hardware. Techniques should be be developed for selecting proper zero-sequence voltage in order to perform inter-inverter SSA. The resulting on current harmonics should then be compared to standard SVPWM operation to understand their effects on motor drive performance.

- **Further Investigation of Active Gate Drive Methods for Mitigating Simultaneous Switching Effects**

To date, a limited degree of work has been carried out investigating the use of closed-loop active gate drive techniques for mitigating switching transient overshoot during simultaneous switching showing that there is some efficacy to the approach. While the impact of simultaneous switching is not completely eliminated, voltage overshoot and switching losses can be decreased to a significant degree. Moreover, industry suppliers are beginning to bring to market off-the-shelf integrated circuit solutions for open-loop active gate drive techniques. These open and closed-loop gate drive approaches should be explored further, in both IGBT and MOSFET circuits, to quantify their efficacy in mitigating simultaneous switching effects in addition to the trade-offs in hardware design complexity.

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