Sensing Switching Power Semiconductor Junction Temperature Using Gate Drive Output Transient Properties

by

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Abstract

The objective of this research is to non-invasively sense switching power semiconductor junction temperature (T_j) in real time. By applying simple circuitry to the gate drive output current, a non-invasive, high bandwidth, and real-time switching power semiconductor T_j sensing can be achieved without an additional temperature sensor. The methodology used to sense a switching power semiconductor T_j is based on the T_j dependency of the "gate drive – switching power semiconductor" interactions during the switching transient. Depending on the type and fabrication of the switching power semiconductor, the gate drive output transient current properties such as peak value, time constant, Miller Plateau duration, and so forth are affected by T_j. Analog signal processing is applied to the gate drive turn-on output current transient in real-time, and the processed current signal is correlated to T_j. The "processed current – T_j" relationship is used for real-time T_j sensing. The online estimated switching power semiconductor T_j is calibrated by testing an un-encapsulated device with a thermal camera. In this research, all sensing hardware are implemented on the gate drive side; not in the power device or on the power circuit side. Real-time T_j estimation is achieved in each switching cycle, and this will potentially benefit switching power semiconductor active ΔT_j control. The methodology is verified on most of the mainstream switching power semiconductors (IGBT, SiC MOSFET, etc.), different types of gate drive topologies, and a wide range of power levels.

Acknowledgments

I would like to acknowledge my graduate advisor, Professor Lorenz, for his support, guidance, and allowing me the great honor to be a part of WEMPEC. The technical and personal insight you have provided me over these few years will undoubtedly prove invaluable in my professional career and personal life.

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Of course I would like to thank the entire WEMPEC family of students, faculty, and staff. I would especially like to thank Hao Jiang and Yichao Zhang for sharing their hardcore technical experience with me, Jiyao Wang for being a great friend, and Ray Marion and Helene Demont for helping me with all the orders, assemblings, and travels.

Lastly, I would like to thank my parents, without your financial support and unwavering belief in me, I could have never made it this far.

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Nomenclature

Symbol	**Description**
T_j	Junction temperature
Si	Silicon
SiC	Silicon-Carbide
GaN	Gallium-Nitride
MOSFET	metal oxide semiconductor field effect transistor
IGBT	Insulated gate bipolar transistor
$V_{DS\text{-}on}$	On-state voltage drop between drain and source
$I_{DS\text{-}on}$	On-state current from drain to source
$R_{DS\text{-}on}$	On-state equivalent resistance between drain and source
V_{CE}	Voltage drop across collector and emitter
TSEP	Temperature sensitive electrical parameters
i_G	Gate current
i_{sense}	Sensed current

Introduction

Research Motivation

The motivation of this research is to realize online switching power semiconductor T_j sensing without invading the converter power circuit.

Switching power semiconductor T_j sensing is normally achieved with a temperature detector. To optimize sensing accuracy, the temperature detectors are placed very close to the power semiconductor chip or embedded on the power semiconductor die. This is inconvenient for power integration, and the hardware implementation has to compromise to the device voltage/current rating, EMI protection, semiconductor fabrication, and the detector's thermal-mechanical stress. In addition, many temperature detectors do not have enough bandwidth to track the power semiconductor thermal dynamics online. This makes the power semiconductor active T_j control infeasible.

The intended outcome of this research is a set of "gate drive design – signal processing" principles that integrate switching power semiconductor T_j sensing into gate drive and enable non-invasive, high bandwidth, real-time T_j estimation utilizing gate drive turn-on output current waveforms. Suitable "gate drive design – signal processing" methods for different types of switching power semiconductors, different power ratings, and different loads will be identified and evaluated.

Overview

This research develops a technology that integrates switching power semiconductor T_j sensing into its gate drive. Applying simple implementations to the gate drive output current, non-invasive, high bandwidth, and real-time switching power semiconductor T_j sensing can be achieved without an additional temperature sensor. Device type dependency, gate drive topology dependency, and load dependency are studied in this research to benefit general application of this technology.

The methodology used to sense the switching power semiconductor T_j is based on the T_j dependency of the "gate drive – switching power semiconductor" interactions during the switching transient. Many switching power semiconductor's intrinsic parameters are T_j sensitive, and some of them (gate threshold voltage V_{TH}, turn-on gate charge Q_G, etc.) are the dominant factors to the gate drive output current transient waveform. Thus, depending on the type and fabrication of the switching power semiconductor, the gate drive output current transient properties, such as peak value, time constant, Miller Plateau duration, and so forth, can be affected by T_j. Simple signal processing (for instance, peak detection, integration) is applied to the gate drive turn-on output current transient in real-time, and the processed current signal is correlated to T_j. The "processed current – T_j" correlation is referenced online for real-time T_j sensing. The T_j dependency of the switching power semiconductor intrinsica parameters is provided by the semiconductor manufacturers. The online estimated switching power semiconductor T_j is calibrated by an un-encapsulated device thermal test using a thermal

camera. Real-time T_j estimation is achieved in each switching cycle, and this will potentially benefit the switching power semiconductor T_j active control. The methodology is applied to most of the mainstream switching power semiconductors (IGBT, SiC MOSFET, etc.), different types of gate drive topologies, and a wide range of power levels.

Finally, this research proposed a set of "gate drive design – signal processing" principles that integrate switching power semiconductor T_j sensing into the gate drives and enable non-invasive, high bandwidth, real-time T_j estimation utilizing gate drive turn-on output current waveforms. Suitable "gate drive design – signal processing" principles for different types of switching power semiconductor, different power ratings, and different loads are identified and evaluated.

Research Contributions

The following list summarizes the key contributions made by this research:

- Established a non-invasive method for real-time switching power semiconductor T_j sensing based on the gate drive turn-on output current transient.
- Developed different "gate drive – switching power semiconductor" transient models to analyze the power semiconductor turn-on transient dynamics.
- Proposed different online analog signal processing methods to extract the "i_G - T_j"dependencies.
- Provided the method of deriving the relationship between gate drive turn-on output current transient i_G and switching power semiconductor T_j.
- Provided the "i_G –T_j" relationships for Si MOSFET, Si IGBT, SiC MOSFET, and GaN HEMT.
- Investigated the hardware implementations for online analog signal processing to extract T_j information from the sensed i_G waveforms.
- Calibrated the proposed T_j sensing method based on the sensing repeatability, thermal operating point effect, and device vertical thermal gradient.
- Evaluated the performance of the proposed T_j sensing method when different gate drive topologies are used. Suitable signal processing methods for the different gate drive topologies are proposed accordingly.
- Provided the effect of DC bus voltage value on the proposed T_j sensing method.

Summary of Chapters

Chapter 1 reviews the state-of-the-art techniques for online T_j sensing, and opportunities for fast and non-invasive T_j sensing.

Chapter 2 defines the power converter circuit dynamic loops and investigates the feasible measuring points for online switching power semiconductor T_j sensing.

Chapter 3 presents the system dynamic modeling for the switching power semiconductors, the gate drives, and the H-bridge inverter.

Chapter 4 presents the experimental test setup used to evaluate the online switching power semiconductor T_j sensing proposed in this research.

Chapter 5 investigates the method to manipulate the switching power semiconductor T_j. The "$i_G - T_j$" relationships for common devices are provided.

Chapter 6 develops the methods to extract the switching power semiconductor T_j information from the sensed i_G waveforms.

Chapter 7 calibrates the proposed T_j sensing method for sensing repeatability, the effect of the system thermal operating point, and the device vertical thermal gradient.

Chapter 8 studies the effect of gate drive topologies on the i_G transient waveforms. Feasible signal processing methods are investigated accordingly.

Chapter 9 investigates the effect of DC bus voltage on the proposed T_j sensing method.

Chapter 10 contains the conclusions and contributions of this research and the recommended future work to improve online switching power semiconductor T_j sensing.

Chapter 1 State-of-the-Art Review

This chapter begins with a review of the thermal-electrical characteristics of switching power semiconductors. The switching/conducting properties of Si MOSFET, Si IGBT, SiC MOSFET, and GaN MOSFET are summarized based on their T_j dependency. A brief discussion about the thermal dynamics of different device packagings is included. The second protion of this chapter reviews the state-of-the-art methods for switching power semiconductor online T_j sensing. The concept of multi-physics integration is also introduced. Finally, a summary of results from previous work will be presented along with the research opportunities that have been identified through examination of previous works.

1.1 Switching Power Semiconductor Thermal-electrical Characteristics

1.1.1 MOSFET

When the power converter is designed to switching with low voltage stress and high switching frequency, the MOSFET is usually the first option for the switching power semiconductor. Compared to the other switching power semiconductors, for example an IGBT, MOSFETs have a simple gate drive requirement, fast but stable switching charactersitcs, and high efficiency at low voltages.

Most of the semiconductor characteristics, such as device conducting channel length, the carrier mobility, and so forth, are junction temperature dependent. As a result, the switching/conducting properties of a switching semiconductor are T_j sensitive. In a dynamic model of power MOSFET, the three dominated T_j dependent parameters are the on-state resistance $R_{DS\text{-}on}$, the gate threshold voltage V_{TH}, and the gate charge Q_G. The temperature dependency of the aforementioned three parameters is usually provided by the device manufacturer's datasheet. Although many other device parameters are also T_j sensitive, their T_j dependency is not generally supported by their device manufacturers.

The MOSFET $R_{DS\text{-}on}$ is used to characterize the MOSFET conducting properties. It is generally a equivalent resistance used to model the conducting channel power dissipation.

Note that the power MOSFET on-state voltage $V_{DS\text{-}on}$ is proportional to its on-state current $I_{DS\text{-}on}$ when MOSFET is operating with its power rating. Accordingly, the MOSFET on-state resistance is defined in (1.1.1) based on this proportional relationship [1].

$$R_{DS\text{-}on} = \frac{V_{DS\text{-}on}}{I_{DS\text{-}on}} \tag{1.1.1}$$

The $R_{DS\text{-}on} - T_j$ dependency has been studied for years, and sometimes this dependency is used for MOSFET T_j estimation. Releying on the power rating and switching speed of the MOSFET, the value of $R_{DS\text{-}on}$ varys between several mili-ohm and several ohm. Most of the MOSFET $R_{DS\text{-}on}$ have positive T_j coefficient ($R_{DS\text{-}on}$ will

increase with increasing T_j). It is very rare for power MOSFET to have a negative $R_{DS\text{-}on}$ – T_j coefficient.

The MOSFET gate threshold voltage V_{TH} is essential for switching characterization and gate drive design. By definition, V_{TH} is the minimum gate-to-source voltage that is needed to create a conducting path between the source and the drain. The MOSFET operation region can be roughly calculated by the threshold voltage V_{TH}, the gate-to-source voltage V_{GS}, and the drain-to-source voltage. If $V_{GS} - V_{TH} > V_{DS}$, the MOSFET is in "linear region" (also refered to as the "ohmic region"), where it behaves like a voltage controlled variable resistor. If $V_{GS} - V_{TH} < V_{DS}$, the MOSFET is in "saturation region" (also refered to as the "active region") where the drain current will not change with V_{GS}. An MOSFET input-output characteristics plot is shown in Fig. 1.1.1.

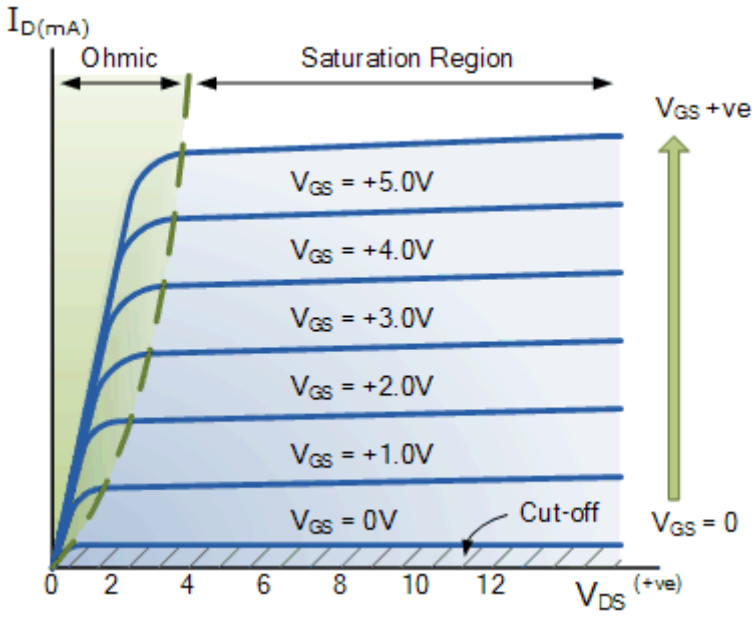


Fig. 1.1.1 A typical n-type power MOSFET input-output characteristics

The MOSFET V_{TH} is directly determined by the semiconductor's oxide thickness and surface potential. The surface potential of semiconductor is directly related to T_j. A 50^oC T_j change can result in an up to 20% change of V_{TH}. Generally, MOSFET V_{TH} is negatively correlated to T_j.

During the MOSFET turn-on transient, a current pulse will be injected into MOSFET gate terminal. After the turn-on transient, the current injecting into the MOSFET gate will be very small. The total charge injected into the MOSFET gate during the MOSFET turn-on transient is defined as the gate charge. Many simplified MOSFET dynamic model will also define the MOSFET input capacitance, and charing the input capacitance to the turn-on voltage can be considered as the mechanism of gate charge injection. However, the MOSFET gate current transient is much more complicated than charging an equivalent capacitor. Generally, the gate charge value and the input capaticance can be found in the device datasheet, but their T_j correlation are not supported.

The silicon MOSFET thermal-electrical charactersitcs is the foundamental of other switching power semiconductors. The device characteristics discussed in the following sections will be frequently refered to this section.

1.1.2 IGBT

The insulated-gate bipolar transistor (IGBT) combines the simple gate-drive characteristics of MOSFET and the the high current and low saturation voltage capability

of bipolar transistor. In other words, in a single device, the gate control is as simple as isolated gate FETs while the output properties is similar to bipolar junction transistor. The aforementioned characteristics make IGBT suitable for high current, high voltage rating power converter systems.

The conduction properties of IGBT is different from MOSFET [2]. Since the voltage across the IGBT collector and emitter V_{CE} cannot be linearly correlated to the IGBT current I_{CE}, it is not feasible to define on-state resistance for IGBT. Instead, V_{CE} is usually regarded as a variable controlled by T_j and I_{CE}, as decribed in (1.1.2).

$$V_{CE} = f\,(I_{CE}\,,\,T_j) \tag{1.1.2}$$

While $R_{DS\text{-}on}$ is sometimes used for MOSFET T_j estimation, V_{CE} is feasible for IGBT T_j estimation. The correlation between IGBT V_{CE}, I_{CE}, and T_j is usually provided by the IGBT manufacturers' datasheet.

Consider that the gate control properties of an IGBT can be modeled as FET input, the threshold voltage and the gate charge thermal-electrical properties for an IGBT is similar to that of a MOSFET.

The transconductance of IGBT is another T_j sensitive coefficient that is essential for IGBT properties. The transconductance gm for an IGBT is defined in (1.1.3). Since gm deals with both the gate properties and the conducting current properties, it is a compound correlation among FET properties to a BJT properties. Although the $g_m - T_j$ dependency is generally agreed and investigated, this correlation is rarely provided by the MOSEFT manufacturer. Deriving the $g_m - T_j$ correlation requires the synchronization of current measurement and voltage measurement.

$$g_m = \frac{dI_{CE}}{dV_{GE}} \tag{1.1.3}$$

During the IGBT turn-on process, the gate-emitter voltage V_{GE} will increase from the off-state gate voltage to the on-state gate voltage. In the transient process, the gate voltage will keep at a certain level for a short period, and reach the on-state gate voltage afterwards. This short staying gate voltage level is called Miller Plateau. In most of the FET-gated device, Miller Plateau can be obseraved during switching transient, and the voltage level of Miller Plateau is T_j sensitive. The "Miller Plateau voltage – T_j" correlation can be ambiguous for a Silicon MOSFET, but it is ususally very explicit for a Silicon IGBT. The T_j dependent definition for IGBT Miller Plateau is stated in (1.1.4), where $g_{m,sat}$ is the satuated transconductance.

$$V_{miller}(T_j) = V_{TH}(T_j) + \frac{I_{CE}}{g_{m.sat}(T_j)} \tag{1.1.4}$$

1.1.3 HEMT

High-electron-mobility transistor (HEMT), also known as heterostructure FET (HFET) or modulation-doped FET (MODFET), is a field-effect transistor incorporating a junction between two materials with different band gaps (i.e. a heterojunction) as the channel instead of a doped region (as is generally the case for MOSFET). A commonly used material combination is GaAs with AlGaAs, though there is wide variation, dependent on the application of the device. Devices incorporating more indium generally show better high-frequency performance, while in recent years, gallium nitride HEMTs have attracted attention due to their high-power performance.

Dispersion has been included in large-signal models by using an additional RF current source and another drain conductance branch or a high-pass feedback network between the drain and gate. Previously, an analytical model including dispersion effects was considered for a small periphery and relatively low power density AlGaN–GaN HEMT on SiC. However, device heating is important, even for GaN (1.3 W/(cm K)) on high thermal conductivity semi-insulating SiC substrates because applications can involve higher temperatures than conventional devices based on GaAs and Si. The heating results in decreased current and transconductance due to a decrease in the two-dimensional electron gas (2DEG) mobility and velocity. Therefore, considering temperature-dependent characteristics in a large-signal model is important to correctly predict high power density operation, e.g., at power levels 10W/mm at 10GHz. Incoperating both the thermal and dispersion effects in an analytical model allows effective circuit development with a harmonic-balance simulator.

The circuit shown in Fig. 1.1.1 is used to model the measured device characteristic dependence on temperature and bias. It includes a thermal circuit, temperature-dependent drain current source, and bias-dependent gate–source and gate–drain capacitances. The thermal model has a current source Ith, a resistance (^{o}C/W), and a capacitance C_{th}. With these elements at a particular bias point, the device junction temperature T_j can be determined.

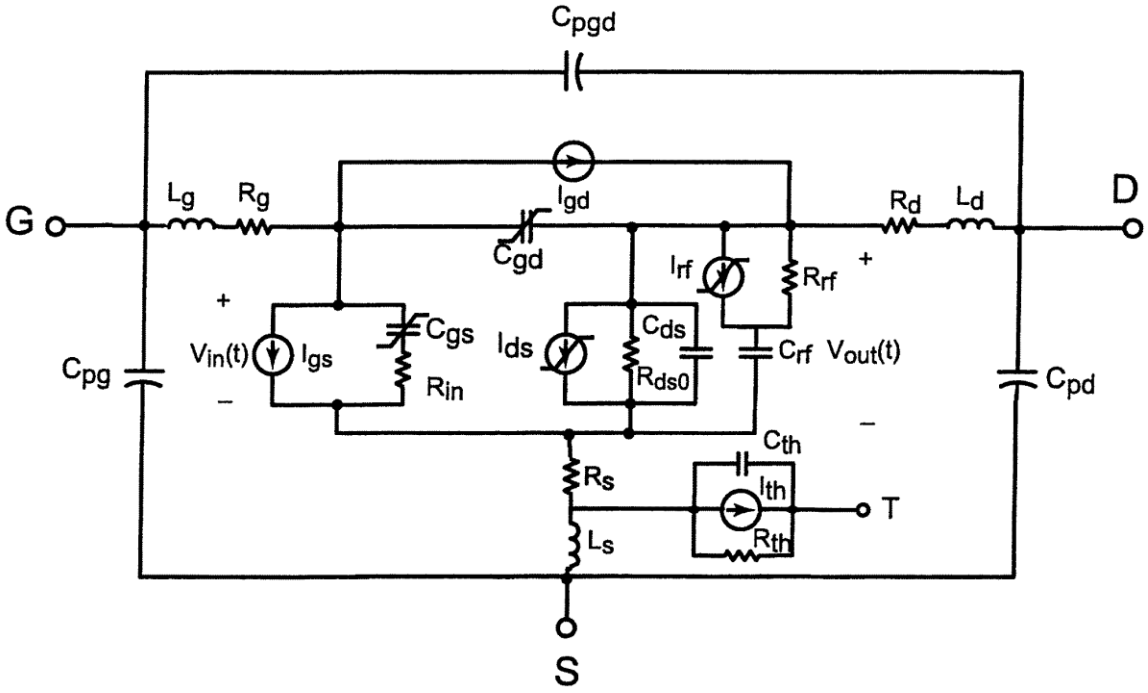


Fig. 1.1.1 GaN HEMT equivalent circuit model with junction temperature dependency

1.2 Semiconductor Package Thermal Dynamics

This section will review the thermal dynamics mechanism of switching power semiconductor device package. A brief discussion about the device thermal-mechanical failure will also be included

1.2.1 Device Thermal Dynamic Modeling

For temperature control consideration, switching power semiconductors operated in a power converter require a cooling system. The cooling system can be air-based or liquid based. An air-cooling metal heat sink attached to the back plate of semiconductor device (or power module) is one simple way to implement the cooling system. A cross-sectional view of a typical thermal dynamic system for SiC MOSFET implementation is

shown in Fig. 1.2.1 [3]. Note that this implementation is for power modules that contains more than one power semiconductors. For a discrete component, the 200μm copper layer and the 500μm Al_2O_3 layer are not used.

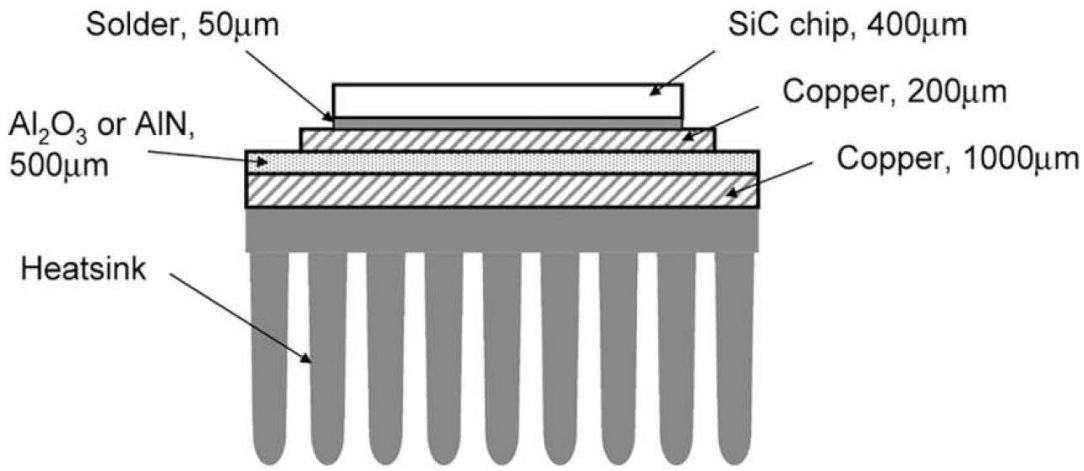


Fig. 1.2.1 cross-sectional view of a typical thermal dynamic system for SiC MOSFET implementation

In Fig. 1.2.1, the power dissipation is generated from the SiC chip which is on the top side of this cross-sectional model. Right below the SiC chip, a 50μm solder layer is used to connect the SiC chip to the 200μm copper layer. The solder layer have a relatively big thermal resistance compared with copper, thus it is always considered as the first thermal barrier for the chip heat generation. The 200μm copper layer is used to connect different chips in one power module. Bond wire can be connected to the 200μm copper layer. Below the 200μm copper, there is a 500μm insulated layer formed by Al_2O_3 or AlN. This insulated layer isolated the electric power conversion inside the module from the outside cooling system. Considering the thickness and the high thermal resistance of this insulated layer, it is also refered to as the second thermal barrier for the

chip heat generation. The 1000μm copper provide the stiffness to the power module, and the heat sink will be applied to the outer surface of this 1000μm copper.

For the steady state analysis, the thermal system in Fig. 1.2.1 can be modeled as the equivalent circuit model in Fig. 1.2.2, where T_j is the chip junction temperature, T_{amb} is the ambient temperature, P_{loss} is the heat generation from the chip, and R is the equivalent thermal resistance between the chip junction and the ambient air.

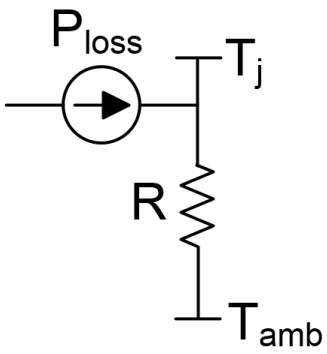


Fig. 1.2.2 Steady state thermal equivalent circuit model.

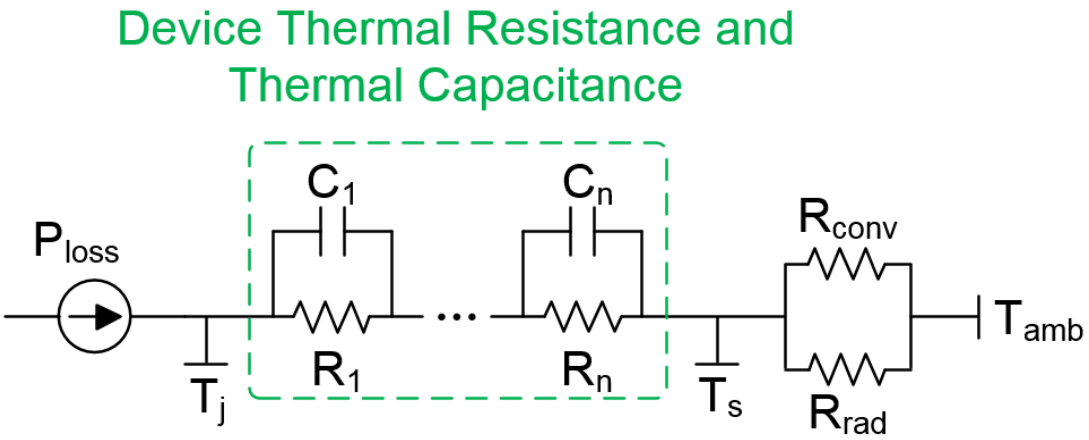


Fig. 1.2.3 Dynamic thermal equivalent circuit model.

1.2.2 Thermal-electrical Failure

The thermal-electrical failure of a discrete component or power module are most likely to happen on the bond wire that attached to the semiconductor chip. A picture for the bond wires in a converter power module is shown in Fig. 1.2.4.

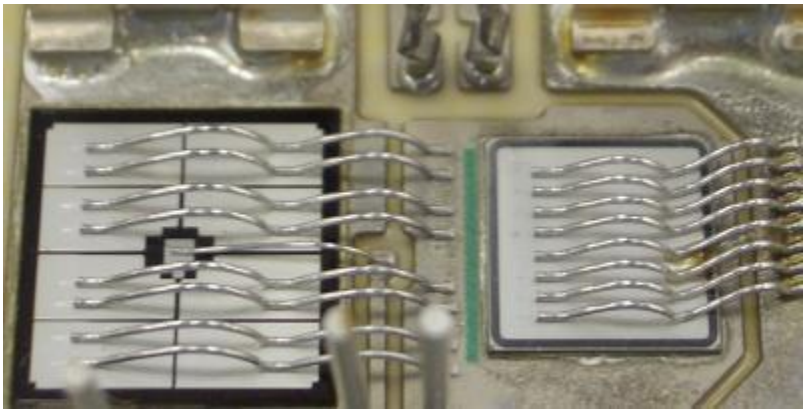


Fig. 1.2.4 Bond wires in a power module

It can be seen from Fig. 1.2.4 that some part of the wire bond is connected to the semiconductor chip surface. As a result, the semiconductor chip surface temperature will directly work on the bond wire connection point. Different PWM can generate different chip thermal dynamics, and ultimately it may generate different thermal strain dynamics for the bond wires [4].

The following damage modes are commonly observed on the bond wires.

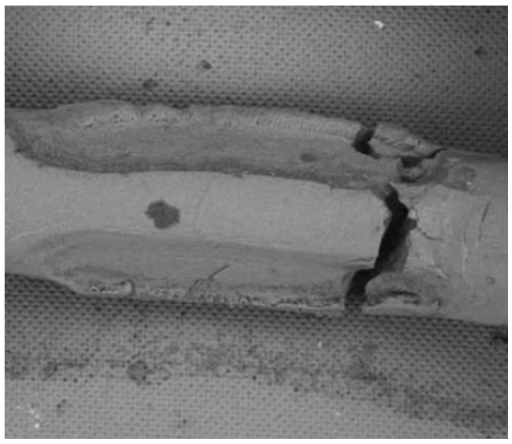
1) Heel crack and fractures (mechanical constraints in the wires and fatigue phenomenon due to the deformation related to temperature swings);

2) Wire bond liftoff (mechanical stress on Al–Si joints due to the difference in the thermal expansion coefficient between Al and Si);

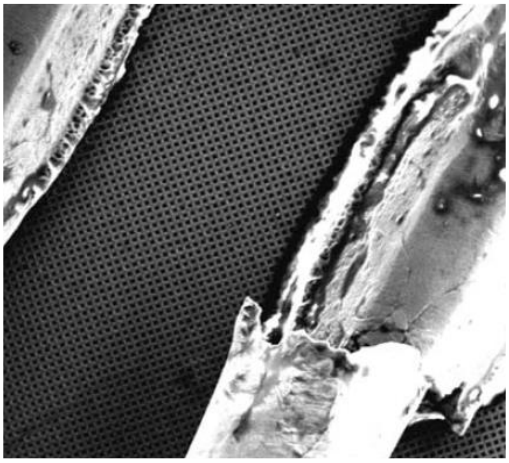
3) Metallurgic damage due to the thermomechanical stress on aluminum resulting in part from the difference.

Pictures for the aforementioned failure is shown in Fig. 1.2.5.

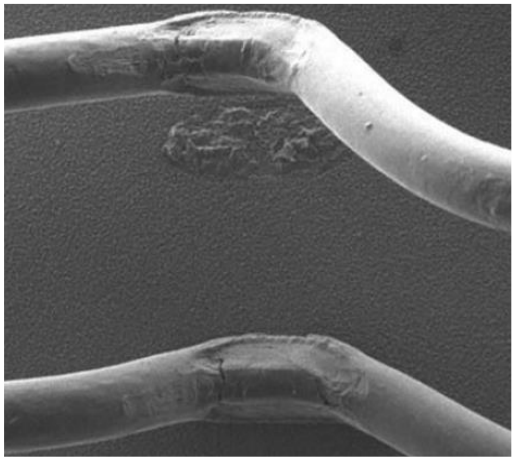
Metallurgic damage



Heel crack



Fracture



Liftoff

Fig. 1.2.5 Examples of bonding damages

By actively control the switching power semiconductor T_j, the strain in the bond wire can be optimized and the damage to the bond wire will be possible to predict.

1.3 Observer-Based T_j Sensing Method

Observer-based T_j sensing is a physics-based approach focused on extracting the un-accessible junction temperature from the directly measureable signal like voltage, current, back plate temperature, and so forth. Properly modeling the switching power semiconductor thermal dynamics is essential to the performance of temperature observer. A typical temperature oberserver need to estimate the swiching power semiconductor heat generation and heat transfer process.

Accordingly, a detailed understanding about the device loss mechanism and device physical integration is necessary. The device loss is usually supported by its manufacturer. The lab test calibration for device power loss is can be achieved with only voltage measurement and current measurement. Different from the device power loss, the device integration information are not always fully supported by the device manufacturer because of confidentiality consideration.

1.3.1 Device Power Dissipation

Switching power semiconductor T_j can be regarded as the accumulation of power dissipation on the device [5]. The power dissipation include device switching loss and conduction loss of each switching cycle [6]. If the device loss in one switching cycle can be calculated, real-time T_j can then be calculated iteratively based on the device thermal model [7]. The typical voltage and current waveform of a single IGBT switching cycle with the correlated loss waveform is shown in Fig. 1.3.1. Although the thermal dynamics

of semiconductor junction is much slower compared with device switching frequency, a junction temperature variation still exists in each swiching cycle.

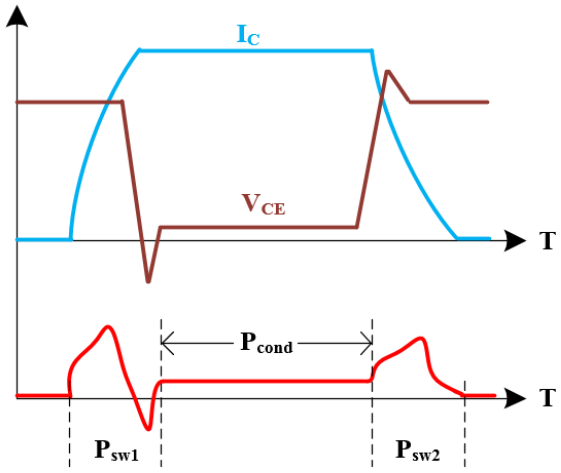


Fig. 1.3.1 Typical voltage and current waveform of a single IGBT switching cycle

The loss of a switching semiconductor depends on the voltage and current on the device, as well as the T_j of the device [8]. In each switching cycle, the estimated device loss $P_{loss\ k}$ has to be updated based on the device voltage v_k and current i_k of this switching cycle, the duty ratio d of this switching cycle, and the estimated T_j of the latest previous switching cycle $T_{j\ k-1}$. A very simple iterative interpretation for the power dissipation based T_j estimation is summarized in (1.3.1) and (1.3.2), where F is the device T_j dependent loss model and G is the device thermal model.

$$P_{loss\ k} = F(v_k , i_k , d , T_{j\ k-1}) \tag{1.3.1}$$

$$T_{j\ k} = G(T_{j\ k-1} , P_{loss\ k}) \tag{1.3.2}$$

The accuracy and consistency of the device power dissipation based T_j estimation largely relies on the accuracy of the loss model F and the thermal model G in (1.3.1) and

(1.3.2). This method has been applied to several topologies [7] [9]. Experimental results indicates a 2^{o}C T_j estimation error and a 2 milli-second estimation delay for Mitsubishi Electric 2-in-1 IGBT module [5]. [10] applied this method to Semikron SKM 100GB 123D IGBT module, and a 3.7^{o}C steady state T_j estimation error was found in the prototype test. For long-term application consideration, the semiconductor aging can slightly change the loss model F in (1) [4] [11]. Thus device aging has to be considered for commercialized products when using the power dissipation based T_j estimation method.

The off-state voltage across the switching semiconductor (v_k in (1.3.1)) and the on-state current through the switching semiconductor (i_k in (1.3.1)) needs to be measured with galvanic isolated sensors, and the voltage sensors are usually invasively connected to the converter power terminals. When applying the power dissipation based T_j sensing method to those complicated topologies (for instance, the modular multilevel converter in [7]), large numbers of switching semiconductor need numerous voltage/current sensors for T_j sensing, making it challenging for power integration. The bandwidth of the voltage/current sensors determines the bandwidth of this online T_j sensing method. If a look-up table for (1.3.1) and (1.3.2) can be created in advance, the computation amount of this method can be significantly reduced.

The performance of the open-loop T_j observer and the closed-loop T_j observer will be highly dependent to the device loss model (1.3.1) and the device thermal dynamic model (1.3.2) dicussed in this section.

1.3.2 Open-loop T_j Observer

In an open-loop T_j observer application, the device loss model (1.3.1) and the device thermal dynamic model (1.3.2) should be derived offline first. With a specific device load current and switching frequency, the open-loop T_j observer can calculate the estimated junction temperature, $\hat{T}_j$, based on (1.3.1) and (1.3.2), as shown in Fig. 1.3.2.

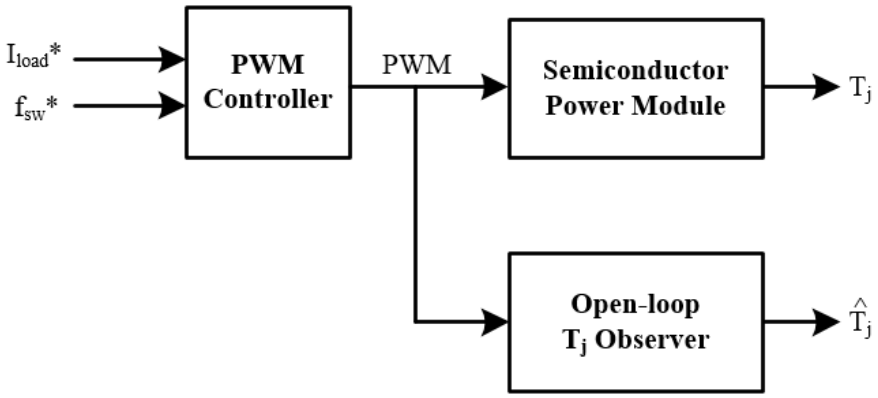


Fig. 1.3.2 Open-loop T_j observer in the inverter system, commanding load current and switching frequency to the PWM controller.

As can be seen from Fig. 1.3.2, the PWM control signal will be calculated by the PWM controller based on the command currnet I_{load}* and the command switching frequency f_{sw}*. This PWM control signal will be sent to the semiconductor power module, generating the actual power PWM waveform. Meanwhile, the PWM control signal is analysed by the open-loop T_j observer as well. By mimicking the loss generation and thermal dynamics of the semiconductor power module, $\hat{T}_j$ can be derived online.

Topologies, like a multilevel inverter, have more than one switching strategy for the power semiconductor, while the fundamental part of the load voltage/current remains

the same. On such case, the PWM controller will have one more freedom to choose the device switching duty ratio based on the position of the PWM rotating vector, as shown in Fig. 1.3.3.

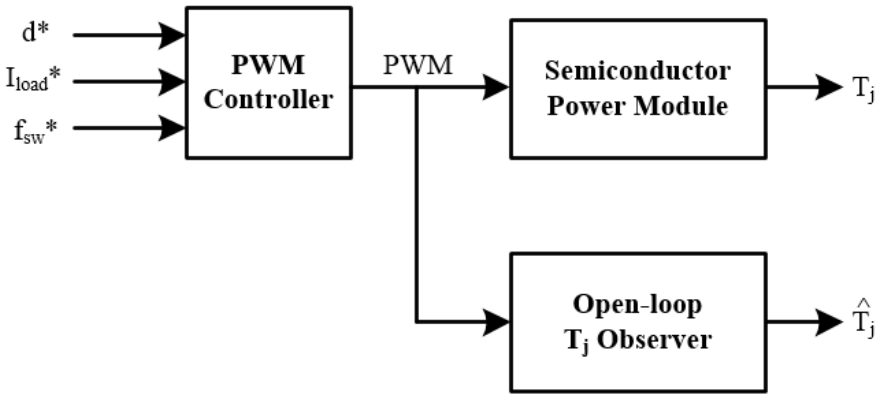


Fig. 1.3.3 Open-loop T_j observer in the inverter system, commanding duty ratio, load current, and switching frequency to the PWM controller.

In the system in Fig. 1.3.3, the duty ratio can be manipulated as d*, thus the switching semiconductor conduction loss can be manipulated in each switching cycle. By manipulating the conduction loss under a specific switching frequency, it is possible to manipulate T_j while commanding load current and switching frequency at the same time, as shown in Fig. 1.3.4.

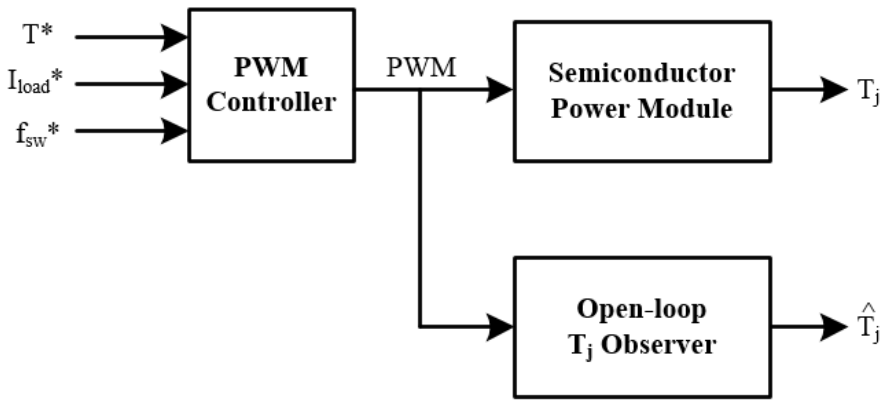


Fig. 1.3.4 Open-loop T_j observer in the inverter system, commanding junction temperature, load current, and switching frequency to the PWM controller.

1.3.3 Close-loop T_j Observer

To build a close-loop T_j observer, feedback signal from the semiconductor power module is required. A temperature sensor can be implemented on the back plate of the semiconductor power modules or bound to the inner copper laying inside the module. The temperature information T_x sensed by these temperature sensors can be fed into the T_j observer to realize close-loop T_j estimation, as shown in Fig. 1.3.5.

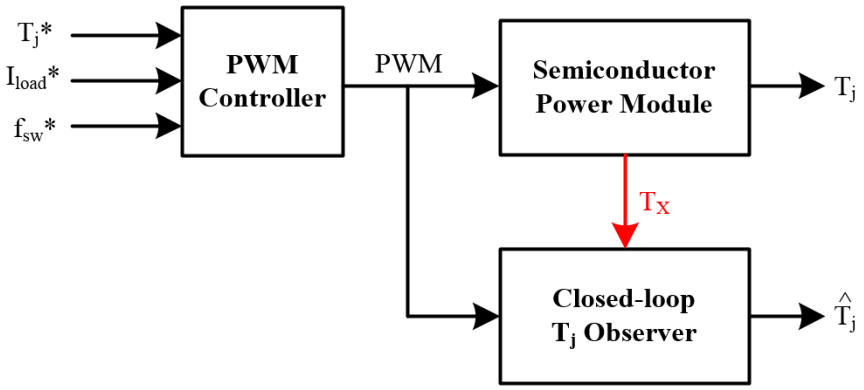


Fig. 1.3.5 Close-loop T_j observer in the inverter system, commanding junction temperature, load current, and switching frequency to the PWM controller.

By using the baseplate temperature of a semiconductor power module, [12] implement an enhanced Luenburger style temperature observer in a simplified three-layer power module thermal dynamic system, as shown in Fig. 1.3.6.

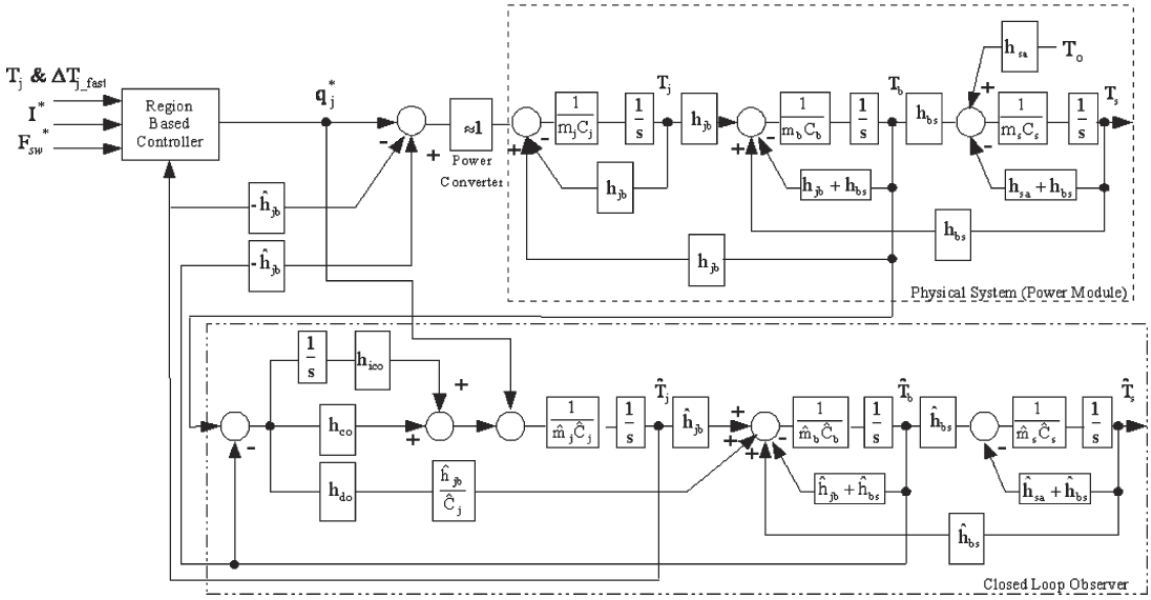


Fig. 1.3.6 Enhanced luenburger style temperature observer in a simplified three-layer power module thermal dynamic system

1.4 T_j Sensing Based on the "Diode-on-Die Technology"

The forward voltage drop of a p-n junction under fixed current is known to be temperature sensitive [13]. Fig. 1.4.1 shows the "output voltage – T_j" relationship of a p-n junction (diode). This relationship is measured using two different methods: injecting constant current though the diode (shown in blue) and using a 62kΩ pull up resistor (shown in red).

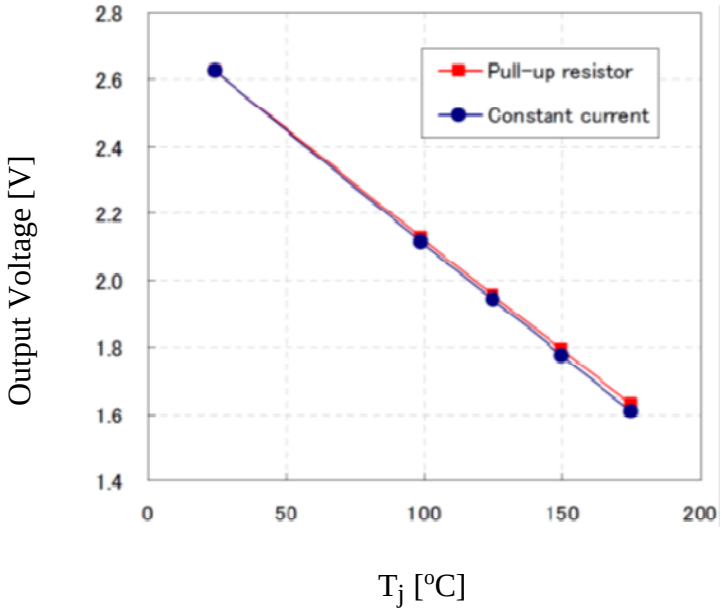


Fig. 1.4.1 "output voltage – T_j" relationship of a p-n junction (diode)

The T_j dependency of p-n junction forward properties can be used for temperature sensing. This type of p-n junction temperature sensor was originally used for an ambient temperature sensor, and the p-n junction was fabricated into a discrete component [14].

With modern semiconductor fabrications, semiconductor manufacturers embedded the temperature sensitive p-n junction on the switching power semiconductor chip and used its properties for online T_j sensing [15] [16] [17]. A picture with a p-n temperature sensor and current sensor integrated on a MOSFET chip is shown in Fig. 1.4.2. In [16], the p-n junction sensor was fabricated on the IGBT chip using poly-silicon with insulation, and in [18] this technology was applied to a SiC MOSFET. Since that, the p-n junction sensor can be considered as a small power rating diode and that the

sensor shares the same die with the power semiconductor; this technology can be referred to as the “diode-on-die technology”.

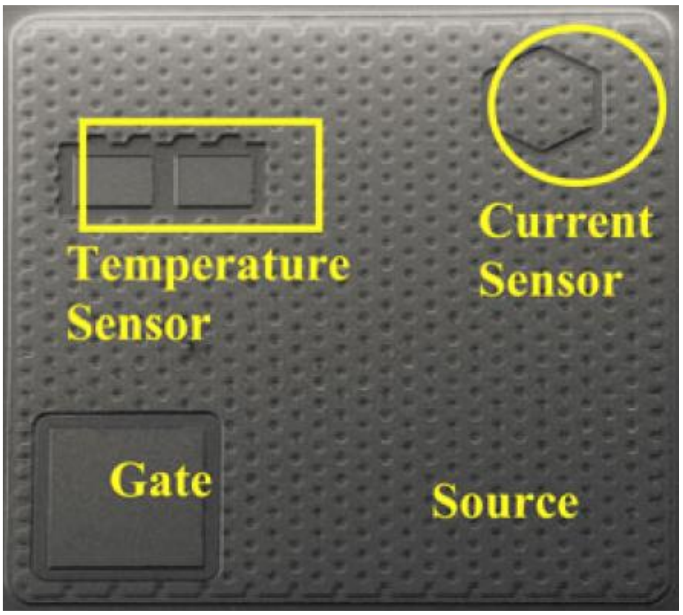


Fig. 1.4.2 p-n temperature sensor and current sensor integrated on a MOSFET chip

Taking a vertical structure IGBT as an example, the T_j sensor can be fabricated as a diode on the emitter side of the IGBT chip’s surface as shown in Fig. 1.4.3. By properly doping and fabricating, the voltage across the diode string can be used for IGBT chip T_j online monitoring [19]. A typical “Voltage drop - T_j” correlation for a “diode-on-die technology” sensor is investigated in [17], and the T_j sensing resolution in the figure can reach 6.7mV/^{o}C.

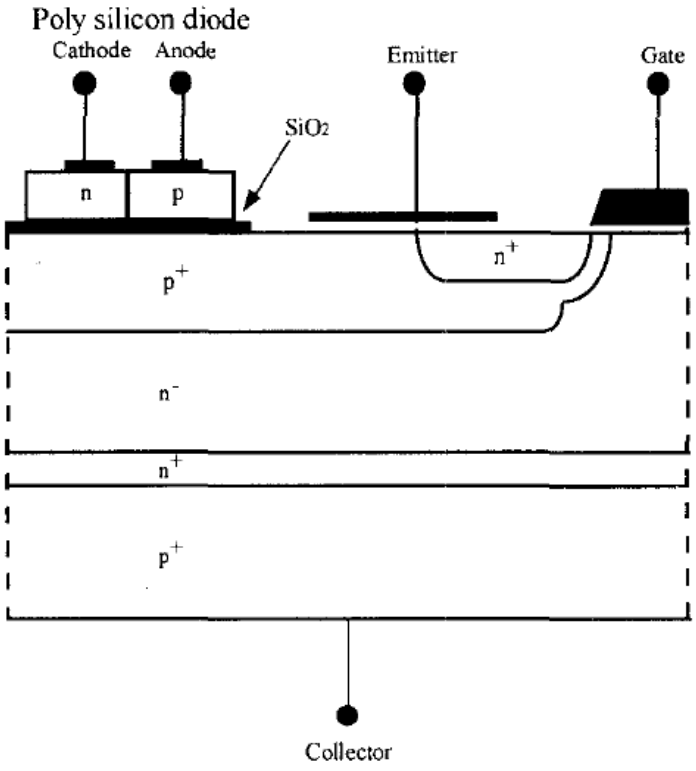


Fig. 1.4.3 T_j sensor fabricated on the emitter side of a IGBT chip

The "diode-on-die technology" provides a more accurate measurement of semiconductor junction temperature compared with those T_j sensing methods with sensors mounted remotely. In addition, considering that the size and the volume of the sensor is very small, the thermal dynamics of the sensor are fast compared with the semiconductor chip. Thus, the response time of this type of sensor is very fast. In [16], a Fuji 7MBP50RA060 IGBT module using a "diode-on-die technology" sensor had a 2 milli-second response time for an over temperature alarm.

Since the p-n junction T_j sensor is isolated from the power semiconductor [18], T_j sensing only needs a signal level constant current source and a voltage measurement setup [17], which can be easily integrated inside the power module.

Several limits exist in the "diode-on-die technology" T_j sensing. Considering the number of stringed diodes is not very big, the T_j sensing consistency control is challenging. Thus, the performance of sensors fabricated in the same batch cannot be guaranteed consistent. [18] shows that T_j dependence of the sensor is not well matched with the analytical model. In addition, the on-chip p-n junction T_j sensor is usually fabricated on a small area on the power semiconductor chip (as shown in figure 8 in [17] and figure 14 in [18]). If a hot spot exists on the semiconductor chip, the sensor might not be able to detect it. Moreover, the on-chip p-n junction T_j sensor needs to be connected to the off-chip circuit setup by wire bond or direct bonded copper (DBC). Since the size of the p-n junction is very small, the position and connection of wire bond or DBC is challenging. The parasitics and contact resistance of the wire bond or DBC has to be carefully controlled [20].

1.5 T_j Sensing Based on Device on-state Properties

Instead of implementing an additional sensor to the switching power semiconductor, the device thermal-electrical properties can be used for online T_j sensing. If the device's switching/conducting properties can be measured online and correlated to T_j with simple and fast implementation, the T_j sensing can be reasibly achieved in realtime.

The semiconductor on-state temperature dependent properties are one option for switching power semiconductor online T_j sensing. Switching semiconductor temperature dependencies, such as the IGBT V_{CE} versus T_j relationship, the MOSFET $R_{DS\text{-}on}$ versus

T_j relationship, and the IGBT/MOSFET V_{TH} versus T_j relationship, are essential for power conversion, thermal management, and gate drive design. Thus, these parameters' T_j dependencies are generally tested by the semiconductor manufacturer under different test conditions and supported with details.

Since the measurement of semiconductor on-state properties are simple in implementation, T_j based on device on-state properties have been studied and adapted in industry for many years.

1.5.1 BJT Common-base Operation T_j Dependency

[1971 New method of] proposed in 1971 that with TSEPs, semiconductor on-state properties can be measured for T_j sensing. Different from the conventional operation of a switching semiconductor, a bipolar junction transistor (BJT) operates on common-base mode, as shown in Fig. 1.5.1.

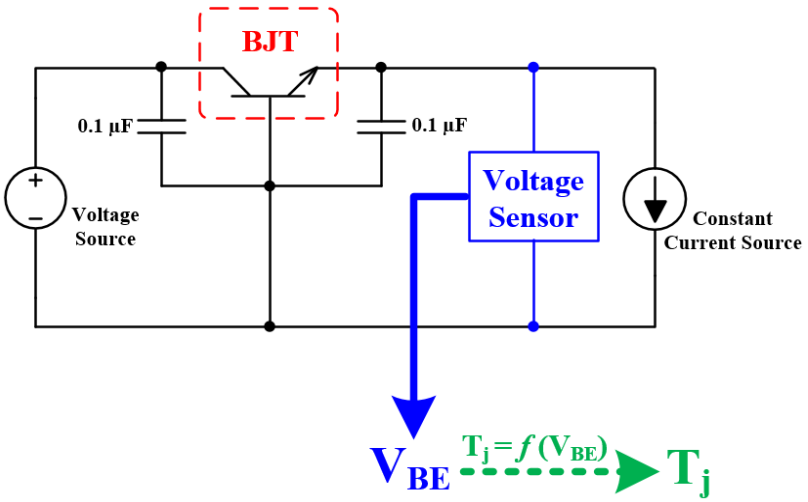


Fig. 1.5.1 BJT T_j sensing based on common-base mode V_{BE}. V_{BE} is measured by voltage sensor.

The procedure and necessary circuitry (Fig. 1.5.1) for measuring junction temperature by this method has been well described in [21]. This technique can be considered a way of obtaining a correlating measurement between V_{BE} and T_j. Essentially, the method involves a measurement of the increase of the base-emitter (BE) junction temperature due to an increase of the power dissipation in the base-collector (BC) junction. That is, at constant emitter current I_E and constant case temperature; an increase in BC voltage ΔV_{BE} will increase collector power dissipation by $I_E \Delta V_{CB}$ (emitter and collector currents are approximately the same for an electrically healthy device). This will reduce the BE junction voltage by ΔV_{BE}. A calibration ofΔV_{BE} against T_j gives the quantity $\partial V_{BE}/\partial T_j \big|_{I_E}$, enabling the temperature rise of the BE junction to be found as

$$\Delta T_j = \frac{\Delta V_{BE}}{\partial V_{BE}/\partial T_j} \Bigg|_{I_E} \tag{1.5.1}$$

Constant current is pulled out from the BJT emitter, and the voltage between BJT base and emitter V_{BE} is correlated to T_j. This method is extended for online BJT T_j sensing in [22], where hardware implementation and data processing is demonstrated in detail. [22] was published in 1991 and a 0.2 second T_j sensing response time is observed.

1.5.2 Using Power MOSFET "$R_{DS\text{-}on} - T_j$" Dependency for T_j Sensing

Power MOSFET on-state resistance $R_{DS\text{-}on}$ is known to be T_j dependent, hereby this property is often used for power MOSFET online T_j sensing [23]. Power MOSFET $R_{DS\text{-}on}$ can be digitally calculated online with (1.5.2) by measuring the MOSFET on-

state voltage $V_{DS\text{-}on}$ and on-state current $I_{DS\text{-}on}$ [24], as shown in Fig. 1.5.2. The online calculated $R_{DS\text{-}on}$ will be correlated to T_j based on the power MOSFET "$R_{DS\text{-}on} - T_j$" relationship.

$$R_{DS\text{-}on} = \frac{V_{DS\text{-}on}}{I_{DS\text{-}on}} \tag{1.5.2}$$

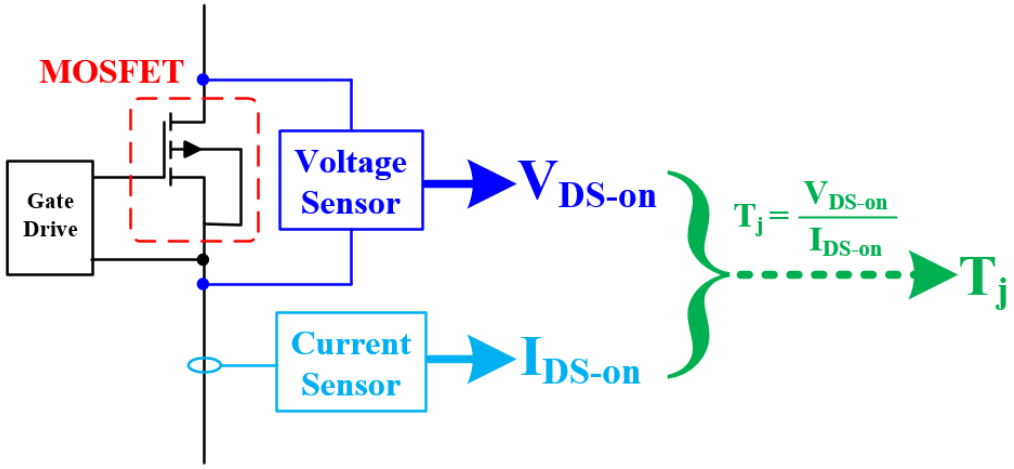


Fig. 1.5.2 Power MOSFET T_j sensing based on $R_{DS\text{-}on}$. $R_{DS\text{-}on}$ is calculated by $V_{DS\text{-}on}$ from voltage sensor and $I_{DS\text{-}on}$ from current sensor

The power MOSFET I-V curve usually has a very linear region, as shown in Fig. 1.5.3 (ON Semiconductor NDF11N50ZG N-channel MOSFET). The linear region ensures that the equivalent on-state resistance defined in (1.5.2) is not $I_{DS\text{-}on}$ sensitive. The linear I-V curve is a unique property of FET based power semiconductors. Other devices like IGBT usually do not have such a linear region, thus defining a load current dependent on-state resistance is infeasible for those devices.

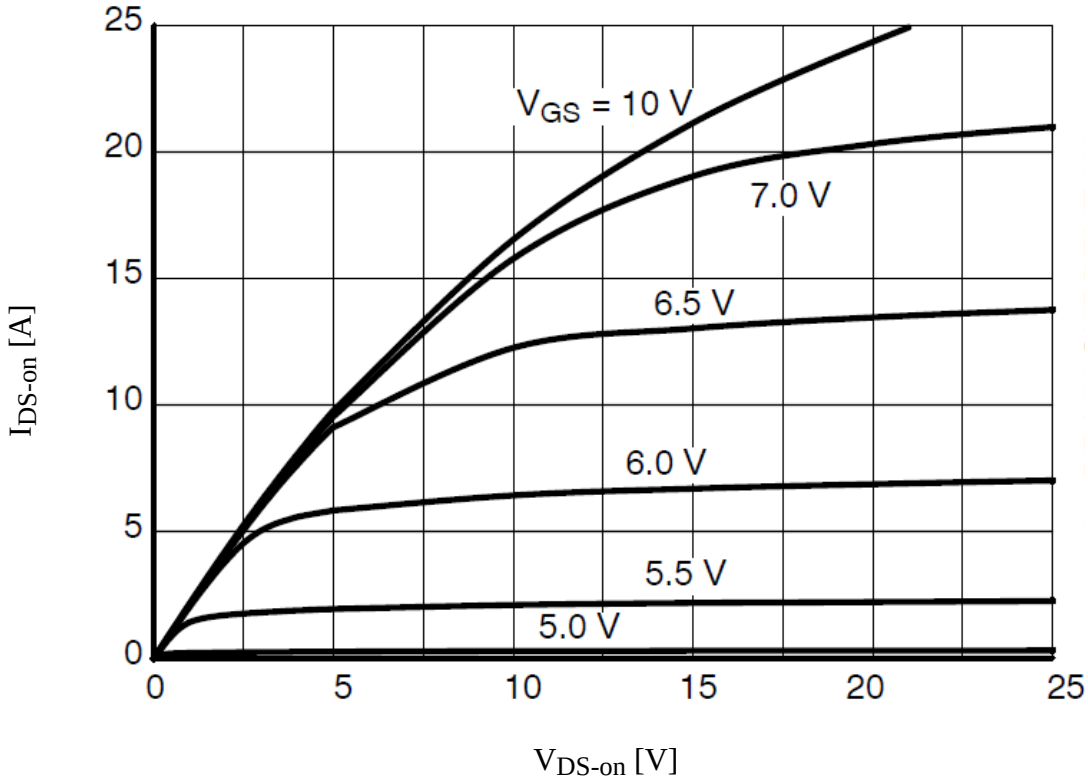


Fig. 1.5.3 ON Semiconductor NDF11N50ZG N-channel MOSFET I-V curve

Based on the discusion in section 1.1.1, the MOSFET I-V linear region is manipulated by the MOSFET gate-to-source voltage V_{GS}. By properly setting the V_{GS} value (generally between 12V and 18V), the MOSFET linear region can cover nearly all the MOSFET steady state operating region.

Using the MOFSET I-V linear region, the equivalent on-state resistance $R_{DS\text{-}on}$ can be calculated. However, this linear region is not rigorously linear, and the $R_{DS\text{-}on}$ should be considered as an approximation. When V_{GS} is fixed, junction temperature Tj and load current $I_{DS\text{-}on}$ can make the MOSFET I-V cureve shifted. The "$R_{DS\text{-}on} - I_{DS\text{-}on}$" dependency and the "$R_{DS\text{-}on} - T_j$" dependency of ON Semiconductor NDF11N50ZG N-channel MOSFET is shown in Fig. 1.5.4 and Fig. 1.5.5, respectively.

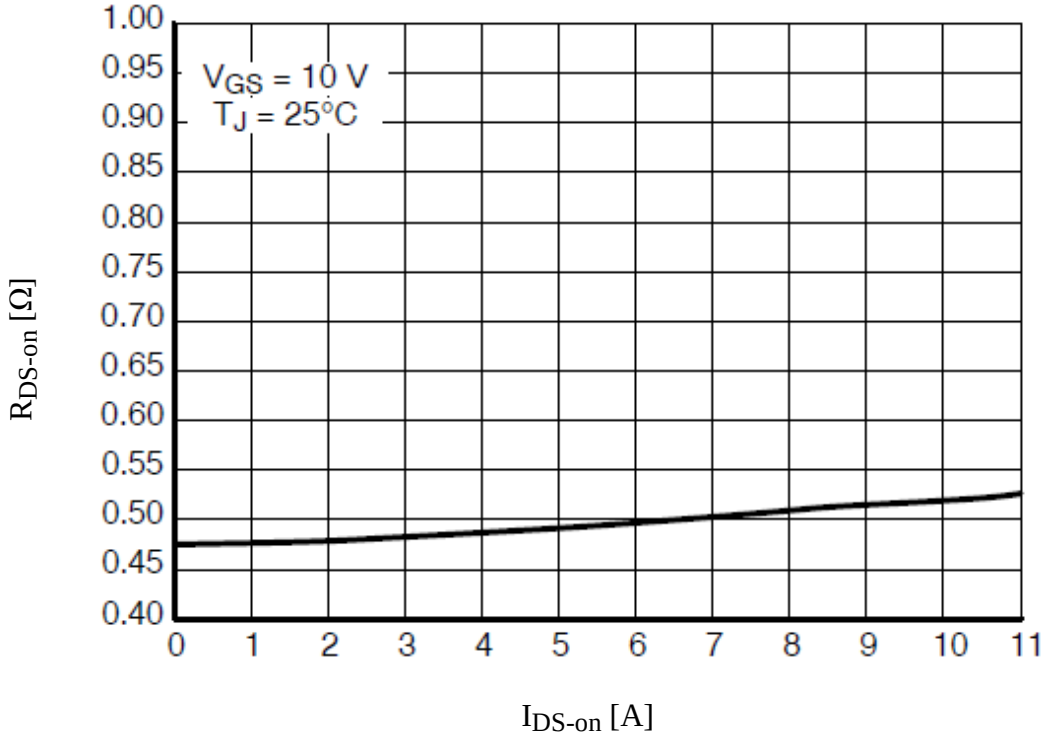


Fig. 1.5.4 ON Semiconductor NDF11N50ZG N-channel MOSFET "$R_{DS-on} - I_{DS-on}$" dependency

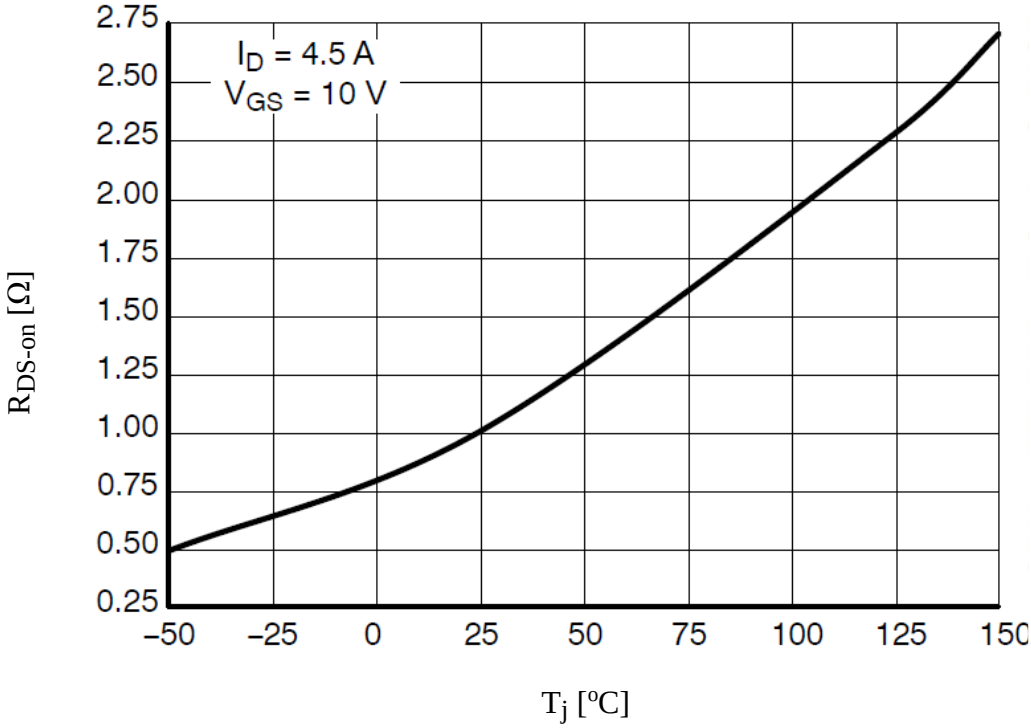


Fig. 1.5.5 ON Semiconductor NDF11N50ZG N-channel MOSFET "$R_{DS-on} - T_j$" dependency

Fig. 1.5.4 and Fig. 1.5.5 cover the entire MOSFET current and temperature operating region. The dependency curve in both figures indicate that when IDS-on increases from 0A to 11A, a 10% R_{DS-on} change is observered. When T_j increases from 25ºC to 150ºC, R_{DS-on} is increased by 175%. To conclude, the "$R_{DS-on} - T_j$" dependency is the dominant factor compared with I_{DS-on}. Consequently, using the "$R_{DS-on} - T_j$" dependency to estimate MOSFET T_j with fixed V_{GS} is considered to be feasible.

Based on (1.5.2), V_{DS-on} and I_{DS-on} need to be measured during the MOSFET on-state. The measurement of I_{DS-on} can be achieved non-invasively using a current transducer. However, to measure the MOSFET V_{DS-on}, invasive methods are most

commonly used. Either embedded in the MOSFET package, or by use of an additional voltage sensor, detector nodes have to be connected to the MOSFET's drain terminal and source terminal. Therefore, galvanic isolation is necessary inside the voltage sensor to keep the MOSFET isolated from the power supply of the voltage sensor. In addition, the voltage sensor should have enough sensing resolution to detect the change of $V_{DS\text{-}on}$ but should also have the capability to stand the big voltage stress during MOSFET off-state.

Regardless of the additional cost for the galvanically isolated voltage sensor, this method is commonly used for power converter calibration in lab benchmark, and power MOSFET T_j sensing in industry applications.

1.5.3 Using IGBT "$V_{CE} - T_j$" Dependency for T_j Sensing

The IGBT on-state collector-emitter voltage drop V_{CE} is T_j dependent, thus it can be used for IGBT online T_j sensing [23] [24]. Indeed, IGBT V_{CE} is also on-state current I_C dependent [23], thus measuring I_C is also required for the V_{CE} based IGBT T_j sensing, as shown in Fig. 1.5.6. By online measuring V_{CE} and I_C, the IGBT T_j can be correlated in real time based on a three dimensional "$V_{CE} - I_C - T_j$" relationship like Fig. 1.5.7, [26].

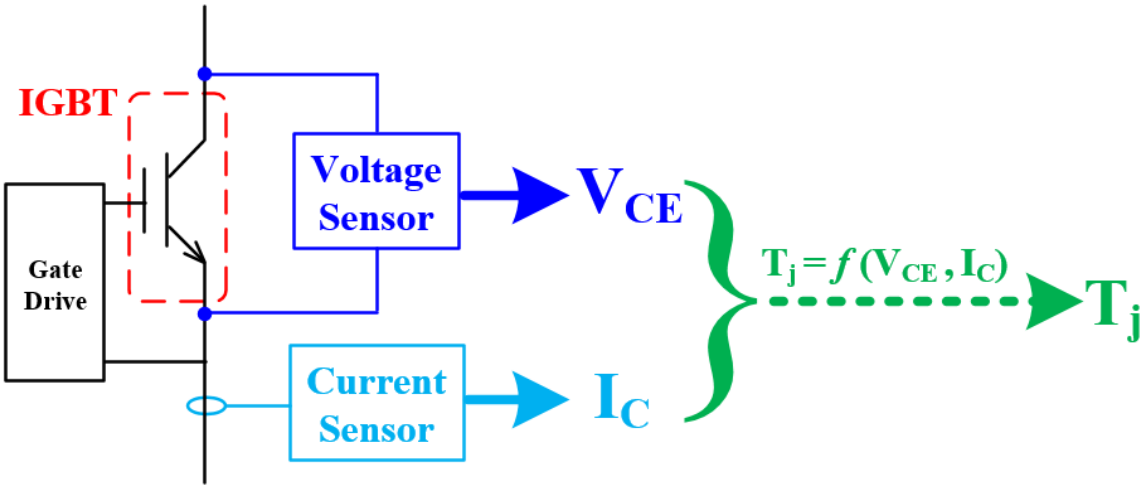


Fig. 1.5.6 IGBT T_j sensing based on on-state V_{CE} and I_C. V_{CE} and I_C are measured by voltage and current sensor respectively.

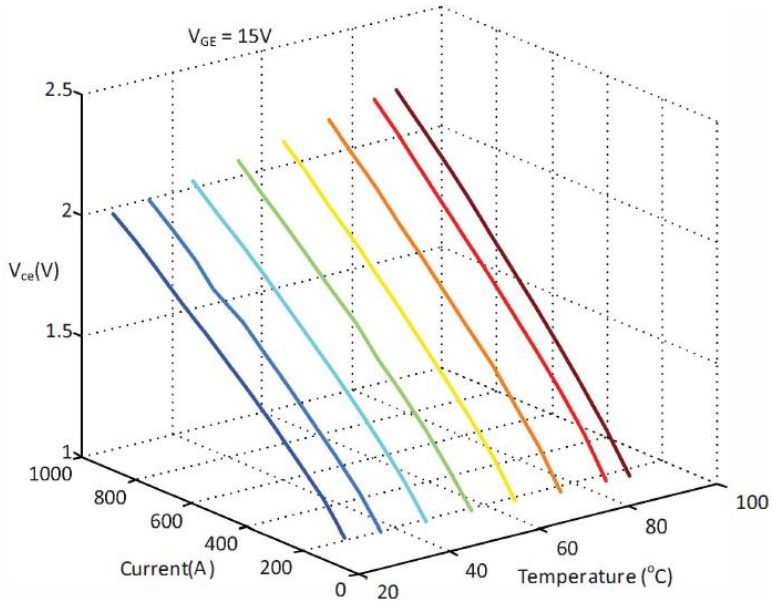


Fig. 1.5.7 Typical three dimensional "V_{CE} – I_C – T_j" relationship for IGBT

Modeling IGBT as a function of T_j is necessary for understanding the mechanism and limit of the "$V_{CE} - T_j$" based temperature sensing methodology. Based on the IGBT thermal-electrical model proposed in [27], the on-state voltage drop between IGBT collector and emitter are non-linearly correlated. Simlutation results based on the IGBT thermal-electrical model are shown in Fig. 1.5.8, where the on-state V_{CE} is the non-linear function of the collector current I_C and junction temperature T_j.

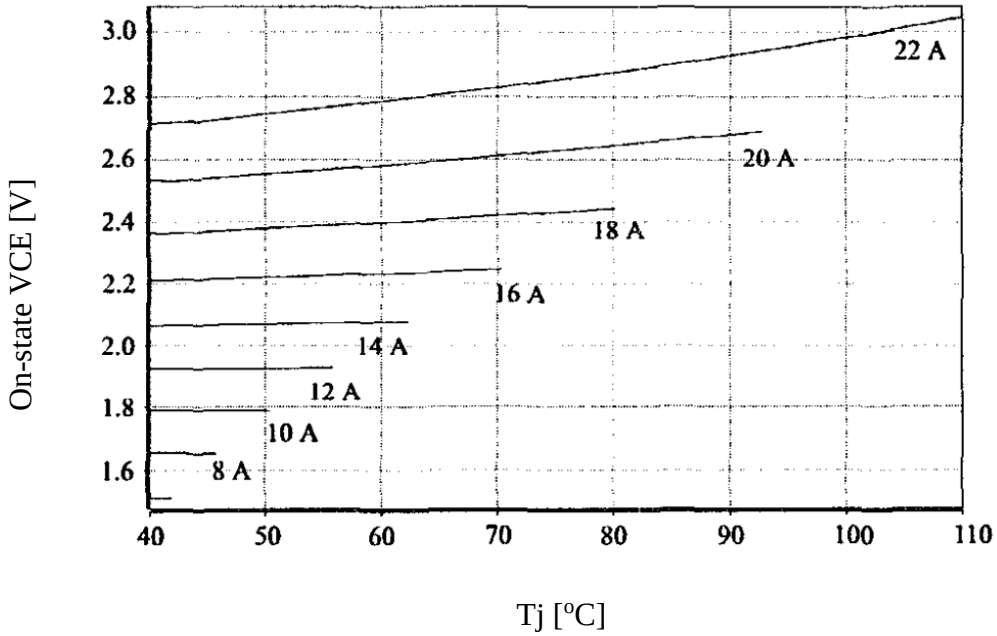


Fig. 1.5.8 Simulated IGBT non-linear "$V_{CE} - I_C - T_j$" relationship based on the model propsed in [27].

Individual tests on IGBT "$V_{CE} - I_C$" dependency and "$V_{CE} - T_j$" dependency are shown in Fig. 1.5.9 and Fig. 1.5.10, respectively. The two test results indicate that both the I_C and T_j can explicitly change the value of V_{CE}. This is different from the on-state T_j dependency of MOSFET, which is dominated by T_j. As a result, a three dimensional

correlation, like Fig. 1.5.7, is necessary for the "$V_{CE} - I_C - T_j$" relationship based IGBT online T_j sensing.

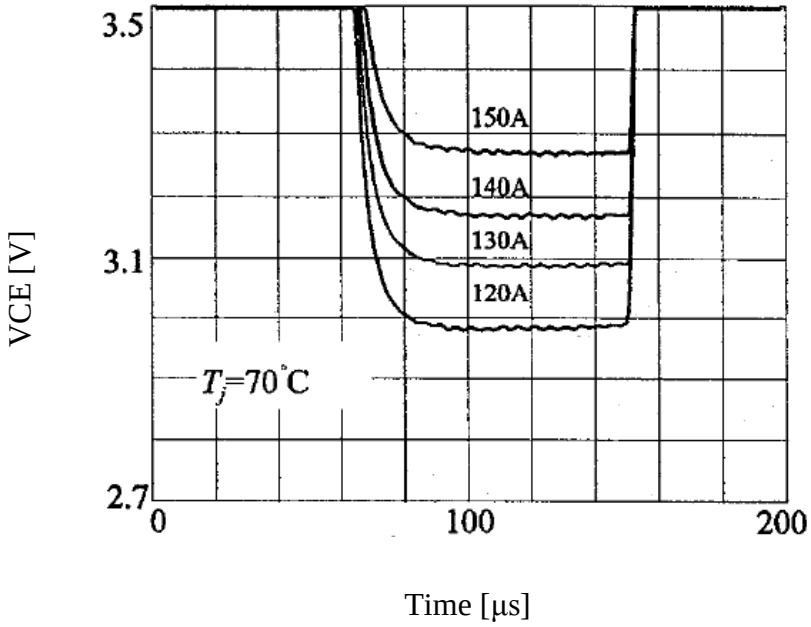


Fig. 1.5.9 IGBT "$V_{CE} - I_C$" dependency with fixed T_j

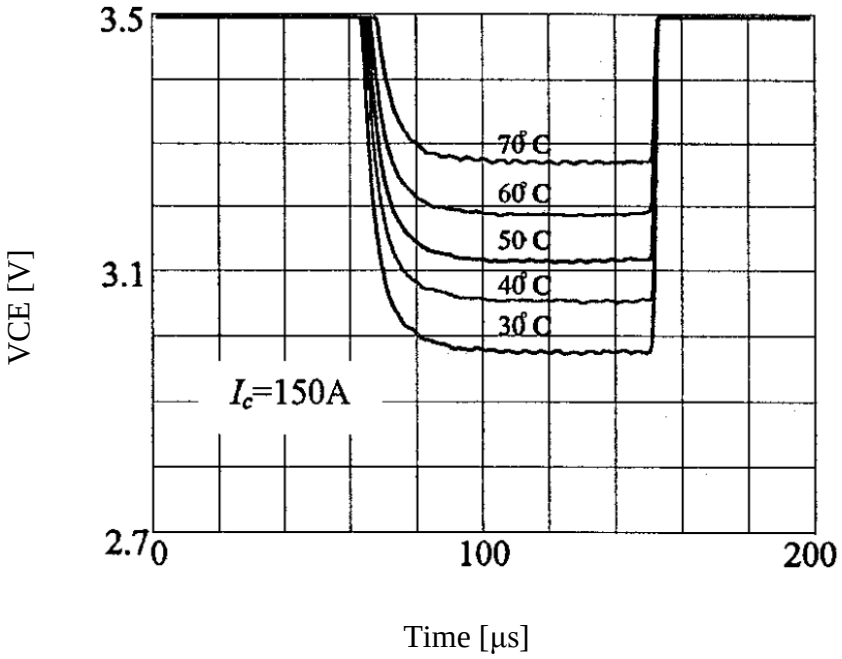


Fig. 1.5.10 IGBT "$V_{CE} - T_j$" dependency with fixed I_C

[28] studied the temperature gradient on the IGBT semiconductor chip when using this V_{CE} based T_j sensing method. [28] claims that the measured V_{CE} and I_C can be correlated to the "current-weighted chip temperature", the "area-weighted chip temperature", and the "peak chip temperature" based on the design and geometry of a semiconductor.

Both the R_{DS-on} based MOSFET T_j sensing and the V_{CE} based IGBT T_j sensing need to measure the voltage across the device and the current through the device. The voltage sensing is invasively connected to the MOSFET/IGBT power terminals. Consequently, galvanic isolation is required for the voltage sensor. When the switching semiconductor is on, the T_j dependent voltage across the device is usually within 5V. When the switching semiconductor is off, the big voltage stress across the device will

also be applied to the voltage sensor. As a result, a floating voltage sensor with good resolution and enough voltage stress rating is necessary for the voltage measurement.

The on-state properties based T_j sensing is suitable for simple topologies like single ending DCDC converters. With more switching semiconductors used in the converter, high resolution voltage sensing and high voltage isolation for each switching semiconductor can largely increase the volume of the converter system.

Because the frequency of the converter load current is much slower compared with converter switching frequency, the semiconductor current can be taken as constant within several switching cycles. Thus high bandwidth load current measurement is not required for the device on-state properties based T_j sensing, and the voltage sensing bandwidth will determine the T_j sensing bandwidth for the device on-state properties based T_j sensing [29]. Generally, the voltage sensing bandwidth for the switching semiconductor voltage is above 100kHz [23].

1.6 T_j Sensing Based on Device Switching Transient "Duration Time"

The T_j dependency of power semiconductor switching transients is another option for online T_j sensing. The T_j sensing can be achieved every time the switching power semiconductor is turned on or off. Thus the maximum bandwidth of the device switching transient properties based T_j sensing depends on the device switching frequency.

The device switching transient properties based T_j sensing methods can be categorized as methods that measure delay time, methods that measure amplitude, or methods that measure resonation.

For those methods that measure the duration time of a specific signal, accurate time counters are required.

1.6.1 Using IGBT Miller Plateau Duration Time for T_j Sensing

[30] uses the IGBT gate emitter voltage V_{GE} for online T_j sensing. It is proved that the Miller plateau width of V_{GE} during the IGBT turn-off is T_j sensitive, as shown in Fig. 1.6.1 in [30]. The online measured V_{GE} turn-off Miller plateau duration time can be correlated to IGBT T_j based on the "Miller plateau duration – T_j" relationship, as shown in Fig. 1.6.2.

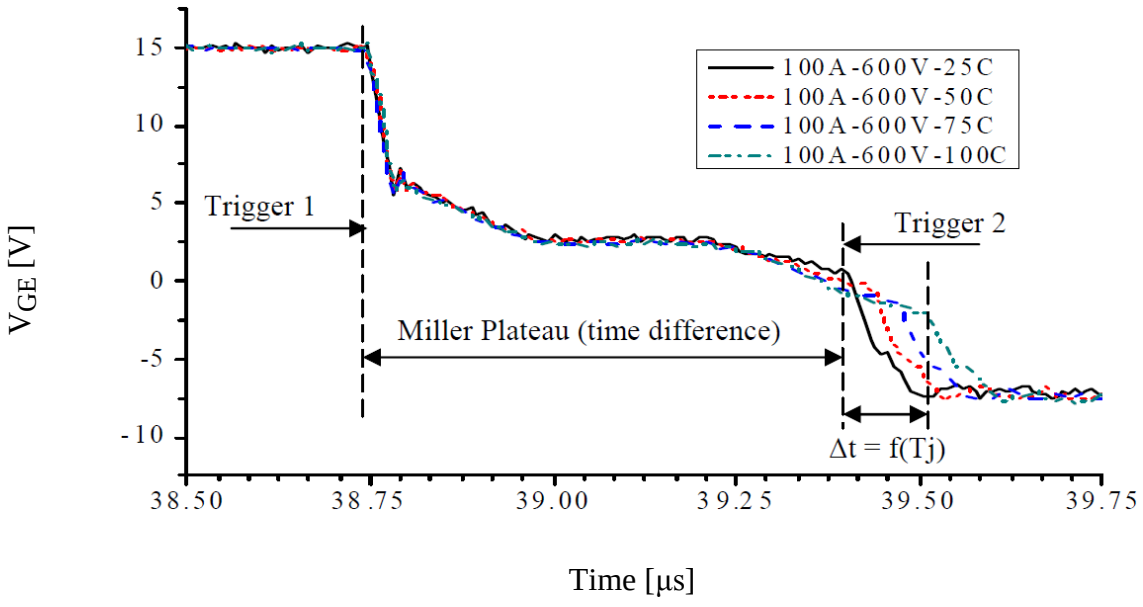


Fig. 1.6.1 VGE waveform temperature dependency at IGBT turn-off transient

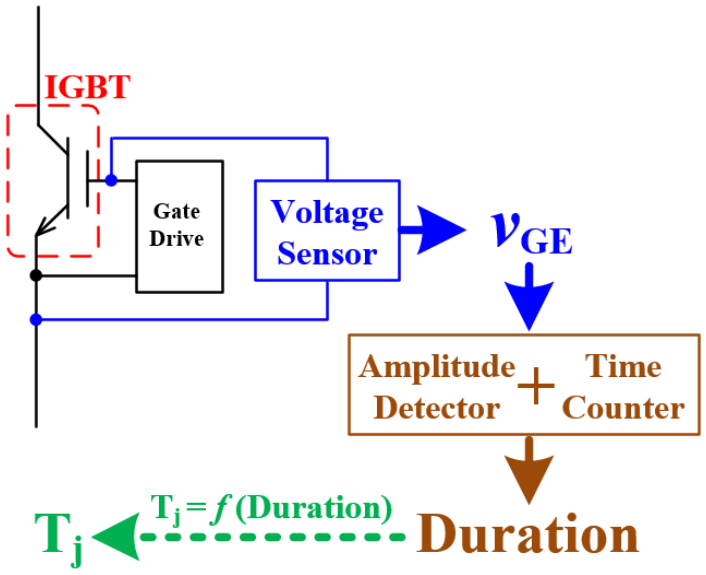


Fig. 1.6.2 IGBT T_j sensing based on turn-off Miller plateau duration

[30] claimed that the Miller Plateau time difference (t_{diff}) is linearly correlated to the measured IGBT T_j. The T_j sensitivity of the Miller Plateau is found to be 1.2ns/^oC when the power module is operating at 600V, 100A, as shown in Fig. 1.6.3.

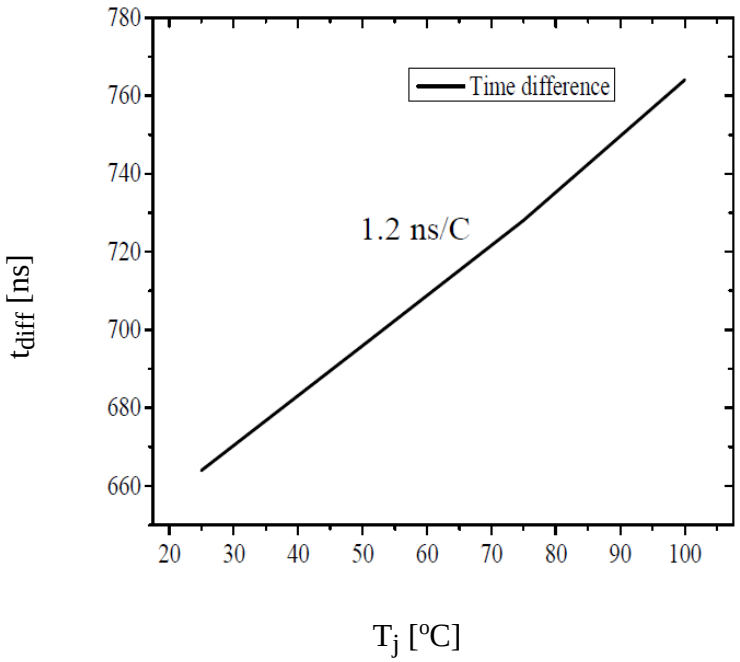


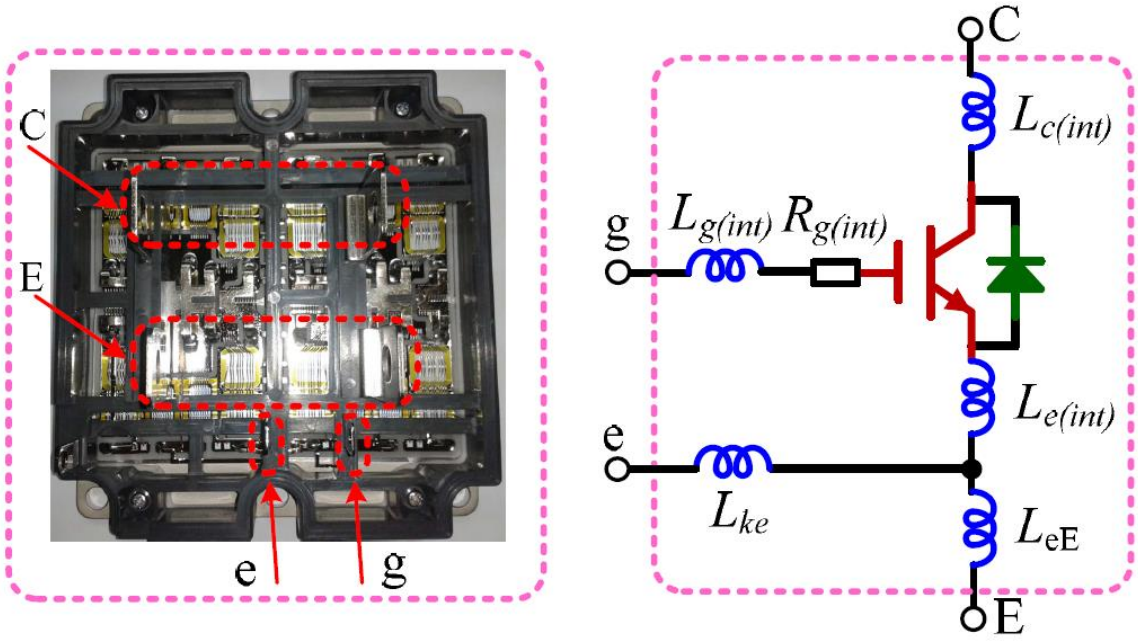
Fig. 1.6.3 T_j vs. t_{diff}, IGBT operated at 600 V, 100A

1.6.2 Using IGBT V_{eE} Delay Time for T_j Sensing

The high power IGBT module comprises a complex multilayer structure of different materials, where a package structure is shown in Fig. 1.6.4 (a), [31].

High power IGBT module consists of a group of IGBT die and anti-parallel diode die, connected in parallel. The dies are connected by aluminum bond wires to upper copper layers to form sub-modules, and sub-modules are connected with copper layers and to the power bus terminals. In this case, the parasitic inductance is in the current flow path, and the manufacturers attempt to minimize it. The internal parasitic inductance equivalent circuit of a high power IGBT module is shown in Fig. 1.6.4 (b), where $L_{c(int)}$, $L_{e(int)}$ and $L_{g(int)}$ represent the parasitic inductances from the power collector C, the power emitter E and the gate; $R_{g(int)}$ is the internal gate driver resistance; L_{ke} represents

the parasitic inductance from the Kelvin emitter connection; L_E is the parasitic inductance from the power emitter connection. The parasitic inductance between the Kelvin emitter and power emitter L_{eE} is the sum of L_E and L_{ke}.



(a) Package Structure (b) Equivalent Circuit

Fig. 1.6.4 Power IGBT module package structure and equivalent circuit with parasitic inductance

In the IGBT turn-off transient, the induced voltage between the Kelvin emitter and the power emitter (referred to as "V_{eE}") has two spikes with amplitudes of 3V and 5V respectively, as shown in Fig. 1.6.5. [31] claims that the delay time between the two spikes (also referred to as "V_{eE} delay time") is IGBT T_j sensitive.

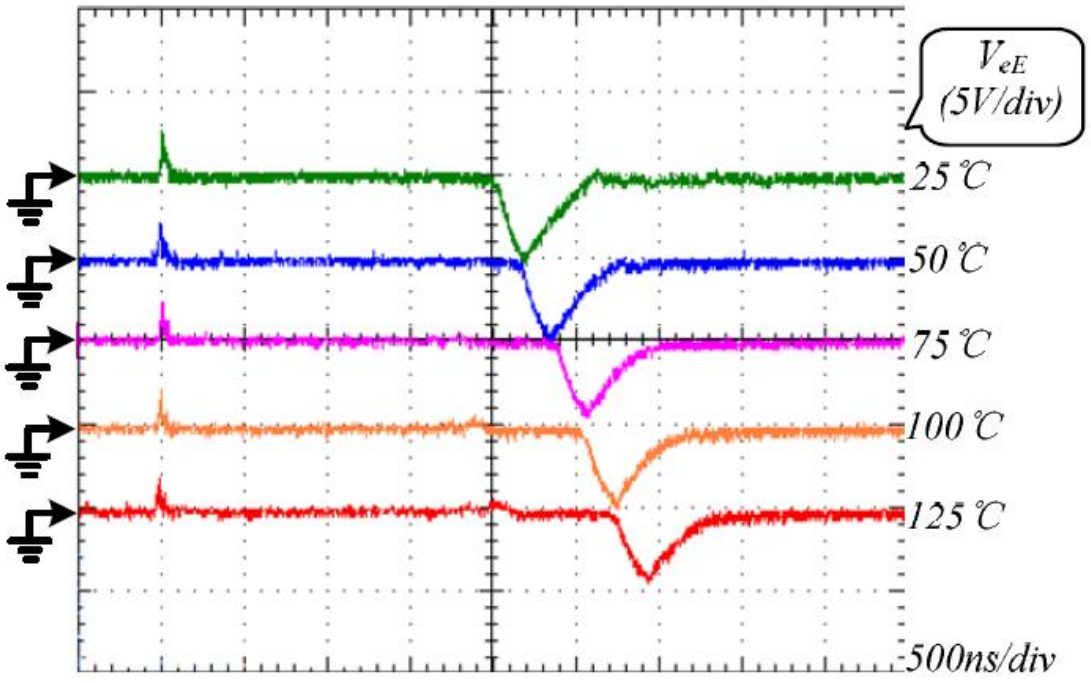


Fig. 1.6.6 Experimental results of V_{eE} delay under different T_j

The V_{eE} delay time can be measured online and correlated to T_j based on the "V_{eE} delay time – T_j" relationship as shown in Fig. 1.6.7 [31]. The illustration for this method is shown in Fig. 1.6.8. With 1°C of T_j variation, the change of the V_{eE} delay time is 8ns.

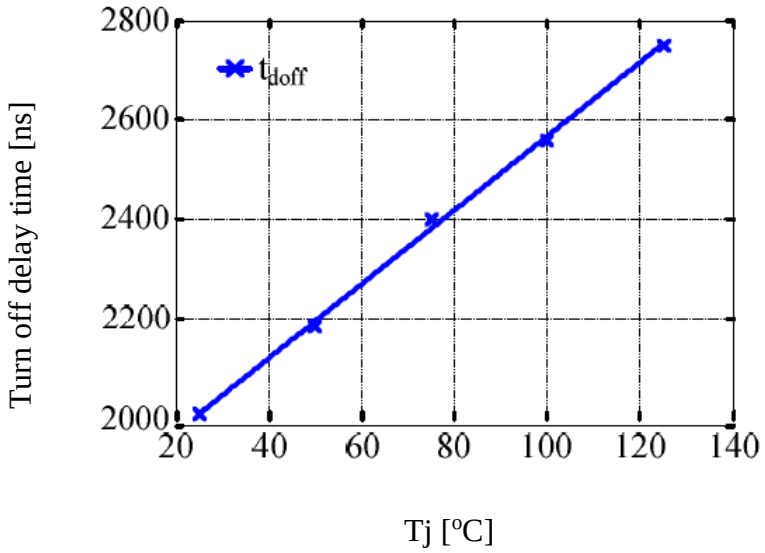


Fig. 1.6.7 "V_{eE} delay time – T_j" relationship

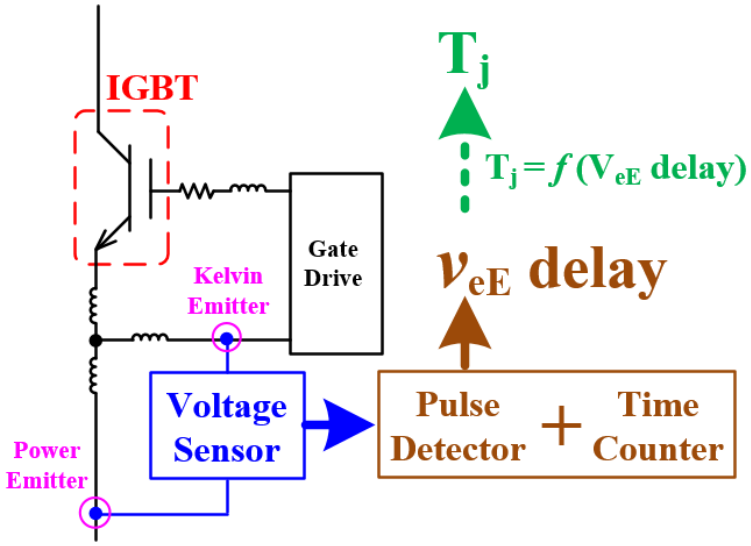


Fig. 1.6.8 IGBT T_j sensing based on V_{eE} delay. V_{eE} delay is measure by pulse detector and time counter.

For the two methods discussed in [30] and [31], high bandwidth voltage comparators (1GHz minimum) and a high resolution time counters (at least 1ns/step) are required for industrial applications. The method from [30] measures V_{GE}, thus the T_j sensing implementation can be integrated into IGBT gate drive. The method from [31] needs to have access to both Kelvin emitter and power emitter, and in such a case T_j sensing is better to be embedded inside the power module or placed very close to the power module. Consider that the voltage measurements in [30] and [31] both use the IGBT emitter as voltage reference, for one IGBT chip, its T_j sensing system and its gate drive system can share the same isolated power supply.

1.7 T_j Sensing Based on Device Switching Transient "Amplitude"

For those methods that measure the amplitude of a specific signal, accurate analog to digital conversions are required.

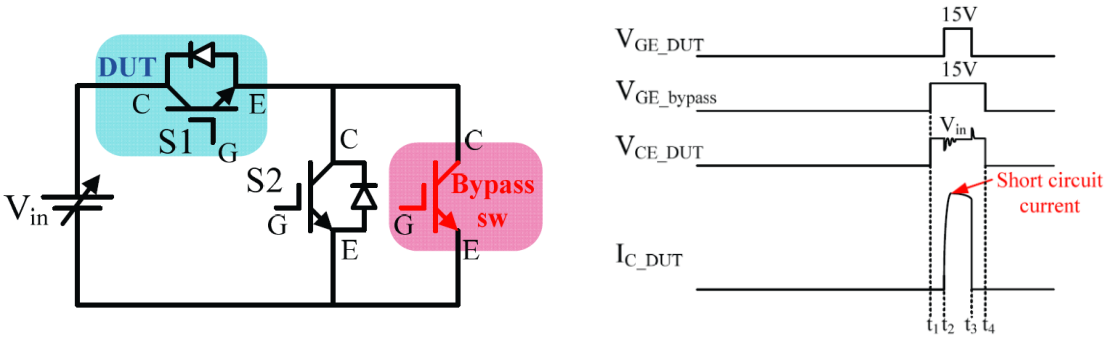
1.7.1 Using IGBT Short Circuit Current for T_j Sensing

[32] proposed that IGBT T_j can be measured using IGBT short circuit current I_{SC}. I_{SC} is a negative temperature coefficient quantity, and [32] has investigated that the IGBT T_j can be correlated to the amplitude of IGBT short circuit current peak.

Simulation and experimental results in [32] indicate that I_{SC} has an adequate T_j sensitivity and linearity. In addition, I_{SC} is not sensitive to device voltage stress, gate

drive voltage, or load. By creating a short circuit pulse (hard switching short circuit fault), the I_{SC} pulse amplitude can be used for T_j online sensing.

To demonstrate the T_j dependency of I_{SC}, a calibration is achieved on an IGBT power module by [32]. Fig. 1.7.1 (a) shows the circuit schematic for calibration. The IGBT power module composed of two IGBT and diode cells is connected directly to the DC bus. During a short circuit period, the short circuit current is determined by the device under test (DUT) IGBT or its complementary IGBT, depending which has a higher junction temperature. To eliminate the effect of the complementary IGBT, a bypass IGBT is connected in parallel with the complementary IGBT. The bypass IGBT has larger current rating than the DUT. When the short circuit occurs, the short circuit current is limited by the DUT, and the bypass IGBT and the complementary IGBT still remain in the saturation region. The illustration for the I_{SC} based T_j estimation method is shown in Fig. 1.7.2.



(a) Circuit Schematic (b) IGBT module switching waveforms

Fig. 1.7.1 Calibration for "I_{SC} – T_j" sensitivity

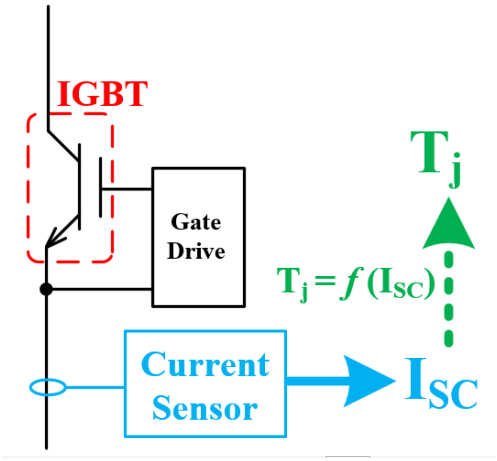


Fig. 1.7.2 IGBT T_j sensing based on short circuit current. I_{SC} is measured by current sensor.

The short circuit current value should be recorded after V_{GE} and V_{CE} pass the switching transients and become steady state. In this case, the short circuit current value at 3μs after the short circuit occurs is used for T_j estimation. Considering the DUT self-heating due to power dissipation generated during the short circuit pulse, the same hold-on time (3μs in this case) should be applied in the actual T_j measurement so as to compensate the self-heating effect. A moving average is applied to the sensed current raw data, and the current value at 3μs is recorded, with the value of 207.4A at 15°C and 174.2A at 110°C.

The short circuit current values I_{SC} at various T_j are recorded, as shown in Fig. 1.7.3. The short circuit current has an adequate temperature sensitivity of 0.345 A/°C and linearity. It is noted that the temperature in the curve is the device junction temperature before short circuit occurs, not at the time when the short circuit currentis recorded. With

the calibration curve, the IGBT junction temperature during converter operation can be derived from the short circuit current value.

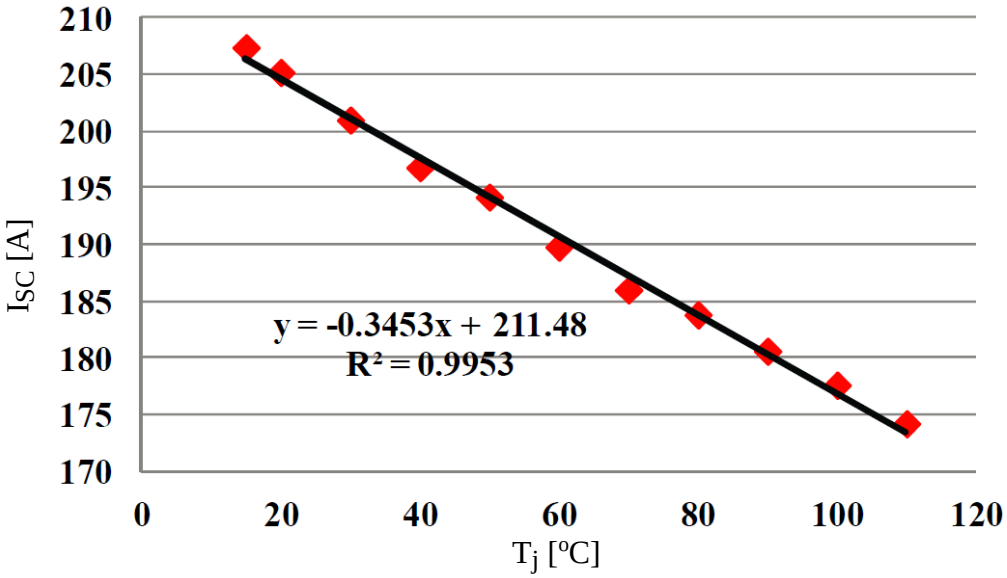


Fig. 1.7.3 Short circuit current ISC as a function of T_j (V_{GE}=15 V, V_{CE}=650 V). R^2 is the coefficient of determination and indicates how well data fit a statistical model.

Under short circuit condition, an IGBT has to sustain both high voltage and high current at the same time. Thus the local device temperature will be significantly increased because of high power dissipation. High local temperature beyond a critical value can increase device degradation and eventually lead to device destruction.

Although I_{SC} can be measured non-invasively using the current transducer, the frequently applied short circuit pulse might not be acceptable by the same hardware implementations. Accordingly, the frequency and the application strategy of I_{SC} should be carefully considered in the online T_j sensing applications.

1.7.2 Using IGBT V_{eE} peak value for T_j Sensing

Similar to [31], [33] also uses the voltage between the Kelvin emitter and the power emitter V_{eE} for IGBT T_j sensing. Thus both methods from [31] and [33], for one IGBT chip, its T_j sensing system can share the power supply with its gate drive system, and the T_j sensing system can be integrated inside the IGBT module. Different from [31] that studies the delay time between the two pulses during IGBT turn-off, [33] only focuses on one of the V_{eE} turn-off pulse. The illustration for this method is shown in Fig. 1.7.4.

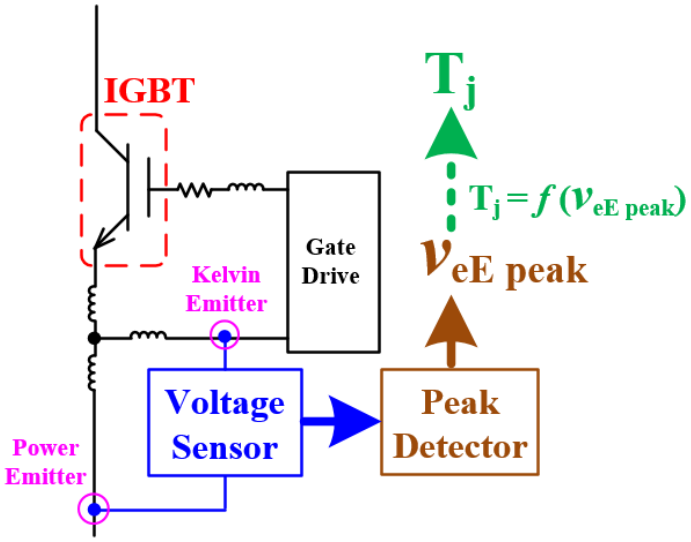


Fig. 1.7.4 IGBT T_j sensing based on turn-off V_{eE} pulse peak. V_{eE} pulse peak is measured by peak detector.

The parasitic inductance L_p between the Kelvin emitter (e) and the power emitter (E) terminals (as shown in Fig. 1.7.4) can be used as a sensor to extract the junction

temperature the IGBT. The derivative of the collector current flowing through this parasitic inductance (L_p) generates a voltage drop given by equation (1.7.1).

$$V_{eE} = L_p \frac{dI_c}{dt} \tag{1.7.1}$$

Where V_{eE} is the voltage drop measured between the Kelvin emitter and the power emitter, L_p is the parasitic inductance across which V_{eE} is measured, Ic is the collector current. The parasitic inductor L_p is shown in Fig. 1.7.4 between the Kelvin emitter (e) and the power emitter terminal (E). The Tj dependent VeE waveform is shown in Fig. 1.7.5.

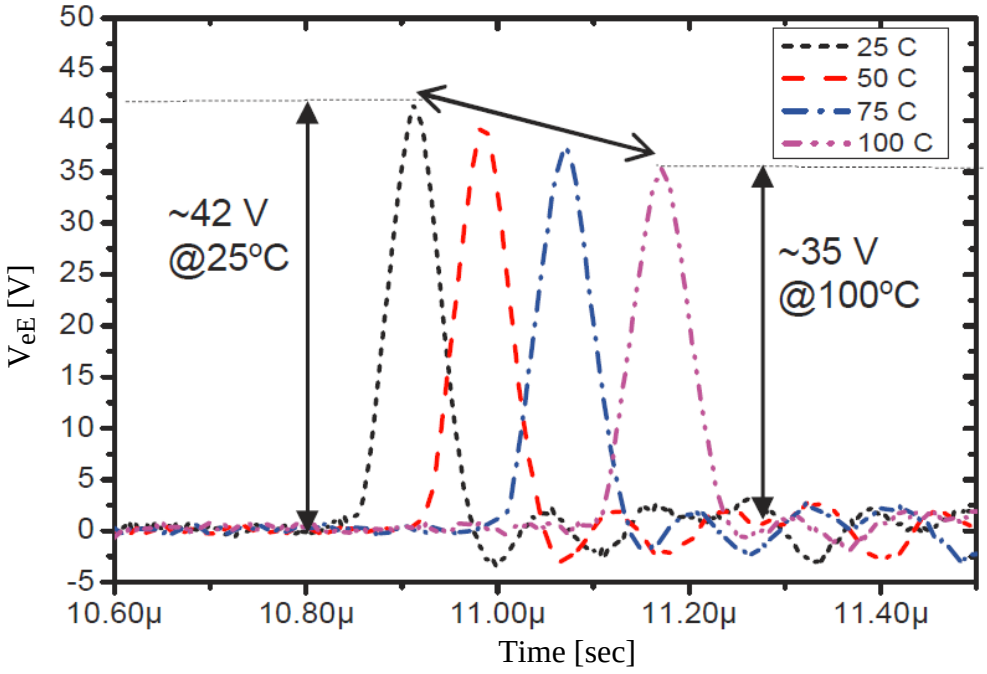


Fig. 1.7.5 V_{eE} across the parasitic inductance for IGBT module at 600 V, 200 A switching condition under different T_j

By using either an integration method or a peak detection method, the amplitude of V_{eE} turn-off pulse can be measured and correlated to IGBT T_j based on the "$V_{eE} - T_j$"

relationship as shown in Fig. 1.7.6. To include the effect of I_c, the "$\int V_{eE} - I_c$" relationship is measured as shown in Fig. 1.7.7.

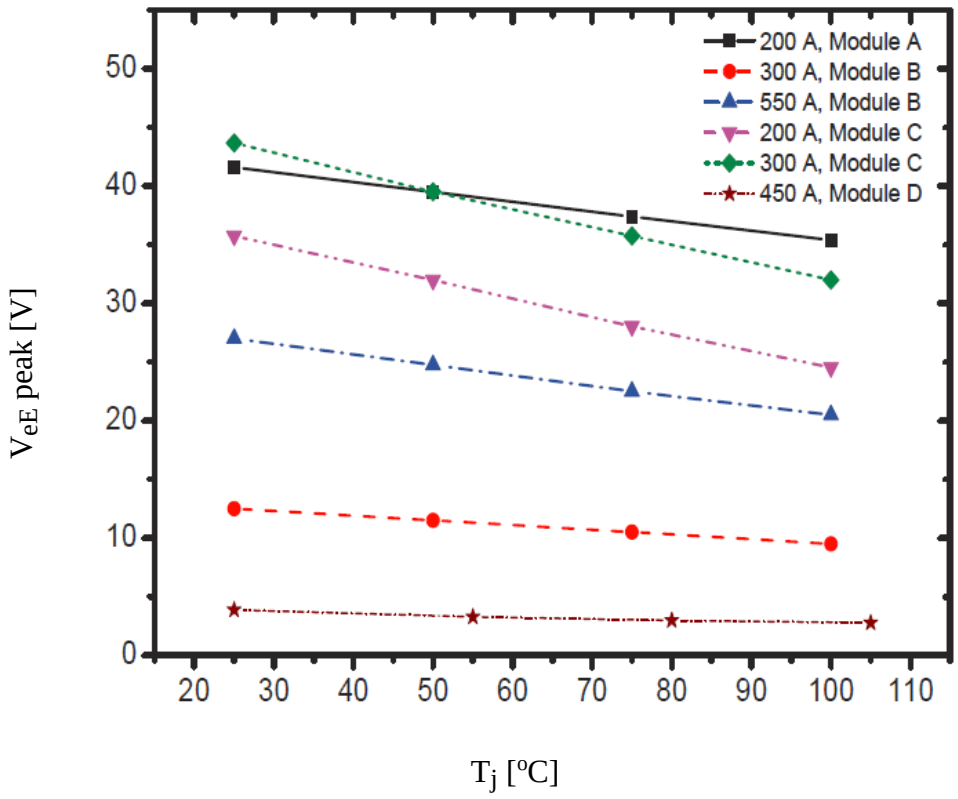


Fig. 1.7.6 The peak amplitude of V_{eE} as a function of T_j measured using peak detector at 600 V for IGBT modules A, B, C and at 900V for IGBT module D.

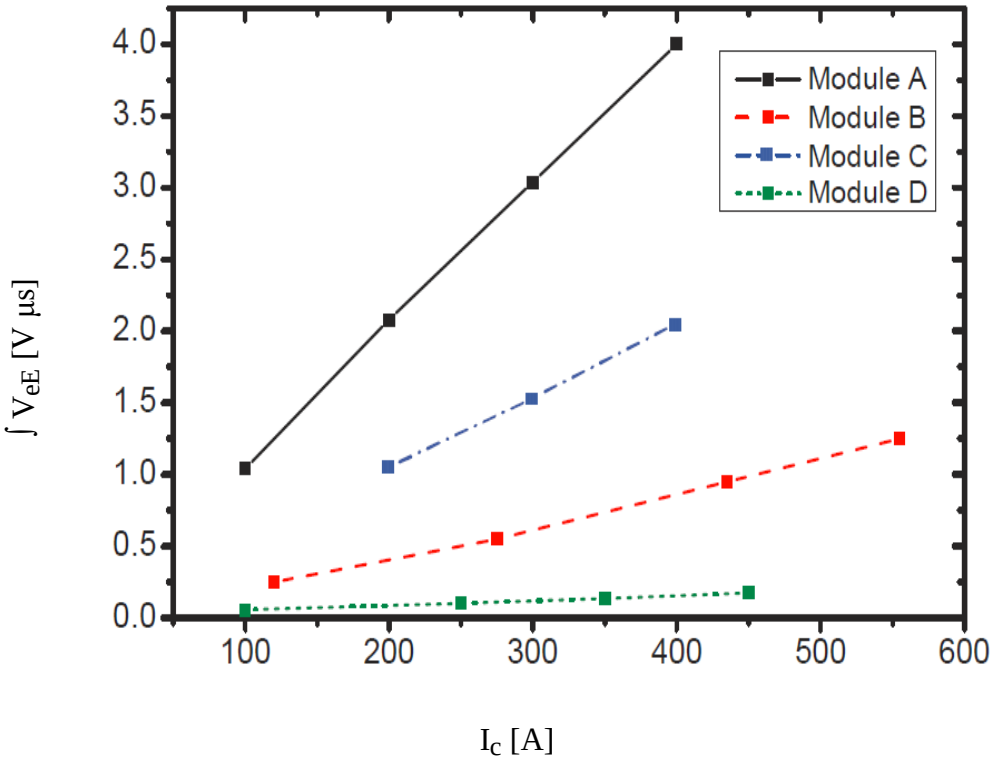


Fig. 1.7.6 The integrator output as a function of load current measured for IGBT modules A, B, C and D.

1.7.3 Using MOSFET V_{TH} for T_j Sensing

The MOSFET turn-on threshold voltage V_{TH} usually has significant T_j dependency. [34] investigated the T_j dependency of the gate threshold voltage V_{TH} and used it for online T_j sensing based on the "$V_{TH} - T_j$" relationship.

Fig. 1.7.7 shows the turn-on waveforms of a power MOSFET. At turn-on (t=0) the gate-source voltage V_{GS} starts to rise while the drain-source voltage V_{DS} and drain current I_d remain constant. The voltage V_{GS} at the time t_d(on) is generally considered as the threshold voltage V_{TH}. As t_d(on) drain current starts to increase, and V_{GS} will keep increasing. The rising time of I_d is regarded as tri in the Fig. 1.7.7. When the drain

current I_d stop increasing, the Miller Effect can be observed where the gate-source voltage remains constant (Miller Plateau). In the Miller Plateau duration t_{fv}, the drain-source voltage collapses. After the Miller Plateau period, the voltage, $V_{GS,}$ start to increase again and ultimately reach the desired on-state V_{GS} value.

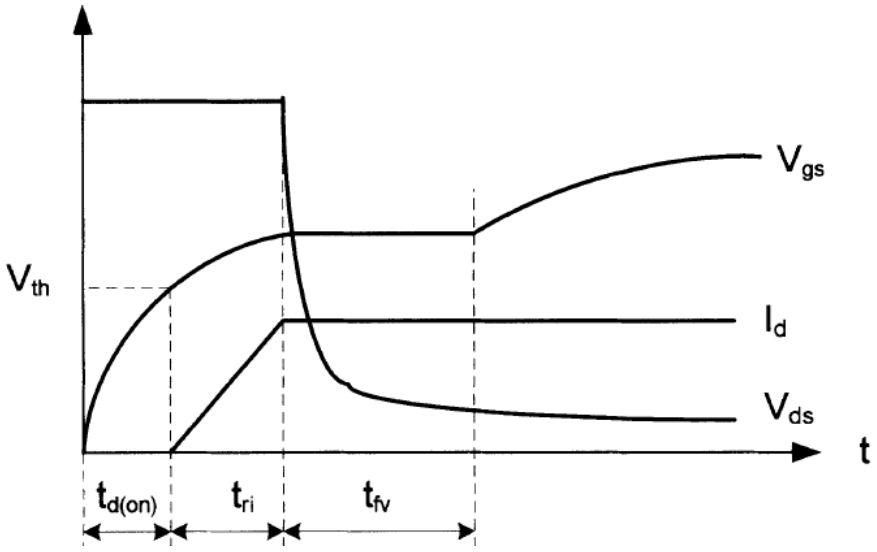


Fig. 1.7.7 Power MOSFET turn-on transient waveforms

The temperature dependency of the threshold voltage is given by (1.7.2) and (1.7.3), where Ψ_B is the distance of the Fermi level from the mid-gap, εsi is the dielectric constant of silicon, NA is the doping density, q is the charge of an electron, $E_g(0)$ is the bandgap at T=0K, COX is the intrinsic gate-channel oxide capacitance and T is the channel temperature.

$$\frac{dV_{TH}}{dT} = \frac{d\Psi_B}{dT}\left(2 + \frac{1}{C_{ox}}\sqrt{\frac{\varepsilon_{si} q N_A}{\Psi_B}}\right) \tag{1.7.2}$$

$$\frac{d\Psi_B}{dT} \approx \frac{1}{T}\left(\frac{E_g(0)}{2q} - |\Psi_B|\right) \tag{1.7.3}$$

A 3mV/^{o}C V_{TH} sensitivity was found experimentally, as shown in Fig. 1.7.8. To measure V_{TH} online, high speed circuitry that synchronously detects the turn-on transient of V_{GS} and drain current is required. To synchronize voltage and current during semiconductor turn-on transient, the circuit design and implementation can be challenging. An illustration for the V_{TH} based T_j sensing is shown in Fig. 1.7.9.

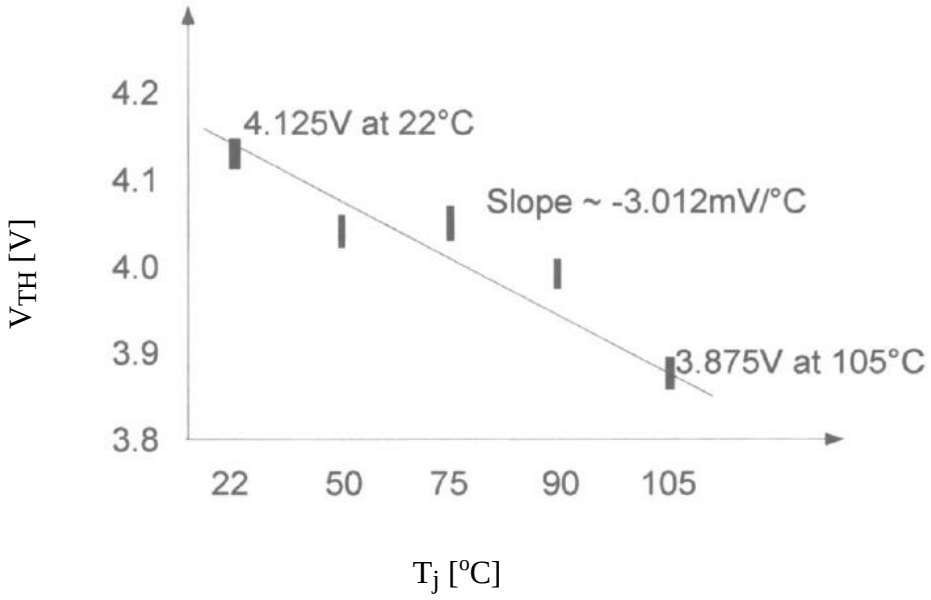


Fig. 1.7.8 Experimentally derived "$V_{TH} - T_j$" relationship

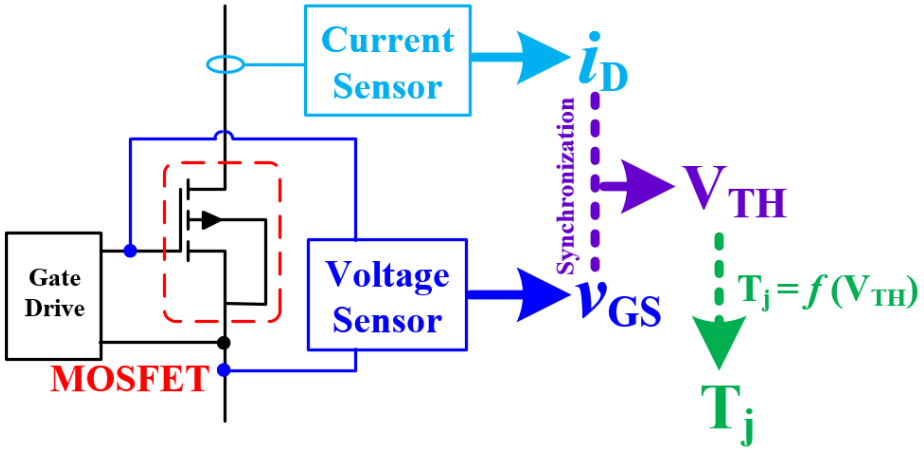


Fig. 1.7.9 Power MOSFET T_j sensing based on V_{TH}. V_{TH} is measured by synchronized i_D and v_{GS}.

1.7.4 Using IGBT V_{GE} Integration for T_j Sensing

[35] claims that the IGBT gate drive turn-on transient gate voltage V_{GE} is T_j sensitive. A series of IGBT V_{GE} waveforms experimentally measured during turn-on transient is shown in Fig. 1.7.10.

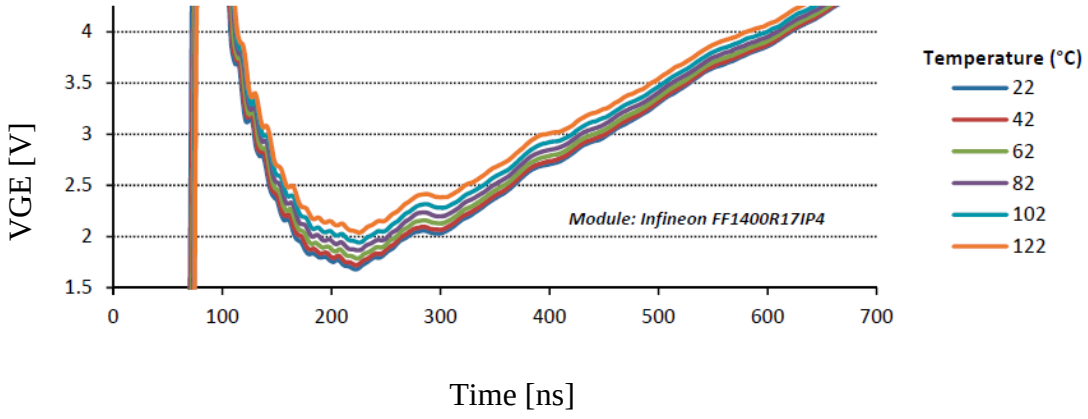


Fig. 1.7.10 Infineon FF1400R17IP4 IGBT V_{GS} turn-on transient under different T_j

Further study indicates that the integration of an IGBT turn-on V_{GE} transient (referred to as "$\int V_{GE}$") is T_j sensitive. By referring to the "$\int V_{GE} - T_j$" relationship online, T_j can be estimated with a resolution of 84mV/^{o}C. Since only V_{GE} needs to be measured, the T_j sensing circuit can be designed inside the gate drive circuit, as shown in Fig. 1.7.11.

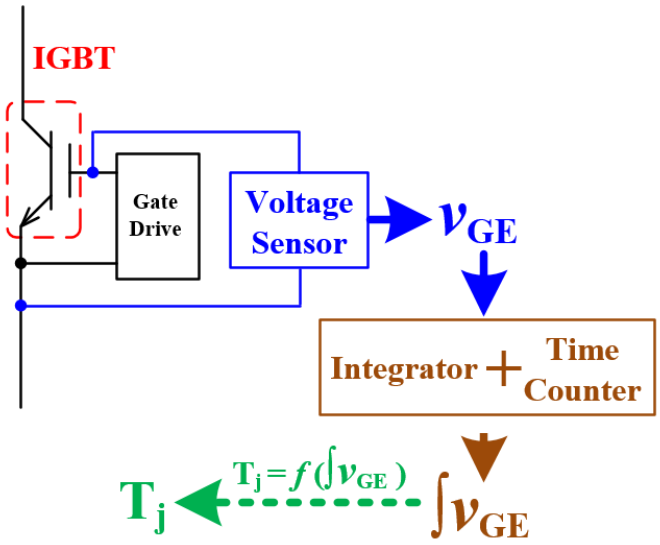


Fig. 1.7.11 IGBT T_j sensing based on $\int V_{GE}$. $\int V_{GE}$ is measured by integrator and time counter

Since the TSEP has an effect on the dynamic interaction between the switching semiconductor and its gate drive system, the gate drive turn-on output characteristics are T_j sensitive. Hereby the switching semiconductor gate drive turn-on output transient current another option for the T_j sensing of power MOSFET [36] and IGBT [37]. Both [36] and [37] implement the T_j sensing inside the gate drive system and measure only the

gate drive turn-on output transient current i_G, as shown in Fig. 10 and Fig. 11. In such cases, T_j sensing implementation only needs to access to semiconductor gate terminals, and the semiconductor power terminals (MOSFET drain and source; IGBT collector and emitter) are not invasively accessed. [36] proposed a peak detection method applied to i_G so that the online measured i_G peak can be correlated to T_j based on the "$i_{G\ peak} - T_j$" relationship as shown in figure 15 in [36]. A 2.4mA/^{o}C T_j sensitivity can be found in figure 15 in [36]. [37] used the integration of i_G for T_j sensing based on the "$\int i_G - T_j$" relationship as shown in figure 20 in [37]. Figure 20 from [37] indicates a 0.34%/^{o}C T_j sensitivity.

1.8 T_j Sensing Based on Device Switching Transient Ringing

Sensing requirements for fast MOSFET T_j control and high power fast switching power converter protection are not easily met with non-intrusive techniques. Many studies have focused on non-invasive circuit modeling-based sensing methods suitable for high bandwidth, hard-switching converter power MOSFET junction temperature estimation without any additional temperature detector.

The ringing superimposed with circuit load current have proven to be T_j sensitive and thus, can be used for MOSFET T_j sensing. Different resonant tank from the converter hardware implementation can generate different frequency component of ringings during the switching transient. Typically, a "power supply-$R_{DS\text{-}on}$-L-C" resonant model can generate ringings at a few hundred kilo herz, and a "gate drive-$R_{DS\text{-}on}$-L-C" can generate ringings up to several mega herz. In this section, the resonant tank

modeling will include gate-drive output parasitics, power MOSFET intrinsic parameters, PCB parasitics and load parasitics.

1.8.1 T_j Sensing Based on the "power supply-R_{DS-on}-L-C" Resonance

The ringing signal from the switching transient is commonly observed in converter load current/voltage waveforms. [23] [38] demonstate that the ringing waveforms contain the switching power semiconductor relative T_j information.

Because the lightly damped natural transient decay envelope that occurs at switch turn-on is dependent to the on-resistance of the MOSFET (or the on-state forward voltage of the IGBT), the resulted ringing waveforms will be T_j sensitive. These waveforms naturally occur at the input/output bus of most of the switching converter topologies. Non-invasive extraction of the temperature information from the converter output ringing would provide a non-invasive, non-contact, realtime sensing technology that would utilize the available periodic switching noise intrinsic to the input/output bus. Furthermore, this methodology is experimentally verified to have a compatible sensing accuracy compared with those traditional temperature sensors and temperature signal communication hardware [38].

Analysis of the measured converter output ringing consists of filtering and system identification [39]. Since the output voltage/current ringing waveform will be distorted by the non-linear characteristics of the circuit (i.e. diode reverse recovery current, gate-drive output ringing, active power supply, etc), the 'power supply-R_{DS-on}-L-C' ringing needs to be extracted using signal processing techniques.

Generally, MOSFET $R_{DS\text{-}on}$ has a positive T_j coefficient, and this means that an increase in temperature will cause an increase in the on-state resistance. Thus, as the power MOSFET changes in temperature, the sinusoidal oscillations of the ringing signal decay at a temperature dependent rate. It was investigated in [40] that the temperature of the power MOSFET could be estimated from the decay envelope of the ringing waveform. Fig. 1.8.1 presents an example of a lightly damped current ringing waveform. The characteristic exponential decay envelope is also included in the waveform.

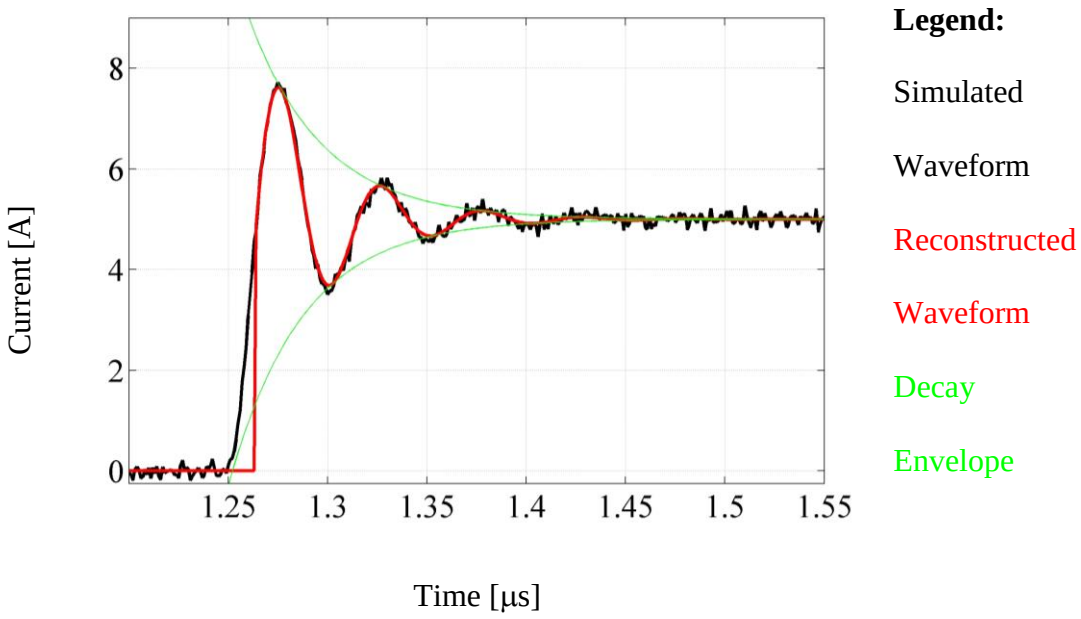


Fig. 1.8.1 Lightly damped current waveform during switching with decay envelope

In [38] and [41], it was further investigated that the switching transient ringing is caused by the parasitic inductances and capacitances within the device. The decay of the ringing is due to the on-state losses of the device. The transient, high frequency model for the power MOSFET in a boost converter configuration shown in Fig. 1.8.2 shows these parasitic elements.

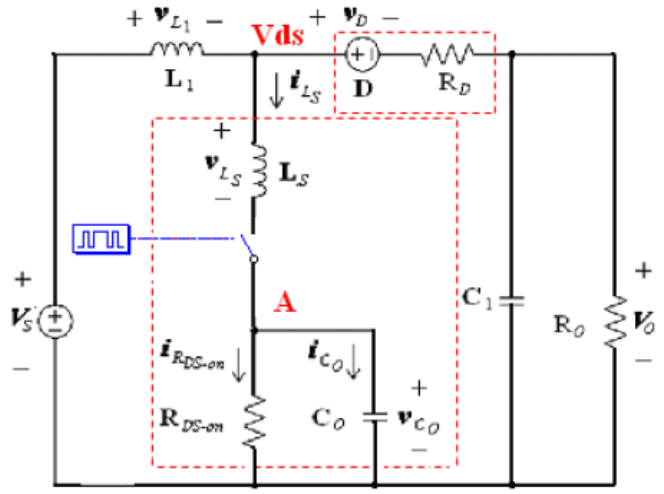


Fig. 1.8.2 Boost converter model includeing MOSFET and diode parasitics

The analysis of this circuit can be simplified to the MOSFET on-state and MOSFET off-state, as shown in Fig. 1.8.3.

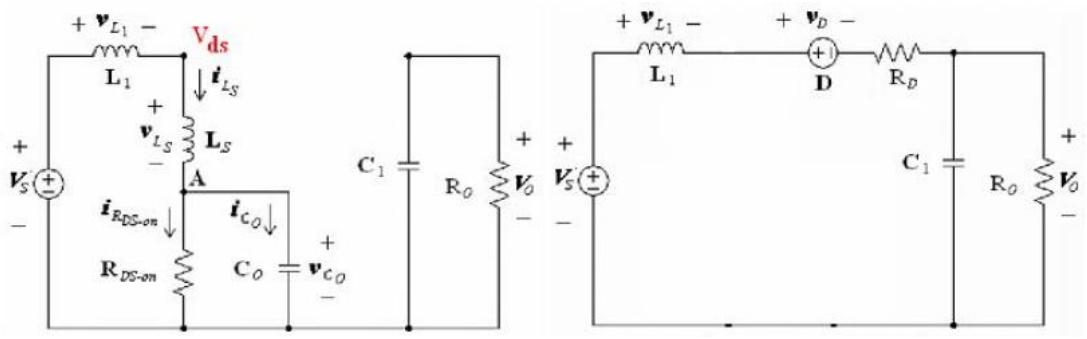


Fig. 1.8.3 Boost converter showing MOSFET on-state (left) and off-state (right)

The behavior of the power MOSFET during a switching transient can be described as that of an under-damped LCR circuit under nearly step excitation. This analysis is based on the following assumptions:

1. $L_1 >> L_s$
2. $C_1 >> C_o$
3. When the switch is on $R_D >> R_{DS\text{-}on}$

Use Kirchhoff's voltage and current laws to solve for the MOSFET voltage V_{DS} at turn-on, the solution of V_{C_o} yields to the second order differential equation (1.8.1).

$$\frac{d^2V_{C_o}}{dt} + \frac{1}{R_{DS\text{-}on}C_o}\frac{dV_{C_o}}{dt} + \frac{1}{L_sC_o}V_{C_o} = \frac{V_S - V_{L_1}}{L_sC_o} \qquad (1.8.1)$$

The homogeneous solution is given in (1.8.2), which is the lightly damped natural response case.

$$V_{C_o}(t) = e^{-at}\left(Ae^{jbt} + Be^{-jbt}\right) \qquad (1.8.2)$$

where

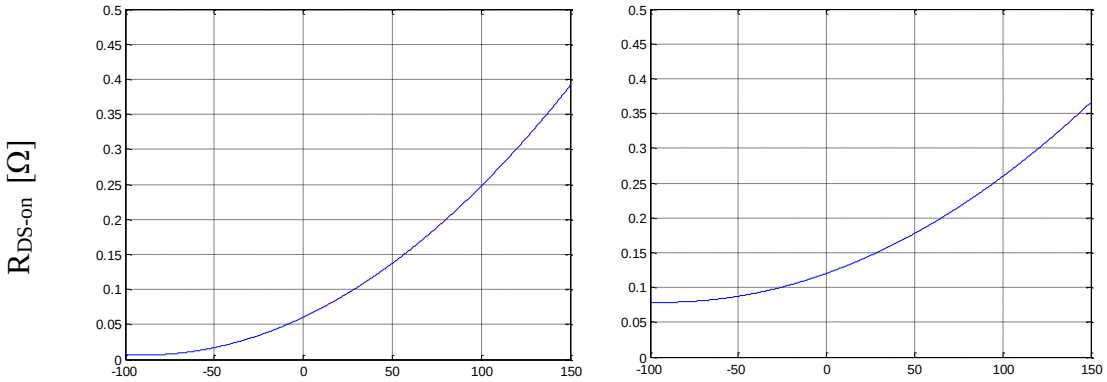
$$b = \sqrt{\frac{1}{L_sC_o} - \left(\frac{1}{2R_{DS\text{-}on}C_o}\right)^2}$$

and

$$a = \frac{1}{2R_{DS\text{-}on}C_o}$$

The solution in (1.8.2) indicates that the exponential decay envelope e^{-at} is directly related to $V_{DS\text{-}on}$ of the MOSFET switch, which is temperature dependent. The complex exponential terms represent the resonant frequency harmonic, which is primarily dependent on L_S and C_O. The harmonic amplitude coefficients, a and b, are dependent on the initial conditions. Of these parameters, only the $R_{DS\text{-}on}$ is significantly temperature-related.

The function of MOSFET $R_{DS\text{-}on}$ with respect to temperature is usually provided by MOSFET manufacture. Fig. 1.8.4 gives example graphs showing the $R_{DS\text{-}on}$ temperature dependency for the 2SK3522 and the 2SK3697.



2SK3522 2SK3697

Fig. 1.8.4 2SK3522 and the 2SK3697 temperature dependency

It can be seen that R_{DS-on} increases with temperature as semiconductor carrier mobility decreases with temperature. This accounts for the MOSFET's characteristic positive temperature coefficient. Consequently, the sinusoidal oscillations of the ringing signal decay at a temperature dependent rate as the power MOSFET changes in temperature. It was first hypothesized in [42] that the temperature of the power MOSFET could be estimated from the decay envelope of the ringing waveform.

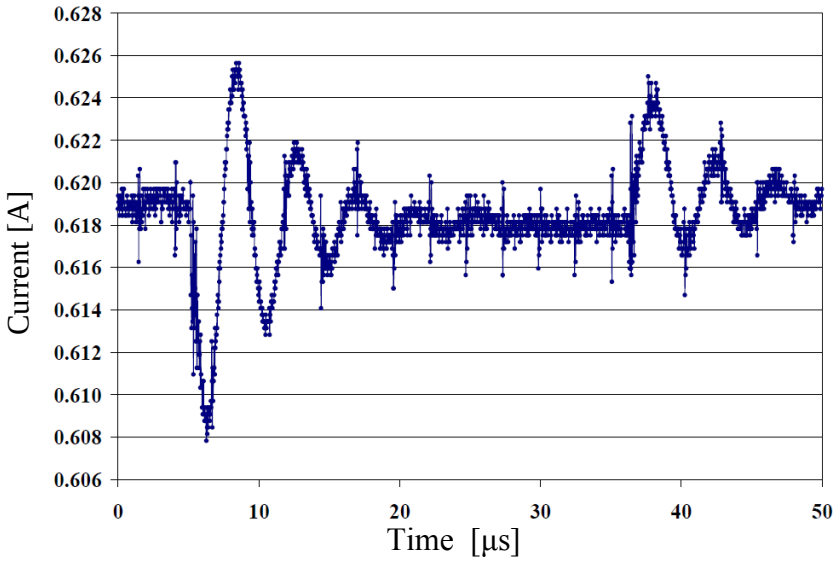


Fig. 1.8.5 Typical converter output current ringing waveform

A typical converter output current ringing waveform is shown in Fig. 1.8.5. It can be seen that current ringing is approximately sinusoidal with exponential decay. This waveform matches the solution for a second order system.

1.8.2 T_j Sensing Based on the "gate drive-R_{DS-on}-L-C" Resonance

In contrast to the "power supply-R_{DS-on}-L-C" ringing signal, the "gate drive-R_{DS-on}-L-C" ringing signal is another option for high bandwidth MOSFET T_j sensing. In this case, the ringing superimposed on the load current waveform is mostly determined by the gate-drive output capability, MOSFET intrinsic parameters, PCB layout parasitics between gate-drive, and the MOSFET (usually in a small area of the PCB, and of simple shape for analysis). The frequency of this "gate drive-R_{DS-on}-L-C" ringing is faster than the "power supply-R_{DS-on}-L-C" ringing and most of the potential harmonic distortion. It also has low harmonic distortion, making the "power supply-R_{DS-on}-L-C" based T_j sensing method have a higher resolution in real-time implementation.

Based on the turn-on mechanism of the power MOSFET [43] [44], the dynamic modeling for a Fuji 2SK3677-01MR power MOSFET is illustrated in Fig. 1.8.6. This model only includes the MOSFET turn-on dynamic characteristic modeling, parasitic capacitance, lead and bonding wire parasitic impedance, and the V_{GS}, V_{BS} amplifying effect (g_m and g_{mBS}) [45].

For analysis and simulation consideration, a simplified model is shown in Fig. 1.8.7. In this simplified model, R_{BS} and C_{BS} are set to zero because the bulk node is internally connected to the source terminal. C_{GB} is negligible in comparison with C_{GS}.

The amplifying effect of V_{GS} and V_{BS} are replaced by $(g_m+1)C_{GD}$. This is because the MOSFET is initially turned on in the saturated zone.

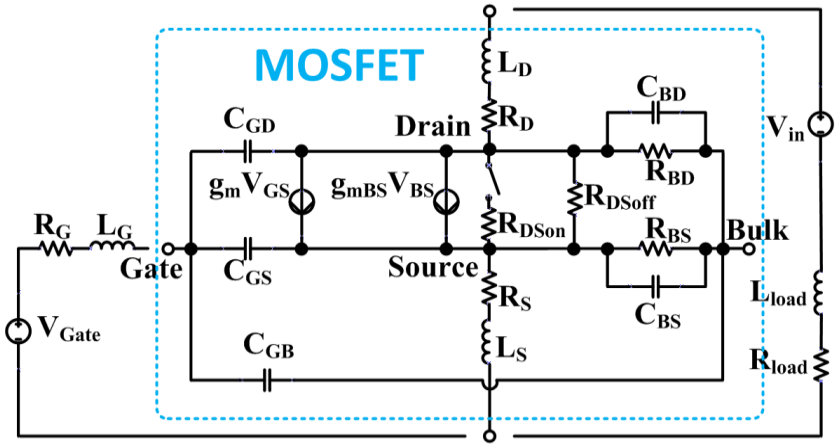


Fig. 1.8.6 MOSFET dynamic model

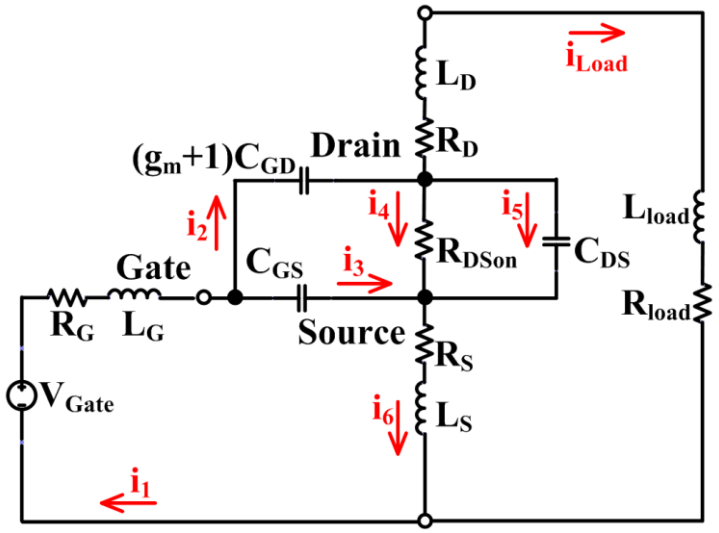


Fig. 1.8.7 Simplified MOSFET dynamic model

In this simplified model, a relatively fast resonant loop ('gate drive-R_{DS-on}-L-C') is formed by the following component: R_G, L_G, C_{GD}, C_{GS}, R_{DS-on}, C_{DS}, R_S and L_S. In

comparison with the values of resonant loop components, R_{Load} and L_{Load} are too big to have a significant effect on the ringing frequency or damping ratio. For the MOSFET intrinsic parameters, $R_{DS\text{-}on}$ is T_j sensitive as shown in Fig. 1.8.8.

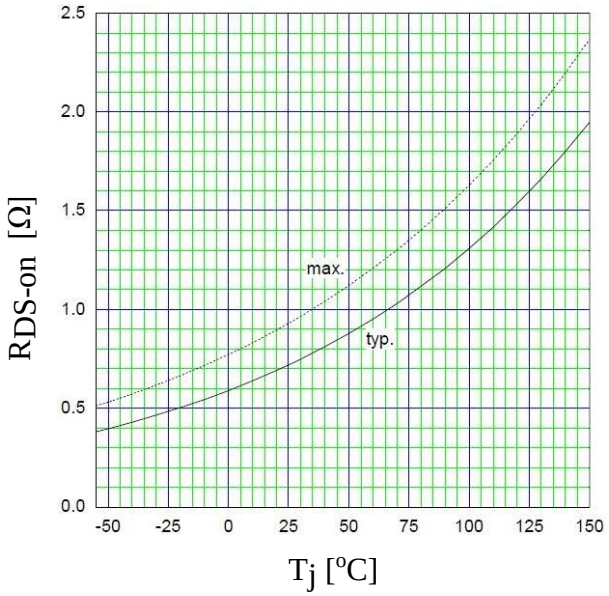


Fig. 1.8.8 Fuji 2SK3677-01MR MOSFET '$R_{DS\text{-}on}$–T_j' characteristic from its datasheet

Meanwhile, $R_{DS\text{-}on}$ is one of the dominant parameters for this resonant system's damping ratio. It will be shown in the experimental results that the value of $R_{DS\text{-}on}$ determines the time constant of the ringing superimposed on the load current waveform. By detecting the time constant of the superimposed ringing when the MOSFET is turned on, $R_{DS\text{-}on}$ and consequently the MOSFET junction temperature can then be estimated. Using Kirchhoff's law on the "gate drive-$R_{DS\text{-}on}$-L-C", the following circuit equations, (1.8.3) to (1.8.14), can be derived.

$$V_{Gate} = R_G i_1 + L_G \frac{di_1}{dt} + U_{C_{GS}} + R_S i_6 + L_S \frac{di_6}{dt} \qquad (1.8.3)$$

$$U_{C_{GS}} = U_{C_{GD}*}+R_{DSon}i_4 \tag{1.8.4}$$

$$R_{DSon}i_4+R_S i_6+L_S\frac{di_6}{dt} = (R_D+R_{Load})i_L+(L_{Load}+L_D)\frac{di_L}{dt} \tag{1.8.5}$$

$$R_{DSon}\, i_4 = U_{C_{DS}} \tag{1.8.6}$$

$$i_3 = C_{GS}\frac{dU_{C_{GS}}}{dt} \tag{1.8.7}$$

$$i_2 = C_{GD}* \frac{dU_{C_{GD}*}}{dt} \tag{1.8.8}$$

$$i_5 = C_{DS}\frac{dU_{C_{DS}}}{dt} \tag{1.8.9}$$

$$C_{GD}* = (g_m+1)\, C_{GD} \tag{1.8.10}$$

$$i_1 = i_2+i_3 \tag{1.8.11}$$

$$i_{Load}+i_4+i_5 = i_2 \tag{1.8.12}$$

$$i_6 = i_3+i_4+i_5 \tag{1.8.13}$$

$$i_1 = i_6+i_{Load} \tag{1.8.14}$$

In the aforementioned current ringing model, the initial conditions, natural frequency, and damping ratio are determined by its gate drive output capability, PCB layout geometry between its gate drive and the MOSFET, and the MOSFET intrinsic parameters. Since load impedance is large, it will not significantly affect the superimposed ringing (only the ringing amplitude is affected by load.) When the MOSFET is used in an H-bridge or other circuit topologies, the load parameters or the

behavior of other semiconductor devices will not significantly affect this current ringing. This makes this method well suited for most power electronics circuit topologies.

In the prototype test in [46], the original load current waveform measured from Fuji Fuji 2SK3677-01MR power MOSFET is shown in Fig. 1.8.9. The experimental results after moving average for the room temperature test and the heated test with ringings from two operating points, "T_j = 24ºC, $R_{DS\text{-}on}$ = 0.69Ω" and "T_j = 103ºC, $R_{DS\text{-}on}$ = 1.14Ω", are shown in Fig. 1.8.10.

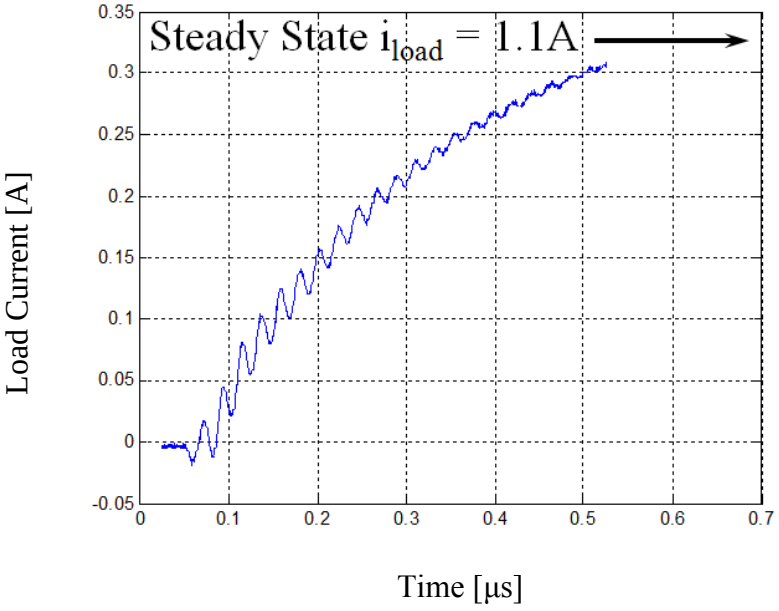
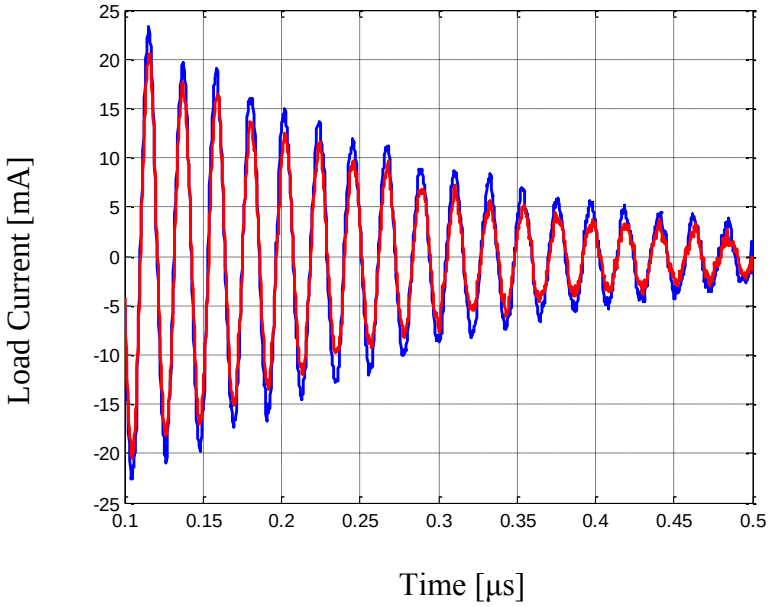


Fig. 1.8.9 load current ringing waveform (raw data)



Tj = 24°C $R_{DS\text{-}on\text{-}gal} = 0.69[\Omega]$ $\tau_1 = 0.201\mu s$
Tj = 103°C $R_{DS\text{-}on\text{-}gal} = 1.14[\Omega]$ $\tau_2 = 0.166\mu s$

Fig. 1.8.10 Experimental ringing decay at different T_j

The MOSFET junction temperature measured by a thermal camera and the junction temperature estimates made by using datasheet's "$R_{DS\text{-}on} - T_j$" characteristic (Fig. 1.8.8) and the different estimated $R_{DS\text{-}on}$ (current ringing estimated $R_{DS\text{-}on}$, V_{DS}/I_{DS} estimated $R_{DS\text{-}on}$), are shown in Fig. 1.8.11.

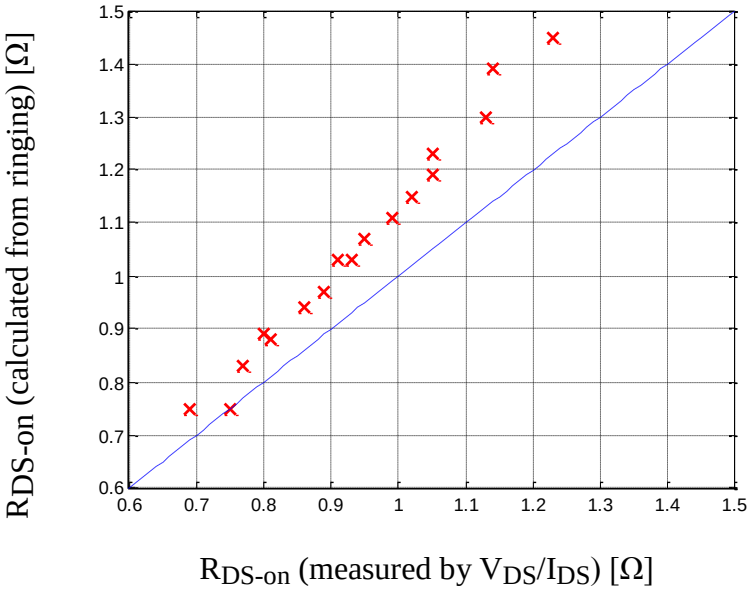
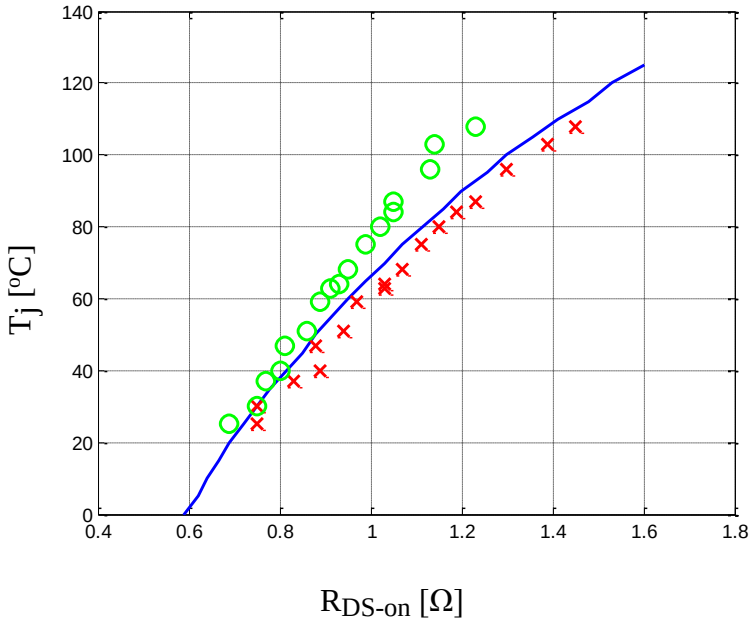


Fig. 1.8.11 Experimental data for $R_{DS\text{-}on}$ (galvanically measured by V_{DS}/I_{DS}) vs. $R_{DS\text{-}on}$ (calculated from measured current ringing)

By combining the data from Fig. 1.8.8 and Fig. 1.8.11, the characteristics for T_j-$R_{DS\text{-}on}$ can be derived as shown in Fig. 1.8.12. The relationship in blue in Fig. 1.8.12 is from the datasheet and is used to compare to the other two '$R_{DS\text{-}on}$–thermal camera' based characteristics. It can be seen from Fig. 1.8.12 that the "gate drive-$R_{DS\text{-}on}$-L-C" based "measured τ method" estimation (red crosses) has a 5°C systematic error compared to the datasheet correlation (blue line). The 'galvanically measured V_{DS}/I_{DS} method' estimation is accurate at 70°C or lower but has an error up to 15°C at high temperature. Therefore, the "gate drive-$R_{DS\text{-}on}$-L-C" based "measured τ method" estimation is proven to be more reliable. The estimation starts from room temperature and ends at 110°C. Note that the test MOSFET, Fuji 2SK3677-01MR MOSFET will stop working at 130°C.



–: $R_{DS\text{-}on}$–T_j relationship from datasheet
X: $R_{DS\text{-}on}$ (calculated from measured τ) vs. T_j from thermal camera
O: $R_{DS\text{-}on}$ (measured by V_{DS}/I_{DS}) vs. T_j from thermal camera

Fig. 1.8.12 T_j estimation using different $R_{DS\text{-}on}$ estimation methods

1.9 Summary and Discussion of Previous Work

This section will review and discuss the aforementioned T_j sensing methodologies based on their circuit invasiveness, hardware integration, signal processing, and so forth.

The performance of the observer based T_j sensing methods are very sensitive to the themal-dynamics of the device package. The device package can have several milli-seconds to 100 milli-seconds difference in thermal dynamics time constant. The sensing bandwidth of the observer based T_j sensing method will be limited by the device package time constant. For those devices with large time constants in thermal dynamics, real time

T_j tracking can be challenging. In addition, the accuracy of the thermal dynamic model is also a critical issure for this method. Consider that it is very difficult to calibrate the device package thermal model, the T_j sensing steady state error is another challenge for the observer based T_j sensing method.

The "diode-on-die technology" T_j sensing requires involves additional fabrication on the power semiconductor die. The fabrication process constraints will be applied to the power semiconductor chip because of the on-chip p-n junction T_j sensor. Considering the number of stringed diodes is not very big, the T_j sensing consistency control is challenging. Thus, the performance of sensors fabricated in the same batch cannot be guaranteed consistent. In addition, the on-chip p-n junction T_j sensor is usually fabricated on a small area on the power semiconductor chip. If a hot spot exists on the semiconductor chip, the sensor might not be able to detect it. Furthermore, the on-chip p-n junction T_j sensor needs to be connected to the off-chip circuit setup by wire bond or direct bonded copper (DBC). Since the size of the p-n junction is very small, the position and connection of wire bond or DBC is challenging. Another problem is the EMI from the swiching power semiconductor. Since the on-chip p-n junction T_j sensor share the same die with the power semiconductor, it is capacitively coupled with the switching power semiconductor. As a result, the switching noise will have a big effect on the p-n junction output.

The on-state properties based T_j sensing requires galvanic isolation for the voltage sensor. When the switching semiconductor is on, the T_j dependent voltage across

the device is usually within 1V. When the switching semiconductor is off, the big voltage stress across the device will also be applied to the voltage sensor. In such case, proper circuit design to block the off-state high voltage stress is necessary. Because the frequency of the converter load current is much slower compared with converter switching frequency, the semiconductor current can be taken as constant within several switching cycles. Thus, high bandwidth load current measurement is not required for the device on-state properties based T_j sensing, and the voltage sensing bandwidth will determine the T_j sensing bandwidth for the device on-state properties based T_j sensing.

For those T_j sensing methods that measure transient signal duration time, accurate counter- start trigger and counter-end trigger are very important. For the two methods discussed in section 1.6, at least 1GHz trigger response time is required. Such requirement can be very challenging since the propagation delay on the PCB and the response time of analog IC can delay the trigger signal for up to several nano seconds. If more than one signal needs to be measured, the signal synchronization is another problem for the counter's trigger.

For those T_j sensing methods that measure transient signal amplitude, high bandwidth analog sensing is essential. Most of the high bandwidth analog signal sensing is invasive to the circuit to be sensed. As a result, galvanic isolation is required if the sensor and the target circuit cannot share the same DC bus. If the target circuit is operated on high power rating, active isolation and high voltage protection will be necessary for the sensing implementation. On the contrary, if the target circuit is operated with only very small voltage/current rating, the voltage/current sensor might not have

enough resolution. Thus, analog signal processing such as differential amplification, peak detection, and signal integration can be used to extract the signal T_j dependency with higher resolution.

The switching transient resonation based T_j sensing requires proper resonant tank design, high bandwidth analog signal sensing, and online digital signal processing. The "design-for-sensing" concept can be introduced to the resonant tank design, so that the damped frequency, peak amplitude, and decay rate can be optimized to the best analog signal sensing resolution. The hardware implementation for the switching transient resonation based T_j sensing method can be complicated since high bandwidth signal processing and digital signal processing need to be applied to each power semiconductor.

To summarize the state-of-the-art methodologies that are feasible for switching power semiconductor online T_j sensing and evaluate them based on metrics such as hardware invasiveness, hardware integration, signal processing requirements and bandwidth capability. The conclusions of the state-of-the-art review are listed as follows.

- The hardware required for T_j sensing methods using only current measurement is less invasive to the converter power terminals than those using voltage measurement.
- The hardware required for the T_j sensing methods implemented on the switching semiconductor gate drive side have less voltage/current stress and can be integrated inside the semiconductor gate drive, whereas the hardware required for the T_j sensing methods implemented on the converter power side need higher voltage/current ratings.

- The T_j sensing methods based on device on-state properties are the simplest to implement, however the hardware required to implement those are more invasive than the hardware to implement T_j sensing methods based on device transient properties. T_j sensing methods based on device transient properties require complex signal processing techniques but can be implemented with minimal or no hardware invasiveness on the converter power side.
- The bandwidth of the T_j sensing methods based on the device on-state properties is limited by the voltage/current sensing response time and signal processing delay, whereas the bandwidth of the T_j sensing methods based on the device transient properties is determined by the switching frequency of the semiconductor.

1.10 Identification of Research Opportunities

The following research opportunities have been identified in the state-of-the-art:

- **Realize (1) real-time sensing, (2) non-invasive sensing, on switching power semiconductor T_j.**
    - In prior art, many T_j sensing methods' bandwidths are not fast enough to track the thermal dynamics of the switching power semiconductor. The time constant of power semiconductor "junction area" is usually between 1ms and 100μs. However, slow sensor response time or complex signal processing can make the T_j sensing infeasible for online T_j estimation. In this research, the T_j sensing bandwidth will be half of the power semiconductor switching frequency.

- The "diode-on-die" technology is invasive to the switching power semiconductor chip, and most of the device properties based in-direct T_j sensing is invasive to the device power terminals. As a result, invasive T_j sensing need additional considering for galvanic isolation, and EMI. In this research, all the T_j sensing hardware will be embedded in the switching power semiconductor gate drive with out invading the semiconductor chip or device power terminals.

- **Use simple implementation for switching power semiconductor T_j sensing.**
  - Some T_j sensing method reviewed in the state-of-the-art requires high speed synchronization for the measured signals. The synchronization of fast transient signal is extremely challenging, thus the hardware implementation will be complex and expensive. This research should propse a method that does not require high speed synchronization.
  - In prior art, complicated digital signal processing like FFT is required by some method. In this research, the switching power semiconductor T_j sensing should use very simple analog signal proceesing.

- **Develop methods for non-invasive T_j sensing, and investigate the system dynamic modeling for simulation, and the experimental setup for calibration.**
  - The system dynamic model, including power semiconductor swiching dynamic model, gate drive output model, and power circuit dynamic model should be developed to simulate the sensitivity of the T_j sensing method.

Finite element model for the semiconductor chip will be built to calibrate the chip vertical thermal gradient.

- Different T_j sensing methods should be included in this research to calibrate the method's accuracy and resolution.

- **Investigate each non-invasive T_j sensing method's applicability on different types of switching power semiconductor and different gate drive topologies.**
  - The performance of the methods should be verified when different types of switching power semiconductors are used, and different types of gate drive topologies are used.
  - "Design for sensing" approach is desired for gate drive topology design, gate drive parasitics control, and gate drive temperature optimization.

Chapter 2 Circuit Dynamic Loop and Measuring Point

In this research, the converter switching transient properties will be used for power semiconductor online T_j sensing. The switching transient signal in the circuit is the superposition of the switching transients from different circuit dynamic loops. The switching transient T_j dependency relies on the circuit dynamic loop and measurement point in the circuit. Considering the non-linear properties from the active/passive circuit component, switching transient generated from the same circuit dynamic loop can have different waveforms if measured in different nodes in the circuit.

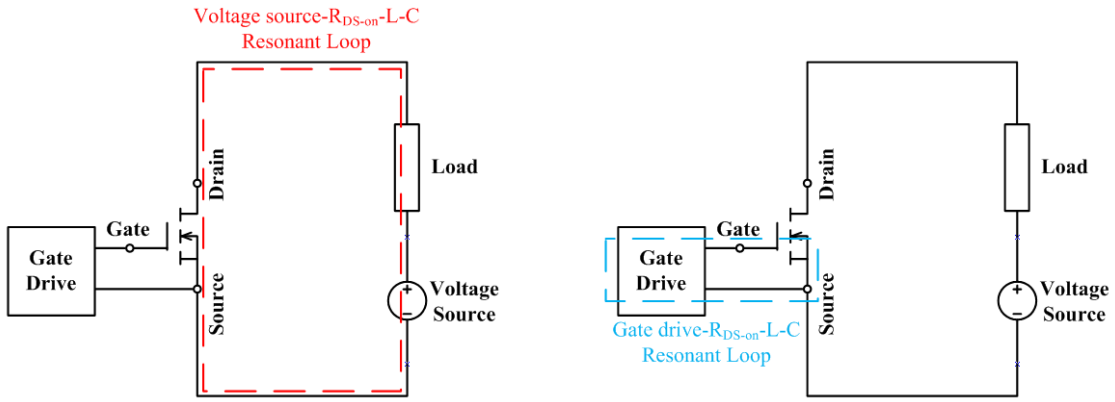
Based on the discussion in chapter 1, current sensing is preferred so as to achieve non-invasive signal extraction. The research in this thesis focuses on the current signal switching transient T_j dependency. High bandwidth current sensing and the extraction of transient current chararcteristics will be investigated in chapter 7.

In this chapter, the switching transient from different circuit dynamic loops will be studied. Current signal measuring point and T_j dependency will be compared.

2.1 Circuit Switching Transient

In a power converter system, different circuit dynamic loops can generate switching transient with different frequencies. As a result, the circuit switching waveform measured in a specific node in the circuit is the superposition of switching transients from different dynamic loops.

To investigate the switching transient superposition, a simple chopper circuit with a gate drive is studied as the first example. It can be seen in Fig. 2.1.1 that two circuit dynamic loops are coupled by the power MOSFET in the system: the slow dynamic loop "voltage source-$R_{DS\text{-}on}$-L-C", and the fast dynamic loop "gate drive-$R_{DS\text{-}on}$-L-C", "L" and "C" indicate the parasitic and intrinsic inductance/capacitance inside the circuit dynamic loop.



(a) "Voltage source-$R_{DS\text{-}on}$-L-C" slow dynamic loop

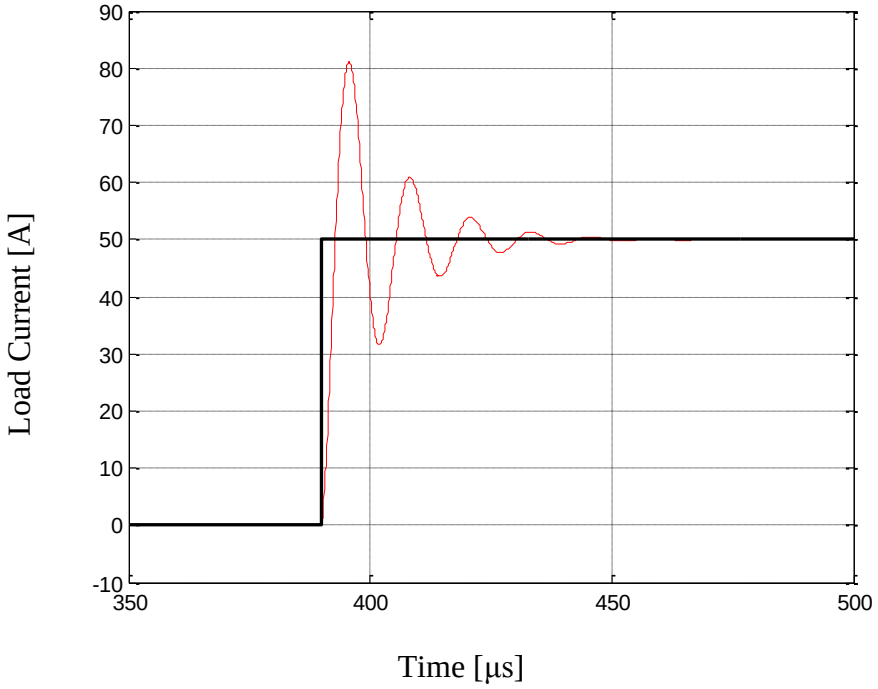
(b) "Gate drive-$R_{DS\text{-}on}$-L-C" fast dynamic loop

Fig. 2.1.1 Chopper circuit with gate drive, two coupled dynamic loops

In the "voltage source-$R_{DS\text{-}on}$-L-C" resonant loop as shonw in Fig. 2.1.1 (a), the load current ringing is the result of the sudden state change (from off state to on state) act on MOSFET intrinsic parameters and load. The resultant current ringing will be superimposed on the ringing load current during the circuit's changing state. In this case, the load current ringing is voltage source and load dependent. Since the frequency of the ringing is usually less than 1MHz (comparable with the bandwidth of some fast active power supply), a very stiff voltage source is usually desired. Meanwhile, most of the

industrial MOSFET gate driver has a bandwidth of more than 1MHz, thus the ringing generated by MOSFET gate driver can be splited from the slow dynamic loop ringing.

When the current is measured from the load side during the MOSFET turn-on transient, a current step-up should be observed as shown in the black waveform in Fig. 2.1.2. Because of the system resonantion in the slow dynamic loop "voltage source-R_{DS-on}-L-C", under-dampled ringing sometimes can be observerd in the step-up current as shown in the red waveform in Fig. 2.1.2. If the slow dynamic loop is over-damped, the "voltage source-R_{DS-on}-L-C" will not generate any ringing during the swithcing transient.

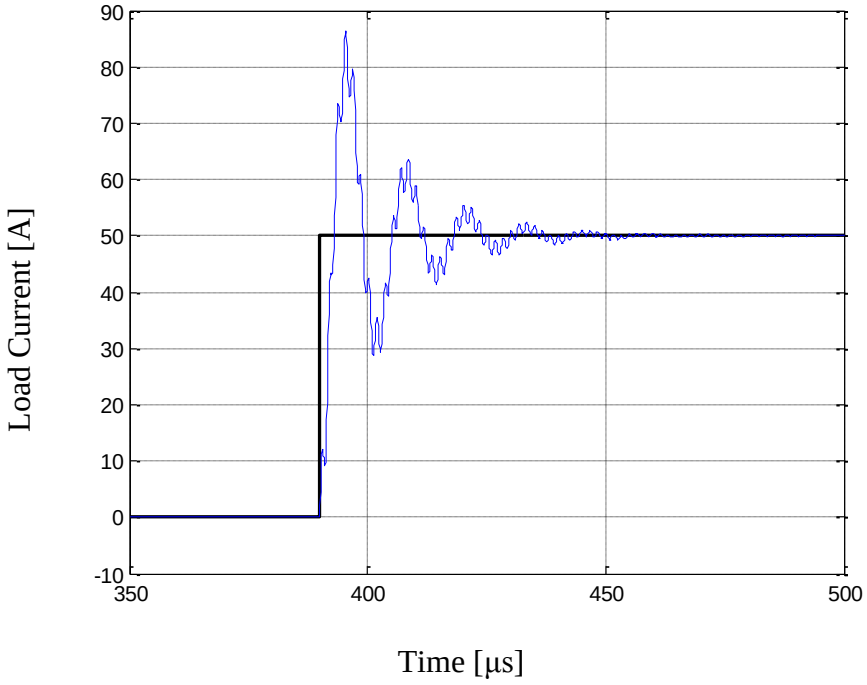


Legend: ideal waveform dynamics from "voltage source-R_{DS-on}-L-C"

Fig. 2.1.2 Simulated chopper circuit turn-on transient load current, including the "voltage source-R_{DS-on}-L-C" dynamics

In the "gate drive-R_{DS-on}-L-C" resonant loop, as shown in Fig. 2.1.1 (b), the load current ringing comes from different circuit partials. It will be shown in the following sections that the ringing superimposed on the load current waveform is mostly determined by the gate-drive output capability, MOSFET intrinsic parameters, PCB layout parasitics between gate-drive and MOSFET (usually in a small area of the PCB, and of simple shape for analysis). The frequency of this "gate drive-R_{DS-on}-L-C" ringing is faster than the 'voltage source-R_{DS-on}-L-C' ringing as well as other non-linear distortions in the circuit. The insensitivity to distortions and load properties make the "gate drive-R_{DS-on}-L-C" ringing feasible for accurate T_j sensing.

If the turn-on transient current is measured from the load side considering both the "voltage source-R_{DS-on}-L-C" resonant loop and the "gate drive-R_{DS-on}-L-C" resonant loop, current ringing superposition can be observed as shown in the blue waveform in Fig. 2.1.3. Generally, the "gate drive-R_{DS-on}-L-C" resonant ringing have a much higher ringing compared with the ringing from the "voltage source-R_{DS-on}-L-C" dynamic loop. In addition, more non-linear characteristics can be observed considering the semiconductor performance from the gate drive output and the MOSFET gate side.



Legend: ideal waveform

dynamics from "voltage source-R_{DS-on}-L-C" and "gate drive-R_{DS-on}-L-C"

Fig. 2.1.3 Simulated chopper circuit turn-on transient load current, including the "voltage source-R_{DS-on}-L-C" dynamics

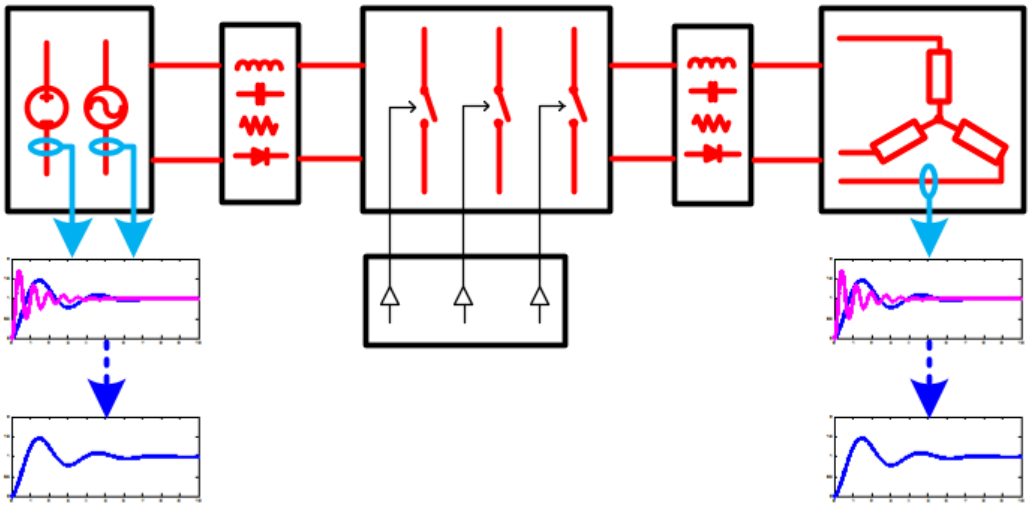
It was demonstrated that the inherent ringing in the output of the converter is dependent upon the junction temperature of the power electronic device. It will be discussed in the following sections that the time constant of ringing decay in either voltage or current is a direct function of the energy dissipation in R_{DS-on}, which is T_j dependent. The transient, high frequency model for the power MOSFET in a Boost converter configuration in [40] indicates that the behavior of the power MOSFET during a switching transient can be described as that of an under-damped LCR circuit under step excitation (aforementioned as 'voltage source-R_{DS-on}-L-C'). This result shows that the

exponential decay of the output voltage ringing is proportional to the on-state resistance of the MOSFET. If the decay envelope of the ringing signal could be easily extracted, it would be convenient to estimate the temperature of the MOSFET [38].

Analysis of the measured converter output ringing consists of filtering and system identification [39]. Since the output voltage and current ringing waveform will be distorted by non-linear characteristics of the circuit (i.e. diode reverse recovery current, gate-drive output ringing, active power supply, etc), the "voltage source-R_{DS-on}-L-C" ringing needs to be extracted by preper signal processing. Sampling the ringing signal and fitting it to a second order auto regressive moving average (ARMA) model can help in curve fitting. An observer based ringing extraction method [47] is useful when the R_{DS-on}-damped ringing frequency has a well-behaved, predictable resonant property. If the signal is complex, i.e. contains multiple harmonics, then Fourier transform analysis is required and may take a large amount time on numerical computation. Thus, complex signal processing is ill-suited for real-time temperature estimation. The following three sections investigated different circuit dynamic loops and different measuring points in order to find the simplest tranisent signal with feasible T_j dependency.

2.2 The 1st Generation T_j Sensing

The first generation online T_j sensing method invented in WEMPEC use the converter power loop as the circuit dynamic loop. The T_j dependent switching transient signal will be measured in the converter power loop as well. Fig. 2.2.1 shows a 1st generation T_j sensing implemented in a three phase inverter.



Circuit Dynamic Loop "—" : power supply, load, power switches, passive component
Intermediate Variable "—" : load/DC bus voltage (current) transient

Fig. 2.2.1 1st generation Tj sensing implemented in a three phase inverter

It can be seen in Fig. 2.2.1 that the circuit dynamic loop in Fig. 2.2.1 inlude the power supply, the passive components, the power swtiches, and the load. Depending on the properties of those components in the circuit dynamic loop, the swiching transient ringing generated by the converter power loop will have a frequency range from 10kHz to 1MHz. Since the switching power semiconductors are included in the circuit dynamic loop, some semiconductor charactersitics (for instance, junction temperature) can be sensed from the ringing generated by this circuit dynamic loop.

The current ringing generated by the converter power loop usually resonate in the lowest frequency and with very large amplitude compared other frequency components. Thus, the currnet ringing from the power loop is easily measured and filtered. An original load current waveform and a filtered (observer corrected) load currnet waveform is shown in Fig. 2.2.2 [47]

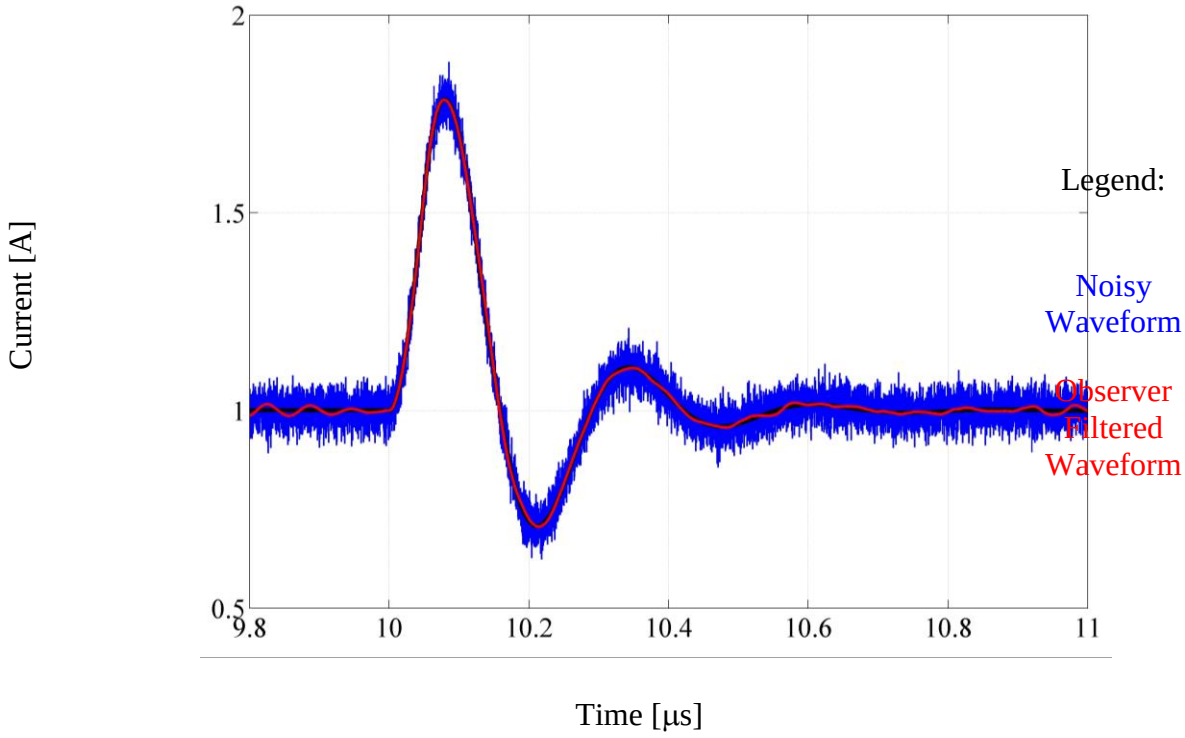
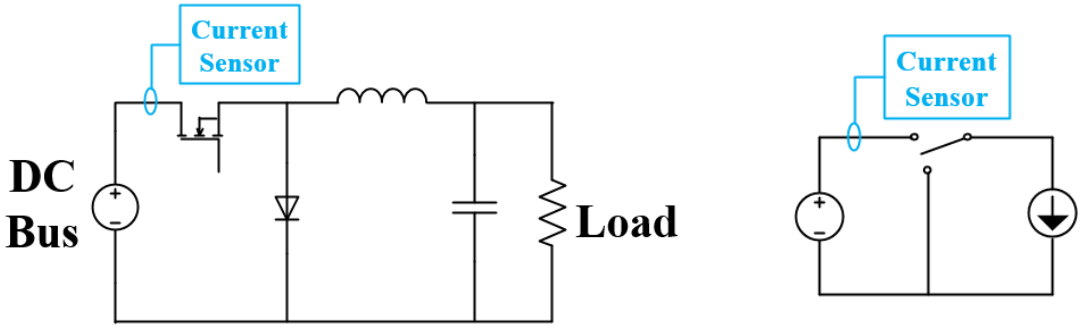


Fig. 2.2.2 Load current switching transient waveform

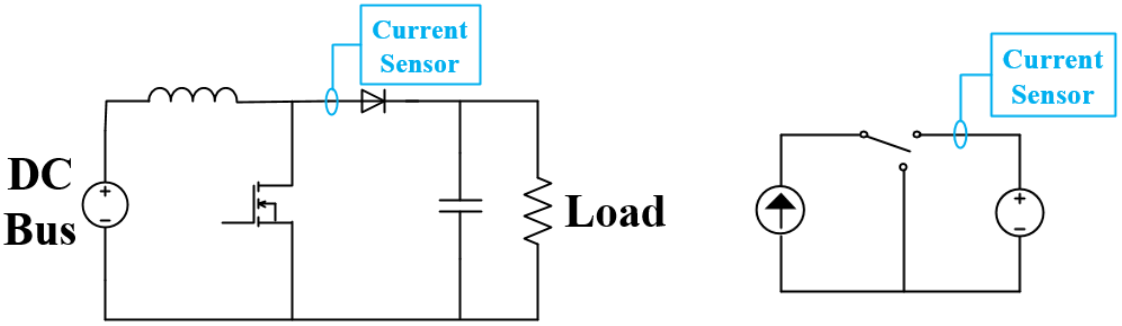
Depending on the converter topology, power loop ringing can be either measured from the converter DC bus side or the converter load side. Taking the dual DC-DC topologies, buck converter and boost converter, as an example. Either of the two dual single ending converters can be modelled as a single-pole-double-throw switch (SPDT) with one side connected to a current stiff loop and the other side connected to a voltage stiff loop. By using current stiff components like the choke inductor, the current in the current stiff side will be limited to very slow dynamics. Similarly, the voltage stiff side uses the filtering capacitor to limit the voltage dynamics. The measurement of the current ringing can be achieved on the voltage stiff side, and the voltage ringing can be measured from the current stiff side.



Buck converter circuit model Buck converter simplified topology

Fig. 2.2.3 Sensing switching transient current ringing in Buck converter. Current sensor is applied to the DC bus side.

The switching transient current ringing measurement for a Buck converter is illustrated in Fig 2.2.3. In a Buck converter, the DC bus side can be modelled as voltage stiff whereas the load side is current stiff. Thus, the current sensor should be applied to the DC bus output trace as shown in the circuit schematic.



Boost converter circuit model Boost converter simplified topology

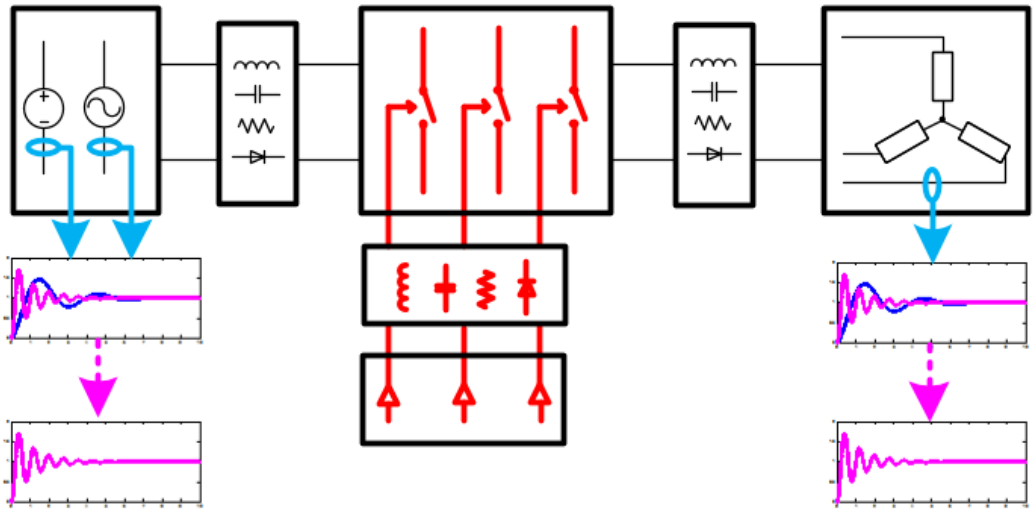
Fig. 2.2.4 Sensing switching transient current ringing in Boost converter. Current sensor is applied to the Load side.

The switching transient current ringing measurement for a Boost converter is illustrated in Fig 2.2.4. On contrary to the Buck converter, in a Boost converter, the DC

bus side can be modelled as current stiff whereas the load side is voltage stiff. Thus, the current sensor should be applied to the load input tracc as shown in the circuit schematic.

The advantage of the 1st generation T_j sensing method is the simplicity on transient current ringing measurement. Since the transient current ringing has low frequency and large amplitude, high resolution and high bandwidth are not required for the transient ringing current sensing. However, because the converter load is in the circuit power loop, this T_j sensing method will be load sensitive. Thus, load measurement will be required so as to calibrate the transient current ringing load dependency online.

2.3 The 2nd Generation T_j Sensing



Circuit Dynamic Loop "—" : gate drive, power switches, passive component
Intermediate Variable "—" : load/DC bus voltage (current) transient

Fig. 2.3.1 2nd generation T_j sensing implemented in a three phase inverter

The second generation online T_j sensing method invented in WEMPEC uses the swiching power semiconductor gate drive loop as the circuit dynamic loop. The T_j

dependent switching transient signal will be measured in the converter power loop. Fig. 2.3.1 shows a 2nd generation T_j sensing implemented in a three phase inverter.

It can be seen in Fig. 2.3.1 that the circuit dynamic loop in Fig. 2.3.1 inludes the gate drive, the passive components, and the power swtiches. Different from the 1st generation T_j sensing method, load and power supply are not included in the circuit dynamic loop in the 2nd generation T_j sensing method. Depending on the properties of those components in the circuit dynamic loop, the swiching transient ringing generated by the converter power loop will have a frequency range from 1MHz to 100MHz. Although the circuit dynamic loop in the 1st generation T_j sensing and the 2nd generation T_j sensing are different, they both include the switching power semiconductor in circuit dynamic loop. Thus, by measuring the switching transient current ringing generated by the different circuit dynamic loops, different device switching transient T_j dependency can be observed.

The current ringing generated by the switching power semiconductor gate drive loop usually resonate in the highest frequency and with a relatively small amplitude compared other switching transients. As a result, if the current ringing from the gate drive loop is measured in the power loop (either from the DC bus or from the load), the high frequency ringing signal has to be extracted using additional signal processing method. Fig. 2.3.2 shows a switching transient waveform with high frequency current ringing from the gate drive loop superimposed on the the low frequency switching dynamics. If a moving average method is applied to the superimposed waveform in Fig. 2.3.2, the high frequency ringing can be extracted as shown in Fig. 2.3.3.

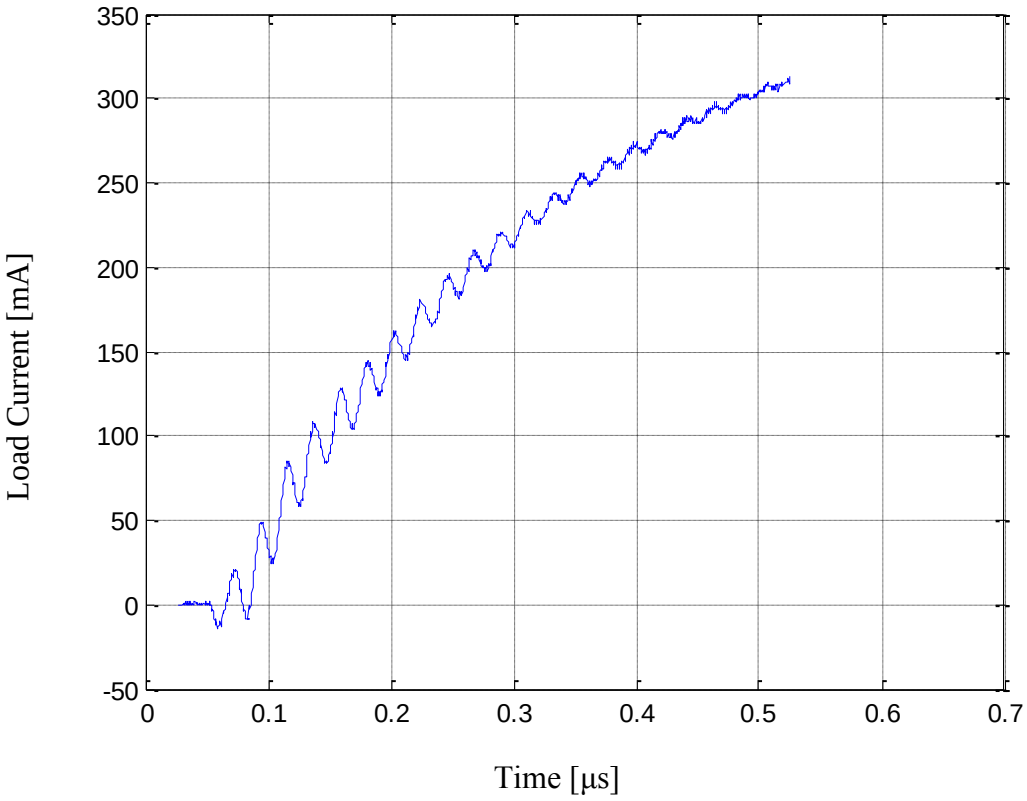


Fig. 2.3.2 Load current ringing with switching transient of different frequencies superimposed together

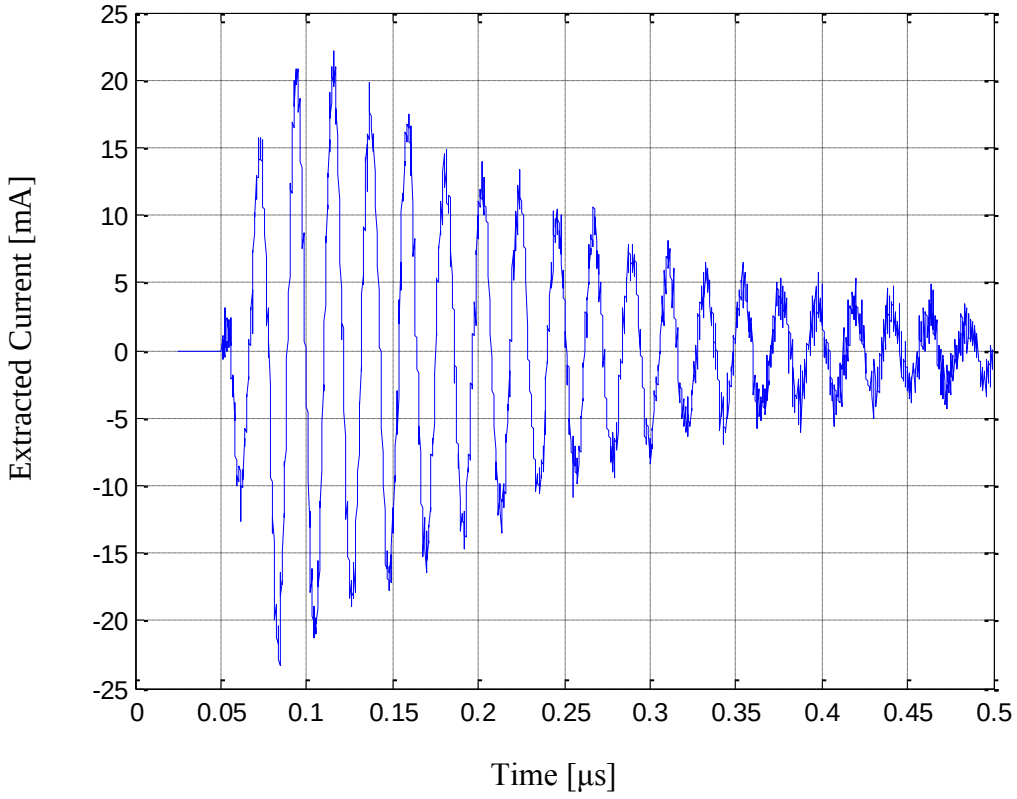


Fig. 2.3.3 Gate drive loop switching transient current ringing extracted from the converter load current

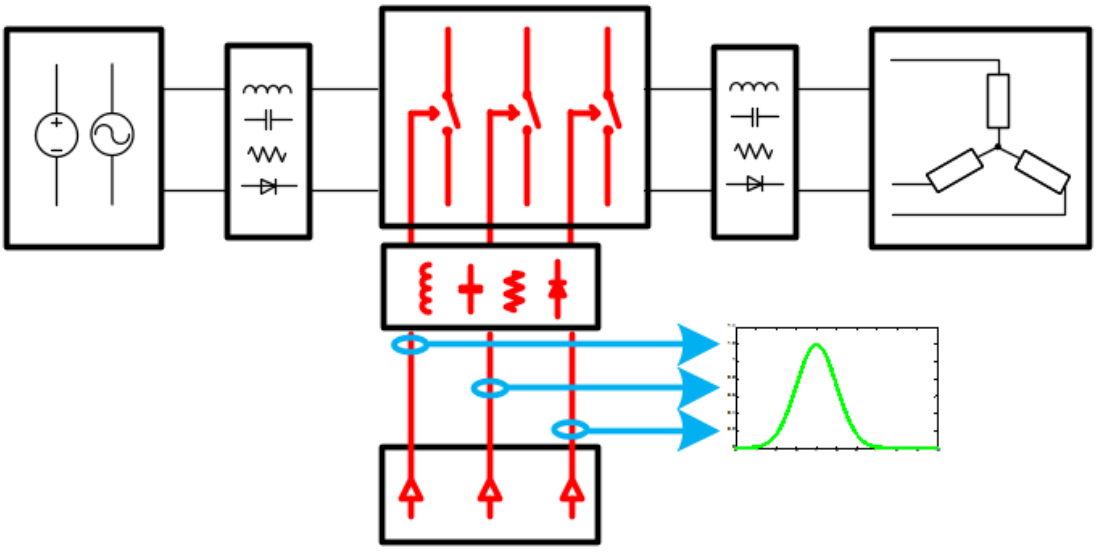
The advantage of using the 2nd generation T_j sensing method is its load dependency. If T_j is correlated to the decay rate of the waveform shown in Fig. 2.3.3 [48], the change of load will not have a significant effect on the ringing decay rate. In addition, since most of the other circuit dynamics is slower than the gate drive loop ringing signal, a quick time domain moving average can filter out most of the switching transient of other frequencies.

The limits of the 2nd generation T_j sensing comes from the high bandwidth current sensing and the realtime moving average method. Current sensing over 1MHz frequency requires recise parasitics control and very stiff power supply system for the high

bandwidth current sensor. High speed digital signal processor will be required to handle the online signal processing like moving average.

2.4 The 3rd Generation T_j Sensing

The third generation online T_j sensing method invented in WEMPEC uses the gate drive loop as the circuit dynamic loop. The T_j dependent switching transient signal will be measured in the gate drive loop as well. Fig. 2.4.1 shows the 3rd generation T_j sensing implemented in a three phase inverter.



Circuit Dynamic Loop "—" : gate drive, power switches, passive component
Intermediate Variable "—" : gate drive output current transient

Fig. 2.4.1 3rd generation T_j sensing implemented in a three phase inverter

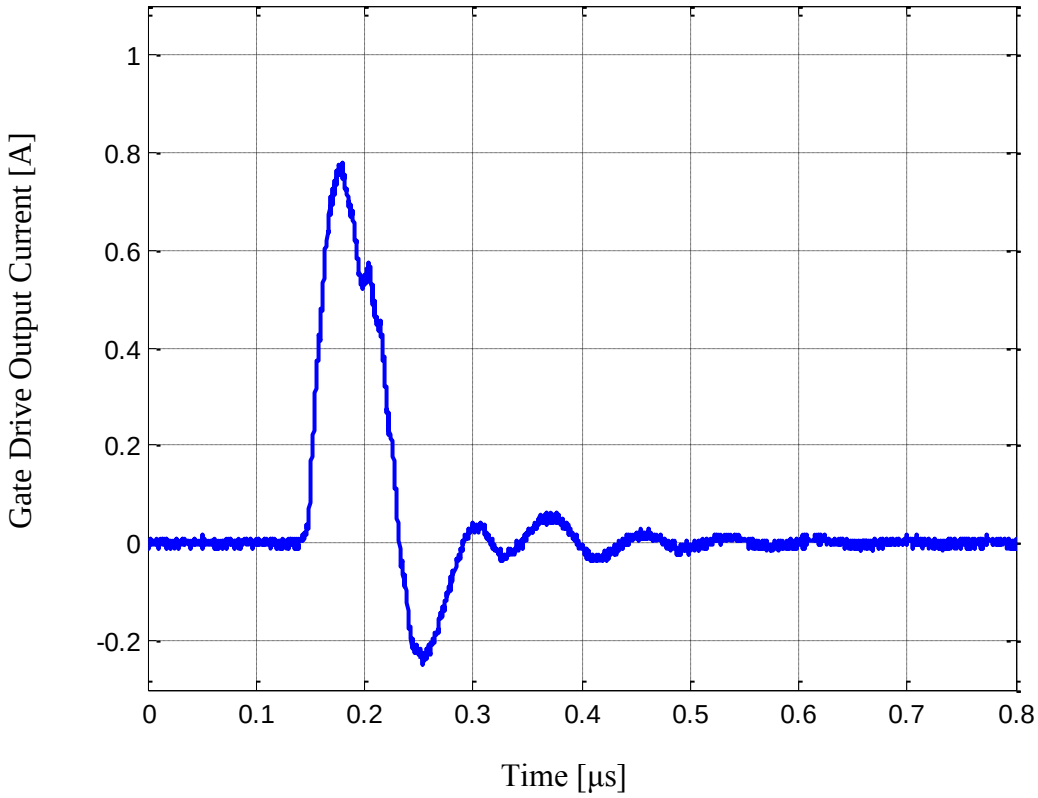


Fig. 2.4.2 Silicon MOSFET gate drive turn-on output transient current pulse

It can be seen in Fig. 2.4.1 that the circuit dynamic loop in 3rd generation T_j sensing inludes the gate drive, the passive components, and the power swtiches. If the gate drive output current switching transient is correlated to the switching power semiconductor T_j, a turn-on current pulse is found T_j sensitive (different from the case of the 1st generation T_j sensing and the 2nd generation T_j sensing, where ringing signal can be found.). Relying on the properties of those components in the circuit dynamic loop, the swiching current transient generated by the converter power loop will have a duration time of 20ns to 2000ns. Fig. 2.4.2 and Fig. 2.4.3 show the gate drive turn-on output currnet transient for a silicon MOSFET and a silicon IGBT respectively. Since the switching power semiconductors are included in the circuit dynamic loop, some

semiconductor charactersitics (for instance, junction temperature) can be sensed from the transient current pulse characteristics.

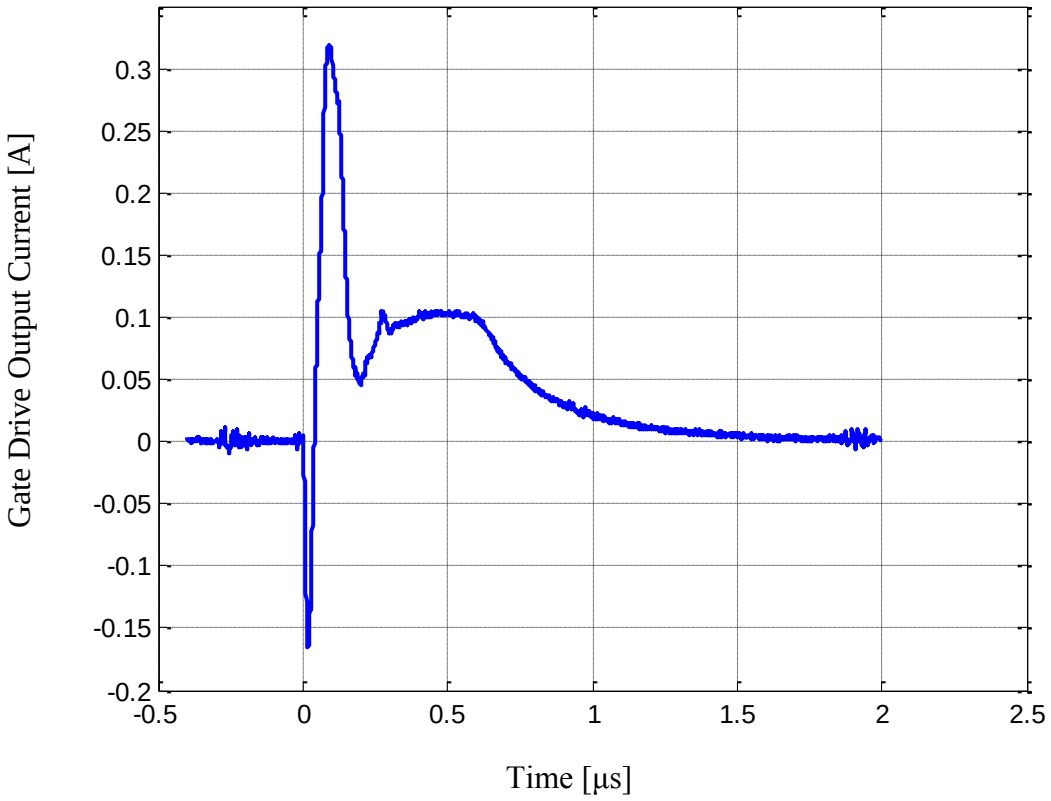


Fig. 2.4.3 Silicon IGBT gate drive turn-on output transient current pulse

The 3rd generation T_j sensing can be completely implemented in the converter gate drive loop as shown in Fig. 2.4.1. Generally, the switching power semiconductor will be included in both converter power loop and gate drive loop. However, the gate terminal of the switching power semiconductor is usually not considered as part of the power loop terminals. As a result, if the gate drive output current sensing is achieved on the switching power semiconductor gate terminal (not the source/emitter terminals), it is considered as sensing out of the power loop, namely, non-invasive to the converter power side.

Because the gate drive turn-on output current transient will have a duration time of 20ns to 2000ns, and the transient's relative T_j dependent change is with in 20%, high bandwidth, high resolution current sensing is necessary. In addition, because of the parasitics control, the gate drives should be implemented close to the switching power semiconductors. Thus, EMI effect from the converter power switching should be considered for the gate drive output current sensing.

2.5 Summary of Choosing Circuit Dynamic Loop and Measuring Point for T_j Sensing

In this chapter, three generations of switching power semiconductor T_j sensing methods based on different circuit dynamic loops and different measuring points are discussed. The basic T_j sensing methodology of the three generations is to observe the switching transient properties of a power semiconductor in a circuit dynamic loop. Usually the switching power semiconductor will resonate with more than one circuit dynamic loop in the converter system, thus the multiple frequency component of switching transients can be observed. The converter power loop and the semiconductor gate drive loop are the two commonly used circuit dynamic loops for T_j sensing. Based on the intrinsic properties of the aforementioned circuit dynamic loop, mostly, the converter power loops have slow dynamics while the gate drive loops have fast dynamics. The converter load and the converter DC bus are included in the power loop, thus the switching transient dyanamics from the power loop are usually more sensitive to the converter load variation.

To conclude, the converter power loop switching transient will be sensitive to converter load while the semiconductor gate drive loop switching transient requires high bandwidth current sensing.

This thesis studies the 3rd generation T_j sensing method. The switching transient from the semiconductor gate drive will be used for online T_j sensing, and the measuring point is on the gate terminal of the switching power semiconductor such that the sensing implementation will not be invasive to the converter power side.

Chapter 3 System Dynamic Model and Simplification

In this chapter, the 3rd generation T_j sensing implemented in an H-bridge inverter will be systematically modeled. The switching transient from the semiconductor gate drive will be used for online T_j sensing, and the measuring point is on the gate terminal of the switching power semiconductor such that the sensing implementation will not be invasive to the converter power side.

The system dynamic modeling includes the modeling for switching power semiconductors, the modeling for the gate drive output stage, and the H-bridge inverter power side. Different modeling methods will be discussed and the parameters of the model are based on the device manufacturer's datasheet and the intrinsic characteristics of the prototype.

The differences of semiconductor materials (Si and SiC) are not considered in this chapter.

3.1 Switching Power Semiconductor Dynamic Model

The switching power semiconductor can be modeled by either equivalent circuit model or Simulation Program with Integrated Circuit Emphasis (SPICE). Basically, the two types of models are both based on linear/nonlinear circuit modeling. The equivalent circuit model mostly relies on the semiconductor performance parameters, while the SPICE model focuses moreso on the semiconductor fabrication parameters.

In this section, the equivalent circuit model for the MOSFET and IGBT used in this research will be discussed respectively. A general introduction for the semiconductor SPICE model will be also be included.

3.1.1 MOSFET Equivalent Circuit Model

The semiconductor turn-on transient properties are essential for the proposed T_j online T_j sensing method. Thus, in this research, the device switching transient properties are characterized with the most effort.

The simplest way to model the MOSFET transient properties of the three terminals (gate, drain, and source) are to characterize the intrinsic capacitance between the three terminals. Generally, the MOSFET input intrinsic capacitance is defined as following:

C_{gs}: input intrinsic capacitance between gate and source

C_{gd}: input intrinsic capacitance between gate and drain

C_{ds}: input intrinisc capacitance between drain and source

However, the three aforementioned input intrinsic capacitances are not always feasibly measurable because of the limitation of MOSFET operating point and measuring implementation. Instead, MOSFET manufacturers prefer to quote C_{iss} (input capacitance, drain and source terminal shorted), C_{oss} (output capacitance, gate and source shorted), and C_{rss} (reverse transfer capacitance, source connected to ground). The relationship between these capacitances and MOSFET input intrinsic capacitance are described as the following.

$$C_{rss} = C_{gd} \tag{3.1.1}$$

$$C_{oss} = C_{ds} + C_{gd} \tag{3.1.2}$$

$$C_{iss} = \begin{cases} (a)\ C_{gs} + C_{gd} & V_{gs}–V_T < 0,\ I_d = 0 \quad \text{(Cutoff Region)} \quad (3.1.3) \\ (b)\ C_{gs} + (1+A_v)C_{gd} & 0 < V_{gs}–V_T < V_{DS} \quad \text{(Saturated Region)} \quad (3.1.4) \\ (c)\ C_{gs} + C_{gd} & V_{gs}–V_T > V_{DS} \quad \text{(Linear Region)} \quad (3.1.5) \end{cases}$$

The gate-to-drain capacitance, C_{gd}, is a nonlinear function of voltage and is always calibrated based on the switching performance of the semiconductor. This is because C_{gd} provides a feedback loop between the output and the input of the circuit. Most of the transient properties from the gate side will be amplified from this feedback loop and inject into the converter power side.

C_{gd} is also called the Miller capacitance because it causes the total dynamic input capacitance to become greater than the sum of the static capacitances. This is the reason for separate analysis of C_{iss}. Note that the value A_v is the Miller effect amplification coefficient for C_{gd}. The Miller effect accounts for the increase in the equivalent input capacitance of an inverting voltage amplifier due to dynamic amplifying effect on the capacitance between the input and output terminals. The virtually increased input capacitance due to the Miller effect is given by:

$$C_M = C(1+A_v) \tag{3.1.6}$$

(3.1.6) is used in the second term of MOSFET C_{iss} in saturated region characterization in (3.1.4). Note that for a power MOSFET model, A_v is a value subject to MOSFET turn-on operation. It is generally concerned that transconductance g_{fs} can be

regarded as a good approximation for A_v at particular operating point in the MOSFET linear region. MOSFET manufacturers usually provide a transconductance curve measured under different I_d, and this curve is only subjected to steady state measurement.

A simple MOSFET model with steady state parasitic capacitance and the Miller amplifying effect is shown in Fig. 3.1.1. Note that the $R_{DS\text{-}on}$ and other junction properties are modeled as a current source I_d.

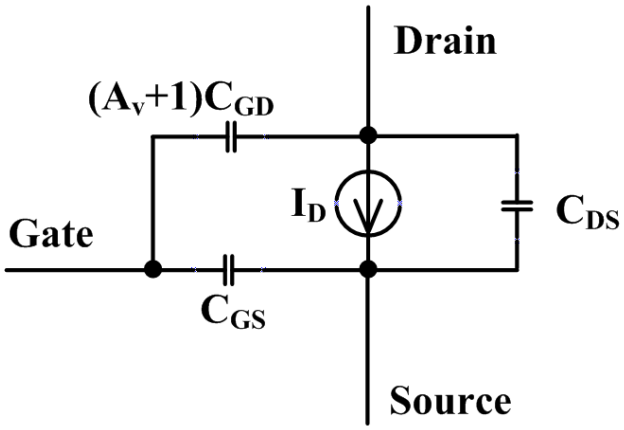


Fig. 3.1.1 MOSFET model with the steady state input intrinsic capacitance and the Miller effect

The input intrinsic capacitance for Fuji 2SK3677-01MR MOSFET is shown in Table. 3.1.1. The value of C_{GD}, C_{GS} and C_{DS} can be calculated based on (3.1.1) to (3.1.5). According to the MOSFET datasheet, input intrinsic capacitance are measured on V_{DS} = 25V, V_{GS} = 0V and f = 1MHz. However, C_{iss} is V_{GS} sensitive. Indeed, C_{iss} is modeled as the input charge for MOSFET. Based on the definition of MOSFET gate charge Q_g, MOSFET input charge property is already included in Q_g. Obviously, the

double modeling for MOSFET (Q_g and C_{iss}) is not redundant. Thus, a smaller C_{iss} value is usually used instead of the typical value from datatsheet.

Table 3.1.1 FUJI 2SK3677-01MR intrinsic capacitance

Parameter	Symbol	Typical Value	Max Value
Input apacitance	C_{iss}	1100 pF	1650 pF
Output Capacitance	C_{oss}	170 pF	255 pF
Reverse Transfer Cap.	C_{rss}	11 pF	17 pF

To further characterize the turn-on transient of power MOSFET, non-linear switching properties and device parasitics should be considered. Ignore the device turn-off properties and the breakdown properties, the following assumptions can be made.

(1) MOSFET will be turned-on only ONCE;

(2) MOSFET is guaranteed to be turned-on with provided V_G;

(3) V_{DS} does not exceed MOSFET breakdown limitation.

Hence, the following MOSFET characteristic need to be modeled into equivalent circuit.

(1) OFF-state and ON-state MOSFET junction resistance;

(2) MOSFET intrinsic capacitance (parasitic capacitance);

(3) MOSFET turn-on Miller effect;

(4) parasitics in bonding wire and leads.

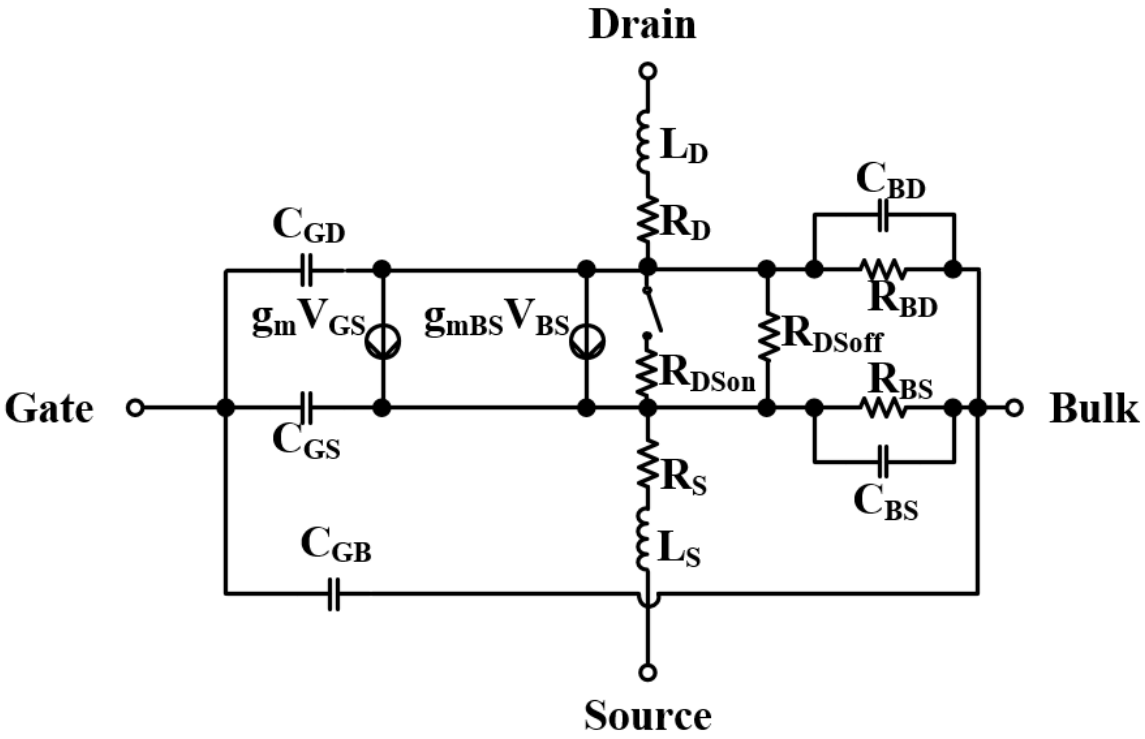


Fig. 3.1.2 Further characterized MOSFET dynamic model with device parasitics and non-linear turn-on properties

Based on the turn-on mechanism of power MOSFET [43], the dynamic modeling for Fuji 2SK3677-01MR power MOSFET is illustrated in Fig. 3.1.2. The on-state and off-state junction resistance ($R_{DS\text{-}on}$ and $R_{DS\text{-}off}$) can be derived from MOSFET datasheet. A large value for $R_{DS\text{-}off}$ should be used in case that the information for $R_{DS\text{-}off}$ is not characterized in datasheet. Note that some MOSFET requires a dynamic modeling of $R_{DS\text{-}on}$ during the MOSFET turn-on transient. A typical value of 0.72Ω is found from datasheet for Fuji 2SK3677-01MR power MOSFET, while the actual estimate value for $R_{DS\text{-}on}$ can vary from 0.69Ω to 1.30Ω.

The modeling of MOSFET turn-on Miller effect with its non-linear properties are characterized in the further characterized MOSFET dynamic model. Two controlled current sources are used to simulate the amplifying effect from V_{GS} and V_{BS}. For simplicity, the g_m and g_{mBS} are defined as follows:

$$g_m = \left.\frac{dI_{DS}}{dV_{GS}}\right|_{op} = \begin{cases} (a)\ 0 & \text{for } (V_{GS} - V_{TH}) < 0 \\ (b)\ \beta(V_{GS} - V_{TH})(1 + \lambda V_{DS}) & \text{for } (V_{GS} - V_{TH}) < V_{DS} \\ (c)\ \beta V_{DS}(V_{GS} - V_{TH}) & \text{for } (V_{GS} - V_{TH}) > V_{DS} \end{cases} \quad (3.1.7)$$

$$g_{mBS} = \left.\frac{dI_{DS}}{dV_{BS}}\right|_{op} = \begin{cases} (a)\ 0 & \text{for } (V_{GS} - V_{TH}) < 0 \\ (b)\ g_m \times ARG & \text{for } (V_{GS} - V_{TH}) < V_{DS} \\ (c)\ g_m \times ARG & \text{for } (V_{GS} - V_{TH}) > V_{DS} \end{cases} \quad (3.1.8)$$

The definition for β, ARG and more detailed discussions can be found in [49] chapter 4. Note that the the T_j dependency of $R_{DS\text{-}on}$ and V_{TH} are usually provided by the semiconductor manufacturer. By selecting the V_{TH} based on T_j, g_m and g_{mBS} under different T_j can be calculated. With $R_{DS\text{-}on}$, g_m, and g_{mBS} calculated based on T_j, the MOSFET model shown in Fig. 3.1.2 can be used for T_j dependent simulation.

Modeling for the parasitics from wire bonds and leads are based on the device physical geometry and material of these parts. Different MOSFET with the same packaging, wire bonds parasitics and leads parasitics should be identical. Thus, it is only necessary to model the parasitics from the existing device package and apply the parameters to all other devices with the same package.

3.1.2 IGBT Equivalent Circuit Model

IGBT is usually considered as a compound device although a real device is fabricated as one. A simplified N-channel IGBT model is shown in Fig. 3.1.3, with an N-channel power MOSFET driving a wide base PNP bipolar transistor in a Darlington configuration.

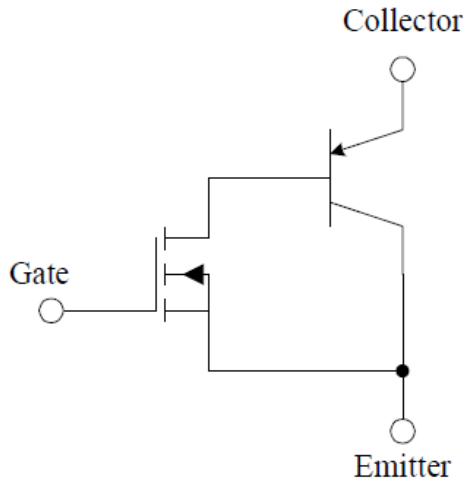


Fig. 3.1.3 IGBT modeled as a compound device

Fig. 3.1.3 charactertizes the conduction properties of IGBT. When IGBT is operated at on-state, there is always at least an one-diode voltage drop between the collector and the emitter, no matter how much is the on-state current. As a result, the IGBT on-state properties cannot be modeled as an on-state resistance (which is different from the modeling of MOSFET).

However, compared to a power MOSFET of the same die size and operating at the same temperature and current, an IGBT can have significantly lower on-state voltage. The reason for this is that a MOSFET is a majority carrier device only. In other words, in an N-channel MOSFET, only electrons flow. On the contrary, the p-type substrate in an

N-channel IGBT injects holes into the drift region. Therefore, current flow in an IGBT is composed of both electrons and holes. This injection of holes (minority carriers) significantly reduces the effective resistance to current flow in the drift region. Stated otherwise, hole injection significantly increases the conductivity, or the conductivity is modulated. The resulting reduction in on-state voltage is the main advantage of IGBTs over power MOSFETs.

A more detailed IGBT model resembles a thyristor as shown in Fig 3.1.4. In this case, the PNPN doping layer is characterized in the model.

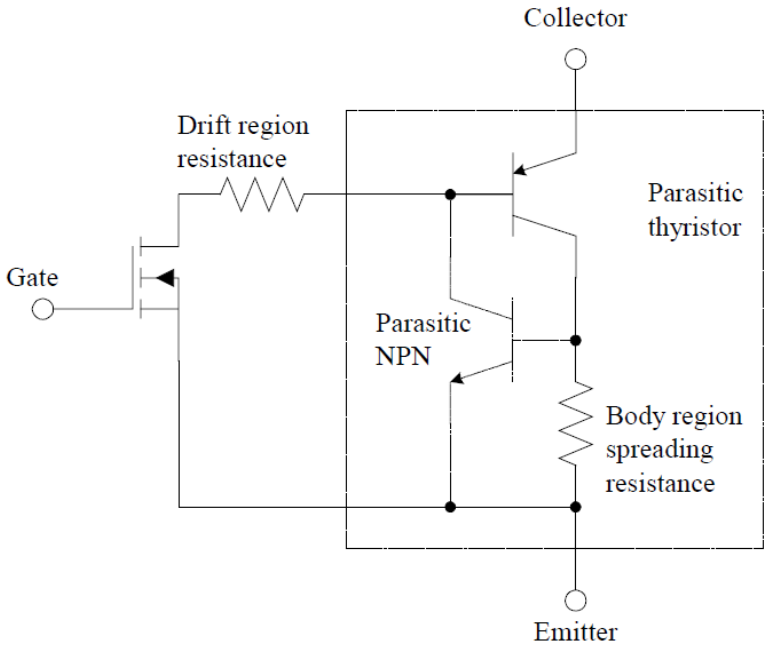


Fig. 3.1.4 IGBT modeled with resembled thyristor

A parasitic NPN bipolar transistor exists in all N-channel power MOSFETs and consequently all N-channel IGBTs. This NPN bipolar transistor is used to characterize the body region, which is shorted to the emitter to prevent it from turning on. Indeed, the body region also has some resistance, commonly regarded as the body region spreading

resistance, as shown in Figure 3.1.4. The P-type substrate and drift and body regions form the PNP portion of the IGBT. The device PNPN structure forms a parasitic thyristor. If the parasitic NPN transistor ever turns on and the sum of the gains of the NPN and PNP transistors are greater than one, latch-up occurs.

To further characterize the turn-on transient of the IGBT, the two bipolar transistor in Fig. 3.1.4 are replaced by controlled current source and capacitance. The gate MOSFET should be characterized with input intrinsic capacitance and the transiconductance amplifying effect. The equivalent circuit model is shwon in Fig. 3.1.5. The controlled current source in the equivalent circuit model is define in (3.1.7) to (3.1.9) [51].

$$I_{css} = \left(\frac{1}{1+b}\right) I_T + \left(\frac{b}{1+b}\right) \frac{4D_p}{W^2} Q \tag{3.1.7}$$

$$I_{bss} = \frac{Q}{\tau_{HL}} + \frac{Q^2}{Q_B^2} \frac{4N_{scl}^2}{n_i^2} I_{sne} \tag{3.1.8}$$

$$I_{mult} = (M - 1)\,(I_{mos} + I_c) + M\, I_{gen} \tag{3.1.9}$$

$$I_{mos} = \begin{cases} 0 & \text{for } (V_{GS} - V_{TH}) < 0 \\ K_p\,(V_{GS} - V_{TH})\,V_{DS} - K_p \dfrac{V_{DS}^2}{2} & \text{for } (V_{GS} - V_{TH}) > V_{DS} \\ K_p\,(V_{GS} - V_{TH})^2 / 2 & \text{for } (V_{GS} - V_{TH}) < V_{DS} \end{cases} \tag{3.1.10}$$

In (3.1.7) to (3.1.10), the Tj dependency of V_{TH} and K_p are usually provided by the semiconductor manufacturer. b, D_p, Q, Q_B, W, I_T, M, N_{scl}, n_i are the device intrinsic parameters. Av can be modeled with g_m, g_{mBS} as discussed in section 3.1.1. With V_{TH}

and K_p derived based on T_j, the IGBT model shown in Fig. 3.1.3 can be used for T_j dependent simulation.

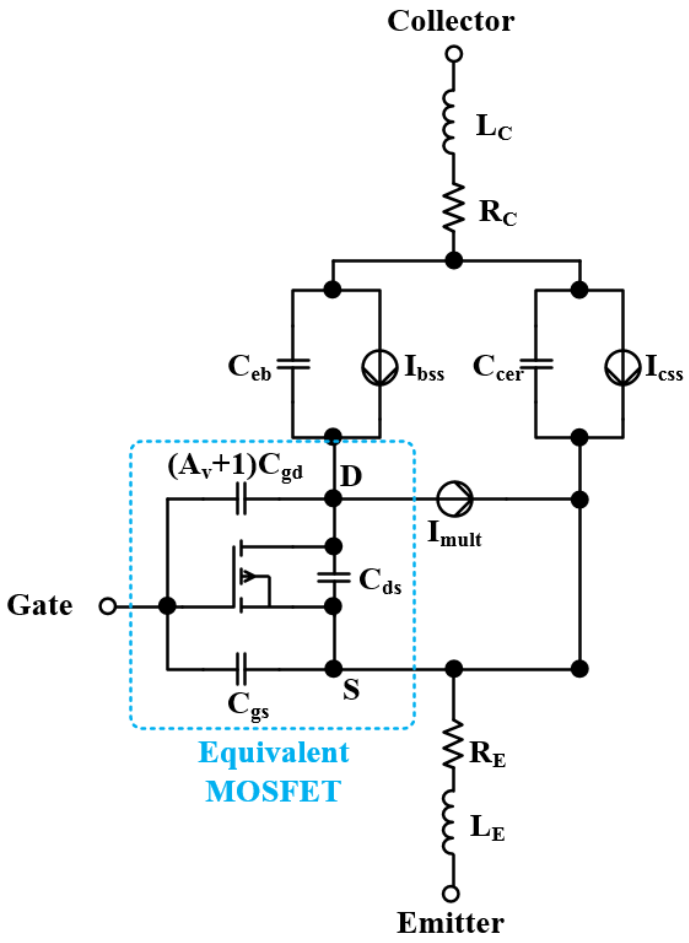


Fig. 3.1.5 IGBT modeled with controlled current source and intrinsic capacitance

The IGBT equivalent circuit model is based upon the IGBT structure without considering the effects of ambipolar transport. The emitter-base diffusion capacitance is represented as a lumped capacitor located at the metallurgical emitter-base junction, and only the flow of the base current through the conductivity modulated base resistance is indicated. However, the voltage drops due to drift and diffusion are actually distributed throughout the base region, and the drift terms of the ambipolar transport equations

depend upon both the base and collector currents. Thus, both the base and collector components of current contribute to the resistive potential drop.

3.1.3 HEMT Equivalent Circuit Model

Wide-bandgap devices such as AlGaN–GaN HEMTs have emerged as a promising solution for the next-generation commercial wireless base-station amplifiers and high-power high-temperature applications due to the relatively low intrinsic carrier generation and high breakdown fields.

As the AlGaN–GaN material system is still in the development stage, different circuit models have been proposed, but many of them still need further evaluation.

A GaN HEMT temperature dependent model is developed in [52] as shown in Fig. 3.1.6, where the temperature-dependent equivalent components are marked in red. A voltage-dependent current source I_{DS} is used to characterize the device's forward and reverse conduction properties of the GaN HEMT. Two voltage-dependent intrinsic capacitances, C_{GD} and C_{DS}, as well as a voltage-independent intrinsic capacitance, C_{GS}, are used to model the device's switching transient properties. Three constant resistors, R_G, R_D, and R_S, are used to represent the device's intrinsic parasitics. Simulation and experimental results used in [52] indicate that load dependency, gate voltage dependency, and T_j dependency are properly characterized in the proposed GaN HEMT model.

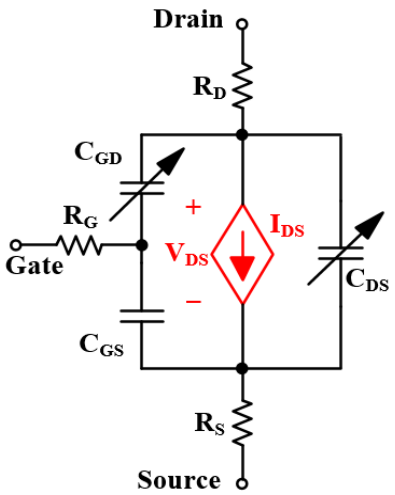


Fig. 3.1.5 GaN T_j dependent model with voltage controlled current source

The simulation model for some GaN HEMT products from EPC Co. are not fully temperature characterized. In the LTSpice sub-circuit model for EPC2030 [53], V_{TH} is set to a constant value of 2.2V, and R_G is set to a constant value of 0.6Ω. Based on the LTSpice simulation model, an equivalent circuit model is created as shown in Fig. 3.1.6, where the equivalent temperature dependent components are marked in red. In the HEMT model in Fig. 3.1.6, two temperature-sensitive diodes, D_{GD} and D_{GS}, are added to characterize the gate-source over-voltage properties.

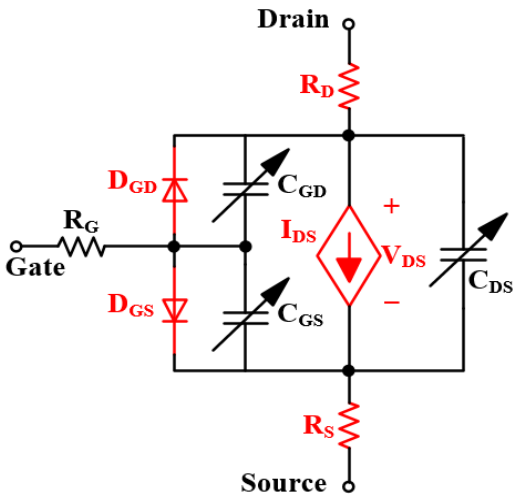


Fig. 3.1.6 GaN T_j dependent model with over-voltage properties

To introduce the temperature dependency of V_{TH} [52] and R_G [53] to the LTSpice simulation model, V_{TH} and R_G are re-characterized in (2.1) and (2.2). Based on the "V_{TH} - T_j" dependency and the "semiconductor resistance – T_j" dependency of EPC2030 GaN HEMT [54], the device switching transient can be fully characterized with K_{T1} = 6.7 x 10-3K-1, V_{TH0} = 1, K_{T2} = 3.7 x 10-3Ω/K, R_{G0} = 0.4Ω.

$$\text{Normalized } V_{TH} = K_{T1} (T_j - 300K) + V_{TH0} \tag{3.1.10}$$

$$R_G = K_{T2} (T_j - 300K) + R_{G0} \tag{3.1.11}$$

The intrinsic capacitance of GaN HEMTs consist of the parasitic capacitance and the junction capacitance. The parasitic capacitance of GaN HEMTs are well understood as bias dependent [55]. The junction capacitance from the metal-semiconductor contact is sensitive to both bias voltage and junction temperature [56] [57]. In this research, the modeling of C_{GS} and C_{GD} include both the parasitic capacitance and the junction

capacitance. The temperature dependency of the device intrinsic capacitance is characterized by (2.3) and (2.4).

$$C_{GS} = K_{T3} (T_j - 300K) + C_{GS0} \quad (3.1.12)$$

$$C_{GD} = K_{T4} (T_j - 300K) + C_{GD0} \quad (3.1.13)$$

The LTSpice model in [54] covers (2.1), but (2.2), (2.3), and (2.4) are not considered. A modified model with (2.1) to (2.4) included is shown in Fig. 5, where the T_j dependencies of V_{TH} and R_G are characterized by the components drawn in green.

The temperature dependency of V_{TH}, R_G, C_{GS} and C_{GD} are not characterized by the LTSpice model in [54]. An improved model, including the aforementioned junction temperature dependencies, is shown in Fig. 3.1.7, with V_{TH}, R_G, C_{GS} and C_{GD} characterized by the components drawn in green.

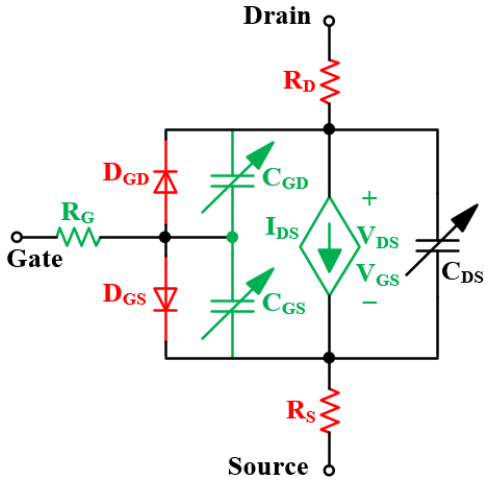


Fig. 3.1.7 GaN HEMT T_j dependent model with the temperature dependency of V_{TH}, R_G, C_{GS} and C_{GD}

3.1.4 Semiconductor SPICE Model

Simulation Program with Intergrated Circuit Emphasis (SPICE) is a computer simulation and modeling simulator used by engineers to mathematically predict the behavior of electronics circuits. Developed at the University of California at Berkeley, SPICE can be used to simulate circuits of almost all complexities. However, SPICE is generally used to predict the behavior of low to mid frequency (DC to around 100MHz) circuits. If the power semiconductor can switch up to 1GHz, the switching transient modeling might need some other simulator to include the radio frequency circuit properties.

SPICE can be used to simulate devices ranging from the most basic passive elements such as resistors and capacitors to complicated semiconductor devices such as MOSFETs and IGBTs. Using these intrinsic components as the basic building blocks for larger models, device manufacturers have been able to define a truly vast and diverse number of SPICE models for their products. These SPICE models from device manufacturers are usually regarded as the first priority to emulate the device electrical properties.

The quality of SPICE models can vary, and not all SPICE models are applicable to every application. It is important to consider this when using the models supplied with a SPICE simulation package. Using a SPICE model inappropriately can lead to inaccurate results, or even generate an error in some circumstances.

A circuit must be presented to SPICE in the form of a netlist. The netlist is a text description of all circuit elements such as transistors and capacitors, and their

corresponding connections. The SPICE model for the SiC MOSFET used in this research, Rohm semiconductor SCT2160KE, is attached as following.

CODE BEGIN

```
*$
* SCT2160KE SiC NMOSFET model
* Model Generated by ROHM
* All Rights Reserved
* Commercial Use or Resale Restricted
* Date: 2013/08/23
******************D G S
.SUBCKT SCT2160KE_a 1 2 3
.PARAM T0=25
.FUNC R1(I)   {110.5m*I*(1+0.4248*(EXP((TEMP-T0)/105.5)-1))+
+            269.6u*I*ABS(I)**(1.428/(1+0.3926*(EXP((TEMP-T0)/-34.01)-1)))*
+           (1+0.8112*(EXP((TEMP-T0)/-16.75)-1))}
.FUNC      V1(V,W)      {V-113.5m*W/(1+0.4495*(EXP((TEMP-T0)/-165.0)-1))-
441.0m*ASINH(W/0.3311)}
.FUNC   V2(V)       {IF(V>0,2.708u*V**(7.313*(1+0.01930*(EXP((TEMP-T0)/-
43.99)-1)))/
+           (1+0.9562*(EXP((TEMP-T0)/-31.80)-1)),0)}
.FUNC I1(V,W) {V*(ABS(W)+1000)/1010*1.2*W/(ABS(W)+2)}
.FUNC C1(V)   {IF(V>-1.749,847.2+152.9*V,1114*(1-V/1.590)**-0.8804)}
.FUNC C2(V)   {C1(V)*(0.3768*TANH((V+1.674)*2.035)+0.5813)+6.306}
V1  1 11 0
E1 11 12 VALUE={R1(LIMIT(I(V1),-1MEG,1MEG))}
V2  2 21 0
E2 21 22 VALUE={I(V2)*17.1}
V3  3 31 0
E3 31 32 VALUE={I(V3)*0.00}
E4 41  0 VALUE={LIMIT(V(22,32),0,22)}
E5 42  0 VALUE={V1(V(41),LIMIT(V(43),0,200))}
E6 43  0 VALUE={V2(LIMIT(V(42),0,20))}
G1 12 32 VALUE={I1(V(43),V(12,32))}
C1 12 32 1p
R1 12 32 1E15
E7 51  0 VALUE={V(22,1)}
E8 52  0 VALUE={V(22,1)}
V4 52 53
C2 53  0 1p
G2 22  1 VALUE={I(V4)*C2(V(51))}
C3 22 32 1.193n
```

```
R2 22 32 1G
********* ********* ********* ********* ********* ********* ********* ********* ********* *********
.FUNC R101(I) {814.1m*ASINH(I/4.137)*EXP((TEMP-T0)/-5063)+1.083m*I*ABS(I)}
.FUNC I101(V) {IF(V>0,587.5u*V**(8.659*EXP((TEMP-T0)/-1022))*EXP((TEMP-T0)/47.71),0)}
.FUNC I102(V) {IF(V<0,1.528n*(EXP(V/10)-1)*EXP(-V/969.2)*EXP((TEMP-T0)/267.4)*
+ (EXP((-V-1720*EXP((TEMP-T0)/1250))/10)+1),0)}
.FUNC C101(V) {IF(V>0.7034,584.0+682.8*V,778.4*(1-V/1.407)**-0.4513)-16.59-12.87m*V}
V101 3 103 0
E101 103 104 VALUE={R101(LIMIT(I(V101),-1MEG,1MEG))}
E102 111 0 VALUE={V(104,1)}
E103 112 0 VALUE={V(104,1)}
V102 112 113 0
C101 113 0 1p
G101 104 1 VALUE={I101(LIMIT(V(111),0,20))+I102(LIMIT(V(111),-3k,0))+
+ I(V102)*C101(LIMIT(V(111),-3k,20))}
.ENDS SCT2160KE
*$
```

CODE END

It can be seen in the SCT2160KE SPICE model that the device operating temperature can be defined by the user in T0. Because the switching and conducting properties of SCT2160KE MOSFET are T_j dependent, most of the device properties are T0 sensitive in the SPICE model. In this research, when simulating the switching power semiconductor under different T_j, the operating temperature like T0 in the SPICE will be preset accordingly.

3.2 Gate Drive System Dynamic Model

For a hard switching power converter, it is always desired that the switching power semiconductor turn-on time (sometimes refered to as the rise time) t_r is as short as possible. This is because a shorter switching time will cause less device switching loss.

Switching power semiconductor manufacturers usually provide the gate charge value for simple t_r calculation. Typically, device turn-on time can be calculated using the following equation:

$$t_r = \frac{Q_g}{I_g} \tag{3.2.1}$$

where I_g is device gate drive output current. Hence, for a particular Q_g, increasing I_g will decrease t_r. Thus, the gate drive output capability will have a significant effect on the power semiconductor switching transient.

Unfortunately, gate drive manufacturers do not provide a detailed circuit model for the gate drive output power stage. Therefore, the gate drive output capability can only be estimated based on its output characteristics. Fig. 3.2.1 and Fig. 3.2.2 shows the output current capability and the output resistance of an IXDN630 integrated gate drive.

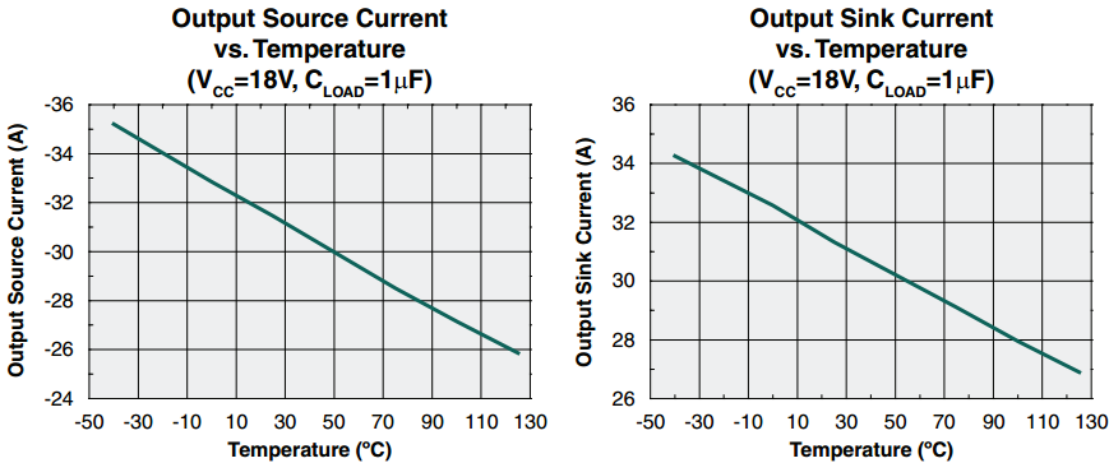


Fig. 3.2.1 Current output capability for IXDN630 gate drive

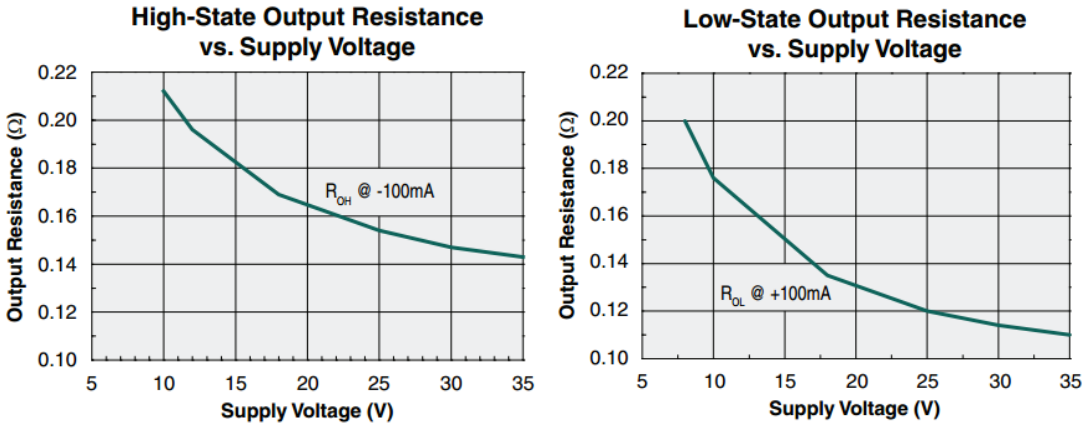


Fig. 3.2.2 Output resistance for IXDN630 gate drive

Based on the switching power semiconductor output power stage topology, the gate drive systems can be categorized into two types: voltage mode and current mode. The voltage mode gate drive (including the push-pull output gate drive, bootstrap capacitor gate drive, and so forth) manipulates the gate drive output voltage, as shown in Fig. 3.2.3. The current mode gate drive (including the current mirror based current source

gate drive, the inductor based current source gate drive, and so forth) manipulates the gate drive output current, as shown in Fig. 3.2.4.

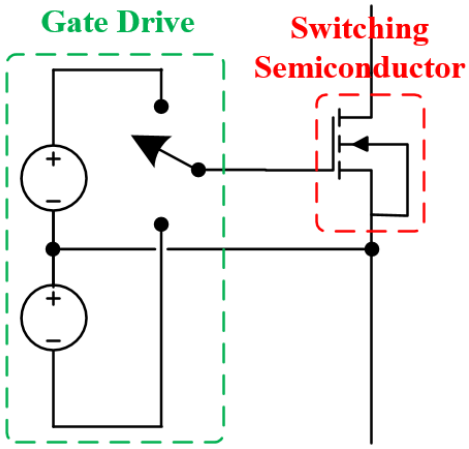


Fig. 3.2.3 Voltage mode gate drive

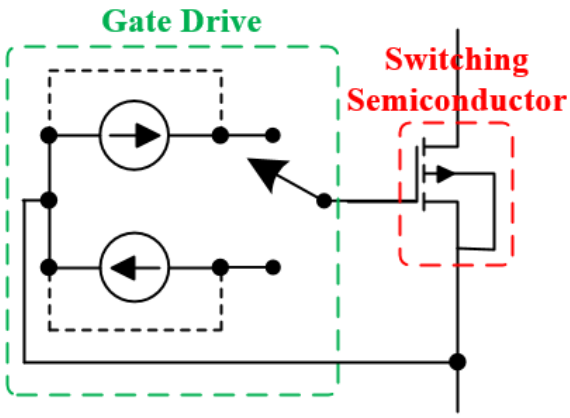


Fig. 3.2.4 Current mode gate drive

3.2.1 Push-pull Output Based Voltage Source Gate Drive

Most of the integrated power semiconductor gate drives use the push-pull output, which achieves simple turn-on/turn-off control and fast hard switching. In this research, to turn on the studied switching power semiconductors, the gate-source voltage (V_{GS}) or

gate-emitter voltage (V_{GE}) should be set between +10V and +18V. To turn off the switching power semiconductors, V_{GS} or V_{GE} should be set between 0V and -10V [50]. In the push-pull output stage, a P-type MOSFET is used as a pull-up transistor and an N-type MOSFET is used as a pull-down transistor. A logic inverter is also included in the gate drive system so that the gate drive input on/off logic can be synchronized to the gate drive output high/low state.

The dynamic model for the push-pull output gate drive is shown in Fig. 3.2.5. The model includes the switching control signal, the logic inverter, the push-pull output stage, the gate drive resistance, and the parasitics in the gate drive system. A current sensing resistor R_{sense1} is implemented in the gate drive system for the gate drive turn-on current (i_{G1}) sensing. An ideal logic inverter model is used in the gate drive system modeling. Spice level 3 MOSFET model is used for the simulation of the two MOSFETs in the push-pull output stage.

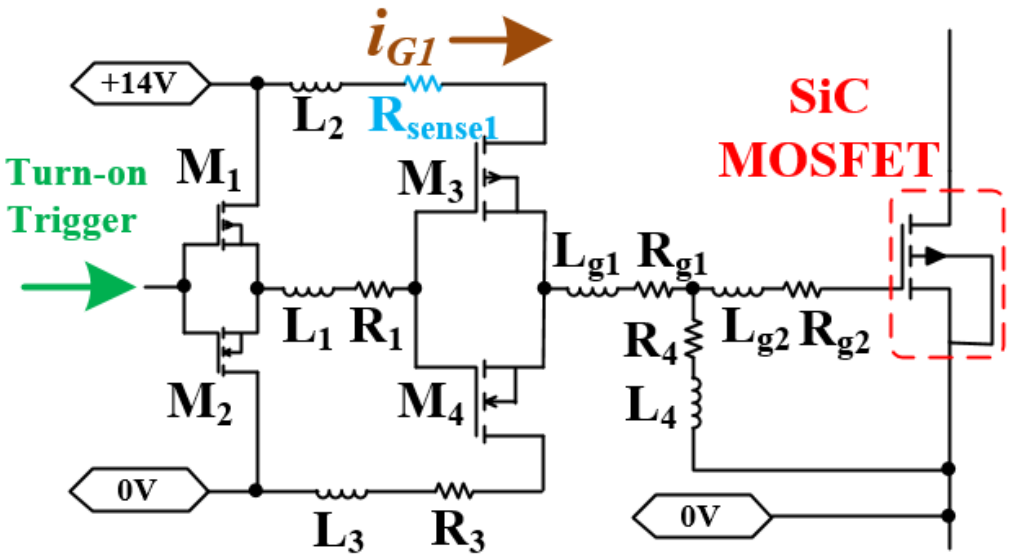


Fig. 3.2.5 Push-pull output gate drive dynamic model

In the device turn-on transient, as shown in Fig. 3.2.6, M_1 in the logic buffer is turned on by the external turn-on trigger. When M_1 is on, the gate drive pull-up switch M_3 will be turned on. The on-state M_3 will connect the SiC MOSFET gate to +14V, and the gate drive turn-on current i_{G1_ON} will charge the gate via R_{sense1}. In the SiC MOSFET turn-off transient, as shown in Fig. 3.2.7, M_2 will be turned on by the external turn-off trigger, followed by the turn-on of M_4. M_4 will connect the gate to 0V, and the gate will be discharged with the gate drive turn-off current i_{G1_OFF}.

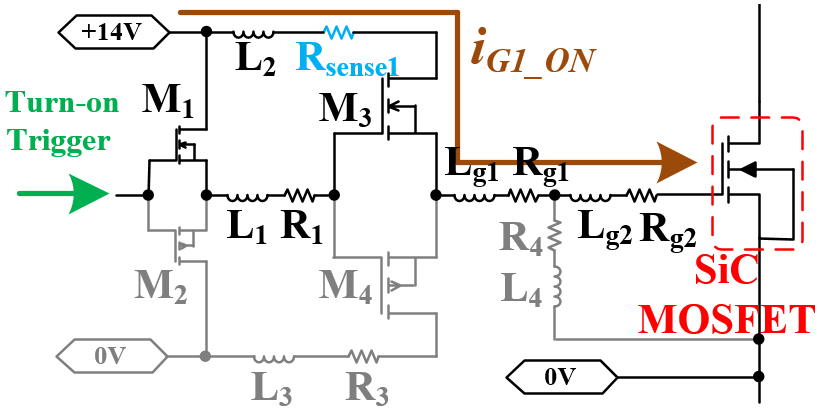


Fig. 3.2.5 Push-pull output gate drive turn-on transient

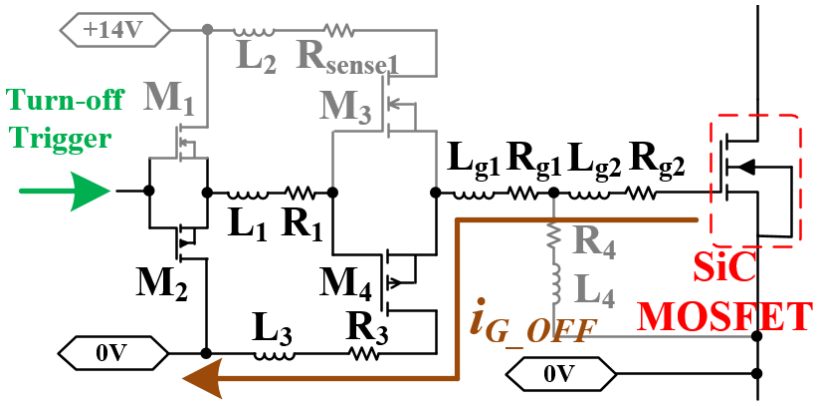


Fig. 3.2.6 Push-pull output gate drive turn-off transient

3.2.2 Current Mirror Based Current Source Gate Drive

Wide bandgap semiconductors using Silicon Carbide (SiC) or Gallium Nitride (GaN) usually have a smaller gate charge value compared with conventional Si MOSFET and IGBT (The comparison should be based on the same power rating). As a result, very large dV_{DS}/dt can make the switching voltage/current overshoot a big risk for the converter system. In such cases, switching speed control from the gate drive is desired. By manipulating the output current value, current source gate drive is feasible for semiconductor smooth switching.

In this research, a current mirror is implemented in the current source gate drive high side using a P type bipolar junction transistor (BJT), as shown in Fig. 3.2.7. The gate drive output current source can be manipulated by adjusting the value of the reference resistance R_{ref}. M_1 can activate the current mirror, and the current mirror will be used only to turn on the SiC MOSFET. To turn off the SiC MOSFET, the MOSFET gate will be connected to the MOSFET source by M_2. If current control turn off is desired, a current sink should be implemented in the gate drive low side.

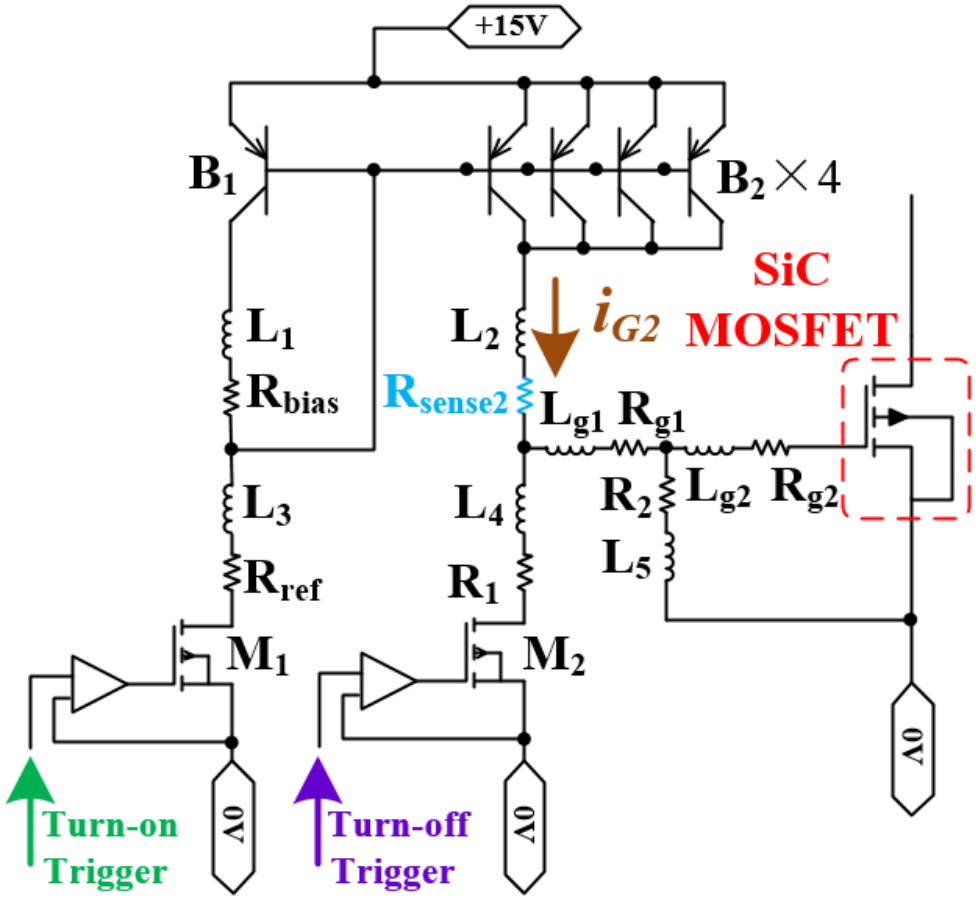


Fig. 3.2.7 Current mirror gate drive dynamic model

In Fig. 3.2.7, the gate drive dynamic model include the current mirror BJTs (B_1 and B_2), the current mirror activating MOSFET M_1, the pull-down MOSFET M_2, the gate drive resistance, and the parasitics in the gate drive system. A current sensing resistor R_{sense2} is implemented in the gate drive system for the gate drive turn-on current (i_{G2}) sensing. SPICE level 3 BJT model is used for the simulation of all the BJTs and MOSFETs in the gate drive system.

The gate drive output current mirror can be manipulated by adjusting the value of the reference resistance R_{ref}. M_1 can turn on the current mirror, and the current mirror

will be used only to turn on the SiC MOSFET, as shown in Fig. 3.2.8. In this research, NXP semiconductor PBSS5540Z PNP type BJT is used for B1 and B2. By implementing one BJT on the current mirror control side (left) and four BJTs on the output side (right), the current ratio between the output side and the control side is 4. To turn off the SiC MOSFET, the gate of SiC MOSFET will be connected to the MOSFET source (0V) by M_2, as shown in Fig. 3.2.9. If current-control is desired during turn-off, a current sink should be implemented in the gate drive low side.

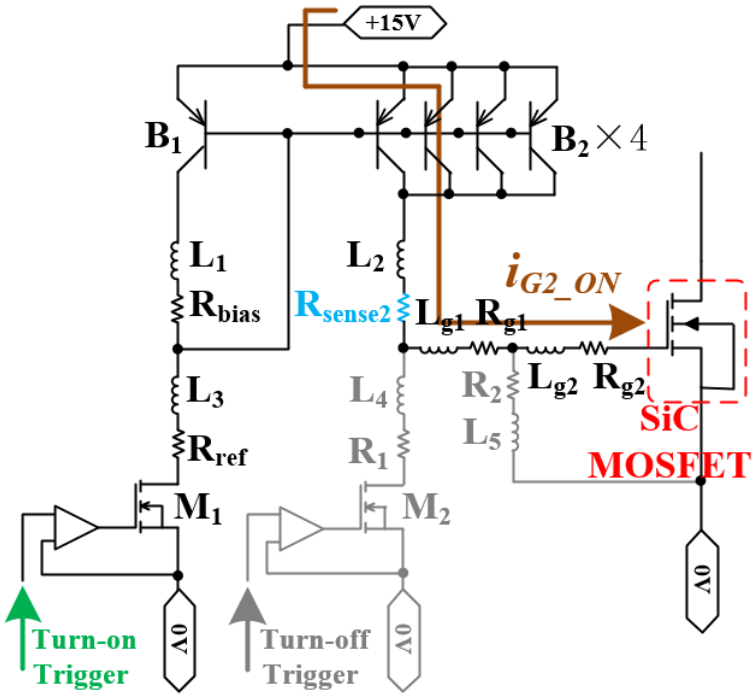


Fig. 3.2.8 Current mirror gate drive turn-on transient

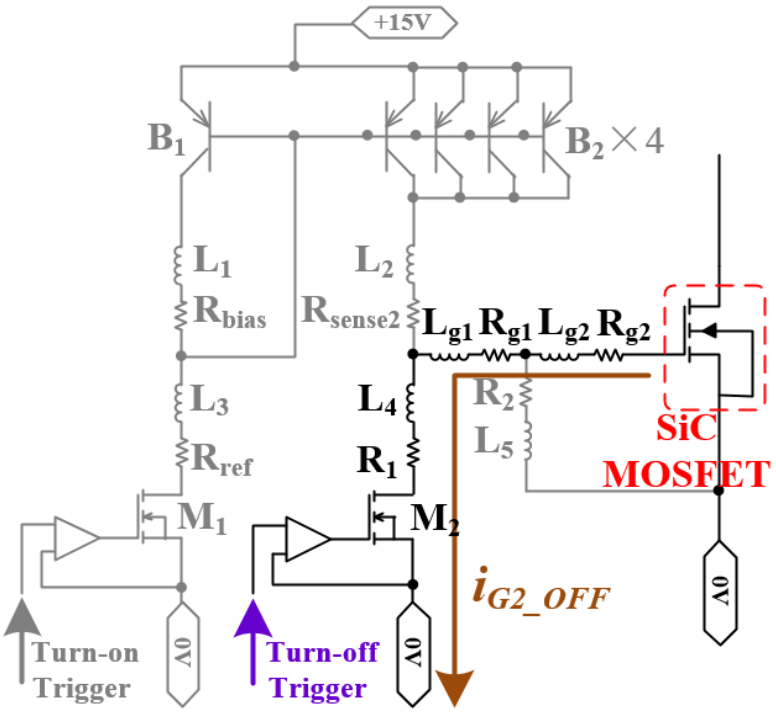


Fig. 3.2.9 Current mirror gate drive turn-off transient

3.2.3 Inductor Based Current Source Gate Drive

In electrical circuits, an inductor can be used as a current stiff component. [58] proposed a gate drive topology using an inductor-based current source gate drive, and this gate drive circuit is used in this research for SiC MOSFET online T_j sensing.

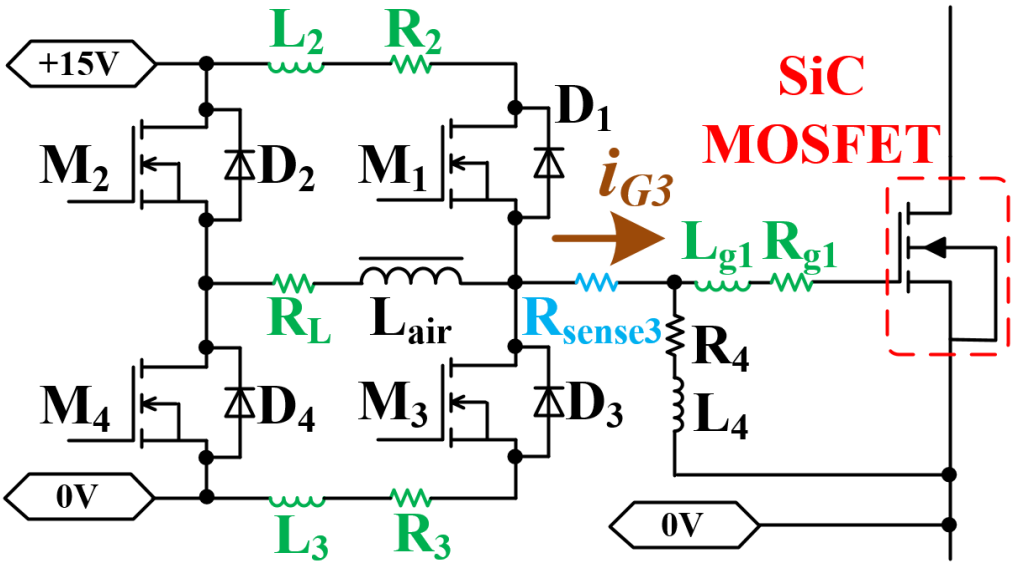


Fig. 3.3.1 Inductor-based gate drive dynamic model

The inductor-based current source gate drive dynamic model from [18] was improved by adding parasitics (green) and a shunt current-sensing resistor (blue) as is shown in Fig. 3.3.1. Four controlled switches (M_1 to M_4) and their anti-parallel diodes (D_1 to D_4) are connected as an H-bridge with an air-core inductor L_{air} implemented as the load. By properly operating the controlled switches, the SiC MOSFET gate turn-on and turn-off process can start with a non-zero pre-charge current. Following the charging and discharging of the SiC MOSFET, the excess energy stored in the inductor can be returned to the 15V power supply, thereby allowing the gate charge energy to be recovered. A current sensing resistor R_{sense3} is implemented in the gate drive system for the gate drive current (i_{G3}) sensing.

The turn-on operation of the inductor-based current source gate drive is summarized as follows:

Stage 1: Before charging the SiC MOSFET gate, L_{air} needs to be pre-charged by activating M_2 and M_3 together, as shown in Fig. 3.3.2.

Stage 2: When L_{air} is charged to the desired current, M_3 is actively shut down, which injects the current from L_{air} into the gate of the SiC MOSFET, as shown in Fig. 3.3.3.

Stage 3: After the SiC MOSFET gate voltage is charged to +15V, M_1 is actively turned on, feeding the residual energy stored in the inductor back to the +15V supply, as shown in Fig. 3.3.4.

Stage 4: M_1 is kept on during SiC MOSFET on-state so that the SiC gate is connected to the +15V supply, as shown in Fig. 3.3.5.

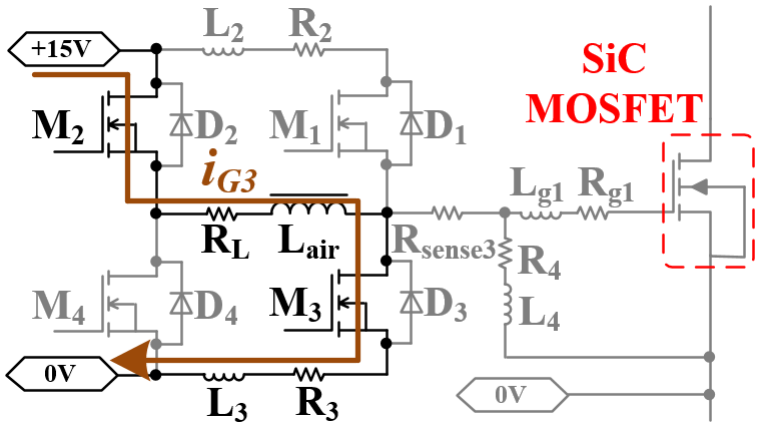


Fig. 3.3.2 Inductor-based gate drive turn-on transient, stage 1

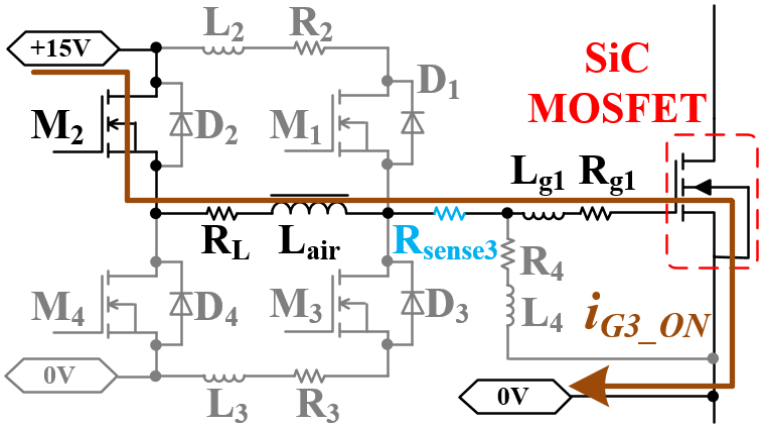


Fig. 3.3.3 Inductor-based gate drive turn-on transient, stage 2

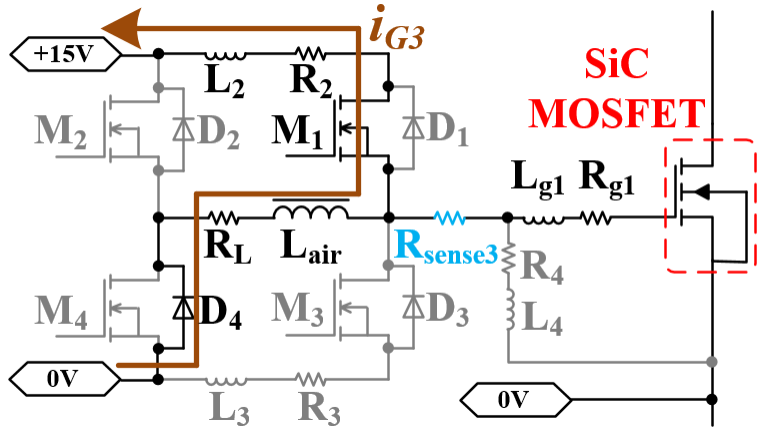


Fig. 3.3.4 Inductor-based gate drive turn-on transient, stage 3

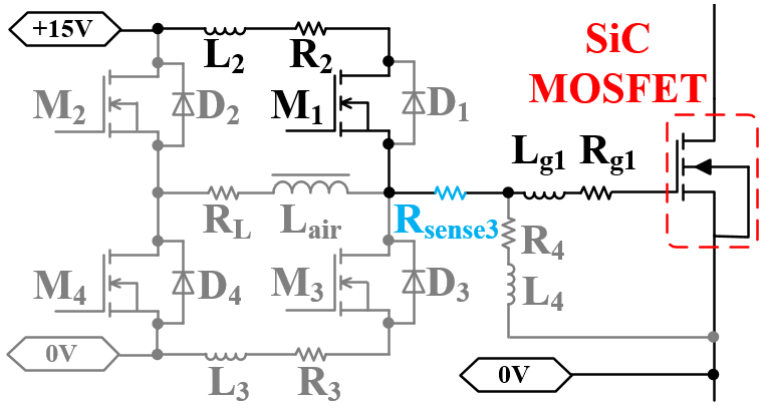


Fig. 3.3.5 Inductor-based gate drive turn-on transient, stage 4

The turn-off operation of the inductor-based current source gate drive is sequenced as follows:

Stage 5: Before discharging the SiC MOSFET gate, L_{air} needs to be pre-charged by activating M_1 and M_4 together, as shown in Fig. 3.3.6

Stage 6: When L_{air} is charged to the desired current, M_1 is actively shut down, which pulls the current out from the gate of the SiC MOSFET by L_{air}, as shown in Fig. 3.3.7.

Stage 7: After the SiC MOSFET gate voltage is discharged to 0V, M_3 is actively turned on, feeding the residual energy stored in the inductor back to the +15V supply, as shown in Fig. 3.3.8.

Stage 8: M_3 is kept on during SiC MOSFET off-state so that the SiC gate is connected to the 0V supply, as shown in Fig. 3.3.9.

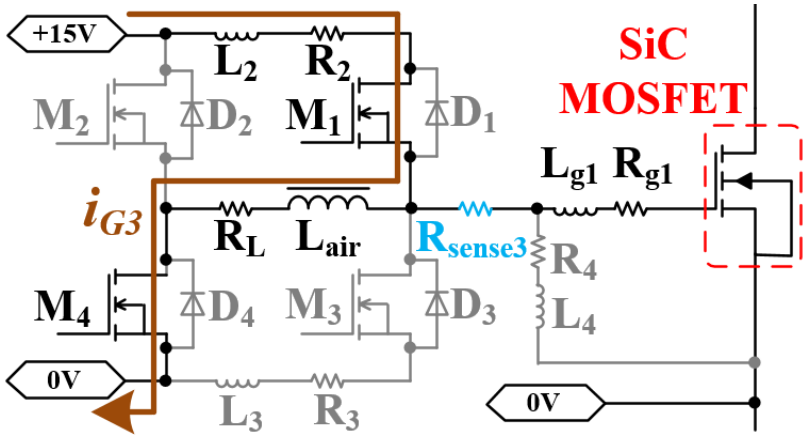


Fig. 3.3.6 Inductor-based gate drive turn-off transient, stage 5

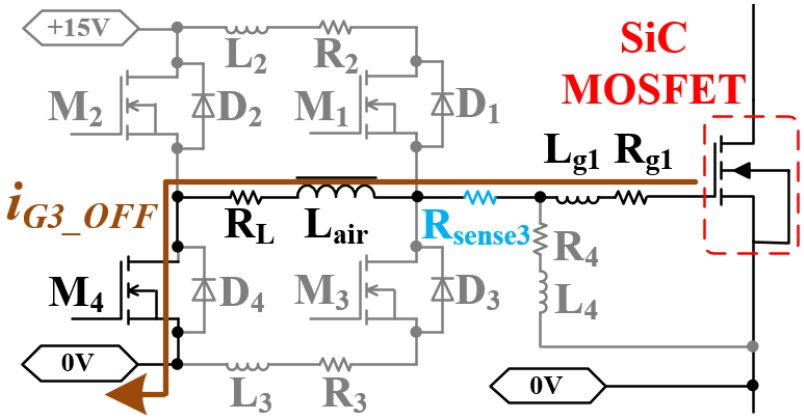


Fig. 3.3.7 Inductor-based gate drive turn-off transient, stage 6

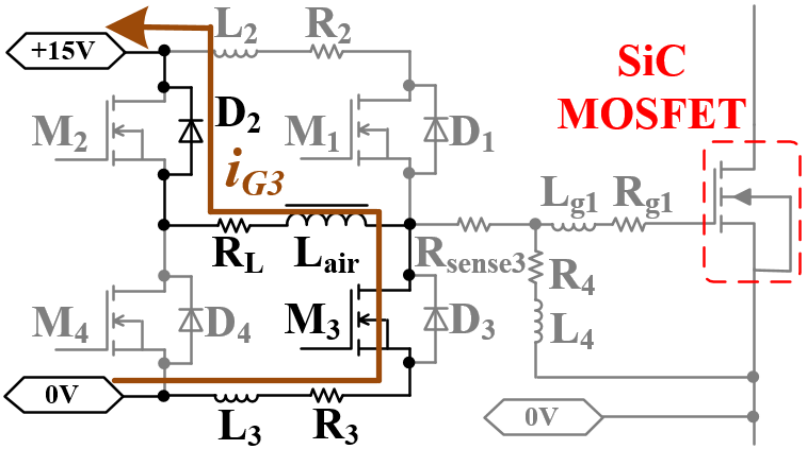


Fig. 3.3.8 Inductor-based gate drive turn-off transient, stage 7

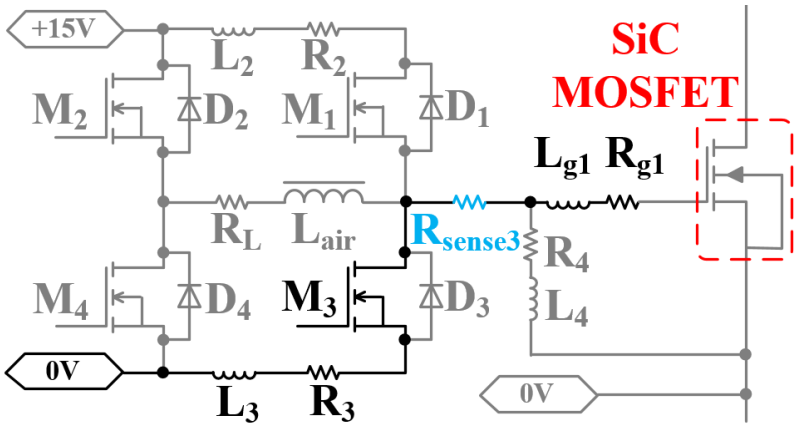


Fig. 3.3.9 Inductor-based gate drive turn-off transient, stage 8

3.3 H-bridge Inverter Dynamic Model

To demonstrate the swiching power semiconductor T_j sensing in this research, either a discrete power device or a power module are implemented in a single phase H-bridge inverter (four switches are used). The H-bridge inverter circuit model is shown in Fig. 3.4.1 including the DC bus voltage source, four power switches with their anti-parallel diodes, four gate drives, and the load. Very simple switching schiem (did you mean scheme?) is applied to the H-bridge inverter with the switching time table drawn in Fig. 3.4.2, and the four power devices will be switched in the same duty ratio. By synchronously adjusting the switching duty ratio of the four power devices, their T_j can be manipulated while other circuit conditions remain the same.

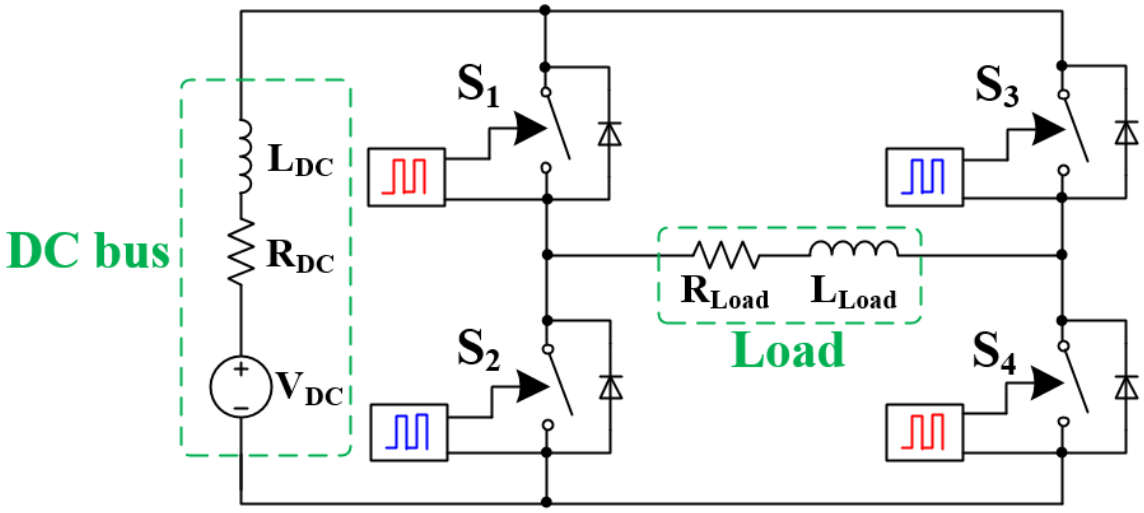


Fig. 3.4.1 Single phase H-bridge inverter modeling

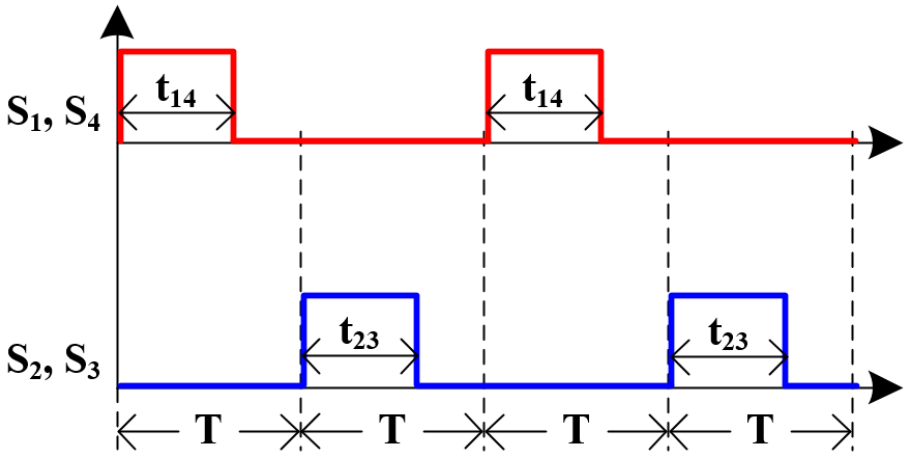


Fig. 3.4.2 Single phase H-bridge inverter switching timeline

3.4 Summary of System Modeling and Simplification

This chapter presented the dynamic modeling and simplification of the T_j sensing implementation. The system dynamic modeling includes the switching power semiconductor turn-on dynamic model, the gate drive output stage dynamic model, and the H-bridge inverter model. The switching power semiconductor turn-on gate characteristics and the gate drive turn-on output transients are modeled with extra effort to benefit the T_j sensing from the gate drive side.

The models proposed in this chapter are based on the hardware setup in this research and will be used to emulate and predict the T_j sensing experimental results. The simulation results from the proposed system dynamic model will be compared with experimental results in chapter 4.

Chapter 4 Experimental Test Stand

This chapter will introduce the experimental test stand used to verify the "gate drive output based T_j sensing" proposed in this research. The discussion will include the test stand for Fuji 2SK3677 discrete silicon MOSFET, Fuji 7MBR15SA140 6-in-1 silicon IGBT power module, and Rohm SCT2160 discrete SiC MOSFET.

4.1 System Level Configuration

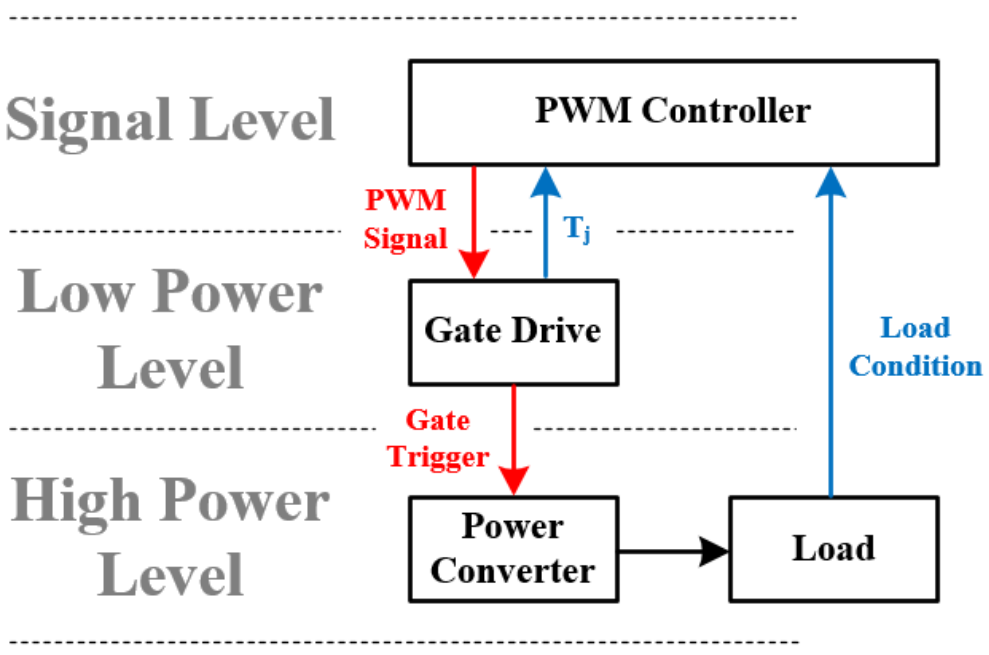


Fig. 4.1.1 Power conversion system with active Tj control

The final system configuration of this research will be a converter system with all the switching power semiconductor T_j sensed from the gate drive side. Based on the feedback T_j information from the converter gate drive system, the control system calculated the PWM signal for the converter in order to actively control the T_j of each

switching power semiconductor in the converter. The illustration for the system with active T_j control is shown in Fig. 4.1.1.

In the prelimary of this research (I'm not sure if this is the correct way to term this), an open-loop system with T_j sensing is implemented as shown in Fig. 4.1.2. In the open-loop system, T_j and Iload can be manipulated from the PWM controller.

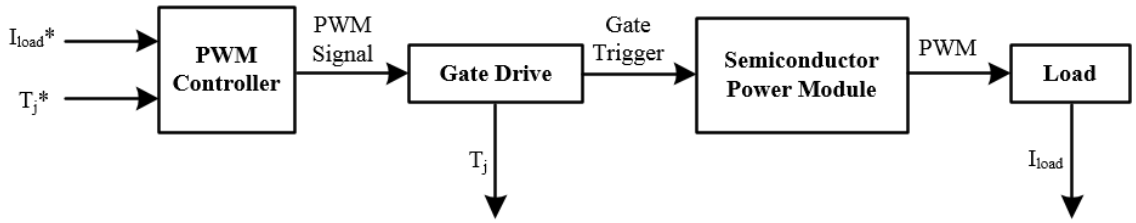


Fig. 4.1.2 Open-loop system with Tj sensing

In the final dessertation of this research, the sensed T_j and load current will be fed back to the PWM controller and a closed-loop system with active T_j control and I_{load} control will be implemented as shown in Fig. 4.1.3.

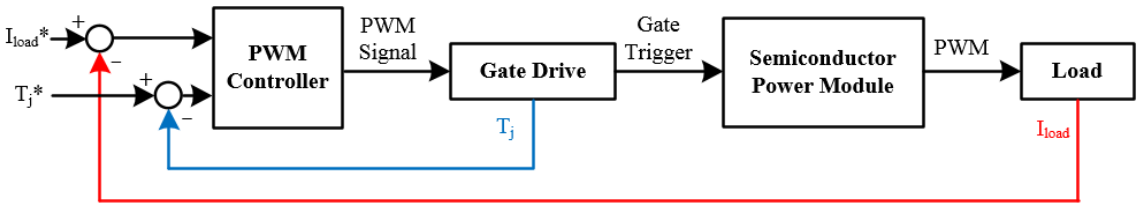


Fig. 4.1.3 Closed-loop system with active Tj control

An EZDSP development board with tms320f28335 digital signal processor is used as the PWM controller. With six independent enhanced PWM modules, a three phase two level inverter can be modulated. To implement the PWM to a multi-level converter in the final dissertation, a field-programmable gate array will be required to

modulate more than six power switches. The picture of the PWM controller is shown in Fig. 4.1.4.

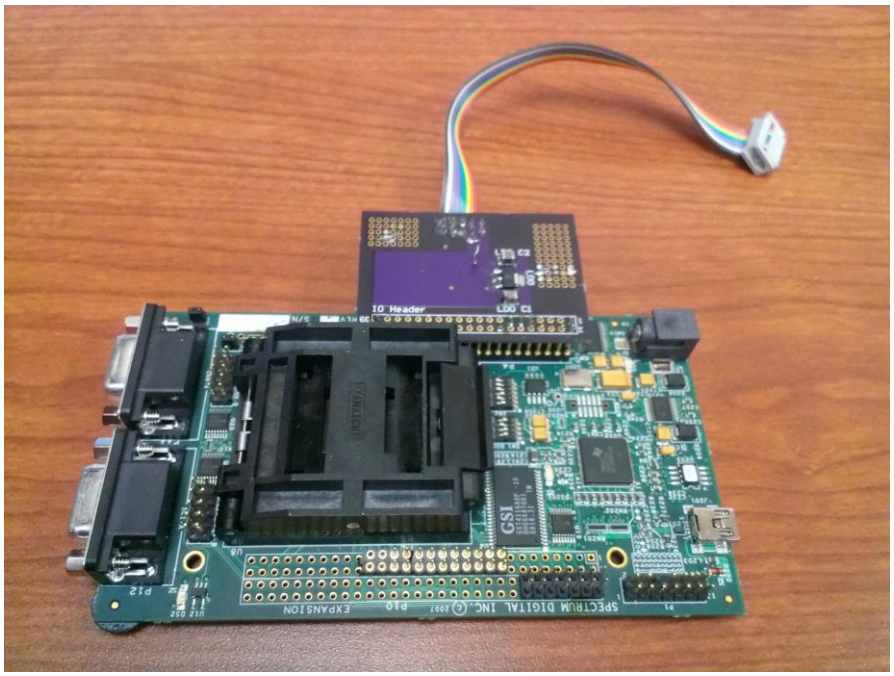


Fig. 4.1.4 EZDSP development board with tms320f28335 digital signal processor

Isolated gate drives are implemented on independent PCBs. The portable gate drives take power from the DC bus. The T_j information sensed by the gate drive will be held by the gate drive in each switching cycle, so that the PWM controller can read T_j feedback from the gate drive when T_j is not updating. A prototype portable IGBT gate drive with integrated T_j sensing on board is shown in Fig. 4.1.5.

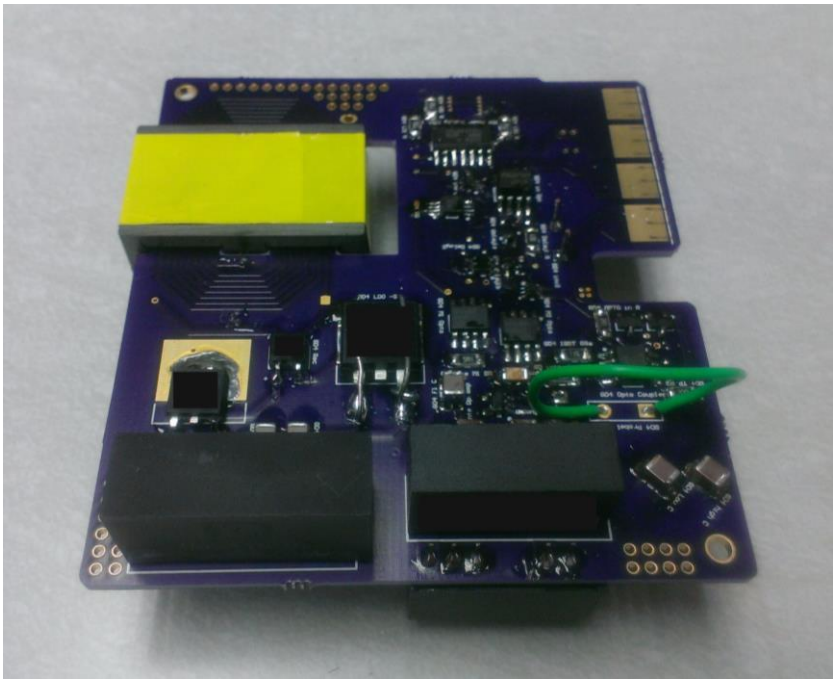


Fig. 4.1.5 Prototype portable IGBT gate drive with integrated T_j sensing

The H-bridge inverter is implemented on the main circuit board as shown in Fig. 4.1.6 with four portable gate drive, the DSP based PWM controller, and the connection to the DC bus and the load.

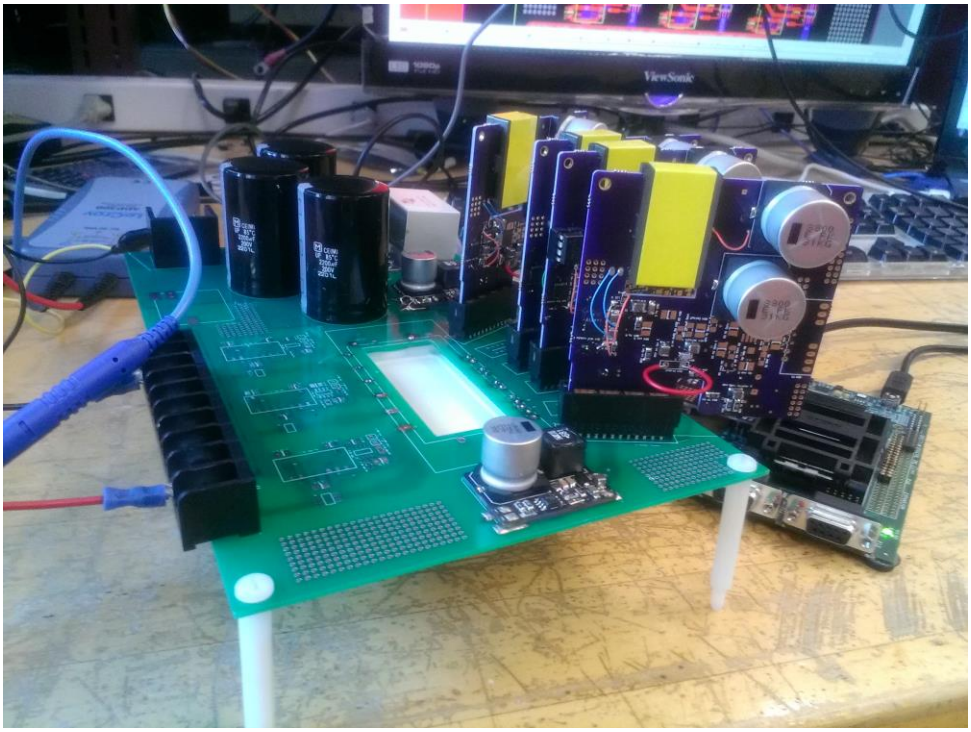


Fig. 4.1.6 H-bridge with gate drive and PWM controller

4.2 Un-encapsulated Sample, De-capsulated Sample, and Open Module

In this research, to calibrate the T_j sensing accuracy of the proposed methods, the semiconductor chip surface temperature will be directly measured by the Flir thermal camera. To access to the swiching power semiconductor chip surface, several methods have been applied to different power devices.

To investigate the Si MOSFET T_j sensing, Fuji 2SK3677-01MR power MOSFETs are implemeneted in the H-bridge inverter prototype. Un-emcapulated samples provided by the device manufacturer can be measured by the Flir thermal camera without further processing, as shown in Fig. 4.2.1. To illustrate the effect of the

device surface emissivity on the Flir thermal camera measurement, all the Si MOSFET device T_j are not painted with black coating.

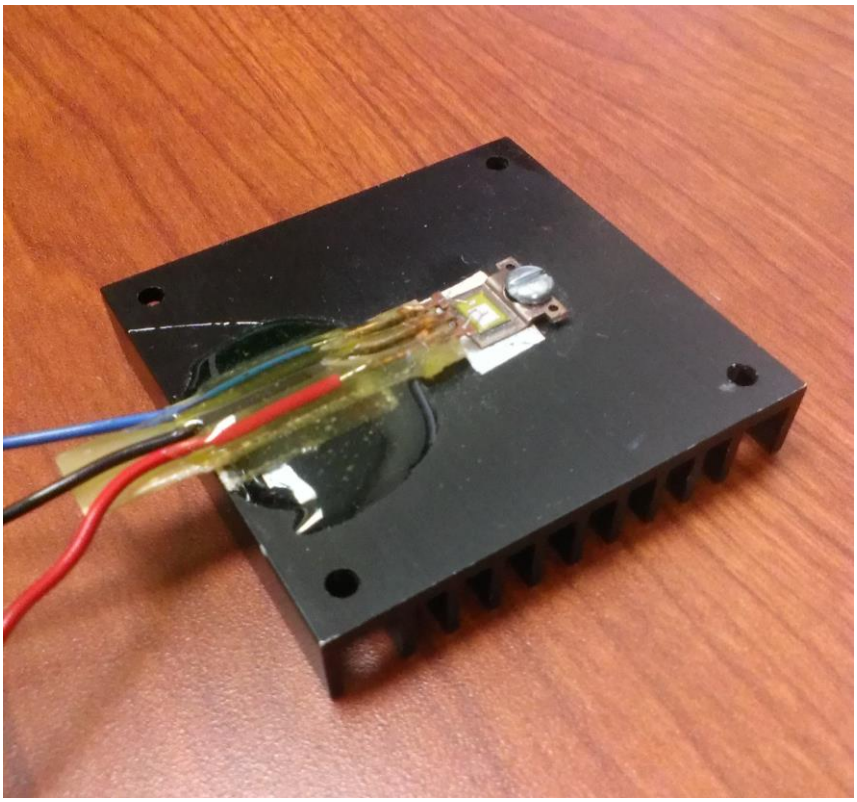


Fig. 4.2.1 Fuji 2SK3677-01MR power MOSFET, un-encapsulated sample

To study the Si IGBT T_j sensing, Fuji 7MBR15SA140 IGBT module is configured as an H-bridge inverter (only four IGBTs in the module is used). The power module is manually opened after manufacture. The stiffness gel in the module is chemically removed, and the power semiconductor chip is entirely exposed as shown in Fig. 4.2.2. In the prototype test, the exposed semiconductor chip is painted with black coating to get consistant surface emissivity, as shown in Fig. 4.2.3.

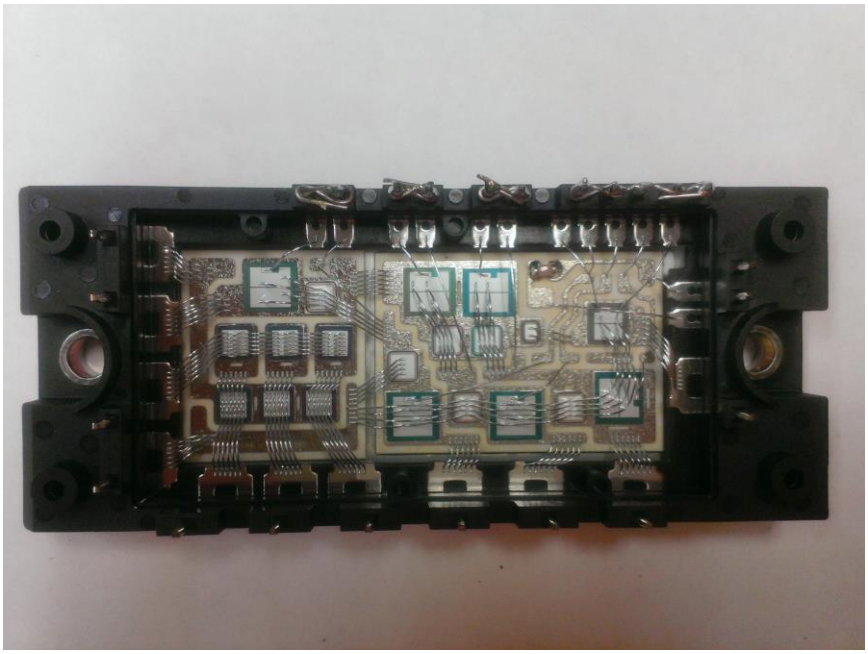


Fig. 4.2.2 Fuji 7MBR15SA140 IGBT module open sample, stiffness gel removed

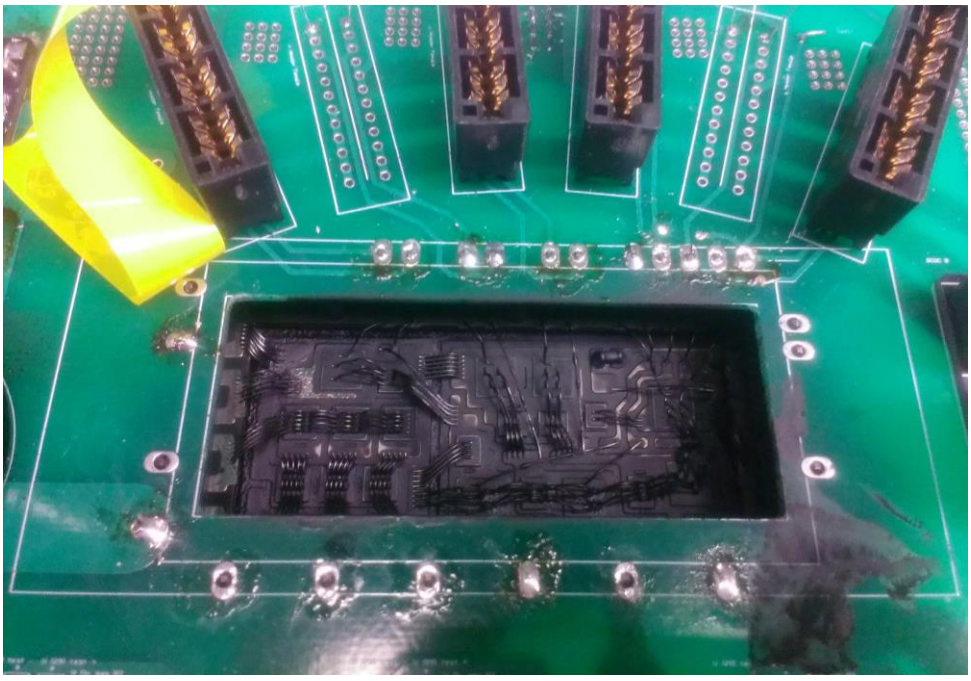


Fig. 4.2.3 Fuji 7MBR15SA140 IGBT module open sample, covered by black coating

To demonstrate the SiC MOSFET T_j sensing, Rohm SCT2160KE SiC MOSFETs are implemented in the H-bridge inverter prototype. The original device is in a TO-247 three-pin package as shown in Fig. 4.2.4.

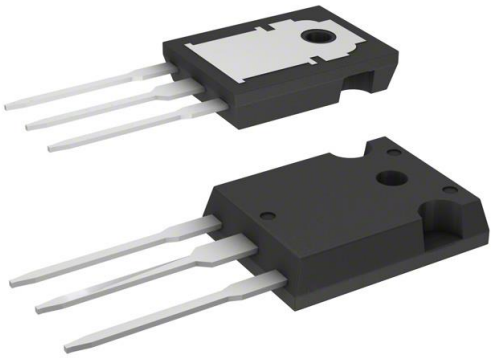
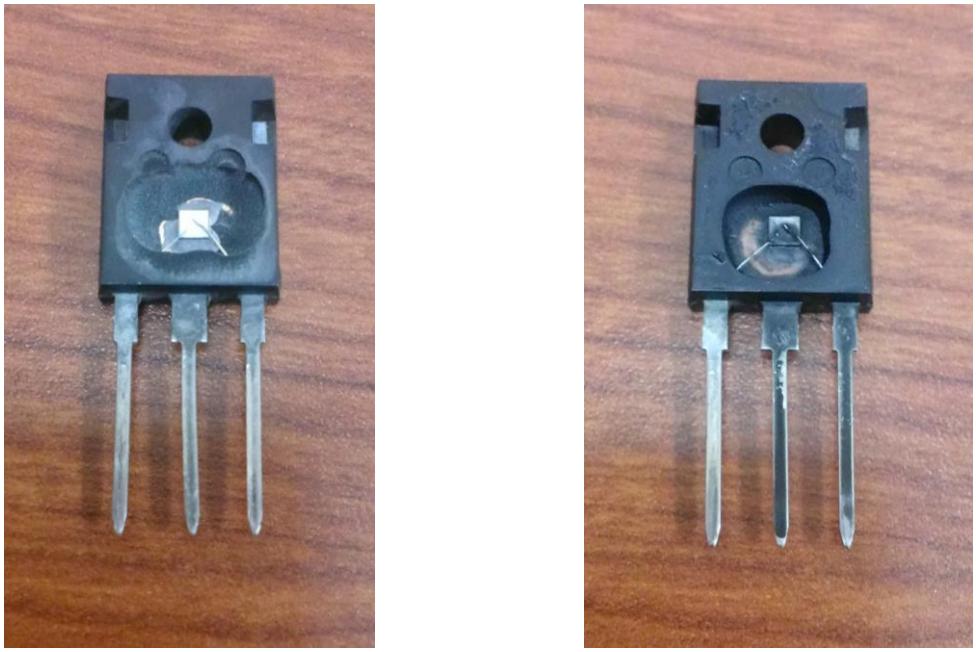


Fig. 4.2.4 TO-247 three-pin package for Rohm SCT2160KE SiC MOSFET

The packed device is de-capsulated physically and chemically as shown in Fig. 4.2.5(a). Black coating is applied to the semiconductor chip surface to achieve consistant surface emissivity as shown in Fig. 4.2.5(b).



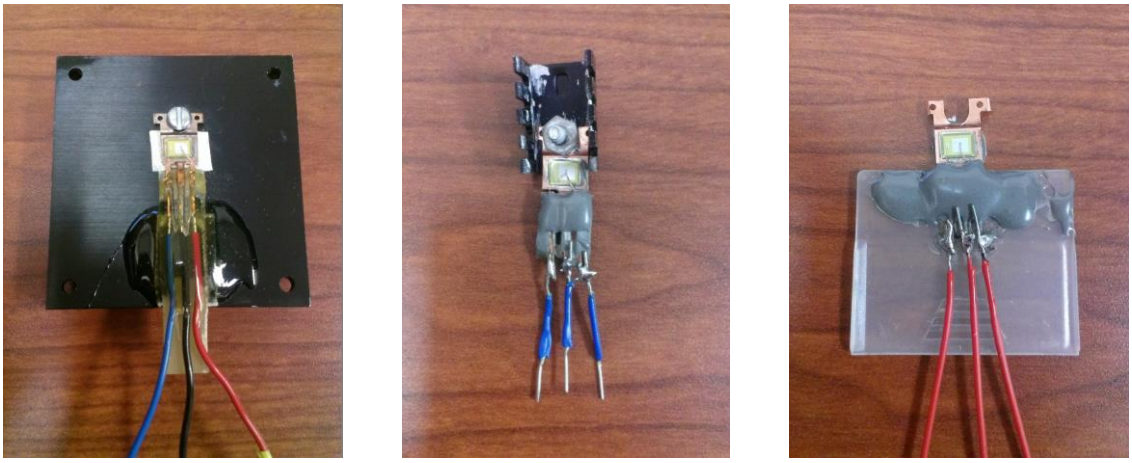
(a) (b)

Fig. 4.2.5 Rohm SCT2160KE SiC MOSFET, decapsulated samples

4.3 Heat Sink

In this research, most of the device thermal test is achieved without using the heat sink. This is because the heat sink can severely slow down the thermal dynamics of the device, making the T_j manipulation time consuming.

However, the effect of using different heat sink is still considered in this research. The heat sink effect test is only achieved on the Fuji 2SK3677-01MR Si MOSFET. The Si power MOSFET with different heat sink is shown in Fig. 4.3.1. The prototype test for the heat sink effect will be discussed in chapter 5.



Big heat sink Small heat sink No heat sink

Fig. 4.3.1 Un-encapsulated Fuji 2SK3677-01MR Si MOSFETs attached to different heat sink

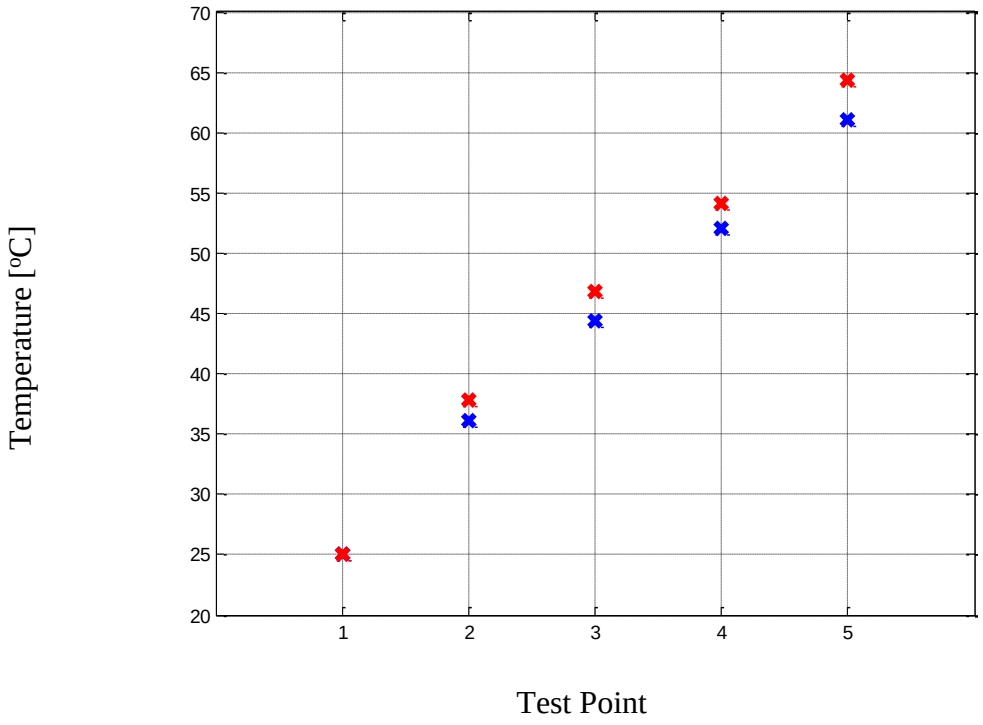
4.4 Flir Thermal Camera and Device Surface Emissivity

In this research, a FLIR SC500 thermal camera is used to calibrate the gate drive output current transient based T_j sensing method. In the prototype test and calibration, a thermal camera is used to capture the thermal image when the device is thermally steady state. The T_j measured by the thermal camera will be compared with the T_j sensed by the switching power semiconductor gate drive.

Depending on the emissive characteristics of the semiconductor chip surface, thermal camera observations have un-negligible systematic errors. The emissivity of the surface of a material is its effectiveness in emitting energy as thermal radiation. It is the ratio of energy radiated by particular material to energy radiated by a black body at the same temperature. A absolute black body have an emissivity $\varepsilon = 1$ while any real object would have an emissivity $\varepsilon < 1$.

There are two basic methods to calibrate the thermal camera with regard to object emissive characteristics. One commonly used method is to paint the surface of the testing object to black. An intentionally painted black surface can be approximately considered as a black body with emissivity $\varepsilon = 1$. However, depending on the thickness of the painting material and the temperature dependent properties of the painting material, the object surface emissivity can still affect testing results at a relatively high thermal test range (100^{o}C).

Another method is to directly calibrate the thermal camera without an intentionally painted black surface. In some research, a high accuracy temperature controlled oven is used to warm up the test circuit to a desired temperature and the thermal camera can be calibrated by a series of thermal test on a temperature-known object surface. The emissivity calibration for FLIR SC500 thermal camera used in this research is shown in Fig. 4.4.1. Because of the oven limitation, the calibration can only be performed below 75^{o}C. Fuji 2SK3677-01MR Si MOSFET without black coating is used in the controlled oven thermal calibration.



Legend: Actual Temperature Thermal Cameral Observation

Fig. 4.4.1 Thermal emissivity calibration for FLIR SC500 thermal camera

It can be seen from the thermal calibration test that the thermal camera has a non-linear systematic error within the test range. When the test temperature is close to the room temperature, the thermal camera has very small systematic error. However, in the high temperature test, an average of 3°C temperature off can be found from the calibration test.

Based on thermal calibration test, the non-linear emissivity property of the Fuji 2SK3677-01MR Si MOSFET should always be considered during the T_j estimation and calibration. It is possible that at higher test temperature, a thermal camera will be more sensitive to object emissivity.

4.5 Summary of Experimental Test Setup

In this chapter, the experimental test setup for the gate drive output transient current based T_j sensing is discussed in detail. To implement the proposed T_j sensing method and calibrate its accuracy, special hardware setup is required for the system integration. Power semiconductor package, heat sink, and the chip surface emissivity are designed to calibrate the sensed T_j from the gate drive.

Chapter 5 The "Junction Temperature – Gate Current Transient" Relationship

In this chapter, the "junction temperature – gate current transient" (also refered to as "T_j – i_G") relationships for different types of switching power semiconductors are investigated.

The "T_j – i_G" relationship is essential to the online T_j sensing method proposed in this research. If the gate drive output current transient is not sensitive to the load current, then a 2-dimensional relationship (5.1.1) is enough with the two variables: junction temperature T_j, and gate current transient i_G. If the gate drive output currnet transient is sensitive to the load currnet, a 3-dimensional relationship (5.1.2) is required with three variables: junction temperature T_j, gate current transient i_G, and load current iload.

$$i_G = f(T_j) \tag{5.1.1}$$

$$i_G = f(T_j, i_{load}) \tag{5.1.2}$$

Based on (5.1.1) and (5.1.2), the expression for T_j can be derived as shown in (5.1.3) without load current effect, and (5.1.4) with load current effect.

$$T_j = h(i_G) \tag{5.1.3}$$

$$T_j = h(i_G, i_{load}) \tag{5.1.4}$$

The "T_j – i_G" relationship will be derived offline first and saved in the PWM controller as a lookup table. When the system is running online, the PWM controller will

read i_G and iload in real time and refer to (5.1.3) or (5.1.4) to calculate the real time T_j. To realize real time T_j estimation, a two-step procedure is summarized as following:

Step 1. Develop the "$T_j = h\ (i_G)$" relationship or the "$T_j = h\ (i_G, i_{load})$" relationship. Record this relationship in digital controller. This step needs to be done offline first.

Step 2. In real time, read the processed i_G from the gate drive and iload from the converter load. Map i_G and iload to T_j using the offline recorded "$T_j = h\ (i_G)$" relationship or the "$T_j = h\ (i_G, i_{load})$" relationship.

The setup of the "processed i_G from the gate drive" in step 2 will be discussed in chapter 6.

5.1 Manipulate Switching Power Semiconductor Junction Temperature

The switching power semiconductor T_j can be manipulated by controlling the device conduction loss. In the H-bridge inverter modeled in section 3.3, with fixed DC bus voltage and fixed switching frequency, the swiching duty ratio is used to control the device conduction loss, and ultimately manipulate T_j. Fig. 3.3.1 and Fig. 3.3.2 are reploted in Fig. 5.1.1 and Fig. 5.1.2 convenient viewing consideration.

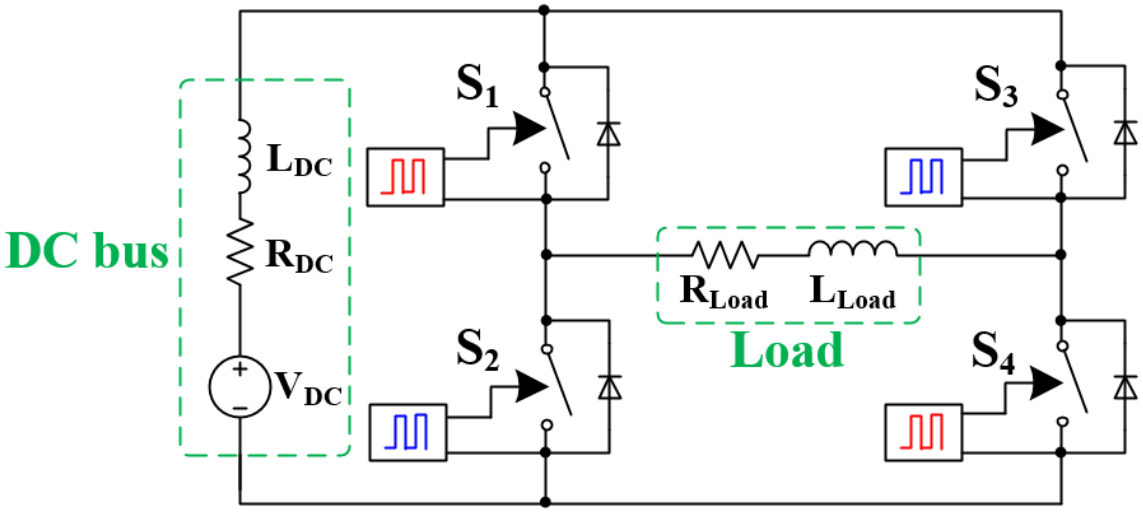


Fig. 5.1.1 Single phase H-bridge inverter modeling

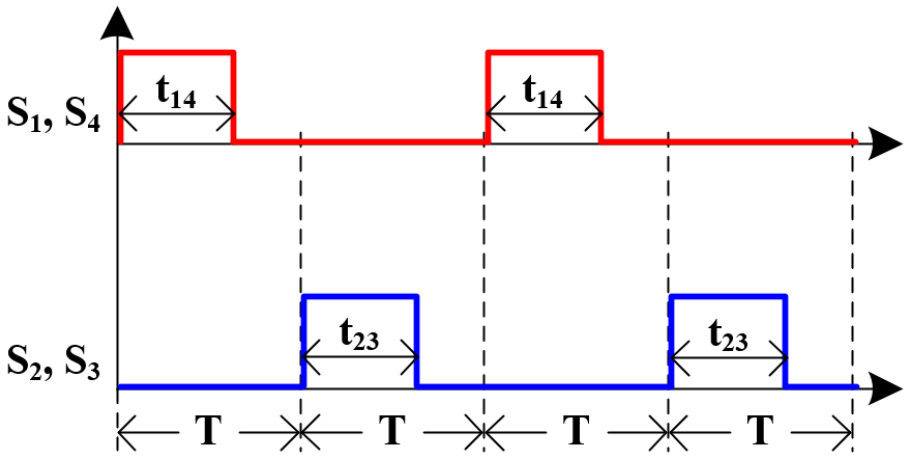


Fig. 5.1.2 Single phase H-bridge inverter switching timeline

The duty ratio (referred to as "D") of the inverter can be defined by (5.1.1) and (5.1.2), as shown in Fig. 5.1.2.

$$\text{For } S_1 \text{ and } S_4, \quad D_{14} = \frac{t_{14}}{T} \tag{5.1.1}$$

$$\text{For } S_2 \text{ and } S_3, \quad D_{23} = \frac{t_{23}}{T} \tag{5.1.2}$$

In this paper, D_{14} and D_{23} are set to the same value D, thus $D = D_{14} = D_{23}$.

5.2 The Si MOSFET "$T_j - i_G$" Relationship

This section investigates the "$T_j - i_G$" relationship for the Fuji 2SK3677-01MR Silicon MOSFET.

5.2.1 Simulation

Simulation parameters in this section are chosen to be close to the experimental parameters in section 5.2.2. The push-pull gate drive model shown in Fig. 5.2.1 and the H-bridge inverter model shown in Fig. 5.1.1 are used for simulation in LTSpice. The values of the inductances and resistances in Fig. 5.2.1 are shown in Table 5.2.1.

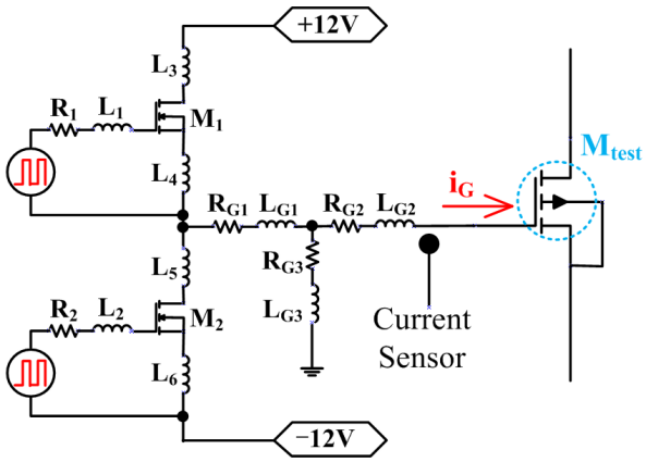


Fig. 5.2.1 Push-pull gate drive dynamic model for Fuji 2SK3677-01MR Silicon MOSFET

Table 5.2.1 Push-pull gate drive simulation parameters

Parameter	Value	Parameter	Value

R_1	0.05 [Ω]	R_{G2}	5 [Ω]
L_1	2 [nH]	R_{G3}	20 [kΩ]
V_{DC}	4 [nH]	L_{G1}	10 [nH]
L_4 (or L_6)	1.5 [nH]	L_{G2}	5 [nH]
R_{G1}	2 [Ω]	L_{G3}	5 [nH]

The values of the inductances and resistances in Fig. 5.1.1 used for this section are shown in Table 5.2.2. Vishay SI2318DS N-channel MOSFETs are selected for M_1 and M_2 in Fig. 5.2.1. LTSpice VDMOS model parameters for Vishay SI2318DS N-channel MOSFET are listed in Table 5.2.3. The Fuji 2SK3677-01MR MOSFET is selected as M_{test} in Fig. 5.2.1. The Spice level 3 NMOS model parameters for Fuji 2SK3677-01MR MOSFET are listed in Table 5.2.4. Note that Table 5.2.4 only lists key parameters used for simulation because of the page limit.

Table 5.2.2 Test circuit (H-bridge) simulation parameters

Parameter	Value	Parameter	Value
R_{load}	0.5 [Ω]	L_{load}	17 [nH]
R_{DC}	1 [Ω]	L_{DC}	17 [nH]
V_{DC}	10 [Ω]		

Table 5.2.3 Vishay SI2318DS N-channel MOSFET LTSpice VDMOS model simulation parameters

Parameter	Value	Parameter	Value
R_g	0.01 [Ω]	C_{gdmax}	45 [pF]
R_d	0.01 [Ω]	C_{gdmin}	40 [pF]
R_s	0.01 [Ω]	C_{gs}	500 [pF]
V_{to}	2.0 [V]	C_{jo}	30 [pF]
Lambda	0.02 [1/V]	I_s	10E-12 [A]
V_j	0.7 [V]	M	0.3
V_{ds}	40 [V]	N	1.19
R_{on}	0.05 [Ω]	TT	1E-9 [sec]
Q_g	9 [nC]	A	0.2

Table 5.2.4 Fuji 2SK3677-01MR MOSFET LTSPICE NMOS model key parameters used for the simulation

Parameter	Value	Parameter	Value
level	3	TOX	1E-7 [m]
L	4e-6	R_s	0 [Ω]
W	0.83	R_d	0 [Ω]
AD	2.49E-6	Kappa	10
PD	1.66 [W]	L_D	0.5E-6[H]
V_{max}	15E4[V]	C_{jsw}	23 [nF]
C_{gso}	2.6E-9[F/m]	V_{to}	3 [V]
TRD	0.00545	CAP	3.2E-9
C_j	7.7E-3 [F]	TLEV	1
R_{on}	0.71 [Ω]	TCV	0.00418

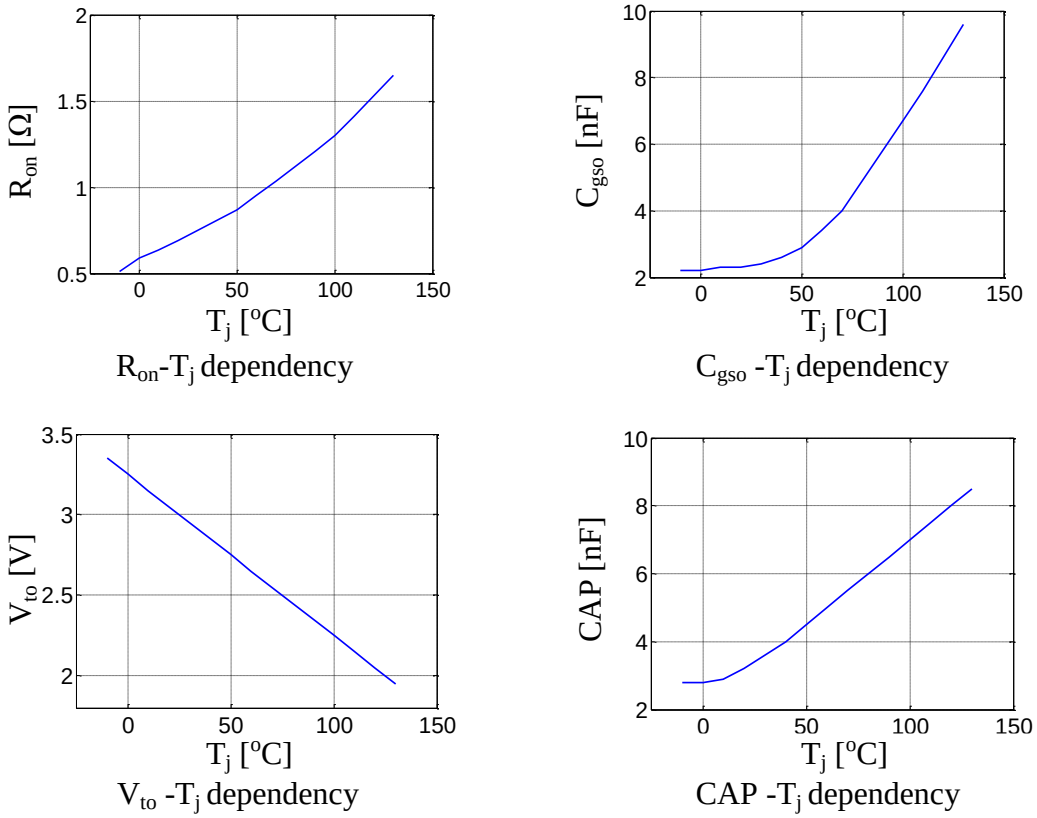


Fig. 5.2.3 Fuji 2SK3677-01MR MOSFET temperature sensitive parameters' Tj dependency

The power MOSFET intrinsic parameters "ON-state resistance"(R_{on}), "Gate-source overlap capacitance"(C_{gso}), "Zero-bias threshold voltage"(V_{to}) and "Gate potential capacitance"(CAP) dominate the MOSFET junction temperature dependency of the gate drive turn-on current waveform, i_G. The T_j dependency of these four parameters, shown in Fig. 5.2.2, can be found in the Fuji 2SK3677-01MR MOSFET datasheet and the technical statistics provided by Fuji Electric. The T_j dependent simulation can be expressed as (5.2.1), where **G** is the MOSFET dynamic model.

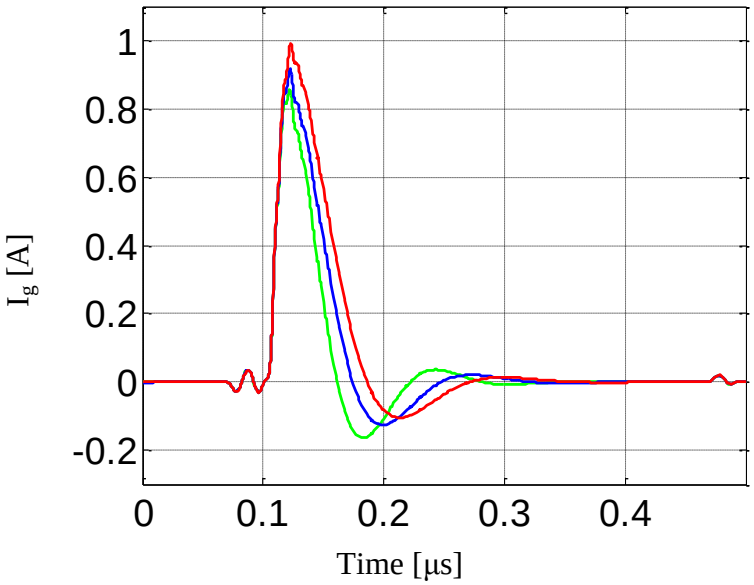


Fig. 5.2.3 Simulated gate drive turn-on current i_G transient waveform,

Fuji 2SK3677-01MR Si MOSFET

$$i_G = \mathbf{G}(R_{on}(T_j), C_{gso}(T_j), V_{to}(T_j), CAP(T_j)) \qquad (5.2.1)$$

Setting T_j to 38ºC, 59ºC and 82ºC, the system dynamic model is simulated for each temperature. The simulation result for gate drive turn-on current, i_G, is shown in Fig. 5.2.3. The comparison between simulation results and experimental results will be discussed in section 5.2.2.

5.2.2 Experimental Result

The gate drive turn-on output current based T_j sensing method for Si MOSFET is evaluated in a PCB based H-bridge inverter. All the simulation parameters were chosen to be close to the prototype test circuit parameters, which are included from Table 5.2.1 to Table 5.2.4. An ezdspf28335 development system is used to generate the PWM control signal for the MOSFET gate drive.

The prototype H-bridge inverter is tested under 20ºC ambient temperature. DC bus voltage, V_{DC}, is set to 40V. To turn on and turn off the test MOSFET, its gate-source voltage V_{GS} is pulled up to +12V and pulled down to −12V, respectively. By setting the test MOSFET duty ratio to 15%, 33%, and 50%, the maximum steady-state junction temperature was found to be 38 ºC, 59 ºC and 82 ºC, respectively, which keeps the un-encapsulated switches within safe operating conditions. The switching waveform of the test MOSFET (Fuji 2SK3677-0.MR) is shown in Fig. 5.2.4. The gate drive output current waveform is also included in Fig. 5.2.4. As a typical hard switching turn-on transient, V_{DS} starts falling as I_S starts rising.

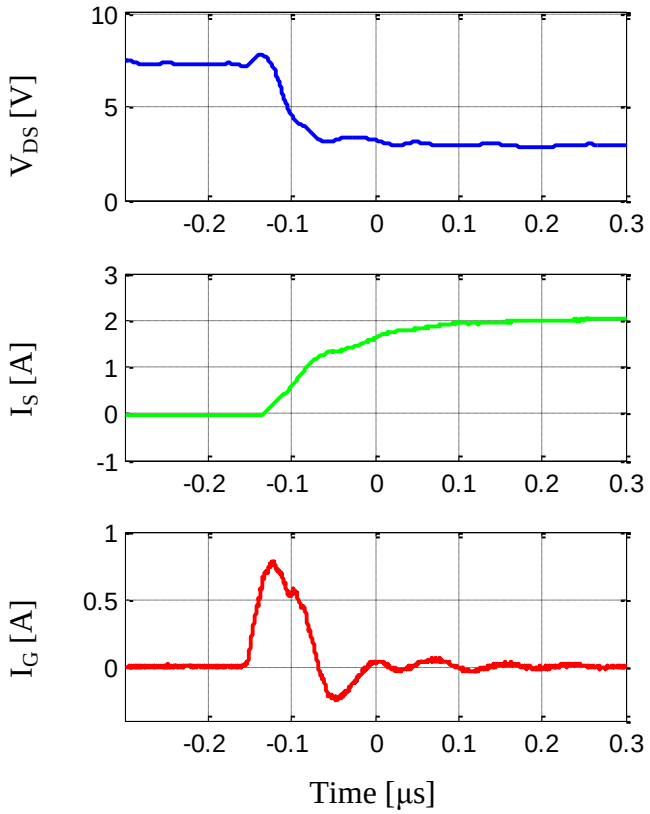
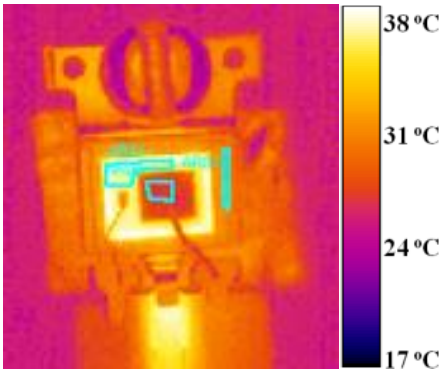
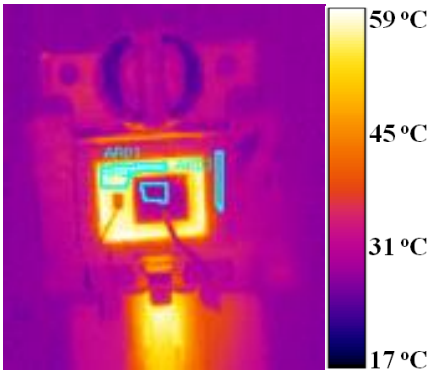


Fig. 5.2.4 Test MOSFET (Fuji 2SK3677-01MR) turn-on transient waveform

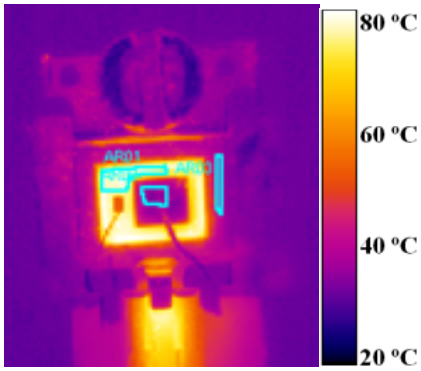
The junction temperature of the un-encapsulated Fuji 2SK3677-01MR power MOSFET (used as test MOSFET) is captured by an AGEMA SC500 thermal camera, as shown in Fig. 5.2.5. Statistics from the thermal camera captured data are listed in Table 5.2.5. Test MOSFET gate drive output current waveforms under the three test conditions are shown in Fig. 5.2.6. It can be seen that with higher MOSFET junction temperature, the amplitude of the gate drive turn-on current transient waveform is higher.



Duty ratio = 15%
Maximum T_j = 38 °C



Duty ratio = 33%
Maximum T_j = 59 °C



Duty ratio = 50%
Maximum T_j = 82 °C

Fig. 5.2.5 Thermal pictures for un-encapsulated Fuji 2SK3677-01MR power MOSFET captured at different test conditions

Table. 5.2.5 Thermal Statistics for Fuji 2SK3677-01MR under Three Different Testing Conditions

Test MOSFET duty ratio		Junction temperature	Substrate temperature
Duty ratio = 15%	Max.	38.1 °C	28.0 °C
	Avg.	37.0 °C	26.8 °C
Duty ratio = 33%	Max.	59.6 °C	32.7 °C
	Avg.	57.2 °C	30.3 °C
Duty ratio = 50%	Max.	82.8 °C	39.1 °C
	Avg.	79.4 °C	34.8 °C

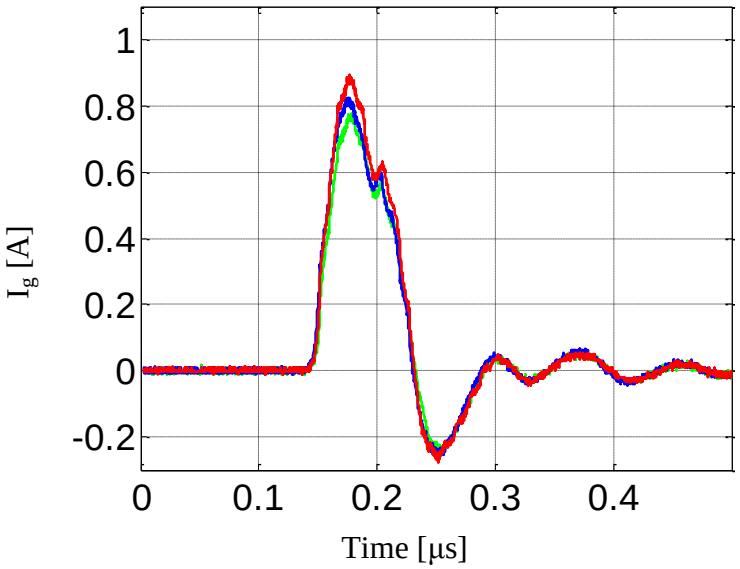


Fig. 5.2.6 Experimental tested gate drive turn-on current transient waveforms

The circuit T_j dependent characteristics can be understood from two perspectives: (I) the build-up of MOSFET common-source amplifying threshold ratio K_v, and (II) the charging of intrinsic capacitors C_{gso} and CAP.

Based on perspective (I), when the gate drive current reaches its peak, MOSFET is not fully turned on but is in the saturated region. Hence, it can be regarded as a common-source amplifier. Since R_{on} increases with junction temperature (Fig. 5.2.3), I_{ds} remains the same, while V_{ds} will increase with junction temperature (5.2.2). Under the same voltage bias, V_{to} will decrease with increasing junction temperature (Fig. 5.2.3), which indicates that V_{th} will also decrease with increasing junction temperature, since the

threshold voltage V_{th} is directly related to V_{to}. As a result, with higher junction temperature, the common-source amplifying threshold ratio K_v (5.2.3) will be larger. Thus, a larger gate charge Q_g will be required to build up larger K_v.

$$V_{ds} = R_{on} I_{ds} \tag{5.2.2}$$

$$K_v = V_{ds}/V_{th} \tag{5.2.3}$$

$$Q_g = \int I_g \, dt \tag{5.2.4}$$

5.3 The Si IGBT "$T_j - i_G$" Relationship

This section evaluates the "$T_j - i_G$" relationship of the Si IGBT in the Fuji 7MBR15SA140 IGBT module.

5.3.1 Simulation

Based on the prototype test setup (discussed in chapter 4), the circuit parameters are carefully estimated from the printed circuit board (PCB) layout. The two-stage push-pull gate drive model shown in Fig. 5.3.1 and the H-bridge inverter circuit model shown in Fig. 5.1.1 are used for the simulation in LTSpice.

Since the first stage of the push-pull gate drive does not have a significant effect on the "gate drive-IGBT" switching dynamics, the first stage (M_1 and M_2 in Fig. 5.3.1) is modeled as ideal switches in the simulation. In the push-pull gate drive second stage, Rohm Semiconductor RRR040P03TL P-channel MOSFET and RTR040N03TL N-channel MOSFET are selected for M_3 and M_4, respectively.

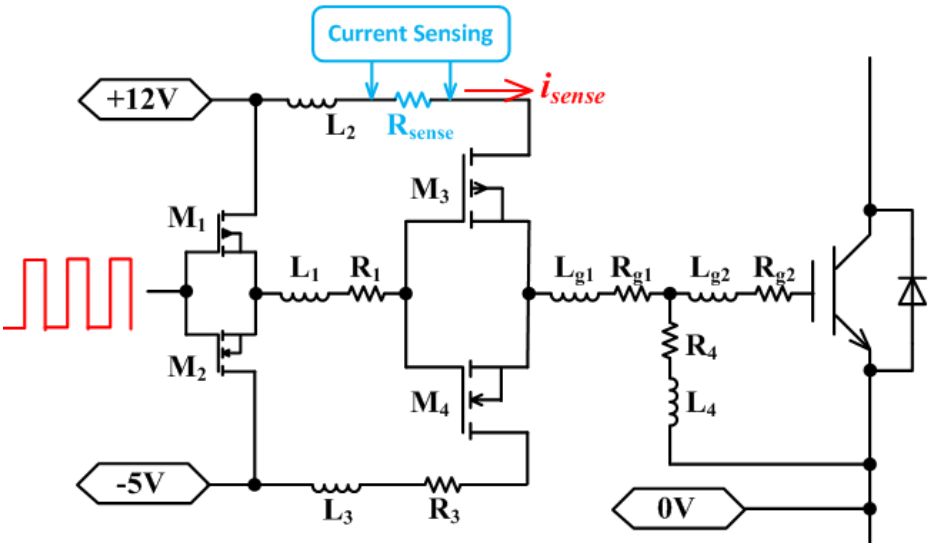


Fig. 5.3.1 Push-pull gate drive dynamic model for Fuji 7MBR15SA140 Si IGBT module

The Fuji 7MBR15SA140 IGBT module includes a three-phase diode rectifier and a three-phase IGBT inverter with anti-parallel diodes. In this research, the IGBT inverter is connected as a single phase H-bridge, and the diode rectifier is not used. A few IGBT intrinsic parameters are T_j sensitive. These parameters will change according to the change of T_j, and consequently the "gate drive-IGBT" switching dynamics will be changed. The IGBT "V_{CE}, I_c versus T_j" relationship from the IGBT datasheet is presented in Fig. 5.3.2. Some IGBT parameters (input capacitance C_{ies}, reverse transfer capacitance C_{res}, output capacitance C_{oes}, and dynamic gate charge Q_g) can be related to T_j based on the "V_{CE}-I_c versus T_j" relationship. The relationships of these parameters to V_{CE} are shown in Fig. 5.3.3 and Fig. 5.3.4.

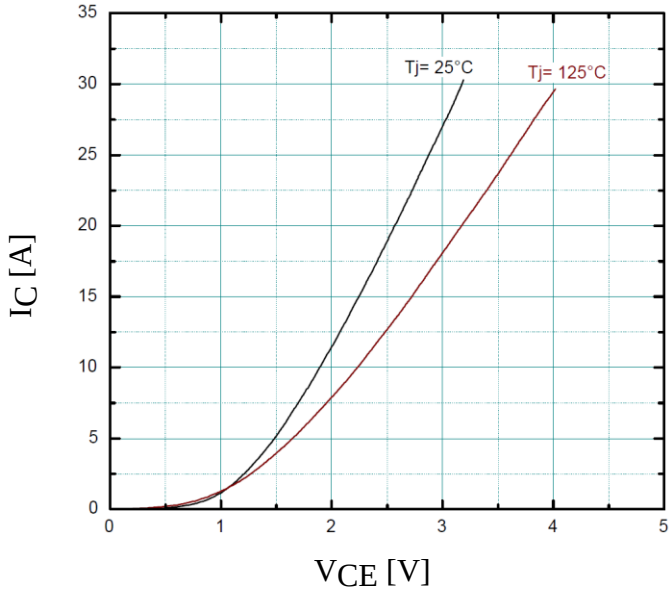


Fig. 5.3.2 The IGBT "V_{CE}, I_c versus T_j" relationship, 7MBR15SA140 IGBT module

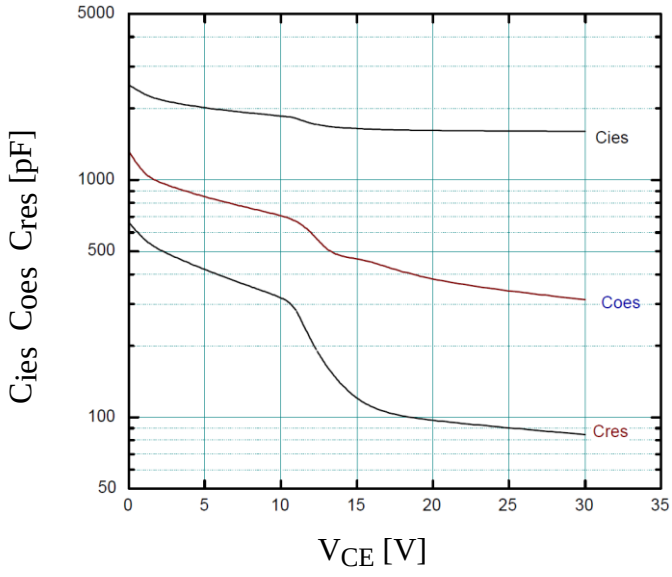


Fig. 5.3.3 The IGBT "intrinsic capacitance versus V_{CE}" relationship, 7MBR15SA140 IGBT module

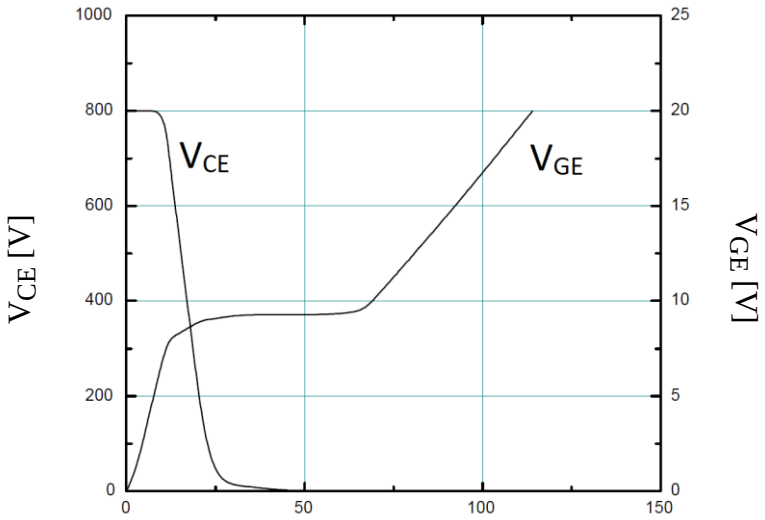


Fig. 5.3.4 The IGBT "Q_g versus V_{CE} and V_{GE}" relationship, 7MBR15SA140 IGBT module

The relationships depicted in Fig. 5.3.2, Fig. 5.3.3, and Fig. 5.3.4 are summarized in (5.3.1) to (5.3.5). If the V_{CE} in (5.3.2) to (5.3.4) are replaced by (5.3.1), (5.3.6) to (5.3.9) can be derived. The T_j dependent simulation can be expressed as (5.3.10), where i_{sense} represents the sensed gate drive turn-on current shown in Fig. 5, and **G** represents the whole IGBT dynamic model.

$$V_{CE} = V_{CE}\,(T_j\,,\, I_c) \tag{5.3.1}$$

$$C_{ies} = C_{ies}\,(V_{CE}) \tag{5.3.2}$$

$$C_{oes} = C_{oes}\,(V_{CE}) \tag{5.3.3}$$

$$C_{res} = C_{res}\,(V_{CE}) \tag{5.3.4}$$

$$Q_g = Q_g\,(V_{CE}\,,\, V_{GE}) \tag{5.3.5}$$

$$C_{ies} = C_{ies}\,(T_j\,,\,I_c) \qquad (5.3.6)$$

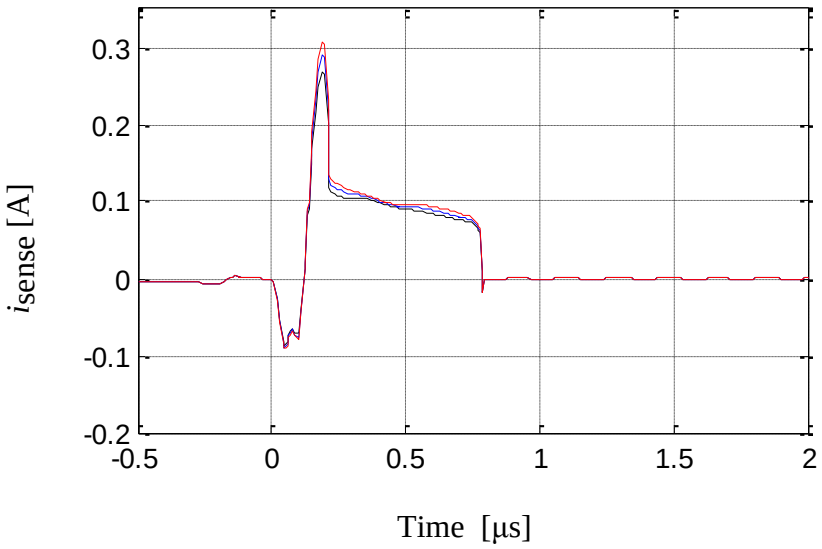
$$C_{oes} = C_{oes}\,(T_j\,,\,I_c) \qquad (5.3.7)$$

$$C_{res} = C_{res}\,(T_j\,,\,I_c) \qquad (5.3.8)$$

$$Q_g = Q_g\,(T_j\,,\,I_c) \qquad (5.3.9)$$

$$i_{sense} = \mathbf{G}\,(\,V_{CE}\,(T_j\,,\,I_c),\,C_{ies}\,(T_j\,,\,I_c),\,C_{oes}\,(T_j\,,\,I_c),\,C_{res}\,(T_j\,,\,I_c),\,Q_g\,(T_j\,,\,I_c)\,) \qquad (5.3.10)$$

The IGBTs are simulated with a Spice model provided by the IGBT manufacturer. Adjusting the values of the T_j dependent parameters in IGBT according to T_j (T_j is set to 33ºC, 59ºC, and 84ºC respectively in the simulation), the simulated gate drive turn-on current isense can be derived shown in Fig. 5.3.5.



Legend: T_j = 33ºC T_j = 59ºC T_j = 84ºC

Fig. 5.3.5 Simulated gate drive turn-on current i_G transient waveform, Si IGBT in Fuji 7MBR15SA140 Si IGBT module

5.3.2 Experimental Results

The H-bridge inverter shown in Fig. 5.1.1 is used for the proposed IGBT T_j sensing evaluation. The parameters used in simulation are estimated based on this prototype circuit test. A Texas Instrument TMS320F28335 DSP will be used to generate the PWM control signal for the H-bridge inverter. A Fuji 7MBR15SA140 IGBT module with an open package, without the stiffness gel (as shown in Fig. 4.2.2) is implemented in the H-bridge inverter. In the IGBT module, only four IGBTs are used, and their T_j will be monitored by a Flir thermal camera. The T_j of S3 will be used for analysis and estimation.

To improve the optical temperature sensing accuracy, it is important to make the device surface emissivity uniformly close to 1. This was accomplished by painting the IGBT open module with a low conductivity black coating. The circuit is tested at 23^{o}C ambient temperature. The DC bus voltage is set to 80V. The load of the H-bridge inverter is 10Ω. To switch the IGBT properly, V_{GE} is pulled up to +12V for turning on, and pulled down to -5V for turning off.

By setting the duty ratio D of the H-bridge inverter to 15%, 40%, and 65%, the maximum steady-state junction temperature of S_3 was found to be 33^{o}C, 59^{o}C, and 84^{o}C, respectively. The thermal images captured by Flir camera under the three tested values of D are shown in Fig. 5.3.6.

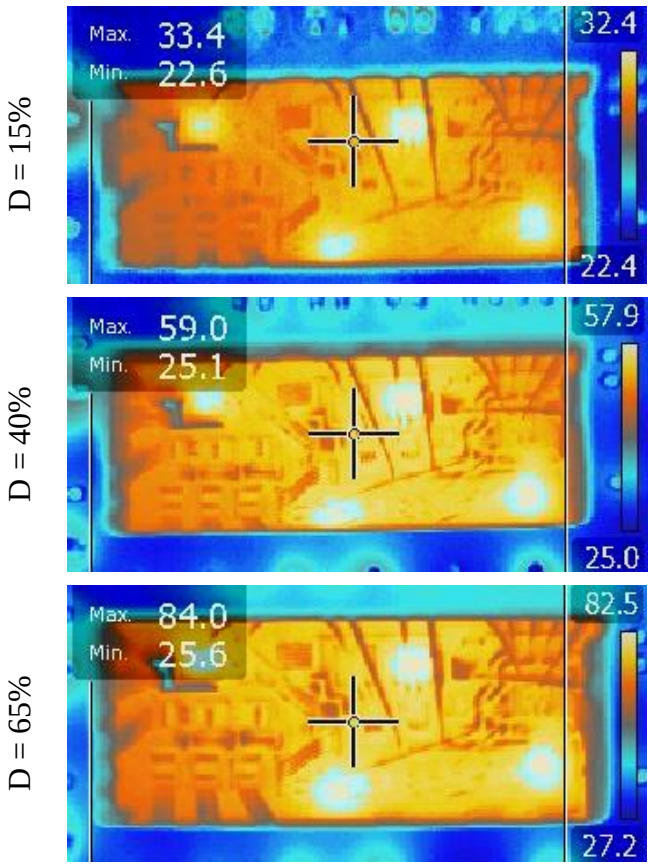
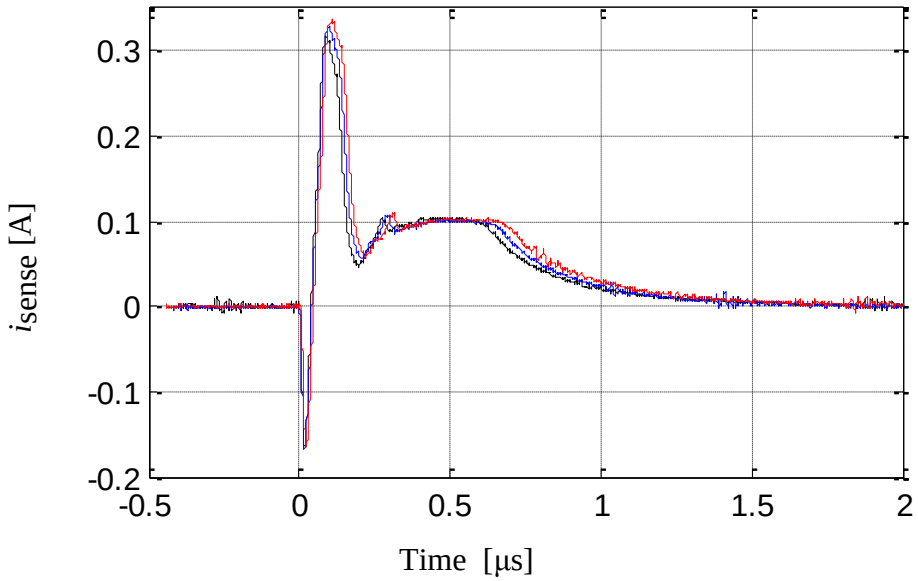


Fig. 5.3.6 Fuji 7MBR15SA140 IGBT module thermal images, varying D

The gate drive turn-on output current i_{sense} waveforms of S_3, are presented in Fig. 5.3.7. According to Fig. 5.3.7, with higher T_j, the IGBT gate drive turn-on output current will have higher pulse peak (the first positive pulse peak) and a longer tail.



Legend: T_j = 33ºC T_j = 59ºC T_j = 84ºC

Fig. 5.3.7 Tested Fuji IGBT gate drive turn-on current i_{sense} for S_3

The T_j dependency of the "gate drive-IGBT" turn-on dynamics can be explained via the T_j dependent IGBT transfer characteristics. IGBT transconductance, g_{fs}, is defined in (5.3.11) where I_c is the steady state collector current.

A large g_{fs} is desirable to obtain a high current handling capability with low gate drive voltage. The IGBT turn-on process builds up V_{CE}, (5.3.12). In (5.3.12), both g_{fs} and $V_{GE(th)}$ are T_j sensitive. This is basically because the carrier mobility will decrease with increasing temperature. With higher T_j, the current handling capability of IGBT is derated. Thus, the channel length and gate turn-on threshold voltage will be affected. As a result, more gate charge is required; V_{CE} will be larger; and the gate drive turn-on output dynamics will change.

$$g_{fs} = \frac{\mathrm{d}I_c}{\mathrm{d}V_{GE}} \tag{5.3.11}$$

$$\frac{\mathrm{d}V_{CE}}{\mathrm{d}t} = \frac{g_{fs}\, V_{GE(th)} + I_C}{g_{fs}\, R_G\, C_{GC}} \tag{5.3.12}$$

5.4 The SiC MOSFET "$T_j - i_G$" Relationship

This section studies the "$T_j - i_G$" relationship for the Rohm SCT2160KE SiC MOSFET.

5.4.1 Simulation

The simulation parameters are selected based on the prototype test setup discussed in chapter 4. The semiconductor models and parameters are based on the library and datasheet from the semiconductor manufacturer.

The Rohm SCT2160KE SiC MOSFET is used as a switching power semiconductor for the T_j sensing test in this section. The SiC MOSFETs are connected as a single phase H-bridge as shown in Fig. 5.1.1. Many device parameters of SCT2160KE are T_j dependent. The T_j dependencies of dominated parameters like threshold voltage V_{TH}, on-state resistance $R_{DS\text{-}on}$, are provided by the device manufacturer, as shown in Fig. 5.4.1 and Fig. 5.4.2. In the SPICE model provided by the device manufacturer as discussed in section 3.1.3, most of the switching properties and conducting properties are temperature characterized. In the simulation, the temperature parameter "T0" will be manipulated accordingly to characterize test results under different T_j.

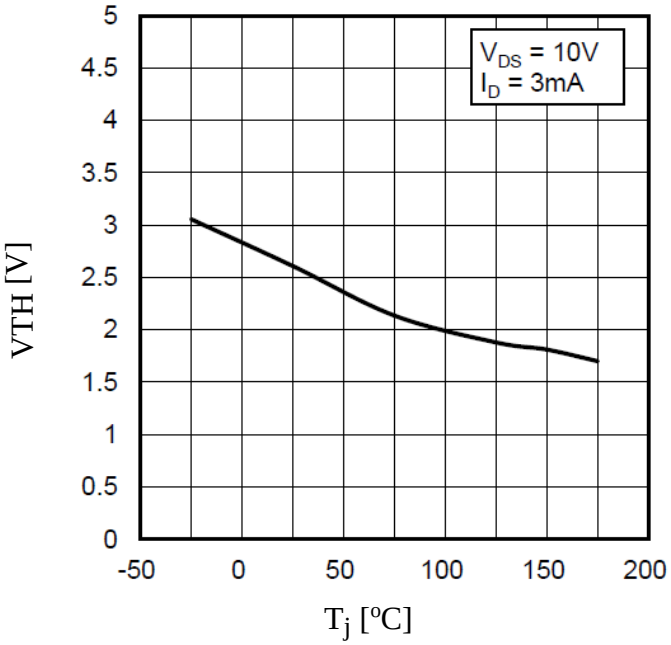


Fig. 5.4.1 Rohm SCT2160KE SiC MOSFET "V_{TH} vs. T_j" relationship

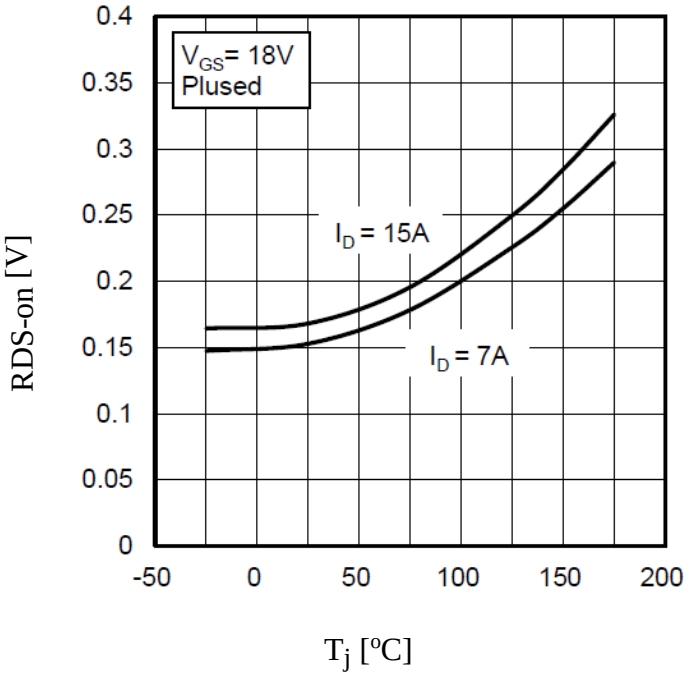


Fig. 5.4.2 Rohm SCT2160KE SiC MOSFET "V_{TH} vs. $R_{DS\text{-}on}$" relationship

The push-pull output based voltage source gate drive is based on the circuit dynamic model as shown in Fig. 5.4.3. Rohm Semiconductor RRR040P03TL P-channel MOSFET and RTR040N03TL N-channel MOSFET are selected for M1 and M2 in Fig. 5.4.3 respectively.

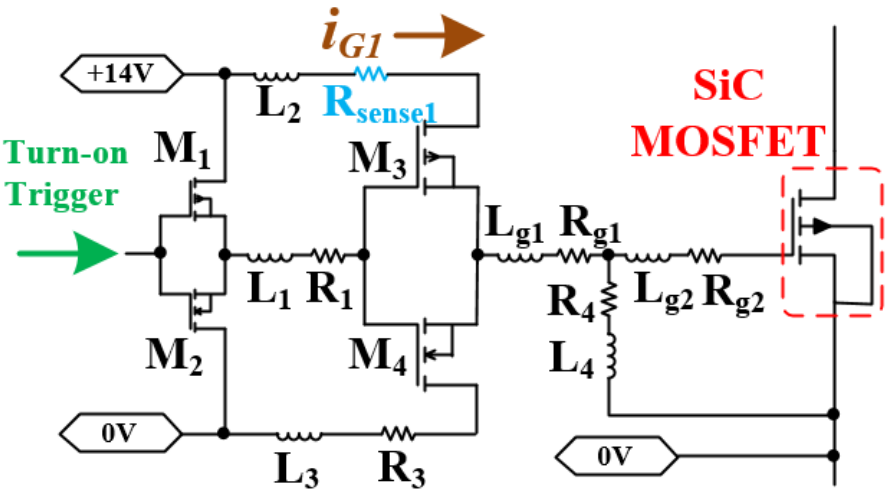
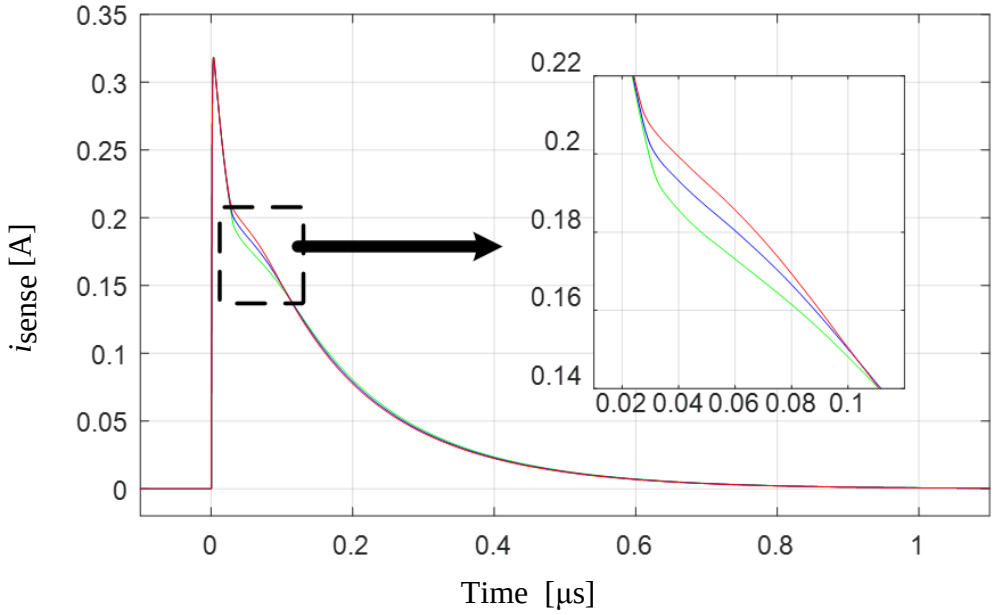


Fig. 5.4.3 Push-pull gate drive dynamic model for Rohm SCT2160KE SiC MOSFET

Setting T_j to 31°C, 67°C and 105°C, the system dynamic model is simulated for each temperature. The simulation result for the gate drive turn-on current, i_G, is shown in Fig. 5.4.4.



Legend: T_j = 31°C T_j = 67°C T_j = 105°C

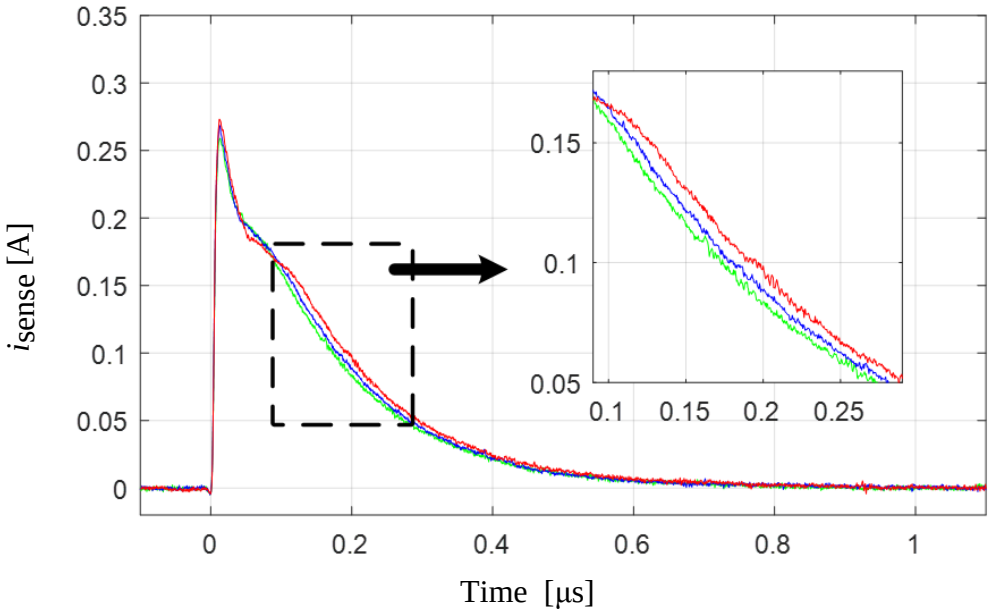
Fig. 5.4.4 Simulated sensed gate drive turn-on output current i_G transient for Rohm SCT2160KE SiC MOSFET

5.4.2 Experimental Results

Four Rohm SCT2160KE SiC MOSFETs are implemented to an H-bridge for the proposed SiC MOSFET T_j sensing experimental evaluation. The value of the parasitics used in simulation are estimated based on the prototype test setup discussed in this section.

Rohm SCT2160KE SiC MOSFETs are chemically de-capsulated so that the properties and structure of device leads, wire bonds, and semiconductor chips remain the same (as shown in Fig. 4.2.5). T_j of the de-capsulated device is calibrated by a Flir thermal camera. To make the surface emissivity close to 1, the de-capsulated device is painted with a low conductivity black coating.

By setting the H-bridge inverter duty ratio D to 15%, 40%, and 65%, the maximum steady-state T_j of Rohm SCT2160KE SiC MOSFETs are found to be 31°C, 67°C, and 105°C, respectively. The experimentally tested gate drive turn-on current isense1 waveforms (under different D) are shown in Fig. 5.4.5.



Legend: T_j = 31°C T_j = 67°C T_j = 105°C

Fig. 5.4.5 Experimentally sensed gate drive turn-on output current i_G transient for Rohm SCT2160KE SiC MOSFET

It can be observed from the experimentally tested waveforms (Fig. 13 and Fig. 15) that i_G changes according to T_j. The turn-on gate charge (referred to as "Q_g") has a positive temperature coefficient. To further investigate the reason of the positive "Q_g – T_j" coefficient, several device temperature dependencies need to be considered.

The SiC MOSFET turn-on gate charge is the result of generating the on-state conducting channel (gate energy injection). The turn-on gate charge is a function of

carrier mobility (M_c), carrier density (n_c), and bandgap energy (E_g) [59], as shown in (5.4.1).

$$Q_g = G(M_c , n_c , E_g) \tag{5.4.1}$$

The semiconductor channel carrier mobility (M_c) has a negative T_j coefficient [60], as shown in (5.4.2), where α is a positive temperature dependent constant.

$$M_c(T_j) = M_c(T_0) \left(\frac{T_j}{T_0}\right)^{-\alpha} \tag{5.4.2}$$

The semiconductor channel carrier density (n_c) has a positive T_j coefficient, as stated in (2) in [61]. However, if the T_j dependency of M_c is characterized, n_c can be considered as a constant then.

The bandgap energy (E_g) of SiC has negative T_j coefficient, as shown in (5.4.3), where $E_g(0)$ is the bandgap energy at absolute zero on the Kelvin scale in the given material, and α_E and β_E are material specific constants [62].

$$E_g(T_j) = E_g(0) - \frac{\alpha_E T_j^2}{T_j + \beta_E} \tag{5.4.3}$$

With higher T_j, lower M_c tend to increase Q_g (in order to build the channel under the same current rating), while the smaller E_g tend to decrease Q_g (because V_{TH} and C_{GS} are lower according to smaller E_g). However, the E_g of most of the semiconductor devices will not be significantly changed if they are operated below the maximum allowed temperature. Note that the maximum allowed temperature is usually limited by device packages. Thus, the temperature dependency of M_c will dominate the temperature dependency of Q_g. As a result, larger Q_g is observed under higher T_j.

5.5 The GaN HEMT "$T_j - i_G$" Relationship

This section studies the "$T_j - i_G$" relationship for the EPC2030 GaN HEMTs.

5.5.1 Simulation

The simulation parameters are selected based on the prototype test setup discussed in chapter 4. The semiconductor models and parameters are based on the library and datasheet from the semiconductor manufacturer.

The EPC2030 GaN HEMTs are used as switching power semiconductor for the T_j sensing test in this section. The GaN HEMT is connected by a single phase half-bridge. Many device parameters of EPC2030 are T_j dependent. The T_j dependencies of dominated parameters like threshold voltage V_{TH}, on-state resistance $R_{DS\text{-}on}$, are provided by the device manufacturer, as shown in Fig. 5.5.1 and Fig. 5.5.2. In the SPICE model provided by the device manufacturer as discussed in section 3.1.3, most of the switching properties and conducting properties are temperature characterized.

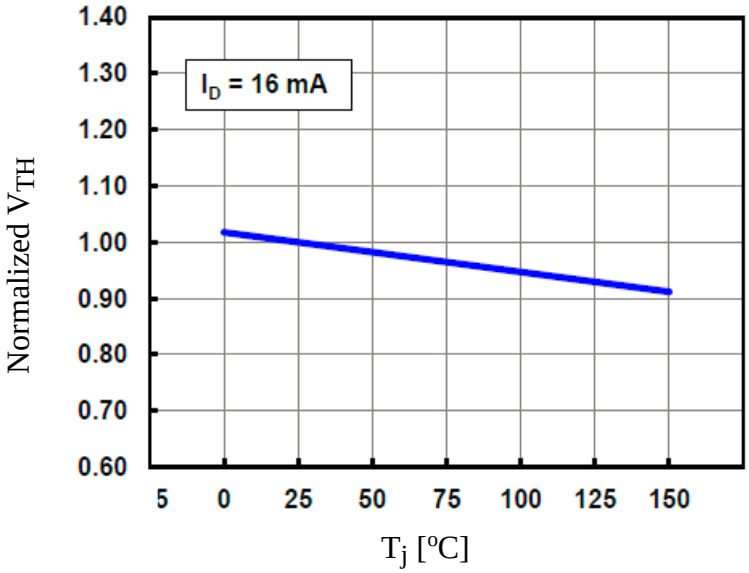


Fig. 5.5.1 EPC2030 GaN HEMTs "V_{TH} vs. T_j" relationship

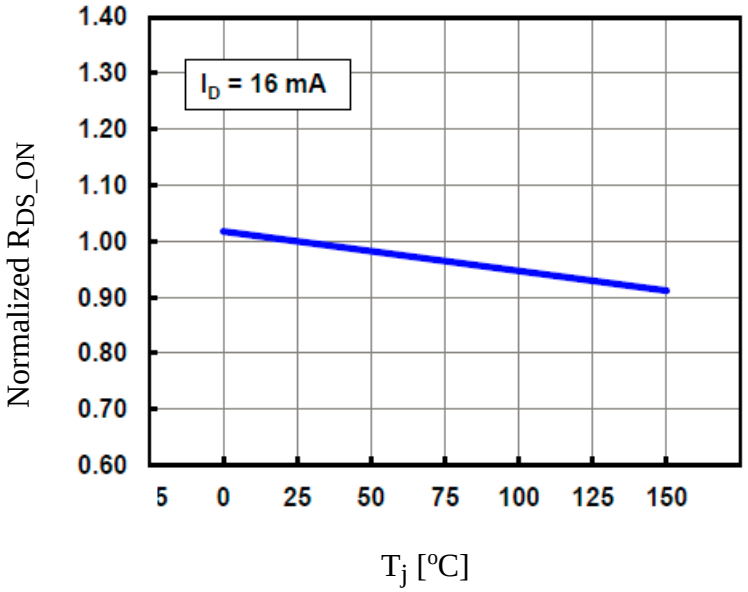


Fig. 5.5.2 EPC2030 GaN HEMTs "V_{TH} vs. $R_{DS\text{-}on}$" relationship

The push-pull output based voltage source gate drive is based on the circuit dynamic model as shown in Fig. 5.5.3. Texas Instrument LM5114 is used to drive the GaN HEMTs.

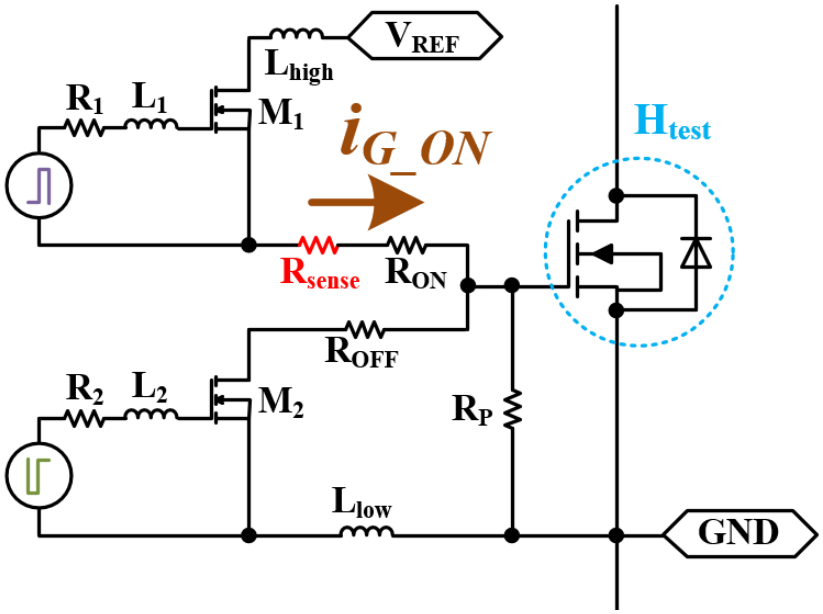
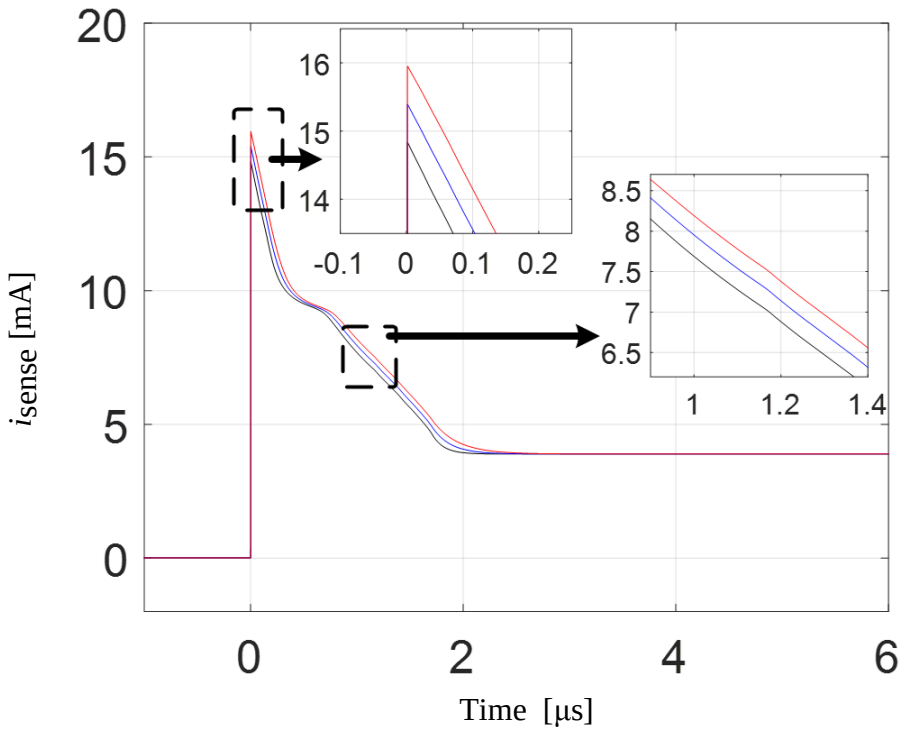


Fig. 5.5.3 Push-pull gate drive dynamic model for LM5114 and EPC2030

Setting T_j to 31°C, 41°C and 51°C, the system dynamic model is simulated for each temperature. The simulation result for the gate drive turn-on current, i_G, is shown in Fig. 5.5.4.



Legend: T_j = 31°C T_j = 41°C T_j = 51°C

Fig. 5.5.4 Simulated sensed gate drive turn-on output current i_G transient for EPC2030 GaN HEMT

5.5.2 Experimental Results

Two EPC2030 GaN HEMTs are implemented to a half-bridge for the proposed GaN HEMT T_j sensing experimental evaluation. The value of the parasitics used in simulation are estimated based on the prototype test setup discussed in this section.

By setting the half-bridge inverter duty ratio D to 8%, 23%, and 38%, the maximum steady-state T_j of EPC2030 GaN HEMTs are found to be 31°C, 41°C, and 51°C, respectively. The experimentally tested gate drive turn-on current i_{sense} waveforms (under different D) are shown in Fig. 5.5.6.

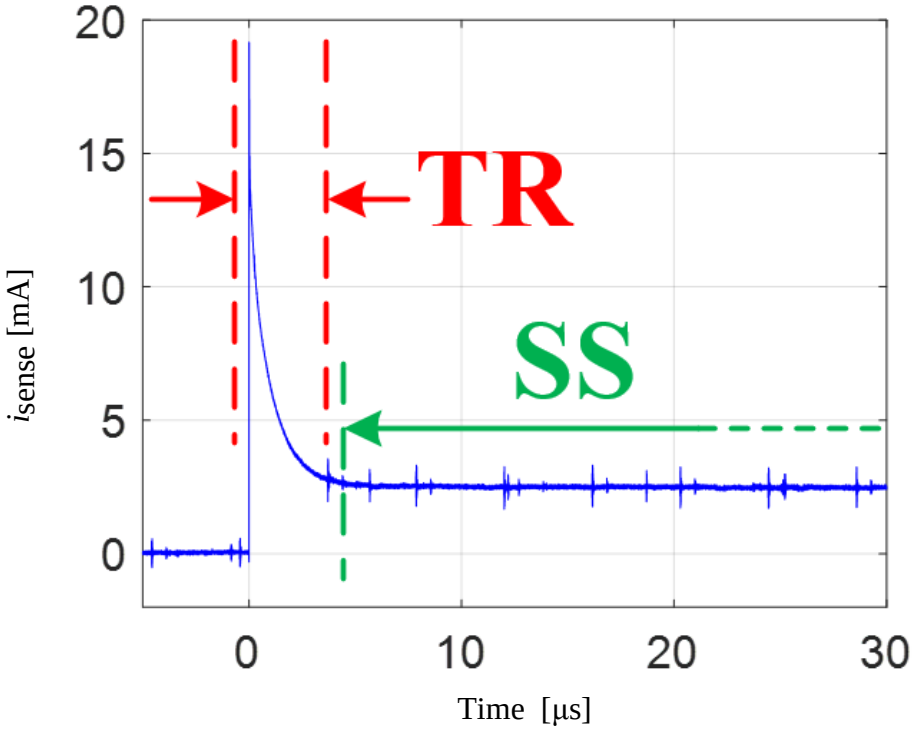
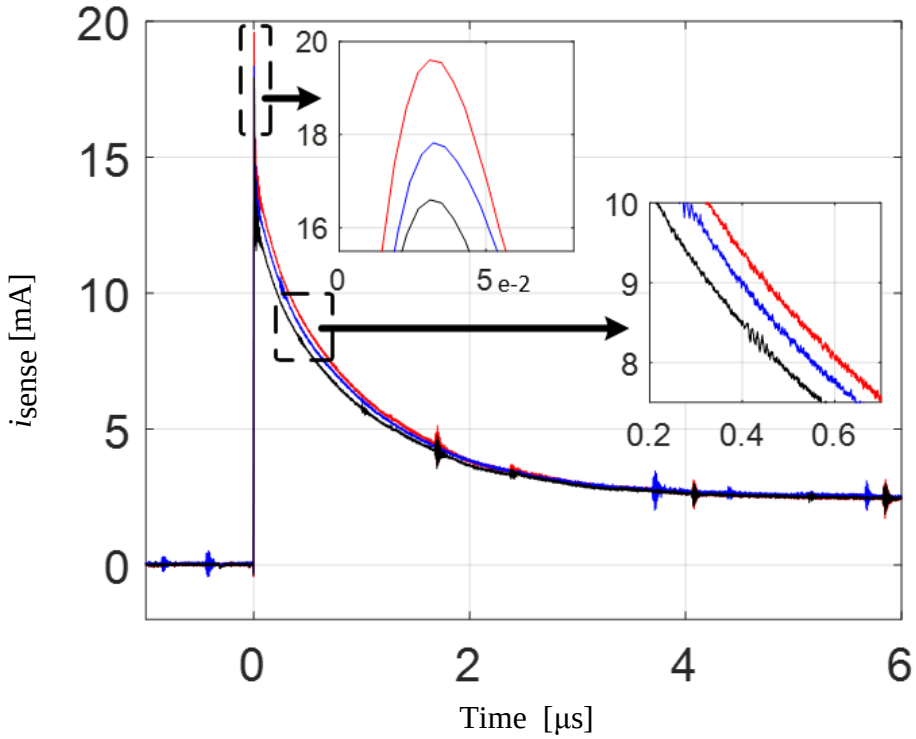


Fig. 5.5.5 Experimentally sensed gate drive turn-on output current i_G transient for EPC2030 GaN HEMT, overview



Legend: T_j = 31°C T_j = 41°C T_j = 51°C

Fig. 5.5.6 Experimentally sensed gate drive turn-on output current i_G transient for EPC2030 GaN HEMT

The gate drive turn-on current, i_{G_ON}, is calculated by measuring the voltage drop across R_{sense}. An overview waveform of i_{G_ON} is shown in Fig. 5.5.5, where the first part of the waveform, "TR", is the GaN HEMT turn-on transient gate current, and the second transient "SS" is the steady state gate drive output current bypassed by R_p. A zoom-in plot for "TR" under different T_j (31°C, 41°C, and 51°C) is shown in Fig. 5.5.6. According to the simulation (Fig. 5.5.4) and experimental results (Fig. 5.5.6), the GaN HEMT turn-on transient gate current is sensitive to T_j. With fixed DC bus voltage, higher T_j will result in larger gate charge (Q_G). Specifically, in the experimental results, the peak value of i_{G_ON} is positively correlated to T_j. Thus, a peak detection method is feasible for the

online extraction of T_j.

The difference between the simulation and the experimental result of i_{G_ON} can be found by comparing Fig. 5.5.4 and Fig. 5.5.6. In the experimentally measured waveform (Fig. 5.5.6), the width of the i_{G_ON} peak is short and only one falling transient can be observed. However, in the simulation waveform, the width of the i_{G_ON} peak is relatively big and two falling transients are observed. The gate current is the bias current from the gate Schottky barrier. The simulation model characterizes this property with two equivalent Schottky barriers (one is between the gate and source, the other is between the gate and drain). The two barriers do not switch their bias state simultaneously during the turn-on transient in simulation. As a result, two transients can be observed in the simulated i_{G_ON} waveform. However, in a real device, the Schottky barrier is distributed between the metal-semiconductor contact of the device gate and the AlGaN layer [64]. The entire area of the metal-semiconductor contact will gradually switch its bias state during the turn-on transient. Thus, the transients of the two equivalent Schottky barriers are merged together, and only one falling transient is observed in the experimentally measured i_{G_ON} waveform.

The T_j dependency of the GaN HEMT gate switching properties has been investigated in [63] [65] [66]. Descriptions for the related symbols are summarized in Table 5.5.1.

TABLE 5.5.1. LIST OF SYMBLS

symbol	***Description***
n	Charge density

D	Density of states
V_T	Thermal voltage
E_f	Position of Fermi level
E_0	Position of the first energy level
E_1	Position of the second energy level
V_g	Gate potential (gate voltage)
V	Local quasi-Fermi potential
q	Electron charge
d	Layer thickness
γ_0	Parameters determined from experiment
ε	Material permittivity
W	Channel width
L	Channel length
n_D	Drain charge carrier density
n_S	Source charge carrier density

In the GaN HEMT structure, the charge density accumulated in the potential well can be calculated by (5.5.1).

$$n = DV_T\left[\ln\left(e^{(E_f - E_0)/V_H} + 1\right) + \ln\left(e^{(E_f - E_1)/V_H} + 1\right)\right] \tag{5.5.1}$$

A simple charge control dynamic model can be derived from (5.1), as shown in (5.5.2). This model is valid in all operation regions. It effectively relates the applied voltage and the charge carrier concentration.

$$V_{g0} - V = \frac{qdn}{\varepsilon} + \gamma_0 n^{2/3} + V_T \ln\left(\frac{n}{DV_T}\right) \tag{5.5.2}$$

The gate charge can be calculated by integrating the charge density along the channel over the gate area, as described in (5.5.3).

$$Q_G = W \int_0^L qn(x)\, dx \tag{5.5.3}$$

By substituting (5.5.1) and (5.5.2) into (5.5.3), and simplifying the expression, the gate charge can be calculated with (5.5.4).

$$Q_G = W\,L\,q\frac{\frac{qd}{3\varepsilon}(n_D{}^3 - n_S{}^3) + \frac{1}{4}\gamma_0(n_D{}^{8/3} - n_S{}^{8/3}) + \frac{1}{2}V_T(n_D{}^2 - n_S{}^2)}{\frac{qd}{2\varepsilon}(n_D{}^2 - n_S{}^2) + \frac{2}{5}\gamma_0(n_D{}^{5/3} - n_S{}^{5/3}) + V_T(n_D - n_S)} \tag{5.5.4}$$

In (5.5.4), V_T, n_D, and n_S are T_j sensitive. As a result, the gate charge value of the device is a function of T_j. In this research, the gate charge can be regarded as the integration of the transient gate current waveform "TR" in Fig. 14. Thus, the "$i_{G\_ON} - T_j$" relationship can be explained as the T_j dependencies of V_T, n_D, and n_S.

In validation, n_D and n_S can be experimentally measured, and V_{TH} can be calculated by (5.5.5).

$$V_T = \frac{kT}{q} \tag{5.5.5}$$

5.6 The "i_G - T_j" relationship for Si MOSFET, Si IGBT, SiC MOSFET, and GaN HEMT

In this section, the extracted T_j information for Si MOSFET, Si IGBT, SiC MOSFET, and GaN HEMT will be provided. The processed i_G signal is derived by the integration or the peak detection of the measured waveform, while T_j is derived by the Flir thermal camera at the same time.

In the case of Fuji 2SK3677 Si MOSFET driven by the push-pull gate drive shown in Fig. 5.2.1, the "i_G peak – T_j" relationship derived by peak detection is shown in Fig. 5.6.1. It can be seen that the i_G peak is positively correlated with T_j.

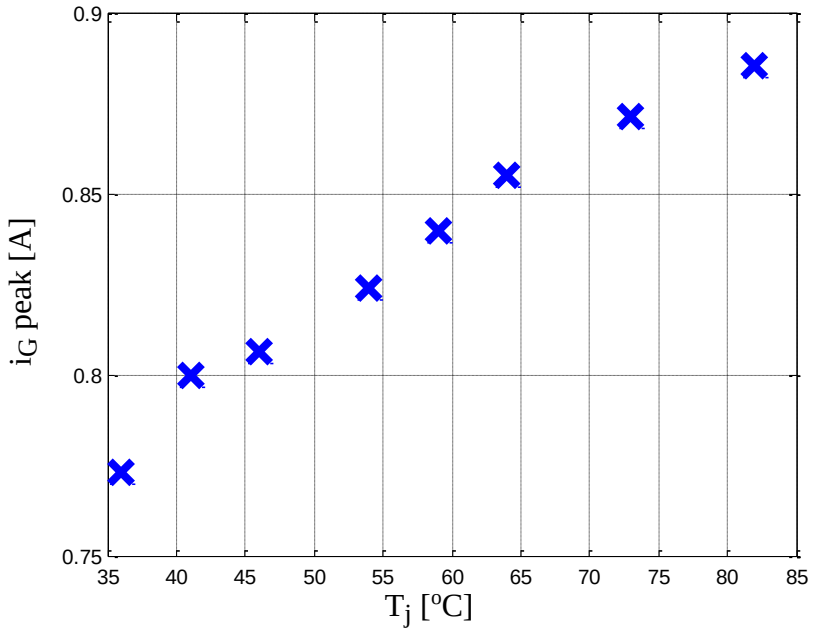


Fig. 5.6.1 The "i_G peak – T_j" correlation between, Fuji 2SK3677 Si MOSFET driven by push-pull gate drive

In the case of Fuji 7MBR15SA140 IGBT module driven by the push-pull gate drive shown in Fig. 5.3.1, the "$\int i_G$ – T_j" relationship derived by the integrator is shown in Fig. 5.6.2. It can be seen that the $\int i_G$ is positively correlated with T_j.

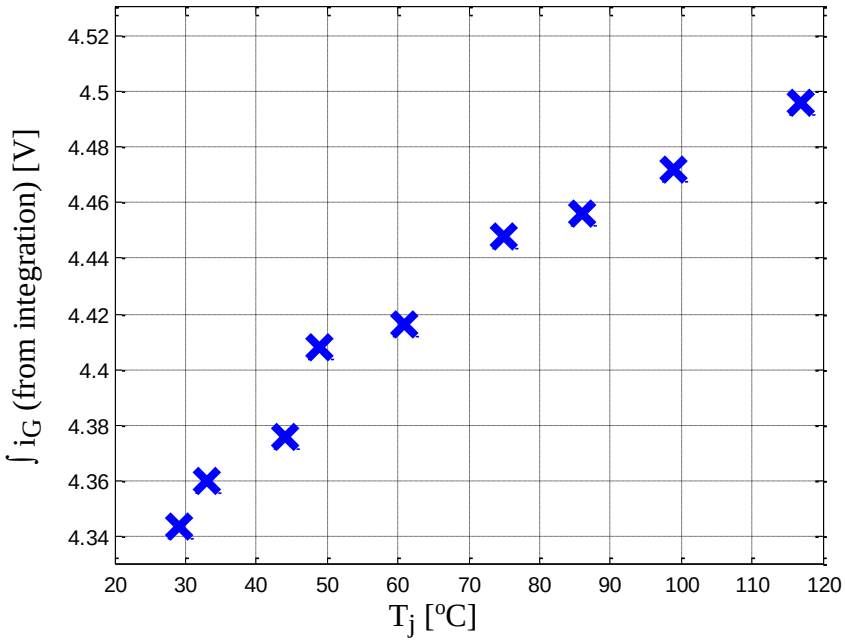


Fig. 5.6.2 The "$\int i_G - T_j$" correlation between, Fuji 7MBR15SA140 IGBT module driven by push-pull gate drive

In the case of Rohm SCT2160KE SiC MOSFET driven by the push-pull gate drive shown in Fig. 5.4.3, the "i_G peak – T_j" relationship derived by integration is shown in Fig. 5.6.3. It can be seen that the $\int i_G$ is positively correlated with T_j.

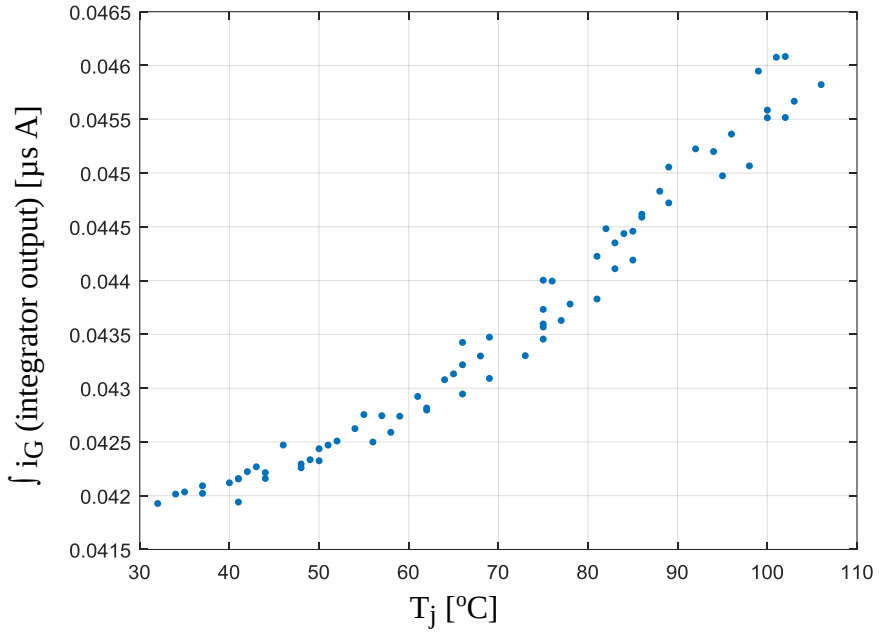


Fig. 5.6.3 The "$\int i_G$ –T_j" correlation, Rohm SCT2160KE SiC MOSFET driven by push-pull gate drive

In the case of EPC2030 GaN HEMT driven by the push-pull gate drive shown in Fig. 5.6.4, the "i_G peak – T_j" relationship derived by peak detection is shown in Fig. 5.6.3. It can be seen that the i_G peak is positively correlated with T_j.

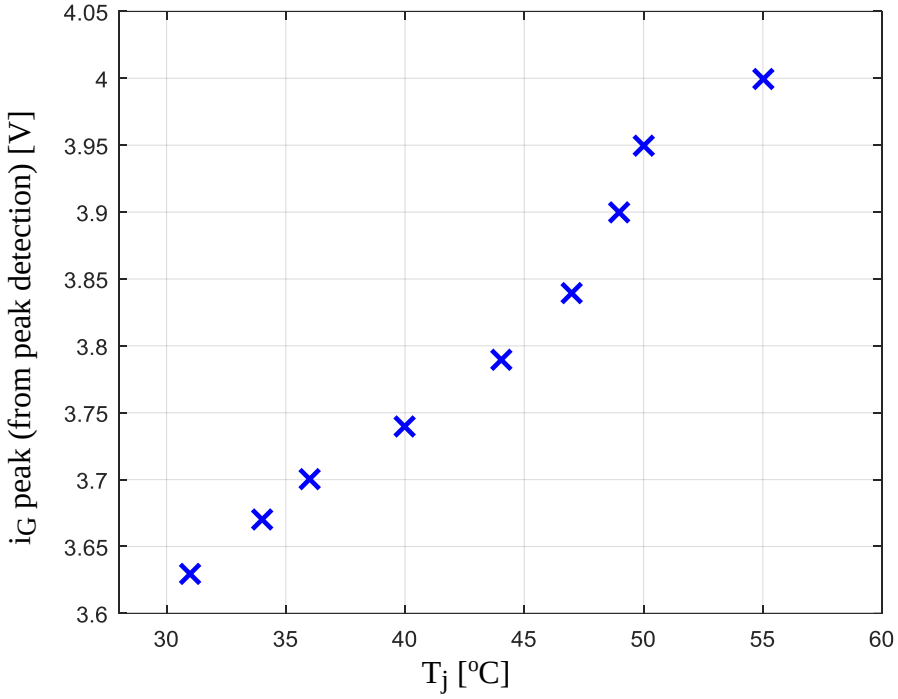


Fig. 5.6.3 The "i_G peak – T_j" correlation, EPC2030 GaN HEMT driven by push-pull gate drive

5.7 Summary of the "Junction Temperature – Gate Current Transient" Relationship

This chapter investigates the "T_j – i_G" relationship for Si MOFSET, Si IGBT, and SiC MOSFET. Simulated gate drive output current transients under different T_j are compared with experimental results. The thermal images for the switching power semiconductor chip surface are used for T_j calibration.

The background for the "T_j – i_G" dependency is studied. The semiconductor carrier mobility and channel length modulation are used to characterize the switching power semiconductor switching transient temperature dependencies.

Chapter 6 Extracting the Junction Temperature Online

In this thesis, the "T_j – i_G" dependency of different types of switching power semiconductors are identified and analyzed. Extracting the T_j information online and sending the extracted signal to the PWM controller requires high bandwidth online signal processing for the sensed i_G signal.

The high bandwidth analog to digital conversion (ADC) is one option to extract the T_j information from the sensed i_G signal. Commercially available ADC can have up to 10GHz sampling rate. Under several gigahertz's sampling rate, the whole i_G waveform can be converted to digital signal and sent to the controller for T_j dependency analysis. However, the communication between the ADC and the controller can be limited by the controller's data receiving rate, and the analysis for the whole i_G waveform will require a tremendous computation amount. Considering that using high sampling rate ADC to process the whole i_G waveform can challenge the controller communication and computation, this method is not recommended for online processing of the sensed i_G signal.

Another option to extract the T_j information from the sensed i_G wavefrom is to locally process the waveform on the gate drive. If the T_j information in the sensed i_G can be converted to one analog voltage level, it can be read by the controller easily. Note that

reading one voltage level is much simpler compared with reading the whole i_G waveform processed by ADC.

Based on the experimental i_G waveforms as shown in chapter 5, some charactersitics of the waveforms are explicitly T_j sensitive. For instance, the peak value of Si MOSFET's i_G as shown in Fig. 5.2.6 can be quickly correlated to T_j, and the integration of Si IGBT's i_G as shown in Fig. 5.3.7 can be conveniently mapped to T_j. Accordingly, peak detection method and integration method can be implemented to the sensed i_G waveform to extract the switching power semiconductor T_j information.

6.1 Peak Detection Method

High bandwidth peak detection has tremendous demands on the performance of amplifiers. High slew rate is required to keep the amplifier internal nodes from over-racing the output stage. As a result, it can cause long-term overload, or DC un-balanced errors. To support the high slew rate on the output side, the amplifier must deliver large currents into the capacitive load of the detector. Coumpounding these problems are issues of amplifier instability with a large capacitive load, as well as the accuracy of the output voltage.

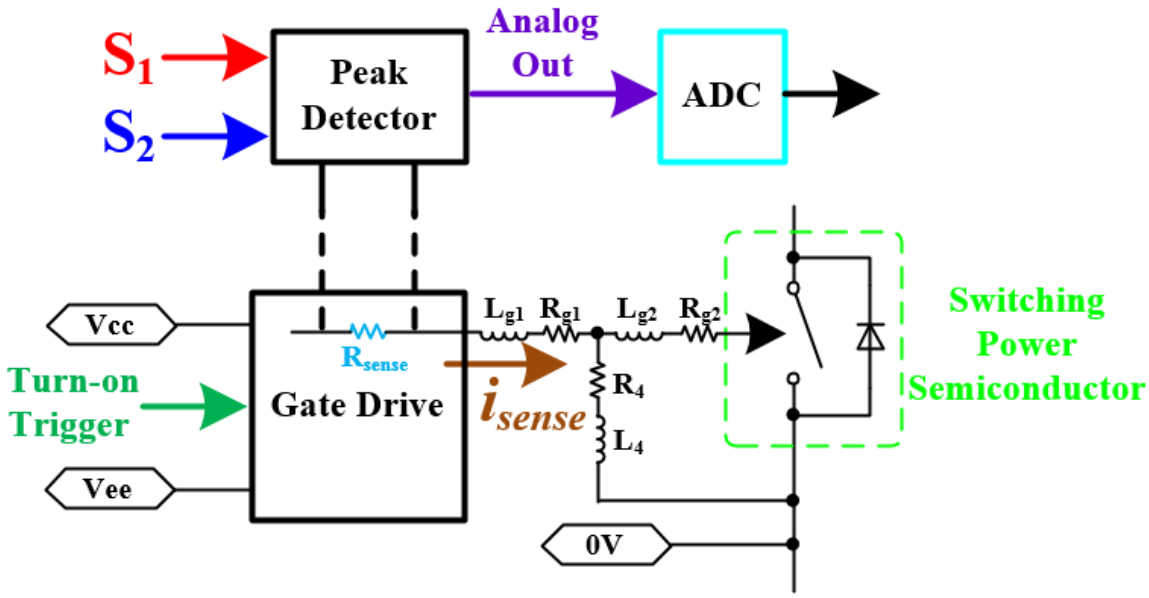


Fig. 6.1.1 Applying peak detector to the sensed gate drive turn-on output current transient

In this research, the gate drive turn-on output current transient i_G should be considered as a current pulse with a duration between 10ns and 1000ns. In the case of Si MOSFET driven by push-pull gate drive (Fig. 5.2.6) and the case of SiC MOSFET driven by push-pull gate drive (Fig. 5.4.5), the i_G peak is explicitly T_j sensitive. Thus, the peak detection method applied to the i_G of the aforementioned cases can feasibly extract the T_j information from the i_G waveforms. The peak detector applied to the sensed i_G (also refered to as isense), is shown in Fig. 6.1.1, where S_1 and S_2 are used to activate the peak detector and reset the peak detector. The time table for the peak detector circuit is shown in Fig. 6.1.2.

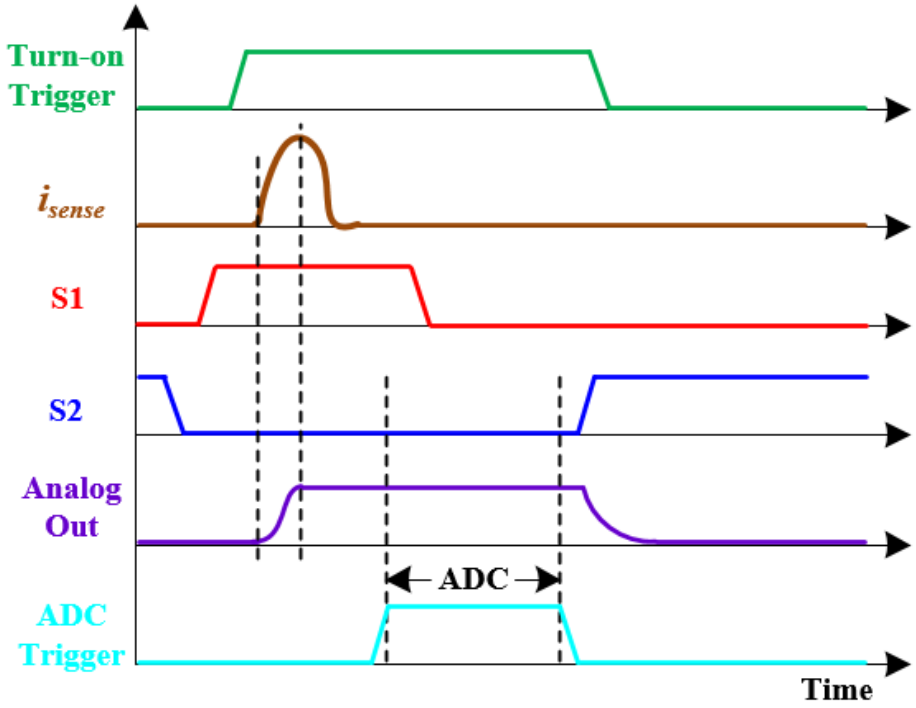


Fig. 6.1.2 The time table for the peak detector circuit

The pulse peak detector can be configured by several different circuit topologies. The most commonly used circuit topology is a feedback opamp charging a capacitor as shown in Fig. 6.1.3. The input signal (the sensed i_G in Volt unit) will be amplified by the left op-amp with the closed-loop gain. If the amplified "sensed i_G" is higher than the voltage across the 1nF capacitor, the capacitor will be charged. If the amplified "sensed i_G" is below the voltage across the 1nF capacitor, the diode will prevent the capacitor being charged. In this circuit, the 1nF capacitor is used to hold the sensed peak value; S_1 is used to activate the peak detector; and S_2 is used to reset the capacitor voltage.

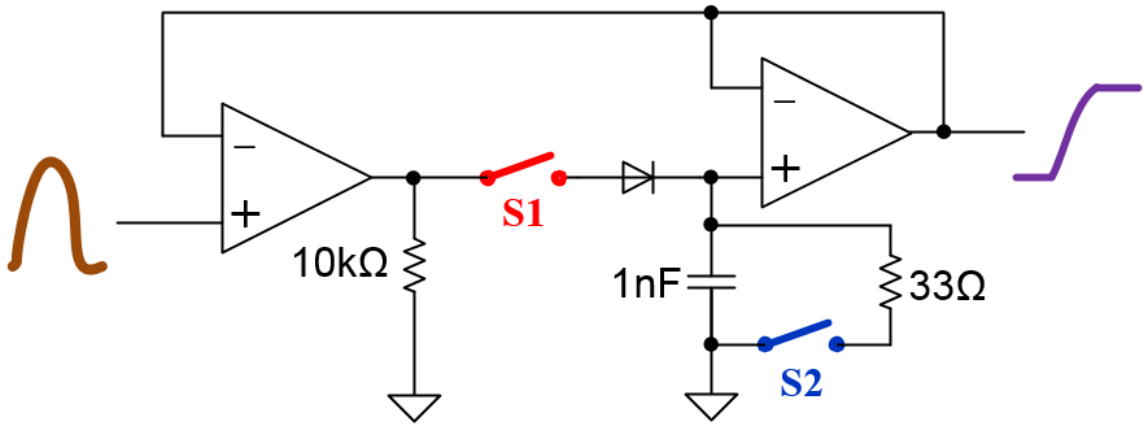


Fig. 6.1.3 Pulse peak detector, feedback op-amp charging capacitor

Another widely used peak detection circuit utilizes the op-amp open-loop amplifying characteristics. The peak detector circuit configuration is shown in Fig. 6.1.4. The input signal (sensed i_G) will be amplified by the left amplifier with open-loop gain. If the amplified "sensed i_G" is higher than the voltage across the 1nF capacitor, the capacitor will be charged. If the amplified "sensed i_G" is below the voltage across the 1nF capacitor, the diode will prevent the capacitor being charged. Similar to the peak detector shown in Fig. 6.1.3, the 1nF capacitor in this circuit is also used to hold the sensed peak value; S_1 is used to activate the peak detector; and S_2 is used to reset the capacitor voltage.

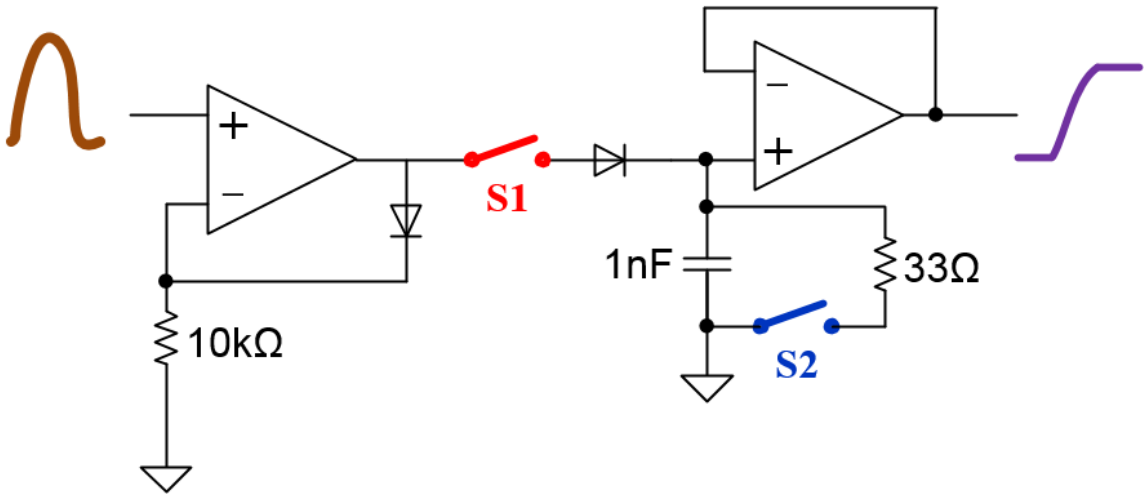


Fig. 6.1.4 Pulse peak detector, open-loop op-amp charging capacitor

6.2 Integration Method

The performance of high bandwith integration circuits relies on the output slew rate of the op-amp. Since the integration will be applied to the whole input signal wavefrom, the op-amp input leakage current will affect the integration of the signals with small amplitude. As a result, an op-amp with high output slew rate and low input leakage current is required.

In this research, the integration of the gate drive turn-on output current transient i_G should be considered as pulse signal integration with a duration between 10ns and 1000ns. In other words, the pulse integrator is used to measure the switching power semiconductor turn-on gate charge. In the case of Si IGBT driven by the push-pull gate drive (Fig. 5.3.7), the i_G integration is dependent on T_j. The integrator applied to the i_G signal (also refered to as i_{sense}) is shown in Fig. 6.2.1, where S_1 and S_2 are used to activate the integrator and reset the integrator. The time table for the integrator circuit is

shown in Fig. 6.2.2.

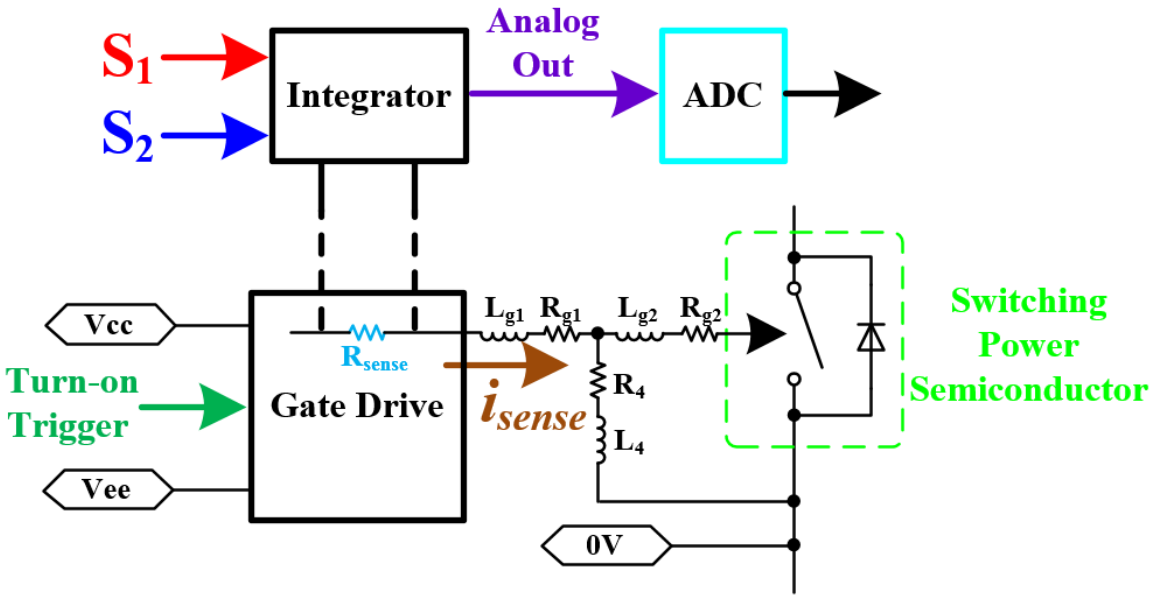


Fig. 6.2.1 Applying integrator to the sensed gate drive turn-on output current transient

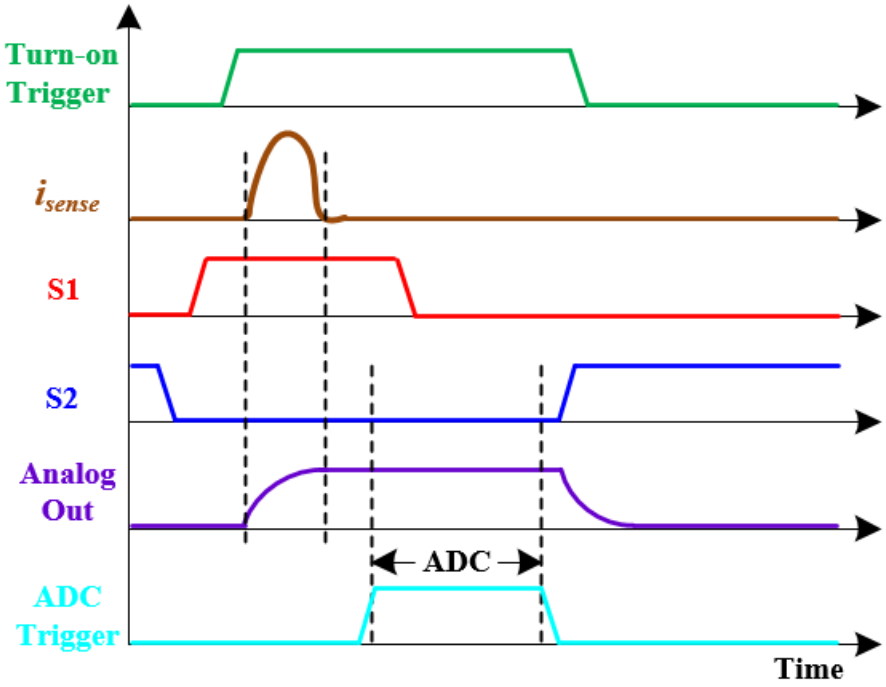


Fig. 6.2.2 The time table for the integrator circuit

The analog integrator can be configured by high bandwidth op-amp feedback with a capacitor as shown in Fig. 6.2.3. The voltage across the feedback capacitor (1nF) is the integration of the input sensed i_G. The left op-amp is used to charge the feedback capacitor and the right op-amp is used as the output buffer for the voltage across the feedback capacitor. S_1 is used to activate the integrator; and S_2 is used to reset the capacitor voltage.

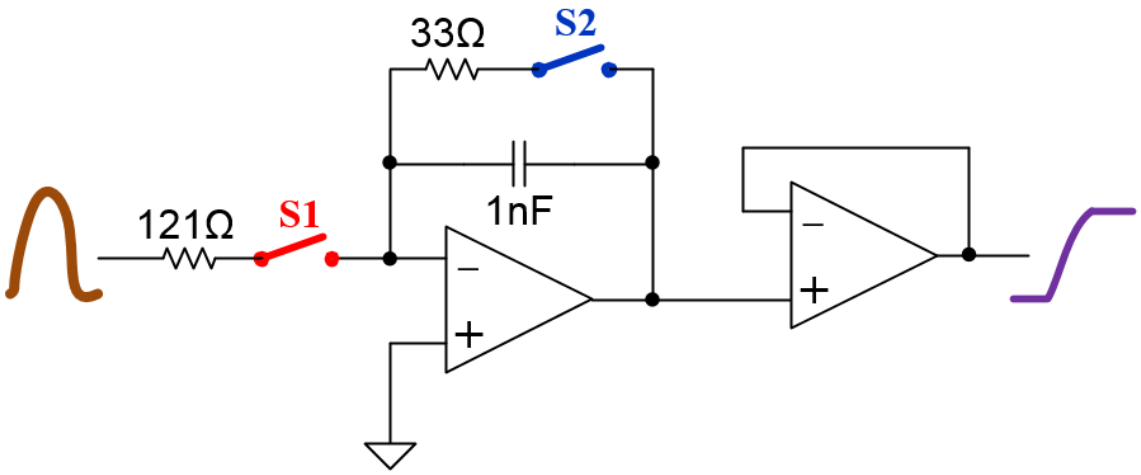


Fig. 6.2.3 Pulse integrator, op-amp charging the feedback capacitor

6.3 Circuit Design for High Bandwidth Signal Sensing

The circuit design is critical for the high bandwidth signal sensing and processing. Ideally, the high bandwidth analog signal processing should be laid out on integrated circuit. With such, the power rating of analog switches, the physical geometry of connections, and the 3-dimensional locations of different function blocks can be feasibly controlled.

However, in this research, the high bandwidth signal processing circuitry are

realized with discrete components. As a result, the switching noise issue, high bandwidth signal transimission line effect, and analog device power level mismatch can more or less affect the quality of the sensing signal.

This section include the layout design recommentations for high bandwidth signal processing. The peak detection circuit used for GaN HEMT Tj sensing is used as a design example.

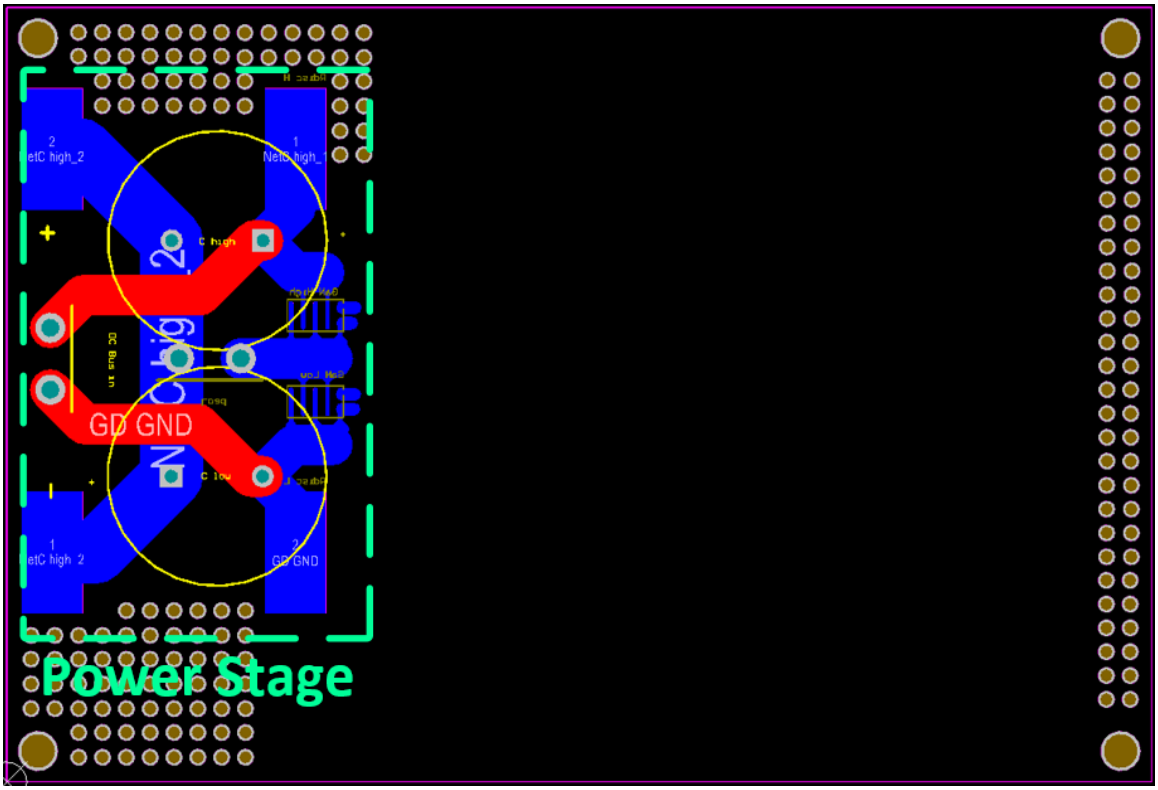


Fig. 6.3.1 Power stage layout

In the power converter design, it is important to separate the power stage switching ciruit and the signal stage sensing/control circuit. Dependeing on the application requirements, the sensing/control circuit can be laid out on one/several pararate PCBs with proper EMI isolations. In this example, all the function block are laid

out on the same PCB.

The power stage switching circuit can be the main in-trace noice source, and EMI source in the circuit. It is recommended that the power stage switching circuit can be set on the side of the PCB, as shown in Fig. 6.3.1.

Note that, in the power stage, the traces follow switching current but not included in the commutation loop should be designed as short as possible. This is because the energy stored in such traces will be released via off-state devices, and generate very high voltage stress.

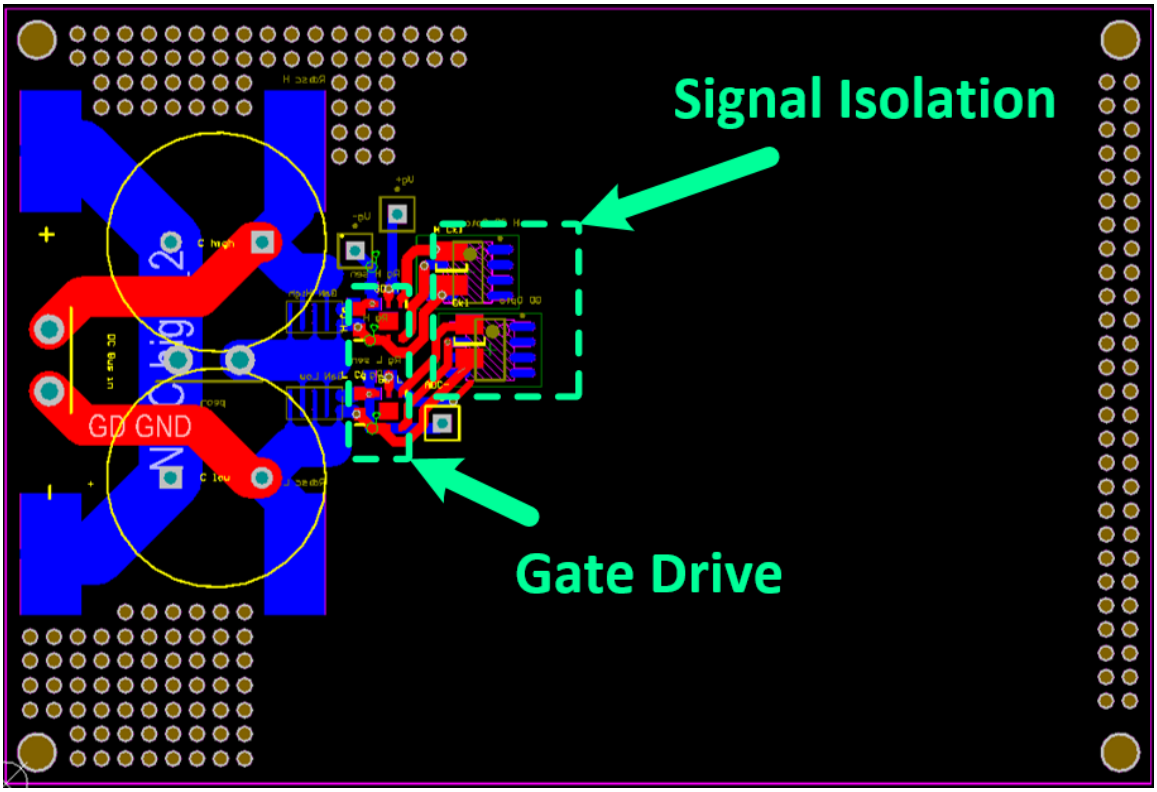


Fig. 6.3.2 Gate drive and its signal isolation layout

Also note that, if the application requires a galvanic connection between the power stage and the sensing/control stage, this connection trce should not be very big,

and decoupling capacitor with large volumes are recommended around such traces.

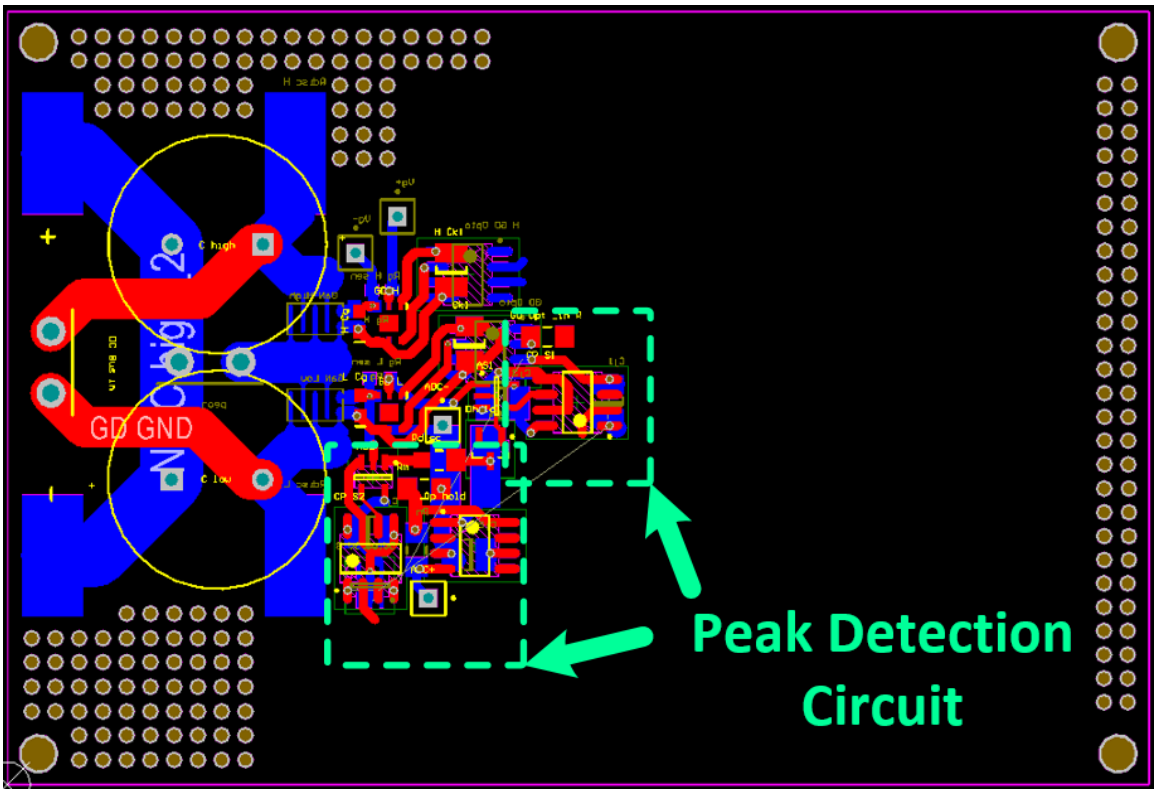


Fig. 6.3.3 Peak detection circuit layout

The power transistor gate drive and the gate drive trigger isolation (usually an opto coupler or a digital coupler) should be located close to the power transistor gate drive as shown in Fig. 6.3.2. The switching quality of of transitor power side is largely related to the gate input signal quality. Although two different gate drives might not be very far from each other, it is not recommended to lay them out very close. This is because the gate signal of one power transistor can be distorted by the switching behavior of other power transistors and other gate drives.

The high bandwidth signal processing circuit (in this case, the peak detection ciruit), should be laid out close enough to the gate signal to be detected. The parasitics in

the peak detection charging loop should be well controlled. The discharging loop does not require too much parasitics control. It is also recommended that the ESL of all the components in the charging loop are minimized. The peak detection circuit is shown in Fig. 6.3.3.

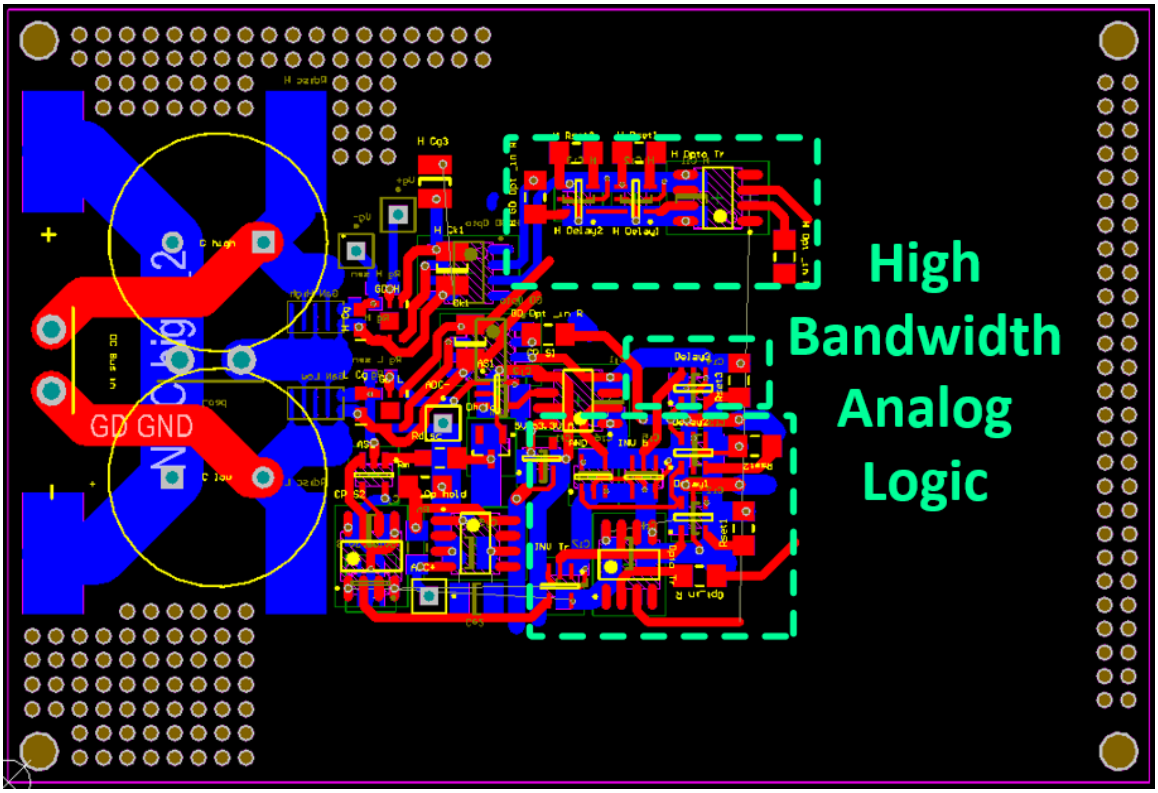


Fig. 6.3.4 High bandwidth analog logic circuit layout

The trigger signal for gate drives, and the two switches in the peak detection circuit requires accurate timing control. It is possible to realize accuate timing with digital controller, however in this case, the trigger signals are realized by analog logic chips. The parasitics control in the analog logic circuit is not as critical as that in the peak detection circuit. Consider that the logic timing is more than 10ns, the transimission delay should be limited within 5ns. The high bandwidth analog logic circuit is shown in

Fig. 6.3.4

The PWM generation circuit is shown in Fig. 6.3.5. The requirement for this part of the circuit includes, (1) not too close to the switching power semicondutors; (2) not to far from the analog logic circuit input.

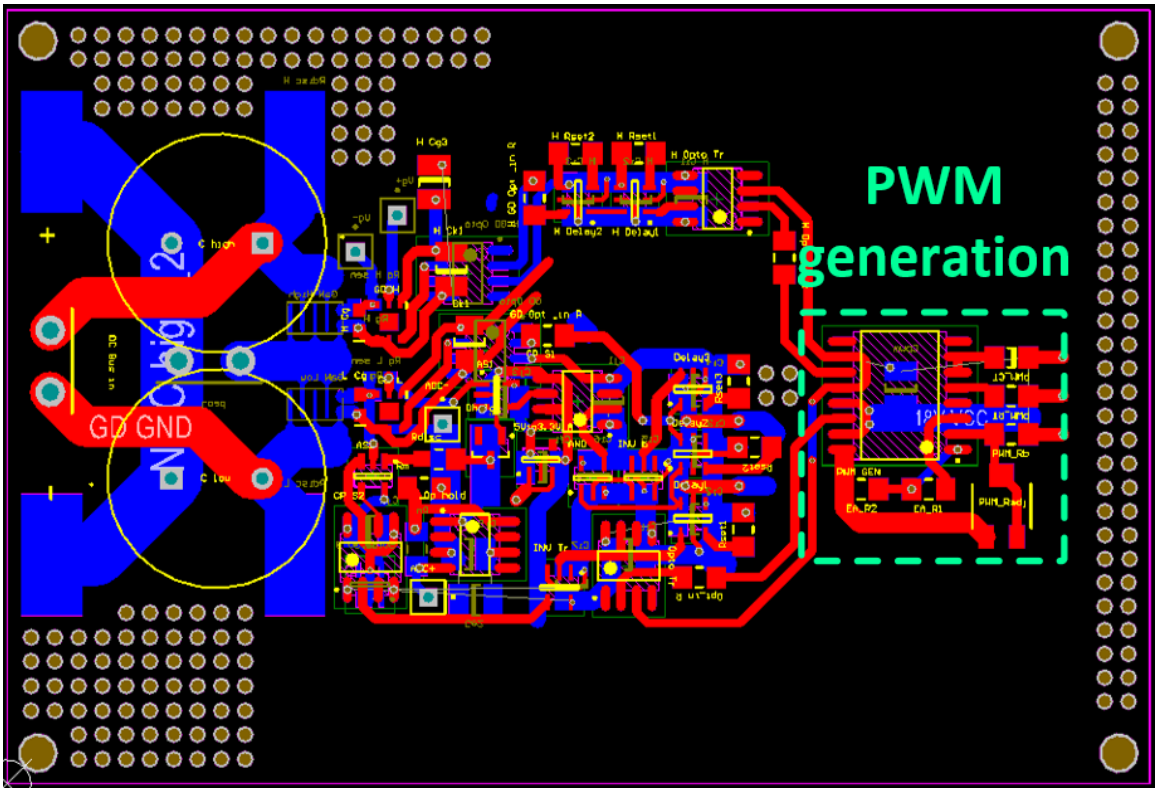


Fig. 6.3.5 PWM generation circuit layout

Some of the aforementioned function blocks requires isolated power supply or voltage regulation. The isolated power suppies are usually transformer isolated switching DCDC converter. The switching frequency of such converters varies from severl kilo-Hz to several hundreds of kilo-Hz. As a result, those isolated power supplies become another noise source on the PCB. It is recommended that those isolated power supplies are not laid out too close to the peak detection circuit. Enough values of output filtering capacitor

(also refered as decoupling capacitor) should be applied to those isolated power supplies. The linear voltage regulators do not generate noise, but can be hot if not properly operated. The auxiliary power supply circuit is shown in Fig. 6.3.6.

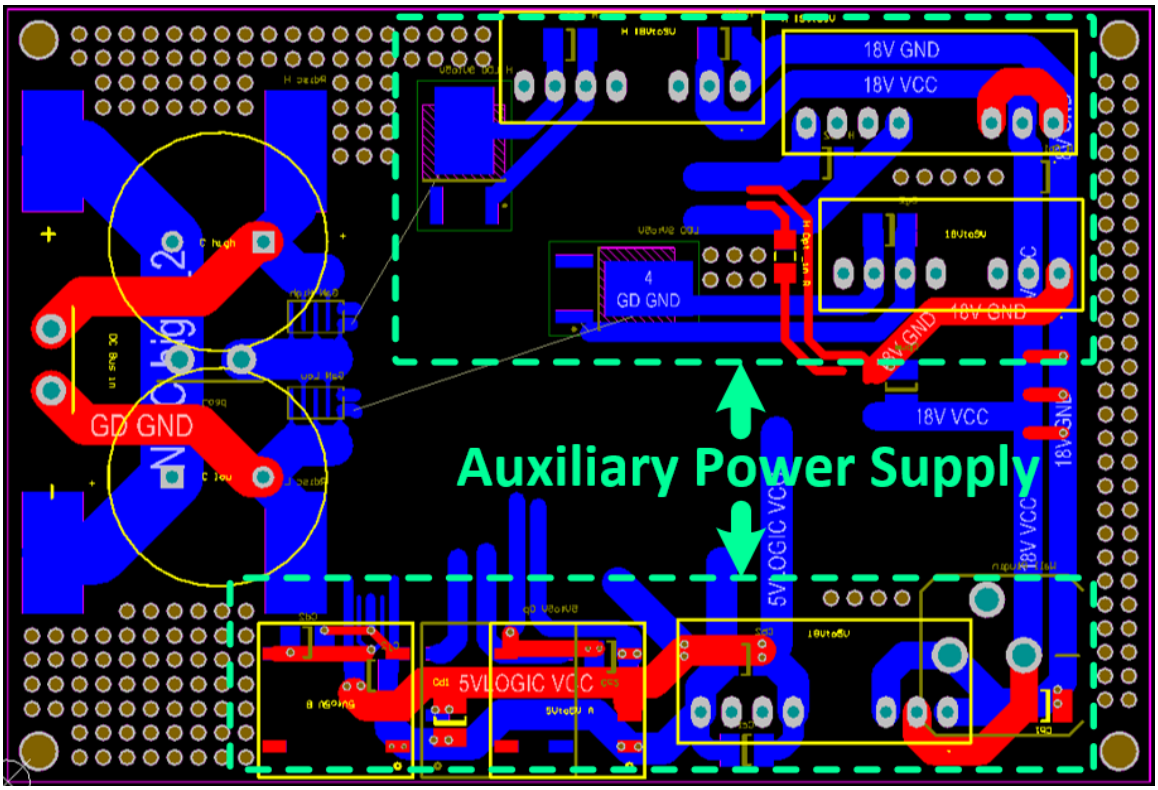


Fig. 6.3.6 Auxiliary power supply circuit layout

With the aforementioned discussion about the layout of different function blocks, the final circuit board layout is shown in Fig. 6.3.7. Using discrete component to build peak detection circuit is the bottleneck of this research. It will be strongly recommended if the gate drive circuit, peak detection circuit, and the analog logic circuit can be integrated on one IC die to benefit parasitics control.

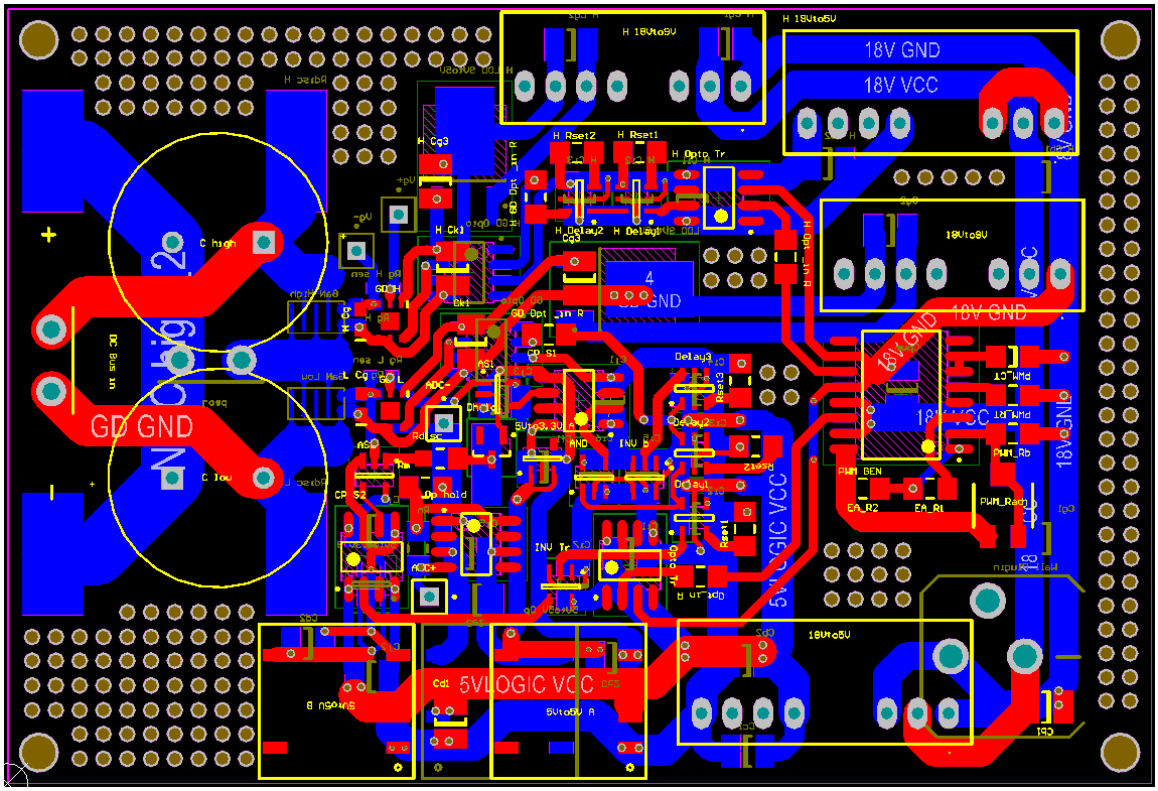


Fig. 6.3.7 Final PCB layout

6.4 Summary of Extracting the Junction Temperature Online

In this chapter, the methodology and the implementation of extracting the T_j information online is discussed. To process the online sensed i_G waveform and convert the T_j information into an output voltage level, analog circuit setup based on high bandwidth op-amp is used. Relying on the sensed i_G waveform T_j dependency, peak detection or integration can be applied to the sensed i_G waveform. Additional switches are configured in the T_j extracting circuit to activate the T_j extraction and reset the T_j extraction.

The T_j extracting implementations are set up to Si MOSFET, Si IGBT, and SiC MOSFET. Depending on the switching power semiconductor turn-on gate charging characteristics, the processed i_G signal (the output voltage level of the T_j extracting circuit) can be positively or negatively correlated to T_j.

Chapter 7 Calibration

This chapter will discuss the calibration of the measured "$i_G - T_j$" dependency. The sensed i_G waveform will be converted to a voltage level by a simple analog circuit (peak detector or integrator). Thus, the repeatability of the analog signal processing can have a significant effect on the T_j sensing accuracy.

The thermal operating point and electrical operating point can also affect the T_j sensing accuracy of the proposed method. If the "$i_G - T_j$" relationship is sensitive to the load current and the rating of the heat sink, the "$i_G - T_j$" based T_j sensing has to be considered the transient load current and the applied heat sink.

Even with the Flir thermal camera, the real junction temperature cannot be feasibly derived since the junction area is buried inside the switching power semiconductor chip.

7.1 Sensing Repeatability

In the proposed T_j sensing method, the PWM controller need to refer to the pre-measured "$i_G - T_j$" relationship in every sampling step. The repeatability of the pre-measured "$i_G - T_j$" relationship is essential to the T_j sensing accuracy.

The "$i_G - T_j$" relationship repeatability can be affected by the following issues: the consistency of the switching power semiconductor performance (especially the gate charging characteristics); and the consistency of the analog circuit for the i_G signal processing.

To verify the repeatability of the "i_G peak – T_j" correlation (Fuji 2SK3677 Si MOSFET driven by push-pull gate drive, re-plotted in Fig. 7.1.1), a repeatability test is shown in Fig. 7.1.2. A 5°C T_j estimation tolerance can be observered from the repeatability test.

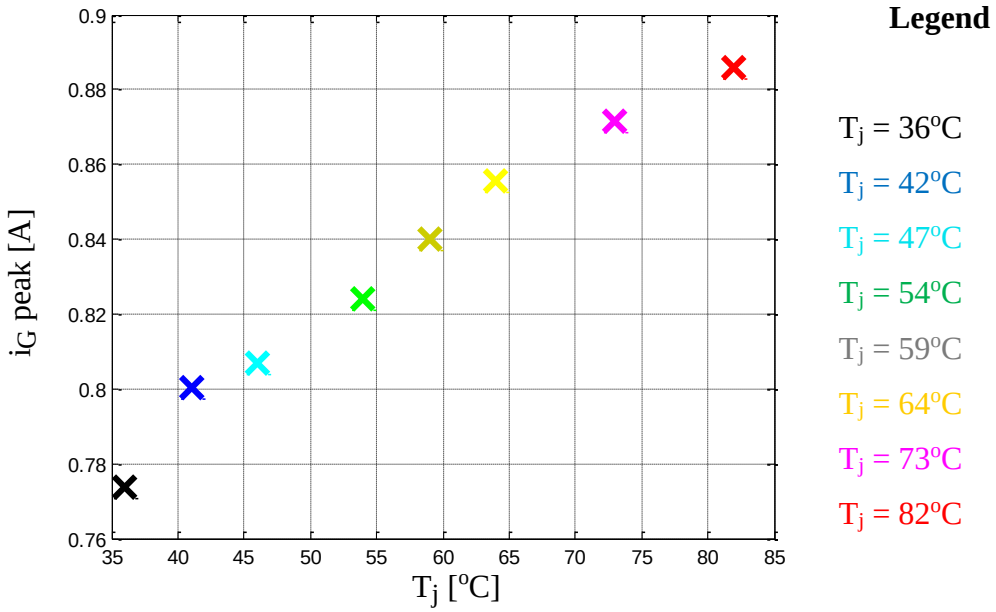


Fig. 7.1.1 The "i_G peak – T_j" correlation, Fuji 2SK3677 Si MOSFET driven by push-pull gate drive

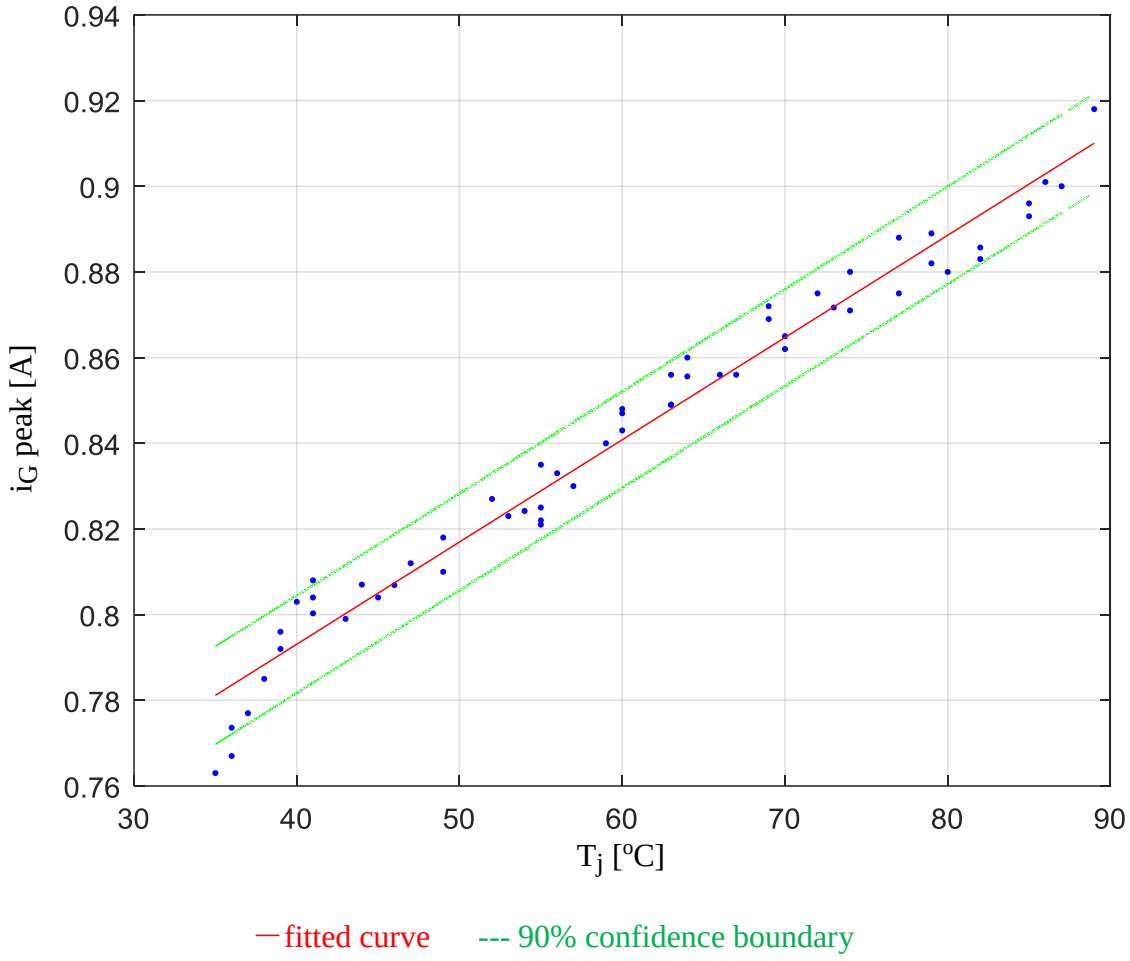
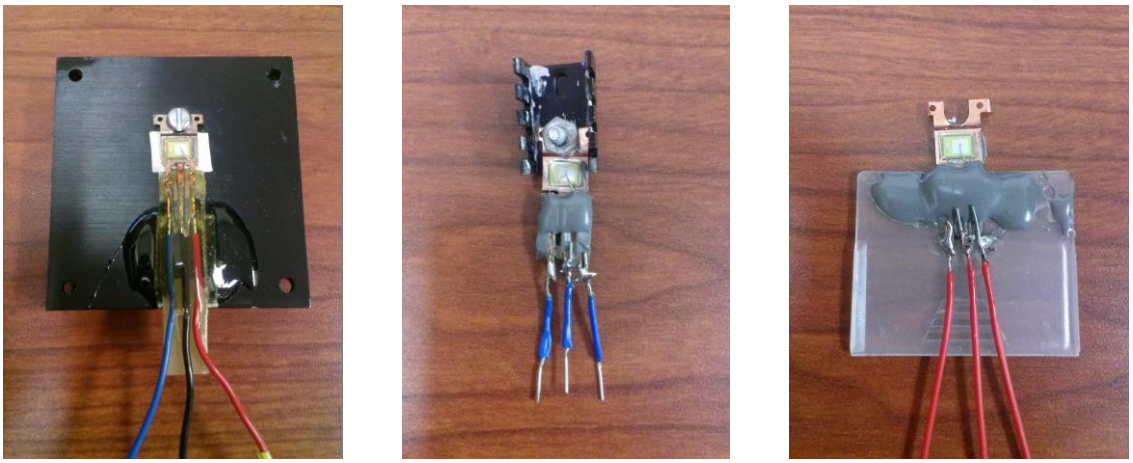


Fig. 7.1.2 The repeatability test for the "i_G peak – T_j" correlation, Fuji 2SK3677 Si MOSFET driven by push-pull gate drive

7.2 The Effect of Heat Sink

In the prototype test, it is possible that the system thermal operating point can affect the "i_G – T_j" relationship, which is used for T_j sensing in this research. In other words, at the same T_j, the temperature difference (or the strain difference) of the device package can cause different turn-on transient i_G waveforms. For instance, the temperature of the device leads can change the parasitic resistance on the leads.

To verify the effect of the system thermal operating point, the rating of the heat sink applied to the switching power semiconductor can be manipulated as aforementioned in section 4.3. The un-encapsulated Fuji 2SK3677-01MR Si MOSFETs attached to different heat sinks are reploted in Fig. 7.2.1 for convenience. The "i_G peak – T_j" test with push-pull gate drive is shown in Fig. 7.2.2 with the colored legend in both Fig. 7.2.1 and Fig. 7.2.2. It can be seen that in the verification test, the rating of the heat sink does not have a significant effect on the "i_G peak – T_j" relationship. Accordingly, in the test setup of Fuji 2SK3677 Si MOSFET driven by push-pull gate drive, the proposed T_j sensing method will not be sensitive to the thermal operating points.



Big heat sink | Small heat sink | No heat sink

Legend: X X X

Fig. 7.2.1 Un-encapsulated Fuji 2SK3677-01MR Si MOSFETs attached to different heat sink

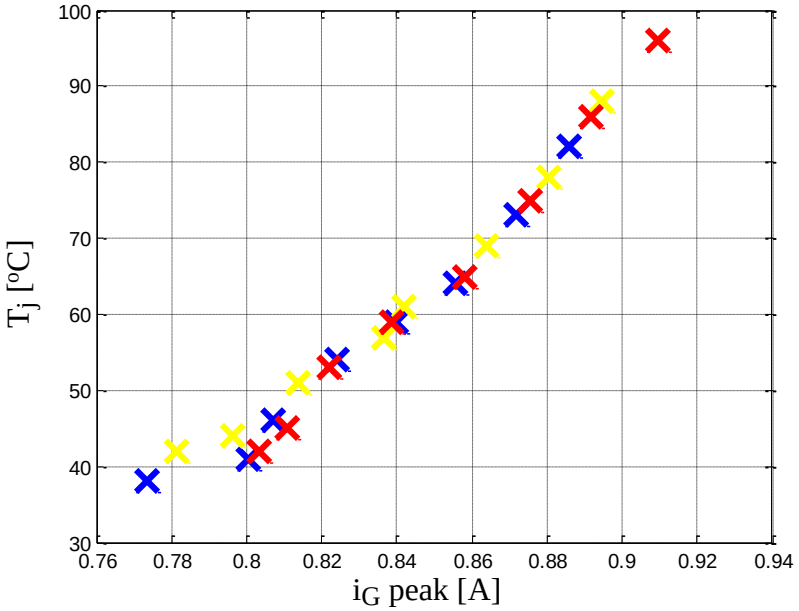


Fig. 7.2.2 Verifiying the effect of thermal operating point on the "i_G peak – T_j" relationship, Fuji 2SK3677 Si MOSFET driven by push-pull gate drive

7.3 Device Vertical Thermal Gradient

In this research, the thermal image captured by the Flir thermal camera is used as the measured T_j in the "i_G – T_j" relationship. In a switching power semiconductor open sample, the real junction area is buried inside the switching power semiconductor chip. The thermal camera can only measure the surface temperature of the chip. Thus, a cross-sectional thermal analysis for the switching power semiconductor chip is necessary.

A 3D model for Fuji 2SK3677-01MR power MOSFET open sample is illustrated in Fig. 7.3.1. The cross-sectional area (highlighted with pink) of the open sample will be used for the 2D thermal analysis in this section.

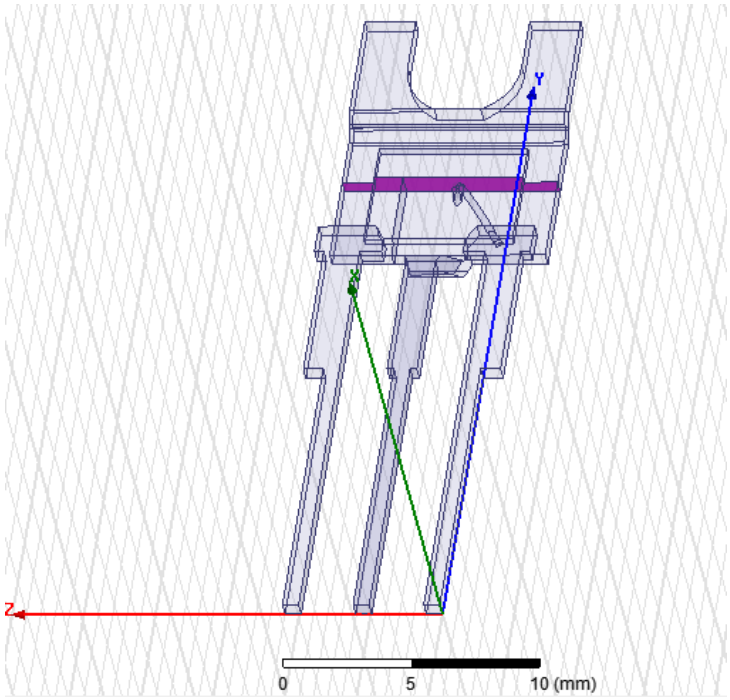


Fig. 7.3.1 3D model for Fuji 2SK3677-01MR power MOSFET

Fuji 2SK3677-01MR power MOSFET cross-sectional temperature contours are derived by 2D finite element analysis (FEA) under the three test conditions stated in Table V, shown in Fig. 19. The full FEA includes MOSFET chip, solder layer, copper layer, and heat sink. Because of the large size of heat sink, it is not shown in Fig. 7.3.2.

Inside the MOSFET chip, heat generation is applied to the whole front-end-of-line (FEOL) and part of the back-end-of-the-line (BEOL) since the upper part of the BEOL should not be considered with heat generation. Surface convection transfers the heat over the entire model to 20 ^{o}C ambient air.

A large temperature gradient can be found in the solder layer and the MOSFET copper layer. Inside the semiconductor chip, the temperature gradient is small. Specifically, in the 15% duty ratio test, a 1^{o}C temperature difference exists inside the

semiconductor chip; in the 50% duty ratio test, this temperature difference is 2°C. This temperature difference inside the semiconductor chip should be considered if high accuracy junction temperature estimation is required.

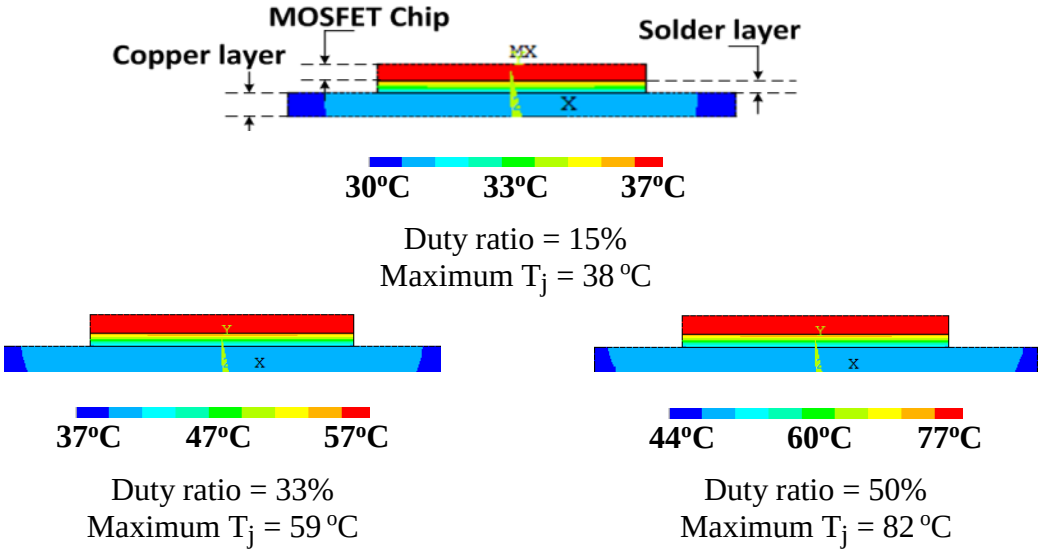


Fig. 7.3.2 Vertical thermal FEA for Fuji 2SK3677-01MR at different T_j

To demonstrate the vertical thermal gradient of the IGBT chip, a 3-D finite element analysis (FEA) model for the partial IGBT module is created in ANSYS APDL, as shown in Fig. 7.3.3. An IGBT chip and an anti-parallel diode chip are included in the model with several other module layers, as shown in the figure. Based on the power dissipation from the IGBT chip and the anti-parallel diode chip, the steady state temperature contours for the 3-D model vertical cut face is simulated, as shown in Fig. 7.3.4.

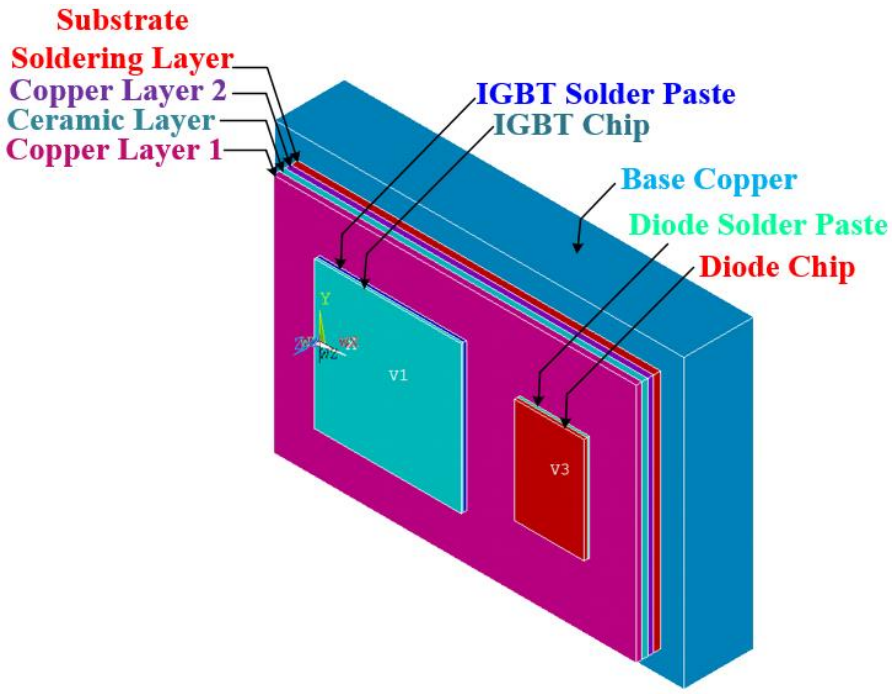


Fig. 7.3.3 3-D FEA model for the partial IGBT module

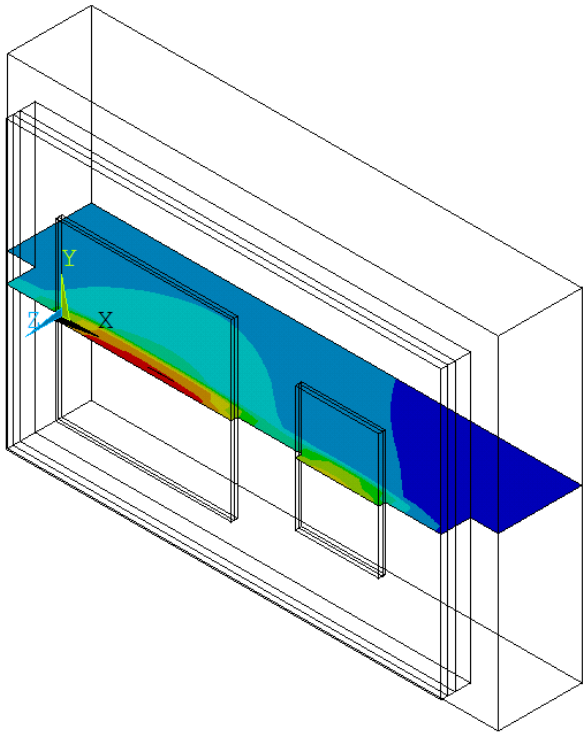


Fig. 7.3.4 Steady state temperature contour for the IGBT 3-D model vertical cut face

Manipulating the maximum T_j to 33.7ºC, 58.6ºC, and 84.9ºC, respectively, the temperature contour plots for the IGBT 3-D model vertical cut face can be derived, as shown in Fig. 7.3.5. It can be seen that in all three different simulated thermal operating conditions in Fig. 7.3.5, the vertical temperature gradient of the whole module is relatively small. The temperature difference between the IGBT chip surface and the chip's inside junction area is about 0.2ºC, which is negligible in this research. Accordingly, the IGBT chip surface temperature measured by the Flir thermal camera is a reasonable approximation of the IGBT T_j.

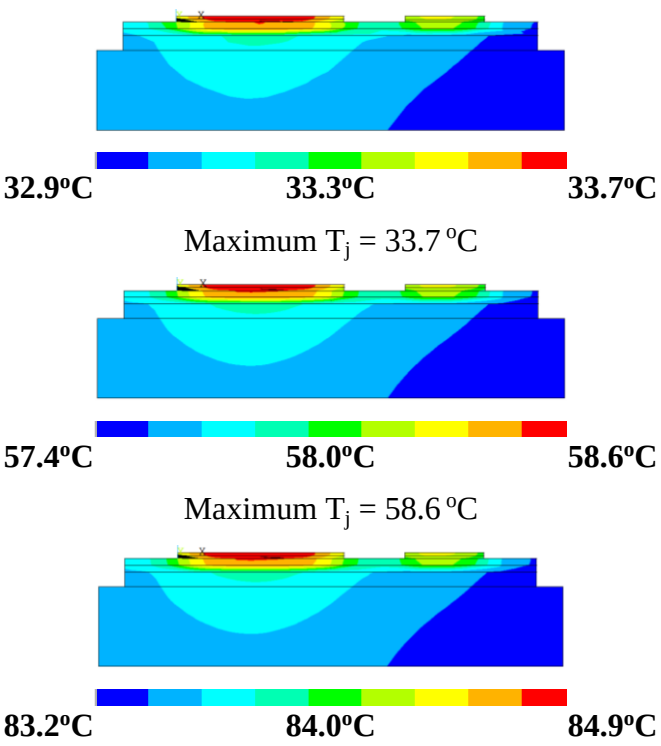


Fig. 7.3.5 Vertical thermal contours for partial Fuji 7MBR15SA140 IGBT module at different T_j

7.4 Summary of Calibration

In this chapter, the calibration for the "$i_G - T_j$" relationship based T_j sensing method is provided. The repeatability test and the thermal operating point test are achieved on the case of Fuji 2SK3677-01MR power MOSFET driven by a push-pull gate drive. In addition, finite element analysis for the power semiconductor chip vertical temperature gradient is provided.

In the case of Fuji 2SK3677-01MR power MOSFET driven by a push-pull gate drive, the "$i_G - T_j$" relationship has 5^{o}C temperature tolerance in the repeatability test. Up to 2^{o}C temperature difference is expected in the semiconductor chip vertical thermal distribution. The "$i_G - T_j$" relationship does not explicitly depend on the thermal operating points of the system.

Chapter 8 Effect of Gate Drive Topologies on the Turn-on Transient Gate Output

In this chapter, the "$i_G - T_j$" relationship based T_j sensing method is applied to SiC MOSFETs, and the T_j sensing properties of using different gate drive topologies are studied.

This chapter will provide the modeling of the Rohm SCT2160KE SiC MOSFET driven by the "voltage source gate drive" using push-pull output stage, and the "current source gate drive" using current mirror. The T_j dependence of i_G under different gate drive system is compared in Spice simulation and prototype test. A feasible T_j extraction method for different gate drive systems is investigated. In the final thesis, the gate drive based T_j sensing comparison will include the "quasi voltage source gate drive" using a bootstrap capacitor and the "current source gate drive" using an inductor.

8.1 Push-pull Output Based Voltage Source Gate Drive

Most of the integrated gate drives use the push-pull output, which achieves simple turn-on/turn-off control and fast hard switching. In this research, to turn on the SiC MOSFET, the gate-source voltage (V_{GS}) should be set between +10V and +20V. To turn off the SiC MOSFET, V_{GS} should be set between 0V and -10V. In the push-pull output stage, a P-type MOSFET is used as a pull-up transistor and an N-type MOSFET is used as a pull-down transistor. A logic inverter is also included in the gate drive system so that

the gate drive input on/off logic can be synchronized to the gate drive output high/low state.

The dynamic model for the push-pull output gate drive is shown in Fig. 8.1.1. The model includes the switching control signal, the logic inverter, the push-pull output stage, the gate drive resistance, and the parasitics in the gate drive system. A current sensing resistor Rsense1 is implemented in the gate drive system for the gate drive turn-on current (i_{G1}) sensing. An ideal logic inverter model is used in the gate drive system modeling. Spice level 3 MOSFET model is used for the two MOSFETs in the push-pull output stage.

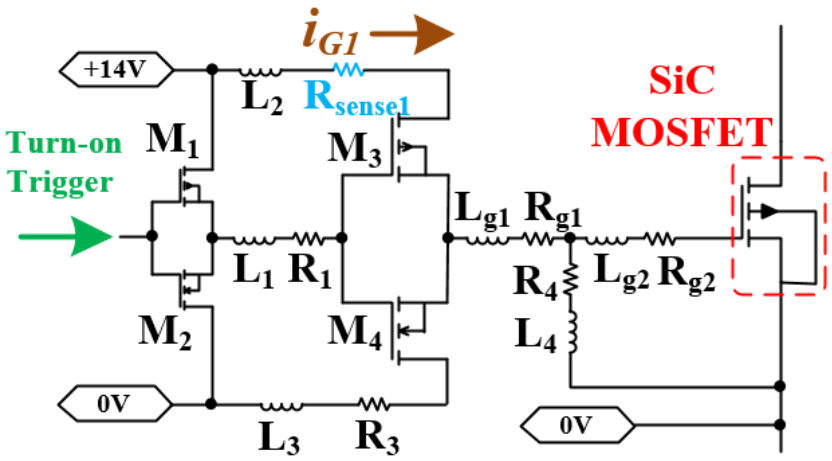
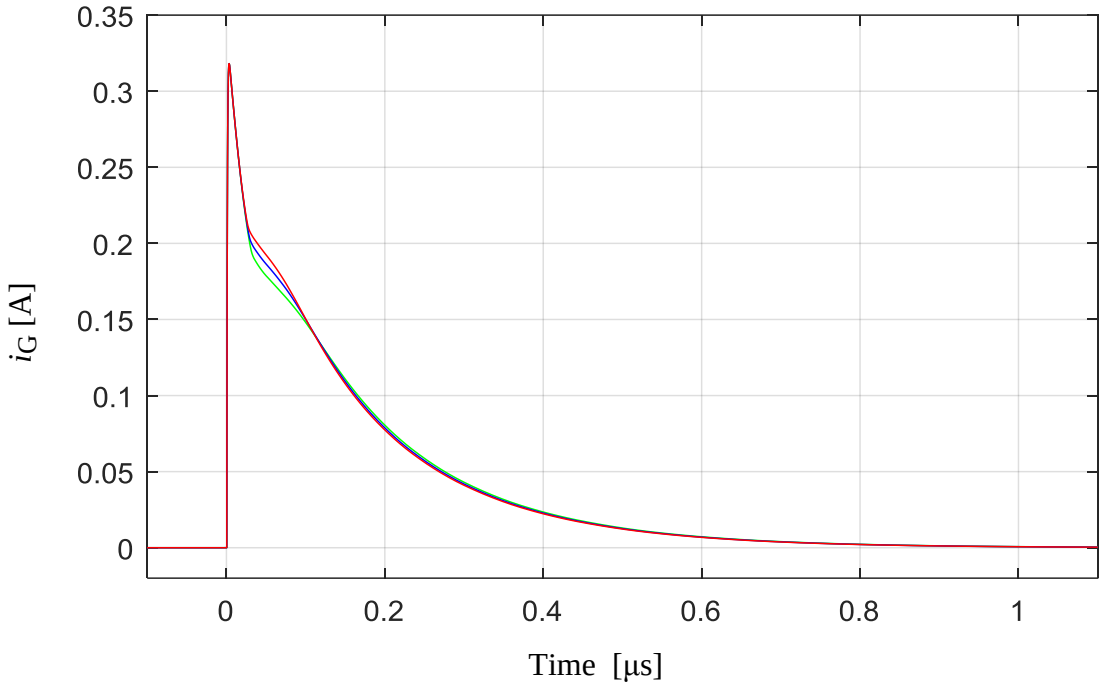


Fig. 8.1.1 SiC MOSFET driven by push-pull output gate drive

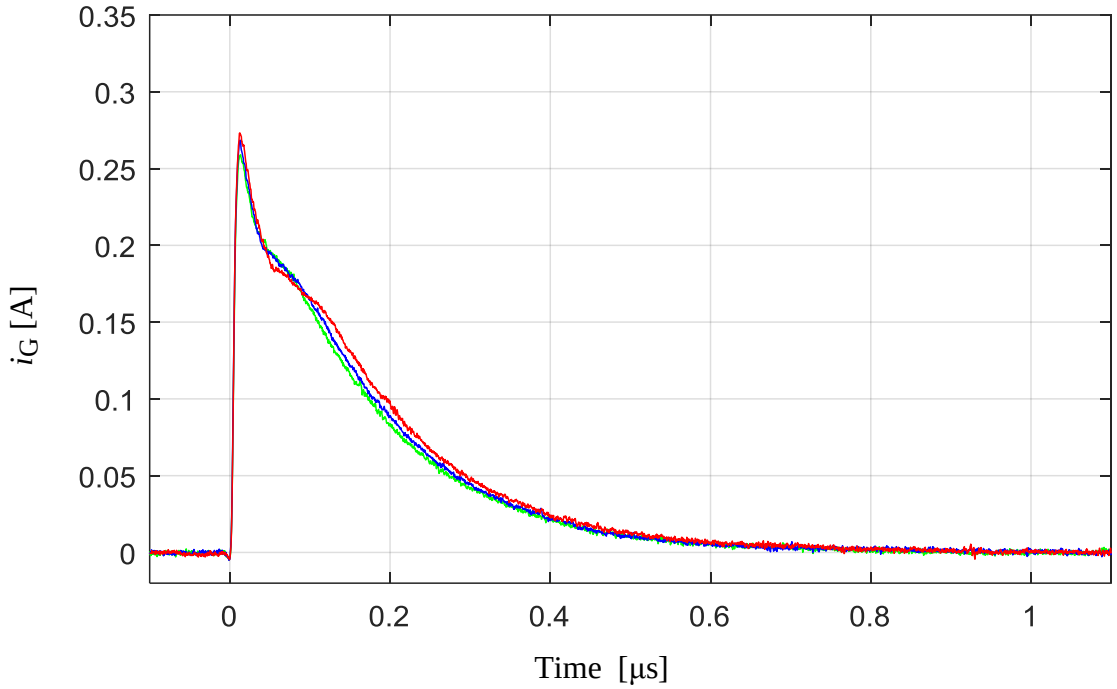
Rohm Semiconductor RRR040P03TL P-channel MOSFET and RTR040N03TL N-channel MOSFET are selected for M_1 and M_2 in Fig. 8.1.1, respectively. Setting T_j to 31°C, 67°C and 105°C, the system dynamic model is simulated for each temperature. The simulation result for the gate drive turn-on current, i_G, is shown in Fig. 8.1.2.



Legend: T_j = 31°C T_j = 67°C T_j = 105°C

Fig. 8.1.2 Simulated sensed gate drive turn-on output current i_G transient, Rohm SCT2160KE SiC MOSFET driven by push-pull output gate drive

By setting the H-bridge inverter (as discussed in chapter 3) duty ratio to 15%, 40%, and 65%, the T_j of the Rohm SCT2160KE SiC MOSFET can be manipulated to 31°C, 67°C and 105°C at steady state. The experimentally tested turn-on i_G waveforms for this setup are shown in Fig. 8.1.3.



Legend: T_j = 31°C T_j = 67°C T_j = 105°C

Fig. 8.1.3 Experimentally measured sensed gate drive turn-on output current i_G transient, Rohm SCT2160KE SiC MOSFET driven by push-pull output gate drive

It can be seen from Fig. 8.1.3 that the integration of the turn-on i_G waveforms are T_j sensitive. Thus, the "$\int i_G - T_j$" relationship for the waveforms in Fig. 8.1.3 can be derived as shown in Fig. 8.1.4.

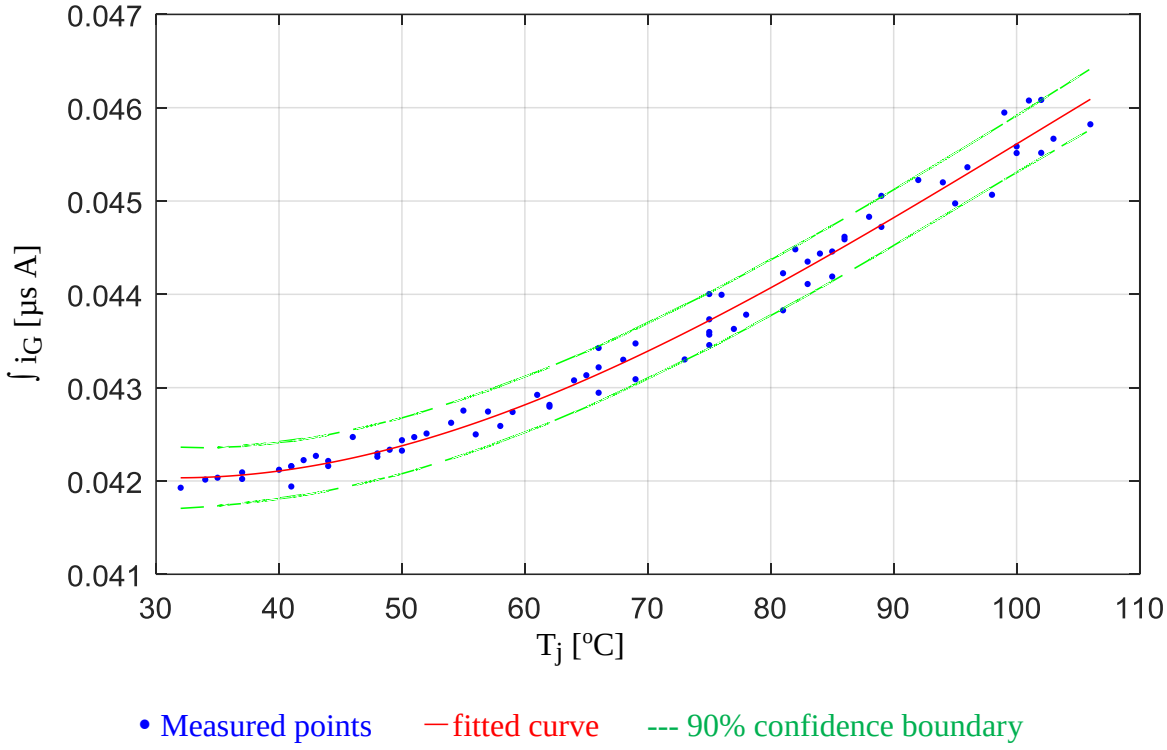


Fig. 8.1.4 The "$\int i_G - T_j$" correlation, Rohm SCT2160KE SiC MOSFET driven by push-pull output gate drive

8.2 Current Mirror Based Current Source Gate Drive

Wide bandgap semiconductors using Silicon Carbide (SiC) or Gallium Nitride (GaN) usually have a smaller gate charge value compared with conventional Si MOSFET and IGBT (the comparison should be based on the same power rating). As a result, very large dV_{DS}/dt can make the switching voltage/current overshoot a big risk for the converter system. In such cases, switching speed control from the gate drive is desired. By manipulating the output current value, current source gate drive is feasible for semiconductor smooth switching.

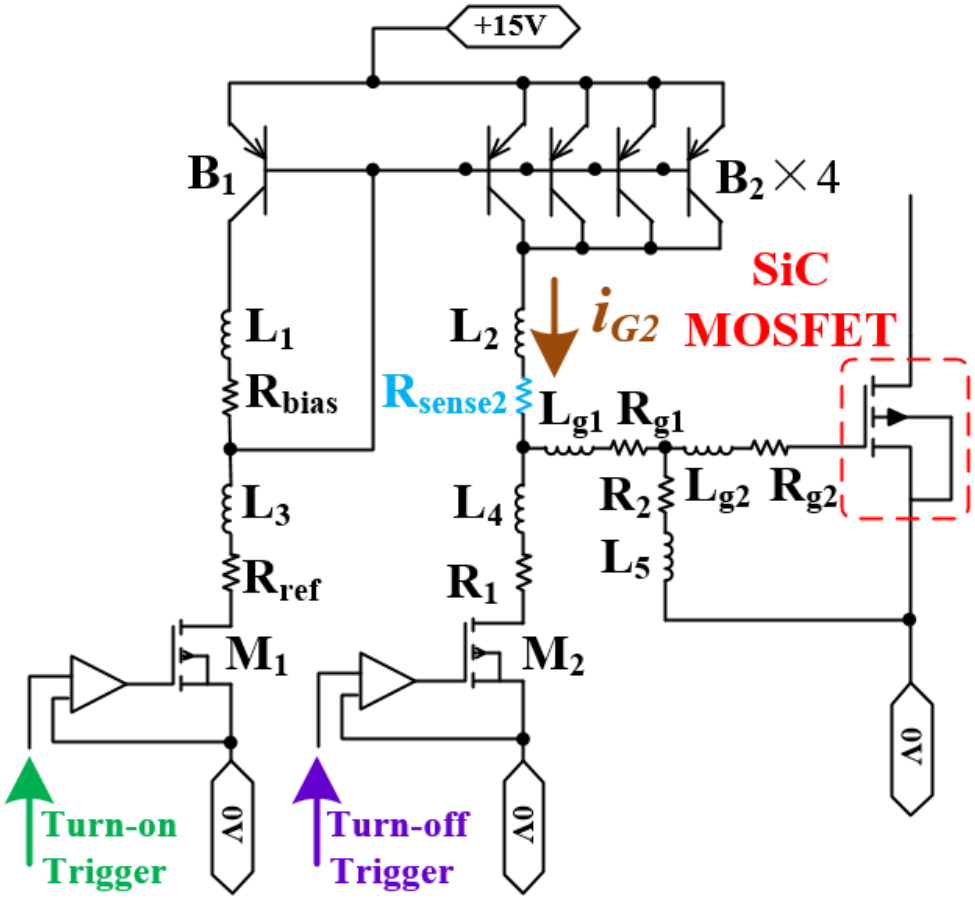
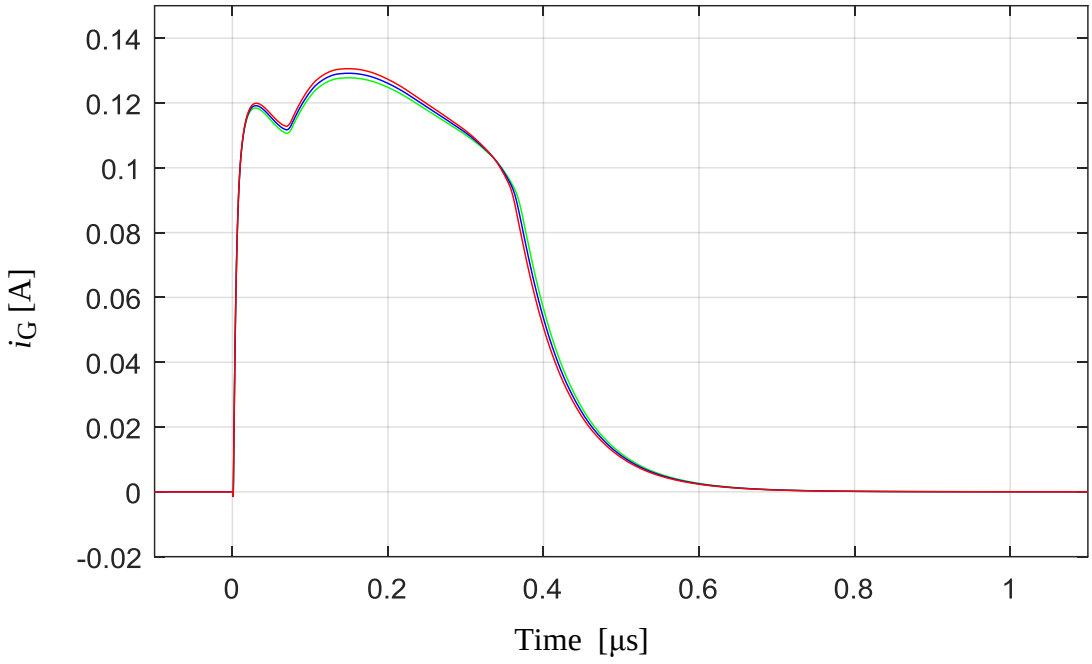


Fig. 8.2.1 Current mirror gate drive dynamic model

In this research, a current mirror is implemented in the current source gate drive high side using P type bipolar junction transistor (BJT), as shown in Fig. 8.2.1. The gate drive output current source can be manipulated by adjusting the value of the reference resistance R_{ref}. M_1 can activate the current mirror, and the current mirror will be used only to turn on the SiC MOSFET. To turn off the SiC MOSFET, the MOSFET gate will be connected to the MOSFET source by M_2. If current control turn off is desired, a current sink should be implemented in the gate drive low side. A detailed operating

mechanism for this current mirror based current source gate drive will be discussed in the final paper.

In Fig. 8.2.1, the gate drive dynamic model includes the current mirror BJTs (B_1 and B_2), the current mirror activating MOSFET M_1, the pull-down MOSFET M_2, the gate drive resistance, and the parasitics in the gate drive system. A current sensing resistor R_{sense2} is implemented in the gate drive system for the gate drive turn-on current (i_{G2}) sensing. Spice level 3 BJT model is used for all the BJTs and MOSFETs in the gate drive system.

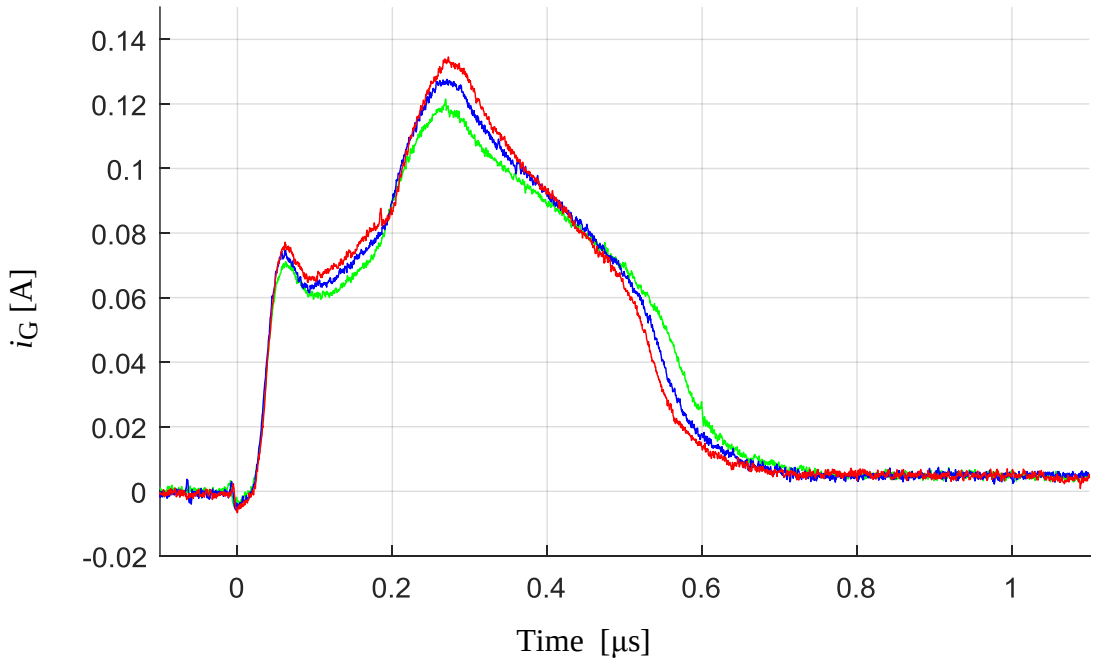


Legend: T_j = 31°C T_j = 67°C T_j = 105°C

Fig. 8.2.2 Simulated sensed gate drive turn-on output current i_G transient, Rohm SCT2160KE SiC MOSFET driven by current mirror gate drive

Rohm Semiconductor RHK005N03 is selected for M_1; Diodes Incorporated DMN100 is selected for M_2; NXP Semiconductor PBSS5540Z is selected for B_1 and B_2.

Note that B_2 includes four NXP Semiconductor PBSS5540Z BJTs connected in parallel. Setting T_j to 31°C, 67°C and 105°C, the system dynamic model is simulated for each temperature. The simulation result for the gate drive turn-on current, i_G, are shown in Fig. 8.2.2. The experimentally tested turn-on i_G waveforms for this setup is shown in Fig. 8.2.3.



Legend: T_j = 31°C T_j = 67°C T_j = 105°C

Fig. 8.2.3 Experimentally measured sensed gate drive turn-on output current i_G transient, Rohm SCT2160KE SiC MOSFET driven by current mirror gate drive

It can be seen from Fig. 8.2.3 that the peak value of the turn-on i_G waveforms are T_j sensitive. Thus the "$i_{G\ peak} - T_j$" relationship for the waveforms in Fig. 8.2.3 can be derived as shown in Fig. 8.2.4.

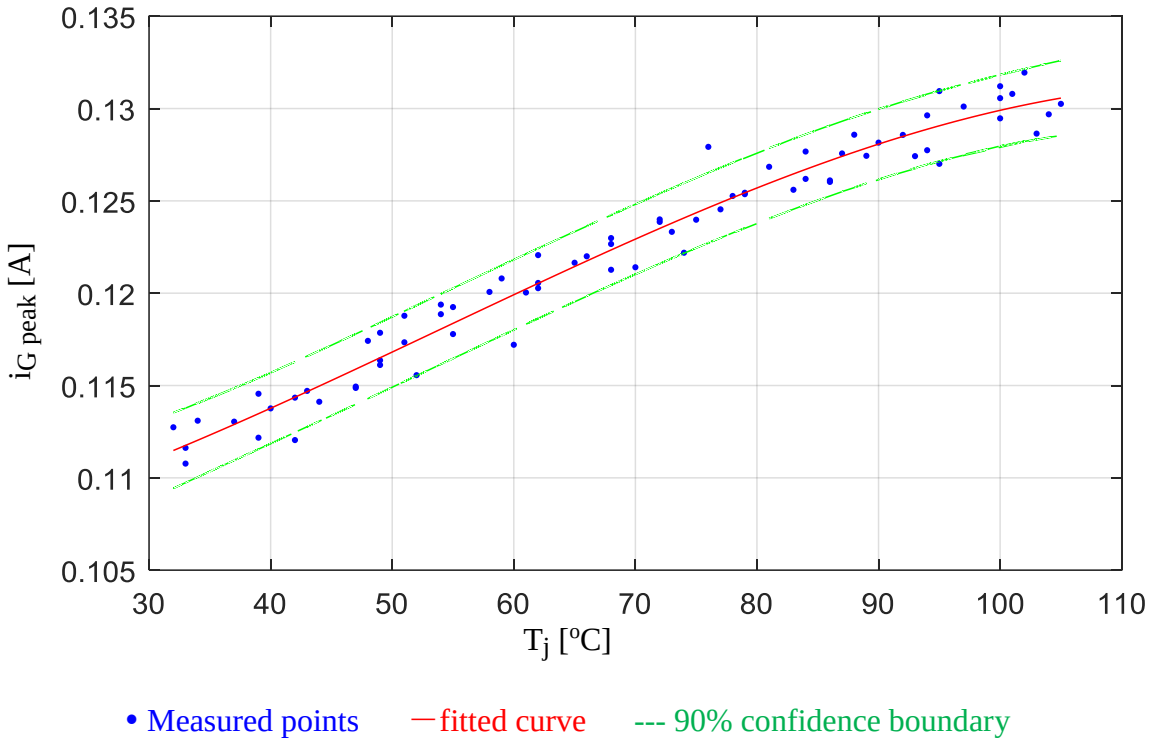


Fig. 8.2.4 The "$i_{G\ peak} - T_j$" correlation, Rohm SCT2160KE SiC MOSFET driven by current mirror gate drive

8.3 Inductor Based Current Source Gate Drive

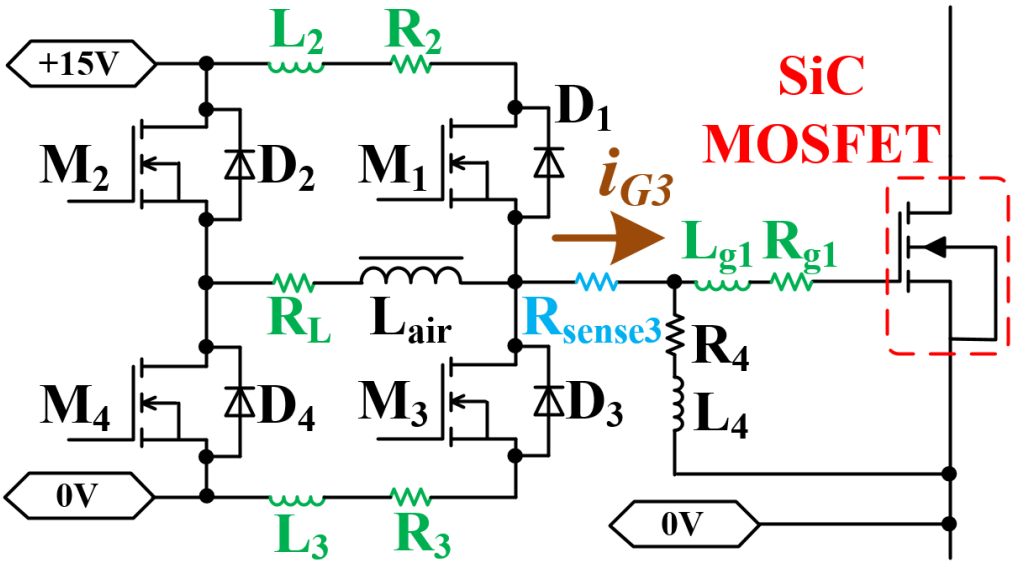
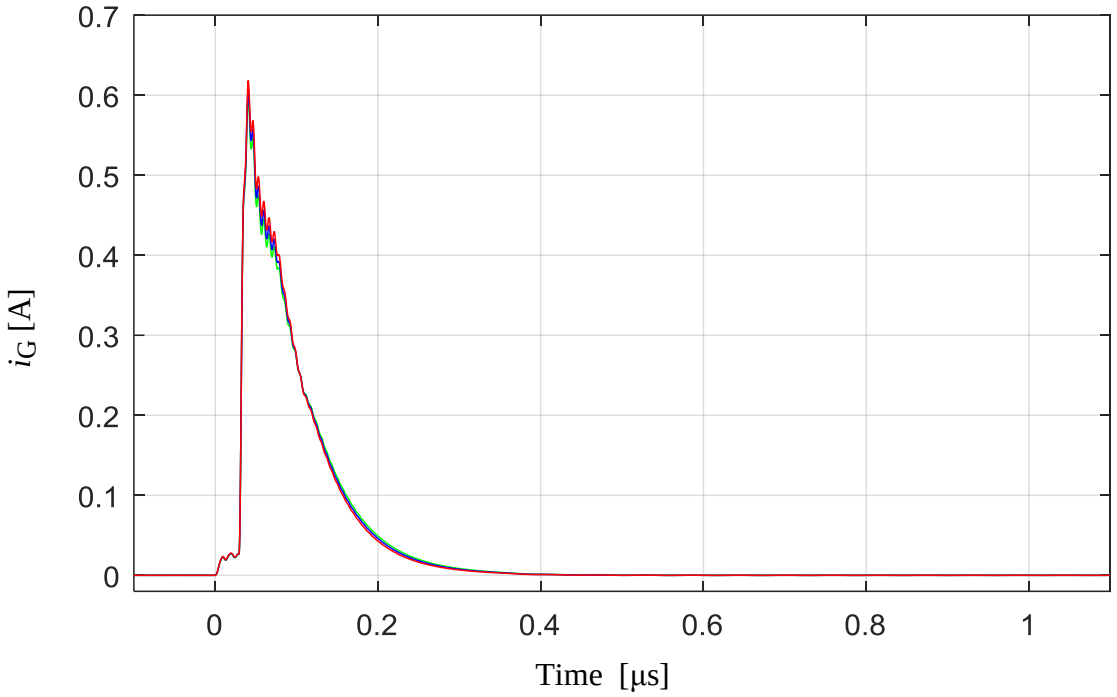


Fig. 8.3.1 Inductor-based gate drive dynamic model

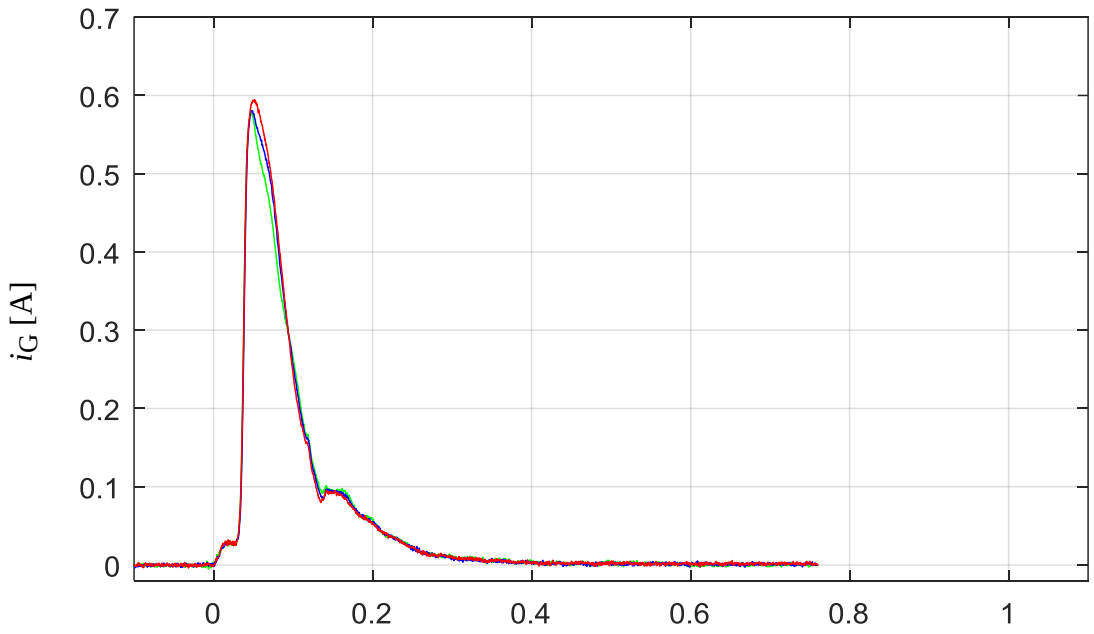
The inductor-based current source gate drive dynamic model was fully discussed in chapter 3, and is shown again in Fig. 8.3.1. Four controlled switches (M_1 to M_4) and their anti-parallel diodes (D_1 to D_4) are connected as an H-bridge with an air-core inductor L_{air} implemented as the load. By properly operating the controlled switches, the SiC MOSFET gate turn-on and turn-off process can start with a non-zero pre-charge current. Following the charging and discharging of the SiC MOSFET, the excess energy stored in the inductor can be returned to the 15V power supply, thereby allowing the gate charge energy to be recovered. A current sensing resistor R_{sense3} is implemented in the gate drive system for the gate drive current (i_{G3}) sensing.

The simulation result for the gate drive turn-on current, i_G, is shown in Fig. 8.3.2. The experimentally tested turn-on i_G waveforms for this setup are shown in Fig. 8.3.3.



Legend: T_j = 31°C T_j = 67°C T_j = 105°C

Fig. 8.2.2 Simulated sensed gate drive turn-on output current i_G transient, Rohm SCT2160KE SiC MOSFET driven by inductor based current source gate drive



Time [μs]

Legend: T_j = 31°C T_j = 67°C T_j = 105°C

Fig. 8.3.3 Experimentally measured sensed gate drive turn-on output current i_G transient, Rohm SCT2160KE SiC MOSFET driven by inductor based current source gate drive

It can be seen from Fig. 8.3.3 that the integration of the turn-on i_G waveforms are T_j sensitive. Thus, the "$\int i_G - T_j$" relationship for the waveforms in Fig. 8.3.3 can be derived as shown in Fig. 8.3.4.

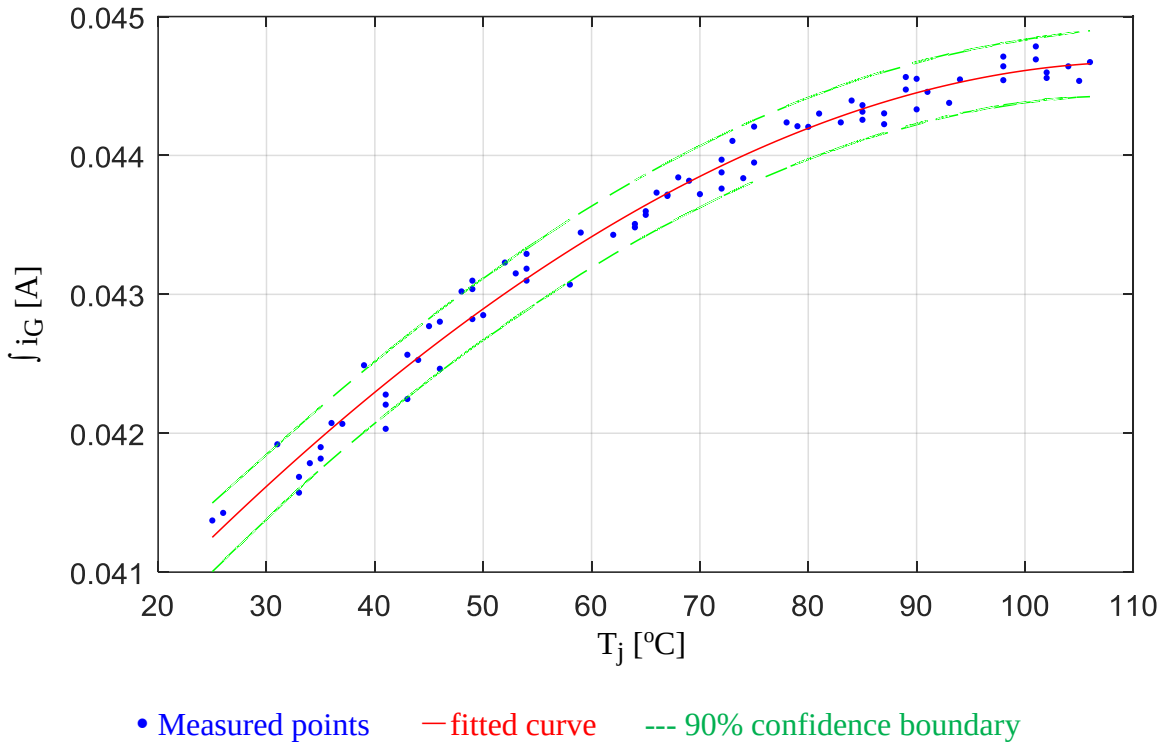


Fig. 8.3.4 The "$\int i_G - T_j$" correlation, Rohm SCT2160KE SiC MOSFET driven by inductor based current source gate drive

8.4 Effects of Gate Drive Topologies on Junction Temperature Sensing

It can be observed from the experimentally tested waveforms (Fig. 8.1.3, Fig. 8.2.3, and Fig. 8.3.3) that i_G will change according to T_j and that different gate drive topologies can have different i_G waveforms. For the three gate drives evaluated (push-pull output gate drive, current mirror gate drive, and the inductor-based gate drive), the turn-on gate charge (referred to as "Q_g") has a positive T_j coefficient. To investigate the SiC MOSFET "$Q_g - T_j$" dependencies, several device temperature dependencies need to be considered.

The SiC MOSFET turn-on gate charge is the result of generating the on-state conducting channel (gate energy injection). The turn-on gate charge is a function of carrier mobility (M_c), carrier density (n_c), and bandgap energy (E_g), as shown in (5.1).

$$Q_g = G(M_c , n_c , E_g) \tag{5.1}$$

The semiconductor channel carrier mobility (M_c) has a negative T_j coefficient, as shown in (5.2), where α is a positive temperature dependent constant.

$$M_c(T_j) = M_c(T_0) \left(\frac{T_j}{T_0}\right)^{-\alpha} \tag{5.2}$$

The semiconductor channel carrier density (n_c) has a positive T_j coefficient. However, if the T_j dependency of M_c is characterized, n_c can be considered as a constant.

The bandgap energy (E_g) of SiC has negative T_j coefficient, as shown in (5.3), where $E_g(0)$ is the bandgap energy at absolute zero on the Kelvin scale in the given material, and α_E and β_E are material specific constants.

$$E_g(T_j) = E_g(0) - \frac{\alpha_E T_j^2}{T_j + \beta_E} \tag{5.3}$$

With higher T_j, lower M_c tend to increase Q_g (in order to build the channel under the same current rating), while the smaller E_g tend to decrease Q_g (because V_{TH} and C_{GS} are lower according to smaller E_g). However, the E_g of most of the semiconductor devices will not be significantly changed if they are operated below the maximum allowed temperature. Note that the maximum allowed temperature is usually limited by device packages. Thus, the temperature dependency of M_c will dominate the temperature dependency of Q_g. As a result, larger Q_g is observed under higher T_j.

8.5 Summary of the Effect of Gate Drive Topologies on the Turn-on transient Gate Output

In this chapter, the online T_j sensing for SiC MOSFET driven by voltage source gate drive and current source gate drive is investigated. The "$i_G - T_j$" dependency with different gate drive topologies are compared.

In the case of Rohm SCT2160KE SiC MOSFET, the gate charge is positively correlated to device T_j. The push-pull gate drive usually do not have a limit on output voltage and thus, the peak detection method is suitable to correlate the turn-on i_G signal to T_j. The current mirror gate drive can manipulate the maximum gate drive output

current, thus using the integration method to measure the gate charge and correlate it until T_j is feasible.

Chapter 9 The Effect of DC Bus Voltage and Load Inductive Properties

This chapter will discuss the effect of the DC bus voltage value and load properties on the proposed T_j sensing method. The aforementioned T_j sensing methods are investigated under a fixed DC bus voltage with resistive load. However, the power transistor gate properties are well known as bias dependent. As a result, changing the off-state voltage stress and the on-state voltage drop can more or less affect the gate properties of the devices. It is necessary to consider the effect of DC bus voltage value and load inductive properties when implementing the proposed T_j sensing method.

This chapter will study the effect of DC bus voltage on the proposed T_j sensing methods. Two types of devices (SiC MOSFETs and GaN HEMTs), two T_j extraction methods (peak detection and integration), and three types of gate drives (push-pull gate drive, current mirror gate drive, and inductor-based gate drive) will be included. To include the effect of DC bus voltage value, three-dimensional correlations, "i_G – T_j – DC bus" are proposed in this chapter.

This chapter will also investigate the effect of load inductive properties on the propose T_j sensing methods. An RL load is applied to the Si IGBT-based H-bridge inverter as discussed in section 3.3. The proposed Tj seninsg method is evaluated with three different RL combinations. To include the effect of load inductive properties, a three-dimensional "i_G – T_j – Load property" correlations are proposed in this chapter.

9.1 The Effect of DC Bus Voltage Value on GaN HEMT

With the half-bridge inverter setup discussed in chapter 5, during the HEMT turn-on transient, the voltage stress across the device drain and source (V_{DS}) decreases from half of the DC bus voltage to almost zero. The switching transient properties of GaN HEMTs are proven to be sensitive to the bias voltage (for both on state and off state) [54]. As a result, varying the DC bus voltage of the half-bridge inverter can affect the switching transient properties of the GaN HEMTs.

To include the effect of the V_{DS} bias voltage in the proposed T_j sensing method, the 2-dimensional "peak vs. T_j" relationship (as shown in chapter 5) is extended to a 3-dimensional "peak vs. T_j vs. DC bus" relationship, as illustrated in Fig. 9.1.1. The "peak vs. T_j vs. DC bus" relationship is experimentally derived based on the method discussed in chapter 5 and chapter 6, with the DC bus varying from 22V to 36V, as illustrated in Fig. 9.1.1.

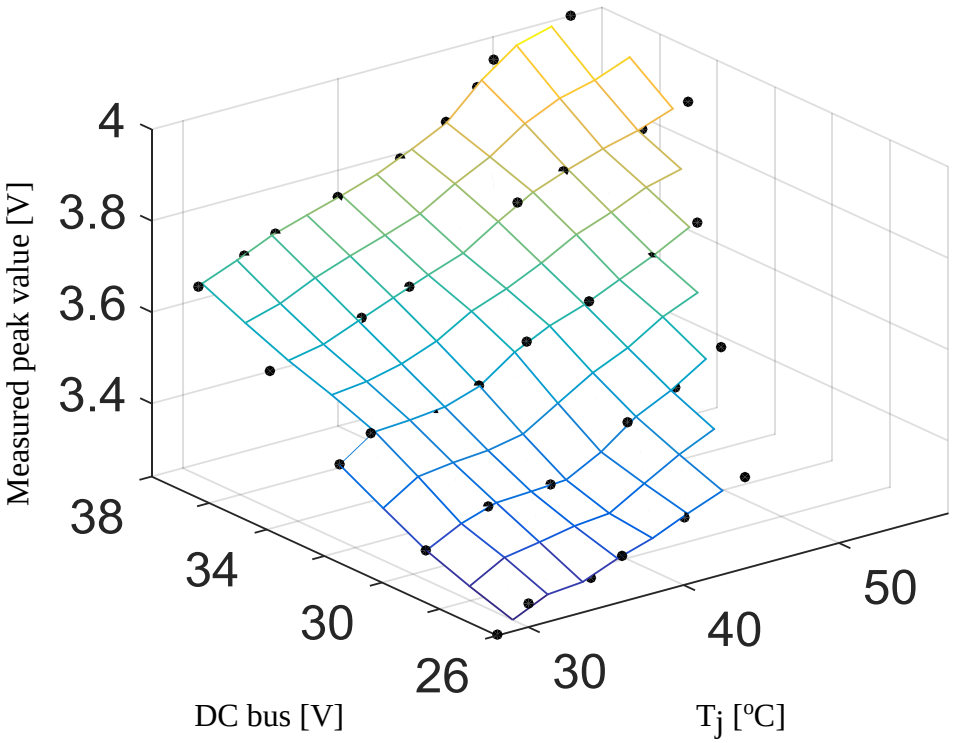


Fig. 9.1.1 Experimentally measured "iG peak vs. T_j vs. DC bus" relationship
Tests evaluated on half-bridge inverter configured with EPC2030 GaN HEMT

It can be seen from Fig. 9.1.1 that the measured peak is positively correlated to the DC bus voltage of the half-bridge inverter. In other power circuitry, if the on-state and off-state V_{DS} can vary during online operation, a 3-dimensional "peak vs. T_j vs. DC bus" relationship is required for the proposed online T_j sensing method.

9.2 The Effect of DC Bus Voltage Value on SiC MOSFET, with Different Gate Drive Topologies

Similar to GaN HEMT as discussed in section 9.1, the gate properties of SiC MOSFETs are also sensitive to the converter DC bus voltage (device bias voltage). In the case of a SCT2160KE SiC MOSFET driven by a push-pull gate drive as discussed in

section 8.1, to include the effect of the V_{DS} bias voltage in the proposed T_j sensing method, the 2-dimensional "$\int i_G$ vs. T_j" relationship (as shown in chapter 5) is extended to a 3- dimensional "$\int i_G$ vs. T_j vs. DC bus" relationship, as illustrated in Fig. 9.1.1. The "$\int i_G$ vs. T_j vs. DC bus" relationship is experimentally derived based on the method discussed in chapter 5 and chapter 6, with the DC bus varying from 130V to 290V, as illustrated in Fig. 9.2.1.

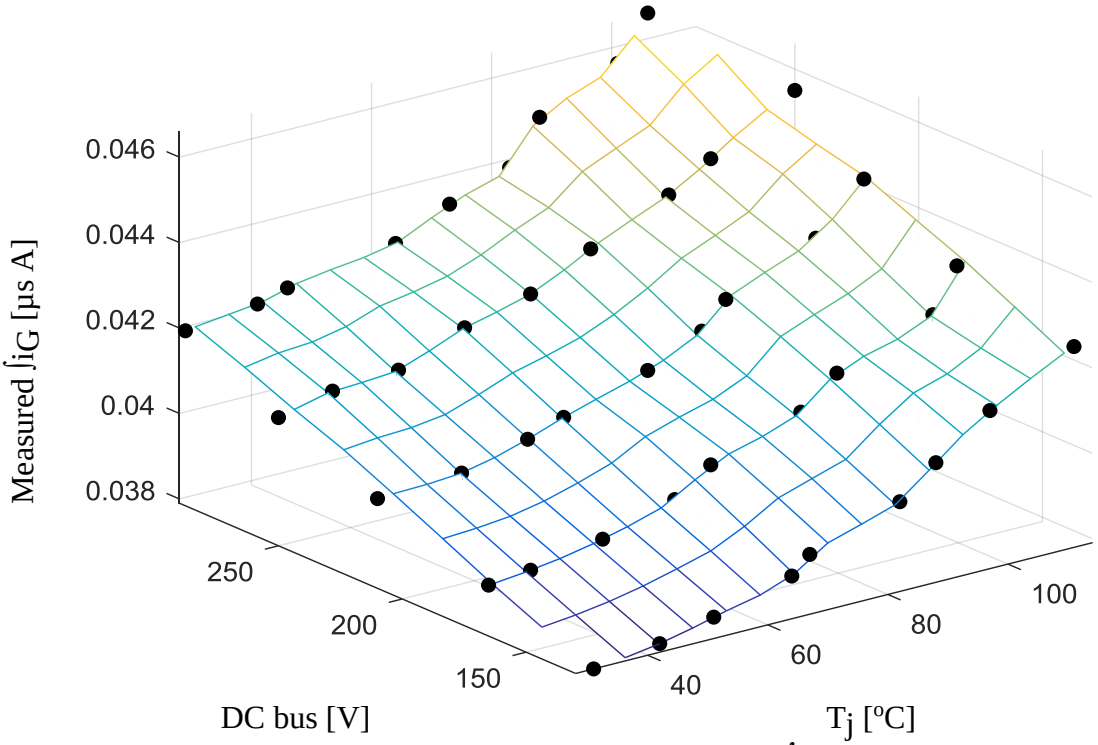


Fig. 9.2.1 Push-pull gate drive, experimentally measured "$\int i_G$ vs. T_j vs. DC bus" relationship
Tests evaluated on H-bridge inverter configured with Rohm SCT2160KE SiC MOSFET

It can be seen from Fig. 9.2.1 that the integration of the gate current is positively correlated to the DC bus voltage of the H-bridge inverter. Based on the "$\int i_G$ vs. T_j vs. DC bus" relationship, the effect of DC bus voltage must be considered if the variation of DC

bus value is larger than 30V in the case of a SCT2160KE SiC MOSFET driven by a push-pull gate drive.

In the case of a SCT2160KE SiC MOSFET driven by a current-mirror gate drive as discussed in section 8.2, to include the effect of the V_{DS} bias voltage in the proposed T_j sensing method, the 2- dimensional "$i_{G\ peak}$ vs. T_j" relationship (as shown in chapter 5) is extended to a 3- dimensional "$i_{G\ peak}$ vs. T_j vs. DC bus" relationship, as illustrated in Fig. 9.2.2. The "$i_{G\ peak}$ vs. T_j vs. DC bus" relationship is experimentally derived based on the method discussed in chapter 5 and chapter 6, with the DC bus varying from 130V to 290V, as illustrated in Fig. 9.2.2.

It can be seen from Fig. 9.2.2 that the measured peak is positively correlated to the DC bus voltage of the H-bridge inverter. Based on the "$i_{G\ peak}$ vs. T_j vs. DC bus" relationship, the effect of DC bus voltage must be considered if the variation of DC bus value is larger than 15V in the case of a SCT2160KE SiC MOSFET driven by a current-mirror gate drive.

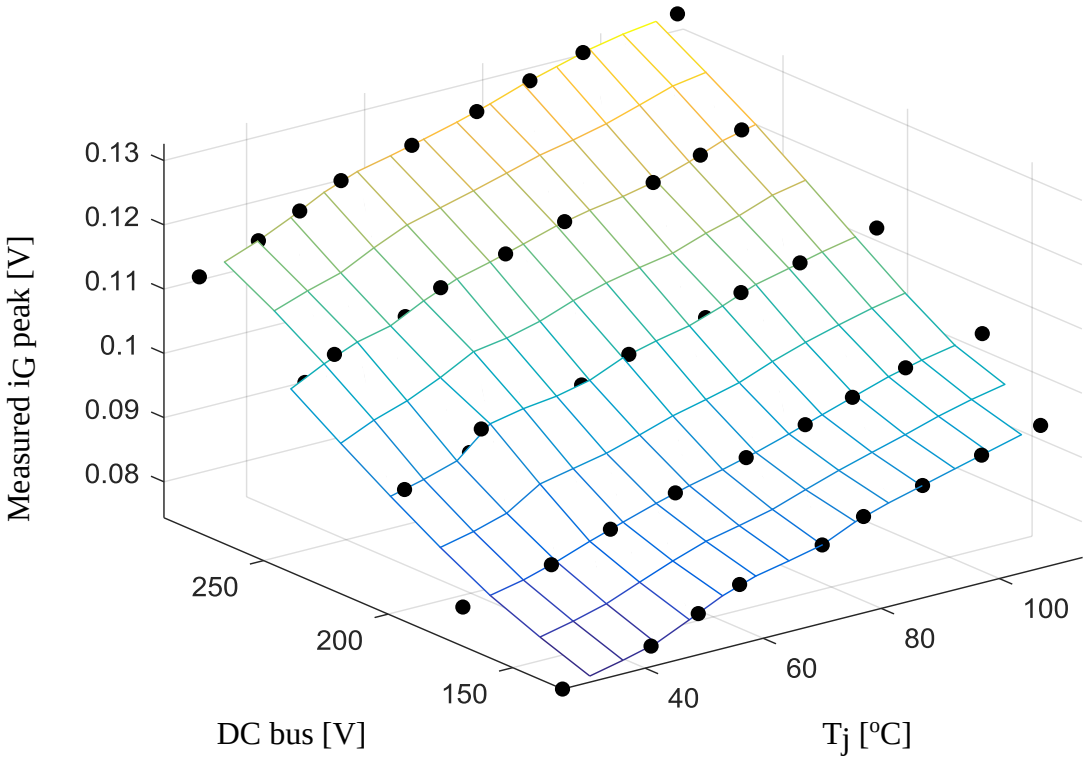


Fig. 9.2.2 Current mirror gate drive, experimentally measured "$i_{G\ peak}$ vs. T_j vs. DC bus" relationship
Tests evaluated on H-bridge inverter configured with Rohm SCT2160KE SiC MOSFET

In the case of a SCT2160KE SiC MOSFET driven by a inductor-based gate drive as discussed in section 8.3, to include the effect of the V_{DS} bias voltage in the proposed T_j sensing method, the 2- dimensional "$\int i_G$ vs. T_j" relationship (as shown in chapter 5) is extended to a 3- dimensional "$\int i_G$ vs. T_j vs. DC bus" relationship, as illustrated in Fig. 9.2.3. The "$\int i_G$ vs. T_j vs. DC bus" relationship is experimentally derived based on the method discussed in chapter 5 and chapter 6, with the DC bus varying from 130V to 290V, as illustrated in Fig. 9.2.3.

It can be seen from Fig. 9.2.3 that the integration of the measured gate currnet is positively correlated to the DC bus voltage of the H-bridge inverter. Based on the "$i_{G\ peak}$ vs. T_j vs. DC bus" relationship, the effect of DC bus voltage must be considered if

the variation of DC bus value is larger than 20V in the case of a SCT2160KE SiC MOSFET driven by an inductor-based gate drive.

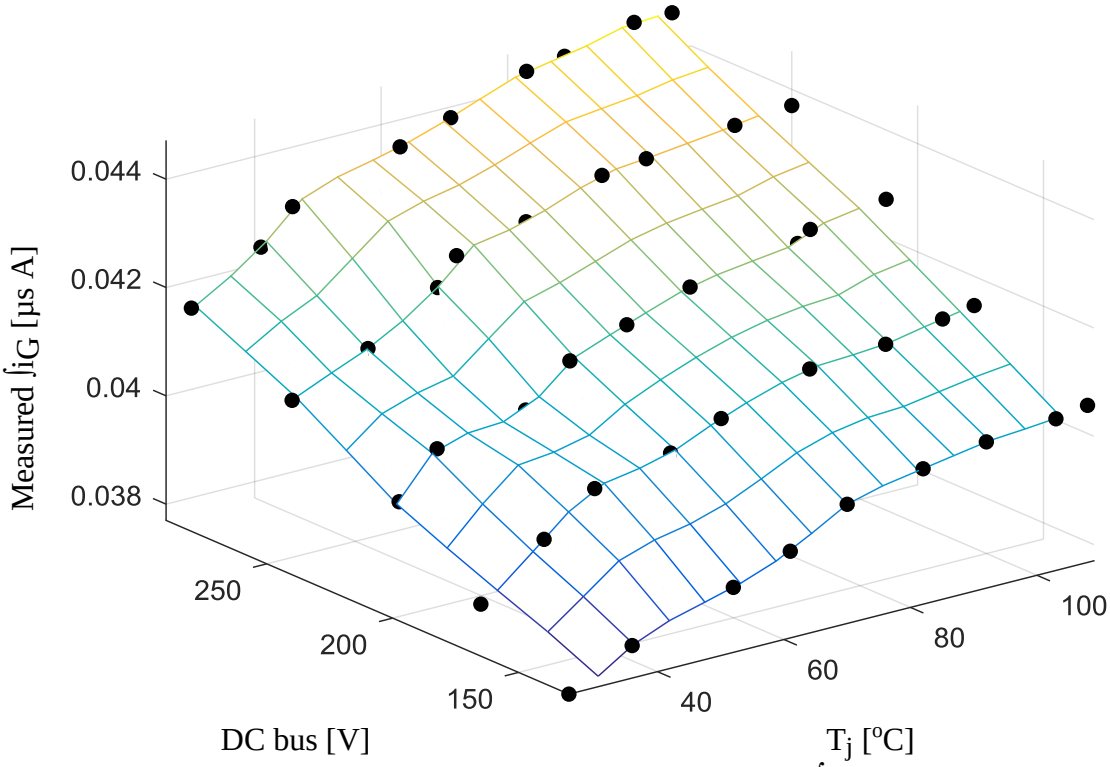


Fig. 9.2.3 Inductor based gate drive, experimentally measured "$\int i_G$ vs. T_j vs. DC bus" relationship
Tests evaluated on H-bridge inverter configured with Rohm SCT2160KE SiC MOSFET

9.3 The Effect of Load Inductive Properties on Si IGBTs

With the H-bridge inverter setup discussed in chapter 3, during the IGBT turn-on transient, the voltage stress across the device drain and source (V_{CE}) decreases from the DC bus voltage to almost zero. With an inductive load applied to the H-bridge, the turn current slope (di/dt) will be affected. This section investigate the effect of load inductive properties to the proposed T_j sensing method.

To include the effect of the load inductive properties, the H-bridge is loaded with a 10Ω-20μH, 10Ω-100μH, and 10Ω-350μH. The H-bridge switched at 10kHz, and same duty ratios are applied to both legs. The "$\int i_G$ vs. T_j vs. Load Properties" relationship is experimentally derived based on the method discussed in chapter 5 and chapter 6, as illustrated in Fig. 9.3.1.

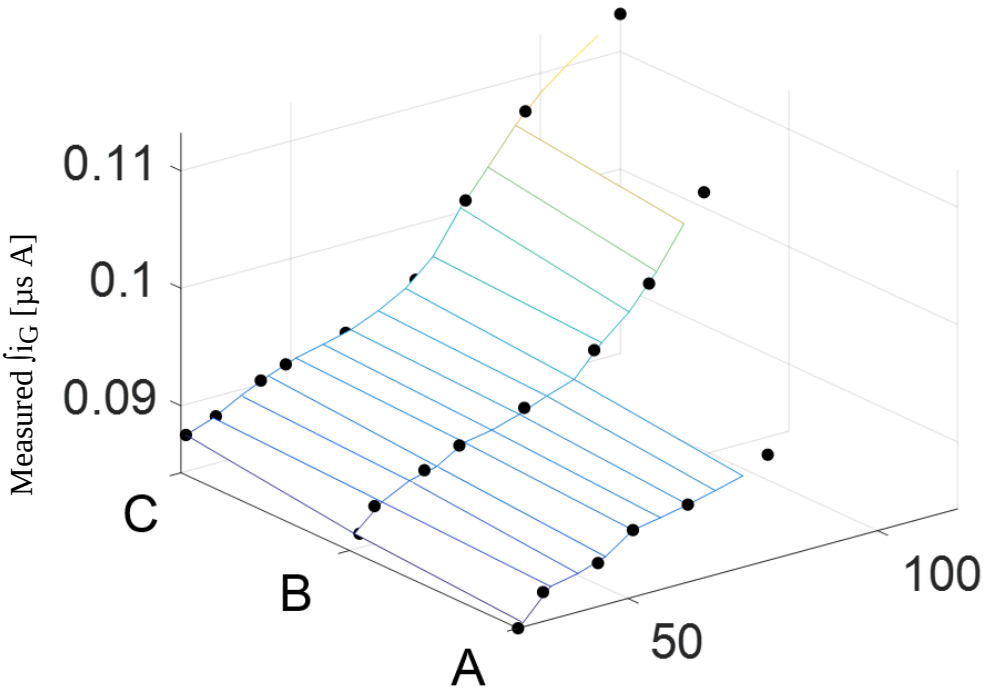


Fig. 9.3.1 Experimentally measured "$\int i_G$ vs. T_j vs. Load Properties" relationship
Tests evaluated on H-bridge inverter configured with Fuji 7MBR15SA140 IGBT module
Load Properties: A: 10Ω-350μH B: 10Ω-100μH C: 10Ω-20μH

It can be seen from Fig. 9.3.1 that when inductive load is applied to the H-bridge inverter, the "$\int i_G$ vs. T_j" relationship is affected by the load properties. In the aforementioned tests, with larger inductor used in the load, the value of $\int i_G$ is smaller under the same junction temperature. It can be observed from Fig. 9.3.1 that, when the inductor varies from 20μH to 350μH, the effect of load inductive properties is in-

significant.

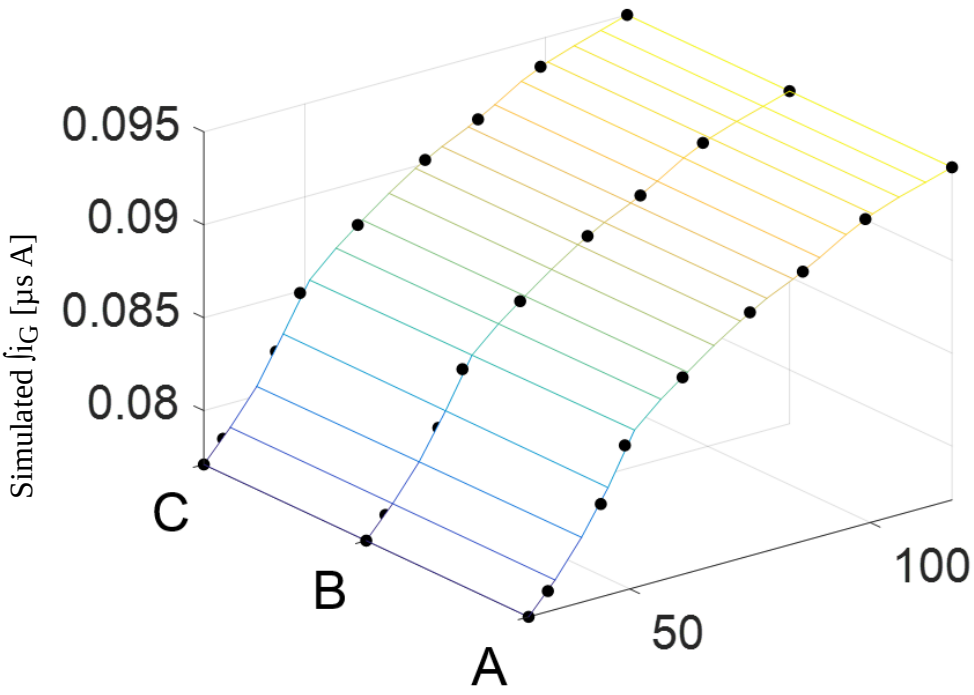


Fig. 9.3.2 Simulated "$\int i_G$ vs. T_j vs. Load Properties" relationship

Simulated with H-bridge inverter configured with Fuji 7MBR15SA140 IGBT module

Load Properties: A: 10Ω-350µH B: 10Ω-100µH C: 10Ω-20µH

The in-significant inductive load dependencies can be shown in simulation as well. In this section, 10Ω-20µH, 10Ω-100µH, and 10Ω-350µH loads are applied to H-bridge inverters configured with different types of devices. It can be seen from the simuation result in Fig. 9.3.2 that, when i_G integration is used for 7MBR15SA140 IGBT module T_j sensing, the effect of load inductive properties is in-significant.

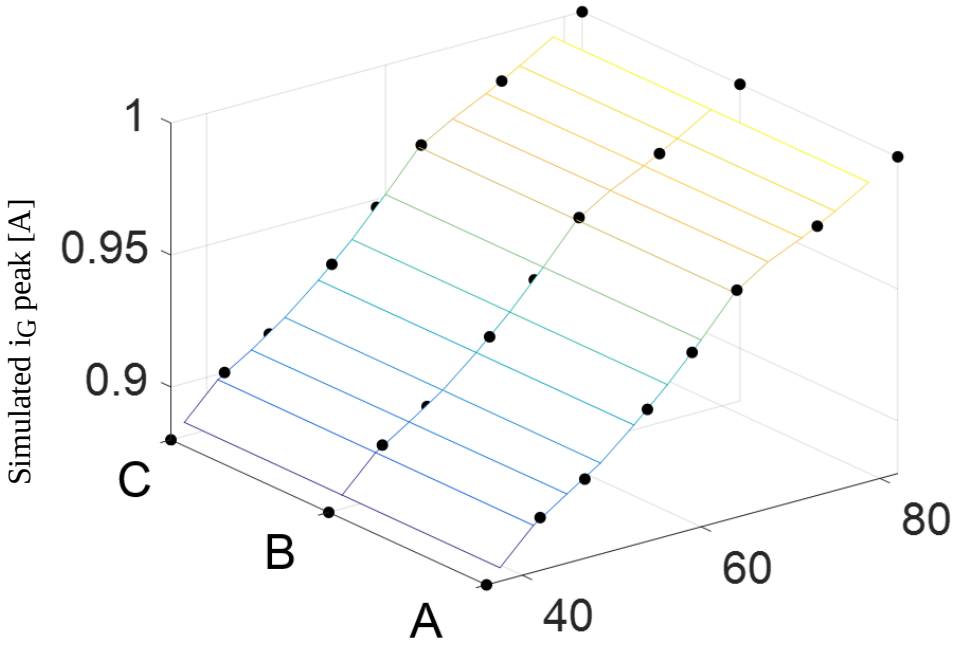


Fig. 9.3.3 Simulated "i_G peak vs. T_j vs. Load Properties" relationship
Simulated with H-bridge inverter configured with Fuji 2SK3677 MOSFETs
Load Properties: A: 10Ω-350μH B: 10Ω-100μH C: 10Ω-20μH

It can be seen from the simuation result in Fig. 9.3.3 that, when i_G peak detection is used for Fuji 2SK3677 MOSFETs T_j sensing, the effect of load inductive properties is in-significant.

9.4 Summary of the Effect of DC Bus Voltage and Load Inductive Properties

In this chapter, the effect of DC bus voltage and the effect of load inductive properties on the proposed T_j sensing method are explored. The 2- dimensional "i_G - T_j" relationships discussed in chapter 5 are extended to 3- dimensional "i_G vs. T_j vs. DC bus" relationships and 3- dimensional "i_G vs. T_j vs. Load properties" relationships.

When studying the effect of DC bus voltage, two types of devices (GaN HEMT and SiC MOSFET), three types of gate drives (push-pull gate drive, current mirror gate drive, and inductor-based gate drive), and two T_j extracting methods (peak detection and integration) are investigated. Depending on the types of gate drives/devices, when the variation of DC bus value exceeds a tolerable value, the 3-dimensional "i_G vs. T_j vs. DC bus" relationships should be used for the proposed T_j sensing method.

The effect of load inductive properties on the proposed T_j sensing method is evaluated on Si IGBT H-bridge. With larger inductor used in the load, smaller $\int i_G$ values are observed under the same T_j.

Chapter 10 Conclusions, Contributions, and Recommended Future Work

10.1 Research Conclusions

The following list summarizes the key conclusions offered by this research:

10.1.1 Conclusions from the state-of-the-art review

- Fast response sensing of the switching power semiconductor's temperature has been achieved with invasive methods such as diode-on-die technology.
- The switching power semiconductor's temperature sensitive electrical properties (TSEP) can be feasibly used for online semiconductor T_j sensing (estimation).
- Both device conduction properties and device switching transient properties are T_j sensitive, but the accuracy of conduction properties is more sensitive to T_j.
- The devices T_j dependency can be related to amplitude or temporal properties of the corresponding signals.
- Current measurements can be non-invasive to the power circuit, but voltage measurements are generally invasive.

10.1.2 Conclusions from the proposed T_j sensing methodology (Chaper 2, 3, and 4)

- For the gate signal, the turn-on transient signal is more sensitive to T_j compared with the on-state signal**.**

- In the power loop, the high frequency ringing decay is sensitive to T_j. In the gate drive loop, the turn-on transient properties are sensitive to T_j.
- The high frequency ringing decay in the power loop is difficult to extract online with simple signal processing.
- The gate drive turn-on transient output current is sensitive to the switching power semiconductor T_j.
- The gate drive turn-on output current transient can be measured inside the gate drive without invading the converter's power loop.

10.1.3 Conclusions for the "i_G - T_j" relationships and the temperature extraction methods (Chaper 5 and 6)

- The power semiconductor SPICE model used to estimate the "$i_G - T_j$" relationship should properly characterize the device's gate side T_j dependency.
- The simulation models provided by semiconductor manufacturers sometimes do not have enough gate side temperature properties, and dynamic properties.
- The gate drive circuit model used to estimate the "$i_G - T_j$" relationship should include detailed dyncamic properties of the gate drive output stage.
- The switching power semiconductor "$i_G - T_j$" relationship can be evaluated with simple signal processing like peak detection and integration.
- The selection of signal processing methods is based on the T_j sensitivity of the i_G waveforms.

- Accumulation based signal processings (averaging, integration) are usually better on noise decoupling compared with single point based signal processing (peak detection).
- The signal processing used to extract the "$i_G - T_j$" relationship can be implemented with high bandwidth op-amp, RF diodes, and proper parasitics in the gate drive.

10.1.4 Conclusions for different issues that can affect the power semiconductor "$i_G - T_j$" relationships (Chaper 7, 8, and 9)

- Si MOSFETs and GaN HEMTs have large "$i_G - T_j$" dependencies, while the "$i_G - T_j$" dependencies of Si IGBTs and SiC MOSFETs are small.
- Voltage-based gate drive, current-based gate drive, or resonant gate drive usually have different transient "$i_G - T_j$" relationships.
- The device chip surface emissivity and the chip vertical thermal gradients can affect the thermal camera calibration.
- The power semiconductor "$i_G - T_j$" relationship will change with DC bus voltage. A three-dimensional "DC bus – $i_G - T_j$" relationship can be used to include this effect.

10.2 Research Contributions

The following list summarizes the key contributions made by this research:

- **Developed a series of T_j sensing methodologies that are based on gate drive output current during device turn-on.**

  This work recognized that for some switching power semiconductors, the turn-on gate drive output current is T_j sensitive. The T_j dependency of the gate current

can be extracted online with high bandwidth signal processing, and used for online temperature estimation.

- **New models for different types of power semiconductor devices are developed with enhancement of the gate side T_j characterizations.**

  Several device temperature dependencies (especially the gate properties during turn-on transient) are not fully characterized by the simulation model from the semiconductor manufacturers. The temperature characterizations for junction capacitance, threshold voltage are added to improve the models for the devices' gate side T_j dependency. Models for Si MOSFET, Si IGBT, SiC MOSFET, and GaN HEMT are developed in this research.

- **New models for different types of gate drives are developed with enhancement of output power stage modeling and parasitics modeling.**

  The turn-on dynamic model for push-pull output based voltage source gate drive, current mirror based current source gate drive, and inductor based current source gate drive are developed with enhancement of models for output stage switching properties and parasitics.

- **Created a series of "$i_G - T_j$" relationships based on simulations and prototype tests.**

  Based on the aforementioned switching power semiconductor model and the gate drive model, the "$i_G - T_j$" relationships for different combinations of "semiconductor – gate drive" are derived from simulations. Those simulated "i_G - T_j" relationships are also evaluated in prototype tests. By configuring the test

switching power semiconductor in different power converter topologies, the device junction temperature can be manipulated by setting the duty ratio of the DUT. All the test switching power semiconductors are open samples, thus a Flir thermal camera can be used to measure the semiconductor's chip surface temperature.

- **Developed a methodology to calibrate the "$i_G - T_j$" relationship experimentally.**

  The MOSFET "$R_{DS\text{-}on} - T_j$" relationships and IGBT "$V_{CE} - T_j$" relationships are usually provided by the semiconductor manufacturers. By measuring the power MOSFET $R_{DS\text{-}on}$ or IGBT V_{CE}, T_j can be estimated with invasive measurement. This invasive method can be used to calibrate the "$i_G - T_j$" relationships derived from the gate current and the thermal camera.

- **Provided several high bandwidth singal processing circuits to extract the device T_j dependency online from the gate drive output.**

  Depending on the combination of "gate drive – switching power semiconductor", a peak detection circuit or an integration circuit can be used to extract the turn-on i_G waveform T_j dependency. Several circuit topologies for peak detection and integration have been studied and evaluated. Control switches are implemented in the circuit to activate signal processing and hold the processed signal.

- **Identified the limitations of the proposed gate drive turn-on current transient based T_j sensing method.**

  Firstly, for different devices from the same batch, inconsistant gate turn-on properties can affect the accuracy of the proposed T_j sensing method. Secondly,

inconsistant layout and output characterisitics of the gate drives can affect the accuracy of the proposed T_j sensing method as well.

- **Provided a methodology to estimate the tolerance of the proposed non-invasive, online T_j sensing method.**

  The repeatability test indicates a less than 10^oC T_j sensing tolerance for the proposed T_j sensing method on a wide range of devices.

- **Presented the effect of thermal operating point on the proposed non-invasive, online T_j sensing method.**

  By changing the heat-sinking capability of the tested switching power semiconductor, the thermal operating points of the prototype are manipulated. Evaluation shows that the proposed T_j sensing method is independent of device thermal operating point.

- **Theoretically investigated the effect of device vertical temperature gradient on the proposed online T_j sensing method.**

  With the power semiconductor thermal dynamic model and proper estimation of converter ambient condition, the three-dimensional temperature distribution of the device can be derived. For all the power semiconductors evaluated in this research, the temperature differences between the device surface and the device junction area are less than 1^oC.

- **Provided the effect of the DC bus voltage value on the proposed T_j sensing method.**

The power semiconductor's "$i_G - T_j$" relationships are evaluated under different DC bus voltages. For those "$i_G - T_j$" relationships sensitive to the DC bus voltage, a three-dimensional "DC bus – i_G – T_j" relationship was used instead for the proposed T_j sensing method.

10.3 Recommended Future Work

Based on the work discussed in this thesis, the following topics are recommended for future work:

- **Evaluate the device design features that could be used to enhance non-invasive online T_j sensing method without degrading power processing capability.**

  The semiconductor design properties that affect these methods of T_j sensing are predominately the gate charge (Q_g) and the threshold voltage (V_{TH}). Device design to enhance these properties could be investigated to see if synergy between design-for-sensing and design-for-power processing could be achieved.

- **Optimize the parasitics and power rating of the T_j sensing setup by integrate the gate drive circuit and the sensing circuit on the same semiconductor die.**

  The to-date T_j sensing setup is built with discrete components. The bandwidth of the analog signal processing circuit is limited by the parasitics and the performance of the op-amp and the analog switches. The current rating of the op-amp and the analog switches should be reduced to limit their junction capacitance.

- **Investigate the proposed non-invasive online T_j sensing method on more of the commonly used gate drive topologies.**

The work to-date has evaluated the proposed T_j sensing method on the push-pull output based voltage source gate drive and current mirror based current source gate drive, and inductor based current source gate drive. In the future work, the charge pump based voltage source gate drive, resonant gate drive, etc. are recommended to be evaluated with the proposed T_j sensing method.

- **Investigate the closed-loop gate drive with the proposed T_j sensing methods.**

  It is recommended to evaluate the proposed T_j sensing methods, if the gate drive output current/voltage is controlled in closed-loop during the turn-on transient. In addition, the future work might consider using the information in the closed-loop controller to improve the proposed online T_j sensing methods.

- **Fully investigate the the proposed T_j sensing methods with different load di/dt in the device full T_j operating range.**

  This research investigate the effect of load di/dt with some experimental tests and simulations. It is recommended in the future work that a wide range of load di/dt can be evaluated under full Tj operating range with different types of devices, different types of gate drives, and different signal processing methods.

- **Investigate the proposed T_j sensing methods when using i_G peak detection and i_G integration at the same time for signal processing.**

  In some "gate drive – semiconductor" combinations, both i_G peak detection and i_G integration can be used to extract the T_j sensitivity online. It recommended to investigate the proposed T_j sensing methods with combined i_G peak detection and

i_G integration signal processing. It is possible that with the combination of the two signal processings, the proposed T_j sensing method can have impoved sensing accuracy.

- **Evaluate the temperature consistency of the gate drive output characterisics when using the proposed non-invasive online T_j sensing method.**

  The output characteristics of an integrated gate drive can be sensitive to gate drive temperature. Although the gate drive circuits are not significantly warmed up during converter operation, it is still reommended to evaluate the proposed Tj sensing method under different gate drive temperatures. If i_G is sensitive to the gate drive temperature, the online calibration concering the gate drive temperature should be included.

- **Actively limit the ΔT_j of the switching power semiconductors of a power converter in a prototype test, commanding the load current trajectories to the converter with limited ΔT_j for all the semiconductors.**

  The proposed non-invasive online T_j sensing method will be used on a power converter to limit the ΔT_j of the switching power semiconductors. The sensed load current and the sensed T_j will be fed back to the PWM controller in order to control the load current with limited ΔT_j.

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