Design of Multilevel Integrated Modular Motor Drive with Gallium Nitride Power Devices

By

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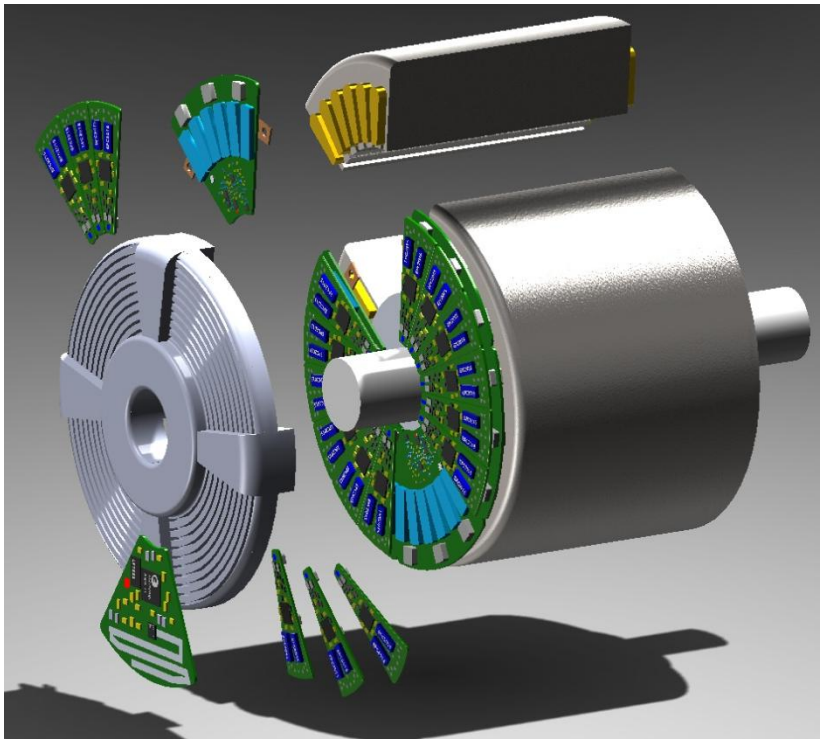
Abstract



Integrated modular motor drive (IMMD) is a concept that integrates both the motor and the drive into a single package. Without extra connecting cables and drive cabinet, the drive system can achieve higher power density and better integration with plug&play capability. However, the physical integration of motor drive and the machine poses many challenges, including thermal management and size minimization. The concept of multilevel converter is able to reduce voltage stress on semiconductor devices, and consequently, provides higher efficiency. This greatly reduces the difficulty of thermal management. However, traditional multilevel topologies have extra inductors, transformers or bulky capacitors and cannot meet the size requirement of IMMD.

In this thesis, a multilevel topology is proposed to realize IMMD. Similar to other multilevel topologies, the proposed one utilizes semiconductor devices with lower voltage stress and better efficiency. Different from other multilevel topologies, the proposed one treats the machine as a

critical magnetic component to provide galvanic isolation, so there is no extra transformer or inductor in the proposed topology. Consequently, the size, weight and cost of the converter can be reduced. It is also proposed in this thesis to build an IMMD with wide bandgap gallium nitride (GaN) field effect transistors (FETs) to deal with the high temperature environment inside machine housing. In addition, GaN FETs can achieve a higher switching frequency that allows further reduction of capacitor size.

This thesis will present technical details of the proposed multilevel topology, including topology comparisons, component sizing and machine winding configurations. To give a better understanding of the converter dynamic, both the analytical model of machine windings and control algorithms are presented. Evaluations of capacitors are also provided to minimize the capacitor size for a machine drive. In addition, this thesis includes various hardware design experiences. A 4-module (i.e. equivalent 5-level) prototype converter with indirect field oriented control (IFOC) is designed and it validates the proposed multilevel concept. An optimized IMMD physical structure is proposed to minimize the size and thickness of the design. Experiment results and design experience of a GaN FETs IMMD are also presented. Through four generations of hardware design, this thesis proves that the proposed multilevel topology and GaN FETs can realize an IMMD with higher power density and fully physical integration.

Acknowledgement

I would like to thank my advisor Professor Yehui Han, for his guidance and support of my graduate research at Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC). His enthusiasm in power electronics and patience always inspire me to pursue the best and face challenges with courage.

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It is my great pleasure to spend my graduate life with all WEMPEC family. WEMPEC faculties are giving very comprehensive and arranged lectures in power electronics, controls, electric machines and power grids. I've also enjoyed the great collaboration with WEMPEC sponsors and other WEMPEC students. In this inspiring research atmosphere, I gain so much experience beyond my own research. Great thanks to all my friends in USA and China, for the pleasant time we spent together.

Finally, I would take this opportunity to express my appreciation to my parents Li Li and Enzhi Wang for their understanding and support. I would like to extend my sincere gratitude and best wishes to them.

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Nomenclature

Symbol

n	number of voltage levels in a multilevel converter
V_{dc}	DC-link voltage
n_i	concentration of intrinsic carriers
f_{sw}	switching frequency
Δi_{dc}	converter module input current ripple
i_c	capacitor current
Δv_{dc}	DC-link voltage ripple
i_{dc}	converter module input current
P	the number of machine poles
P_{park}	Park transformation matrix
i_a , i_b , i_c	the a-b-c-axis currents
v_a , v_b , v_c	the a-b-c-axis voltages
i_d , i_q , i_0	the d-q-0-axis currents
v_d , v_q , v_0	the d-q-0-axis voltages
i_{xk}, x = a,b,c,d,q,0	the x-axis current of motor segment #k
v_{xk}, x = a,b,c,d,q,0	the x-axis voltage of motor segment #k
M_r	the decoupling time variant row operation matrix
ω	the speed of reference frame
θ	the angle of reference frame
V_k	the DC voltage of converter module #k
I_k	the DC current of converter module #k

Abbreviations

2DEG	2 dimensional electron gas
ASD	adjustable speed drive
BFoM	Baliga's figure of merit
CHB	cascaded H-bridge
CSI	current source inverter
CVB	centralized voltage balancing
DC	direct current
DVB	distributed voltage balancing
FC	flying capacitor
FET	field effect transistor
GaN	gallium nitride
GTO	gate turn off thyristor
IFOC	indirect field oriented control
IGBT	insulated gate bipolar transistor
IGCT	integrated gate commutated thyristor
IMMD	integrated modular motor drive
MMC	modular multilevel converter
MMF	magnetomotive force
MOSFET	metal oxide semiconductor field effect transistor
MV	medium voltage
NPC	neutral point clamped
PCB	printed circuit board
PWM	pulse width modulation
SiC	silicon carbide
SVPWM	space vector pulse width modulation
WBG	wide bandgap

Introduction

Research Overview

The objective of this research is to design an integrated modular motor drive that achieves higher power density and better integration with plug&play capability. This requires the motor drive design to have high efficiency and small size.

In this research, an input-series multilevel topology and Gallium Nitride power FETs are proposed to realize the integrated modular motor drive. Key concepts and techniques to realize such a system will be covered in this research.

Summary of Chapters

Chapter 1 presents the state of the art review of multilevel converters, wide bandgap semiconductor power devices and integrated modular motor drive. Based on the reviews, research opportunities are identified.

Chapter 2 introduces the proposed multilevel converter topology. Technical details and comparisons of the proposed converter are presented.

Chapter 3 develops the analytical model of the split machine segments and investigates different voltage balancing methods. Both simulation and experiment results are presented to validate the proposed multilevel converter.

Chapter 4 presents the capacitor evaluations. Since capacitor is typically the largest component in a machine drive, it is very important to optimize the selection of capacitor and to minimize capacitor size. This chapter will also provide comparisons of capacitor size at different switching frequencies.

Chapter 5 introduces gate signal interleaving technique for the proposed multilevel converter. This technique can reduce DC-link voltage ripples and common-mode voltage. Both simulation and experiment results validate the technique.

Chapter 6 presents the prototype hardware design with 4 converter modules. Experiment results validate the proposed multilevel concept in this thesis. The results also prove that the multilevel converter can be controlled easily and extended with great flexibility.

Chapter 7 presents the hardware design of an IMMD, along with the PCB design for Gallium Nitride power FETs.

Chapter 8 concludes the thesis and summarizes the contributions of this research. This chapter also includes recommended future work.

Chapter 1

State of the Art Review

The first part of this chapter presents the state of the art review of existing multilevel topologies for motor drive. These topologies are classified into three categories according to their DC-link capacitor connections. Wide bandgap (WBG) semiconductors are briefly reviewed in the second part of this chapter. Several existing WBG products, including GaN and SiC are introduced. Thirdly, integrated modular motor drive (IMMD) is reviewed, following by the discussions of its advantages and challenges. At the end of this chapter, based on the review of multilevel topologies, WBG semiconductors and IMMD, research opportunities are identified.

1.1 Multilevel Converter Motor Drives

1.1.1 Introduction

In recent years, there has been increasing attention given to the efficiency of energy conversion since electric motors utilize 45 percent of global electricity. Increased energy efficiency in electric motors will provide tremendous economic, environmental, human ecological, and security benefits.

Grid tied motors are operating at a fixed rotating speed and lack of control ability. In applications such as compressors in air conditioners, the grid tied motors are either turned on at full speed or completely shut down. The on-off operating cycle not only increases the power loss, but also reduces the life span of mechanical parts.

An adjustable speed drive (ASD) is a power electronic device that controls the speed of motor. They are found very appealing because of their efficiency and controllability. ASDs also improve building efficiency and save energy for industry processes that require adjustable speed or control of flow from a fan or pump. ASDs have already replaced many conventional fixed-speed drives in low-power and low-voltage applications such as air conditioners, washing machines, electric bicycles, and small vehicles with stepless speed change, making up a large portion of the market. For high-power and medium-voltage (MV) applications including industrial air compressors, water pumping stations, cooling fans, railway traction systems, steel rolling mills, marine propulsion, and renewable energy systems, ASDs are even more attractive because the cost saving from electric power is even more significant than it is in low-voltage and low-power applications. MV products are generally considered to be in the voltage range of 2.3 kV to 6.6 kV and in the power range of 1 to 50 MW [1]. At such voltage and power levels, the investment payback time for ASDs is only 1.0 to 2.5 years [2].

The MV ASDs could be realized by current-source-inverter (CSI) using gate-turn-off thyristor (GTO) rated as high as 6 kV. Limited by the performance of MV GTO, CSI leads to low power quality, high harmonic components and thus causes extra loss. Also, the high dV/dt in the system will accelerate the wear of insulation layer and shorten the insulation lifespan, which is known as the major factor in motor service life. Considering the high switching loss of GTO, the system is usually operating no more than several hundred Hz. It is also possible to connect the lower voltage semiconductor switches in series in order to get a higher voltage rating. Extra auxiliary circuits are needed to guarantee the switches turn on and off simultaneously [3].

Multilevel converters are a preferred solution for adjustable-speed medium-voltage motor drives. The concept of multilevel converter is to synthesis several DC voltage sources (or DC

capacitors) to get an output with higher voltage. With proper multilevel topology, semiconductor switches are clamped by the DC voltage sources (or DC capacitors) and it is guaranteed by the topology that the voltage on each switch is within the limit. In other word, semiconductor switches can operate at a lower voltage than the total input or output voltage of the ASD. Several switches are equivalently connected in series to achieve the higher voltage. Compared to conventional two-level converters or CSI using high power switches such as GTOs, multilevel converters improve the quality of output voltage waveforms and reduce the total harmonic distortion. The following figure shows the typical output waveforms of a conventional two-level converter and a 5-level multilevel converter.

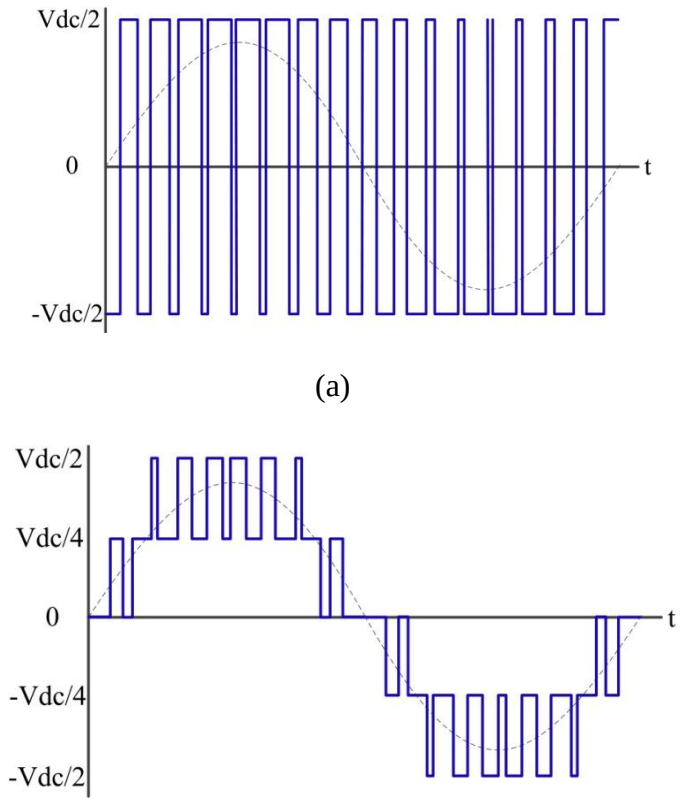


Fig. 1.1. Typical output waveforms
(a) two-level converter, and (b) 5-level multilevel converter

A two-level converter can perform a pulse width modulation (PWM) based on two voltage levels, i.e., the output voltage can either be $-V_{dc}/2$ or $V_{dc}/2$. The semiconductor switches used in a two-level converter must have a voltage rating of V_{dc}. By comparison, the 5-level converter can output 5 voltage levels, i.e., $-V_{dc}/2$, $-V_{dc}/4$, 0, $V_{dc}/4$ and $V_{dc}/2$. The rating voltages of these semiconductor switches are only $V_{dc}/4$. In total, at most 4 switches are equivalently connected in series to handle the total voltage V_{dc}. With more voltage levels, the waveform is more close to the desired sinusoidal output. In theory, the harmonic distortion is zero when the number of voltage levels is infinity.

With more voltage levels, the voltage of each level is decreasing and so does the voltage stress on semiconductor devices. At lower voltage stress, a large variety of less expensive, high-performance semiconductor devices can be selected including metal-oxide-semiconductor field-effect transistors (MOSFETs), insulated-gate bipolar transistors (IGBTs) and integrated gate-commutated thyristors (IGCTs). Using these high-performance semiconductor devices, multilevel converters can improve performance, increase efficiency, and reduce the overall cost. The cost per kilowatt of a MV ASD is at least five times the cost per kilowatt of a present-day 480 V ASD [4].

In applications where the semiconductor devices are FETs, it is beneficial to decrease the voltage rating. This is because the on-resistance of a FET increases much faster than the rating voltage. Several low voltage FETs connected in series will have a smaller on-resistance compare to a single FET that can handle the total voltage. Multilevel converter can utilize more FETs at low voltage, and hence the conduction loss will decrease significantly.

Since the first multilevel converter was invented in the late 1960s [1], multilevel converters have evolved over nearly a half-century. Some topologies have been successfully commercialized and have a wide range of applications in motor drives. Brief reviews of multilevel converters are presented in [5][6][7][8][9]. In the next section, existing multilevel motor drives are classified into three categories according to their DC-link capacitor connection.

1.1.2 Non-modular Clamping Topologies

Neutral Point Clamped (NPC) and Flying Capacitor (FC) are considered as very classic topologies because they have been commercialized for industrial products and widely used for decades [1].

Fig. 1.2 shows a 3-phase, 3-level NPC converter [10] with half of the DC-link voltage on each of the capacitors. The voltage ratings of the diodes and switches in a 3-level NPC converter are also half of the DC-link voltage. The diodes provide paths for AC current to flow and clamp the switch voltages. To avoid an over-voltage on a switch, certain switching patterns should be followed. The DC capacitors will clamp the voltage of the switches. [11]

In general, an n+1 level NPC converter typically consists of n series capacitors with a voltage rating of V_{dc}/n. All switches and diodes are also rated at V_{dc}/n. To properly clamp the switch voltages, several diodes are connected in series between any two different levels. As a result, the number of diodes in an n+1 level, 3-phase NPC converter is 3n(n-1), yielding a quadratic growth as a function of n. The 3-level NPC converter is popular because of a simple front-end rectifier design and lower device count. When the number of levels is more than three, the unequal power provided by each level will cause unbalanced capacitor voltages. In theory, the basic NPC converter can only provide reactive power, so to supply real power and balance

the capacitor voltages, the NPC converter must be paired with a front-end AC-DC converter which provides the exact amount of required real power [12]. Moreover, with more than three levels, the device stresses in NPC are also unequal and consequently, switching devices are overdesigned and incur extra losses and cost.

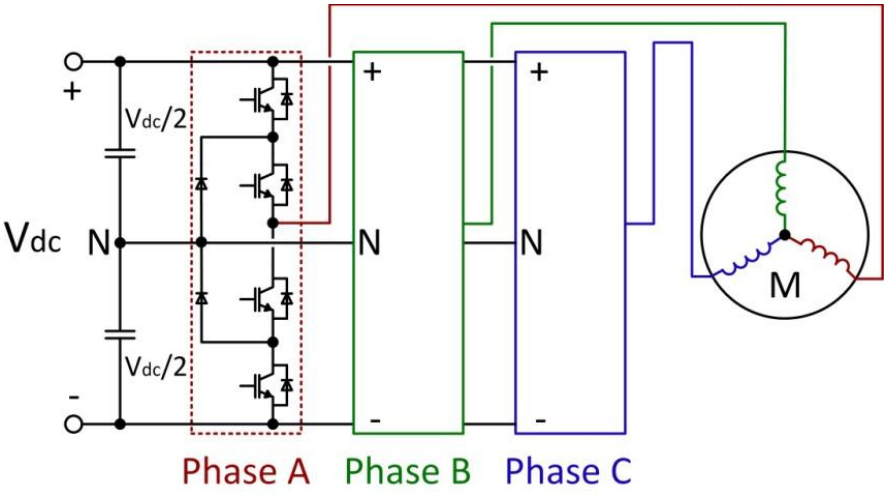


Fig. 1.2. 3-level 3-phase neutral point clamped (NPC)

The FC topology, as illustrated in Fig. 1.3, was introduced in 1970s [13]. The capacitors between switches are floating and clamp the switch voltages. In general, an n+1 level FC converter has n DC-link capacitors and 3n(n-1)/2 flying capacitors. Although an FC converter can provide real power and has a simple front-end rectifier design, the voltage of flying capacitors are not balanced when the switches have different turn-on turn-off delays [14]. Switching patterns are required in order to balance the capacitor voltages. One of the effective methods to balance the voltages is phase shifted sinusoidal PWM. It creates a combination of different output voltage levels in one fundamental cycle to balance the charge and discharge of each flying capacitor [15].

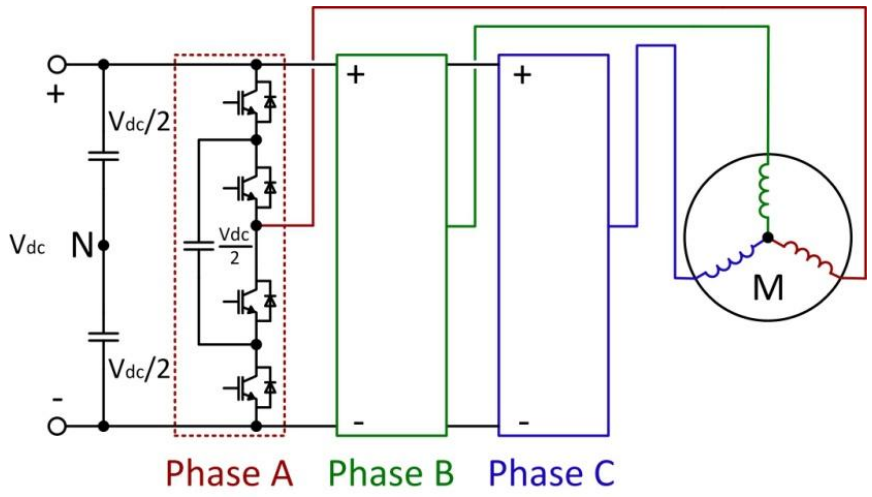


Fig. 1.3. 3-level 3-phase flying capacitor (FC)

In this thesis, NPC and FC are classified as 'clamping topologies' because these two classic topologies have many properties in common. A generalized topology is proposed in [16], from which NPC and FC topologies can be developed. The common properties of these two topologies are listed as follows.

- Several DC-link capacitors are connected in series at the DC input. If there are n DC-link capacitors, all the components will have the voltage rating V_{dc}/n.
- n switches are connected in series. Voltage on each switch is guaranteed to be V_{dc}/n by the clamping topology.
- There are total n+1 output voltage levels, i.e.,

$$V_{out} = -\frac{V_{dc}}{2n} + k \cdot \frac{V_{dc}}{n}, \qquad k = 0, 1, 2, \dots, n \tag{1.1}$$

- The number of clamping diodes or flying capacitors is a quadratic growth as a function

of n. Hence n is usually limited to 3, 5 or 7. A converter with a large n is almost unpractical to build because the component quantity will be large and the topology will be too complicated.

1.1.3 Modular Topologies with Multiple Inputs

Compare to the clamping topologies, topologies with multiple inputs utilize transformers and inductors to generate multiple isolated DC voltage inputs. Since the DC inputs are isolated, the output voltage levels can be synthesized directly via connecting the DC inputs in series.

Cascaded H-bridge (CHB) is the most representative topology in this category, as shown in Fig. 1.4. This topology was introduced in 1960's in [17] and became more related to industrial applications in 1990's [18]. There are no extra clamping diodes or flying capacitors in a CHB converter. Each H-Bridge can provide 3-level outputs: $-V_{dc}/n$, 0, and V_{dc}/n. The output terminals of H-bridges are connected in series, leading to a superposition of the output voltages from each H-bridge. [19] presents an example of CHB used for grid interface wind power alternator. A 2n+1 level CHB converter consists of n H-bridges in each phase, from which it is possible to generate an output voltage of $\pm kV_{dc}/n$ (k from 0 to n). Since a CHB converter does not have clamping capacitors or diodes that lead to a quadratic growth with the number of levels n, it is possible to construct a CHB converter with more output voltage levels [1]. Voltage balancing technique is introduced in [20] to keep the module voltage to be equal. The CHB converter has drawn significant attention because of its modular structure, and the component quantity is a linear increase as n. However, there are also disadvantages associated with CHB converters. First, CHB converters are supplied by isolated voltage sources or phase shift transformers for each bridge. The required number of individual voltage sources or transformer

windings is 3n. An 18 or 24-pulse rectifier system can be used to supply a CHB converter and improves the power quality but it is complicated and more expensive [21]. Second, each H-bridge only supplies a single-phase module and the instantaneous power from the input DC source is fluctuating. This inevitably requires extra power buffering capacitance and physically oversized DC capacitors.

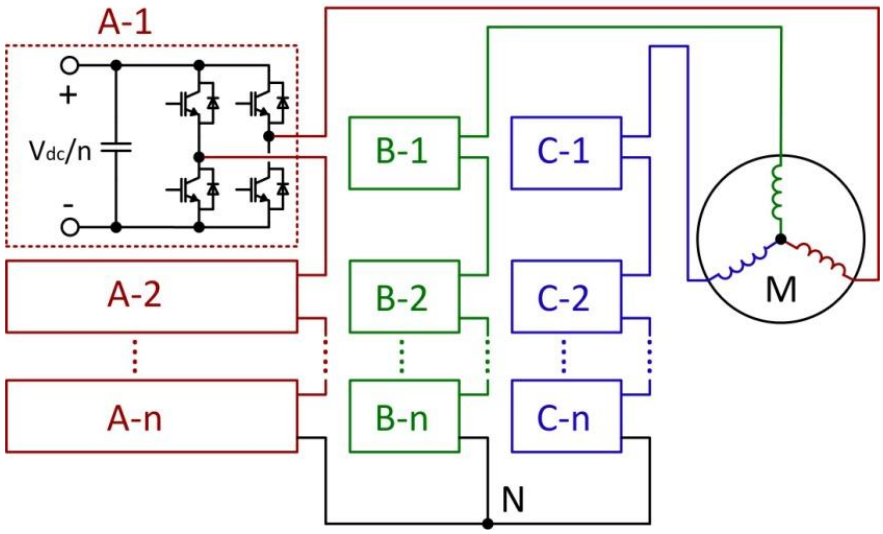


Fig. 1.4. 2n+1 level cascaded H-bridge (CHB)

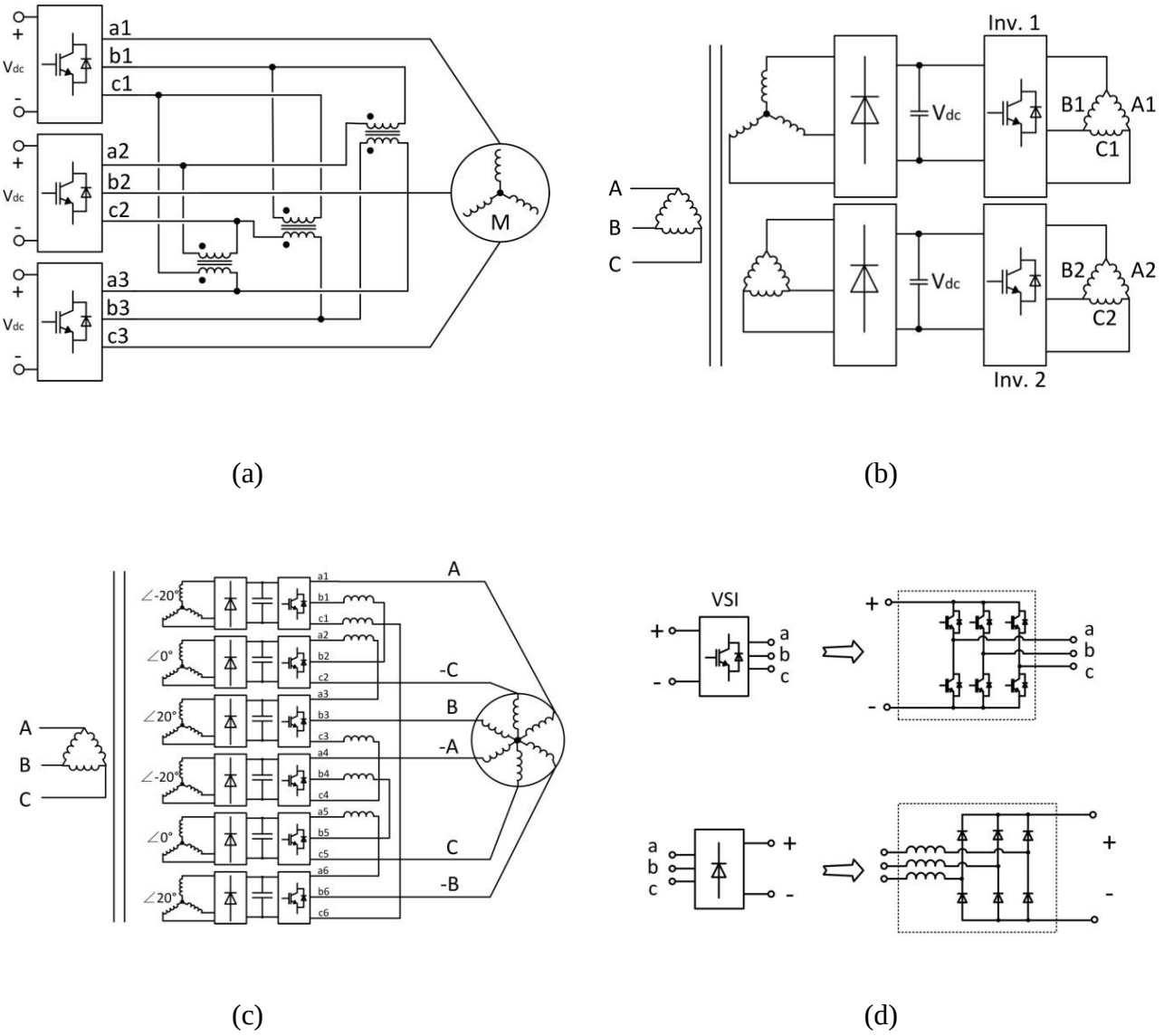


Fig. 1.5. Topologies with multiple DC inputs
(a) topology with 3 inputs and 3 transformers [4],
(b) topology with 2 DC inputs supplied by a multi-winding frontend transformer [22],
(c) hexagram converter with 6 inductors and a multi-winding frontend transformer [23],
and (d) the configuration of converter/rectifier modules

Several recent topologies can solve some problems of CHB converters, as shown in **Fig. 1.5**.

Instead of having one individual DC source for each single-phase bridge, the topology shown in

Fig. 1.5(a) [4] only requires one individual DC source for each three-phase bridge. The capacitor size is reduced because the three-phase topology has little power fluctuation. However, extra transformers, which inevitably increase the cost, size, and loss, are needed in this topology to combine the output voltages from each bridge. The same authors proposed another multilevel converter topology without combining transformers [22]. The topology is shown in **Fig. 1.5**(b) and it utilizes the machine winding properties. Standard windings of an MV motor can be reconnected into several three-phase groups, but meanwhile the electrical and mechanical properties of the motor are maintained. Each winding group is driven from a separate three-phase inverter. The output voltages of the inverters are combined by the machine windings instead of transformers. However, each inverter still needs an isolated voltage source, and the front-end rectifier and input transformer are expensive and complex.

Proposed in [23] and shown in Fig. 1.5(c), a hexagram multilevel converter consists of six 3-phase inverter bridges interconnected through inductors. The six output terminals of the hexagram converter are connected to an open-winding, 6-lead machine. The voltage stresses on each inverter are further decreased and allow for the use of lower-voltage semiconductor devices with better switching characteristics. The hexagram multilevel converter is a three phase modular design, which is easy to maintain and construct and has a lower DC capacitance requirement than a CHB converter. However, this topology not only requires isolated voltage sources, but also needs extra inductors. Moreover, certain switching patterns are prohibited in order to prevent circulating current between different inverter modules.

The common properties of these topologies are:

- n DC-link capacitors are independently supplied by n isolated DC voltage inputs. Typically it needs a dedicated front-end multilwinding transformer to provide these

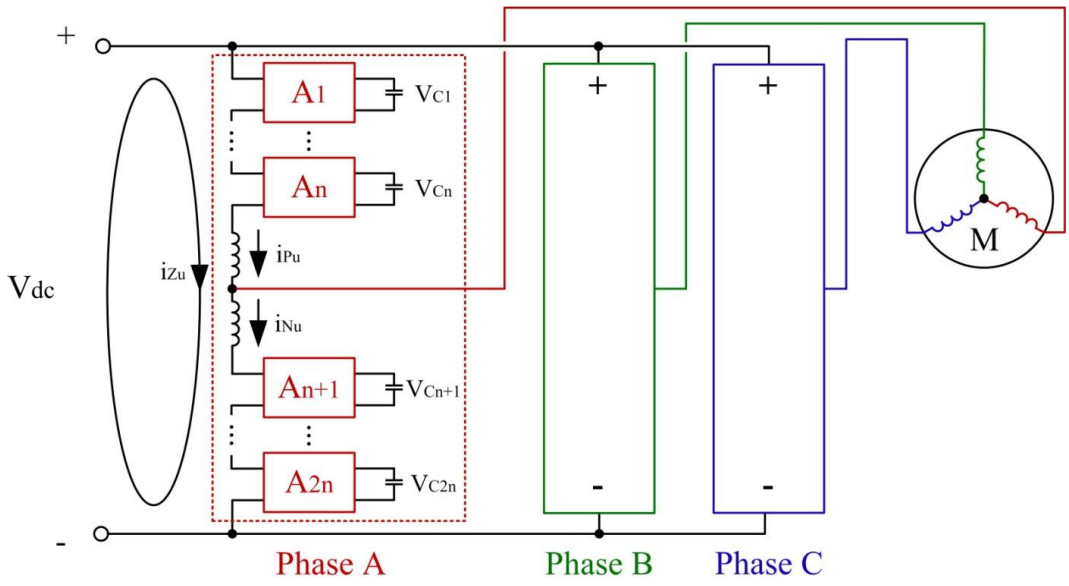
isolated DC inputs.

- Each DC-link capacitor is connected to a converter module.
- The output voltages from different converter modules are synthesized.
- Due to modular structure, the quantity of components is a linear increase as a function of n.

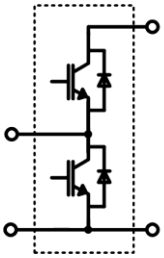
1.1.4 Modular Topologies with Single Input

In the previous section, modular topologies considerably extend the voltage levels due to their modular design. However, isolated voltage sources are required to power the converter modules. This section introduces recent topologies that can overcome this problem and only use one DC input source.

Modular multilevel converter (MMC), also referred as bridge of bridge (BoB) converter, is proposed by A. Lesnicar and R. Marquardt in 2003 [24], as shown in **Fig. 1.7**. It has been considered a very promising topology in recent years. Several half bridge modules (also called cells) with DC capacitors are connected in series to combine into an arm. Each half bridge is acting as a controllable 2-level voltage source. When several bridges are connected in series, they are able to output a multilevel waveform. Two arms are connected in series and combine into a single phase leg. They have complementary output waveforms that add up to the total DC input voltage. This topology requires a filter inductor in each arm. Since the module of MMC forms a boost converter topology, the component voltage in MMC must be slightly higher than V_{dc}/n.



(a)



(b)

Fig. 1.6. Modular multilevel converter (MMC)

(a) MMC topology, and (b) module topology

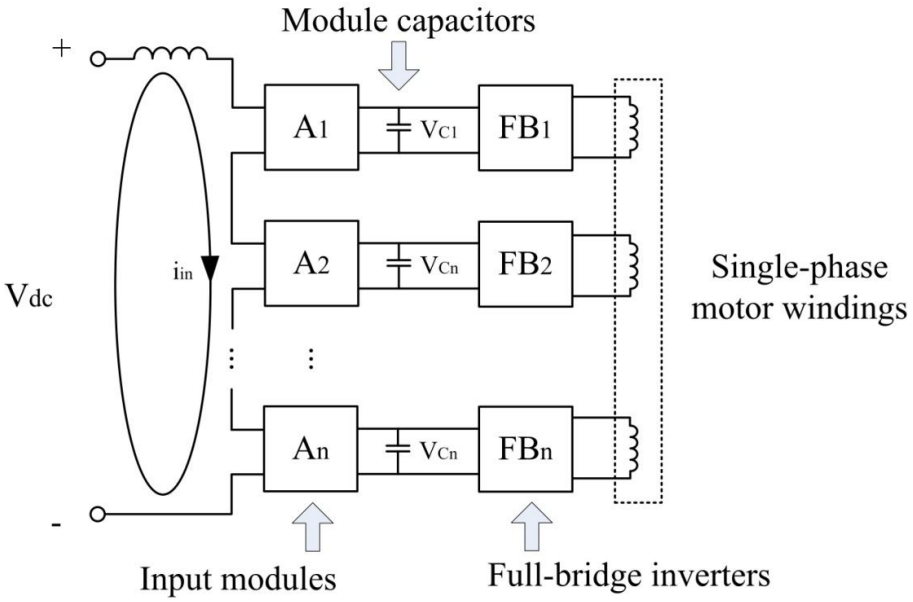
The control of MMC is more complicated than the other topologies discussed previously. As discussed in [25][26], several closed loop controllers are required for the single phase leg to properly function: (1) output voltage of the leg, (2) arm currents i_{Pu}, i_{Nu}, i_{Zu} and (3) DC voltages on module capacitors V_{C1}, V_{C2}, …, V_{C2n}.

The MMC concept can be easily extended. If the modules in **Fig. 1.6**(b) are full bridge modules, MMC can operate as an AC to AC converter [27]. MMC offers great opportunities for power grid applications such as flexible AC transmission system and static compensator. 12 to 48 modules are installed in an arm to realize a high voltage converter >100 kV by SIEMENS [28]. MMC is the most efficient structure that can easily increase voltage levels and it is very suitable for power grid applications.

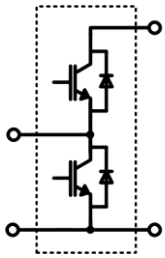
The single phase structure of MMC also leads to challenges when design the control algorithm. For single phase structure, there exists a large amount of energy fluctuating at twice the output frequency. Large capacitors are needed to buffer this fluctuating energy. Besides, a well designed controller is required to maintain the voltage balance on all modules. In [29], the authors propose an algorithm that estimates the fluctuating energy stored in the capacitors and generates a compensation command for the voltage balance control.

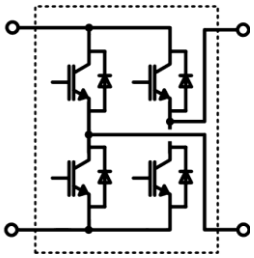
The same inventor of MMC also proposes modular high frequency converter (MHF) in [30]. This topology has similar input structure as MMC. Multiple input modules with capacitors are connected in series to build the total DC input voltage. The outputs are dedicated for multi-winding motor or transformer. Full bridge inverters, which are directly supplied by the module capacitors, provide multiple AC outputs. The synthesizing of these AC outputs relies on isolation provided by the motor windings [30] or transformers [31]. The module capacitors will buffer the single phase fluctuating power, so MHF topology needs some design considerations on the capacitor size. Although the input modules can help to handle the single phase power fluctuation, the module capacitors must deal with the negative instantaneous power [32]. Control algorithms are applied to actively regulate the capacitor voltages [33][34]. Same as MMC, the input module

of MHF is a boost converter and hence the component voltage in MHF must be slightly higher than V_{dc}/n.



(a)





(b) (c)

Fig. 1.7. Modular high frequency converter (MHF)

(a) MHF topology, (b) input module, and (c) full bridge inverter

In summary, this branch of multilevel topologies are identified by

- n half bridge input modules are connected in series (2n for MMC) to combine into a phase leg. Each module is equipped with a DC capacitor buffering the single phase power fluctuation.
- There is only one DC input with voltage V_{dc}. The voltage of each module is slightly higher than V_{dc}/n.
- Every phase leg requires filter inductors.
- Modular structures reduce design complexity as well as the overall cost of the system. It is also very easy to increase n by simply connecting more modules in series.

1.2 Wide Bandgap Semiconductor Power Devices

The technology of silicon (Si) power devices has been developed for decades. The power density, operating temperature and switching performance have almost reached the limits of Si [35]. However, in the area of transportation, mining, military, renewable energy, and etc., power converters with higher power density, operating temperature and switching frequency are still quite demanding. In recent years, an increasing number of research papers are focusing on wide bandgap (WBG) semiconductor materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) due to their superior properties. The term ‘wide bandgap’ typically refers to semiconductor materials with a bandgap greater than 3 eV. Because of the use of WBG materials, breakthrough technology in semiconductor is taking place and gradually changes the market.

1.2.1 Material Properties

As shown in Table 1.1 [36], the bandgaps of SiC and GaN are 3.2 eV and 3.4 eV respectively. Comparing to Si (1.1eV), SiC and GaN are three times higher. The bandgap property decides the probability of ionization and thermal-equilibrium statistics. The concentration of intrinsic carriers n_i in a semiconductor device is an exponential function of temperature and bandgap energy, represented by (1.2) [37]:

$$n_i^2 = N_c N_v \exp\left(\frac{-E_G}{k_B T}\right) \tag{1.2}$$

, where N_c and N_v are related to conduction band and valence band density of states respectively, E_G is the bandgap energy and k_B is the Boltzmann constant.

Material properties	Si	SiC	GaN
Bandgap [eV]	1.1	3.2	3.4
Critical field [MV/cm]	0.3	3.0	3.5
Electron mobility [cm^2/Vsec]	1450	900	2000
Electron saturation velocity [10^6cm/sec]	10	22	25

Table 1.1. Material properties

[36]

(1.2) is also plotted in **Fig. 1.8**, where the "2H", "6H" and "3C" refer to the crystal structure of the material. The p-n junction leakage current is decided by n_i in a quadratic function. At high

temperature, the leakage current increases and the device loss also increases. For normal Si semiconductor, the operating temperature cannot be high because of the significant leakage current. As a result of WBG, n_i is much lower and the p-n junction leakage current can remain relatively low at high temperature [38]. This allows SiC and GaN WBG power devices to operate at a much higher temperature than Si devices. It is reported that a 4H-SiC JFET can operate at extremely high ambient temperature up to 450℃ [39].

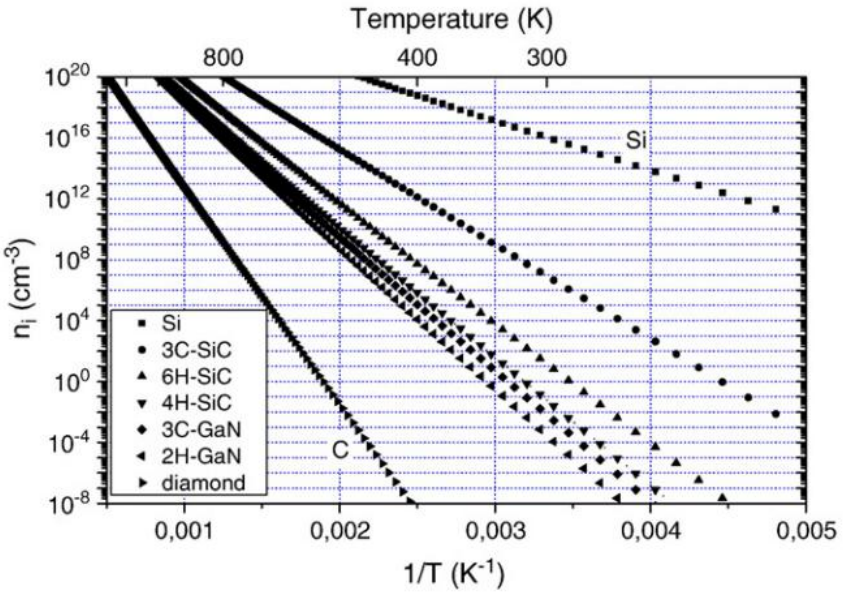


Fig. 1.8. Concentration of intrinsic carriers in semiconductor vs. temperature [40]

As shown in Table 1.1, the critical field of GaN and SiC are respectively 11.7 and 10 times higher than Si. The higher critical field will allow a higher breakdown voltage for identical epitaxial thickness. In other words, thinner epitaxial layer is needed for a certain breakdown voltage. The SiC and GaN devices can reach "record-high break down voltages" [41] or very low resistance. This characteristic is especially important for high-power or high-efficiency

applications. The following figure shows the specific on-resistance vs. breakdown voltage for Si, SiC and GaN devices.

The electron mobility and electron saturation velocity are also critical parameters that affect the transconductance, and output gain of FETs, which will decide the switching performance of the power devices [42]. Since GaN have largest electron mobility, it should ultimately be the best material for high frequency operation [36].

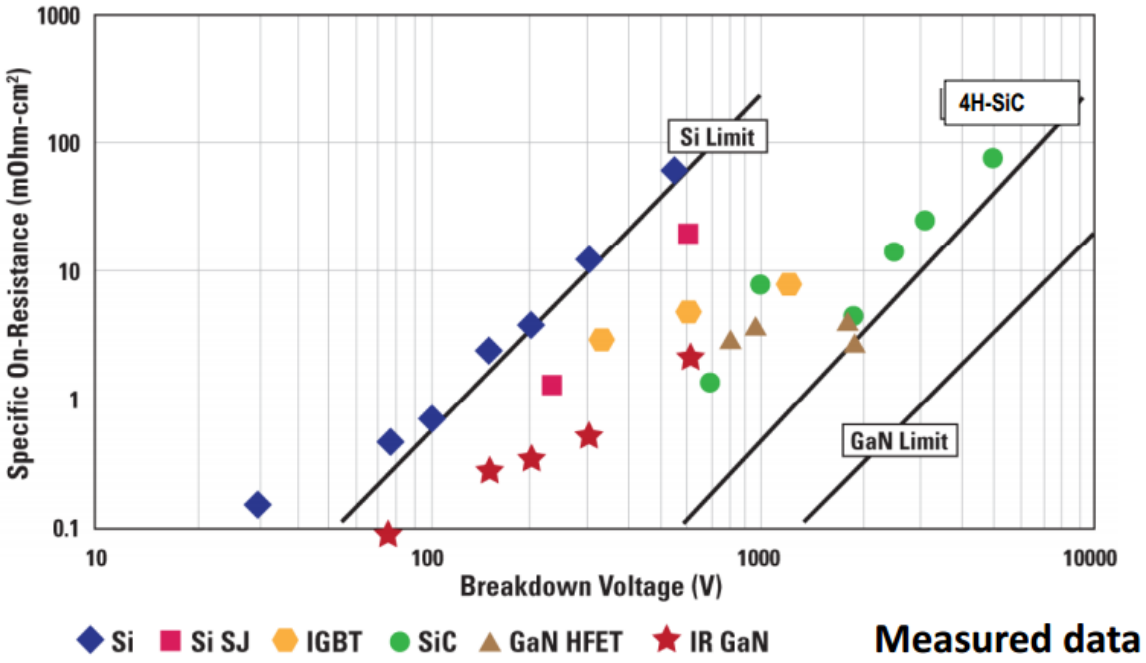


Fig. 1.9. The specific on-resistance vs. breakdown voltage

[43]

For high power application, the thermal performance is a critical factor that affects the device reliability. The following table shows the material properties associated with thermal performance. The thermal conductivity of SiC is better than Si and GaN, meaning the heat is

dissipated easily in the material. For this reason, SiC is generally considered to be the best high power material.

GaN exhibits a low thermal conductivity at 1.3 W/cmK, making it less appealing in high power application. Actually, the theoretical value of GaN thermal conductivity is estimated as 4.1W/cmK [44], which is comparable to 4H-SiC. GaN cannot reach its theoretical value because the formation of high quality defect-free GaN layers is difficult and is considered as one of the major technical challenges [45]. The defect crystal results in a lower thermal conductivity. However, with the development of GaN process, the thermal conductivity has a tendency to increase [45], and higher thermal conductivity (2.53W/cmK) is already achieved in [46].

The thermal conductivity is not the only parameter that affects the device thermal performance. Baliga's figure of merit (BoFM) is a measure of the on-resistance of a unipolar device, which will dominate the conduction loss of the device. The values are calibrated to 1.0 relative to Si. A larger value indicates smaller on-resistance and lower conduction loss. The conduction loss of a SiC device will decrease by a factor of 500 compare to Si [47]. With the same device size, the area for thermal dissipation is identical for different materials. But the conduction loss of SiC is 500 times smaller than the Si counterpart. GaN illustrates even better performance, i.e., 2400 times smaller than Si, which is equal to 21% conduction loss of SiC.

Material properties	Si	4H-SiC	GaN
Thermal conductivity [W/cmK]	1.5	3.8	1.3 / 4.1*
BFoM [47]	1	500	2400

*The theoretical value of GaN thermal conductivity [44]

Table 1.2. Material properties II

Both SiC and GaN exhibit great advantages over Si semiconductor. The performance gets improved by several orders of magnitude, which will allow the power electronics to operate at unprecendented high frequency, high efficiency and high temperature.

1.2.2 Existing Wide Bandgap Devices

It has been a long time since the beginning of SiC and GaN researches in labs. Only in recent years, SiC and GaN devices begin to present in the market. In this section, several representative SiC and GaN devices are introduced.

- **SiC schottky diode**

SiC schottky diode is the most mature WBG semiconductor power device. The silicon based schottky diode was suffered from the relative low voltage rating and high reverse leakage current. The voltage rating is typical 50 V and below. Although 200 V schottky diode is available, the reverse leakage current is very sensitive to the operating temperature. As a consequence, the device with a higher voltage rating will have worse thermal stability.

The SiC schottky diodes with rating voltage up to 1.7 kV become available in the market since 2011. The operating temperature can be as high as 200℃. It even allows radiative cooling in aerospace applications [48]. Since this voltage level and temperature is beyond the reach of silicon devices, SiC has already taken the market in the branch of schottky diode.

- **SiC FET**

SiC FETs become quite available in the market and the voltage rating is in the range of 600 V to 1.7 kV. Although the price of SiC device is higher than Si FET, the performance is much better. There are only a few comparable Si products using advanced semiconductor technologies,

e.g., CoolMOS by Infineon and MDmesh by STMicroelectronics, but the voltage range is limited to 500-900 V. For devices rating at 1.2-1.7 kV, the SiC devices are dominating the market. Si FETs at this voltage rating usually have very large on-resistance. Hence the current ratings of Si FETs are limited to several amps. The use of Si FETs is quite limited at this voltage level. By comparison, a variety of choices are available for SiC FETs at this voltage level. To compare Si and SiC devices, a 1.2 kV Si and a SiC FET are chosen to have identical on-resistance 0.35 Ω, as shown in the following table. In this way, the two FETs will have identical conduction loss. However, the performance of the SiC device is 1-2 orders of magnitude better than the Si device, indicated by the input capacitance and output capacitance. If the body diode is conducting, SiC FET will also have much better performance than Si FET, allowing it to operate in higher switching frequency. Moreover, a SiC FET with much lower on-resistance is available from the market, but there is almost no such choice for Si FET.

	Si	SiC
Manufacture	IXYS	Rohm
Manufacture #	IXFB30N120P	SCT2280KE
Rds(on)@25°C [Ω]	0.35	0.36
Input cap. [pF]	22500	667
Output cap. [pF]	950	27
Body diode reverse recovery time [ns]	300	22
Body diode reverse recovery charge [nC]	1600	21

Table 1.3. Comparison between 1.2kV Si and SiC devices

- **GaN FET**

Depletion mode (normally-on) GaN devices first started to appear in 2004 by Eudyna Corporation in Japan [49]. In recent years, an increasing number of researches are directed towards high performance GaN transistors. However, this has never been easy. Due to the thermal mismatch between different materials, there exists a thermal stress between GaN and the substrate when the temperature changes. Hence GaN is very difficult to grow on the substrate without defect [43]. Tremendous work has been down to improve the growth of GaN layer on Si substrate [50], sapphire substrate [51] or SiC substrate [52].

The growth of GaN on a SiC substrate has several advantages. The SiC material has a smaller thermal mismatch, which means GaN can grow easier on a SiC substrate. The high thermal conductivity of SiC is another advantage, which is preferred in high power density applications where the thermal performance plays a significant role. The drawback of SiC is the high cost of the material. As a comparison, Si substrate is much cheaper than SiC. Although it is more difficult to grow GaN on a Si substrate due to the thermal mismatch, the device cost is much lower than SiC substrate. Hence Si substrate is more suitable for commercialization.

The depletion mode (normally-on) is an inherent behavior of GaN devices with conventional structure. This is due to the strong built-in polarization electric field, which will cause two dimensional electron gas (2DEG) exists in the channel [53]. 2DEG cannot be easily depleted at zero gate voltage, so the GaN device exhibits normally-on behavior. Generally speaking, a normally-on device is not quite desirable in a voltage source power converter. During start-up, under-voltage transient, ESD and many other events, the control-unit will lose its functionality. As a result, the power circuit will become short-circuit and damage the devices, control units or even the input power sources. Compare to a normally-off device, the normally-on device requires

more circuit components and more complicated circuit design to guarantee the reliability. Normally-off devices are more preferred in power applications.

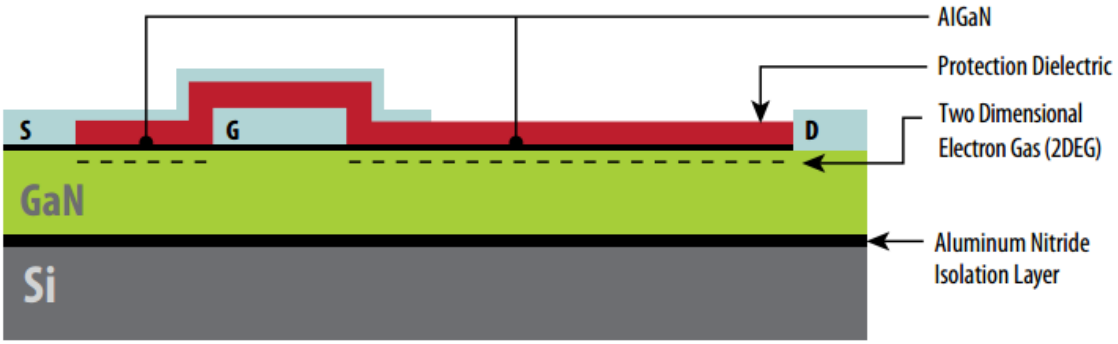


Fig. 1.10. The structure of EPC GaN FET

[49]

The existing commercialized normally-off GaN devices belong to two major branches. The first is the invention of enhancement mode GaN devices, which are normally-off devices. Efficient Power Conversion Corporation (EPC) introduced the first enhancement mode GaN FET on Si substrate. Through technology breakthrough, the 2DEG problem is dealt with so the device exhibits normally-off behavior. The following figure shows the lateral structure of an EPC GAN FET. EPC currently offers a wide range of enhancement mode GaN FETs. The voltage ratings are from 30V to 450V, available for the applications up to several kilowatts power converters.

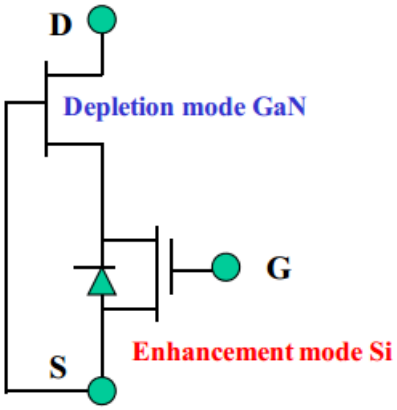


Fig. 1.11. Illustration of cascode solution

[54]

Another major branch is a solution that can convert a depletion mode GaN device into an equivalent normally-off device. This solution is referred as “cascode solution”. An enhancement mode Si device and a depletion mode GaN FET are combined into a cascade switch. The gate of GaN FET is tied to the source of the bottom switch, as shown in Fig. 1.11. By this way, the gate voltage of the upper switch is the source to drain voltage of the bottom Si switch, which is a negative value and securely turn off the upper GaN device. The cascode switch behaves as a normally off device, and the gate terminal is more like a low voltage Si device. In 2014, GaNSystems starts to provide cascode 100V and 650V GaN FETs. The device price is currently very high comparing to its Si counterparts.

- **Wide Bandgap IGBT**

Bipolar device such as IGBT has the advantage of smaller on-resistance than unipolar device such as MOSFET. However, there is an on-state voltage drop for IGBT inducing more conduction loss and making it less appealing for low power applications. In general, unipolar

devices are preferred at low voltages and bipolar devices are chosen for high voltages [55]. For Si, 400V to 900V is the rough border between unipolar and bipolar devices.

With WBG material, the on-state voltage drop for bipolar device such as IGBT is higher than Si. As a result, WBG IGBTs have more conduction loss than Si IGBTs at low power. For SiC, 3-5 kV is seen as the rough border [55]. For operating voltage below 3-5 kV, FETs have better performance than IGBTs.

1.3 Integrated Modular Motor Drive

1.3.1 Introduction

In applications such as electric vehicles, traction, robotics and servo motors, it is desirable to reduce the footprint and boost the efficiency of the whole motor and drive system. A conventional drive being used today is placed in a cabinet separated from the electrical motor being driven. Additional cables are required to connect the drive as well as the control and monitor units to the motor. Such kind of design inevitably adds to the volume and weight of the motor drive system and also increases the risks of generating high voltage transients on the motor windings due to long cable effect. For example, in electrical motors, a critical factor that can shorten a product's service life is the aging of stator winding insulation layers. Cases have been documented in industry when a motor ran well for several years but suddenly failed in a few weeks after installing a variable frequency drive [56]. The failure is usually due to an overshoot voltage damaging winding insulation layers. The peak voltage on a motor winding when the cable is 1000 ft (>300 m) long is more than double the peak voltage on the motor

winding when the cable is 30 ft (~10m) long [56]. To ease the overvoltage problem, bulky line reactors or AC filters are often added at the motor input terminals [57].

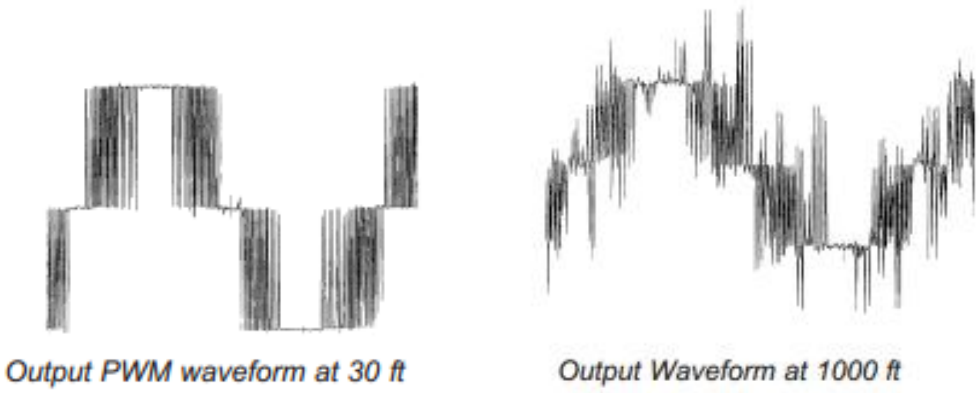


Fig. 1.12. Long cable effect on the motor windings
[56]

Several motor drive manufactures already provide commercialized integrated motor drive products. **Fig. 1.13** shows five examples. Schneider Electric offers integrated stepper motor drive, as shown in **Fig. 1.13** (d). This motor drive has Ethernet communication ability. It eliminates the communication cables and significantly simplifies the control of multiple distributed motors. The operator can control motors located at different places and exchange information via Ethernet. Lenze smart motor m300, as shown in **Fig. 1.13** (e), also has the advanced communication ability: it can be controlled through a smart phone. This greatly simplifies the control, data collection and diagnostic of the motor drive system. SEW EURODRIVE provides an integration system with a motor drive, a motor and the gear box. This design can reduce the installation space by 20-25% and achieve great efficiency.

The structures of these products are quite simple and straightforward-- the drive uses a ‘piggybacked’ design and it is physically mounted on the top of the motor. This design greatly

reduces the length of power cable and attenuates the long cable effect. However, the integration is limited to the physical attachment of the motor and the drive. The electrical properties remain identical to other conventional, separated motor drives.

(a) (b) (c)

(d) (e) (f)

Fig. 1.13. Examples of available commercialized integrated motor drives

(a) ElectroCraft PT series brushless DC motor, (b) Danfoss FCM series induction motor, (c) Rexroth Inadrive servo grade integrated motor drive, (d) Schneider Electric LMD series stepper motor, (e) Lenze smart motor m300 series, (f) SEW EURODRIVE MOVIGEAR series integrated motor drive and gear box

1.3.2 The Concept of IMMD

As presented in [58][59], a more compact way to achieve higher power density is to use segmented motor drive modules. The original motor drive is split into several smaller modules, as shown in **Fig. 1.14** and **Fig. 1.15**. The stress on each module is reduced and several modules are combined to provide the total power. The motor drive has a round shape and can be mounted on the back side of the motor. Power semiconductor devices are mounted on a piece of heat sink with liquid cooling. Compare to the piggybacked design, this is a more compact design approach to integrate the motor and drive. These researches have demonstrated very promising power density.

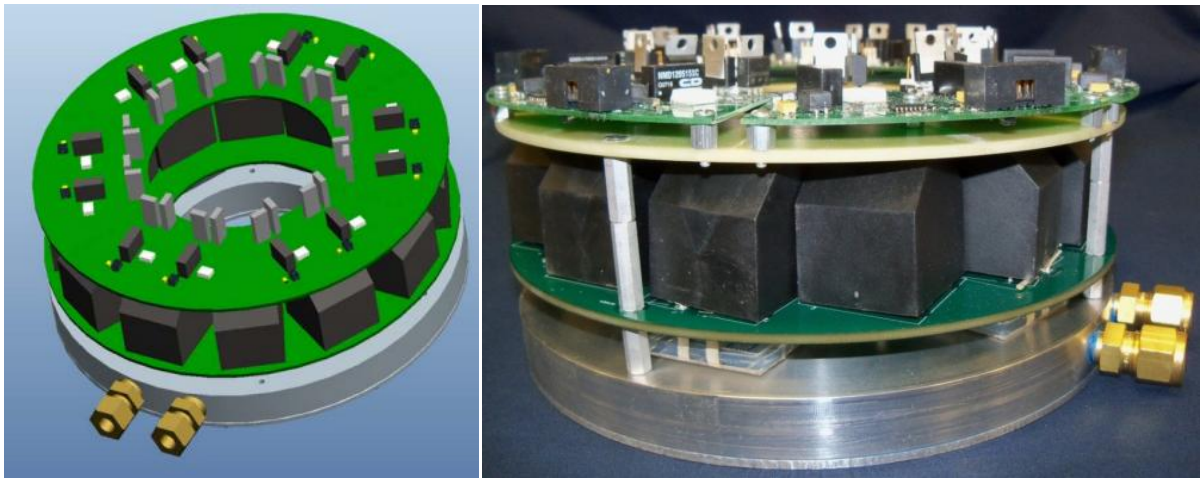


Fig. 1.14. Segmented motor drive

[58]

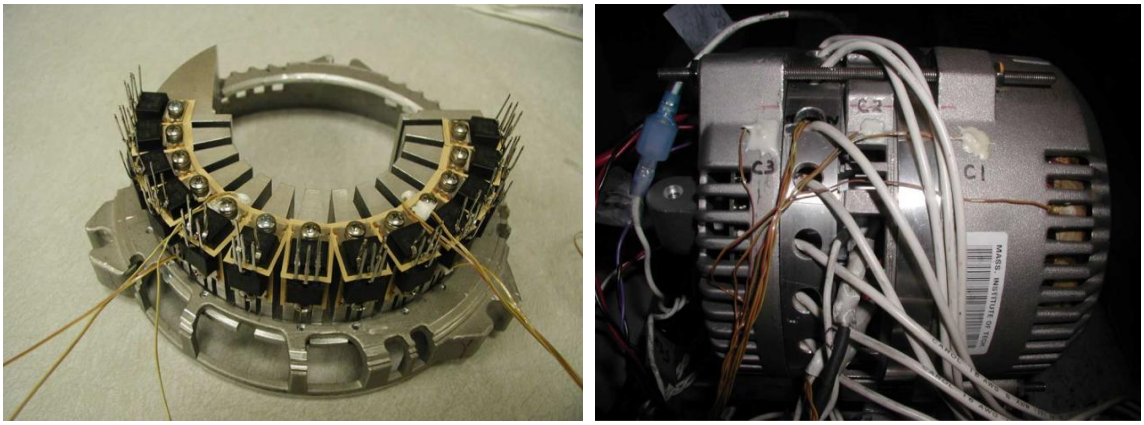


Fig. 1.15. Integrated automotive alternator

[59]

In [60] the authors present a matrix motor concept that the semiconductor switches can be mounted around the motor. In this research, the switches are used for the motor drive. Instead, they are used for online reconfiguration of the motor. This concept can be easily extended to design an integrated motor drive in the future.

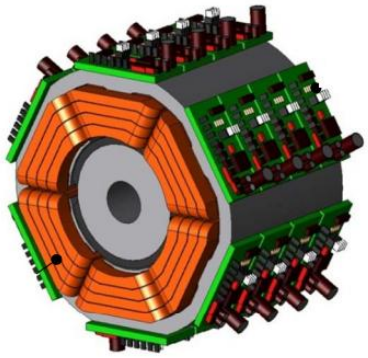
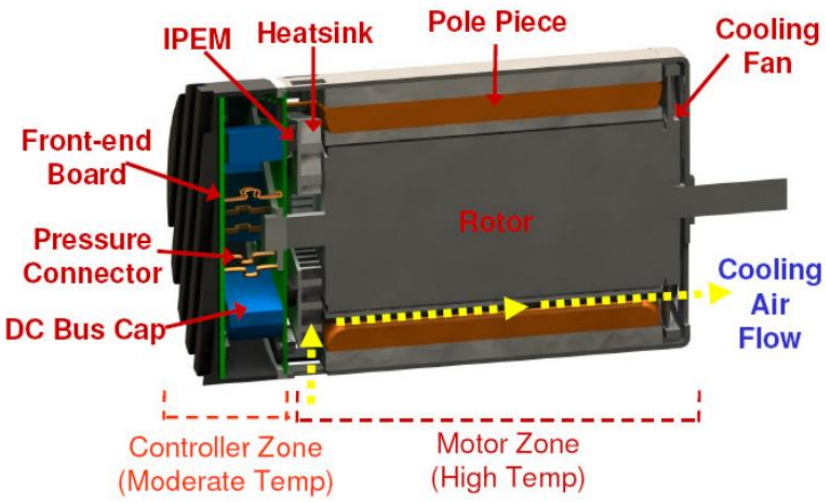


Fig. 1.16. Matrix motor with semiconductor switches for reconfiguration

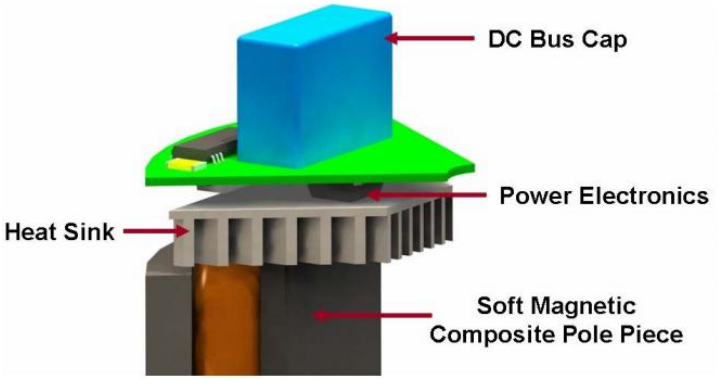
[60]

It is possible to achieve system integration with even higher level. Not only the drive, but also the motor itself can be modularized and segmented into several stator pole pieces. The motor,

the control unit, as well as the communication and protection modules are combined into a single compact package, as illustrated in **Fig. 1.17**. This new design approach is referred as "Integrated Modular Motor Drives (IMMD)". Researchers in Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC) have demonstrated both the concept and hardware designs in [61][62][63], which are huge steps in IMMD development.



(a)



(b) (c)

Fig. 1.17. IMMD demonstration model

(a) Cross-section view, (b) one IMMD module, and (c) the photo of an IMMD [62]

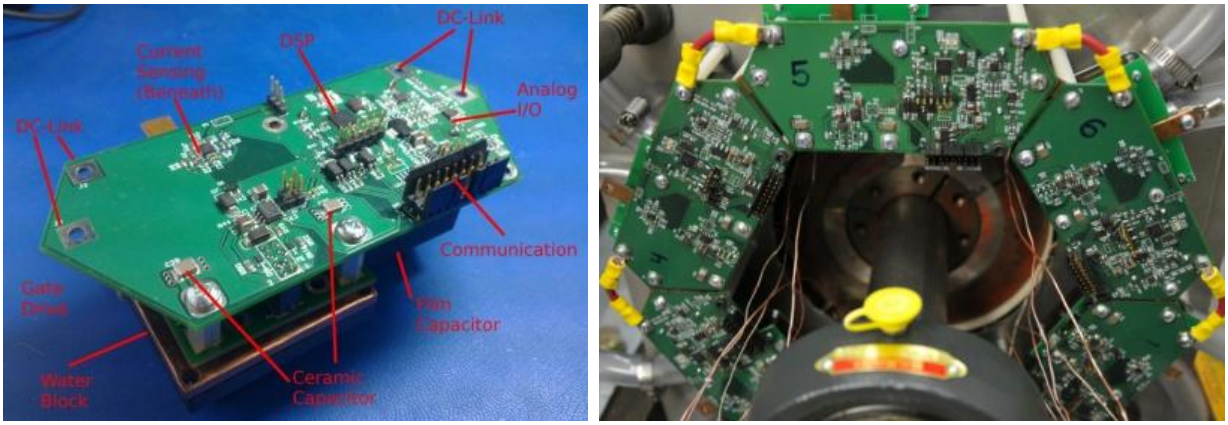


Fig. 1.18. IMMD demonstration model with distributed control

[63]

An IMMD module usually consists of:

- A stator piece that has a concentrated coil winding
- A power converter dedicated to the stator piece and corresponding gate drivers
- DC-link capacitors
- Thermal management
- Current and voltage sensors (optional)
- Communication and control units (optional)

1.3.3 Advantages of IMMD

Compare to conventional motor drives, IMMD has the following advantages:

- Without the transmission cable, EMI and long cable effect are greatly attenuated. The extra expense of power connecters and power cables are reduced.

- The cost of IMMD is reduced due to modular design. It simplifies the design procedure because all modules are identical. The fabrication cost is reduced due to the mass production of smaller converter modules. The maintenance is also less expensive because when IMMD fails, only the broken module needs to be replaced.
- All the motor and drive components are combined into a single package. The overall system will greatly benefit from this IMMD concept, and become faster, smaller, quieter and cheaper.
- The thermal performance is better. Several IMMD modules share the same total power but semiconductor devices are spread out with larger surface area per volume. The total surface area of semiconductor devices is increased and the heat is distributed over a larger area. The heat sink can be designed to be more efficient and the hot spot temperature of IMMD is reduced.
- Fault tolerance is better because the motor and drive are designed for one another. The motor does not necessarily have 3-phase configuration. Instead, a high phase order configuration can be used. The operation can be maintained even with the loss of 1 or 2 phases for a 5-phase motor [62].

1.3.4 IMMD Challenges

The physical integration of the drive and the motor inside a single housing poses a number of technical challenges. Firstly, the environment inside the motor housing is very unpleasant for the drive to operate. The motor temperature can be too high and damage the power devices. As a consequence, the motor drive has to install separate heatsinks with lower temperature.

The large size of DC-link capacitors is another problem faced by IMMD. Bulky capacitors take a large volume, which will inevitably increase the size and weight of IMMD. These capacitors are the tallest components on the printed circuit board (PCB) and they often determine the overall height of an IMMD. The volume of an IMMD is approximated by taking the cross-section area of the PCB and multiplying it by the IMMD height. Hence the total size of the IMMD is directly proportional to the capacitor height. As show in **Fig. 1.14** and **Fig. 1.17**, these capacitors are too tall. It becomes very difficult to fully integrate an IMMD and all the DC-link capacitors into a flat package. Moreover, capacitors with large sizes and heights will cause physical vibration when the motor is running.

The hardware design of an IMMD is another challenge. To simply cut the PCB into a round shape is not an effective way. A compact IMMD design requires optimal placement of components, careful arrangement of connectors, proper management of thermal and vibration, and etc.

1.4 Research Opportunities

In this section, research opportunities are identified based on state of the art review of multilevel converter, WBG semiconductors and IMMD.

1.4.1 Multilevel Topology for Motor Drive

Many multilevel converter topologies have been successfully commercialized and proven to be feasible technologies. However, there still remain a number of challenges to improve

efficiency, compactness, modularity, reliability, and cost performance. An ideal multilevel motor drive should have the following characteristics:

- It would have a modular design that is reliable and easy to manufacture and maintain.
- The number of modules is easily expanded with few constraints.
- The multilevel converter requires only one DC-input voltage source.
- The semiconductor devices would have even voltage, current and power stresses.
- The DC capacitors in converter modules will only handle switching ripples instead of single-phase pulsating power.
- There is no voltage balance problem in the DC capacitors.
- It would allow the flexible use of low-voltage, less-expensive devices such as MOSFETs or higher-voltage, more-expensive devices such as IGBTs or new devices fabricated from SiC and GaN.
- It would have no clamping diodes, clamping capacitors, extra transformers or inductors. The quantity of components should be minimized.

However, none of the existing multilevel topologies have all the desirable features. Most of the existing multilevel topologies are not optimized for motor drive applications. They are general solutions to both motor drive and power grid applications. This forces the topology to have exactly three output terminals and limits the topology diversity to some extent. It is desirable to develop a multilevel topology dedicated for motor drive applications. The properties of a motor should be considered and utilized to benefit the multilevel converter design. By

utilizing the properties of a motor, many new opportunities are provided to optimize the converter design, shrink the converter size and reduce the overall cost.

1.4.2 Motor Drive Using GaN Power Devices

In applications such as hybrid electric vehicle, the underhood ambient temperature for power converters is up to 120℃ to 140℃ [64]. The junction temperature of power devices will be even higher. For this reason, the motor drive is typically arranged in a separate housing from the motor [65]. It is desirable to utilize WBG power devices in a motor drive to increase the operating temperature, so the drive can share the same housing and heat sinks with the motor.

A higher operating temperature will also help to reduce the size of heat sinks. To dissipate a certain amount of heat, smaller surface area is needed when the temperature difference is larger. With WBG power devices, the temperature of heat sinks can increase so that the temperature difference between heat sinks and the ambient is larger. As a result, the volume and weight of overall system is reduced by using WBG power devices.

Moreover, the superb efficiency of WBG devices benefits the power converter. WBG devices will induce less converter loss and less heat. Hence the size of heat sinks is fundamentally reduced. The converter can also operate at a higher switching frequency, enabling smaller passive components and filter size, which will further reduce the converter size. With a higher switching frequency, the converter dynamic response is faster. It helps the converter to execute a user command in shorter time and better reject disturbance.

High power motor drive using SiC devices has been investigated in many researches [55][66]. At lower power, GaN FETs are better than SiC devices. However, only in recent years

the GaN power devices are becoming available to the market. There still remain many questions to be answered: Whether GaN devices are suitable for motor drive applications? How to design a GaN motor drive? What is the performance of GaN devices? and etc. The design of a motor drive that utilizes GaN devices is a great research opportunity. PCB designs and solid experiment results are needed to demonstrate the capability of GaN devices in a motor drive application.

1.4.3 Demonstration IMMD Hardware Design

To demonstrate the concept of IMMD, a fully integrated motor drive including not only power converters and DC-link capacitors, but also controls, communications and sensors is desired. It is desirable to build a fully functional, fully integrated IMMD demo to extend the previous works.

Opportunities and challenges are identified to realize such a compact system. There is very limited space inside a motor housing, and hence a reasonable IMMD structure is required in order to properly manage the limited space. The IMMD should have a round shape and the size of it should match the size of the motor. The thickness of the IMMD must be minimized otherwise the IMMD is hard to remain physical integrity in the vibrational environment in a motor housing. This requirement calls for very low profile DC-link capacitors. To realize a compact IMMD, it needs very careful design and selection of DC-link capacitors. Different types of capacitors should be compared for motor drive applications. Moreover, it is desirable to investigate different methods to further reduce the size of capacitors, for instance, applying gate signal interleaving technique and properly increasing switching frequency.

1.4.4 The Combination of Multilevel, GaN Devices and IMMD Concepts

The concepts of multilevel converter, GaN devices and IMMD are not independent. Instead, these concepts will greatly benefit each other when they are combined. The GaN semiconductors can achieve the switching frequency and operating temperature that was not possible via Si semiconductors in the past. The efficiency of GaN devices is also superb so the thermal challenge of IMMD is attenuated. Consequently, the sizes of capacitors and heatsinks are greatly reduced and the IMMD is more compact.

With the help of multilevel converter, the voltage stress of capacitors and semiconductor devices are reduced. With the flexible selection of voltage, the IMMD design can be optimized so the capacitor volume and height are minimized to integrate into the IMMD package.

One important feature of FETs is that the on-state resistance increases rapidly with the voltage rating. **Fig. 1.9** shows that the resistivity (specific on-resistance) of a FET increases by 200 times if the voltage increases from 100 V to 1000 V. In other words, if 10 FETs with 100 V rating voltage are connected in series, the series resistance is 20 times lower than a single FET that can handle 1000 V. In this case, using series-connected low voltage FETs will result in 20 times lower conduction loss. Moreover, high voltage GaN FETs are not quite mature at this moment and are much more expensive than low voltage GaN FETs. Thanks to multilevel converter topology, the voltage stress of semiconductor devices can be easily reduced and result in higher efficiency, smaller heatsinks and lower cost.

With IMMD concept, the motor drive is combined with the motor in a modular way. The modular motor structure makes it possible to develop a novel multilevel topology that utilizes the motor properties and has minimum number of components.

Chapter 2

The Proposed Converter Topology

This chapter will introduce the proposed multilevel motor drive topology, in which the motor windings are considered as part of the converter. As a consequence, there is no extra component in the proposed converter. Details of the motor split windings are discussed in this chapter. The component quantity and sizing between existing multilevel topologies and the proposed one are compared. An extended version of the proposed topology is also introduced in this chapter.

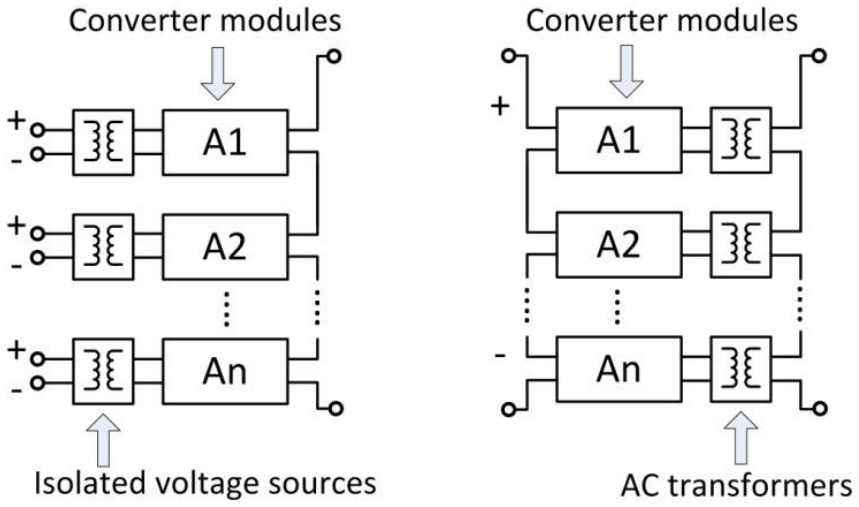
2.1 The Fundamental Topology

2.1.1 Voltage Synthesizing of Existing Topologies

In a multilevel converter, there always exists an approach to synthesis the voltages of the semiconductor devices so the whole converter can operate at higher input and output voltages than the devices. In the clamping topologies, the input voltage is effectively shared, i.e. equally divided, by the DC-link capacitors, which are directly connected in series. Since the DC-link capacitors are not floating, the clamping topologies must rely on the clamping diodes or flying capacitors to synthesize the output voltages. Diodes or capacitors are needed between any two voltage levels, and hence the component quantity is a quadratic function of n. As a result, these topologies are becoming much more complicated when there are more voltage levels n. In a CHB, the component quantity is a linear growth as n, because it utilizes isolated voltage sources as the input synthesizing approach. The individual converter modules are floating so there is no

limitation on the output synthesizing approach. The outputs of CHB modules are simply connected in series so the output AC voltages are superimposed.

CHB is a very good point to start with because of its simplicity. **Fig. 2.1**(a) shows the single phase structure of a CHB converter. The input power is flowing through the isolated voltage sources, followed by the converter modules and finally to the machine. One major drawback of CHB is the extra cost and space of isolated voltages sources, which are supplied by either isolated DC-DC converters or frontend multi-winding transformer with passive rectifiers.



(a) (b)

Fig. 2.1. Single-phase converter topologies
(a) the CHB topology, and (b) a converter with AC transformers

Alternatively, CHB can morph into another structure by changing the sequence of power flow. In the alternative structure, outputs of converter modules are synthesized with low-frequency AC transformers, as shown in **Fig. 2.1**(b). This structure can replace the isolated voltage sources by

low-frequency AC transformers. In this case, the control and the total output voltage of converter modules are identical to a CHB. Since the outputs are synthesized by isolation transformers, there is no limitation on the input side. The simplest way is to connect module inputs in series, i.e., the DC-link capacitors of the modules are connected in series, just like in the clamping topologies. However, the AC transformers handle the full power and the frequency is identical to the motor electric frequency. Hence they are usually bulky and expensive, and as a consequence, advantages are unclear except for simplified DC inputs.

2.1.2 The Proposed Single Phase Topology

A desirable topology is one that provides the advantages of existing topologies while minimizing the disadvantages. The topologies shown in **Fig. 1.5** have demonstrated the possibility to utilize machine windings to realize multilevel converters. These topologies indicate that the co-design of an electric machine and its associated multilevel converter has the potential to increase the overall system performance and reduce the size and cost. However, the inputs of these topologies still come from several separate isolated DC sources. As a result, these topologies have limited output voltage levels and complex front-end rectifier design. To avoid the isolated voltage sources in **Fig. 2.1**(a) or AC transformers in **Fig. 2.1**(b), a different isolation approach is needed.

The proposed approach is to utilize the motor itself to act equivalently as isolation AC transformers. The motor will be the ideal isolation device because it handles the full power without adding extra components, and also induces zero extra power loss. The motor is an inherent magnetic component but in other motor drive topologies, it is typically treated as the converter load. Actually, its windings are magnetically coupled and electrically isolated, which

allows for the design of a multilevel converter that takes advantage of the winding properties. The multilevel converter can then utilize the motor windings, stator or even rotor as coupling transformers to achieve the desired output. As shown in **Fig. 2.2**, several split motor windings are connected to the converter modules and synchronize converter outputs. The outputs from different converter modules are combined inside the machine to create a machine magnetomotive force (MMF) identical to **Fig. 2.1**. As long as the MMF does not change, the machine torque ripple and magnetic loss will be identical.

The outputs of converter modules are connected to individual motor windings that provide electric isolation. There is no limitation to the inputs, allowing the proposed topology to connect converter modules in series at the input and use only one DC input source.

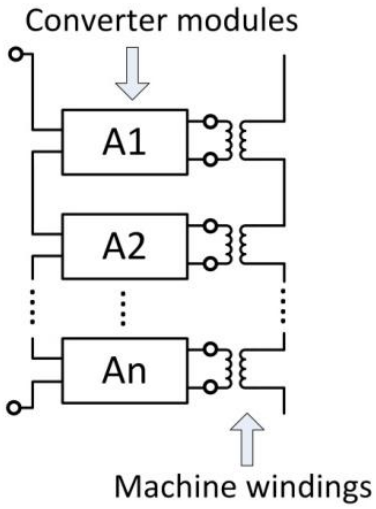


Fig. 2.2. Proposed single-phase converter structure utilizing motor windings

2.1.3 The Proposed Three Phase Topology

Assume the single phase voltage and current are $v_a(t)$ and $i_a(t)$ respectively.

$$v_a(t) = V_{p-p} \cdot \sin(\omega t)$$
$$i_a(t) = I_{p-p} \cdot \sin(\omega t + \phi)$$

The single phase instantaneous power can be calculated:

$$\begin{aligned} p_a(t) &= v_a(t) \cdot i_a(t) \\ &= \frac{1}{2} V_{p-p} \cdot I_{p-p} \cdot \cos(\phi) - \frac{1}{2} V_{p-p} \cdot I_{p-p} \cdot \cos(2\omega t + \phi) \end{aligned} \tag{2.1}$$

The first part of (2.1) is a time invariant value equals to the single phase real power. The second part is a time variant value represents the power fluctuating at twice the fundamental frequency. If a single phase power converter is used, e.g., a full-bridge inverter, its input is DC and output is single phase AC. The imbalance between the constant input DC power and output AC fluctuating power will cause a large voltage swing on the module capacitors. The capacitors must be large to suppress the voltage swing.

In a three phase system, the three phase voltages and currents are as follows:

$$v_a(t) = V_{p-p} \cdot \sin(\omega t) \quad , \quad i_a(t) = I_{p-p} \cdot \sin(\omega t + \phi)$$

$$v_b(t) = V_{p-p} \cdot \sin(\omega t - 120^\circ) \quad , \quad i_b(t) = I_{p-p} \cdot \sin(\omega t + \phi - 120^\circ)$$

$$v_c(t) = V_{p-p} \cdot \sin(\omega t + 120^\circ) \quad , \quad i_c(t) = I_{p-p} \cdot \sin(\omega t + \phi + 120^\circ)$$

The instantaneous power of this balanced three phase system will be:

$$\begin{aligned} p(t) &= v_a(t) \cdot i_a(t) + v_b(t) \cdot i_b(t) + v_c(t) \cdot i_c(t) \\ &= \frac{3}{2} V_{p-p} \cdot I_{p-p} \cdot \cos(\phi) \end{aligned} \tag{2.2}$$

The instantaneous power is a time invariant value equals to the three phase real power. The reactive power of each phase is balanced by the other two phases. Compare to a single phase module, the DC-link capacitor in a three phase module will handle constant power during steady-state operation. Hence only switching ripples will present in the capacitors. Since the switching frequency (typically >1 kHz) is much higher than the motor fundamental frequency (typically <100 Hz), the required capacitance can be effectively reduced by increasing the switching frequency.

The proposed three-phase converter topology is shown in **Fig. 2.3**. A converter module consists of a three-phase inverter, a DC-link capacitor and a motor winding segment. All of the converter modules are connected in series and share the same dc input, but there are no clamping diodes, clamping capacitors, filter inductors or isolation transformers. The total output voltage is combined inside the machine without any extra components.

The proposed topology is similar to WEMPEC research in 2008 [61]-[63] where the converter modules are all connected in parallel. This topology with converter modules connected in series was introduced in [67][68][69][70] for high voltage wind turbine generator applications. In this thesis, this multilevel topology is proposed for integrated motor drive applications to improve the performance and minimize the size.

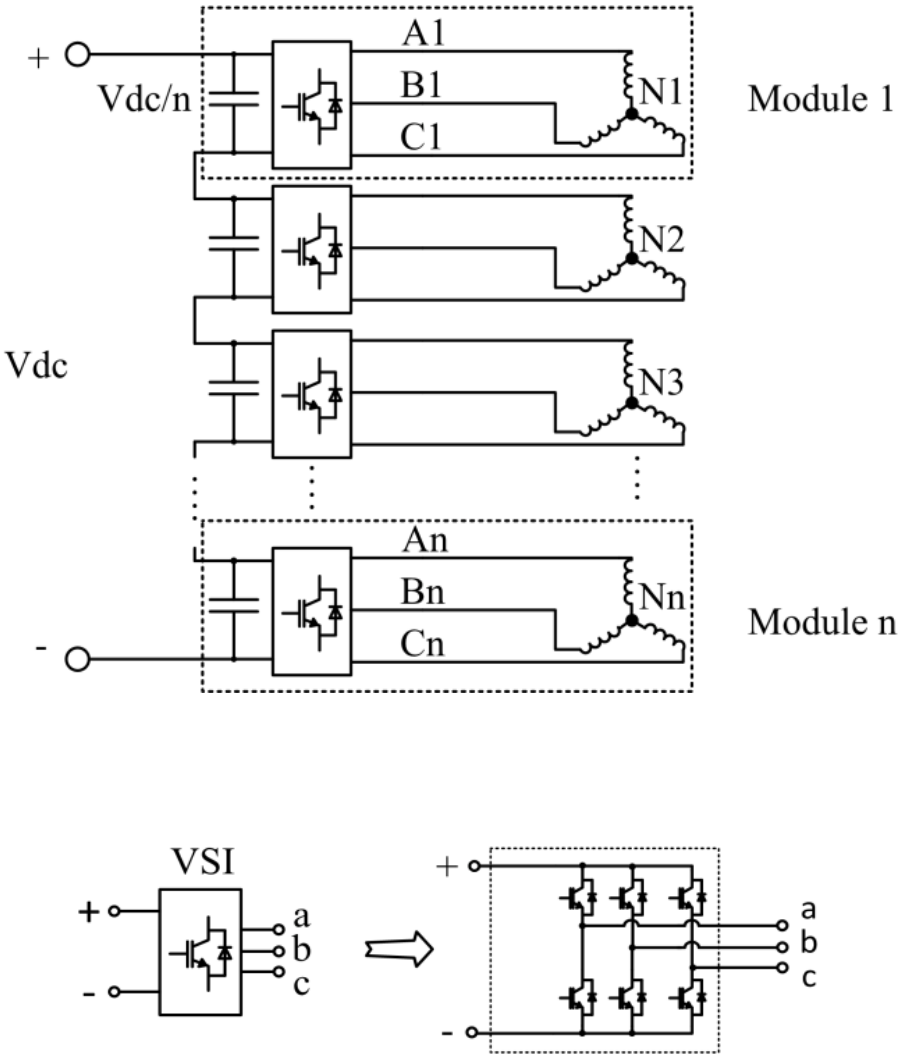


Fig. 2.3. Proposed topology with n converter modules

2.2 Split Winding Machine

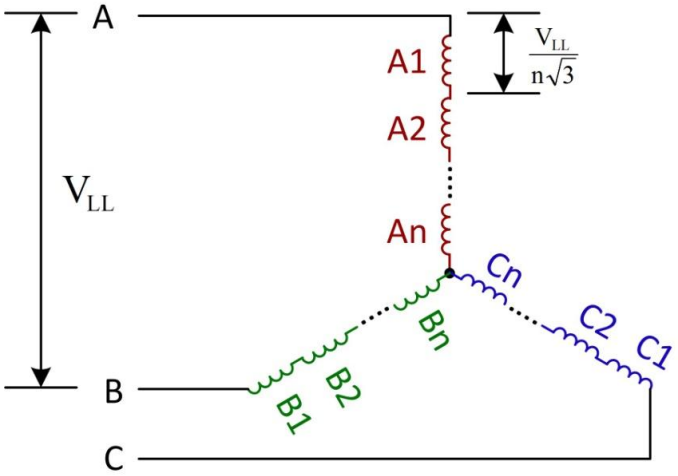
In the proposed converter topology, motor windings are becoming an important part to synthesize the output voltages. Different from a conventional 3-lead motor or 6-lead open winding motor, the proposed motor needs to change the arrangement of the motor windings. This section will discuss the split winding technique.

2.2.1 The Concept of Split Windings

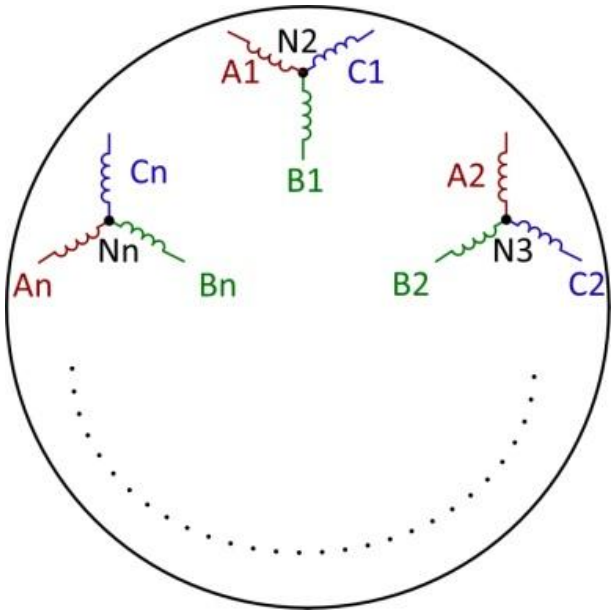
As shown in **Fig. 2.4**(a), the winding coils in a conventional motor can be connected in series to share the phase voltage. It is also normal in a conventional motor to connect the winding coils in parallel so the phase current is shared among different coils. In either case, the winding coils A1, A2, … , An are the fundamental elements in the motor. The interconnections between winding coils will not affect the properties of the coils. In the proposed topology, individual motor winding coils have the same gauge, number of turns and configuration as in a conventional motor. The only difference is the changed interconnections between the winding coils.

The winding coils are distributed along the stator circumference. The coils in adjacent three phases Ax, Bx and Cx are proposed to connect to their local neutral points Nx can combine into a winding segment, as shown in **Fig. 2.4**(b). In this way, this segment can be separated from other segments and supplied by its individual power converter bridge. These coils are also isolated from other coils and theoretically, the neutral point voltage can be an arbitrate value within the limit of motor insulation.

This kind of motor winding configuration maintains all of the electrical and mechanical properties of the motor, because it does not alter the coils in motor slots. It can be easily generated from a conventional motor design without any extra cost or re-design. The split winding design also benefits the manufacturing because it eliminates the interconnection between different motor segments, which will reduce the end winding cost and size, as well as simplify the manufacturing process.



(a)



(b)

Fig. 2.4. Motor winding configuration

(a) Conventional motor winding configuration of an n-pole-pair machine, and

(b) Proposed winding configuration

2.2.2 High Phase Order Machine

The proposed concept can be extended to drive a high phase order machine, which has the advantage of small torque ripple and large power rating [71]. A machine with a high phase order will inherently have many windings for different phases. The capacitors in converter modules can be minimized as long as the converter modules provide constant power that is not a time variant function of motor fundamental frequency. A six phase machine [72] inherently has two 3-phase segments. The machine can be driven by two converter modules, respectively connecting to the windings of 0°, 60°, 120° and 180°, 240°, 300°. It is also possible to split the machine into 0°, 120°, 240° and 60°, 180°, 300°. For either case, the two converter modules will provide constant power and valid for the proposed topology. Similarly, a nine phase machine [71] has three 3-phase segments and can be driven by three converter modules. For a five phase machine [73] however, there is no such option for constant power windings, unless all five phases are driven by a single converter. But there still exists some way to split the machine into multiple segments, as will be discussed in the next section.

2.2.3 Fundamental Winding Configurations

There can be various arrangements of winding coils in different motors. For the sake of simplification, two fundamental winding configurations are introduced. These two configurations are quite different from each other. To achieve more design flexibility in a real design, these two configurations can be combined into a more complicated one. Although the winding configurations are also applicable for high phase order machines, only three phase examples are illustrated in this section for simplification.

- **Configuration #1: split winding coils in different pole pairs**

In a motor with multiple pole pairs, there are three phases in each pole-pair. To clearly identify this fundamental winding configuration, a simplified example is presented in Fig. 2.5. In this example, the motor only have 2 stator pole pairs and 12 slots. Phase A has four slots, i.e., slot #1, 4, 7, and 10. The winding coils in different pole pairs are split into two segments. The two winding segments could be connected in series or in parallel in a conventional motor so they share the same output terminals. However for the split winding design, the windings in different pole pairs are separated and have their own neutral points N1 and N2 as well as output terminals A1 and A2. The winding segments are located at different halves of the motor without overlapping. This split winding configuration will separate the coils electrically and physically.

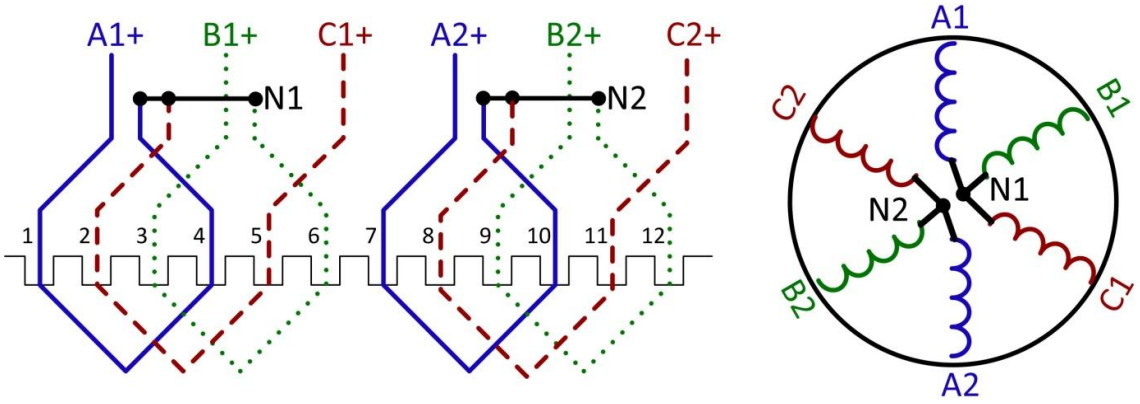


Fig. 2.5. Simplified model for winding configuration #1

This concept can also be applied to a motor with concentrated windings. For example, a 6-slots stator will have 6 winding coils and 2 coils for each phase. The individual coils are inherently non-overlapping with each other, as shown in the following figure.

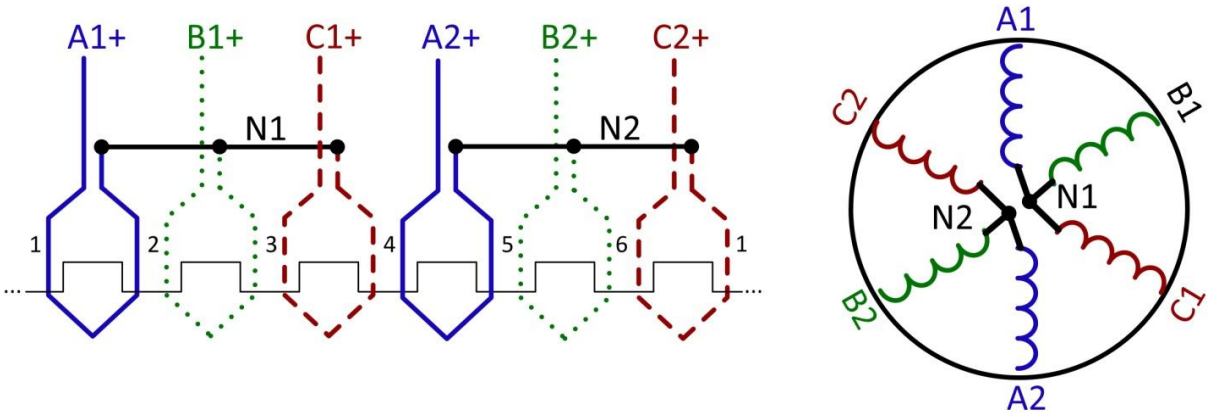


Fig. 2.6. Motor with concentrated winding for configuration #1

This configuration can be extended to a stator with multiple phase windings so the motor is possible to split into multiple segments. This winding configuration will completely separate the motor into several segments. Each segment has exactly the same electromagnetic properties. As will be shown in this thesis, since the winding segments are not overlapping, the magnetic coupling factors in dq axis between different segments are always zero.

- **Configuration #2: split winding coils in identical pole pair**

The second fundamental configuration is shown in **Fig. 2.7** and **Fig. 2.8**. As shown in **Fig. 2.7**, there is usually more than one coil in one phase, which belongs to the branch of distributed winding machine. The distributed lap winding coils in a 3-phase, 2-pole and 12-slot motor (two slots per pole per phase) is split into two segments. They should be series-connected in a conventional motor to form a lap-winding configuration. In the proposed design, the winding coils in two adjacent slots are completely separated and can be controlled individually. The split winding approach is very flexible when there are more slots per pole per phase (SPP). For

example, if SPP=6, it is possible to split the motor into 1, 2, 3, or 6 segments. Any factor of SPP can be achieved by simply alter the interconnection between winding coils.

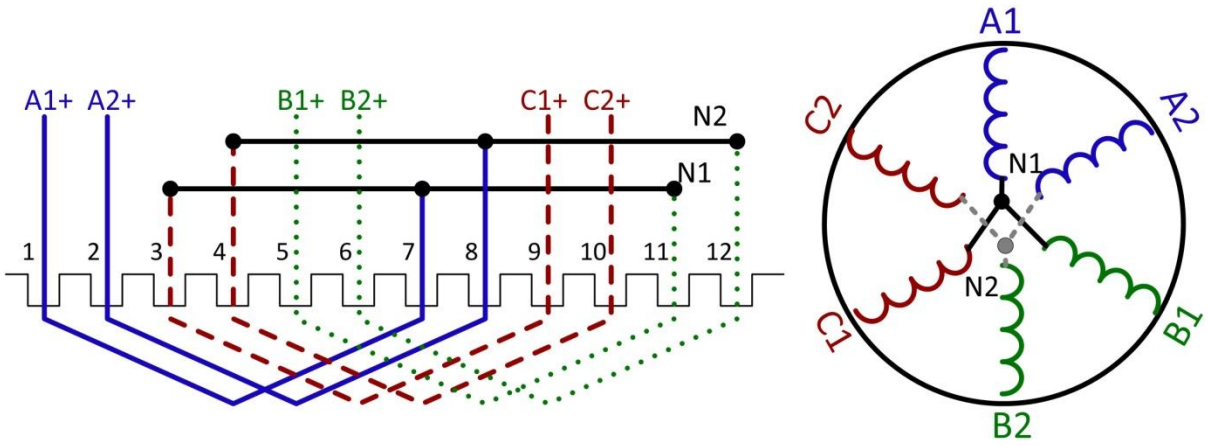
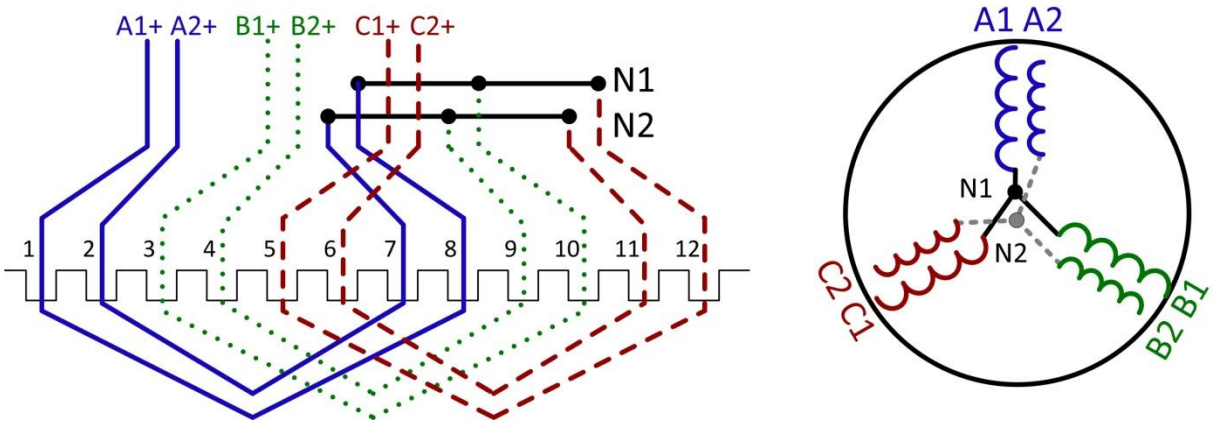
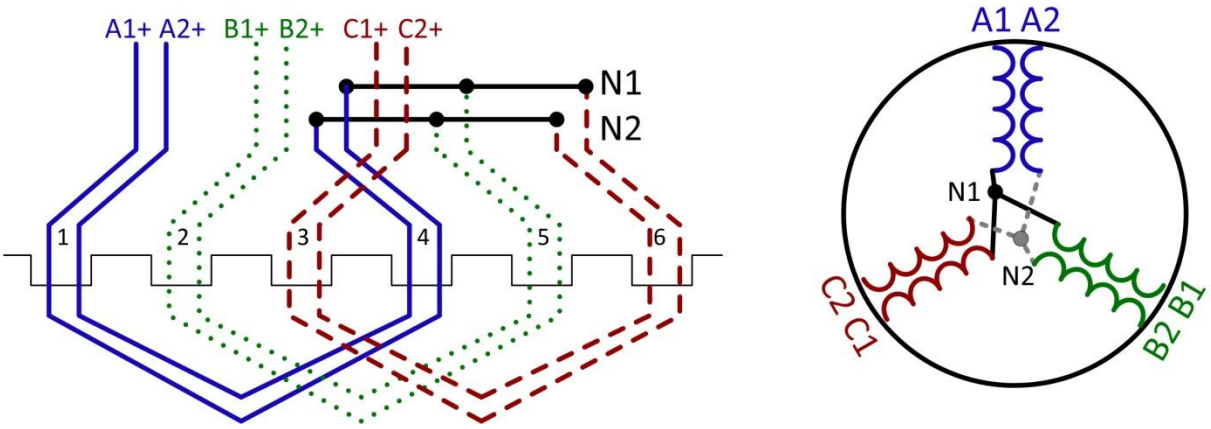


Fig. 2.7. Simplified model for winding configuration #2

This configuration will split the motor with distributed lap winding into several non-identical segments. All the segments have the same current and voltage ratings, but they are locating at different stator angles. Under identical excitation, the MMF generated by these segments will have different spatial angles.



(a)



(b)

Fig. 2.8. Other examples of configuration #2.
(a) concentric winding coils (b) same slot coils

A machine with other distributed winding, e.g., concentric winding, can also be split. The concentric winding split segments have identical angle, but the coil spans are different, resulting in a little different voltages on the coils, as represented by **Fig. 2.8**(a). Similarly, the winding turns in a single slot can be split into several segments when needed. In this way, the coils will have identical properties, as shown in **Fig. 2.8**(b).

By applying configuration #2, the power, voltage and current of each motor segment are very flexible for design. For configuration #2, the winding segments are overlapping with each other. There is a strong magnetic coupling between winding segments because the coils in different segments are located in adjacent slots. If two coils are in the same slots, they tend to have a coupling factor close to 100%. With strong magnetic coupling, the windings will behave as the primary and secondary sides of a transformer.

- **The combination of two fundamental configurations**

In a more general case, these two configurations are both possible for one motor. For example, a motor with 4 poles, 2 slots per pole per phase could be split into 4 winding segments. 2 segments are split according to configuration #1 and the other two are split as configuration #2.

The configuration #1 is more preferred because physical separation of winding segments is more desirable. This will allow the motor drive modules to physically attach to the winding segments without overlapping. There is a limit for configuration #1 since the motor has a certain number of non-overlapping winding segments. For configuration #2, it enables more flexible design, especially when the number of required segments does not match the number of pole-pairs. By configuration #2, a motor can be split into small segments with any desired power and voltage ratings such that the other components in the multilevel converter can be optimized, e.g. the semiconductor devices and the DC-link capacitors.

2.3 Component Quantity and Sizing

In this section, the size and quantity of components in different converter topologies are calculated and compared. NPC, FC, CHB, MMC, MHF and the proposed converter topology are involved. Assume all the converters have a DC input with voltage V_{dc}, and all the power switches, diodes and capacitors are targeting to have a V_{dc}/n voltage rating, which are typically considered as n+1 level converters. The only exception is CHB topology since it uses isolated voltage sources. On each phase of CHB, n modules can generate 2n+1 levels. To make a fair comparison to other topologies, the CHB topology only has n/2 modules in each phase to generate n+1 voltage levels.

2.3.1 Component Quantity

As introduced in the state-of-the-art-review, NPC and FC topologies have a quadratic component increase as n. CHB requires multiple input sources. MMC and MHF needs filter inductors. **Table 2.1** summarizes the component quantity of these topologies. The extra components of each topology are marked as bold.

	Switches	Clamp diodes	Flying cap.	Input sources	DC-link cap.	Filter inductors	Switch stresses	Modular design
NPC	6n	**3n(n-1)**	0	1	n	0	**Uneven**	**No**
FC	6n	0	**1.5n(n-1)**	1	n	0	**Uneven**	**No**
CHB	6n	0	0	**1.5n**	**1.5n**	0	Even	Yes
MMC	6n	0	0	1	**3n**	**6**	Even	Yes
MHF	6n	0	0	1	n	**1**	Even	Yes
Proposed	6n	0	0	1	n	0	Even	Yes

Table 2.1. Quantities of components to realize an equivalent n+1 voltage level

It shows that the proposed topology has the same number of power switches as other topologies. Unlike NPC and FC converters, the device stresses in the proposed topology are all the same which means the proposed topology is easily extended to more voltage levels. Compared to other topologies, the proposed one avoids clamp diodes, flying capacitors, and

input DC sources, extra DC-link capacitors and filter inductors. There is no extra component in the proposed topology because the machine windings can function as filter inductors and isolation transformers. Reductions in the component quantities are made without degrading to the system performance. As a result, the proposed converter has a very simple structure.

2.3.2 Component Sizing

The component sizing requirements of different topologies are calculated for comparison. All the power devices, capacitors and filter inductors must be able to handle the worst case stress. The size of a power switch or a power diode is decided by the product of its current stress and voltage stress. The size of a capacitor or an inductor is decided by the energy stored in the component [74].

- **Assumptions**

1. Since the application is motor drive instead of power grid, the output frequency and voltage are changing in a large range. The voltage stress of a power device is the peak voltage on the device. The peak voltage on the device equals to the capacitor voltage V_C. The ripple voltage on the capacitor is small so it has negligible effect. The current stress of a power device is typically defined as the RMS current for a MOSFET or average current for a diode or an IGBT. However, in a motor drive application, the fundamental frequency can be very low such that the devices can be overheated during the peak current. As a result, the current stress of a power device is defined as the peak current.

2. The size of a capacitor is decided by its stored energy, i.e.

$$E_C = \frac{1}{2} \cdot C \cdot V_c^2 \tag{2.3}$$

The capacitance C is usually decided by the voltage ripple. For a given current waveform, larger C will result in smaller voltage ripple. The voltage ripple is set as ±5% of the capacitor average voltage V_c. It is also possible to reduce the capacitance value by increase the voltage ripple. However, the voltage rating of the capacitor will also increase because the peak voltage of the capacitor is the sum of V_c and the peak voltage ripple. The charge to the capacitor is:

$$\int i_c dt = \Delta Q_C = \Delta V_C \cdot C \tag{2.4}$$

3. The converter uses SVPWM so the DC-link voltage is $\sqrt{3}$ times of maximum machine phase voltage peak value [75].

4. Per unit values:

Base voltage: The machine line to line voltage RMS value $V_{LL\text{-}rms}$ = 1.0 p.u.

Base current: The machine line current peak value $I_{L\text{-}pk}$ = 1.0 p.u.

Base frequency: the machine fundamental electric frequency ω_{eR} = 1.0 p.u.

Other values can be calculated according to the base values.

The machine line to line voltage peak value $V_{LL\text{-}pk} = \sqrt{2}$

The machine phase voltage peak value $V_{phase\text{-}pk} = \sqrt{\frac{2}{3}}$

The total input DC-link voltage is $V_{DC} = \sqrt{3} \cdot V_{phase\text{-}pk} = \sqrt{2}$

The DC voltage on each capacitor $V_C = \frac{\sqrt{2}}{n}$

- **FC**

The power devices total rating is:

$$6 \bullet n \bullet V_C \bullet I_{L\text{-}pk} = 8.485 \tag{2.5}$$

The worst case of a flying capacitor is when the capacitor is charged in one switching cycle and discharged in the next cycle:

$$\int_0^{T_{sw}} (I_{L\text{-}pk}) dt = \frac{1}{f_{sw}} \tag{2.6}$$

The peak charge buffered by capacitor is half of the total charge:

$$Qc = \frac{0.5}{f_{sw}} \tag{2.7}$$

Capacitor value will be

$$C = Qc / \Delta Vc = \frac{0.5}{f_{sw} \bullet 5\% \bullet V_C} = 5\sqrt{2} \bullet n \bullet \frac{1}{f_{sw}} \tag{2.8}$$

The total flying capacitors energy will be

$$1.5n(n-1) \bullet \frac{1}{2} \bullet C \bullet V_c^2 = 10.61 \bullet (n-1) \bullet \frac{1}{f_{sw}} \tag{2.9}$$

The worst case of a DC-link capacitor is when the capacitor is charged in half switching cycle and discharged in the other half cycle. The value of capacitance will be half of (2.8).

$$C = 2.5\sqrt{2} \bullet n \bullet \frac{1}{f_{sw}} \tag{2.10}$$

The total DC-link capacitors energy will be

$$n \cdot \frac{1}{2} \cdot C \cdot V_c^2 = 3.54 \cdot \frac{1}{f_{sw}} \tag{2.11}$$

The total capacitors energy, including the flying capacitors and DC-link capacitors will be

$$(10.61 \cdot n - 7.08) \cdot \frac{1}{f_{sw}} \tag{2.12}$$

- **NPC**

The power switches and diodes total rating is:

$$[6 \cdot n + 3 \cdot n \cdot (n-1)] \cdot V_C \cdot I_{L\text{-}pk} = \sqrt{2}[3n + 3] = 4.24 \cdot (n+1) \tag{2.13}$$

The capacitors in NPC are decoupling the six-pulse machine current [76][77]. The energy variation in the capacitor can be calculated by:

$$\frac{1}{\omega_{eR}} \int_{\alpha=60^\circ}^{120^\circ} \sin(\alpha)\, d\alpha = \frac{1}{\omega_{eR}} = 1.0 \tag{2.14}$$

The average value of one pulse is

$$\frac{1.0}{(120^\circ - 60^\circ)} = \frac{3}{\pi} \tag{2.15}$$

The peak charge buffered by capacitor in one pulse is the difference between the sinusoidal waveform and the average value.

$$Qc = I_{L\text{-}pk} \cdot \frac{1}{\omega_{eR}} \int_{\alpha=\arcsin(3/\pi)}^{\pi - \arcsin(3/\pi)} \left(\sin(\alpha) - \frac{3}{\pi}\right) d\alpha = 0.0181 \tag{2.16}$$

The required capacitor value will be

$$C = Qc / \Delta Vc = \frac{0.0181}{5\% \bullet V_C} = 0.362 \bullet n \tag{2.17}$$

The DC-link capacitors energy will be

$$n \bullet \frac{1}{2} \bullet C \bullet V_c^2 = 0.362 \tag{2.18}$$

Besides, the DC-link capacitors will also handle the switching ripple. The total DC-link capacitors energy will be the sum of (2.11) and (2.18).

$$0.362 + 3.54 \bullet \frac{1}{f_{sw}} \tag{2.19}$$

- **CHB**

The power devices total rating is the same as (2.5).

The total energy buffered by the single phase capacitor is (assume 1.0 power factor):

$$\frac{V_{phase\text{-}pk}}{n} \bullet I_{L\text{-}pk} \bullet \frac{1}{\omega_{eR}} \int_{\alpha=45^\circ}^{90^\circ} \sin^2(\alpha)\text{-}0.5 \, d\alpha = \frac{1}{4n}\sqrt{\frac{2}{3}} \tag{2.20}$$

The charge of the capacitor is:

$$Qc = \frac{1}{4n}\sqrt{\frac{2}{3}} / V_C = \frac{1}{4\sqrt{3}} \tag{2.21}$$

Capacitor value will be

$$C = Qc / \Delta Vc = \frac{1}{4\sqrt{3} \bullet 5\% \bullet V_C} = \frac{5}{\sqrt{6}} \bullet n \tag{2.22}$$

The total capacitors energy for single phase fluctuation will be

$$1.5n \bullet \frac{1}{2} \bullet C \bullet V_c^2 = 3.06 \tag{2.23}$$

Taking switching ripple into account, the total DC-link capacitors energy will be the sum of (2.11) and (2.23). Notice that in CHB the number of capacitors is 1.5 times more.

$$3.06 + 5.31 \bullet \frac{1}{f_{sw}} \tag{2.24}$$

- **MMC**

The power devices total rating is the same as (2.5).

According to [78] (28a), the energy variations in the module capacitors in a MMC are single phase fluctuation. This conclusion is also consistent with [79]. Assume 1.0 power factor and the maximum modulation index, the energy variation is identical to CHB (2.20):

$$\frac{V_{phase\text{-}pk}}{n} \bullet I_{L\text{-}pk} \bullet \frac{3}{2} \bullet \frac{1}{12} \bullet \frac{1}{\omega_{eR}} \bullet (4\text{-}1\text{-}2) = \frac{1}{4n}\sqrt{\frac{2}{3}} \tag{2.25}$$

Hence the total capacitors energy for single phase fluctuation will be

$$3n \bullet \frac{1}{2} \bullet C \bullet V_c^2 = 6.12 \tag{2.26}$$

The total capacitors energy including switching ripple is

$$6.12 + 10.62 \bullet \frac{1}{f_{sw}} \tag{2.27}$$

- **MHF**

The power devices total rating is the same as (2.5).

The power in MHF is fluctuating when the module output power is negative [32]. Assume power angle is $35^{\circ} = 0.61$ rad, then the capacitor needed for buffering the negative power is

$$C = \frac{2 \bullet 0.61^3 \bullet I_{L\text{-}pk} \bullet \frac{V_{phase\text{-}pk}}{n}}{V_c^2 \bullet 12 \bullet 5\% \bullet \omega_{eR}} = 0.309\ n \tag{2.28}$$

The total DC-link capacitors energy will be

$$n \bullet \frac{1}{2} \bullet C \bullet V_c^2 = 0.309 \tag{2.29}$$

The total DC-link capacitors energy including switching ripple will be

$$n \bullet \frac{1}{2} \bullet C \bullet V_c^2 = 0.309 + 3.54 \bullet \frac{1}{f_{sw}} \tag{2.30}$$

- **The proposed topology**

The power devices total rating is the same as (2.5).

The DC-link capacitor is identical to (2.11).

- **Comparisons**

Table 2.2 shows the sizes of power devices and capacitors for different multilevel topologies calculated previously. Because of quadratic function of component quantity, NPC has a device rating related to n, and FC has a capacitor rating related to n. In NPC, CHB, MMC and MHF, the capacitor sizes have a constant base value, which is decided by the fundamental machine frequency. In FC and the proposed topology, the capacitor sizes are only decided by the switching frequency.

	Power switches and diodes	Capacitor energy
NPC	4.24• (n+1)	$0.362 + 3.54 \bullet \frac{1}{f_{sw}}$
FC	8.485	$(10.61 \bullet n - 7.08) \bullet \frac{1}{f_{sw}}$
CHB	8.485	$3.06 + 5.31 \bullet \frac{1}{f_{sw}}$
MMC	8.485	$6.12 + 10.62 \bullet \frac{1}{f_{sw}}$
MHF	8.485	$0.309 + 3.54 \bullet \frac{1}{f_{sw}}$
Proposed	8.485	$3.54 \bullet \frac{1}{f_{sw}}$

Table 2.2. Component sizing of different topologies

To better illustrate the size of capacitors, numerical values are calculated, as shown in **Table 2.3**. Assume the machine fundamental frequency is 60 Hz = 1.0 pu and number of level is n+1 = 7. The capacitor size for the proposed topology and FC are much smaller at higher switching frequencies. But the FC topology is still ten times larger than the proposed topology, because there are a large number of capacitors in FC.

Switching frequency	500 Hz	1kHz	5kHz	15kHz	100kHz
NPC	0.787	0.574	0.404	0.376	0.364
FC	6.79	3.39	0.679	0.226	0.034
CHB	3.70	3.38	3.12	3.08	3.06
MMC	7.39	6.76	6.25	6.16	6.13
MHF	0.734	0.521	0.351	0.323	0.311
The proposed	0.425	0.212	0.043	0.014	0.0021

Table 2.3. Capacitor size at different switching frequencies

2.4 Voltage Stress

2.4.1 Voltage Stress on Converter Modules

The power switches and DC-link capacitors of a multilevel converter module are designed to operate at lower voltage than the total input/output voltages. The voltage stress of these power components is identical in different topologies. However, the voltage stresses on other components, such as signal isolators, are typically much larger.

In a typical converter module, the ground is tied to the negative lead of the DC-link capacitor. It is desirable to have a stable converter ground voltage. However, the converter modules are connected in series and the ground of it is floating. The converter modules must handle this voltage stress during operation. As illustrated in the following figure, the converter module needs

isolated power supply for its controllers, gate drivers and sensors. Signal isolators such as optocouplers, digital isolators or fiber optic cables are used for transmitting communication signals. The cost and size of these isolation devices are directly decided by the voltage difference between the converter ground and the real ground.

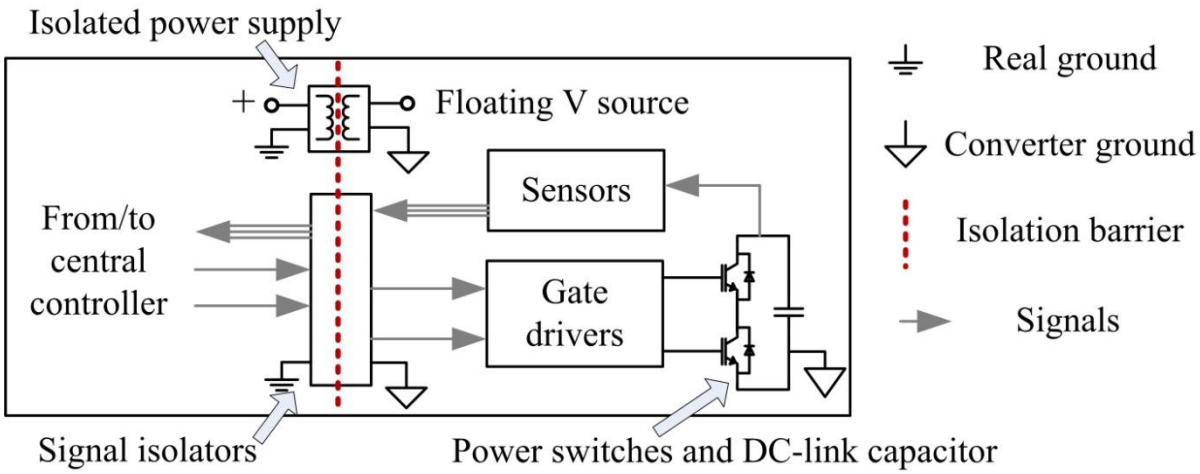


Fig. 2.9. Illustration of the isolation devices in a typical converter module

Several factors will affect the isolation devices. The maximum voltage of a module is the peak voltage between the converter ground and the real ground. All the isolation devices must withstand this voltage without break down. The voltage swing is defined as the voltage range that a module will experience. A large voltage swing is not desirable because it adds more stress to the isolation devices. Compare to a steady DC voltage, an AC voltage swing is more difficult to handle. In the isolation power supply, there is usually an isolation transformer. There exists parasitic capacitance in the insulation layer between the primary and secondary windings. The AC voltage swing will keep charging and discharging the parasitic capacitance, resulting in

common mode current and it will cause insulation worn out. For this reason, the voltage swing usually dominates the cost and size of isolation devices. The slope of voltage swing (dv/dt) is also an important parameter of converter reliability. If the slope is too steep, i.e., the voltage potential of a module changes too fast, it will result in incorrect communication signals, fault gate trigger and transformer resonance inside the isolated power supply.

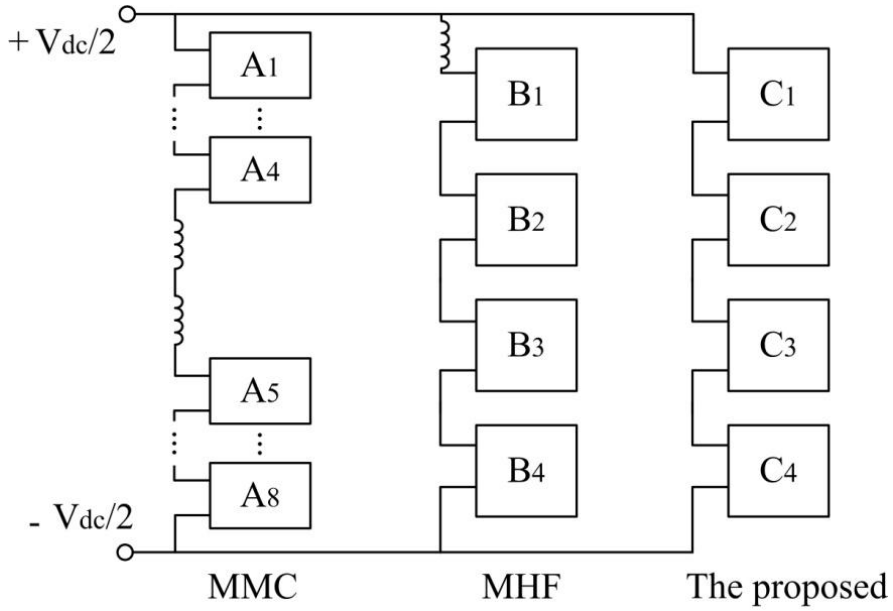
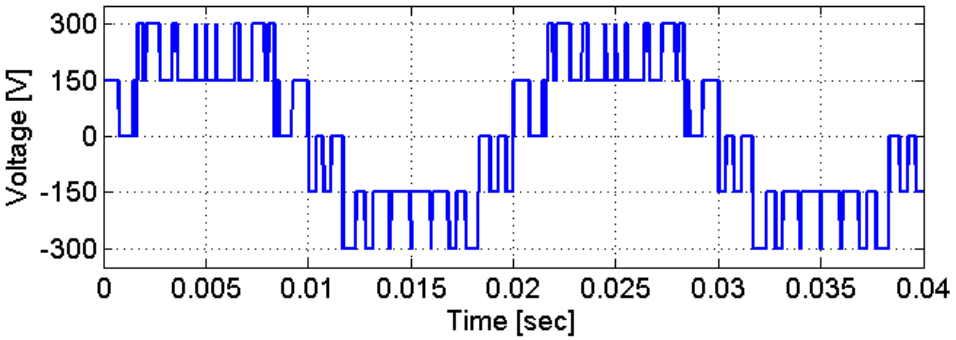
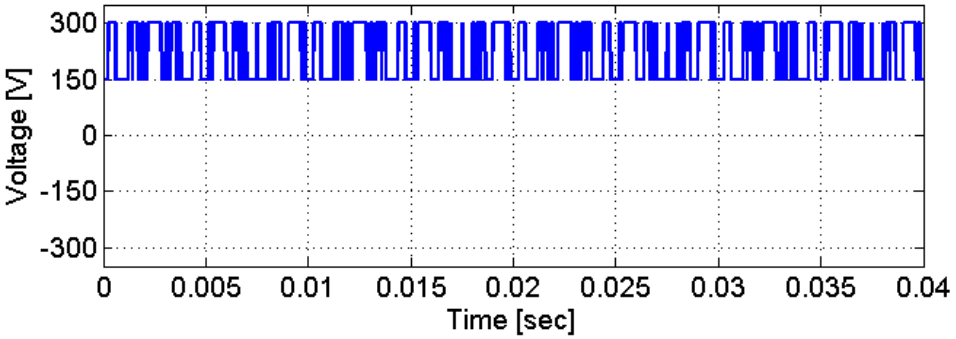


Fig. 2.10. Comparison of different converters

MMC, MHF and the proposed converter are compared, as shown in **Fig. 2.10**. Assume the total input DC-link voltage is V_{dc} and module voltage is $V_{dc}/4$. MMC will have 4 modules per arm and 8 modules per phase. MHF and the proposed converter will have 4 modules.



(a)



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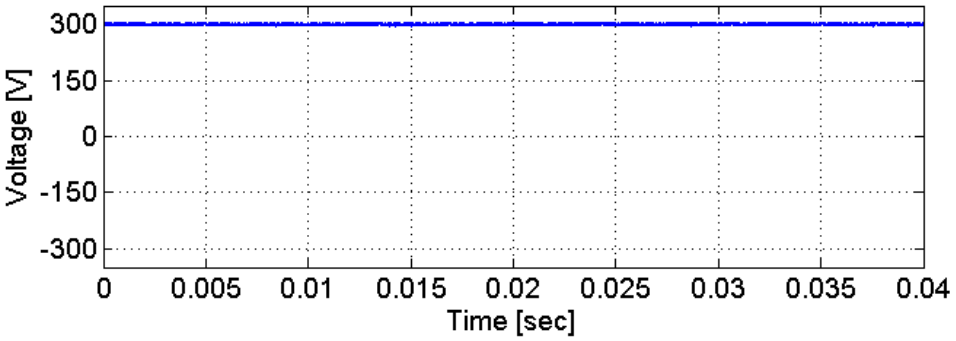


(c)

Fig. 2.11. The maximum module voltage waveforms for ±300 V DC-link and four modules

(a) A4 in MMC, (b)B1 in MHF, (c) C1 in the proposed topology

	MMC	MHF	The proposed
Max. voltage	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
Max. voltage module #	A8	B4	C4
Max. voltage swing	V_{dc}	$V_{dc}/4$	Cap. ripple
Max. voltage swing module #	A4	B1, B2, B3	C1, C2, C3
Slope of voltage swing	Power switches	Power switches	Cap. ripple

Table 2.4. Voltage stress on converter modules

If the input DC voltage is ±300 V and the module voltage is 150 V, the ground voltage waveforms of modules in different topologies are shown in **Fig. 2.11** and summarized in **Table 2.4**. The maximum voltage on the isolation devices are $V_{dc}/2$, i.e. 300V in this example, which is greater than the 150 V voltage stress on the power components. When there are more modules, the isolation devices will handle even larger voltage stress. For MMC, the four modules in the upper arm can be shorted to generate a maximum output voltage. At this moment, the module A4 is tied to the positive DC-link with voltage $V_{dc}/2$. When the bottom arm is shorted, A4 is tied to the negative DC-link with voltage $-V_{dc}/2$. This is a significant AC voltage swing that poses great voltage stress on isolation devices. For MHF, the modules will experience a voltage swing with an amplitude $V_{dc}/4$. The ground voltage of a module will be decided by the switching state of its lower module. Hence the voltage swing of a MHF module equals to the module voltage. In MMC and MHF, the modules are connected in series at the power switching nodes. Consequently, the voltage of a module will change according to the turn-on and turn-off of

power switches in another module. The power switches will generate a voltage slope as high as tens of kV/μS. Moreover, resonance and overshoot during turn-on or turn-off, as well as the recovery of anti-parallel diode will make the case even worse. A very steep voltage slope will be experienced by the modules. Special design is needed to deal with the extreme voltage stress [80]. By comparison, in the proposed topology, all module capacitors are connected in series at the input. The ground of a module is very stable and only small capacitor ripples are presenting. The voltage slope equals to the capacitor ripples of the modules, which is usually < 0.1V/μS. Compare to MMC and MHF, this voltage slope is negligible. The voltage stress on the module is a steady DC bias and can be handled easily. The isolation devices will be smaller and cheaper in the proposed topology.

2.4.2 Voltage Stress on Motor Windings

The life span of a machine usually depends on its winding voltage stress and thermal stress. Common-mode voltage stress of the winding will result in bearing current and cause bearing failure. The common-mode voltage problem of the proposed converter will be solved by interleaving technique, as will be further explained in the following chapter in this thesis. In this section, the focus is on the winding voltage stress on the winding insulation system. Due to voltage source converter with PWM, repetitive voltage surges will be generated. The voltage surges accelerate the aging of insulation system and lead to stator winding failure.

The aging of insulation system is primarily due to partial discharge [81]. When the voltage across the insulation layer or the air gap between insulation layers exceeds their electric breakdown voltage, it will trigger a small electric spark, i.e. a partial discharge. The partial discharge will eventually erode insulation and lead to electrical aging.

For PWM motor drives, there also exist problems caused by the high dv/dt of power switches, resulting in overvoltage impulses due to long cable transmission line effect and imbalance voltage stress distribution [82][83]. Because of the existence of insulation capacitance, 50% of the fast voltage impulse is distributed over the turns in the first coil [84]. These problems can be solved by 1) using insulation materials suitable for PWM drives, 2) avoid air gaps between insulation layers to reduce partial discharge, 3) using multilevel converters to reduce voltage step, 4) apply IMMD structure to reduce the long cable effect and 5) reduce the dv/dt of switches.

To attenuate the insulation aging, the peak voltage stress on it must be reduced below the breakdown voltage [85]. The highest voltage stress is identified to locate at the terminals of the machine windings since they experience the overall phase to ground and phase to phase voltage.

	NPC, FC, CHB, MMC	MHF (n>3)	The proposed
Phase to ground voltage peak value	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
Phase to ground voltage p-p	V_{dc}	$2V_{dc}/n$	V_{dc}/n
Phase to phase voltage peak value	V_{dc}	$4V_{dc}/n$	V_{dc}/n
Phase to phase voltage p-p	V_{dc}	$4V_{dc}/n$	V_{dc}/n

Table 2.5. Voltage stress on machine terminals

In NPC, FC, CHB and MMC, the terminal voltages are the full range machine voltages. The terminals will experience a full range AC voltage for both phase to ground and phase to phase. In MHF and the proposed converter, there are more machine terminals for different voltage levels.

As a result, the voltage change at each terminal will be smaller. The phase to ground voltage on terminals will be a partial AC voltage plus a DC voltage. The phase to phase voltage is only a partial AC voltage. As a result, the voltage burden is reduced. The proposed converter is even better than MHF because the converter modules have steady grounds, not like MHF modules that have swing grounds.

For MHF and the proposed converter, however, the high frequency PWM switching voltage will add insulation burden. There are more terminals and more power cables exaggerate long cable effect. Hence IMMD is highly recommended for these two topologies. Using more modules is also desirable since the voltage on each module will reduced. If needed, filters can be added to protect the machine insulation. The filter size is small because of relatively high switching frequency.

2.5 Extended Topologies

2.5.1 Extended Topology with Multilevel Converter Modules

The proposed topology is a flexible, compatible modular design that can incorporate other multilevel building blocks instead of basic 2-level 3- phase bridge. The proposed topology in Fig. 2.3 can be easily extended to a class of multilevel motor drives. As shown in Fig. 2.12, in order to further increase the output voltage levels or reduce the number of motor winding leads, each module in the proposed topology can be NPC and FC instead of a two-level three-phase bridge.

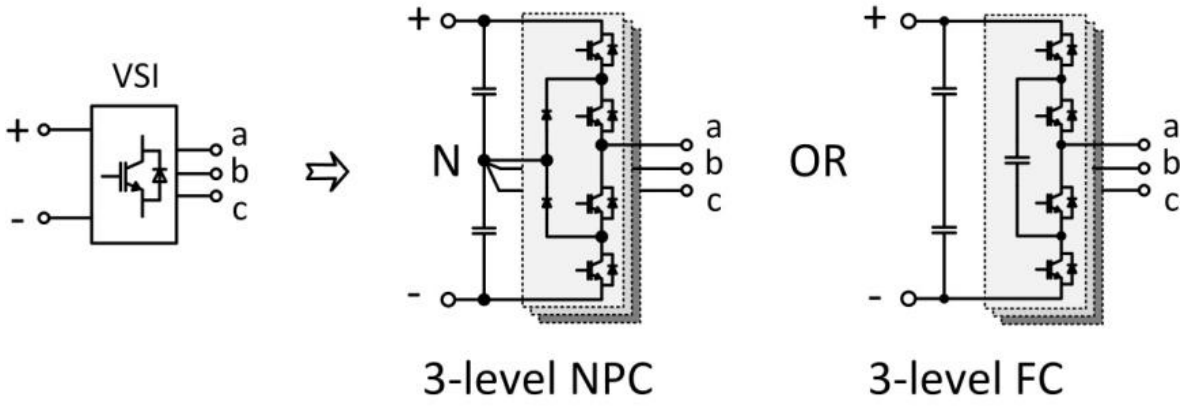
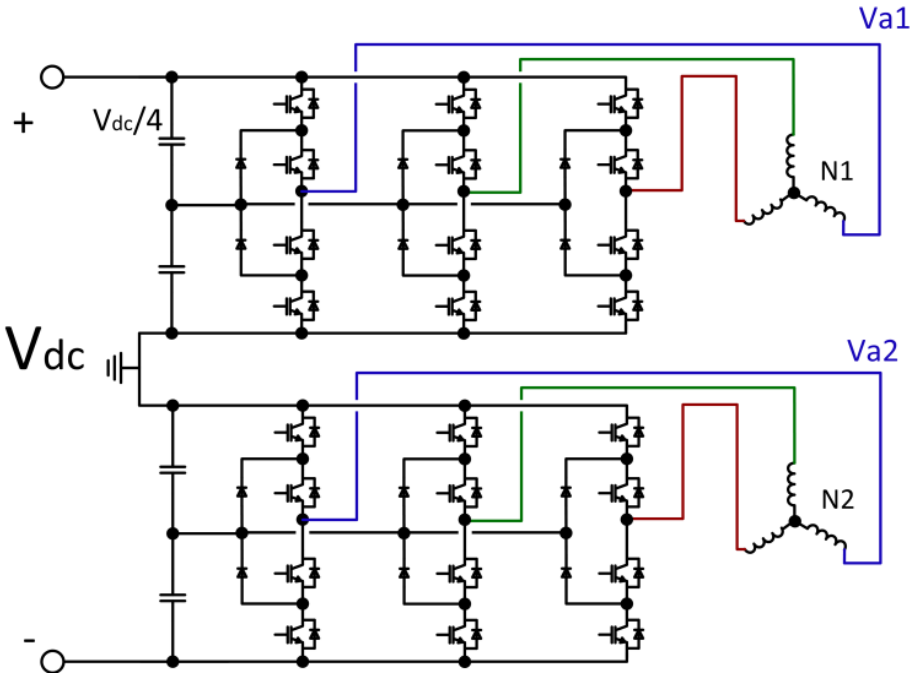


Fig. 2.12. The modules in the extended topology

The original proposed topology can realize 5-level by using four modules, and all the power components are rating at $V_{dc}/4$. If 3-level NPC or 3-level FC are used as the converter modules, it only needs two modules to realize 5-level with components rating at $V_{dc}/4$, as shown in Fig. 2.13. Meanwhile, the number of machine leads is reduced from 12 to 6.



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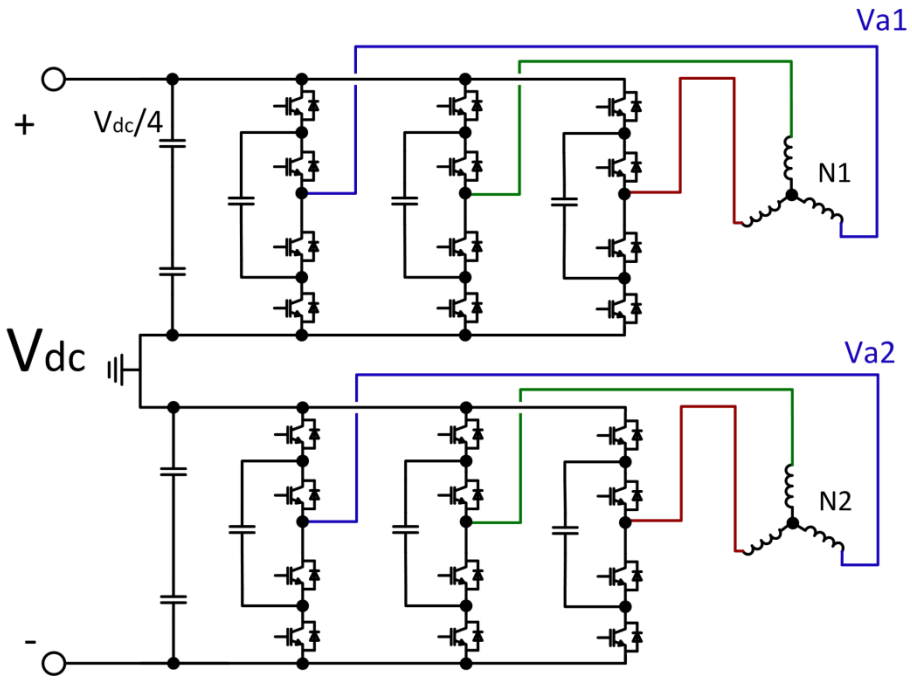

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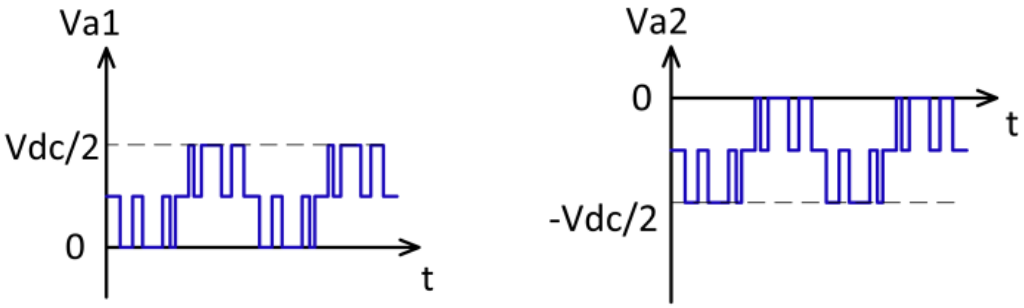


(c)

Fig. 2.13. The extended topologies

(a) 3-level NPCs as converter modules, (b) 3-level FCs as converter modules, and (c) the output multilevel voltage waveforms

NPC and FC topologies are not modular design and suffer from a quadratic increase of component quantity when the number of voltage levels increases. However, at only 3 levels, the

quadratic function does not affect much. Actually, 3-level NPC and 3-level FC are very common, standard and cost effective. The 3-level NPC does not have the power imbalance problem and can supply real power. The MMC can also be used as modules in the proposed topology, though it will result in a very large capacitor size due to the single phase structure of MMC.

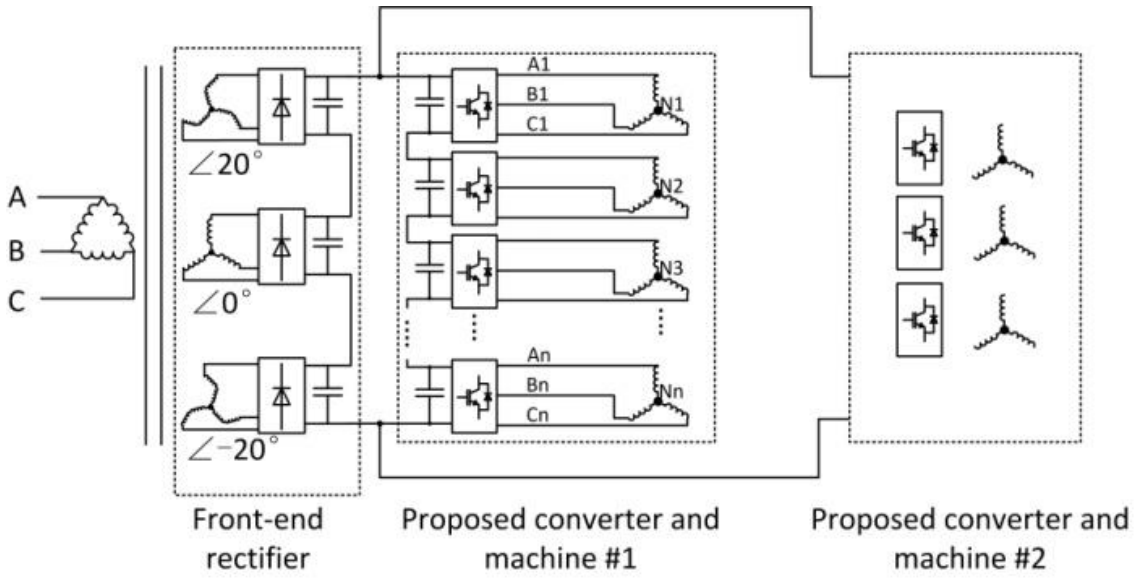
	NPC	FC	CHB	MMC	MHF	Proposed	NPC Extended with NPC	Extended with FC
Switches	24	24	24	24	24	24	24	24
Clamping diodes	36	0	0	0	0	0	12	0
Flying capacitors	0	18	0	0	0	0	0	6
Input DC sources	1	1	6	1	1	1	1	1
DC-bus capacitors	4	4	6	12	4	4	4	4
Machine leads	3	3	3	3	8	12	6	6

Table 2.6. Component quantities in different multilevel converters

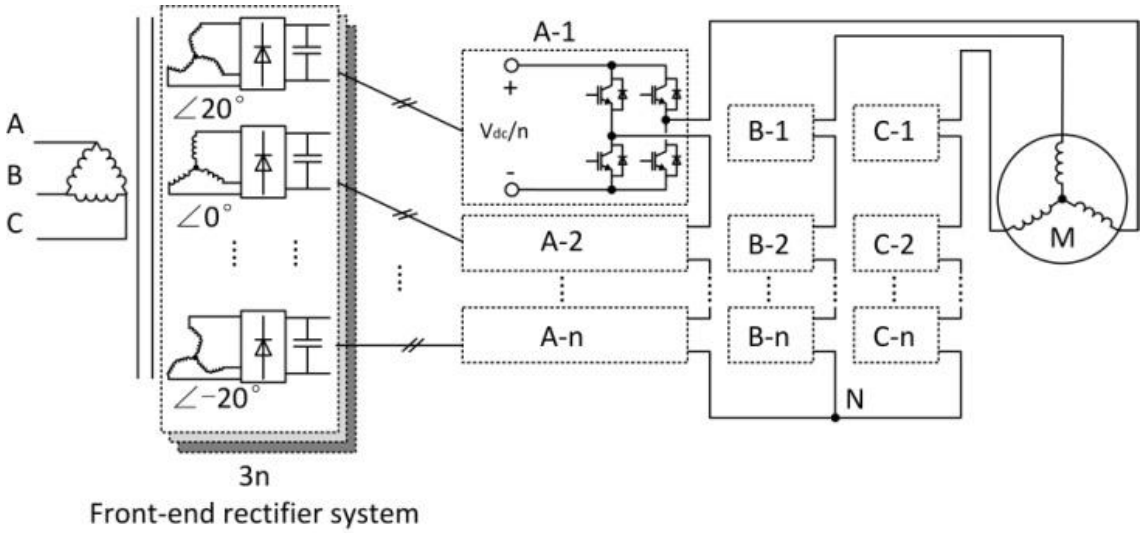
The proposed concept is flexible in using various combinations of machine leads, number of voltage levels and the module topologies. As shown in the following table, the cost and size are reduced if a 5-level NPC is replaced by extended topology with 3-level NPC, since the number of clamping diodes is only one third of a NPC. If the extended topology with FC is used instead of a 5-level FC, the number of flying capacitors also reduces from 18 down to 6. Moreover, the capacitor voltage of a 3-level NPC or FC is much easier to be balanced than the capacitor voltages of a 5-level NPC or FC.

2.5.2 Extended Topology with Flexible Frontend Rectifiers

The proposed design can be supplied by either a single dc source or several dc sources to power each module. The front-end rectifier design is separated from the multilevel converter. Whether or not a single rectifier, multiple 12-pulse rectifier, dc grid, or batteries supply the dc sources, the proposed design is always compatible. The voltage rating, power rating, and the number of front-end rectifier modules can be different from the number of modules used in the proposed multilevel converter. Several multilevel converters can also share the same rectifier such as in an industrial dc bus system. **Fig. 2.14**(a) shows two proposed multilevel converters sharing the same input rectifier and driving two individual machines. In comparison, **Fig. 2.14** (b) shows the complex front-end rectifiers for a CHB converter, which cannot share input rectifier with other converters.



(a)



(b)

Fig. 2.14. Frontend rectifier design

(a) Proposed converters drive two machines with the same input rectifier

(b) CHB converter needs multiple separate input rectifiers

2.6 Summary of the Proposed Topology

This chapter presents the proposed multilevel motor drive that utilizes the machine winding properties. The machine windings are not only acting as the loads of converter modules, but also acting as the isolation transformers to synthesis output voltages. Since the machine winding is used as part of the converter, no extra component is needed such as clamping diodes, flying capacitors, isolation transformers or filter inductors. Compare to other multilevel topologies, the proposed one achieves the minimum component quantity and simple structure.

All converter modules in the proposed topology are identical. The benefits of modular design include manufacturing cost reduction, faster product development, easy maintenance, and simple construction. In comparison, the NPC and FC topologies cannot be easily modularized because of uneven switching stresses. The CHB, MMC and MHF converters are modular designs but they need different gate signals for different modules, making control hardware complicated. The proposed topology can have (but not limited to) identical gate signals for different modules and hence they can share the signals from one PWM generator. This is more suitable for a fully modular design. By comparison, a MMC or MHF usually needs an FPGA to generate different PWM signals for every module.

The proposed three phase converter modules provide constant power instead of pulsating power as in single phase modules. Only switching ripples will present at the DC-link. This can significantly reduce the DC-link capacitance. Hence the size, weight and cost of the proposed topology are reduced.

The module voltage balancing in the proposed converter is very simple. As will be discussed later in this thesis, the proposed converter can operate normally even without voltage balancing control at all. The converter can rely on the motor windings to balance the module voltage. Alternatively, the module voltage can be controlled such that the power loss of a module is controlled by active thermal management to improve module reliability and lifespan [86].

The proposed topology has access to the voltage and current of all motor windings. This enables detection of machine faults quickly and accurately through the measurements of winding voltages and currents, and machine fault-tolerance can be improved [63]. Since there are several converter modules and require position measurements, it is also desirable to implement self-sensing technique so the machine's rotor position encoder can be eliminated and the reliability can be improved [87][88]..

Different from other topologies, the proposed one is the only one that can utilize three-phase multilevel modules such as 3-level NPC or FC as its own module. This allows a very flexible design for the proposed topology.

Compared to other topologies, the voltage stresses on converter modules and motor windings are reduced in the propose converter. The AC voltage stress on a converter module is almost negligible, and hence the cost of isolation devices in a converter module can be reduced. The AC voltage stress on the motor winding is also reduced, leading to longer motor lifespan.

The proposed topology increases the number of motor leads. Large motors usually have multiple leads for reconnection as discussed in [22][89]. Several ways to split the motor windings are also introduced in this chapter. The split winding will not change the motor design or motor properties at all. Moreover, the split windings can eliminate the interconnection end

windings that connect two different pole-pairs and require extra insulation. Without the end windings, the manufacture of a motor can be simpler.

The concept of integrated modular motor drive (IMMD) is very suitable for the proposed topology since IMMD eliminates the interconnection wires between the converter and the motor windings. The converter modules can be directly mounted on the local motor winding segments.

Chapter 3

Modeling and Control

The proposed input-series converter structure requires a machine with split winding segments. In this chapter, the modeling of the split winding machine is presented. For different winding configurations, the model is different. As will be shown in this chapter, the split winding machine can automatically balance the input-series converter modules, without any control. This chapter also presents optional voltage control methods which can provide better regulation of module voltages.

3.1 Modeling of Machine Segments in Different Pole Pairs

In section 2.2, winding configuration #1 illustrates how the machine segments are split according to the machine pole-pairs. The multiple machine segments are individually controlled by different converter modules, which is very different from a conventional machine. To clearly illustrate the behavior of one machine segment, closed form equations are derived in this section. The parameters are summarized as follows:

P : the number of machine poles

g : the equivalent air gap length

L_s : the length of machine stack

r_g : the average air gap radius

τ_p : length of one pole pitch

μ_0 : the vacuum permeability constant

N_i : the number of turns in coil i

I_i : the current in coil i

For simplification, the machine lamination is assumed to be perfect soft-magnet material with infinite permeability and negligible MMF drop. The entire MMF drop is confined within the air gap.

3.1.1 The Self-Inductance of One Coil

Different from a conventional machine, a single winding coil in a split machine will generate an asymmetry flux density. In the first step, it is desired to calculate the self-inductance of a single coil in one machine pole-pair. It is desirable to examine the machine through the view of machine air gap, as show in **Fig. 3.1**. Since the MMF drop in stator and rotor iron is ignored, the flux density is evenly distributed in the air gap. The polarity of flux density is changed at the coil locations, marked by the + and -. Notice that the flux density absolute values B_{in} and B_{out} are not necessarily identical because the width of air gap are not the same. It is different from a conventional analysis where the contributions from all pole-pairs are taken into consideration. As a consequence, the flux density absolute values will be identical along the air gap.

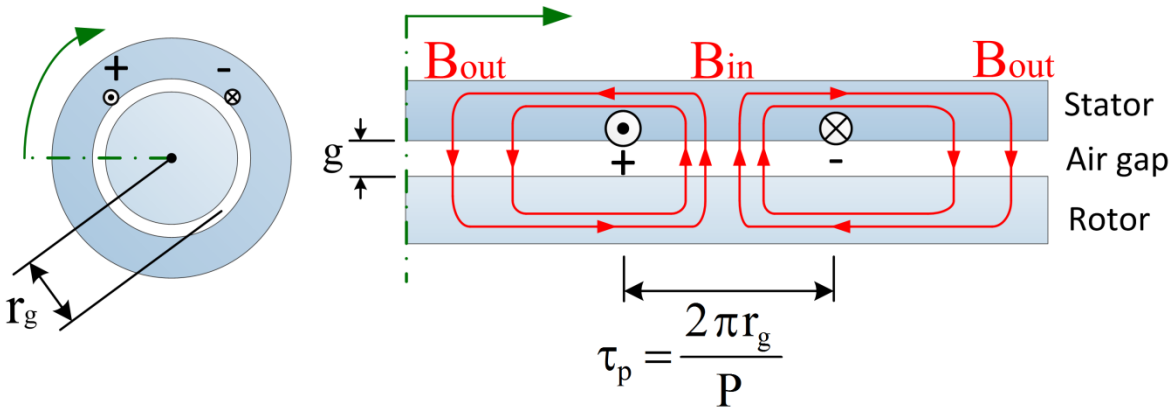


Fig. 3.1. Self-inductance of a single coil in a split winding machine

The reluctance of the inside air gap is:

$$R_{in} = \frac{g}{\mu_0 A_{in}} = \frac{g}{\mu_0 L_s \tau_p} = \frac{g}{2\pi r_g L_s \mu_0} P \tag{3.1}$$

The reluctance of air gap that is outside the pole pitch:

$$R_{out} = \frac{g}{\mu_0 A_{out}} = \frac{g}{\mu_0 L_s (2\pi r_g - \tau_p)} = \frac{g}{2\pi r_g L_s \mu_0} \frac{P}{P-1} \tag{3.2}$$

The total reluctance of the single coil:

$$R_{tot} = R_{in} + R_{out} = \frac{g}{2\pi r_g L_s \mu_0}\left(P + \frac{P}{P-1}\right) = \frac{g}{2\pi r_g L_s \mu_0}\left(\frac{P^2}{P-1}\right) \tag{3.3}$$

The self-inductance of the winding is:

$$L_1 = \frac{N_1^2}{R_{tot}} = \frac{2\pi r_g L_s N_1^2 \mu_0}{g}\left(\frac{P-1}{P^2}\right) \tag{3.4}$$

In conventional machine design [90], L1 is only half of the value of (3.4). This is because the number of turns N_1 is defined as the integration of sine-winding, which has the peak value of $N_1/2$, and the flux density is linked to a total of N_1 turns. The difference of self-inductance will not affect the final results.

The flux densities are calculated as:

$$B_{in} = \frac{\Phi_1}{A_{in}} = \frac{\lambda_1}{N_1 A_{in}} = \frac{L_1 I_1}{N_1 A_{in}} = \frac{N_1 \mu_0 I_1}{g}\left(\frac{P-1}{P}\right) \tag{3.5}$$

$$B_{out} = \frac{\Phi_1}{A_{out}} = \frac{B_{in} A_{in}}{A_{out}} = B_{in}\left(\frac{1}{P}\Big/\frac{P-1}{P}\right) = \frac{N_1 \mu_0 I_1}{g}\frac{1}{P} \tag{3.6}$$

3.1.2 The Mutual-Inductance between Two Coils

Assume there is a second coil shifted from coil #1 by a mechanical angle α. As shown in **Fig. 3.2**, the angle is within one pole-pair range so that the two coils are overlapped, i.e.

$$0 \le \alpha \le \frac{2\pi}{P}$$

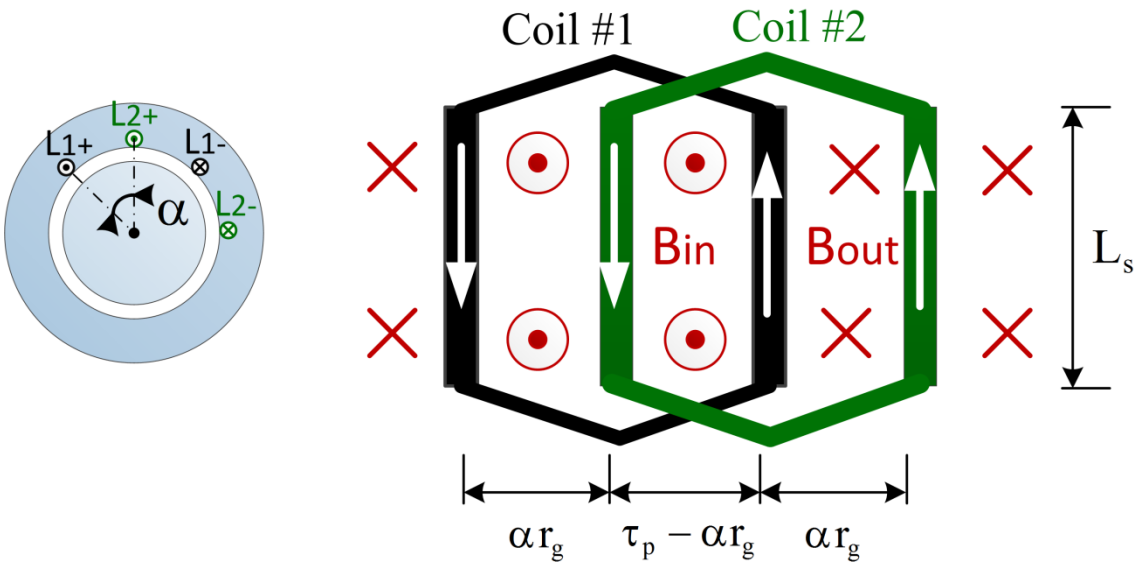


Fig. 3.2. Two overlapped coils

A portion of the flux created by coil #1 will be experienced by coil #2, which is corresponding to the mutual inductance.

$$\Phi_{12} = B_{in}A_{L2,in} - B_{out}A_{L2,out} = \frac{2\pi N_1 r_g \mu_0 L_s I_1}{g}\frac{P-1}{P^2}\left(1-\frac{\alpha}{2\pi}\frac{P^2}{P-1}\right) \tag{3.7}$$

Assume the number of turns of coil #1 and #2 are identical. The mutual inductance is:

$$L_{12} = \frac{\lambda_{12}}{I_1} = \frac{N_1\Phi_{12}}{I_1} = L_1\left(1-\frac{\alpha}{2\pi}\frac{P^2}{P-1}\right) \tag{3.8}$$

It is trivial and easy to extend the displacement angle α to negative value, i.e.,

$$-\frac{2\pi}{P} \le \alpha \le \frac{2\pi}{P}$$

And the mutual inductance will be:

$$L_{12} = L_1\left(1-\frac{|\alpha|}{2\pi}\frac{P^2}{P-1}\right) \tag{3.9}$$

It is also possible that the coil #2 is not overlapped with coil #1, as shown in **Fig. 3.3**.

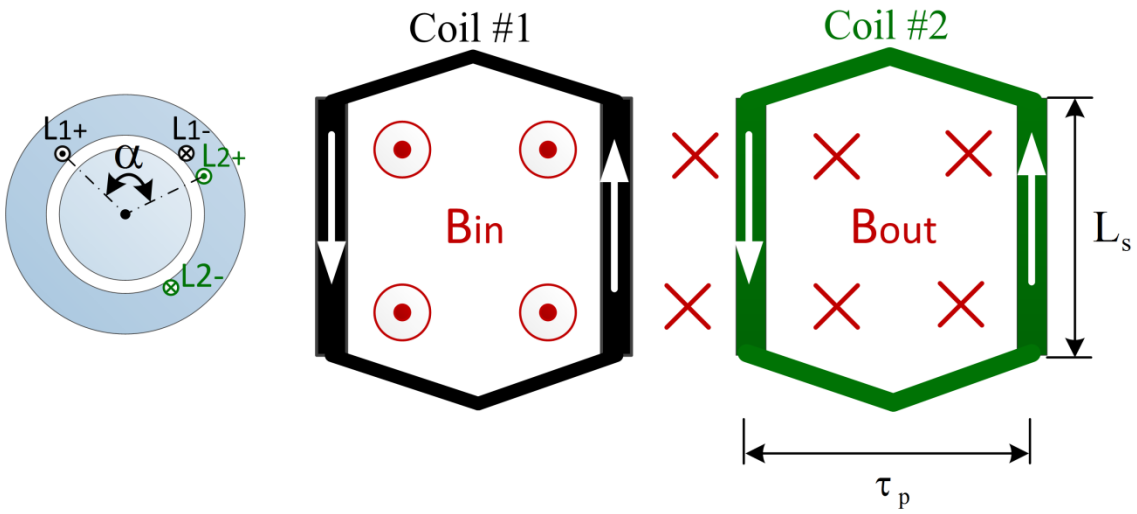


Fig. 3.3. Two non-overlapped coils

The flux experienced by coil #2 will no longer change with angle α.

$$\Phi_{12} = -B_{out}A_{L2} = -\frac{2\pi N_1 r_g \mu_0 L_s I_1}{g}\frac{P-1}{P^2}\frac{1}{P-1} \tag{3.10}$$

$$L_{12} = \frac{\lambda_{12}}{I_1} = \frac{N_1\Phi_{12}}{I_1} = L_1\left(-\frac{1}{P-1}\right) \tag{3.11}$$

As a summary, the mutual inductance between different coils is

$$L_{12} = L_1 \cdot k(\alpha) \tag{3.12}$$

$$k(\alpha)=\begin{cases}1-\dfrac{|\alpha|}{2\pi}\dfrac{P^2}{P-1} & ,|\alpha|\le\dfrac{2\pi}{P}\\ -\dfrac{1}{P-1} & ,|\alpha|>\dfrac{2\pi}{P}\end{cases} \tag{3.13}$$

, where L_1 is the self-inductance and k(α) is the mutual factor function, as shown in **Fig. 3.4**.

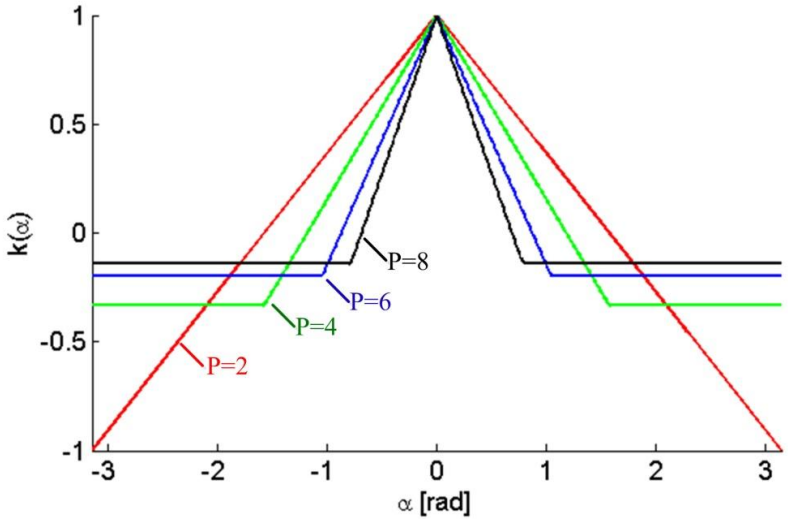


Fig. 3.4. The mutual factor function

This function can also be verified by FEA results. In FEA, a motor with 36 stator slots, 1 mm airgap length and 100 mm rotor radius will be investigated. The slot opening of this motor is 1/3 of slot pitch. There exists a Carter Factor that accounts for the influence of slot openings. The Carter Factor for this case is 1.26. There are 100 turns in each coil and the current is low to avoid saturation.

- **Motor with 2 Poles**

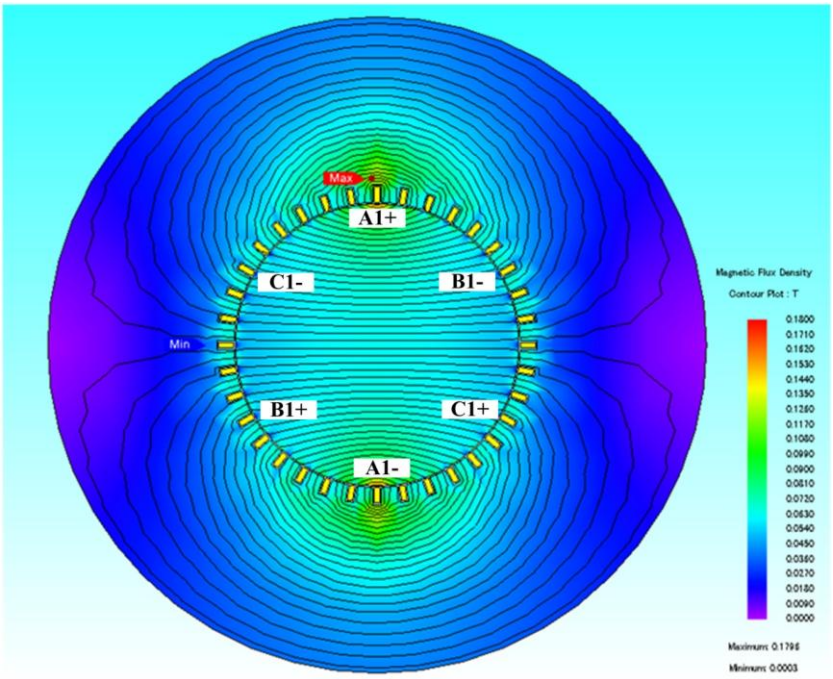


Fig. 3.5. FEA results for a 2-pole motor

Fig. 3.5 shows the FEA results for a 2 pole motor. In this motor, there are 3 coils occupying 6 slots. Each coil has a span of 18 slots and two coils are shifted by 12 slots. Since the motor has 2 poles, there is only one group of three phase coils. Only coil A1 is excited in FEA. **Table 3.1** shows the numerical values of the motor. L1a is the self-inductance of phase A1. K1a,1b stands for the mutual factor between phase A1 and phase B1 in pole-pair #1 (there is only one pole-pair in this motor). As can be seen in the table, the analytical results are consistent with the FEA results.

	Analytical	FEA results
L1a	1.567	1.564
K1a,1b	-0.333	-0.331
K1a,1c	-0.333	-0.331

Table 3.1. The comparison for the 2-pole motor

- **Motor with 4 Poles**

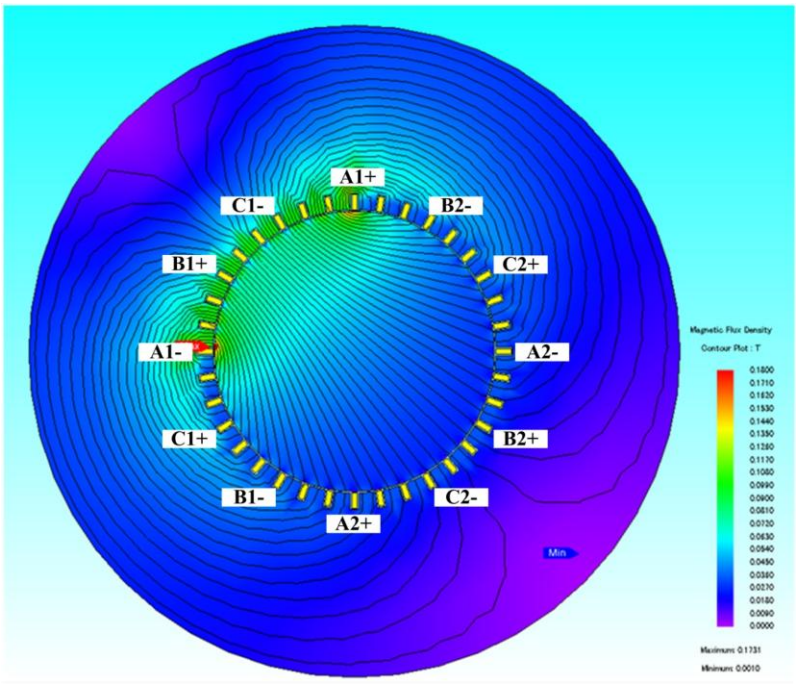


Fig. 3.6. FEA results for a 4-pole motor

	Analytical	FEA results
L1a	1.175	1.176
K1a,1b	0.111	0.116
K1a,1c	-0.556	-0.551
K1a,2a	-0.333	-0.331
K1a,2b	-0.333	-0.331
K1a,2c	0.333	0.331

Table 3.2. The comparison for the 4-pole motor

Different from the 2-pole motor, there are 2 sets of three-phase coils in the 4-pole motor. The span of a single coil is 9. Only A1 is excited in this case study. As can be seen in **Table 3.2**, all coils from pole-pair #2 have identical mutual factor -0.331 in FEA, which is consistent with the

analytical results. Notice that the C2 coil is in the reverse direction of **Fig. 3.3** so the mutual factor is positive.

- **Motor with 6 Poles**

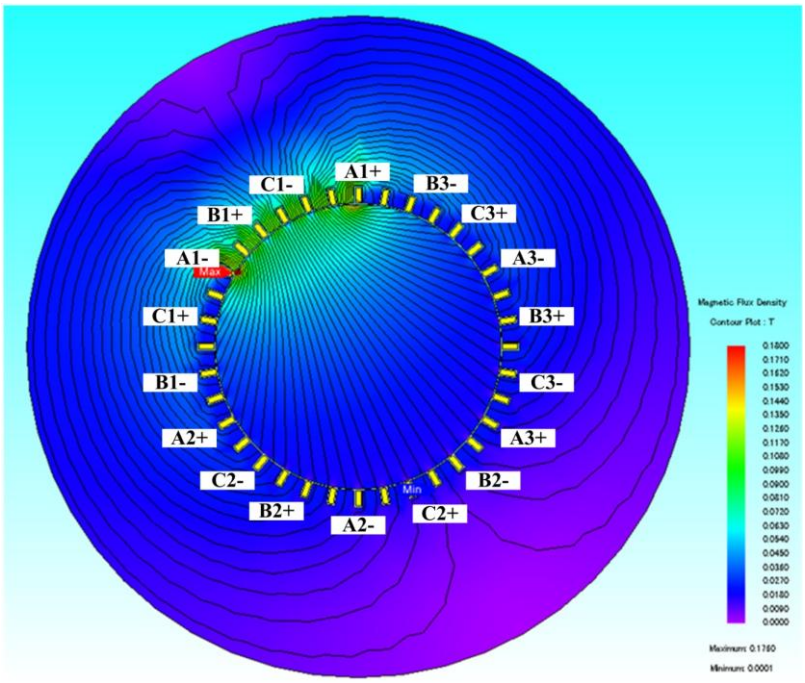


Fig. 3.7. FEA results for a 6-pole motor

	Analytical	FEA results
L1a	0.870	0.873
K1a,1b	0.200	0.198
K1a,1c	-0.600	-0.594
K1a,2a	-0.200	-0.198
K1a,2b	-0.200	-0.198
K1a,2c	0.200	0.198
K1a,3a	-0.200	-0.198
K1a,3b	-0.200	-0.198
K1a,3c	0.200	0.198

Table 3.3. The comparison for the 6-pole motor

Through the 2-pole, 4-pole and 6-pole FEA results, (3.4) and (3.12) are justified.

3.1.3 The Inductance Matrix of One Pole Pair

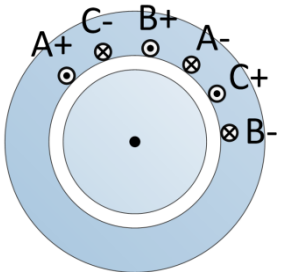


Fig. 3.8. The coil arrangements in one pole pair

In this section, we will briefly review the dq-axis inductance matrix of one pole-pair. The three-phase coils in one pole-pair are shown in **Fig. 3.8**. For motor with 2 poles, there does not exist non-overlapping pole-pairs. For motor with more than 2 poles, the phase C winding is in a reverse direction so the coils will fully occupy the pole pitch. Consequently, the coupling between C and other phases has a negative sign. According to the equations of last section, the inductance matrix of one pole pair can be developed as following:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = L_1 \begin{bmatrix} 1 & k_{1a,1b} & k_{1a,1c} \\ k_{1b,1a} & 1 & k_{1b,1c} \\ k_{1c,1a} & k_{1c,1b} & 1 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.14}$$

Define the inductance matrix of this pole-pair as:

$$L_{pole-pair} := L_1 \begin{bmatrix} 1 & k_{1a,1b} & k_{1a,1c} \\ k_{1b,1a} & 1 & k_{1b,1c} \\ k_{1c,1a} & k_{1c,1b} & 1 \end{bmatrix} \tag{3.15}$$

, and according to (3.12) ,

$$k_{1a,1b} = k_{1b,1a} = k\left(\frac{120°}{P/2}\right) = \frac{P-3}{3P-3}$$

$$k_{1a,1c} = k_{1c,1a} = k_{1b,1c} = k_{1c,1b} = -k\left(\frac{60°}{P/2}\right) = -\frac{2P-3}{3P-3}$$

Then (3.14) becomes:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = L_{pole-pair}\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.16}$$

The inductance matrix in abc-axis is the fundamental matrix. However, it is not convenient for motor control. It is more useful to develop the inductance matrix in dq-axis. Park transform is used to convert abc-axis into dq-axis with an arbitrary reference angle θ.

$$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta-\frac{2\pi}{3}) & -\sin(\theta+\frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} := P_{park}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{3.17}$$

, where x denotes either voltage or current.

With park transform,

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{d}{dt}\left\{P_{park}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}\right\} = \left(\frac{d}{dt}P_{park}\right)\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + P_{park}\left(\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}\right) \tag{3.18}$$

Hence

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = P_{park}^{-1}\left(\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} - \left(\frac{d}{dt} P_{park} \right)\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \right) \tag{3.19}$$

It is trivial to prove by definition of park transform that

$$\left(\frac{d}{dt} P_{park} \right)\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \omega \begin{bmatrix} i_q \\ -i_d \\ 0 \end{bmatrix} \tag{3.20}$$

, where ω is the reference speed and equals to the time derivative of θ.

Based on (3.19) and (3.20), (3.16) becomes

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = P_{park} L_{pole-pair} \frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = P_{park} L_{pole-pair} P_{park}^{-1} \left[\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} - \omega \begin{bmatrix} i_q \\ -i_d \\ 0 \end{bmatrix} \right] \tag{3.21}$$

Define

$$L_{dq-pole} = P_{park} L_{pole-pair} P_{park}^{-1} \tag{3.22}$$

Then

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = L_{dq-pole} \frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} - L_{dq-pole} \begin{bmatrix} \omega i_q \\ -\omega i_d \\ 0 \end{bmatrix} \tag{3.23}$$

This form is the well-known stator dq-axis model. It consists of an inductance term and a speed related cross-coupling term. However the numerical value is a little different from the

conventional dq model. Since only one pole-pair in the motor is considered, the matrix $L_{dq-pole}$ in (3.23) is actually not a diagonal matrix. Instead, it is a time variant, non-diagonal matrix.

3.1.4 The Inductance Matrix of Two Pole Pairs

Based on (3.13) and (3.16), the inductance matrix can be extended to two pole pairs, in abc-axis.

$$\begin{bmatrix} v_{a1} \\ v_{b1} \\ v_{c1} \\ \cdots\cdots \\ v_{a2} \\ v_{b2} \\ v_{c2} \end{bmatrix} = \begin{bmatrix} & L_{pole-pair} & \vdots & L_1\left(-\frac{1}{P-1}\right) & L_1\left(-\frac{1}{P-1}\right) & L_1\left(\frac{1}{P-1}\right) \\ & & \vdots & L_1\left(-\frac{1}{P-1}\right) & L_1\left(-\frac{1}{P-1}\right) & L_1\left(\frac{1}{P-1}\right) \\ & & \vdots & L_1\left(\frac{1}{P-1}\right) & L_1\left(\frac{1}{P-1}\right) & L_1\left(-\frac{1}{P-1}\right) \\ \cdots\cdots & \cdots\cdots & \cdots\cdots & \cdots\cdots & \cdots\cdots & \cdots\cdots \\ L_1\left(-\frac{1}{P-1}\right) & L_1\left(-\frac{1}{P-1}\right) & L_1\left(\frac{1}{P-1}\right) & \multicolumn{3}{c}{\multirow{3}{*}{$L_{pole-pair}$}} \\ L_1\left(-\frac{1}{P-1}\right) & L_1\left(-\frac{1}{P-1}\right) & L_1\left(\frac{1}{P-1}\right) & & & \\ L_1\left(\frac{1}{P-1}\right) & L_1\left(\frac{1}{P-1}\right) & L_1\left(-\frac{1}{P-1}\right) & & & \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{a1} \\ i_{b1} \\ i_{c1} \\ \cdots\cdots \\ i_{a2} \\ i_{b2} \\ i_{c2} \end{bmatrix} \tag{3.24}$$

If we define

$$\begin{bmatrix} v_{a1} \\ v_{b1} \\ v_{c1} \end{bmatrix} = L_1\left(-\frac{1}{P-1}\right) \begin{bmatrix} 1 & 1 & -1 \\ 1 & 1 & -1 \\ -1 & -1 & 1 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{a2} \\ i_{b2} \\ i_{c2} \end{bmatrix} := L_{mutual} \frac{d}{dt} \begin{bmatrix} i_{a2} \\ i_{b2} \\ i_{c2} \end{bmatrix} \tag{3.25}$$

Then (3.24) becomes

$$\begin{bmatrix} v_{abc1} \\ \cdots\cdots \\ v_{abc2} \end{bmatrix} = \begin{bmatrix} L_{pole-pair} & \vdots & L_{mutual} \\ \cdots\cdots & & \cdots\cdots \\ L_{mutual} & \vdots & L_{pole-pair} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{abc1} \\ \cdots\cdots \\ i_{abc2} \end{bmatrix} \tag{3.26}$$

The park transform on two different pole pairs will be

$$\begin{bmatrix} X_{dq1} \\ \cdots\cdots \\ X_{dq2} \end{bmatrix} = \begin{bmatrix} P_{park} & \vdots & 0 \\ \cdots\cdots & & \cdots\cdots \\ 0 & \vdots & P_{park} \end{bmatrix} \begin{bmatrix} X_{abc1} \\ \cdots\cdots \\ X_{abc2} \end{bmatrix} \tag{3.27}$$

, where X_{abci} and X_{dqi} represents the voltage or current vector in abc-axis and dq-axis respectively.

Then (3.19) can be extended to two pole-pairs.

$$\frac{d}{dt}\begin{bmatrix} i_{abc1} \\ \cdots\cdots \\ i_{abc2} \end{bmatrix} = \begin{bmatrix} P_{park}^{-1} & \vdots & 0 \\ \cdots\cdots & & \cdots\cdots \\ 0 & \vdots & P_{park}^{-1} \end{bmatrix} \bullet \left\{ \frac{d}{dt}\begin{bmatrix} i_{dq1} \\ \cdots\cdots \\ i_{dq2} \end{bmatrix} - \left(\frac{d}{dt}\begin{bmatrix} P_{park} & \vdots & 0 \\ \cdots\cdots & & \cdots\cdots \\ 0 & \vdots & P_{park} \end{bmatrix} \right) \bullet \begin{bmatrix} i_{abc1} \\ \cdots\cdots \\ i_{abc2} \end{bmatrix} \right\} \tag{3.28}$$

Based on (3.22), (3.26) and (3.28),

$$\begin{bmatrix} v_{dq1} \\ \cdots\cdots \\ v_{dq2} \end{bmatrix} = \begin{bmatrix} P_{park} & \vdots & 0 \\ \cdots\cdots & & \cdots\cdots \\ 0 & \vdots & P_{park} \end{bmatrix} \begin{bmatrix} v_{abc1} \\ \cdots\cdots \\ v_{abc2} \end{bmatrix} = \begin{bmatrix} P_{park} & \vdots & 0 \\ \cdots\cdots & & \cdots\cdots \\ 0 & \vdots & P_{park} \end{bmatrix} \begin{bmatrix} L_{pole-pair} & \vdots & L_{mutual} \\ \cdots\cdots & & \cdots\cdots \\ L_{mutual} & \vdots & L_{pole-pair} \end{bmatrix} \frac{d}{dt}\begin{bmatrix} i_{abc1} \\ \cdots\cdots \\ i_{abc2} \end{bmatrix}$$

$$= \begin{bmatrix} L_{dq-pole} & \vdots & P_{park} L_{mutual} P_{park}^{-1} \\ \cdots\cdots & & \cdots\cdots \\ P_{park} L_{mutual} P_{park}^{-1} & \vdots & L_{dq-pole} \end{bmatrix} \bullet \left\{ \frac{d}{dt}\begin{bmatrix} i_{dq1} \\ \cdots\cdots \\ i_{dq2} \end{bmatrix} - \left(\frac{d}{dt}\begin{bmatrix} P_{park} & \vdots & 0 \\ \cdots\cdots & & \cdots\cdots \\ 0 & \vdots & P_{park} \end{bmatrix} \right) \bullet \begin{bmatrix} i_{abc1} \\ \cdots\cdots \\ i_{abc2} \end{bmatrix} \right\} \tag{3.29}$$

The equation is no difference for pole-pair #1 or #2. Hence we will only focus on the pole-pair #1 of (3.29). Denote

$$L_{dq-mutual} = P_{park} L_{mutual} P_{park}^{-1} \tag{3.30}$$

The first three rows of (3.29) becomes

$$\begin{bmatrix} v_{d1} \\ v_{q1} \\ v_{01} \end{bmatrix} = L_{dq-pole}\left\{\frac{d}{dt}\begin{bmatrix} i_{d1} \\ i_{q1} \\ i_{01} \end{bmatrix} - \begin{bmatrix} \omega i_{q1} \\ -\omega i_{d1} \\ 0 \end{bmatrix}\right\} + L_{dq-mutual}\left\{\frac{d}{dt}\begin{bmatrix} i_{d2} \\ i_{q2} \\ i_{02} \end{bmatrix} - \begin{bmatrix} \omega i_{q2} \\ -\omega i_{d2} \\ 0 \end{bmatrix}\right\} \tag{3.31}$$

This equation at this moment has a lack of technical meaning because this model is still a cross-coupled model. It is desirable to find a proper matrix operation such that the machine model becomes decoupled, so the conventional control method can be used to control the machine. This process is also called manipulate input decoupling.

Given the fact that the machine is either Y-connection or delta-connection and both the zero-axis voltage and current are zero, the third row of (3.31) is always zero. Consequently, performing any matrix operation on the third row will not change the equality of (3.31).

The equality will maintain when the third row is multiplied by a scalar and then it is subtracted from the first and second row respectively. There exists a special row operation matrix that will result in desirable results. The row operation matrix is:

$$M_r = \begin{bmatrix} 1 & 0 & -k_{lc1} \\ 0 & 1 & -k_{lc2} \\ 0 & 0 & 1 \end{bmatrix} \tag{3.32}$$

, where

$$k_{lc1} = 2\left[\cos(\theta) + \cos(\theta - \frac{2}{3}\pi) - \cos(\theta + \frac{2}{3}\pi)\right]$$

$$k_{lc2} = -2\left[\sin(\theta) + \sin(\theta - \frac{2}{3}\pi) - \sin(\theta + \frac{2}{3}\pi)\right]$$

Then (3.31) yeilds

$$\mathbf{M}_r\begin{bmatrix} v_{d1} \\ v_{q1} \\ v_{01} \end{bmatrix} = \begin{bmatrix} v_{d1} \\ v_{q1} \\ v_{01} \end{bmatrix} = \mathbf{M}_r\mathbf{L}_{dq-pole}\left\{\frac{d}{dt}\begin{bmatrix} i_{d1} \\ i_{q1} \\ i_{01} \end{bmatrix} - \begin{bmatrix} \omega i_{q1} \\ -\omega i_{d1} \\ 0 \end{bmatrix}\right\} + \mathbf{M}_r\mathbf{L}_{dq-mutual}\left\{\frac{d}{dt}\begin{bmatrix} i_{d2} \\ i_{q2} \\ i_{02} \end{bmatrix} - \begin{bmatrix} \omega i_{q2} \\ -\omega i_{d2} \\ 0 \end{bmatrix}\right\} \tag{3.33}$$

With the row operation matrix $\mathbf{M}_r$, it can be proved that the upper-left 2 by 2 submatrix of $\mathbf{M}_r\mathbf{L}_{dq-pole}$ is a diagonal, time-invariant matrix decided by the self-inductance of the winding coil, and the upper-left 2 by 2 submatrix of $\mathbf{M}_r\mathbf{L}_{dq-mutual}$ is always zero. Technically speaking, the undesirable coupling terms are decoupled in this operation.

The third row of (3.33) has no function for motor control so it is neglected. The first two rows of (3.33) are:

$$\begin{bmatrix} v_{d1} \\ v_{q1} \end{bmatrix} = \mathbf{L}_1\begin{bmatrix} \frac{2P}{3P-3} & 0 \\ 0 & \frac{2P}{3P-3} \end{bmatrix}\left\{\frac{d}{dt}\begin{bmatrix} i_{d1} \\ i_{q1} \end{bmatrix} - \begin{bmatrix} \omega i_{q1} \\ -\omega i_{d1} \end{bmatrix}\right\} \tag{3.34}$$

Zero-axis voltages and currents are always zero, which is guaranteed by the proposed topology. There is zero coupling between the pole-pair#1 and the pole-pair#2. There is also zero coupling between the d-axis and q-axis within the pole-pair#1.

Typically, the machine coil is not concentrated. Instead, it is distributed sinusoidally. This will affect the value of the non-zero terms in (3.34), but will not change the nature of the results.

3.1.5 Summary of Machine Modeling

(3.34) is a conventional dq model for the split winding machine. Each pole-pair segment of the machine can be represented by an independent equation. As long as the zero-axis current is zero, there will be no coupling between different non-overlapping pole-pairs.

As a summary,

- Machine segments in different pole-pairs have no dq-axis coupling between each other.
- An individual machine pole-pair behaves as a smaller machine with a classical decoupled dq model.
- Although machine segments are not coupled magnetically, they are still tied to the same rotor shaft and share the mechanical properties. The control method introduced in [91] can be applied.
- The zero-axis coupling between two segments is not zero. Under abnormal condition (short circuit or open circuit), the zero-axis current/voltage may not be zero, which may directly change the flux level at the local pole-pair, and indirectly affect other pole-pairs.

3.2 Converter Control for Machine Segments in Different Pole Pairs

The proposed converter topology has an input-series structure. The control of the converter has two tasks. The first, of course, is to control the machine. Conventional methods, such as open loop V/f control, closed loop current control or direct torque control, should be able to implement. The second task is to control the voltage of each converter module. Unbalanced module voltages degrade the fault tolerance and control stability of the converter. It will also damage the devices when the module voltage exceeds its limit. To prevent this from happening, converter voltage control methods must be investigated.

3.2.1 Fundamentals of Voltage Balancing

The voltage balancing problem has long existed in series-connected capacitors. The capacitors can be balanced by passive resistors, which are connected in parallel with the capacitors. The resistor shares the same voltage with the corresponding capacitor. When there exist voltage differences on the capacitors, the currents flowing through the resistors will be different. Larger voltage results in larger current consumption on the resistor. The resistor current will discharge the corresponding capacitor so the voltage will drop. These passive resistors usually have large values in the range of 10 kΩ. The current balancing capability of these resistors is 100 μA/V, which is sufficient for balancing the capacitor since the imbalance of capacitor leakage current is small. The balancing capability will increase when the resistors have smaller values. However, the steady state Ohmic loss will increase significantly.

For the proposed topology, similar idea can be applied. For simplicity, an equivalent circuit for converter with 2 series-connected modules is shown in Fig. 3.9. Assume the voltages on two modules are V1 and V2 respectively. The currents I1 and I2 are the current consumptions of converter modules. When I1 and I2 have mismatches, the voltages V1 and V2 will be different. Consequently, the resistor currents IR1 and IR2 will compensate for the voltage difference. As long as the resistance is small and hence the compensation is strong enough, it will keep the voltages almost equal.

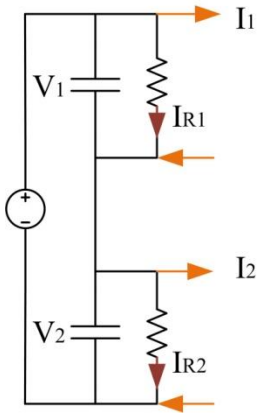


Fig. 3.9. Equivalent circuit for converter with 2 series-connected modules

This idea can be easily extended to a more general case that multiple converter modules are connected in series. The advantage of more modules is that when losing one module, other healthy modules will share the total input voltage equally. When there are only two modules, the healthy one will have to hold 200% of its rated voltage. When there are N modules, the healthy ones will hold N/(N-1) of their rated voltages.

3.2.2 Passive Voltage Balancing

Passive voltage balancing refers to the methods that do not require any control technique. Instead, the voltage balancing is achieved in the circuit level.

In DC-DC converters, the series-connected modules can be driven by identical gate signals and it will be stable. This method is called ‘common duty-ratio’ [92][93][94]. For the proposed converter, since the motor is built symmetry and the motor segments are identical, common duty-ratio method is also applied.

When the motor segments are identical and converter gate signals are identical, each series-connected module will be the same. Any module with a larger voltage will have a larger motor winding current and vice versa. The larger winding current will damp the extra voltage and maintain the module voltage to be equal to other modules. The common duty-ratio method is actually utilizing the motor windings as identical loads to balance the module voltages.

However, by this method the converter modules cannot have identical voltages when there are mismatches on machine segments. The mismatches may be caused by manufacture asymmetry, partial saturation of motor, unbalanced magnetics, or a fault with motor windings or converter modules.

The asymmetry of motor segments is typically very small. The small mismatch will result in unbalanced module voltages, but the unbalance is negligible. **Fig. 3.10** illustrates the experiment result of the proposed converter with 2 modules. In the first second, the total DC-link voltage is rising to 100 V in 4 steps. Then the voltage supply is cut so the DC-link voltage is damping exponentially. The converter modules are programmed to have same duty ratios. As can be seen in the figure, the module voltages maintain balanced, i.e., the module voltages are always half of the total DC-link voltage during the whole cycle.

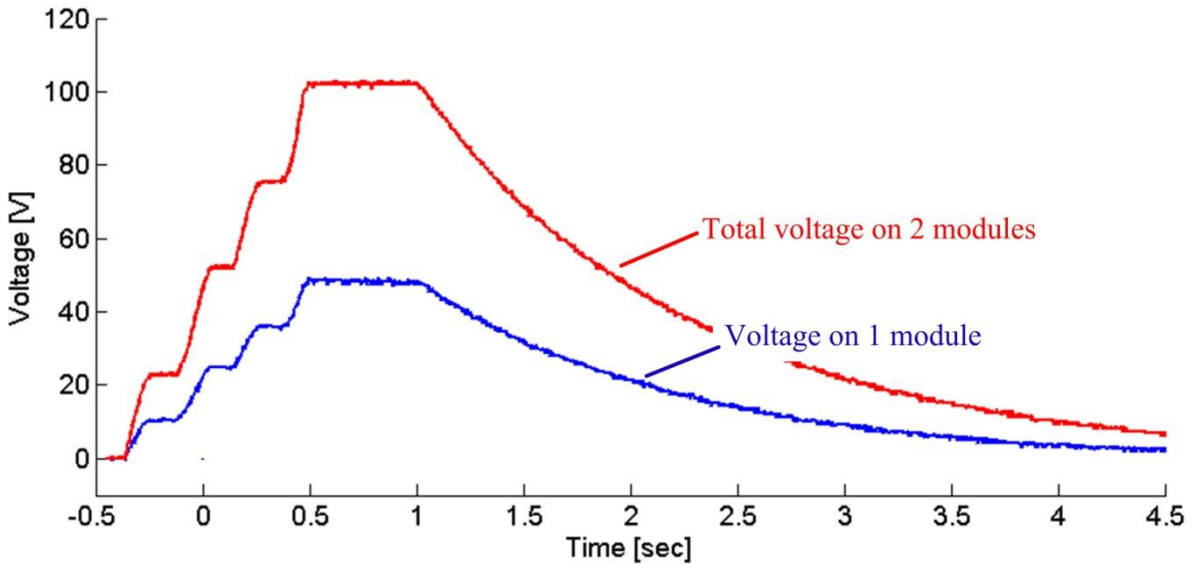


Fig. 3.10. Experiment result for passive voltage balancing

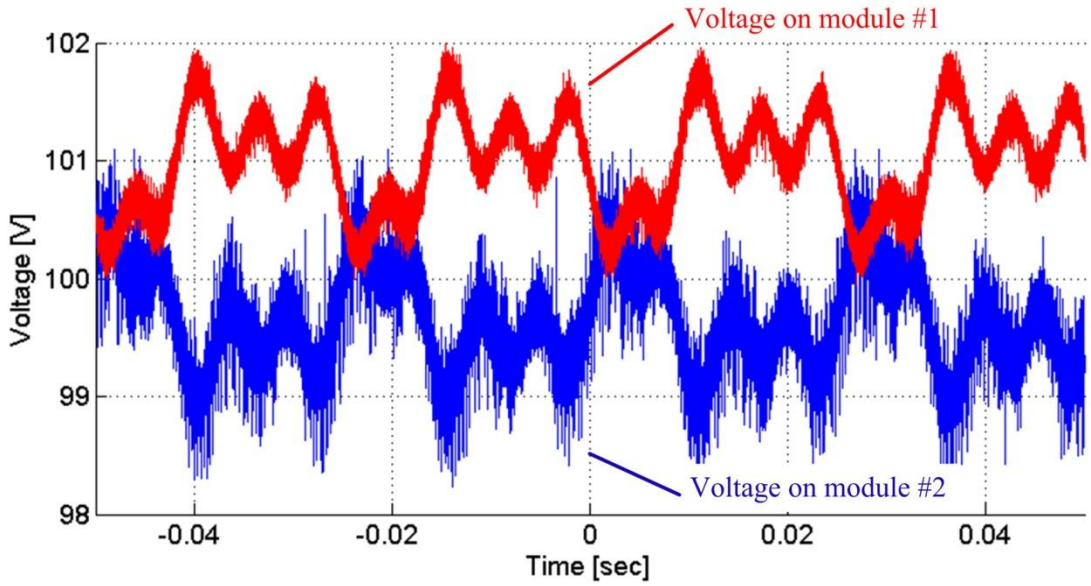


Fig. 3.11. Experiment result of zoomed in voltage ripples under full load

There actually exists very tiny mismatch between the two modules. Under full load operation, the module voltages are recorded and zoomed in, as shown in **Fig. 3.11**. The voltages of two

modules have a DC bias as well as AC components. The DC bias is typically caused by the mismatch of capacitors, semiconductor devices or static eccentricity of motor shaft [95]. The AC components, as shown in the figure, have a fundamental component and a fourth harmonic. The fundamental component could be caused by dynamic eccentricity of rotor [96]. The harmonics could be caused by the stator or rotor slot openings.

The experiment results illustrate that the mismatches of the motor segments and converter modules are typically not large enough to affect the module voltage significantly. The voltage balancing can be achieved by paralleling a resistor at 10 kΩ. If a larger balancing ability is needed, a hardware voltage balancer with semiconductor switch [97][98] can be added. Compared to a pure resistor solution, it has large balancing current but small steady state loss.

In order to better protect the converter module under fault conditions when there is a large mismatch, a chopper circuit can be added to each module. The chopper resistor does not need to be a large power resistor. Instead, it is fine as long as the resistor can discharge the module DC-link capacitor safely. Of course, the chopper resistor can be a large power resistor and act as the full-power breaking chopper. As a summary, the passive voltage balancing circuit schematic is shown in **Fig. 3.12**.

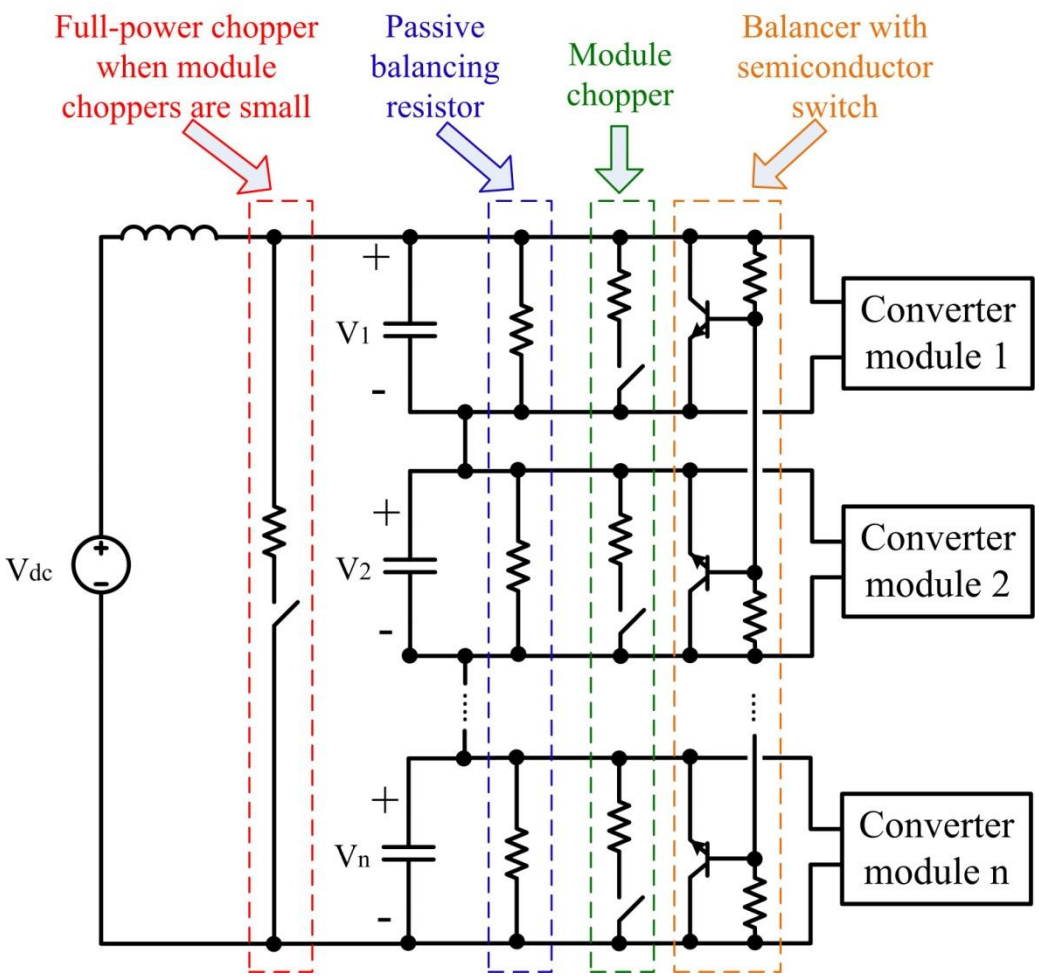


Fig. 3.12. Illustration of different techniques for passive voltage balancing method

3.2.3 Centralized Voltage Balancing Control

In the passive voltage balancing control, the converter can shut down safely when large mismatch presents. However, it is not possible for the converter to keep operating under such condition otherwise there will be a large amount of power dissipated by the balancing circuits.

Fig. 3.13 shows a simulation schematic with large mismatch on the loads. The three-phase loads are RL loads with different resistor values. The top module, module #1, has a light load

because the resistor value is intentionally increased. Besides, in phase A there is also an AC disturbance of which the amplitude is 10% rated voltage. As shown in **Fig. 3.14**, the module input voltages are 120 V and 80 V respectively, which are 20% away from the rated value, 100V. This is because the module #1 has larger resistors and absorbs lower current. The current difference between the modules will charge the capacitor in module #1 and discharge module #2 until the load current becomes identical. The voltage disturbance in phase A also cause an AC swing on the DC-link voltages of both modules.

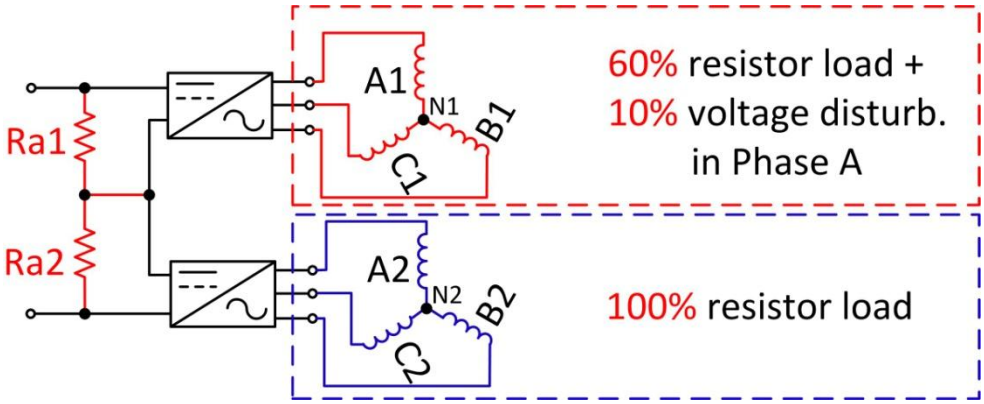


Fig. 3.13. Simulation model for machine segments with large mismatch

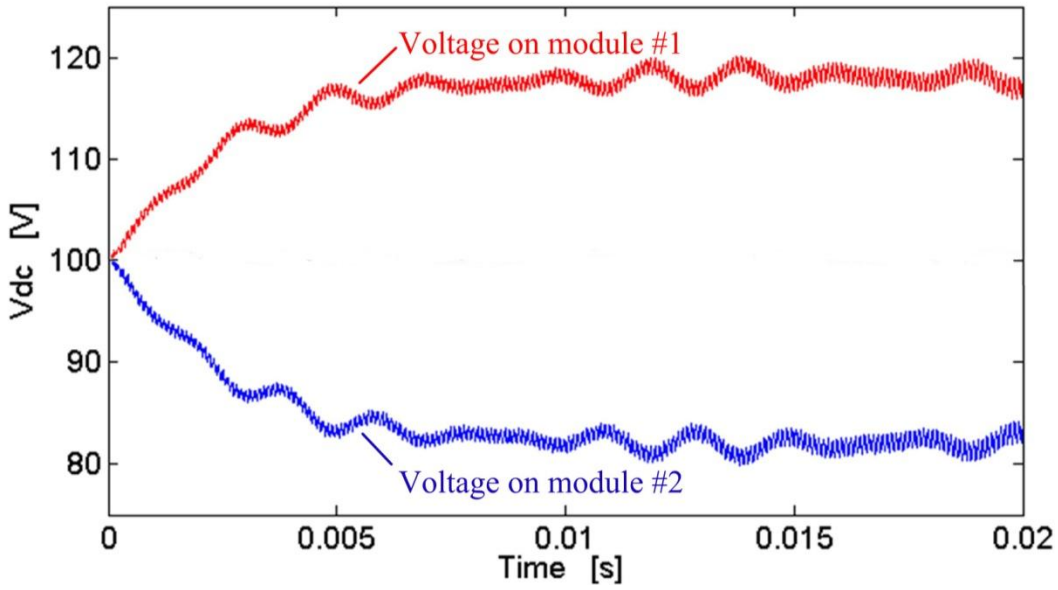


Fig. 3.14. Simulation result for machine segments having large mismatch

In order to operate the converter under such abnormal conditions, a simple but effective method is proposed in this thesis. Similar to passive balancing method, the modules of the motor drive is using common duty ratio control, i.e., identical gate signals. When any module voltage does not equal to the others, there will be an adjustment on the duty ratio of this module. Similar work has been done in Input-Series-Output-Parallel DC-DC converters [99][100][101][102] and in Input-Series-Output-Independent DC-DC converter [103]. For the proposed motor drive, it is different from DC-DC converters since both d-axis and q-axis are involved in the AC system.

Fig. 3.15 illustrates the diagram for the proposed centralized voltage balancing (CVB) control. The current controller is just a normal one as in a conventional motor drive. It treats the motor as a single piece without any information of the module voltages. The outputs of the current controller are the voltage commands, i.e., the duty ratios.

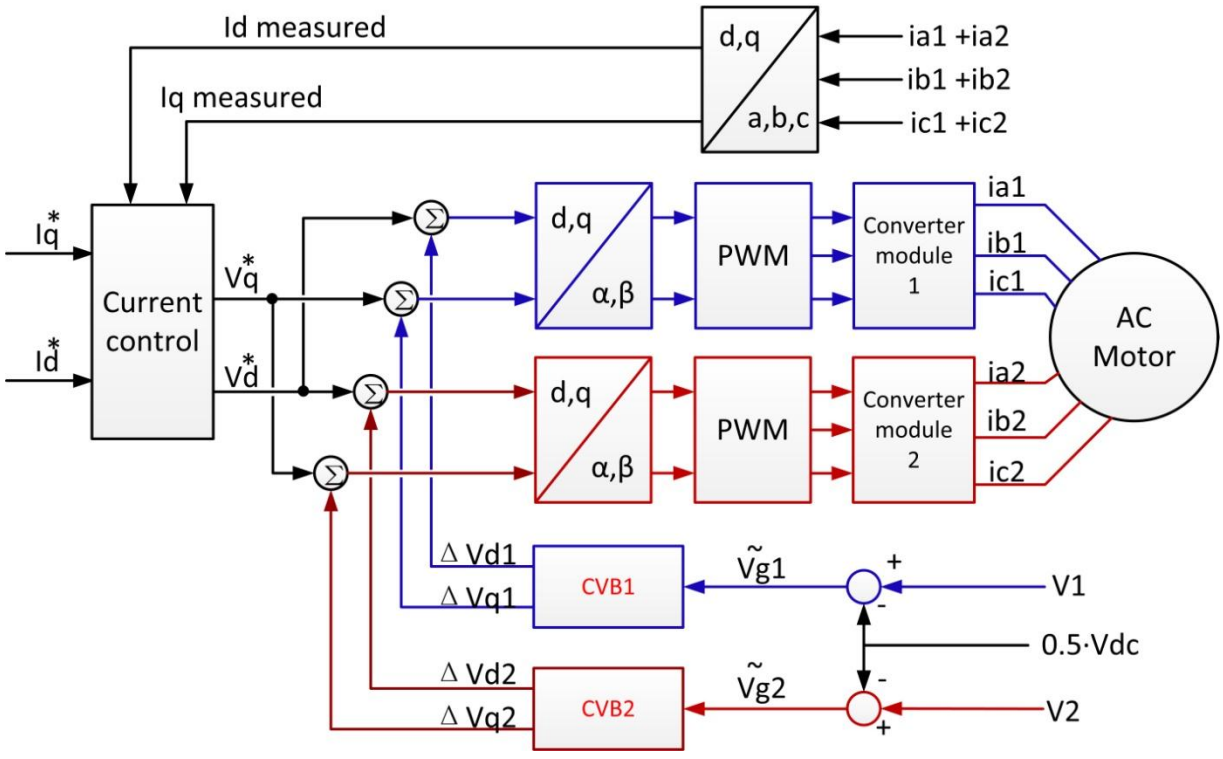


Fig. 3.15. Control diagram for CVB

The input of the CVB is the voltage mismatch of the corresponding module. When the module voltage is not the desired value, the controller will generate an adjustment value to compensate the duty ratio. An intuitive way to generate the adjustment value is to use a proportional gain between the input and output, i.e., voltage mismatch and adjustment value respectively. When the module voltage is higher than the desired value, the duty ratio is changed in the direction such that the output current is increased to dissipate the extra energy on the module.

This method creates an equivalent parallel resistor, with very small value and no power loss, as indicated by Ra1 and Ra2 in **Fig. 3.13**. The performance of the equivalent resistor actually depends on the dynamic of the motor winding. At small power level when the motor winding is well damped, this method is very effective. **Fig. 3.16** shows the simulation result for CVB. Compare to **Fig. 3.14**, **Fig. 3.16** shows very good voltage balancing ability.

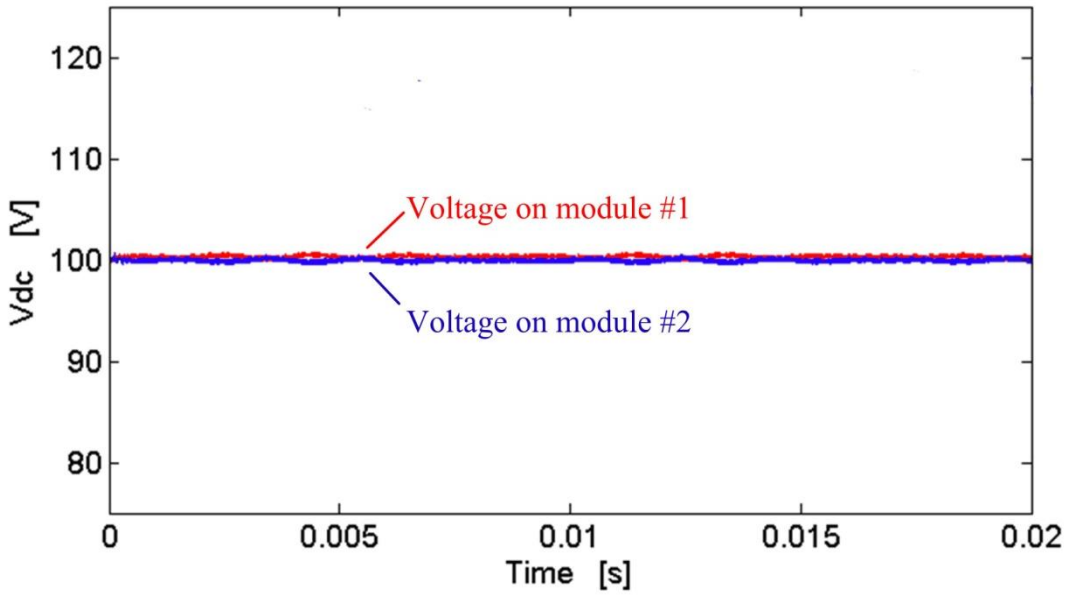


Fig. 3.16. Simulation result for machine segments having large mismatch with CVB control

In experiment, the motor does not have such a large mismatch, as shown previously in **Fig. 3.11**. There is about 4 V peak to peak value of the DC-link voltage difference due to module mismatch. With CVB, the peak to peak value of the voltage difference drops to 0.7 V, as shown in **Fig. 3.17**. It is hard to see any mismatch in the experiment result because the voltage ripple is dominated by switching ripple instead of mismatch.

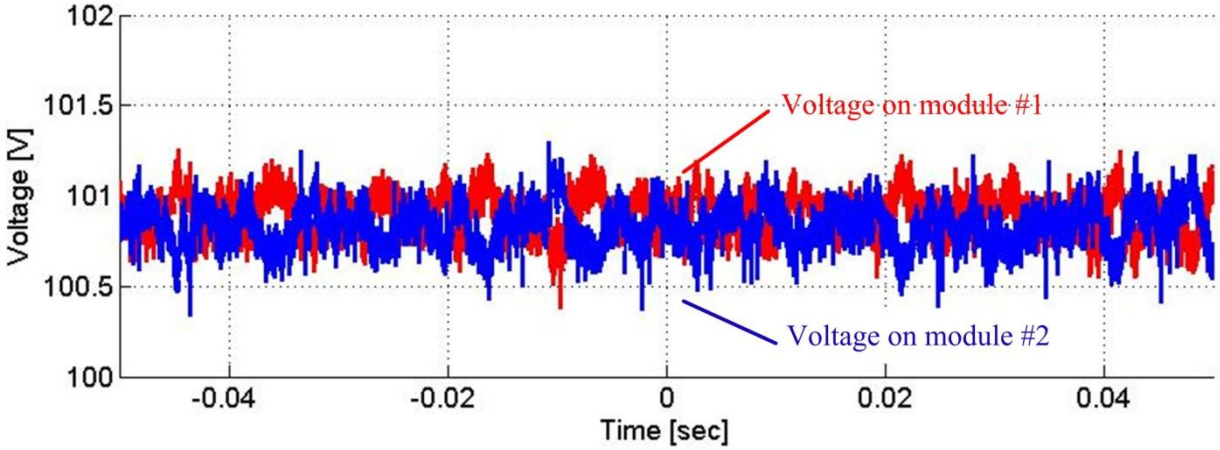


Fig. 3.17. Experiment result of zoomed in voltage ripples with CVB

3.2.4 Distributed Voltage Balancing Control

The CVB is effective in most of the cases, but it still has some limits. For example, when the motor has a large power and the winding resistance is very small, it is difficult to create the equivalent resistance by CVB. The CVB method also requires a central controller to send out the common duty ratios. However, a central controller is not always available. In some application, it requires the converter modules to have their own controllers on board. Each converter module will have its own current control algorithm [63] and different modules will operate

independently. [104][105] investigate the control for DC-DC converters with input-series modules.

To realize a robust voltage balancer in the proposed converter, an active resistor can be created directly by the control algorithm via adjusting the current of each module. All converter modules share the same current command through a relatively low frequency communication port. Any voltage error on a module will generate an adjustment on the current command such that the corresponding motor segment will output a different current and power. The current command adjustment will be equivalent to an active damping resistor but there is no power loss.

The difference between DVB and CVB balancing is that CVB adjusts the voltage and relies on the motor winding to act as the damping resistor. The value of the equivalent damping resistor depends on the motor winding, winding current and modulation index. By contrast, DVB adjusts the current command and relies on the current controller to execute the current command. The equivalent resistor value purely depends on the control program and can be adjusted freely.

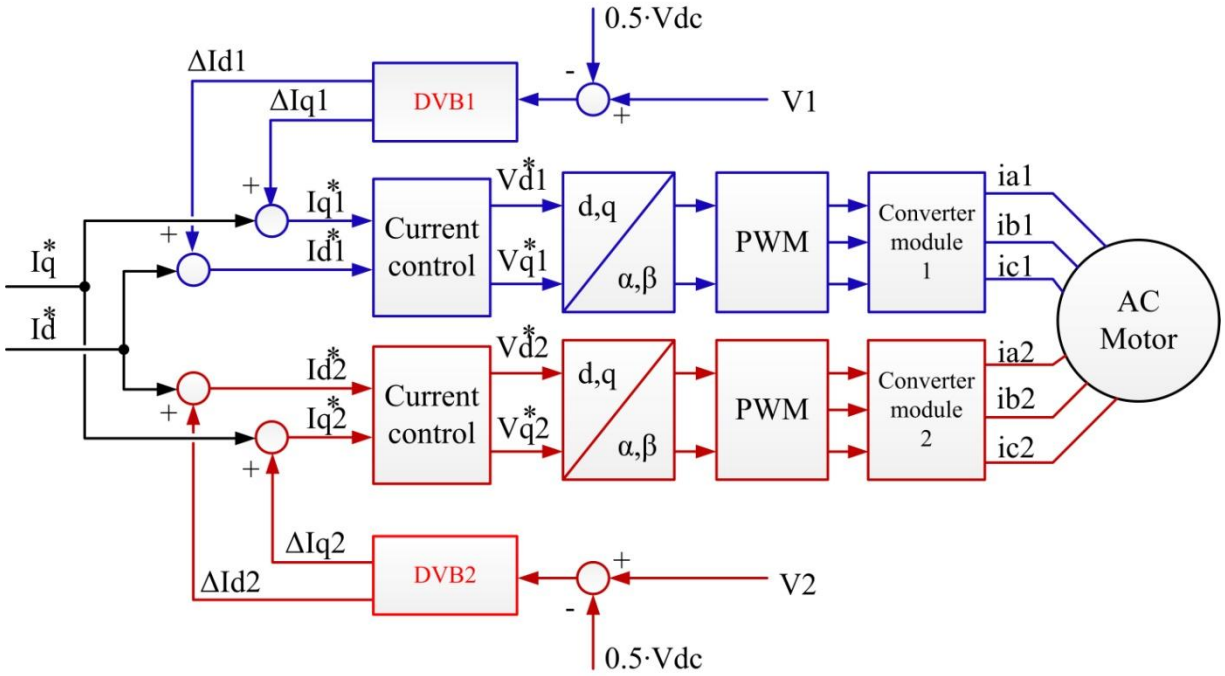


Fig. 3.18. Control diagram for active voltage balancing

However, in DVB, the independent close-loop current control is equivalent to a negative resistance. Consequently, the voltages of series-connect modules are inherently unstable. The voltage balancing control is required in DVB. By contrast, without voltage control, the CVB method is exactly the same as the passive voltage balancing method and it is stable. In DVB, to properly control the module voltages, the control program must follow a rule that the equivalent balancing resistance has a lower value than the equivalent resistance of the current control. Therefore the whole converter module plus control will be equivalent to a positive resistance.

In simulation, there are two converter modules and the total DC-link voltage is 200 V. The d-axis and q-axis current command is 0 and 3 A respectively. The electric speed of the motor is set to 50Hz.

Fig. 3.19 shows the voltage simulation results without DVB but with close-loop current control. The voltages of both modules are not stable. The voltage on module #1 jumps to 160 V and the voltage on module #2 drops to 40 V. The voltages are finally constant because the current loop PI controller becomes saturated. Without the saturation limit of current controller, the module voltages will have a larger difference.

Fig. 3.20 and **Fig. 3.21** show the current waveforms of both modules. The converter module #1 has a higher voltage and is able to execute the voltage command from current controller. As a result, the current controller can still work properly and regulate the current to the command value. By contrast, the module #2 can no longer regulate the current properly because its DC-link voltage is too low. Only when the module loses its current regulation, the module voltages will maintain constant. At this moment, the converter is in over-modulation region and will not execute the voltage command from current control. Hence the negative equivalent resistance created by close-loop current control no longer exists. The module voltages become stable, but not at the desired value.

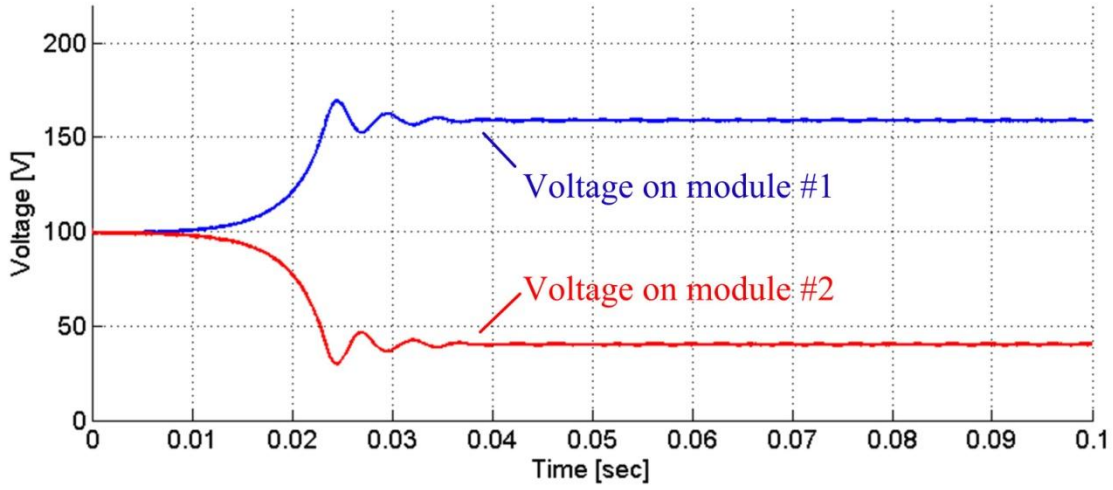
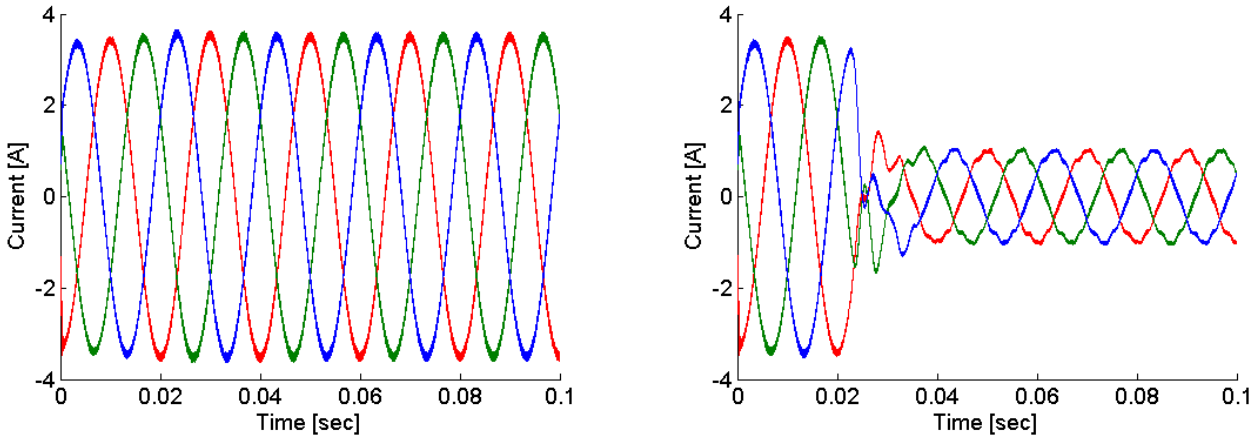
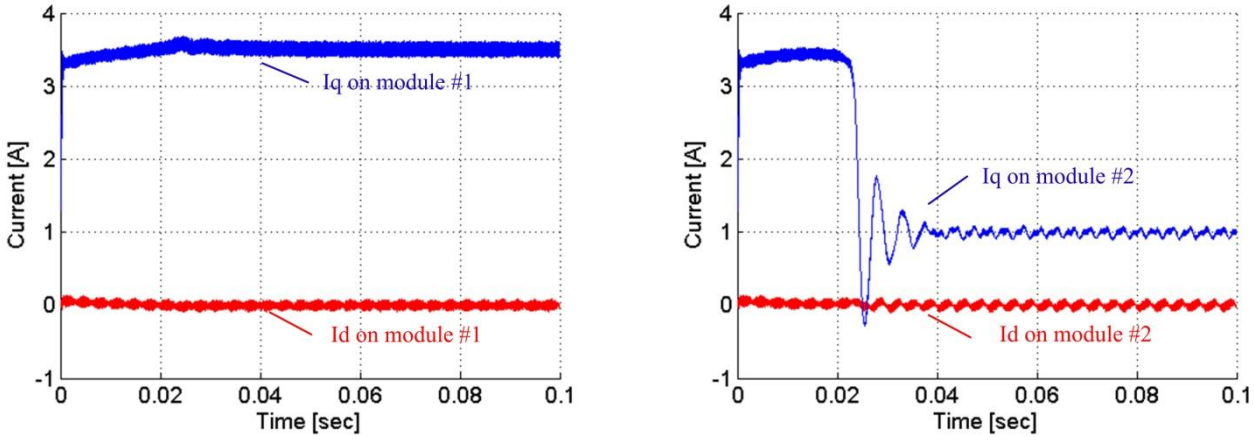


Fig. 3.19. Simulation result of Fig. 3.18 without DVB: the voltage on both modules



(a) (b)

Fig. 3.20. Simulation result of Fig. 3.18 without DVB: the 3-phase currents on both modules



(a) (b)

Fig. 3.21. Simulation result of Fig. 3.18 without DVB: the dq currents on both modules

The simulation is run again with DVB, as shown in **Fig. 3.22**, **Fig. 3.23** and **Fig. 3.24**. In order to test the performance of DVB, the module voltages are intentionally pre-charged to 120 V and 80 V on module #1 and #2 respectively.

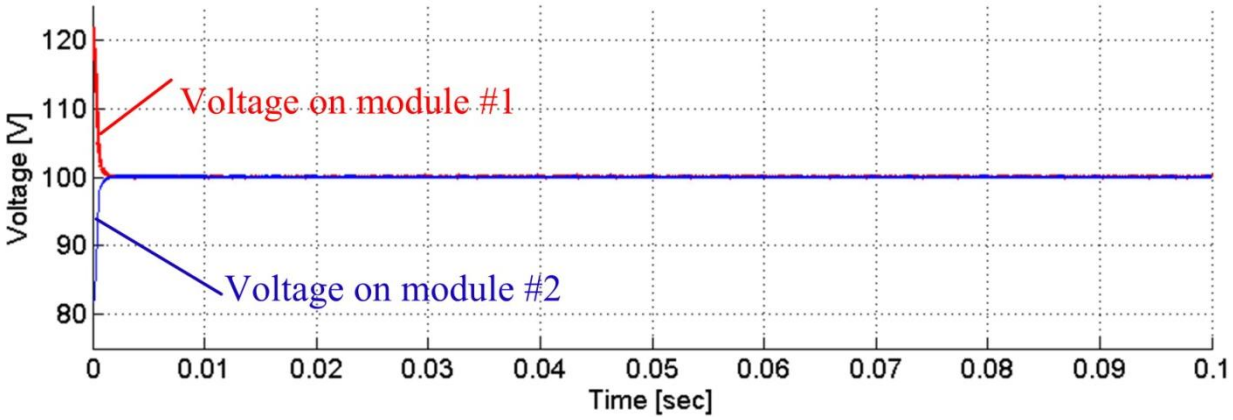
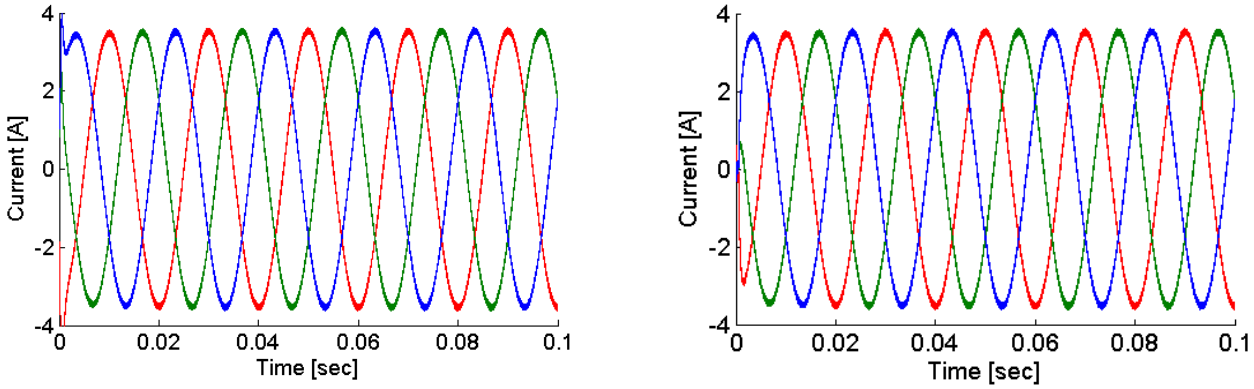
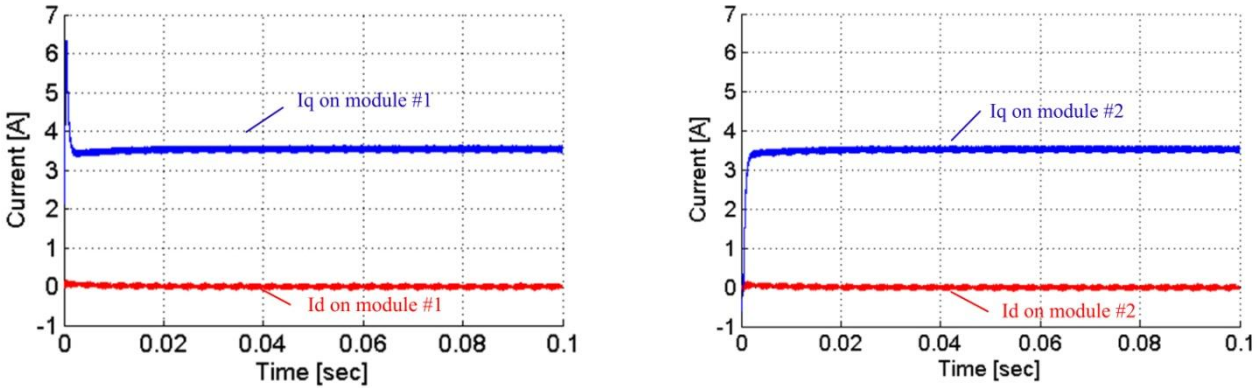


Fig. 3.22. Simulation result of Fig. 3.18 with DVB: the voltage on both modules



(a) (b)

Fig. 3.23. Simulation result of Fig. 3.18 with DVB: the 3-phase currents on both modules



(a) (b)

Fig. 3.24. Simulation result of Fig. 3.18 with DVB: the dq currents on both modules

At the beginning, the dq-axis currents are not the desired values because the module voltages are not balanced. Since module #1 has a higher voltage, its dq-axis currents are larger so that the module #1 will output more power. Module #2 has a lower voltage and as a result, its currents are lower. With DVB, the module voltages are regulated to the desired values quickly. As long as the voltages are balanced, the voltage balancer will no longer affect the module currents and consequently, the currents will be exactly the same as the current commands.

In the simulation, the voltages are balanced on both modules and the currents are well regulated. These simulation results have proved two things: 1) DVB is working as expected, and 2) DVB is compatible with the conventional current control.

3.2.5 Summary of Converter Control

There are three methods to balance the module voltages for the proposed converter: they are 1) passive method, 2) CVB and 3) DVB.

In passive method, the converter modules are driven by identical duty ratios. Hence the module with higher DC-link voltage will output higher voltage to the motor segment. If all motor segments are identical, the converter module with higher voltage will lead to a higher current in the corresponding motor segment. The higher current will discharge the DC-link and hence the voltage will drop. This mechanism maintains the converter modules to have balanced voltages. Some hardware circuit, such as passive parallel resistors, choppers and balancing semiconductor switches, can help the converter to balance the voltages and safely shut down the converter during fault conditions.

If a more robust converter is needed, CVB can be applied so that the converter can keep operating even when the motor segments are very different from each other. CVB will directly adjust the duty ratio of every module based on the module DC-link voltage. The adjusted duty ratio will affect the output voltage of the module, and hence receive a current response from the motor windings. The current response is equivalent to a parallel resistor that can balance the module voltage. Different from the passive method, CVB can have a very small equivalent resistor that has strong balancing capability without induce real power loss. CVB requires the motor windings to have enough damping and it needs a centralized controller to control all converter modules.

In situations where the motor has very large power so the motor windings cannot provide enough damping, or the converter modules have their own distributed controllers instead of a

centralized controller, DVB is preferred. The DVB method uses a voltage balancer to adjust the current command of each converter module. This is a pure software solution and the performance can be programmed without considering the damping of the motor windings.

Other advanced control techniques are also possible. For example, deadbeat direct torque and flux control (DB-DTFC)[106][107] is a very promising candidate because it provides very fast dynamic response such that the voltage balancing on different modules are fast enough to reject voltage variations.

3.3 Modeling of Machine Segments in the Same Pole Pair

Section 2.2 proposes the winding configuration #2, where the machine windings in the same pole pair are split into several segments. In this configuration, machine segments have strong magnetic coupling. Different from the case of non-overlapping pole-pairs discussed in section 3.1, the machine segments in the same pole-pair are overlapping and cannot be decoupled from each other. Machine segments are no longer equivalent to individual small motors for this configuration. As shown in **Fig. 3.25**, two coils A1 and A2 are closely located and have a high coupling factor (usually >90%).

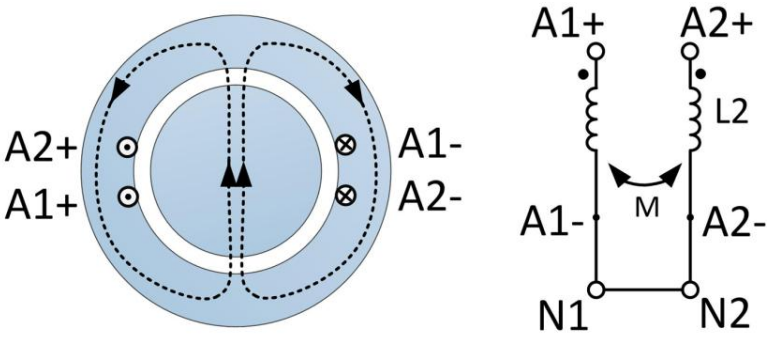


Fig. 3.25. Machine coils in the same pole pair

Because of the strong coupling, any voltage applied to A1 will be experienced by A2 and vice versa. The coils A1 and A2 are acting as the primary side and the secondary side of a single phase transformer with nearly 1:1 turns-ratio. Both A1 and A2 coils simultaneously excite the motor phase A.

In the previous section, the machine model is a three-phase decoupled model, where A1, B1 and C1 are considered as a three-phase unity. However it will be no longer valid in this section, because the strong coupling between A1 and A2 will dominate the winding behavior. As a consequence, the single-phase coupling between A1 and A2 has a higher priority than the three-phase coupling between A1, B1 and C1. The discussion in this section will focus on single-phase coupling between A1 and A2.

The following paragraphs will give detail discussion on two different possible winding patterns. The first one is that the machine segments are located in the same pole pair but different slots, as presented in **Fig. 2.7** and **Fig. 2.8** (a). The second pattern is when the machine segments are located in exactly the same slots, as shown in **Fig. 2.8** (b). These two patterns are quite different and exhibit different behavior.

3.3.1 Machine Segments in Different Slots

For reader's convenience, **Fig. 2.7** is repeated here to illustrate the case of machine segments in different slots. The coupling factor between these two segments can be directly calculated by (3.9). Since the displace angle α is usually small, the coupling factor is usually greater than 90%, indicating a strong coupling between these segments. However, the angle α is not small enough to neglect. The non-unity coupling factor will create a leakage inductance term in the equivalent transformer [108].

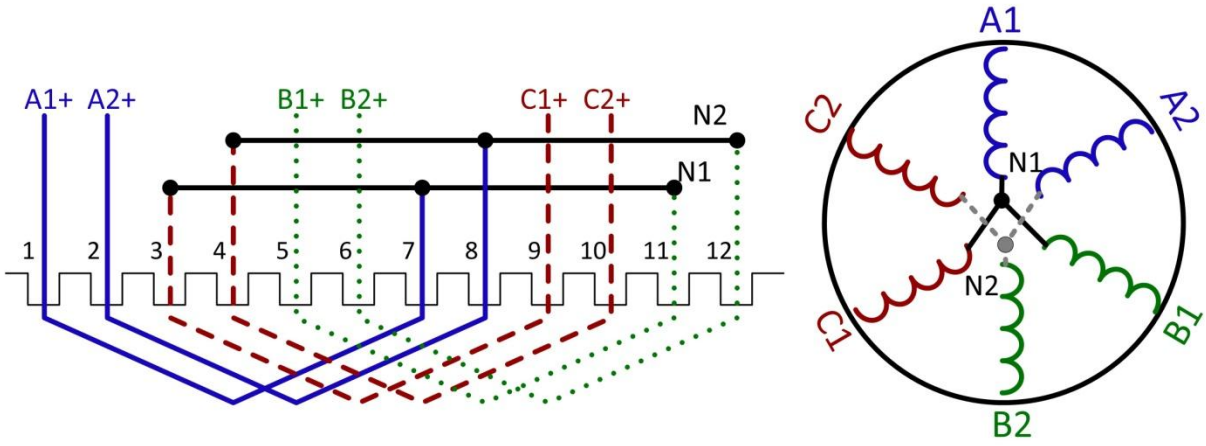


Fig. 2.7. Simplified model for winding configuration #2

Fig. 3.26 illustrates the single-phase equivalent transformer circuit of the machine segments, where L_{sA1} and L_{sA2} are the leakage inductance of coil 1 and coil 2 respectively, R_{A1} and R_{A2} are the coil resistance.

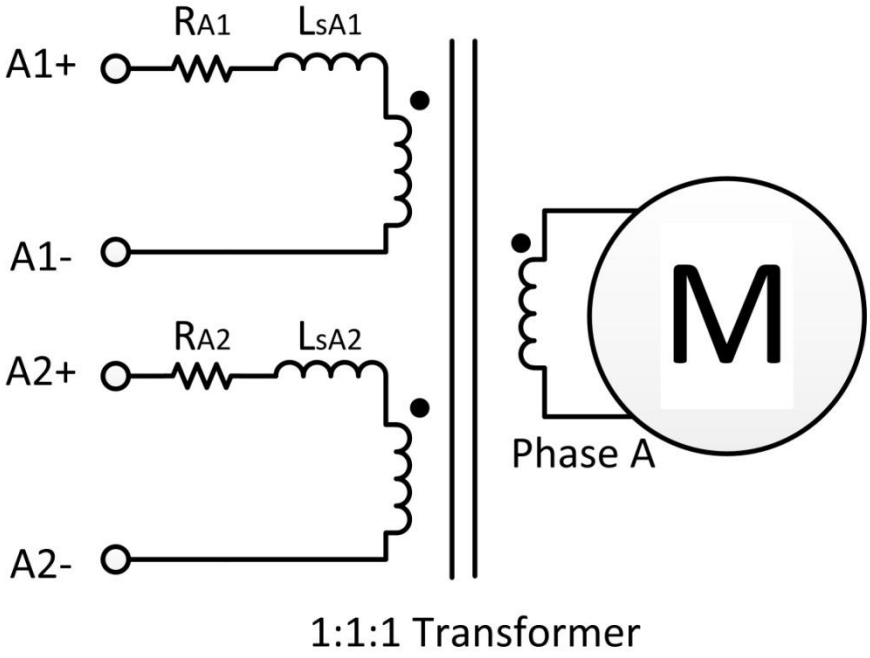


Fig. 3.26. Single-phase equivalent circuit of machine segments in different slots

3.3.2 Machine Segments in Same Slot

When the machine coils A1 and A2 are located in the same slot, a simple 1:1:1 transformer model cannot correctly represent them. This is because the coils are so close to each other such that the parasitic capacitance plays a significant role. **Fig. 3.27** illustrates examples for winding coils in the same slot. Viewing from the terminals of A1 and A2, the impedance is typically capacitive, ranging from pF to nF.

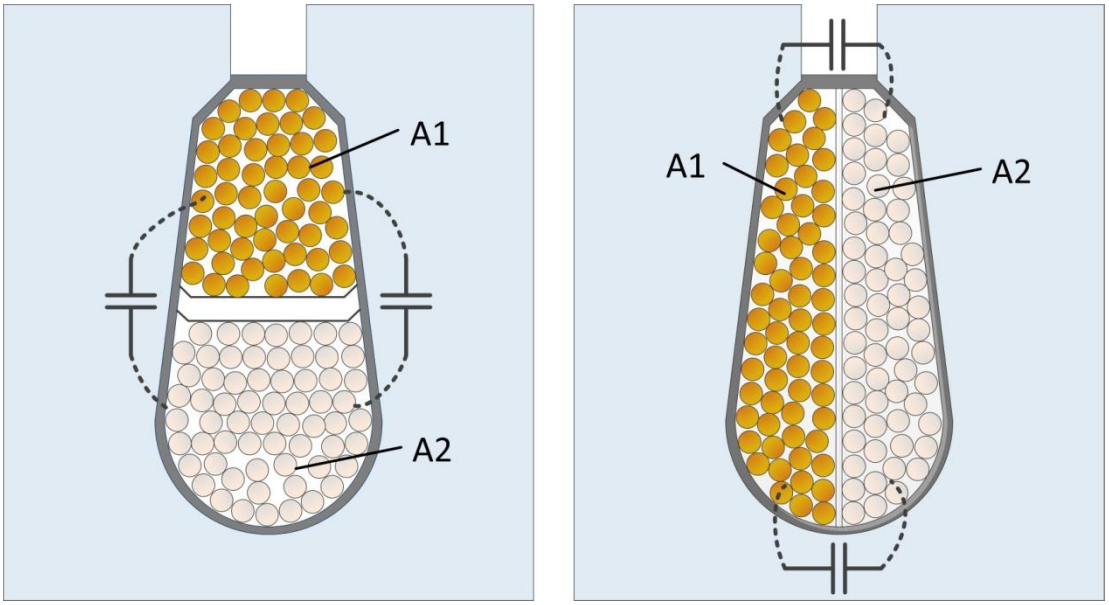


Fig. 3.27. Parasitic capacitance in one machine slot

Moreover, the displace angle α is zero in this case. As a consequence, the coupling factor between the coils is almost 100% (>99%). Hence the leakage inductance in the equivalent transformer is usually as low as microHenry.

The parasitic capacitance, leakage inductance and coil resistance are distributed along the coils. This is quite similar to a transmission line. The coils can be modeled by "nominal π" circuit, in which the distributed circuit parameters can be represented by concentrated parameters. **Fig. 3.28** shows the equivalent circuit for single-phase machine model, where C_{in} and C_{out} represents the parasitic capacitance between the coils.

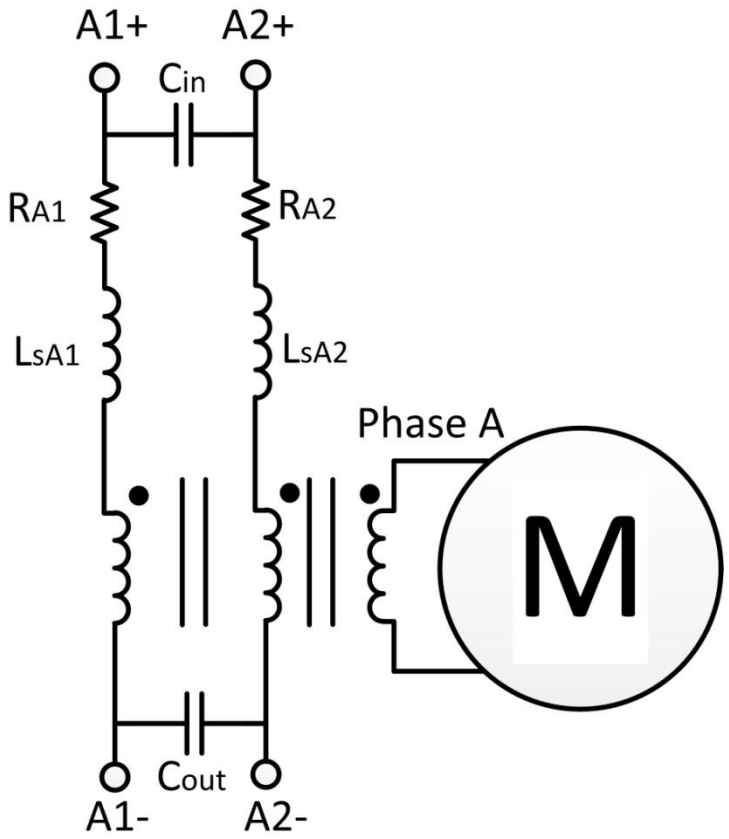


Fig. 3.28. Single-phase equivalent circuit of machine segments in the same slot

3.4 Converter Control of Machine Segments in the Same Pole Pair

Due to the existence of magnetic coupling, the voltage balance of input-series converter modules can be quite different from section 3.2. In the following paragraphs, control methods will be discussed in details.

3.4.1 Voltage Balancing for Machine Segments in Different Slots

When machine segments are located in different slot, they typically have 90% - 95% coupling factor. For simplicity of this study, assume the coupling factor is 90%. That's to say, the leakage inductance is about 10% of the machine magnetic inductance.

At the converter switching frequency (~10 kHz for Si devices and >100 kHz for GaN devices), this leakage inductance still has very large impedance to provide enough filtering. Hence small ripple approximation can be applied for the equivalent circuit. The output voltage of a single phase converter leg is equal to its duty ratio multiplying its DC bus voltage. The converter module, therefore, is equivalent to an ideal DC transformer. **Fig. 3.29** illustrates how the equivalent circuit is evolving when viewing from A1+ side. In the circuit, the converter module capacitor is C_{dc} and it is reflected to the machine coil A1+ side. Notice that the impedance of the capacitance is changing from 1/Cs to D^2/Cs, which is equivalent to the capacitance changing from C to C/D^2.

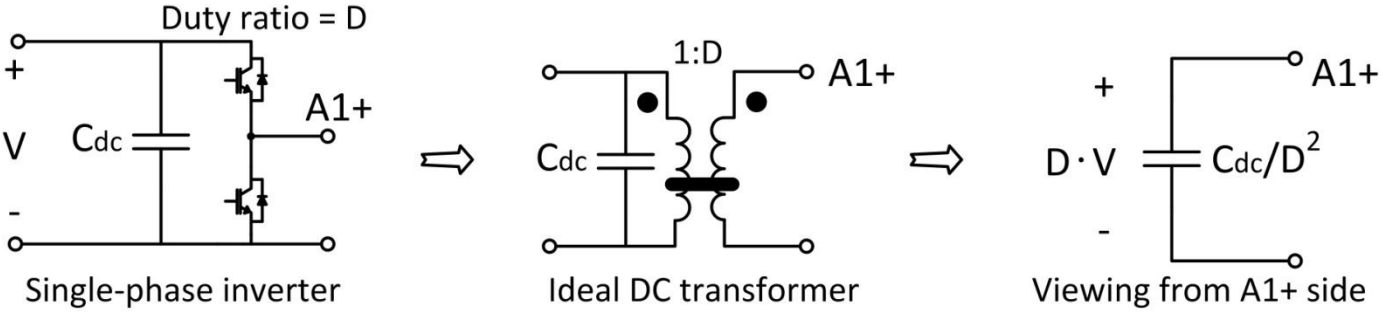


Fig. 3.29. Equivalent circuit of the converter module viewing from machine coil side

The model of converter & machine system can be derived by combining **Fig. 3.26** and **Fig. 3.29**. For simplicity, it is also desirable to exclude the effect of the quiescent operating point

related to the machine. **Fig. 3.30** shows the equivalent circuit of two converter modules supplying A1 and A2 respectively.

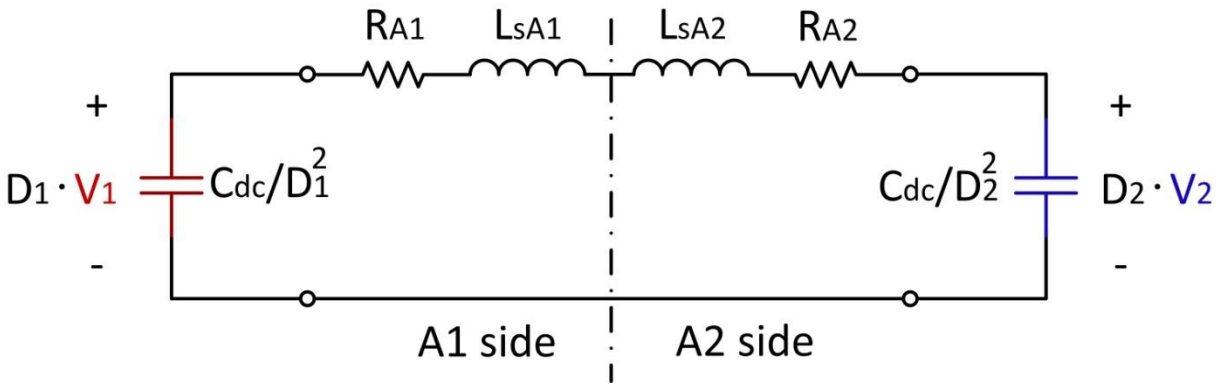


Fig. 3.30. Single-phase equivalent circuit of machine segments in different slots

In reality, the coils A1 and A2 will have different voltage potential and there is a DC bias between the coils. However, the DC bias is isolated by the coil transformers, so it has no effect on the circuit. For this reason, the DC bias is neglected in **Fig. 3.30**, so A1 and A2 coils have same potential.

The circuit has inherent voltage balancing capability when common-duty-ratio method is applied, i.e., the duty ratio of two converter modules D1 and D2 are identical. Any voltage mismatch between two modules will lead to a current flowing through the windings to neutralize the voltage mismatch.

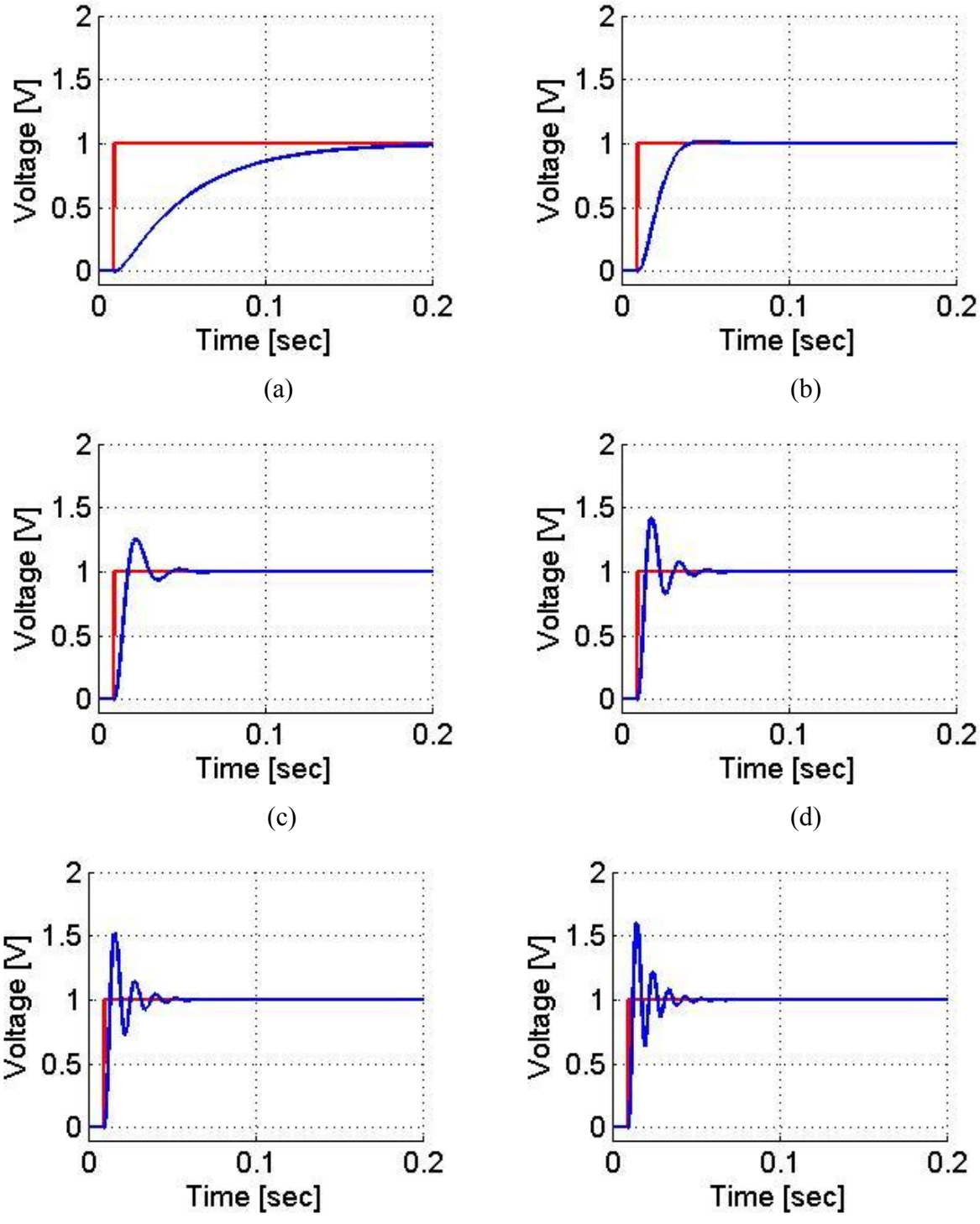


Fig. 3.31. Simulation results: voltage disturbance of V1 (step change, red) and voltage response of V2 (blue)

(a) D=0.1, (b) D=0.2, (c) D=0.4, (d) D=0.6, (e) D=0.8 and (f) D=1.0

Machine parameter	$L_{sA1}+L_{sA2}$	$R_{A1}+R_{A2}$	C_{dc}
Value	37.8 [mH]	8.4 [Ω]	60 [μF]

Table 3.4. Simulation parameters based on Danfoss FCM315 Machine with 90% coupling factor

Fig. 3.31 illustrates the simulation results of the voltage balancing. As shown in the figure, giving a disturbance step change of V1 will result in a response of V2. The voltage V1 and V2 will eventually become equal. The converter is a non-linear model and as a consequence, the dynamic response of V2 also depends on the duty ratio D. As D gets larger, the resonant frequency of the circuit is higher, the settling time is shorter and the overshoot is higher.

Active voltage balancing methods, such as CVB and DVB, are also effective in this winding configuration.

3.4.2 Voltage Balancing for Machine Segments in Same Slot

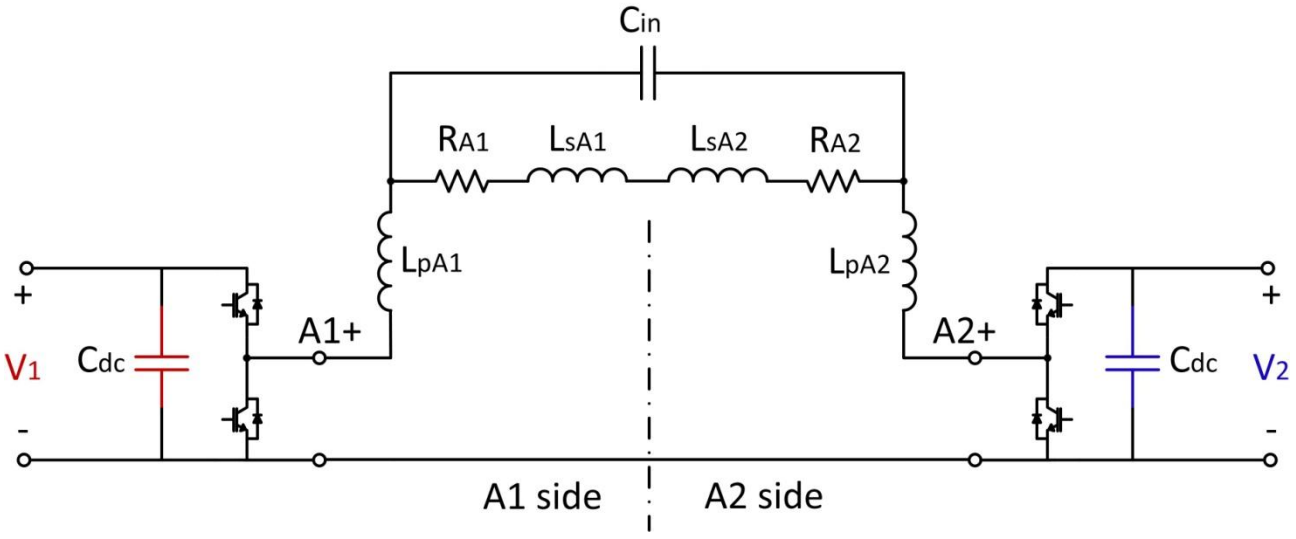


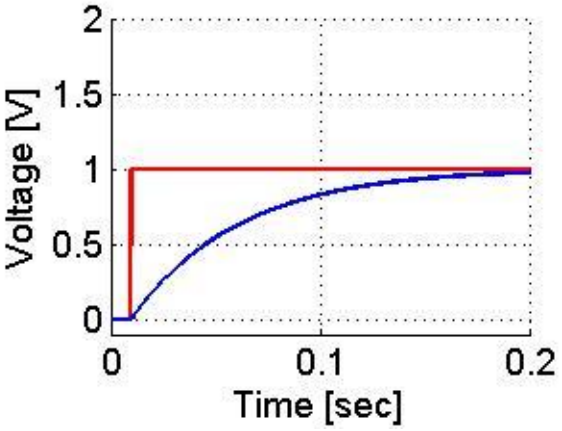
Fig. 3.32. Single phase equivalent circuit of machine segments in the same slot

Machine parameter	$L_{sA1}+L_{sA2}$	$R_{A1}+R_{A2}$	C_{in}	$L_{pA1}+L_{pA2}$
Value	378 [μH]	8.4 [Ω]	16 [nF]	100 [nH]

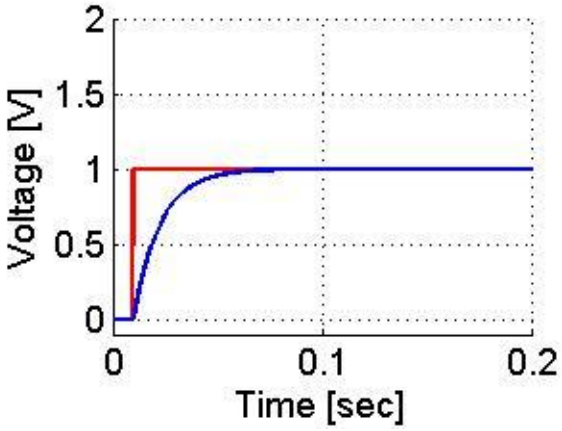
Table 3.5. Simulation parameters based on Danfoss FCM315 machine with 99.9% coupling factor

As discussed in previous section, machine segments in the same slot have parasitic capacitance between them. **Fig. 3.32** shows the single phase equivalent circuit when two segments are connected to two converter modules. L_{pA1} and L_{pA2} represent the parasitic inductance between the converter and the motor. This inductance can be attributed to the power cables and connectors.

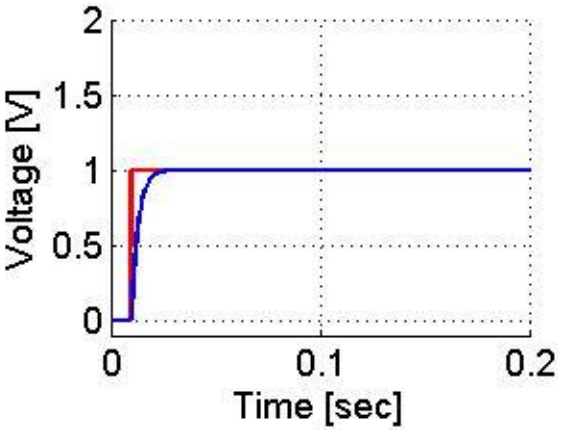
The circuit parameters are summarized in **Table 3.5**. The leakage inductance in this case is 378 μH, much smaller than 37.8 mH in previous section. As a result, the voltage disturbance response will have much stronger damping, as shown in **Fig. 3.33**.



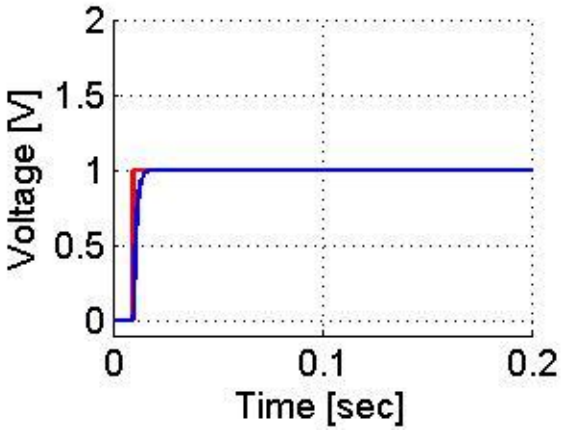
(a)



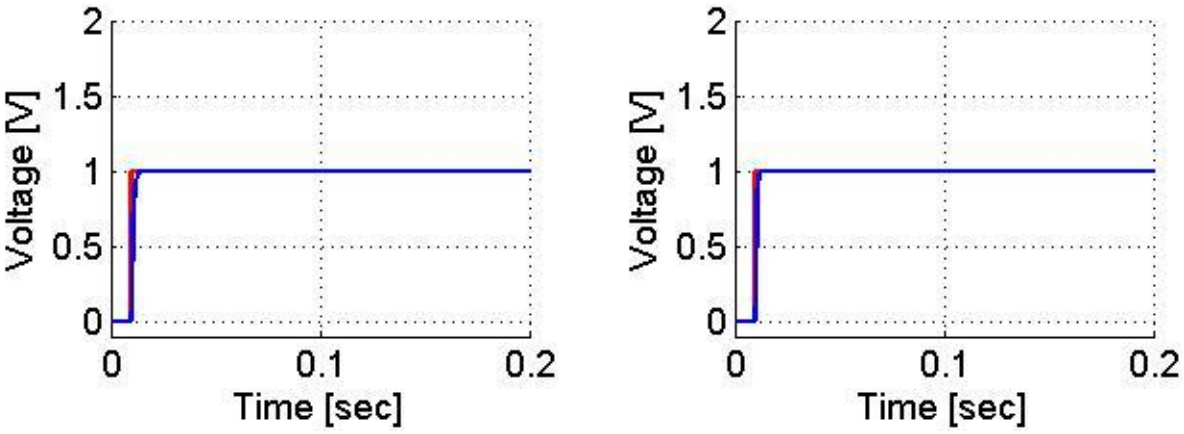
(b)



(c)



(d)



(e) (f)

Fig. 3.33. Simulation results: voltage disturbance of V1 (step change, red) and voltage response of V2 (blue)
(a) D=0.1, (b) D=0.2, (c) D=0.4, (d) D=0.6, (e) D=0.8 and (f) D=1.0

The equivalent circuit can be re-drawn into a LCL circuit, as shown in **Fig. 3.34**. The voltage mismatch between A1+ and A2+ is decided by the corresponding single-phase inverter.

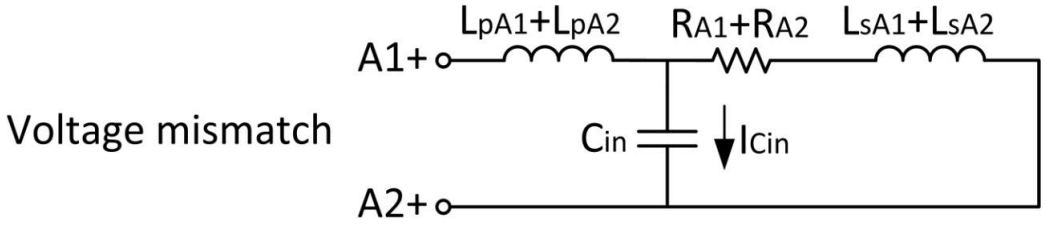
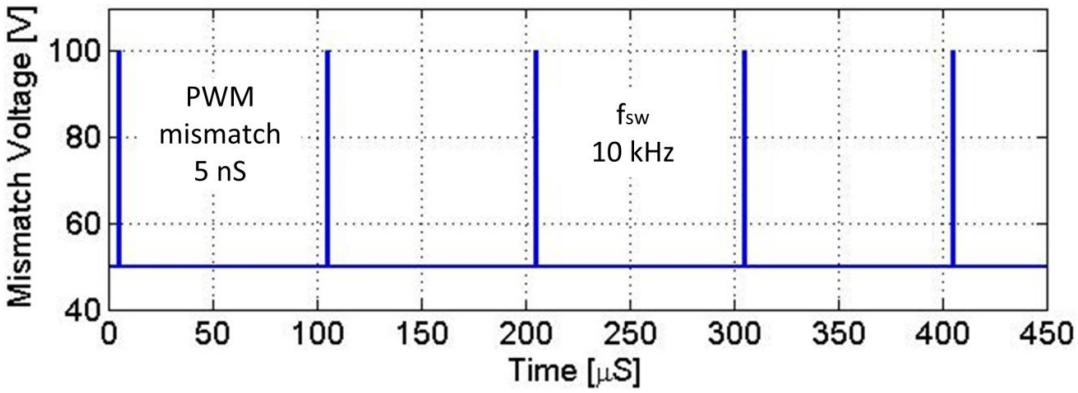


Fig. 3.34. Simplified equivalent circuit of machine segments in the same slot

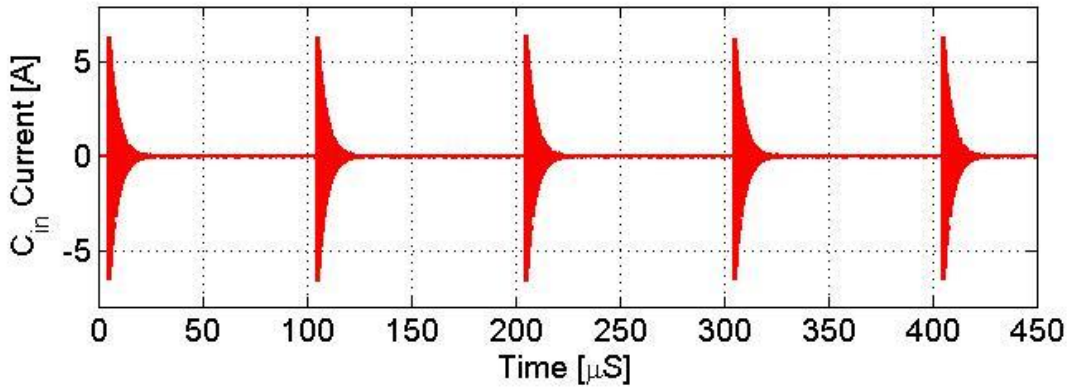
If there is no voltage mismatch between A1+ and A+2, the parasitic capacitance C_{in} will only hold a steady constant module voltage (the voltage between two series-connect modules).

However, when there is any voltage mismatch, since the numerical values of L_{pA1} and C_{in} are very small, it will cause a large current I_{cin} that flowing through the insulation layer of the machine windings and cause machine failure.

To avoid I_{cin}, A1+ and A2+ should have exactly identical PWM signals so they will have exactly identical PWM output voltage supplying A1+ and A2+. However, there always exists PWM mismatch due to the mismatches of MOSFETs and gate drivers. As shown in **Fig. 3.35**, the PWM mismatch can have a width of 5-10 ns and amplitude of the module voltage (50V in this case). There will be a huge charging current I_{cin}.



(a)



(b)

Fig. 3.35. Simulation results of mismatch voltage and response current

(a) mismatch voltage, and (b) response current

The advantage of this charging current is that, it strongly forces the modules to have identical voltages. Even a small voltage mismatch can lead to a huge current balancing the module voltage.

The disadvantage is that, the current response is too sensitive to the voltage mismatch. The PWM mismatch is impossible to avoid, and it can cause undesirable resonant current that breaks down the machine insulation.

Adding an extra LC filter to the circuit is a suggested method to deal with the undesirable I_{cin}. The size of LC filter can be very small because the PWM mismatch is only 5-10 ns. With the LC filter, the machine windings are protected because they will no longer experience the fast changing PWM mismatch.

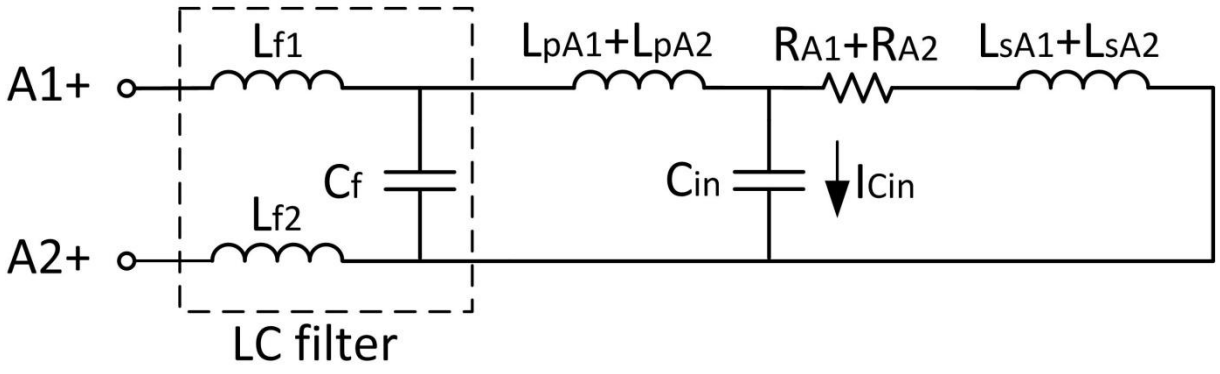
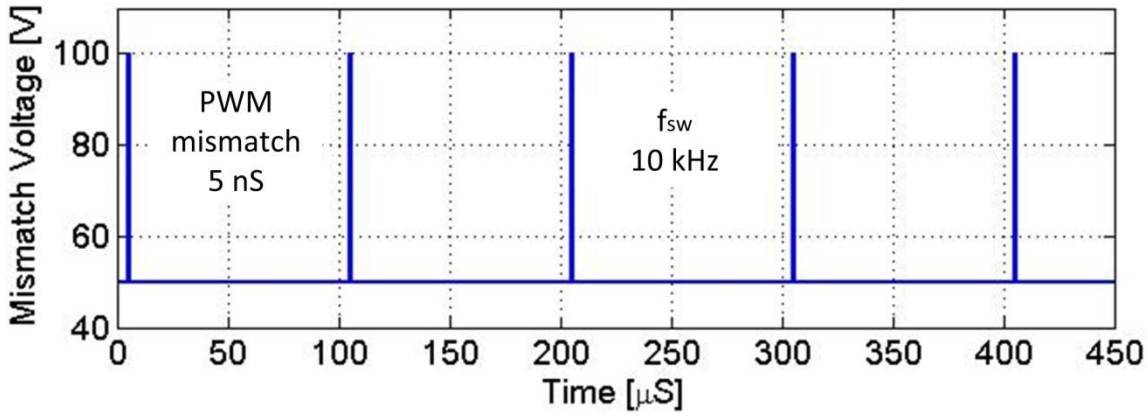


Fig. 3.36. Extra LC filter for machine segments in same slot

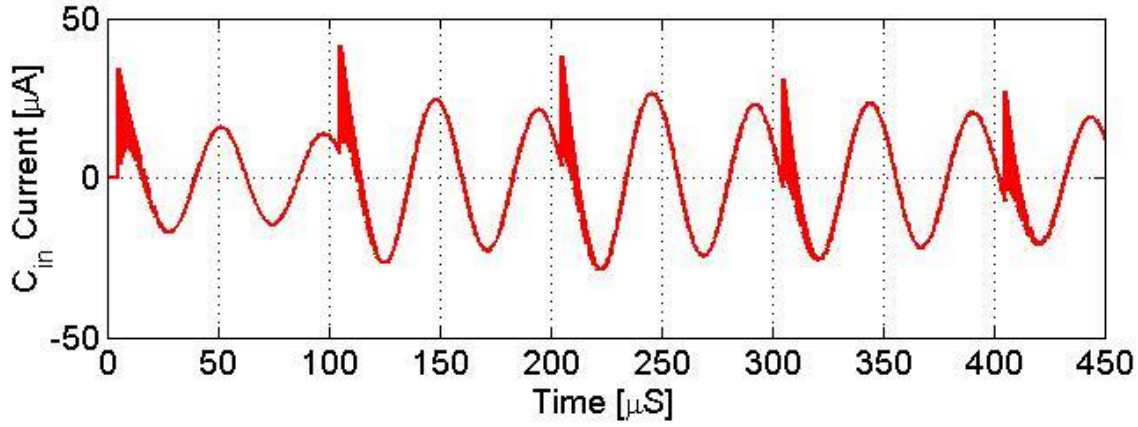
Filter parameter	$L_{f1}+L_{f2}$	C_f
Value	66 [μ H]	1 [μ F]

Table 3.6. Example of LC filter parameters

Fig. 3.37 shows the simulation result with LC filter. The current flowing through the machine insulation is limited within 50 μA. This result shows that the LC filter is very effective in reducing the charging current and protect the machine insulation from damage by PWM mismatch.



(a)



(b)

Fig. 3.37. Simulation results of mismatch voltage and response current with LC filter (a) mismatch voltage, and (b) response current

3.4.3 Summary of Converter Control for Segments in Same Pole-Pair

The magnetic coupling between machine segments in same pole pair helps to balance the voltages of converter modules. The machine segments are equivalent to a transformer and force the module voltages to be identical. Compare to the machine segments in different pole pair (no coupling), the machine segments in same pole pair has much stronger passive balancing performance.

The machine segments can locate in same pole pair but different slots. They tend to have about 90%-95% coupling factor. This will result in leakage inductances that act as filter inductors. The leakage inductances are large enough to filter the ripples at PWM switching frequency. All active control method introduced in section 3.2 can be applied here, including passive voltage balancing, CVB and DVB.

The machine segments can also locate in exact same slot. In this case they will have a nearly perfect coupling factor (>99%) and a parasitic capacitance between the segments. Because of the high coupling factor, the machine segments will experience the strongest passive voltage balancing. Due to the existence of parasitic capacitance, the machine-drive system will be very sensitive to PWM signal mismatch. There will be an undesirable current flowing through the machine winding insulation. To filter out the PWM mismatch, a small LC filter is recommended to be installed.

Active control method, such as CVB and DVB can be applied. But the control method will generate larger PWM mismatch. As a result, CVB and DVB can be applied only when the LC filter is large enough to filter the PWM mismatch. Generally speaking, CVB and DVB are not even needed in this case because the inherent passive balancing is strong enough.

Chapter 4

Capacitor Evaluations

DC-link capacitors occupy a large portion of converter volume. It is necessary to evaluate the size of different types of capacitors in order to make the best decision. This chapter presents rules to select capacitors for a machine drive, followed by side-by-side comparison between different types of capacitors.

4.1 Capacitor Selection Rules

This section will cover important requirements when selecting capacitors, such as capacitor RMS current and voltage ripples. A simulation model will be used to simulate the performance of one converter module and verify the requirements of capacitor RMS current and voltage ripples.

4.1.1 Introduction to the Simulation Model

In the simulation, a converter module with three-phase, two-level output will be analyzed, as shown in Fig. 4.1. It is actually identical to a conventional three-phase motor drive. Different switching frequencies are used so the RMS current and voltage ripples can be compared. A close-loop PI current controller is used to regulate the motor dq-axis currents so the comparison is fair.

In a converter module, the capacitor average voltage must be identical to the input voltage source V_{dc}. The input current ripple Δi_{dc} is proportional to the voltage ripple amplitude Δv_{dc} and inversely proportional to the filter inductor value L_p and the switching frequency.

$$\Delta i_{dc} \propto \frac{1}{L_p \bullet f_{sw}} \Delta v_{dc} \tag{4.1}$$

The filter inductor L_p in this simulation is large enough such that the input current ripple Δi_{dc} from the voltage source is negligible compared to the current ripples into the capacitor. Hence the input current can be treated as a constant value and the capacitor current, i_c, is totally decided by the motor line currents and the switching pattern. As a result, the switching ripple from the converter is fully handled by the DC-link capacitor. To buffering switching current ripple is exactly the function of a DC-link capacitor.

In the simulation, the switching frequency is a changing parameter. The line currents will be regulated to the command values. The line currents, as well as the DC-link capacitor current i_c, and the DC-link capacitor voltage ripple Δv_{dc} will be recorded for further analysis.

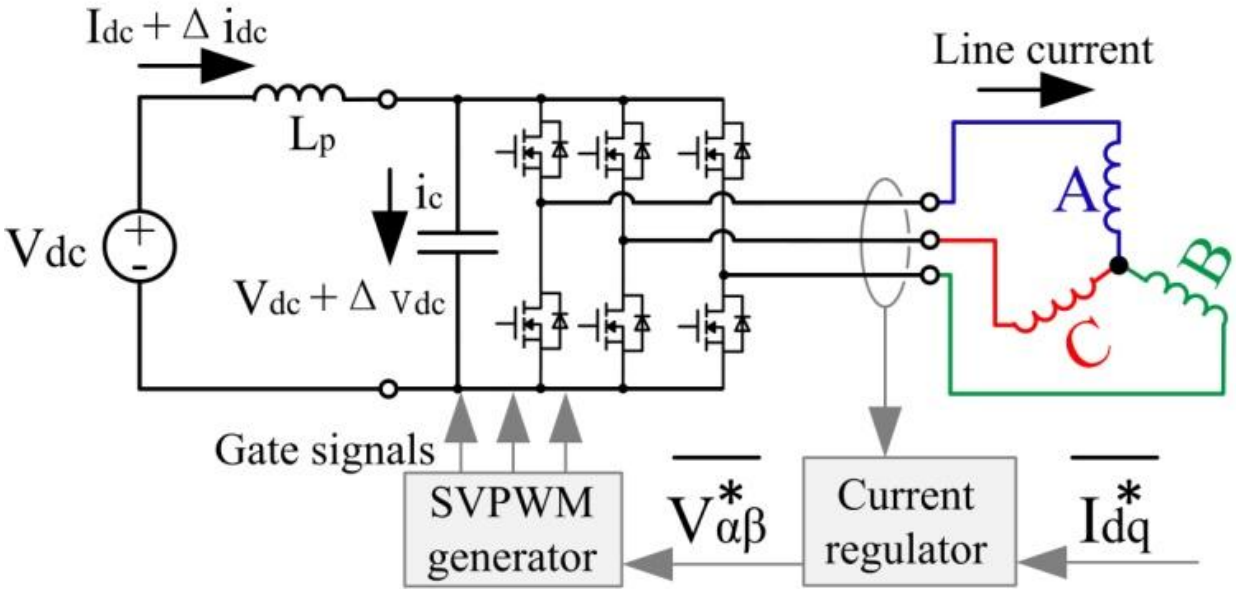


Fig. 4.1. Simulation model for one converter module

4.1.2 Capacitor Current

The RMS value of capacitor current is an important factor that affects the lifespan of the capacitor. The RMS current will induce resistance loss inside the capacitor and generate extra heat. The capacitor lifespan is very sensitive to the heat induced by RMS current. In this section, the RMS current of a converter module will be simulated.

Fig. 4.2 and **Fig. 4.3** show the simulation results for 20 kHz and 40 kHz switching frequency respectively. In both simulations, the motor line currents have the same fundamental components, because the currents are regulated by the close-loop current controller. The motor line currents are almost identical for these two cases, except that the currents have different ripple amplitudes. As shown in **Fig. 4.4**, the current ripple peak to peak value for 20 kHz switching frequency is about 0.35 A, and 0.18 A for the 40 kHz switching frequency, which is half of the 20 kHz case.

The capacitor current is actually decided by the absolute value of the line current. The line current ripples are very small compare to their fundamental component, and as a result, the line current ripples will not affect the absolute value of the line current or capacitor current. In **Fig. 4.2** (b) and **Fig. 4.3** (b), the capacitor currents have different frequencies but identical amplitude. The 40 kHz capacitor current looks like a squeezed version of 20 kHz case. The RMS value of the currents are 1.80 A and 1.78 A respectively, which are almost identical. These simulation results prove that, changing switching frequency will almost not affect the RMS value of the capacitor current. This result is consistent with the previous research presented in [109].

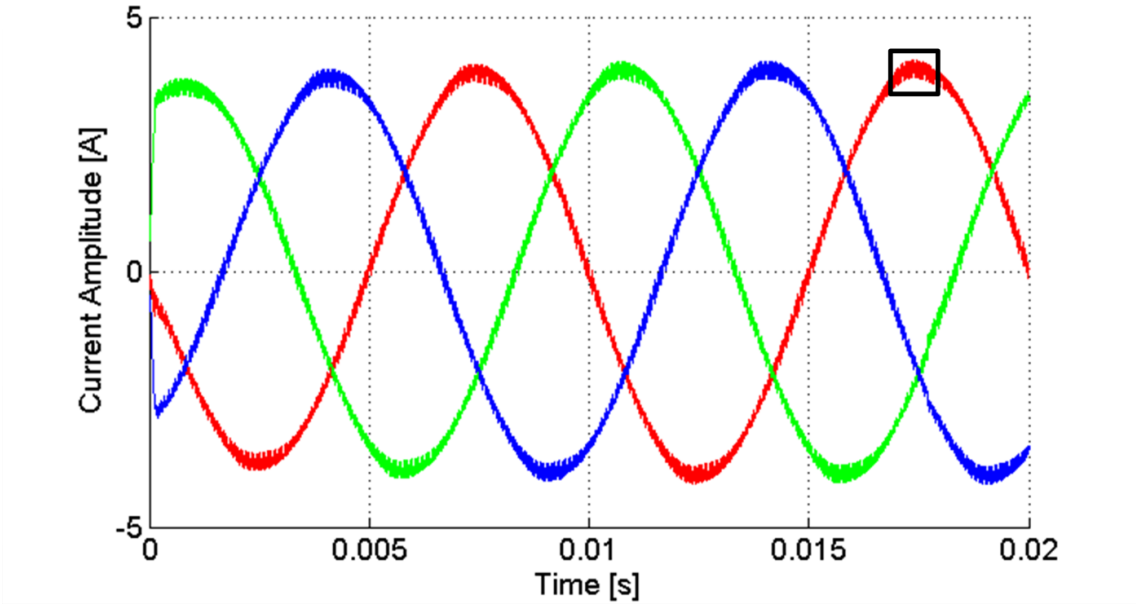
Following the design procedure in [110], the DC-link capacitor must satisfy the worst case current, and the capacitor RMS current value of a three-phase inverter can be calculated by (4.2) as derived in [110]:

$$\max(\ i_c) = I_{Line\_RMS}\sqrt{2m\left[\frac{\sqrt{3}}{4\pi}+\cos^2\Phi\left(\frac{\sqrt{3}}{\pi}-\frac{9}{16}m\right)\right]_{max}} \approx 0.65\ I_{Line\_RMS} \qquad (4.2)$$

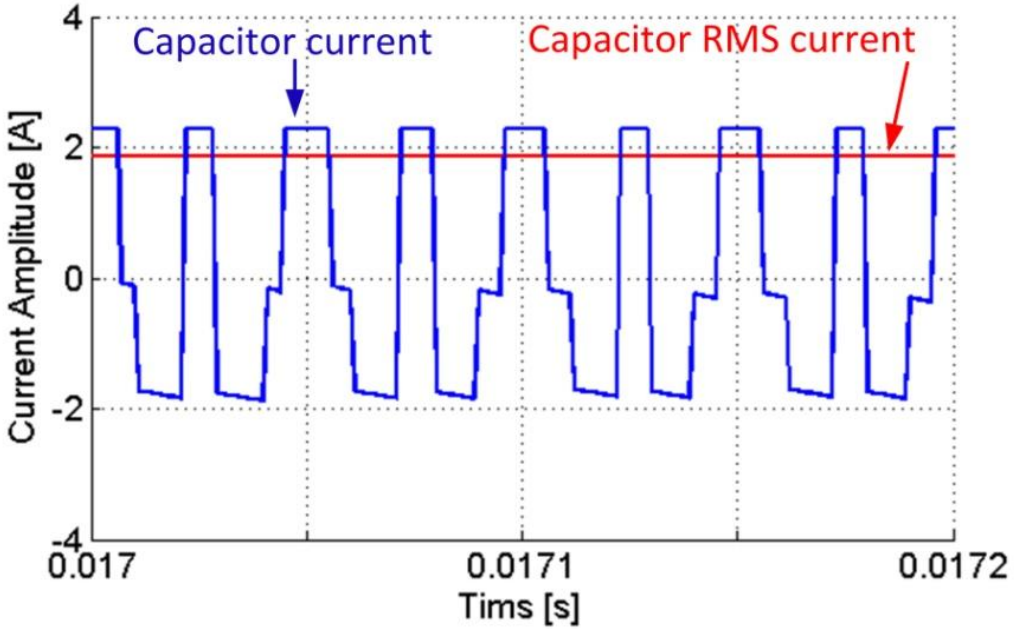
$$m = \frac{\widehat{V}_{out}}{0.5V_{dc}}\ , \qquad m \in \left[\ 0\ ,\ \frac{2}{\sqrt{3}}\right]$$

,where m is the modulation index defined as the peak amplitude of the output voltage divided by half the dc-link voltage, and cosΦ is the power factor. The maximum value is reached when m=0.6 and cosΦ = 1.0 [110].

Based on (4.2), the RMS current is 1.84 A for the converter module used in simulation. This is consistent with the simulation result.



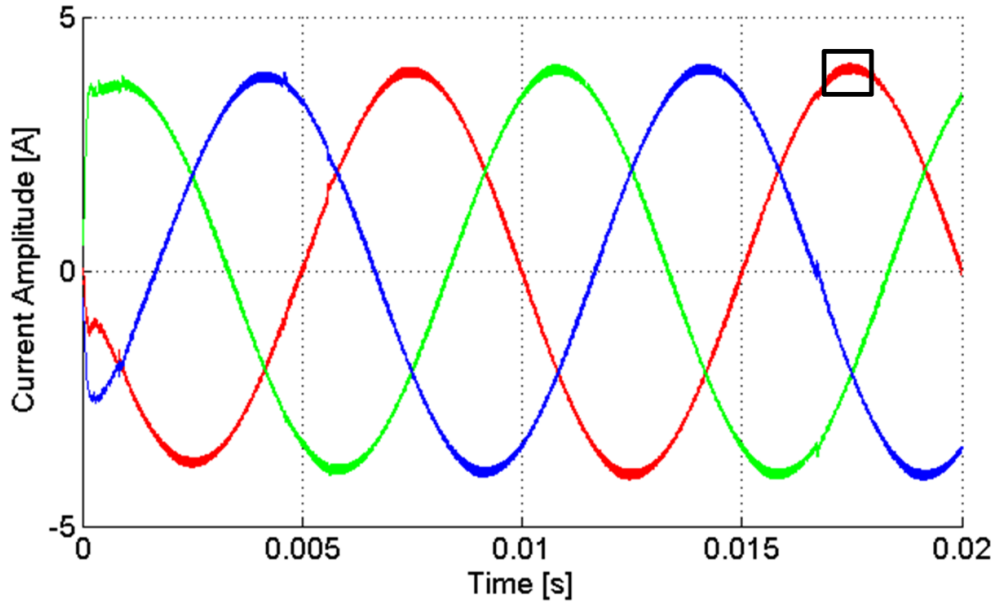
(a)



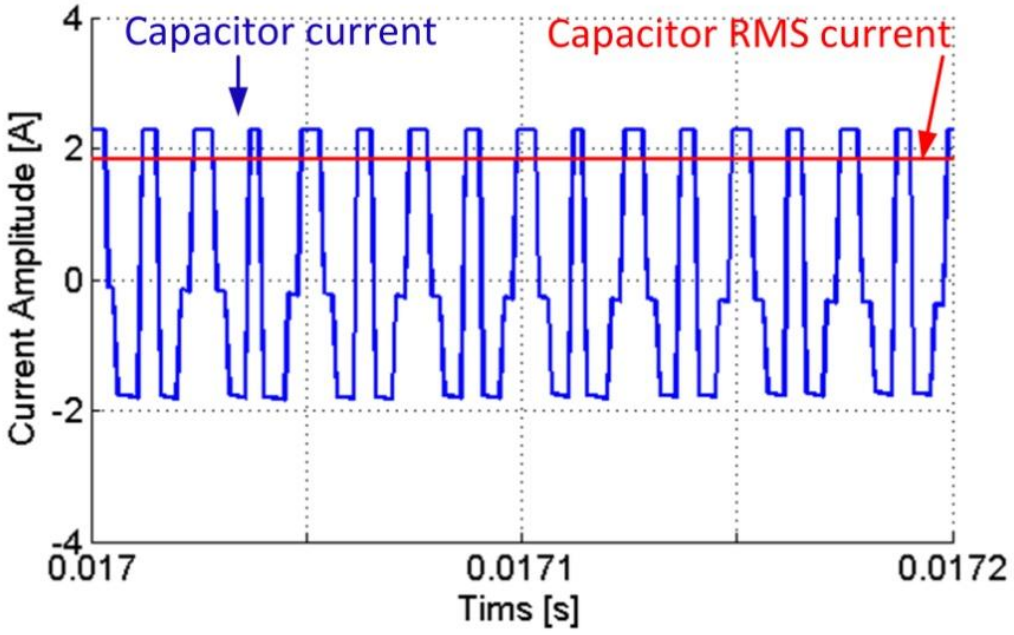
(b)

Fig. 4.2. Simulation results with 20 kHz switching frequency

(a) output line currents, (b) DC-link capacitor current with 1.80 A RMS value

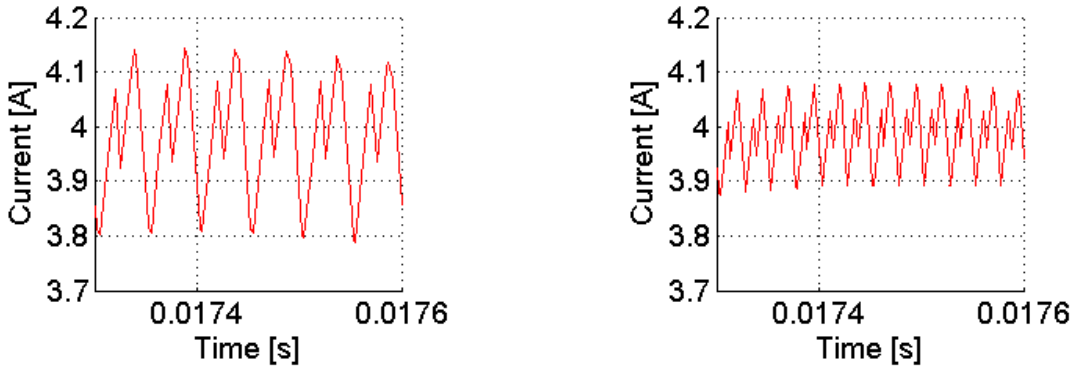


(a)



(b)

Fig. 4.3. Simulation results with 40 kHz switching frequency
(a) output line currents, (b) DC-link capacitor current with 1.78 A RMS value



(a) (b)

Fig. 4.4. Simulation results of line current ripples
(a) at 20 kHz switching frequency, (b) at 40 kHz switching frequency

In order to use the capacitor without overheating it, the capacitor rated RMS current must exceed the RMS current from the converter module. As long as the line current of the motor is known, the RMS current from the converter module can be decided by (4.2).

4.1.3 Capacitor Voltage Ripple

The DC-link capacitors have the important function to handle the current ripple of the converter and separate it from the input DC source. The capacitor voltage ripple, Δv_{dc}, is decided by the integration of capacitor current. The capacitance must be sufficient to keep Δv_{dc} small enough. Otherwise, the maximum DC-link voltage will be higher and the rating voltages of all semiconductor devices must be increased.

Moreover, a large ripple on the DC-link will lead to other issues such as EMI and control difficulty. As reported in [111], the typical amplitude of voltage ripple is 1% - 2% of the DC-link voltage.

According to the simulation results, for a module converter switching at 20 kHz with 200V DC-link voltage and 4 A peak line current (2.83 A RMS), a 40 μF capacitor is enough to handle the current ripple and results in a 1% voltage ripple. This simulation result can be easily extended to other voltage and current levels. Based on the simulation result, (4.3) can be derived to calculate the practical value of capacitance needed.

$$\begin{aligned} \text{Capacitance needed} &= 400\ \mu\text{F kHz V/A}_{\text{Line–PEAK}} \\ &= 566\ \mu\text{F kHz V/A}_{\text{Line–RMS}} \end{aligned} \tag{4.3}$$

As the switching frequency increases, smaller capacitance will be needed to fulfill the voltage ripple requirement. If the voltage ripple requirement is more strict, i.e., smaller voltage ripple, the capacitance value has to increase. If the line current increases, more capacitance is needed.

For example, the converter module switching at 40 kHz with 200 V DC-link voltage and 4 A peak line current will need a capacitor:

$$C = \frac{400\ \mu\text{F kHz V/A}_{\text{Line–PEAK}}}{40\ \text{kHz} \bullet 1\% \bullet 200\ \text{V}} \bullet 4\ \text{A} = 20\ \mu\text{F} \tag{4.4}$$

, which is exactly half of the 20 kHz case.

Changing the power of the converter module will not affect the nature of capacitance needed. For example, according to (4.4), a 20 μF, 200 V capacitor is needed for the converter module.

Now we assume the power of converter module is doubled by either double the voltage or the current. If the module voltage is doubled to 400 V, the required capacitance is 10 μF. This is exactly equivalent to two 20 μF, 200 V capacitors connected in series. Instead, if the module line current peak value is doubled to 8 A, the required capacitance is 40μF, which is equivalent to two 20 μF, 200 V capacitors connected in parallel. These two examples illustrate that, the power density of capacitor will not change with the module voltage or current. The only way to change the power density of capacitor is to change the switching frequency.

4.1.4 Capacitor Size and Height

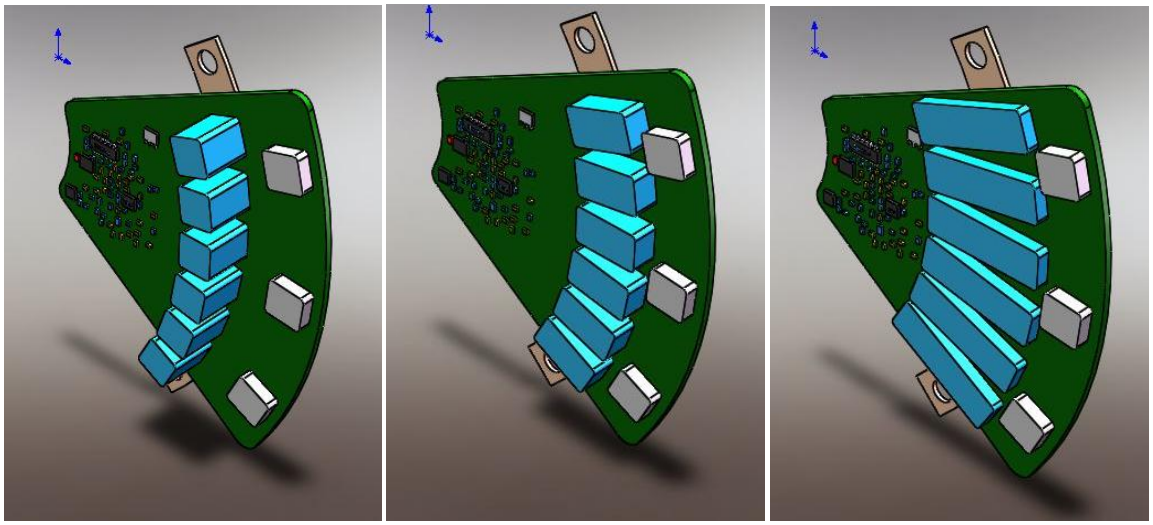
In a practical IMMD design, the capacitor is the most bulky component. It occupies a large portion of converter volume [61][62]. For example, bulky capacitors take approximate 30% of the total converter size in the motor drive [112]. Generally speaking, for same type of capacitor and a given DC-link voltage, the volume of a capacitor is directly decided by its capacitance.

Reducing the capacitance is only one of the goals for an IMMD. The capacitors are the tallest components on the printed circuit board (PCB) and they often determine the overall height of an IMMD. The cross-section area of the IMMD is usually identical to the cross-section area of the motor. As a result, the overall IMMD volume is the product of motor cross-section area and the capacitor height. Not only will the total capacitance greatly affect the size of IMMD, but also the height of the capacitors. If the capacitors are too tall, it becomes a problem as shown in [61] and [62] that a traditional IMMD cannot fully integrate all the dc-link capacitors into one package. Moreover, capacitors with large sizes and heights may cause physical vibration when the motor is running.

According to the analysis of the previous section, the power density of the DC-link capacitor will not change with the module voltage. However, reducing the voltage is a very effective way to reduce the capacitor height. It may not change the overall volume of the capacitor, but as long as the height of the capacitor is reduced, the overall size of IMMD will be reduced.

In the proposed input-series structure, the choice of capacitor is more flexible because the converter module input voltage is a design variable and can be different from the total DC-link input voltage. With more converter modules, the voltage of individual module is reduced. At low voltage levels, there are much more choices of different types of capacitors and more flexibility in capacitor selection and optimization. As a result, the capacitors can be more flat and the height of capacitors is reduced.

Moreover, the more flat capacitors can be distributed over a larger surface area and it benefits the heat dissipation. **Fig. 4.5** illustrates different designs of an IMMD module with same capacitance volume but different capacitor heights. An optimal design should take advantage of all available PCB area to minimize capacitor height.



(a) (b) (c)

Fig. 4.5. Capacitor selection for IMMD
(a) Worst, (b) better, and (c) best choice

4.1.5 Other considerations

There are three different types of capacitors can be used as DC-link capacitors. They are electrolytic capacitors, film capacitors and ceramic capacitors.

- **Aluminum electrolytic capacitors**

Electrolytic capacitors are the most common used capacitors for motor drive applications for they have very high capacitance per volume and low cost. The electrolytic capacitors have self-heal ability so they are suitable for the vibration environment in motor drive. There are also variety of choices for electrolytic capacitors at different voltage and current levels.

Compare to other types of capacitors, electrolytic capacitor uses liquid electrolyte that is more sensitivity to temperature change. When temperature changes, the damage to the film will

increase and cause more hydrogen gas to be generated and result in higher inner pressure or even capacitor failure [113].

Although the electrolytic capacitors have high capacitance, their RMS current rating is very low. Electrolytic capacitor size is actually limited by the capacitor RMS current instead of the capacitance. In other words, if an electrolytic capacitor is selected such that the current rating meets the requirement, its capacitance is far more than necessary.

- **Polypropylene film capacitors**

The film capacitors are non-polarized, high current capacitors usually used in high power applications and AC filters. Compare to electrolytic capacitors, film capacitors have very low capacitance density but high current density. This makes the film capacitors limited by the voltage ripple requirement of a motor drive. If a film capacitor is chosen based on the voltage ripple requirement, i.e., the capacitance, its RMS current value is usually more than enough. Large current handling capability and small parasitic inductance are the advantages of film capacitors [114].

Film capacitors are also self-healing and have better temperature stability [115]. This means the film capacitors can better handle the vibration and temperature in a motor drive, compare to other types of capacitors.

- **Multi-layer ceramic capacitors**

Ceramic capacitors are small size, non-polarized, low cost capacitors. These are very desirable characteristics for an IMMD. However, the noted capacitance of a ceramic capacitor is measured at very low voltage instead of rated voltage. As the terminal voltage is increasing to the

rated value, the capacitance will reduce by 40%-80% [116]. More ceramic capacitors should be installed to compensate for the capacitance drop.

The ceramic capacitors do not have self-heal ability meaning that the size of a ceramic capacitor cannot be very large. Otherwise, thermal mismatch or vibration will cause cracks in the capacitor layers and lead to capacitor failure. For an IMMD where the temperature and vibration are not quite comfortable, the size of a single ceramic capacitor is limited. A converter module may need multiple ceramic capacitors to connect in series and in parallel to match the voltage rating and capacitance requirement. However, for a converter module with more than 1 kW, it usually needs tens of ceramic capacitors connected in parallel. It is very difficult to share the current equally among these capacitors. Consequently, the ceramic capacitors are usually limited within 1 kW design.

The RMS current of a ceramic capacitor is also limited by the thermal performance. Since the capacitor is very small size, it is easy to dissipate heat and avoid hot spot in the inner layers. Same as a film capacitor, a ceramic capacitor usually has excessive RMS current ability but limited capacitance.

4.2 Comparative Evaluation of Different Capacitor Types

4.2.1 Design Specifications

The capacitor will be installed in a converter module with 200 V DC-link input voltage and 1% voltage ripple. The line current peak value is 4 A.

(4.2) calculates the capacitor RMS current to be constant 1.84 A for the converter module. From (4.3), the capacitance needed for this converter module is 800 μF/kHz,which is inversely proportional to the switching frequency. The selected capacitor must meet both current and capacitance requirements. The specifications are summarized in **Table 4.1**.

The result in this section is linearly scalable to other voltage and current ratings.

Switching frequency	1 kHz	10 kHz	20 kHz	40 kHz	80 kHz
Capacitor RMS current	1.84 A	1.84 A	1.84 A	1.84 A	1.84 A
Max. voltage ripple	2 V	2 V	2 V	2 V	2 V
Capacitance needed	800 μF	80 μF	40 μF	20 μF	10 μF

Table 4.1. Capacitor specifications for the converter module

4.2.2 Selection of Different Types of Capacitors

The selection of electrolytic capacitor only depends on the RMS current because it has excessive capacitance. As shown in **Table 4.2**, the capacitor selection does not alter with the switching frequency.

Switching frequency	1 kHz	10 kHz	20 kHz	40 kHz	80 kHz
Electrolytic cap. type	250 V Panasonic EETXB2E821KJ				
Capacitance	820 μF				
RMS current rating	2.0 A				
Volume	35325 mm^3				
Voltage ripple	1.9 V	0.19 V	0.09 V	0.046 V	0.023 V

Table 4.2. Electrolytic capacitor selection

The film capacitor has large RMS current rating, and hence it is selected according to the capacitance requirement. In this case, the EPOS 250V 10 μF capacitor is used as the basic element in capacitor bank. It is because this capacitor height is only 1 inch and the power density is a little higher than other capacitors in the same series. As the switching frequency increase, the required capacitance is reducing.

Switching frequency	1 kHz	10 kHz	20 kHz	40 kHz	80 kHz
EPOS 250 V 10 μF in parallel	80	8	4	2	1
Capacitance	800 μF	80 μF	40 μF	20 μF	10 μF
RMS current rating	216 A	21.6 A	10.8 A	5.4 A	2.7 A
Volume	677240 mm^3	67724 mm^3	33862 mm^3	16931 mm^3	8465 mm^3
Voltage ripple	2 V	2 V	2 V	2 V	2 V

Table 4.3. Film capacitor selection

The ceramic capacitors occupy very small volume, compare to other two types. But the quantity is too large to be implemented when the switching frequency is below 20 kHz. The ceramic capacitors, though very appealing, are limited to low power and high switching frequency motor drives.

Switching frequency	1 kHz	10 kHz	20 kHz	40 kHz	80 kHz
TDK 100V 10 μF in parallel and series	640	64	32	16	8
Capacitance	800 μF	80 μF	40 μF	20 μF	10 μF
RMS current rating	960 A	96 A	48 A	24 A	12 A
Volume	41950 mm^3	4195 mm^3	2098 mm^3	1049 mm^3	524 mm^3
Voltage ripple	2 V	2 V	2 V	2 V	2 V

Table 4.4. Ceramic capacitor selection

It is clear that the film capacitors and ceramic capacitors are more favorable for higher switching frequency. At low switching frequency, electrolytic capacitors will be more compact and less expensive.

4.2.3 Optimal Switching Frequency

At higher switching frequency, less capacitance is needed and the RMS current rating of the capacitors will drop. There exists a switching frequency where the RMS current rating of the capacitor drops to the RMS current of the converter. Beyond this switching frequency, the capacitor is limited by the RMS current and can no longer reduce its size by increasing the switching frequency. This is the optimal switching frequency for the capacitor.

The capacitors shown in **Table 4.2**, **Table 4.3** and **Table 4.4** have their own optimal switching frequencies, which are 0.976 kHz, 117.4 kHz and 522 kHz respectively. At these switching frequencies, the capacitors will reach their minimum volume. It is desirable to identify the limit of the capacitors and make the best decision when designing a motor drive module. In a real design, the switching frequency of a converter module is also decided by many other factors, such as switching loss, circuit protection speed and motor winding limit.

Fig. 4.6 shows the capacitor volume used in a converter module as specified in section 4.2.1. This figure provides a volume comparison between different types of capacitors.

Using film capacitors or ceramic capacitors with small capacitance values may have a disadvantage that the DC-link voltage is not robust and causes some voltage ringing. This problem is discussed and solved in [117].

Increasing the switching frequency will not induce extra loss in the motor. As discussed in [118], the motor copper loss due to the switching ripple will decrease with higher switching frequency. The motor iron loss will maintain almost identical for switching frequency higher than 4-5 kHz [119].

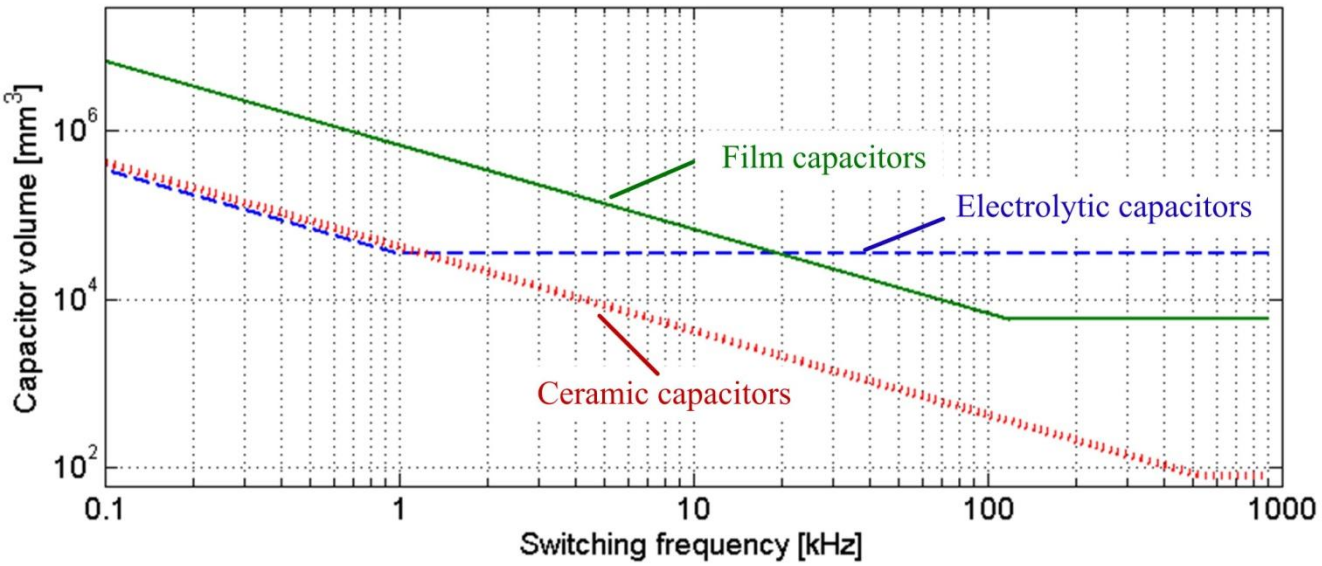


Fig. 4.6. Capacitor volume vs switching frequency

Chapter 5

Gate Signal Interleaving

One advantages of the proposed multilevel motor drive is that it has multiple converter modules. Multiple modules provide more control freedom. For example, the PWM of different modules can be triggered at different instance to achieve desirable features.

Gate signal interleaving technique is a well known PWM shifting technique that can reduce capacitor size and improve the performance of buck converter with multi-legs [120]. This chapter discusses the advantages when applying gate signal interleaving to the proposed series-connect multilevel topology. Simulation and experiment results are presented to validate the advantages of this technique.

5.1 Review of Conventional Interleaving Technique

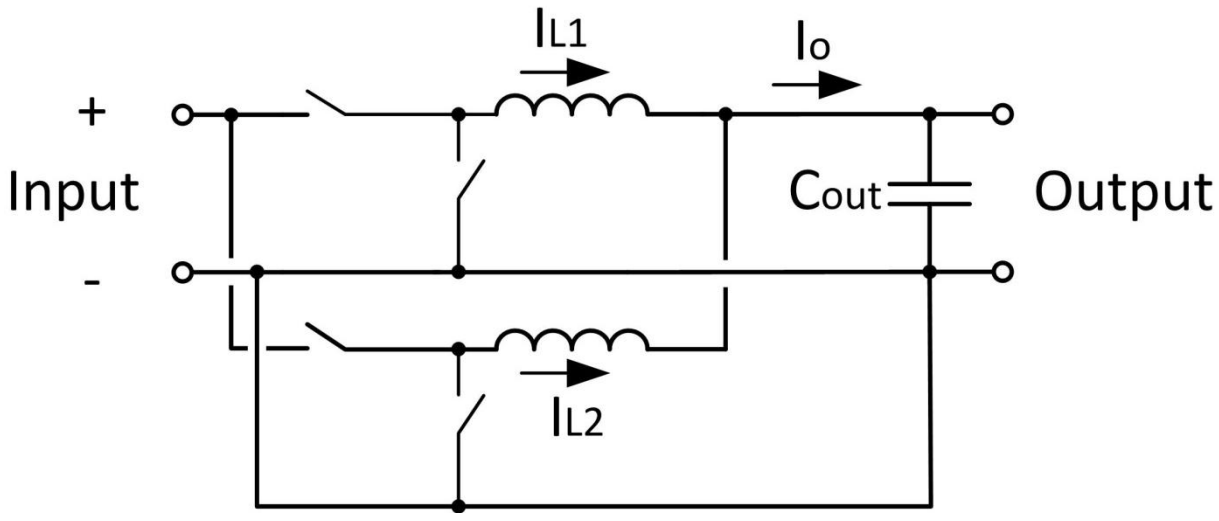


Fig. 5.1. Conventional interleaving technique for parallel-connect modules [120]

Conventional gate signal interleaving technique is widely used in voltage regulator for computer processors, where the output voltage is low but output current is very high. Two buck converters are connected in parallel and supply the same output capacitor, as shown in **Fig. 5.1**.

These buck converters could have exactly the same gate signal so the output current I_{L1} is equal to I_{L2}, and I_o is simply twice of I_{L1}. The current ripple of I_o is also twice of I_{L1}.

An alternative way to operate the buck converters is to shift the gate signals of the second buck converter by 50% of its switching cycle. This is called gate signal interleaving. As a result, its current I_{L2} will also be shifted by 50% of its switching cycle. When triangle-shape I_{L1} and I_{L2} are added up, the total current ripple of I_o is smaller than the case without interleaving. **Fig. 5.2** [120] demonstrates this current ripple canceling effect.

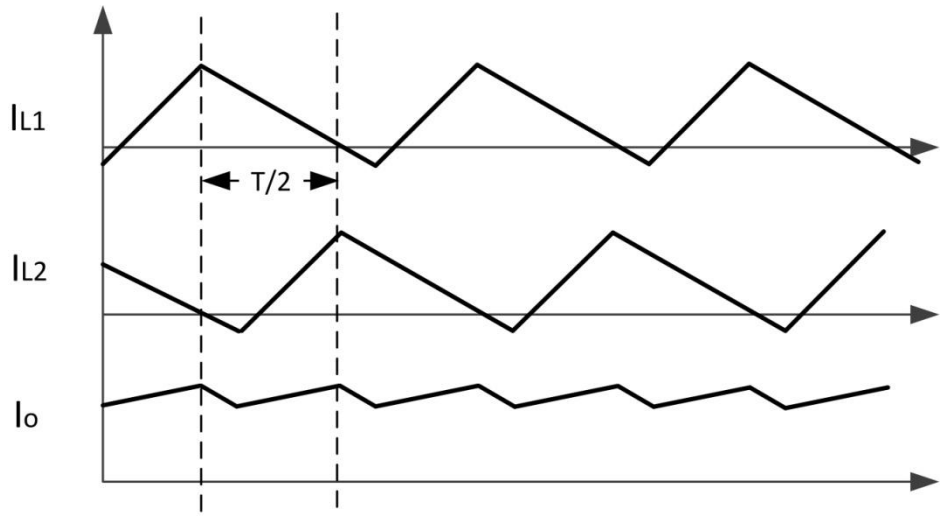


Fig. 5.2. Triangle current ripple canceling effect [120]

The parallel-connect buck converters will greatly benefit from interleaving technique. When there are several buck converters share the total output current, the total current ripple is greatly reduced by interleaving. To meet the output voltage ripple requirement, the output DC capacitor C_{out} can have much smaller size.

5.2 Proposed Gate Signal Interleaving for Series-Connect Modules

5.2.1 Realization of Interleaving Gate Signals

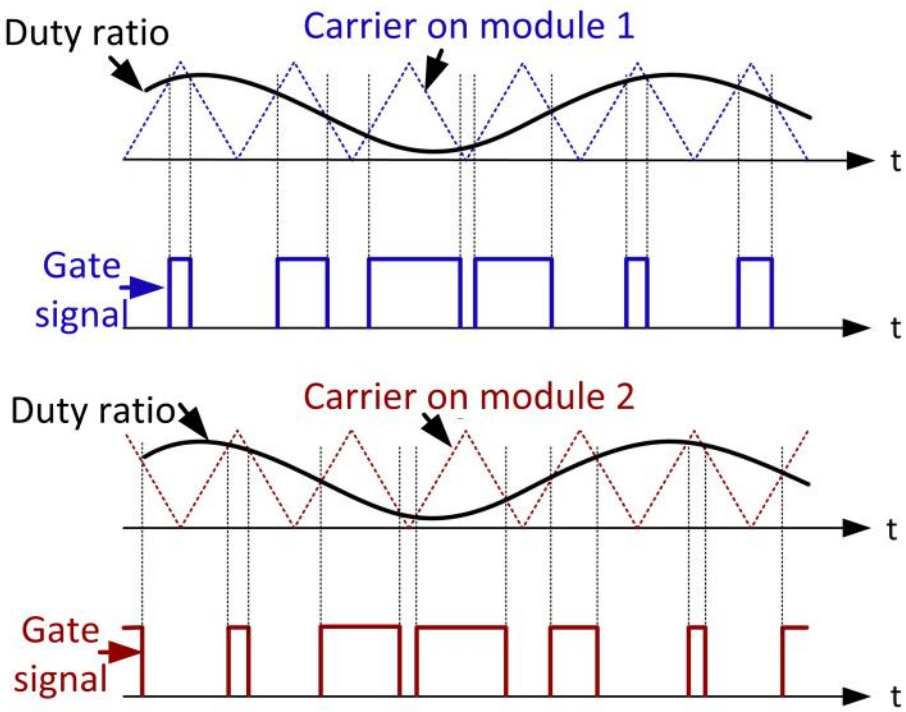
Conventional interleaving can cancel triangle current ripple for buck converters, as shown in **Fig. 5.2**. For a motor drive module, however, the current ripple (i.e. capacitor current) is a square wave. The DC-link capacitor voltage ripple is in triangle shape. It is proposed in this thesis to cancel the triangle voltage ripple of series-connect converter modules. This proposed gate signal interleaving technique is actually a duality form of the conventional interleaving technique for parallel-connect buck converters.

In a motor drive module, the function of DC-link capacitors is to stabilize the DC-link voltage and to smooth the input current from a DC source. The total DC-link voltage ripple needs to meet the 1% requirement to protect the input DC source, as discussed in Chapter 4. The purpose of interleaving gate signals is to build converter modules with even smaller capacitors. To achieve this, the gate signals of different modules are shifted from each other. Since they still have identical duty ratios, the fundamental components of the output sinusoidal voltages are the same. However, the shifted gate signals will create shifted voltage ripples. Thus when the ripples

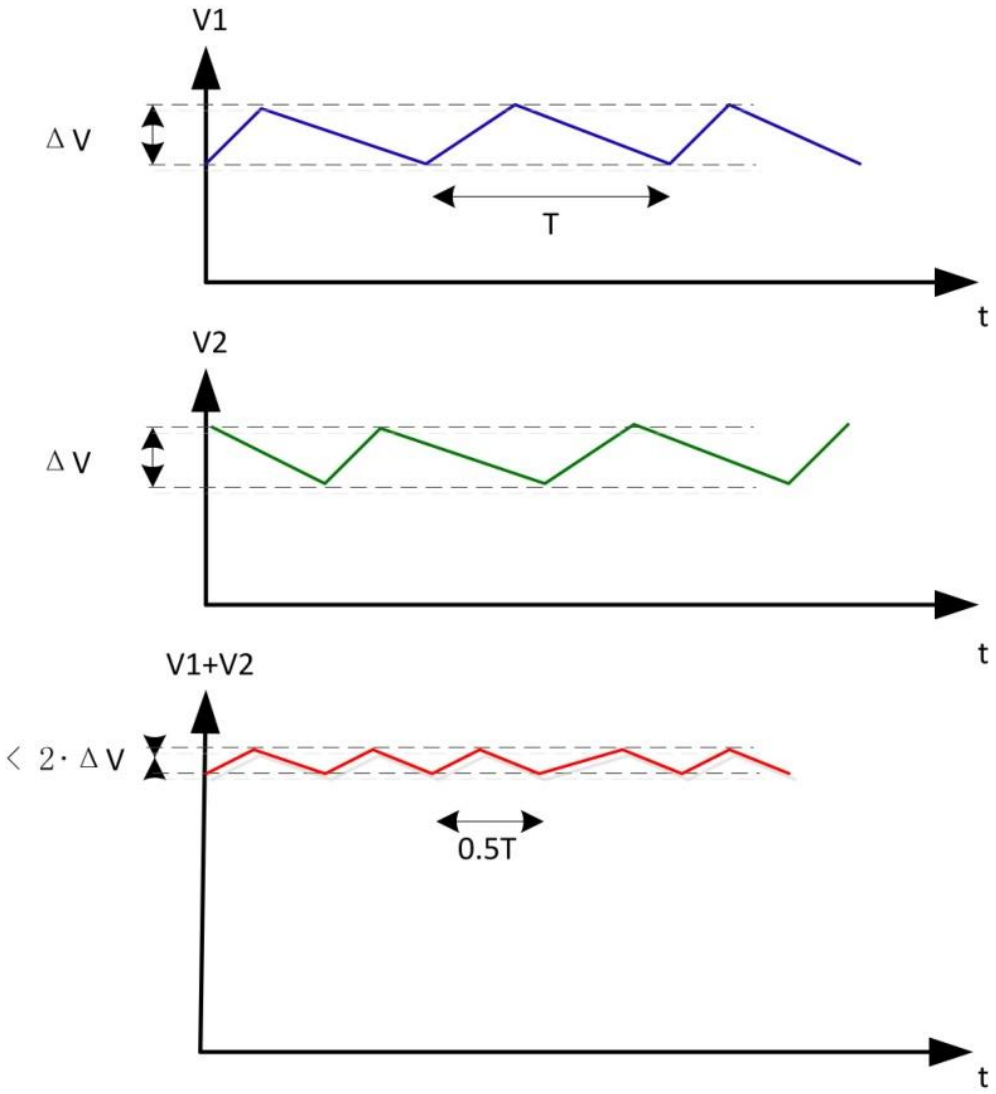
are combined, they tend to cancel each other and result in a smaller total ripple voltage on the DC-link.

By interleaving, the voltage ripple on one module can be larger than 1%, but when several modules are working simultaneously, the total DC-link ripple can still meet the 1% requirement and the capacitor size is smaller than the case without interleaving. In another hand, if the module still has 1% voltage ripple, the total DC-link ripple can have a total voltage ripple smaller than 1%. This helps to reduce the input filter size and compress EMI.

Fig. 5.3 shows an example of two converter modules with gate signal interleaving. Module PWM carriers and gate signals are shifted by 180 °. This interleaving technique reduces the voltage ripple requirement on each module, but it does not reduce the capacitor current. As a result, film capacitors and ceramic capacitors are more beneficial from interleaving since they are limited by the voltage ripple requirement, as discussed in Chapter 4.



(a)



(b)

Fig. 5.3. Illustration of proposed gate signal interleaving
(a) The generation of gate signals, (b) the synthesized voltage ripples

The interleaving mechanism is also effective for space vector PWM (SVPWM). The active switching vectors for two modules are shifted by half switching cycle. Hence the voltage ripples from two modules are also shifted by 180°. In this way, smaller total voltage ripples can be achieved.

5.2.2 Experiment Verification of Interleaving Technique

To validate the interleaving technique, DC-link voltage ripple with and without interleaving should be compared. However the DC-link voltage ripple is typically too small to be measured accurately. In the experiment, to illustrate the interleaving in a better way, DC-link input current Δi_{dc} is measured to indicate the voltage ripple of DC-link, as shown in **Fig. 5.4**. The switching frequency is intentionally reduced to 20 kHz in the experiment, so there will be a larger current ripple.

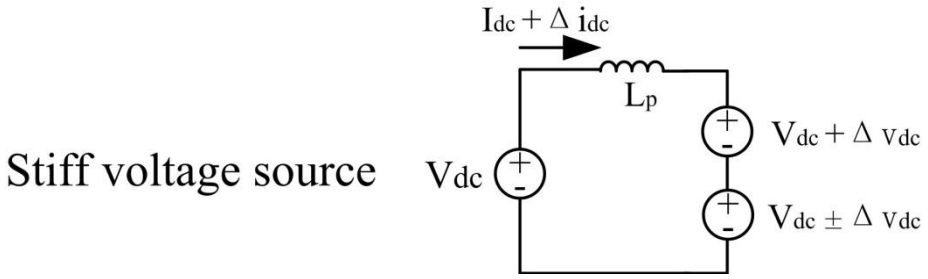


Fig. 5.4. Equivalent circuit of IMMD with two modules

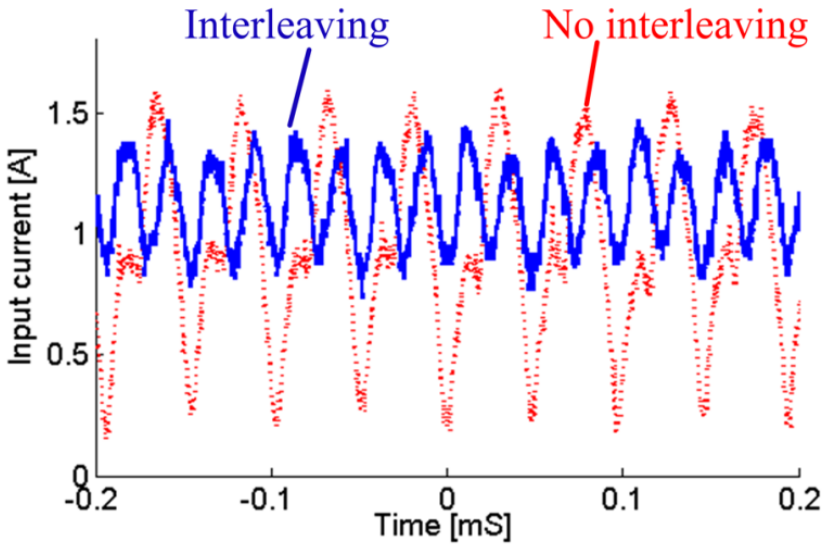


Fig. 5.5. Experiment result: put current ripple with and without interleaving

The experiment results are shown in **Fig. 5.5**. With interleaving technique, the input current ripple is reduced by 57%. This validates the effectiveness of interleaving technique.

5.3 Comparisons between Series-Connect and Parallel-Connect Converter Modules

Motor drive modules can be connected in parallel so the square-shape current ripple can be shared and reduced [59][112]. This interleaving method is also effective in reducing the capacitor size and voltage ripple.

To understand the advantages and limits of both interleaving technique, a side-by-side comparison is presented in this section.

5.3.1 Interleaving of Parallel-Connect Converter Modules

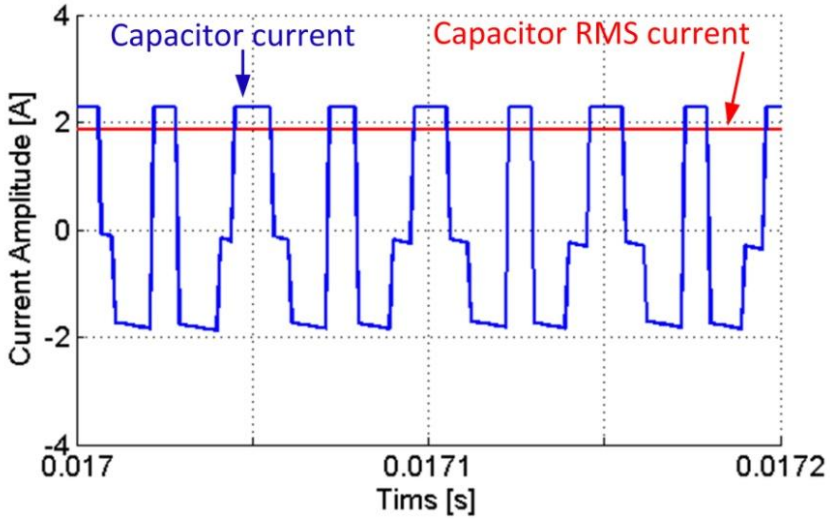


Fig. 4.2(b). Square-shape capacitor current in a motor drive module with 20 kHz switching frequency

The motor drive module capacitor has a square-shape current waveform. For reader's convenience, **Fig. 4.2(b)** is repeated here. When two interleaving motor drive modules are connected in parallel, the square-shape current ripples from two modules can combine and cancel each other. As a result, the net current flowing through the module capacitor can be reduced. The DC-link voltage ripple can thus be reduced [59][112].

However, as shown in **Fig. 5.6**, there exists parasitic inductance L_m between the motor drive modules, typically in the range of 100 nH - 1000 nH.

If L_m could provide an instant change of current to compensate the square-shape current ripple between two modules, the interleaving would be effective. However this is not true. The voltage on L_m is decided by the DC-link voltage difference between two modules, which is a triangle-shape voltage ripple with small amplitude.

The parasitic inductance L_m tends to prohibit the cancelling of square-wave current ripples. The effect of interleaving technique in this case is quite limited by L_m, especially at high switching frequency.

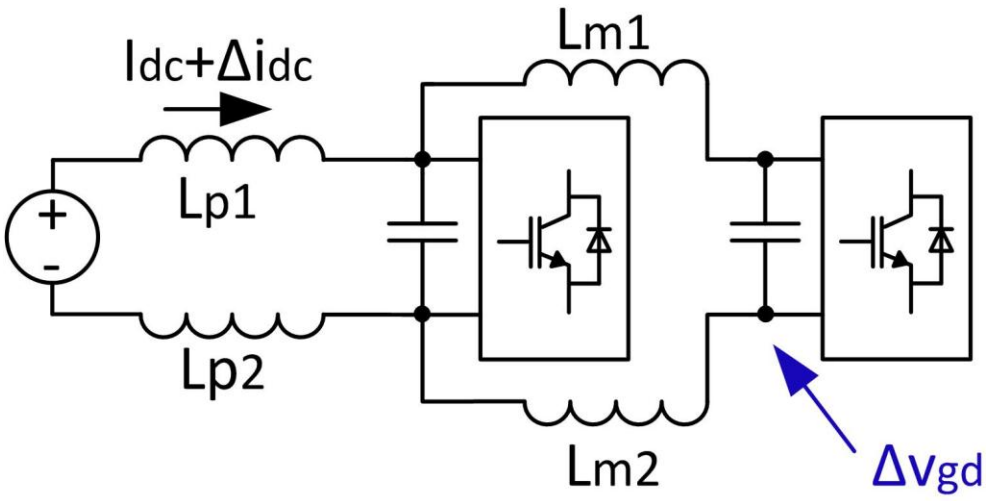


Fig. 5.6. Parallel-connect motor drive modules with parasitic inductances

5.3.2 Comparison of Simulation Results

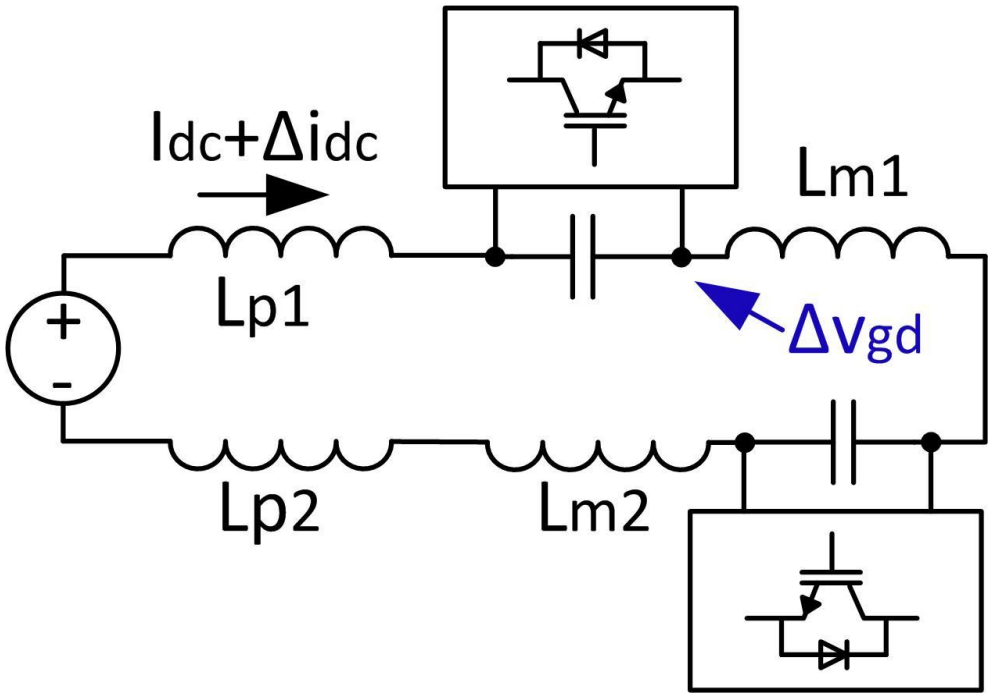


Fig. 5.7. Series-connect motor drive modules with parasitic inductances

Parameter	Module Capacitor	Module Voltage	$L_{p1,2}$	$L_{m1,2}$
Value	10 [μF]	100 [V]	1 [μH]	500 [nH]

Table 5.1. Simulation parameters

The comparison between parallel-connect and series-connect interleaving can be demonstrated by simulation results. **Fig. 5.6** and **Fig. 5.7** are used as simulation models, and all converter modules in simulation models are identical. As a result, the parallel-connect model will

have half voltage and twice current comparing to the series-connect model. To make a fair comparison, the simulation results are converted. The current of parallel-connect model is divided by two.

In the simulation, the input current ripple ΔI_{dc} is measured to indicate the effect of interleaving technique. The module ground voltage ripple ΔV_{gd} is also measured because it directly decides EMI and module reliability. The simulation is run at different switching frequency (50 kHz, 100 kHz, 150 kHz, 200 kHz) and different load current (5 A, 10 A). The modulation index is 0.7. The simulation results are summarized in **Table 5.2**, **Table 5.3**, **Fig. 5.8**, and **Fig. 5.9**.

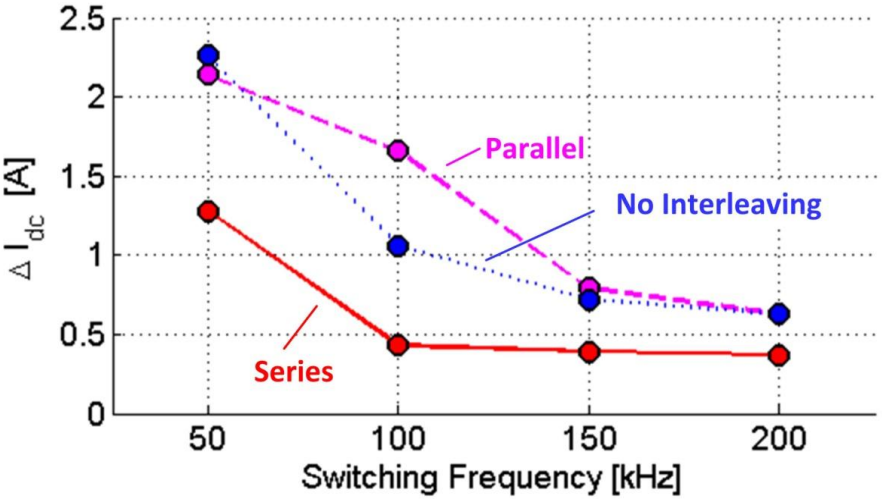
Switching frequency		50 kHz	100 kHz	150 kHz	200 kHz
Series-connect	ΔI_{dc} [A]	1.28	0.43	0.39	0.37
	ΔV_{gd} [V]	2.43	1.21	0.83	0.63
Parallel-connect	ΔI_{dc} [A]	2.14	1.66	0.79	0.63
	ΔV_{gd} [V]	0.96	1.49	0.79	0.6
Without interleaving	ΔI_{dc} [A]	2.26	1.06	0.72	0.63
	ΔV_{gd} [V]	2.07	0.88	0.68	0.57

Table 5.2. Simulation results for interleaving @ 5 A load current

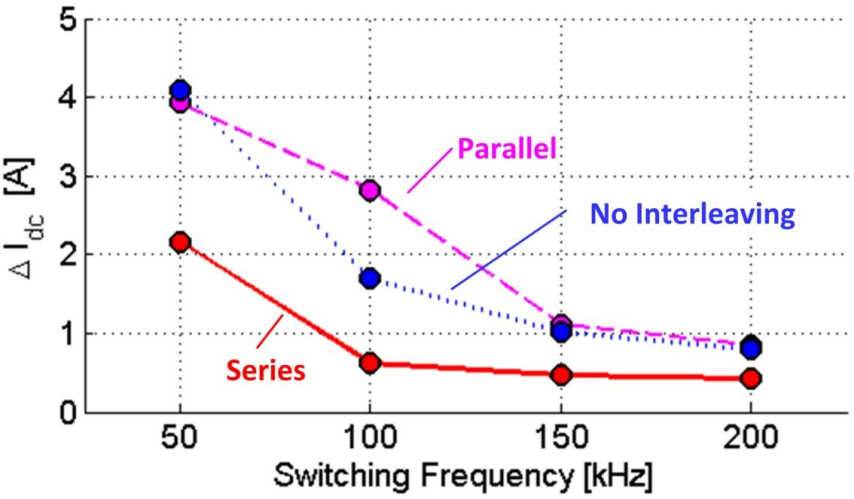
Switching frequency		50 kHz	100 kHz	150 kHz	200 kHz
Series-connect	ΔI_{dc} [A]	2.16	0.62	0.47	0.42
	ΔV_{gd} [V]	4.84	2.37	1.58	1.21
Parallel-connect	ΔI_{dc} [A]	3.93	2.82	1.11	0.85
	ΔV_{gd} [V]	1.74	2.78	1.33	1.01
Without interleaving	ΔI_{dc} [A]	4.10	1.69	1.01	0.80
	ΔV_{gd} [V]	3.95	1.59	1.18	0.94

Table 5.3. Simulation results for interleaving @ 10 A load current

As shown in **Fig. 5.8** (a) and (b), the simulation results of input current ripple ΔI_{dc} are consistent under different load currents. For series-connect modules, regardless of switching frequency, ΔI_{dc} is almost reduced by half comparing to the case without interleaving. This result proves that interleaving technique is working effectively for series-connect modules at different load currents and switching frequencies.



(a)



(b)

Fig. 5.8. Simulation results of input current ripple ΔI_{dc}

(a) 5 A load current ,and (b) 10 A load current

By contrast, the simulation results for parallel-connect modules are not consistently improved when comparing to the case without interleaving. At 50 kHz switching frequency, parallel-

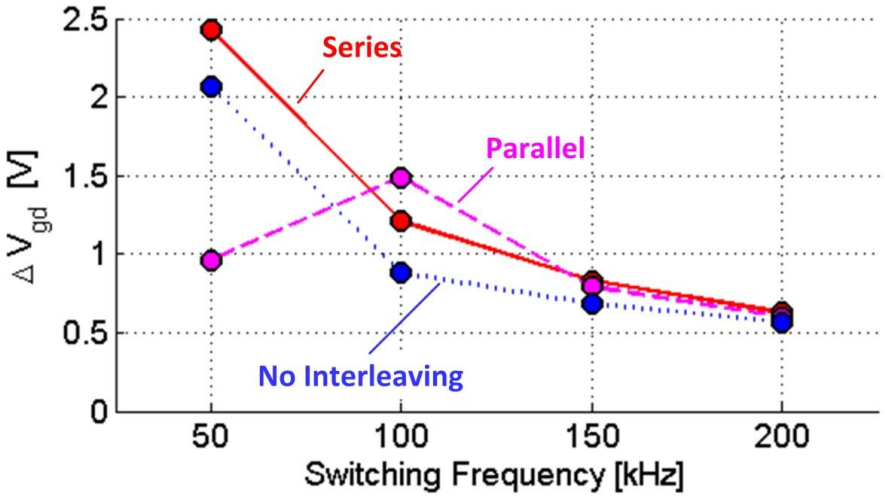
connect interleaving has a slightly smaller current ripple than no interleaving. Because of parasitic inductance which prohibits the cancelation of current ripples, interleaving technique is working but not very effective at this switching frequency. At 100 kHz, this problem becomes more severe, because interleaving technique leads to a current ripple larger than no interleaving. At this switching frequency, the parallel-connect modules and parasitic inductance are forming into a parallel resonant tank. The circuit is becoming sensitive to any disturbance. However, the interleaving technique itself is a very large disturbance generator. As a result, the input current ripple is increased and the interleaving technique has an adverse effect at this frequency. 150 kHz and 200 kHz are frequencies beyond the resonant frequency. Hence the parasitic inductance tends to dominant the parallel-connect modules. The interleaving will lose its effect because the parasitic inductance will almost 'block' the current ripple canceling between parallel-connect modules. As a result, input current ripple does not change, no matter with or without interleaving. This phenomenon can be proved by the simulation results.

As shown in **Fig. 5.9** (a) and (b), the simulation results of ground voltage ΔV_{gd} are also consistent under different load conditions.

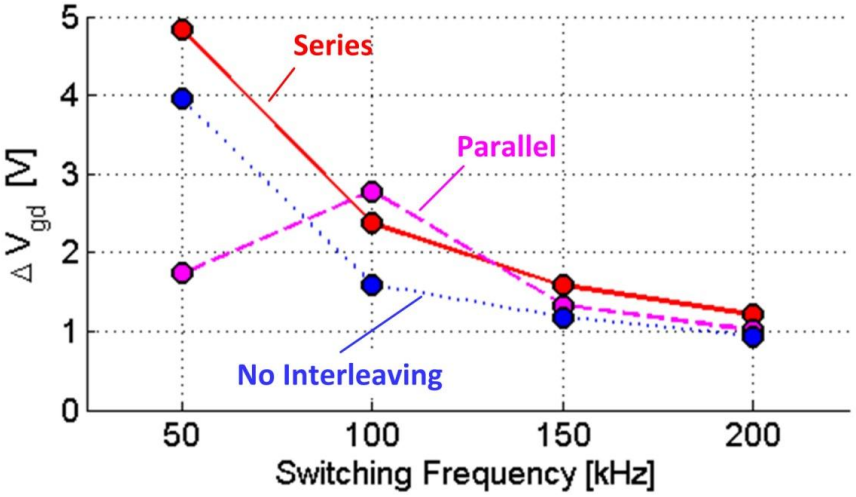
ΔV_{gd} of series-connect modules are slightly larger than no interleaving case at 50 kHz and 100 kHz. This is due to the nature of series-connection: the ground of the upper converter module is floating. This is not a problem because the difference between series-connect and no-interleaving is actually very small. At 150 kHz and 200 kHz, the difference already becomes negligible.

For parallel-connect modules, again, the interleaving technique does not always work as expected. At 100 kHz, interleaving is harmful due to resonance. At lower frequency (50 kHz), the impedance of parasitic inductance is still small enough and interleaving works properly. At

higher switching frequencies (150 and 200 kHz), the parasitic inductance dominates the circuit model and blocks the current ripple cancelation. As a result, the ground voltage ripples for interleaving and no interleaving are consistent.



(a)



(b)

Fig. 5.9. Simulation results of ground voltage ripple ΔV_{gd}

(a) 5 A load current ,and (b) 10 A load current

5.3.3 Summary of Interleaving Techniques

Conventional interleaving technique is applied to buck converters to reduce output capacitor triangle-shape current ripple. The parasitic inductances between different branches will not affect interleaving at all because the parasitic inductances are connected in series with the main filter inductors.

Interleaving technique can also be adapted to converter modules in machine drive. However, for machine drive, the desire is to reduce the size of input capacitor. The story is very different because the input DC-link capacitor has a square-shape current ripple.

Conventional parallel-connect modules can use interleaving technique to reduce DC-link capacitor current and input current ripple [59][112]. However, it is limited by the parasitic inductance between converter modules. At a certain switching frequency that coincides with the parallel resonant frequency, interleaving technique will have an adverse effect. At frequencies higher than the resonant frequency of parallel modules, interleaving has no negligible effect.

The proposed series-connect modules can use interleaving to reduce total voltage ripple and input current ripple. Total voltage ripple is the superposition of different series-connect modules. It is not limited by the parasitic inductance because there is no square-shape current involved. Actually, the parasitic inductance can act as an input filter and helps to further reduce the input current ripples. The effect of interleaving will not degrade when switching frequency becomes higher.

5.4 Common-Mode Voltage/Current Reduction

Common-mode voltage can cause serious machine problems in a PWM machine drive system [121][122]. The common-mode voltage will induce common-mode current and bearing current, leading to bearing failure and conducted/radiated EMI.

There exist parasitic capacitance between stator windings, rotor windings and machine frame, as discussed in [121] and shown in **Fig. 5.10**. The machine frame is connected to ground through a ground wire. The parasitic capacitance provides a path for the common-mode current. For simplicity, the machine common-mode circuit is modeled as an equivalent capacitance in this thesis. Further detail of the machine circuit is beyond the scope of this thesis.

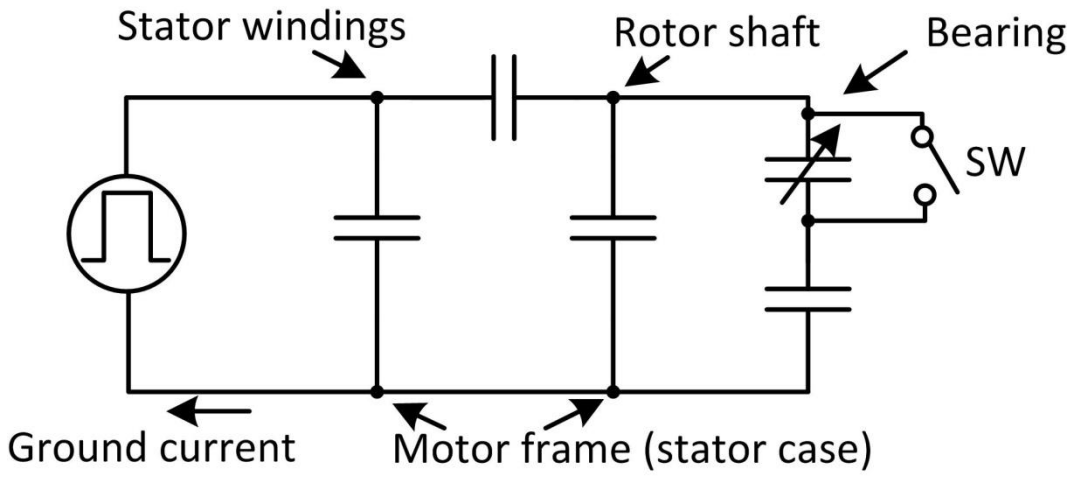


Fig. 5.10. Common-mode equivalent circuit of a machine [121]

5.4.1 Common-Mode Voltage with Interleaving

The machine segments are supplied by individual converter modules. Without interleaving, all the converter modules will output identical voltage and hence identical common-mode voltage. The contributions from all converter modules will be superimposed inside machine stator.

With interleaving, the contributions from different converter modules will be different and tend to cancel each other. The superposition of common-mode voltages from all modules in this case will be smaller. To illustrate how interleaving technique works, an example of two modules with SVPWM is shown in **Fig. 5.11**.

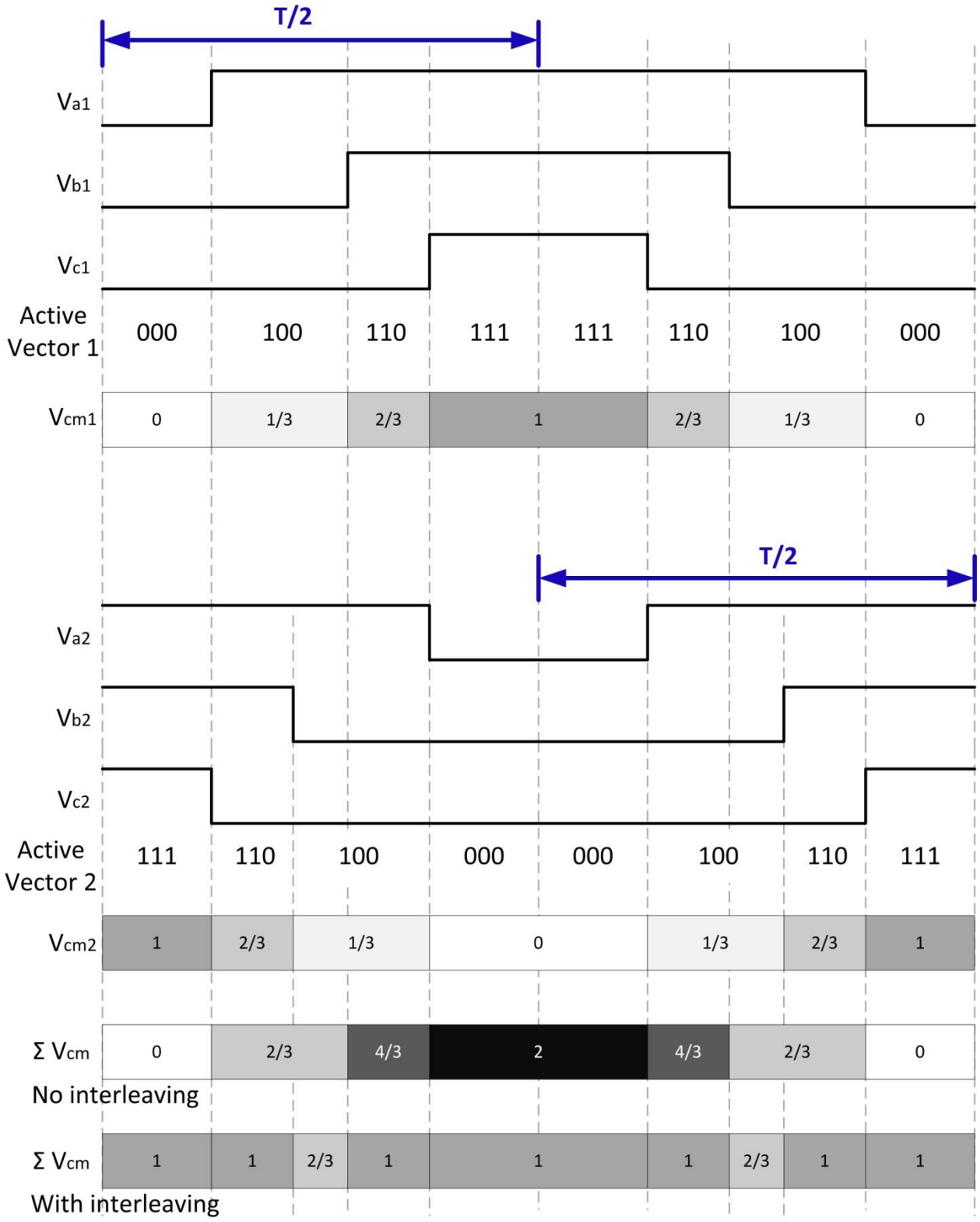


Fig. 5.11. Illustration of common-mode voltage with interleaving

The common-mode voltage V_{cm} of a module can be calculated by its switching pattern. V_{cm} does not depend on the three-phase output voltage of the module. Instead, it only depends on the count of '1's in the switching vector. When the active switching vector is "000", V_{cm} reaches its minimum value 0 p.u.. When the active switching vector is "111", V_{cm} reaches its maximum value, i.e 1 p.u.. Without interleaving, V_{cm} from two modules will be identical and the total V_{cm} thus has a minimum value 0 p.u. and a maximum value 2 p.u..

With interleaving, as shown in **Fig. 5.11**, the active switching vector 2 is shifted from active switching vector 1 by half switching cycle. In this way, the maximum of V_{cm1} is always overlaying the minimum of V_{cm2}, and vice versa. In this example, at most of the time, ΣV_{cm} is exactly 1 p.u.. In general, the effectiveness of interleaving technique also depends on the modulation index and orientation of output voltage vector.

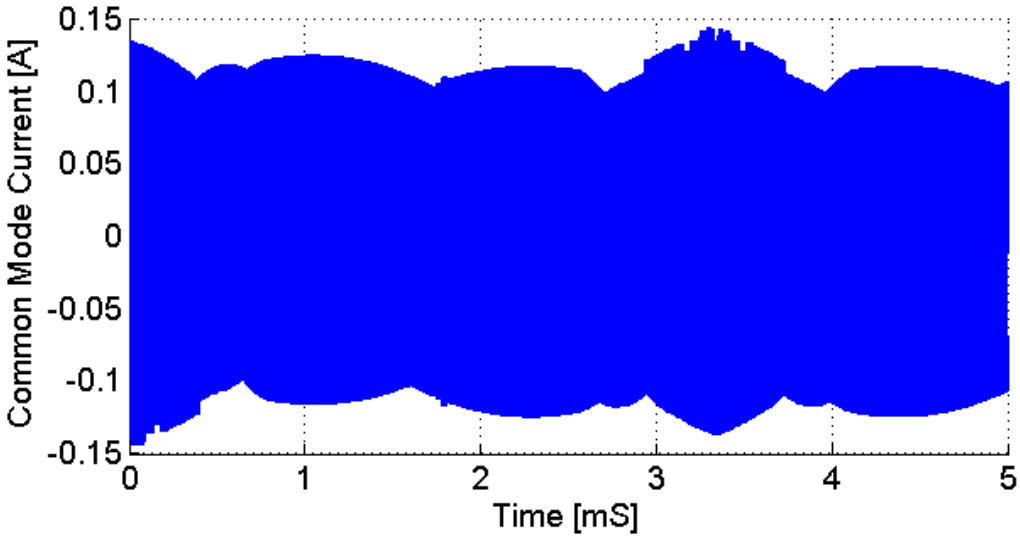
With interleaving technique, the common-mode voltage of the whole machine is very smooth and has small AC amplitude, though the individual machine segment still experience a common-mode voltage generated by their own converter module. The common-mode current will be limited inside the machine stator. The current through the machine ground wire and bearing can be reduced by interleaving.

5.4.2 Simulation Results

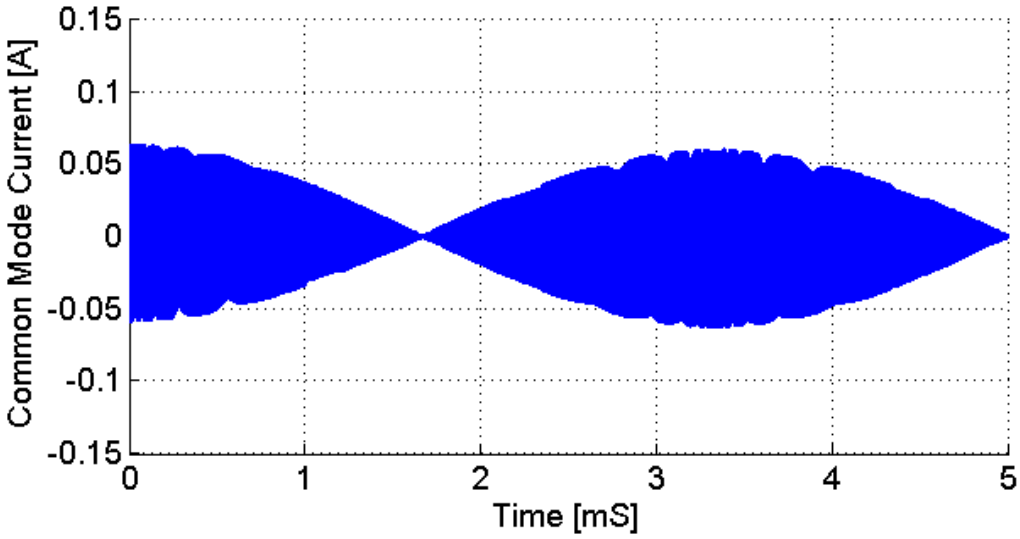
In simulation, the machine is modeled as an equivalent capacitor with 1.1 nF. Two converter modules are operated at 100 V and 100 kHz switching frequency. Constant sinusoidal voltage with 80 Vpp is supplying the machine segments. As shown in **Fig. 5.12**, the machine common-mode current is greatly reduced by interleaving technique. Without interleaving, the common mode current has a 0.27 A peak to peak value. With interleaving, the peak to peak value is

reduced to 0.11 A. With interleaving, there also exist some ‘sweet’ points where the common-mode current is exactly 0. At certain points, the interleaving can perfectly cancel the common-mode voltage from two modules. SVPWM is probably not an optimal PWM technique to minimize common-mode voltage/current. With interleaving, other advance PWM modulation technique may be able to maintain the common-mode voltage/current to be always zero. This is a possible future work beyond this thesis.

Fig. 5.13 shows the simulation results of zoom-in common-mode current. This provides a close view of the shape of current waveform. Without interleaving, the current has many high frequency harmonics due to the asymmetry of common-mode voltage in one switching cycle. By comparison, when interleaving is applied, the common-mode current is triangle-shape with twice the switching frequency. This simulation result shows that both the fundamental amplitude and harmonic components of common-mode current are reduced by interleaving technique.



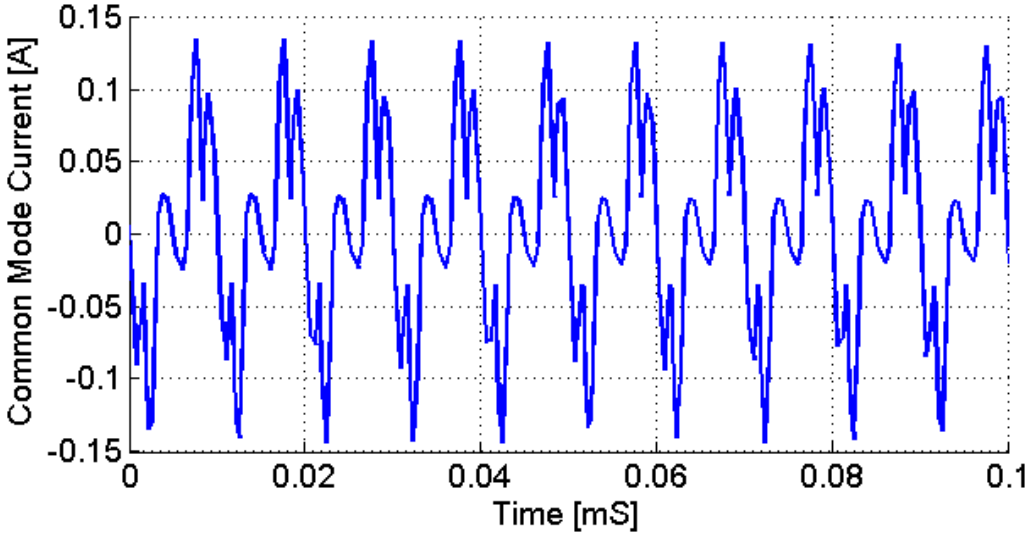
(a)



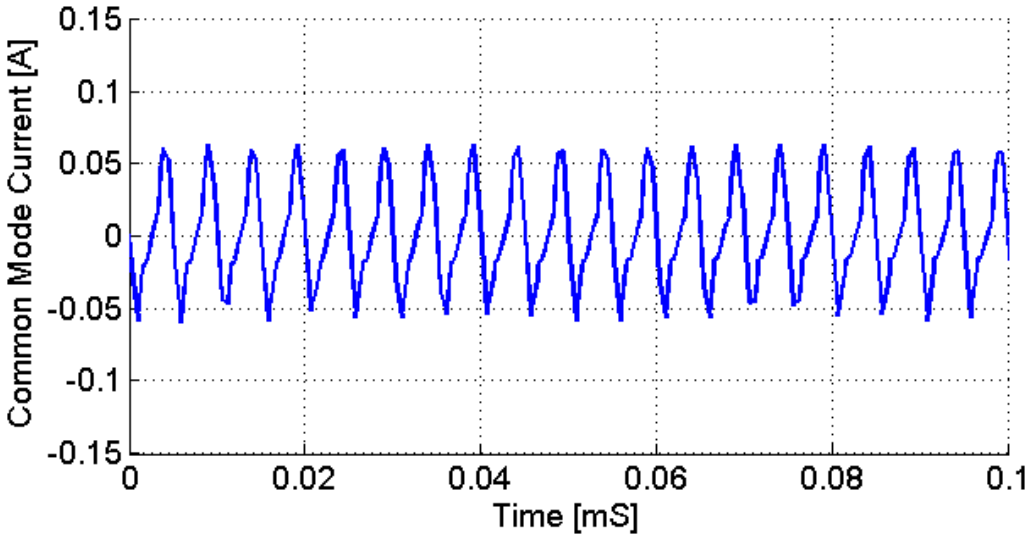
(b)

Fig. 5.12. Simulation results of common-mode current

(a) without interleaving, and (b) with interleaving



(a)



(b)

Fig. 5.13. Simulation results of zoom-in common-mode current

(a) without interleaving, and (b) with interleaving

5.5 Interleaving Effect on Machine Line Current Ripples

Machine is supplied by converter modules with PWM output voltages. Typically the machine line current is sinusoidal waveform and its current ripple is negligible because of high PWM switching frequency and large machine inductance.

However, careful considerations need to be taken when the machine is split into several segments. Interleaving technique intentionally put different voltages on machine windings. In this section, the interleaving effects and limits are discussed.

5.5.1 Machine Segments in Different Pole Paires

As proved in previous sections, machine segments located in different pole pairs have zero magnetic coupling between each other. Different machine segments are equivalent to different individual small machines. The machine inductances will act as filter inductors. As a result, interleaving on different converter modules will have no effect on the machine line current ripples. No matter interleaving is applied or not, the machine current ripples do not change.

5.5.2 Machine Segments in Same Pole Pair but Different Slots

As discussed in section 3.4.1, machine segments in same pole pair but different slots tend to have a large magnetic coupling factor and act as an equivalent transformer. Interleaving technique will apply different PWM signals to the primary and secondary sides of the transformer.

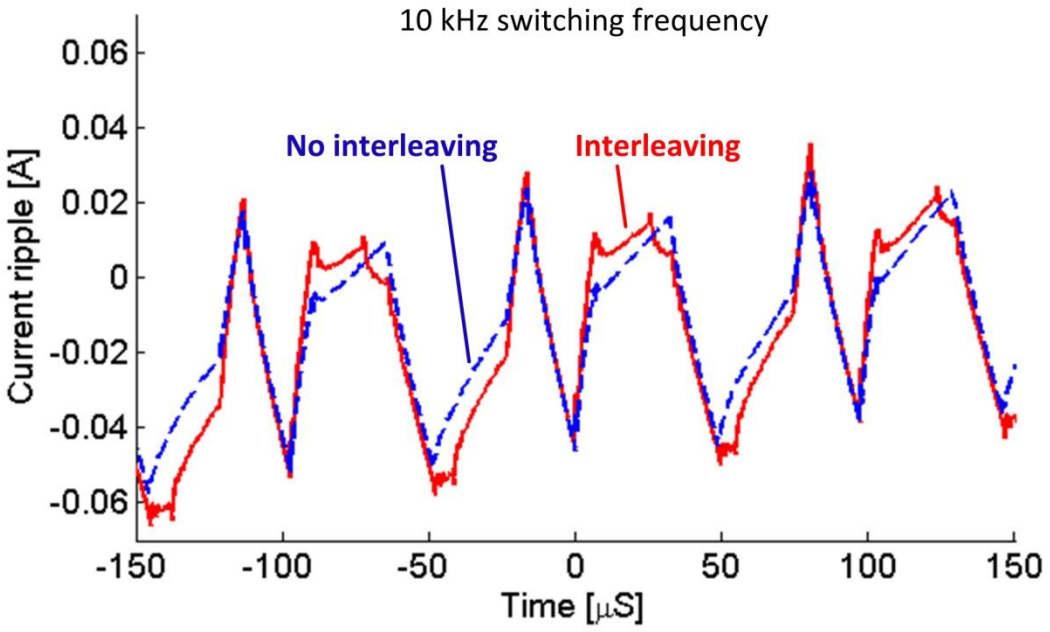
Since all PWM signals have identical duty ratio, the fundamental sinusoidal current waveform of the machine will be identical. However, the interleaving within one switching cycle tends to increase the line current ripples [123]. This effect depends on the leakage inductance of the equivalent transformer.

In general, the leakage inductance is large enough to filter the current ripple and provides a smooth current waveform. Although the current ripple is increased, it is still negligible comparing to the fundamental current waveform. A set of experiment test results are presented to show the effect.

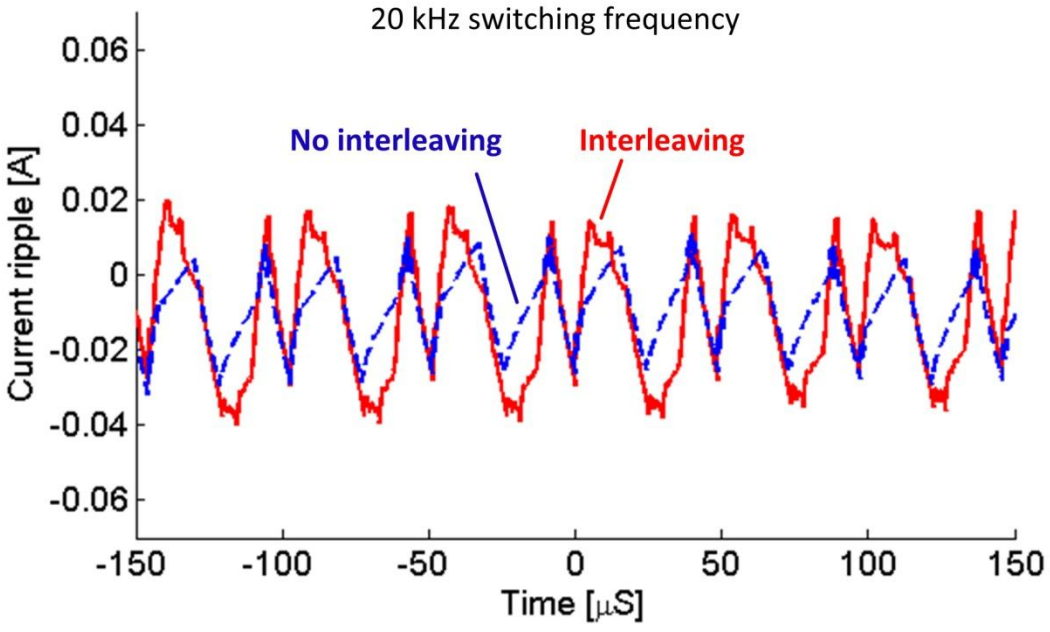
Notice that in the experiment, machine line currents (with 5 A peak value) are directly measured. The fundamental components of the line currents are changing very slowly and can be treated as almost constant values at the tested switching frequencies. The current ripples can be extracted by excluding the contributions from these fundamental components.

Shown by the experiment results, the machine line current ripples are increasing at all switching frequencies by interleaving technique. It is undesirable to have this negative effect caused by interleaving. However, compare to the 5 A fundamental current, the amplitude of these current ripples are below 1%. They are negligible and have no adverse effect on the machine operation.

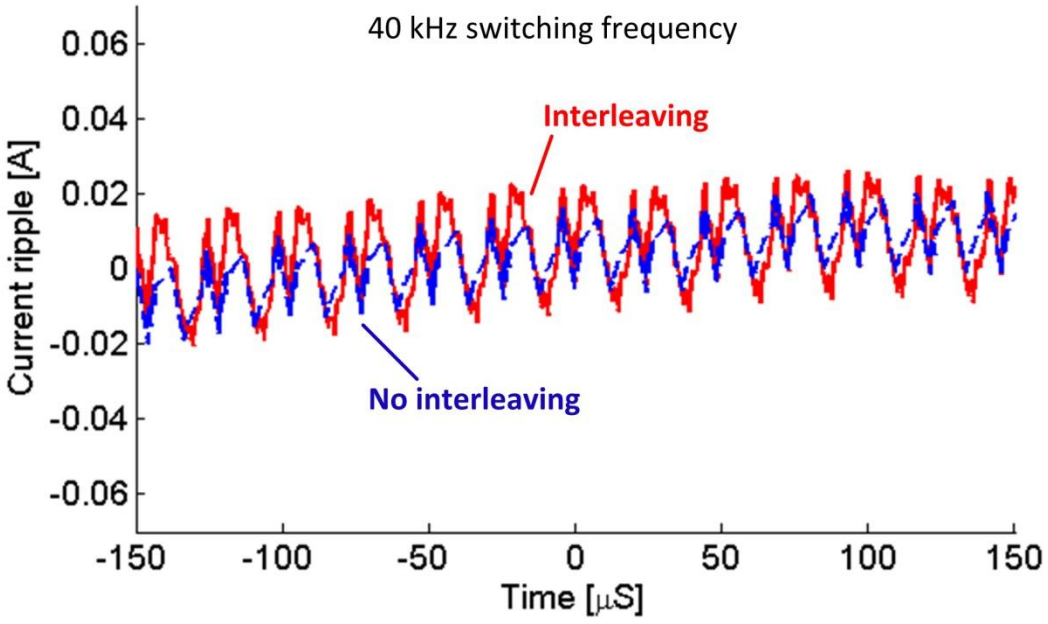
The experiment results also clearly verify the machine equivalent transformer model introduced in Chapter 2, because there is no other reason that explains interleaving can increase the current ripples.


10 kHz switching frequency
No interleaving
Interleaving
Current ripple [A]
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-150
-100
-50
0
50
100
150
Time [μS]

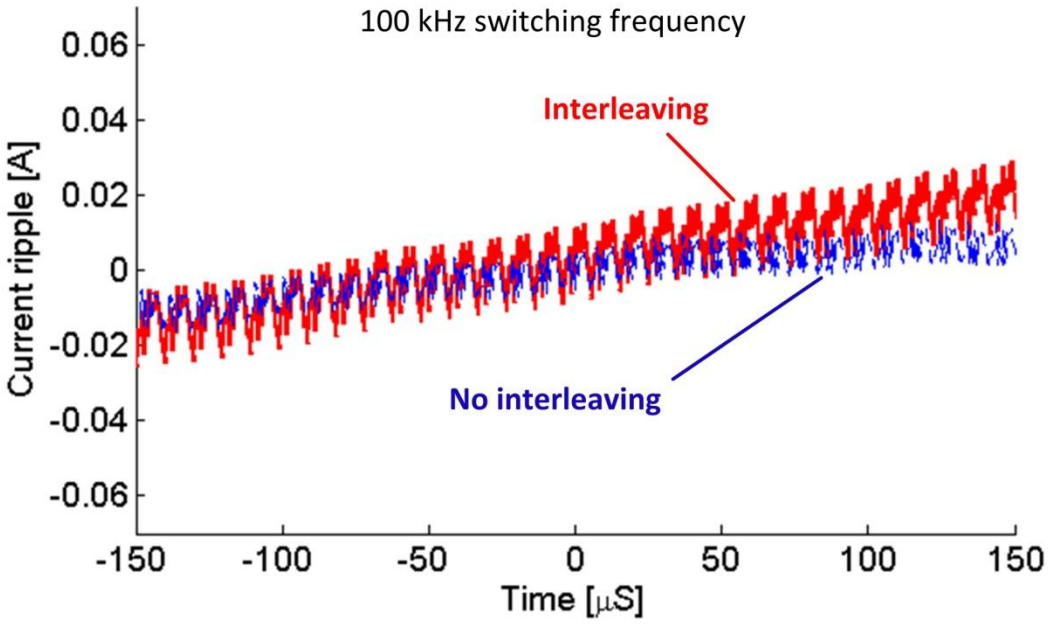
(a)


20 kHz switching frequency
No interleaving
Interleaving
Current ripple [A]
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-150
-100
-50
0
50
100
150
Time [μS]

(b)



(c)



(d)

Fig. 5.14. Experiment results: switching current ripples with and without interleaving at different switching frequencies (a) 10 kHz, (b) 20 kHz, (c) 40 kHz, and (d) 100 kHz

5.5.3 Machine Segments in Same Slots

Machine segments in same slots will have parasitic capacitance between them. Any voltage mismatch between the machine segments will cause a large machine line current ripple. Hence interleaving technique is not recommended to implement in this case.

However, with the aim of extra LC filters, as discussed in section 3.4.2, it is possible to apply interleaving technique. The LC filters must be able to suppress the current ripples at switching frequency. In this case, tradeoff is involved between the extra cost/size of LC filter and the benefit from interleaving technique. Generally speaking, at high power rating, DC-link capacitors are very large. It is desirable to apply interleaving to reduce DC-link capacitors by sacrificing extra cost of LC filters. By comparison, at low power rating, filter inductors are typically very large. It is better not to use interleaving technique to avoid the extra cost of LC filters.

5.6 Summary

In this chapter, gate signal interleaving technique is discussed. It is effective in reducing DC-link voltage ripples, as proved by both simulation and experiment results. DC-link capacitors can be reduced if the DC-link voltage ripples are maintained.

Interleaving technique is compared between series-connect and parallel-connect structures. Interleaving for parallel-connect structure is effective in reducing DC-link capacitor current at low frequency. At high frequency, due to the limit of parasitic inductance, interleaving technique is no longer effective. By comparison, interleaving for series-connect structure is a duality form

of conventional interleaving for buck converters. It is effective in reducing DC-link voltage ripples at all simulated frequencies.

Common-mode voltage of the machine drive is also reduced by interleaving technique. The machine is benefit from lower common-mode voltage, because ground current and bearing current can be reduced.

The only undesirable effect of interleaving is the machine line current ripple is increasing if machine segments are in the same pole-pair. However, as shown by the experiment results, it is not a problem because the machine line current ripple is still negligible even when interleaving technique is applied. The small increase in machine line current ripple will not affect the machine operation.

Chapter 6

Prototype Design and Experiment Results

To validate the proposed multilevel concept, a prototype multilevel machine drive with 4 series-connect modules is built. The prototype supplies a 4-segment induction machine with rewound windings. The experiment results show that the voltages are shared equally among all converter modules, even without any active control. This prototype experiment demonstrates the capability of the proposed machine drive to control the machine using a conventional Indirect Field Oriented Control (IFOC) algorithm.

The proposed structure is simple and stable, and every easy to increase the number of modules. Even with only 4 modules, it is possible to extend the operating voltage to medium voltage range by using standard 3-phase converter modules with 1.2 kV MOSFETs/IGBTs.

6.1 Test bench setup

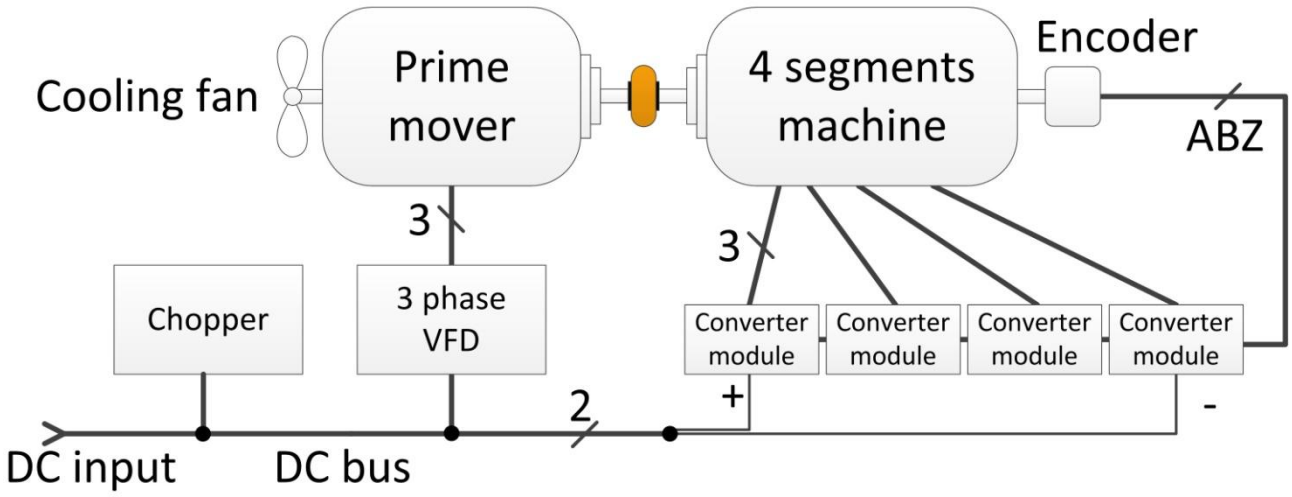


Fig. 6.1. Machine test bench setup

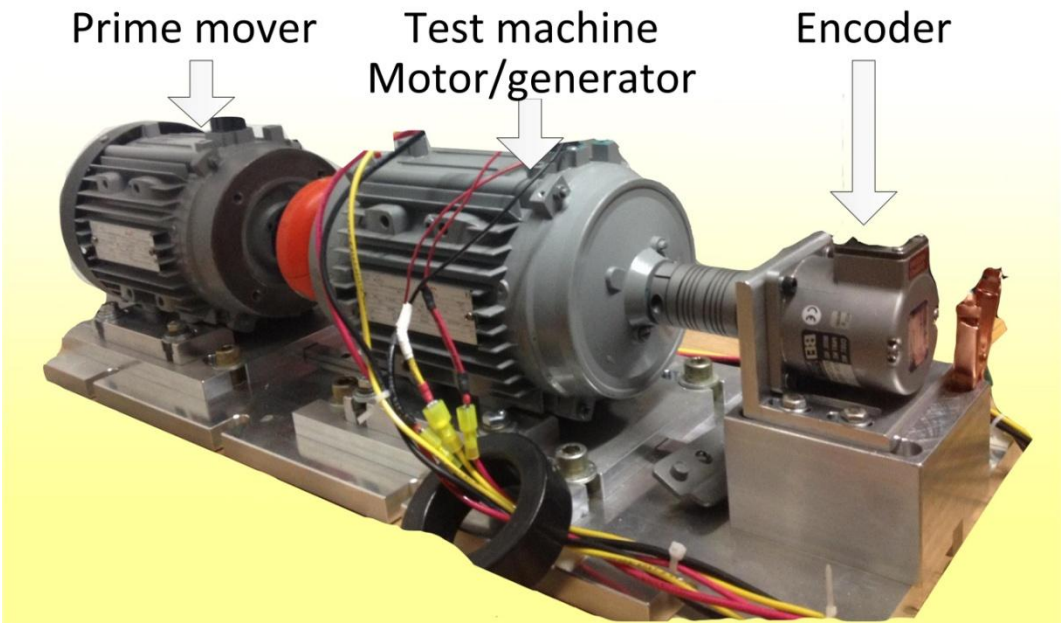


Fig. 6.2. Photo of machine test bench setup

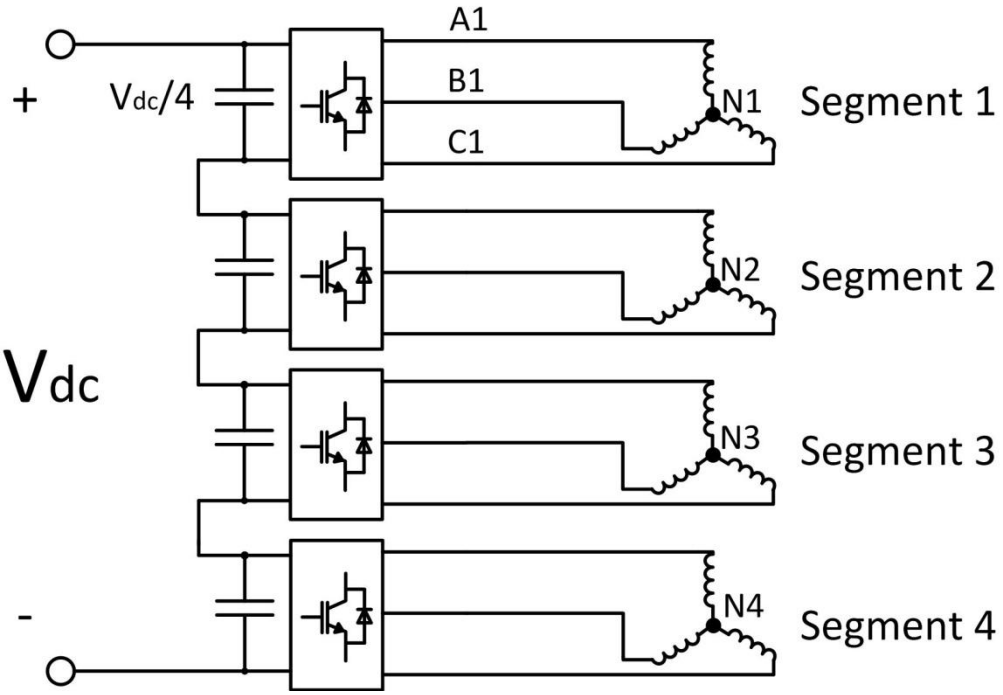


Fig. 6.3. Schematic of the 4-module multilevel converter

The test bench is equipped with two identical commercial induction machines. The induction machine is 1.5 kW, 4-pole, FCM315 machine from Danfoss [124]. One of the induction machines is serving as the prime mover providing the shaft speed. It is supplied by a conventional 3-phase variable frequency drive (VFD) with open loop V/f control.

The other machine is the test machine providing either negative (generating) or positive (motoring) torque. The test machine is rewound into 4 segments without any difficulty. The coils inside the machine slots are exactly the same. Only the end windings of the machine are altered/removed.

A 4096-line optic encoder with A-B-Z quadratic encoder interface is used in the test to provide position and speed measurements. A DC-link chopper is installed in the test to prevent

the DC-link voltage from being too high. The chopper can either operate automatically when the voltage exceeds the programmed limit, or operate manually by a switch button.

6.2 Hardware Design

6.2.1 Design of 4-Segment Machine

The 1.5 kW, 4-pole induction machine for test has 36 slots. There are 3 slots per pole per phase. Two machine pole-pairs are originally connected by end windings, as shown in **Fig. 6.4**.

The machine is proposed to split into 4 segments, and **Fig. 6.4** shows the phase A windings. A1 and A2 are located in the same slots and same pole pair. As discussed in previous chapters, these two segments form into an equivalent transformer and they exhibit exactly identical properties. A3 and A4 are also in the same slots and same pole pair.

The A1/A2 segments and A3/A4 segments are located in different pole pairs. As a result, they are magnetic decoupled.

Number of poles	4
Motor # slots	36
Stator resistance [Ω]	4.2
Rotor resistance [Ω]	4.0
Stator/rotor leakage inductance [mH]	23
Magnetizing inductance [mH]	378
Rated slip frequency [Hz]	1.9

Table 6.1. Original machine parameters

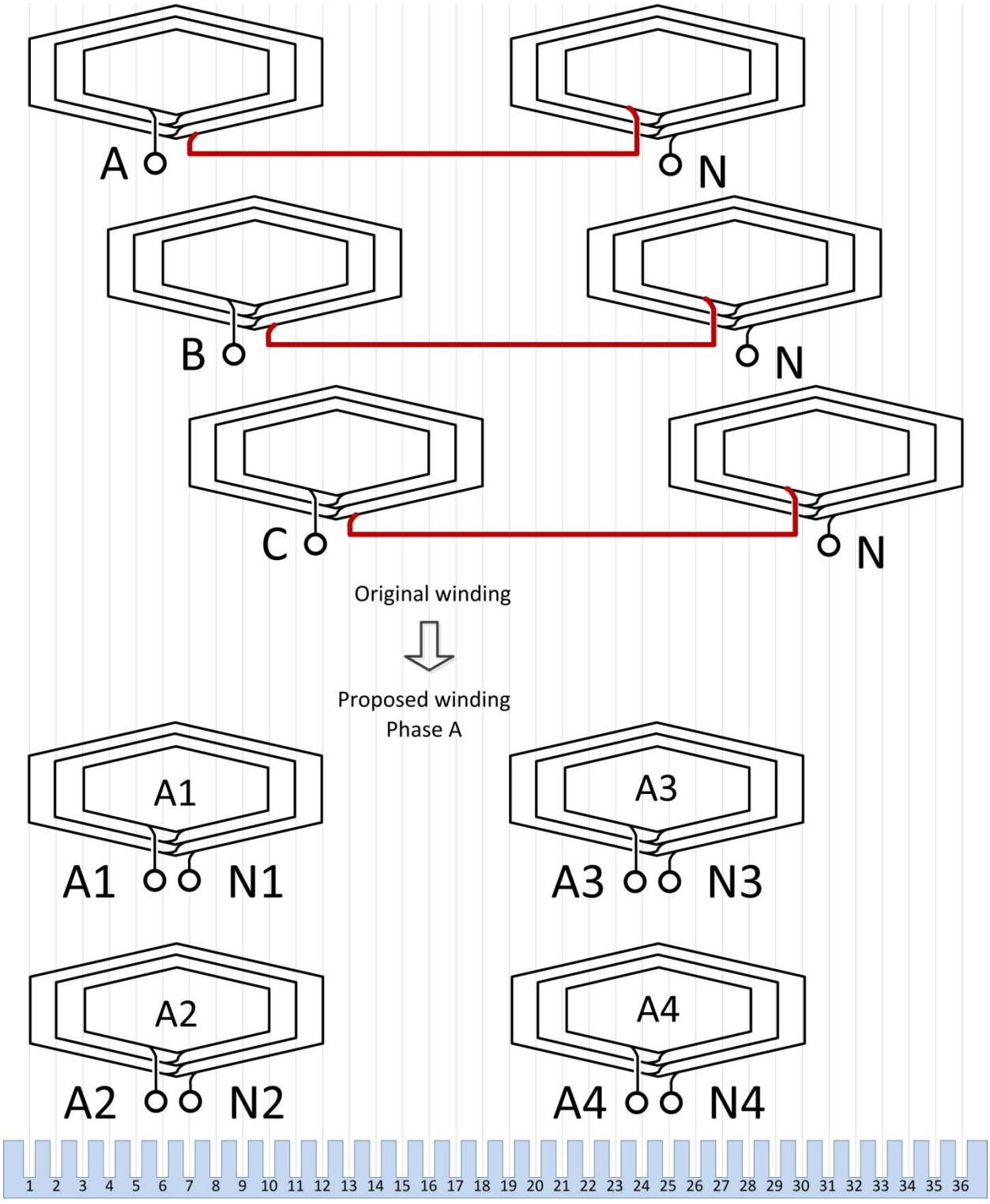
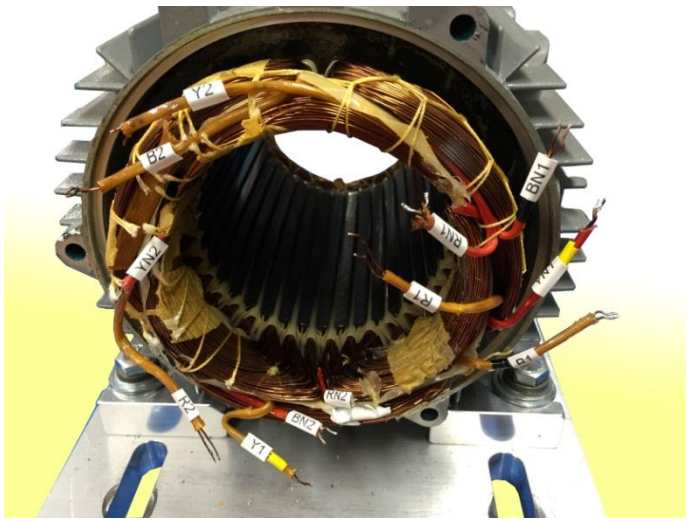


Fig. 6.4. Proposed Phase A winding configuration of the test machine



(a)

(b)

Fig. 6.5. Photos of the test machine

Each machine segment consists of three concentric coils and can be further split. It is possible to split the machine into 2, 6 or 12 modules, without changing any coil inside the machine slots. Moreover, if the machine coils are allowed to rewound, it is possible to get any number of desired segments.

6.2.2 Design of LC Filters

Since A1 and A2 segments are located in exactly the same slots, they will form a parasitic capacitance between them. Extra LC filters are recommended in this thesis to deal with the mismatch of PWM signals from A1 and A2, as discussed in section 3.4.2.

The parasitic capacitance C_{in} of the machine is measured using an impedance analyzer. The test setup is shows in **Fig. 6.6**.

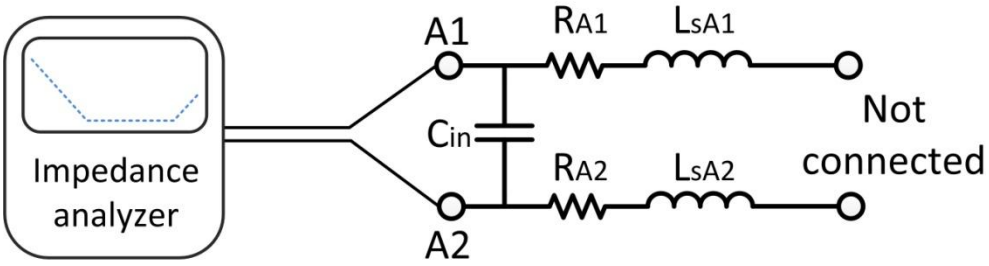
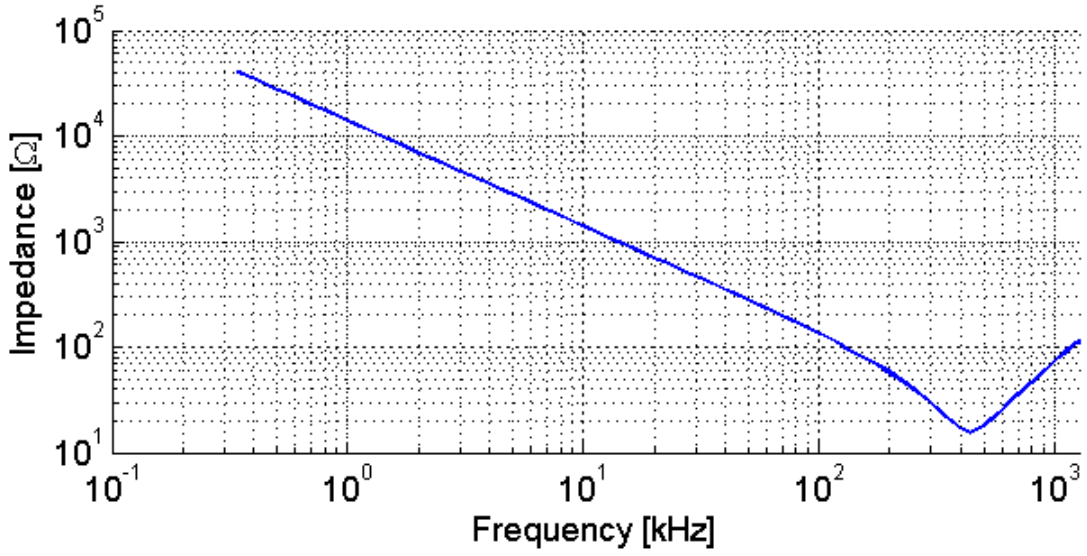
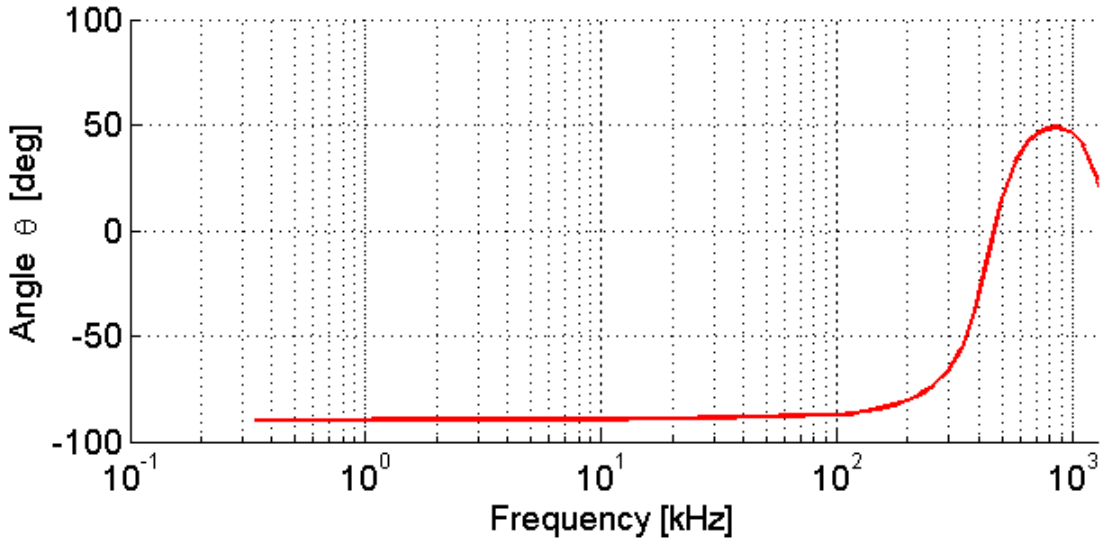


Fig. 6.6. Test setup for measuring parasitic capacitance

According to the measurement results from impedance analyzer, the impedance between A1 and A2 terminals is pure capacitive up to 100 kHz. The parasitic capacitance C_{in} is calculated to be 11.4 nF. The lowest impedance is identified at 420 kHz.



(a)



(b)

Fig. 6.7. Impedance measurement result of parasitic capacitance

(a) impedance measurement, and (b) angle measurement

Fig. 6.8 shows the circuit of recommended LC filters. Two independent filters are connected between A1/A2, A3/A4. No filter is needed between A1 and A3 because they are located in different pole-pairs. Similarly, LC filters are installed for phase B and phase C.

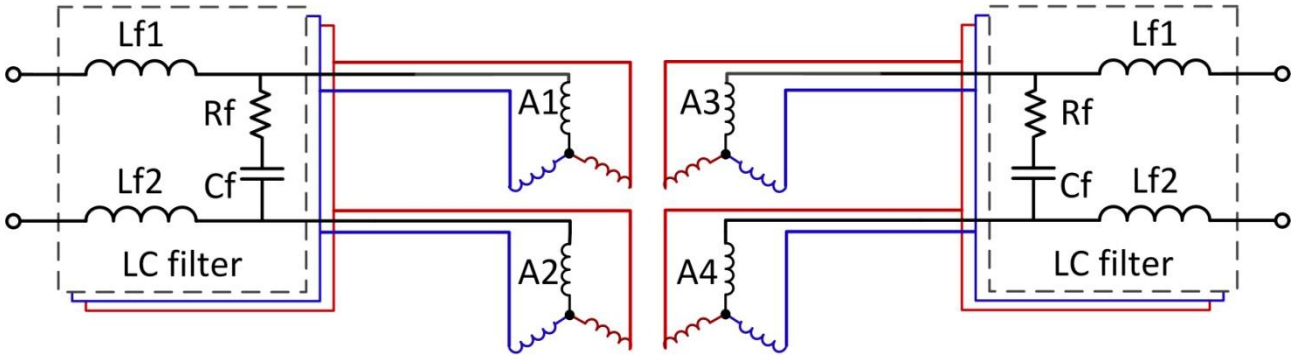


Fig. 6.8. Design of LC filters for PWM mismatch

The purpose of the LC filter is to prevent current spikes during PWM mismatch. According to the MOSFETs and gate drivers of the converter modules, the PWM mismatch between modules is up to 8 ns. Hence, a LC filter with 1 μH and 1μF (providing a 1μs bandwidth) is enough for filtering the PWM mismatch. In the hardware design, LC filter is intentionally over-designed to give greater test flexibility. A damping resistor R_f is connected in series with the capacitor C_f. When PWM mismatch occurs, R_f provides strong damping to the circuit. When there is no PWM mismatch, the loss of R_f is 0. The numerical values of LC filter are shown in **Table 6.2**. Although the LC filter is over-designed, the size of it is still very small.

Component	L_f	C_f	R_f
Value	33.0 [μ H]	1.0 [μ F]	1.0 [Ω]

Table 6.2. LC filter parameters

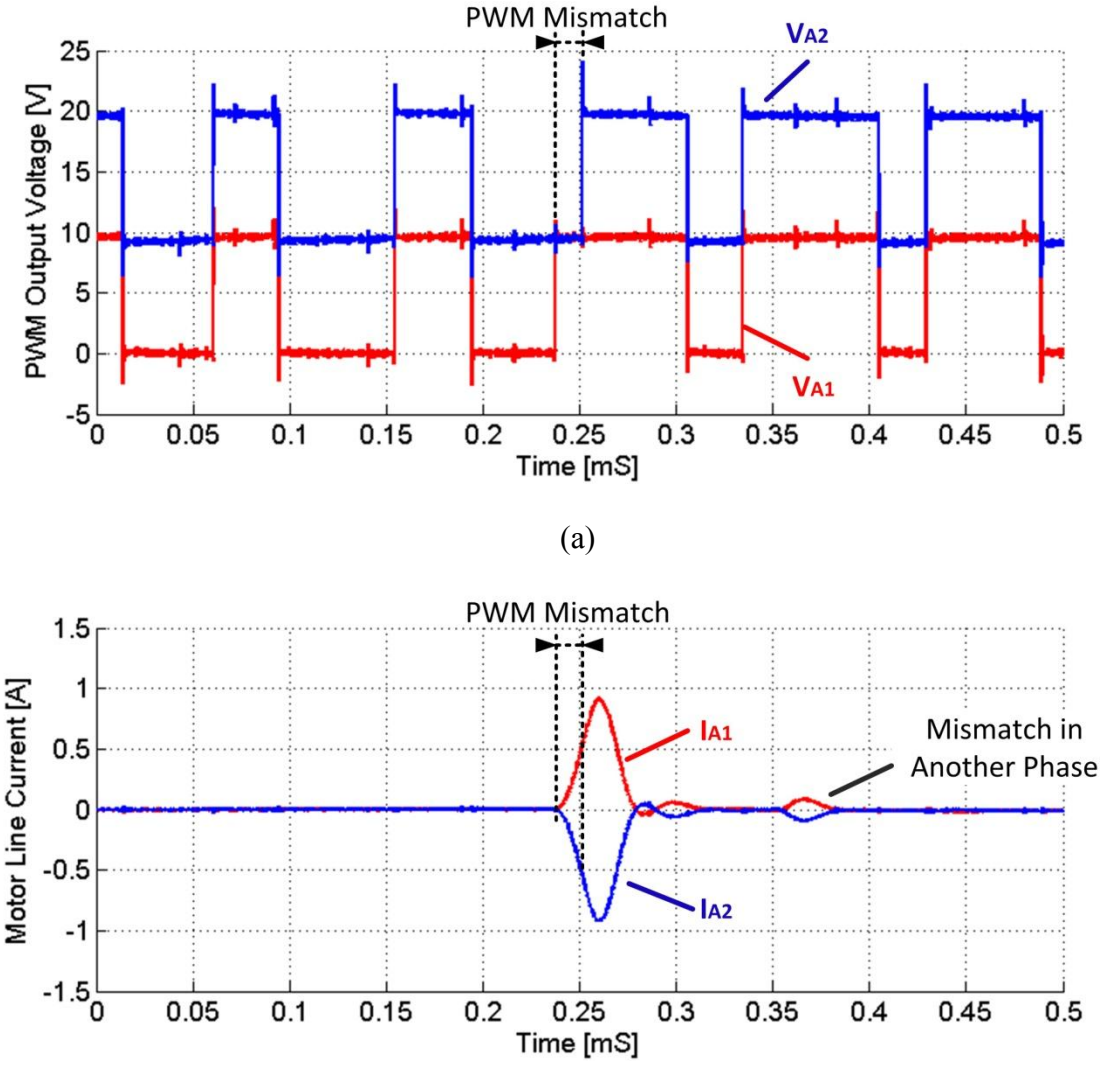


Fig. 6.9. Experiment results of LC filter

(a) voltage mismatch disturbance, and (b) current response

Fig. 6.9 presents the experiment results to test the performance of LC filter. In the test, an PWM mismatch with 10 μs is injected as a disturbance. This PWM mismatch generates a higher voltage on A1. Consequently, a positive current response is observed on A1. The current response on A2 is complementary, because this is the returning loop of the current response.

Notice that the 10 μs disturbance in the experiment is ridiculously large. The proposed small LC filter can properly limit and damp the current response as expected. If the switching frequency were higher, for example, 100 kHz, this LC filter would be enough for applying interleaving technique.

6.2.3 Design of Converter Modules

Several photos of the converter design are shown in this section. There are 12 pieces of single-phase bridges combining into a total of 4 converter modules. A dual-DSP control board is designed for controlling this prototype converter. All these assemble parts, along with two 12 V BLDC cooling fans, are connected to the mother board.

The single-phase bridge with GaN FETs is the key part for power conversion. It consists of two EPC2001C eGaN FETs from EPC, a bridge gate driver LM5113 from TI and two hardware deadtime generators. The GaN FETs are rating at 100 V and 36 A continuous current. Due to cooling limit of the GaN FETs, the single-phase bridge in this thesis can operate at 25 A current. As a result, the converter with 4 modules connected in series is capable of a 400 V maximum voltage and 25 A continuous current. More design considerations of GaN power converter will be covered in next chapter.

The microcontrollers used in this prototype are dsPIC33EP512GM710 from Microchip Tech. Inc. This DSP is 16-bit fix-point with hardware 16-bit*16-bit multiplier and 32-bit/16bit divider.

Each DSP is equipped with 6 PWM generators (12 channels), 2 I2C, 3 SPI and 2 ADC modules. The communication between two DSPs is achieved by two I2Cs, one SPI and 8 parallel ports. For debugging and monitoring, the DSP can also drive a LCD display screen via SPI.

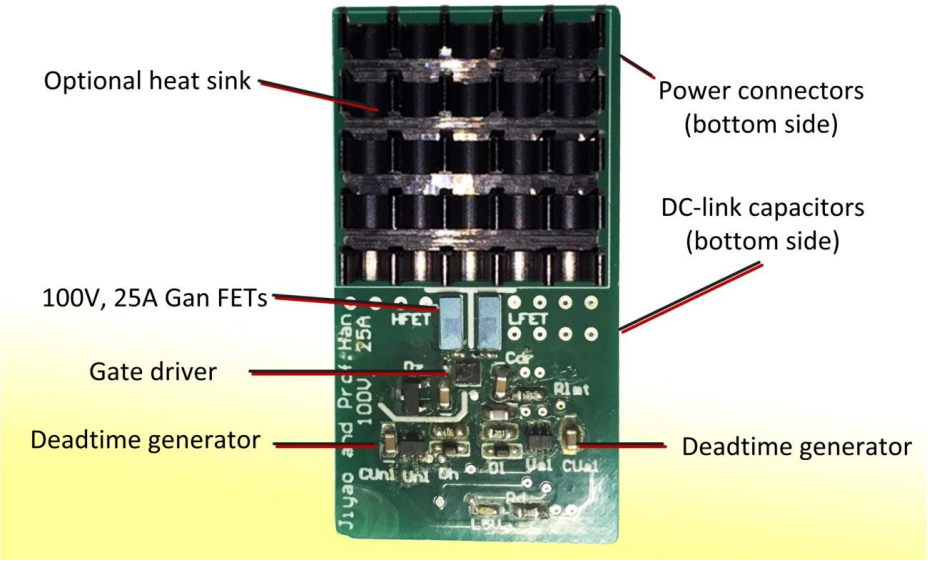


Fig. 6.10. Design of single-phase half-bridge with GaN FETs

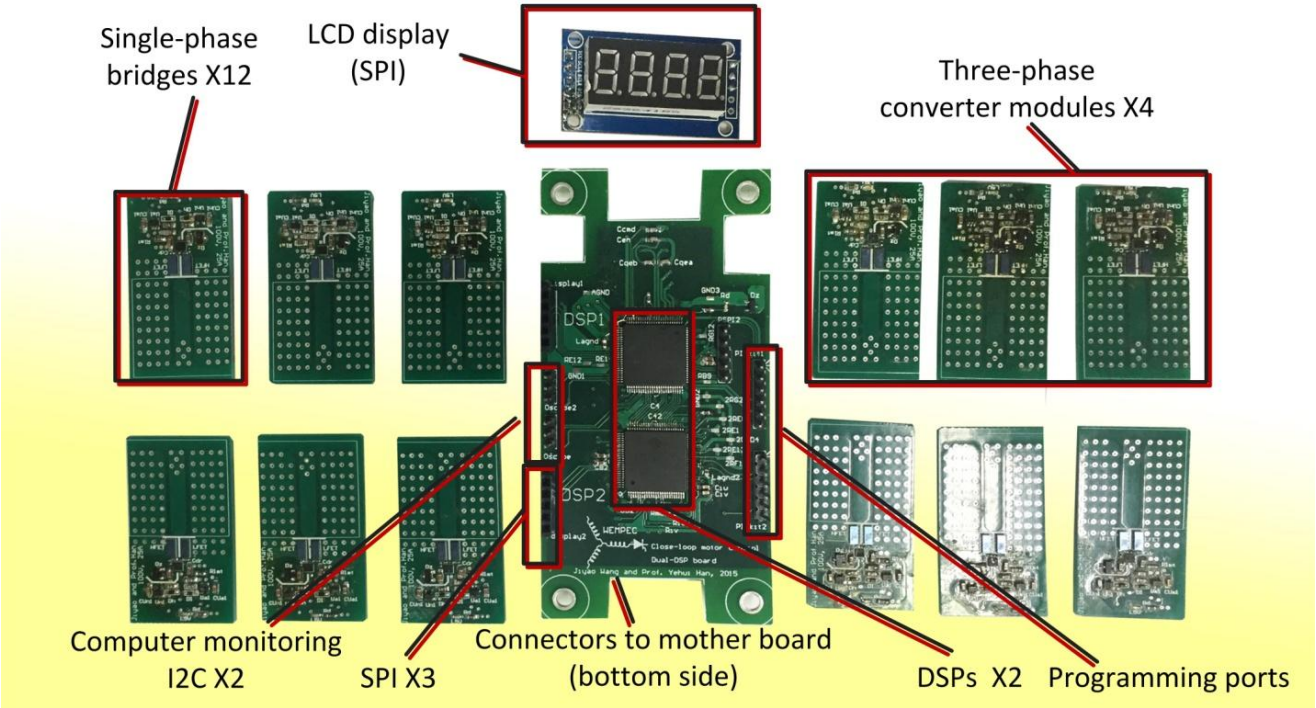


Fig. 6.11. Design of all assemble parts

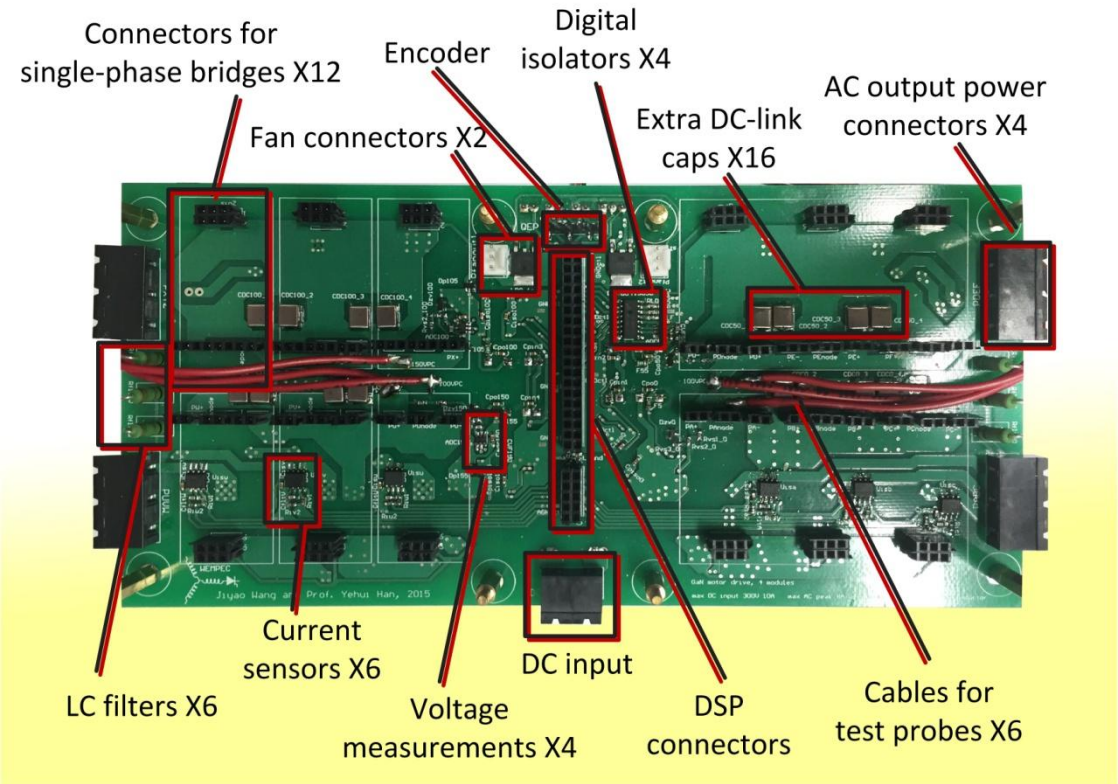


Fig. 6.12. Design of the mother board

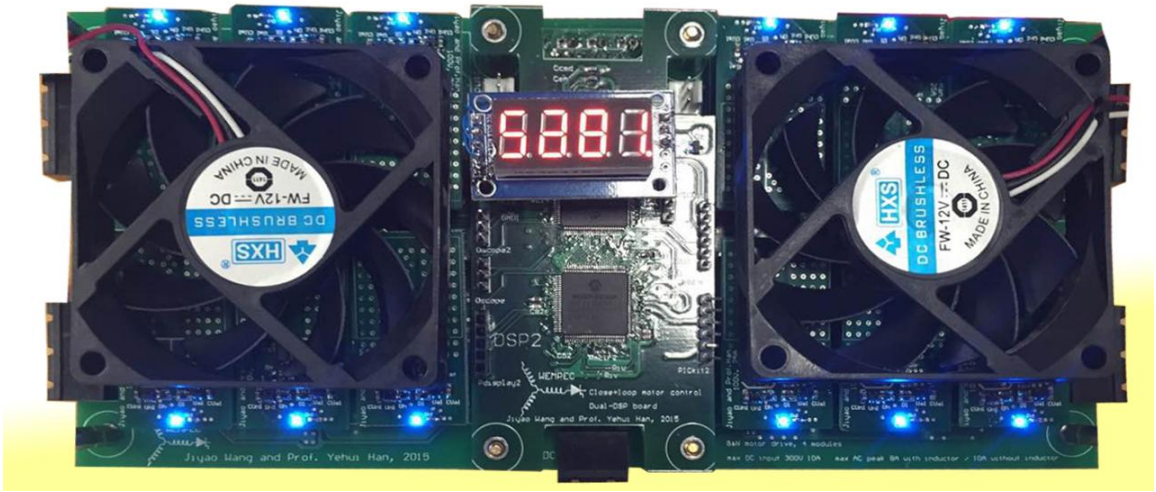


Fig. 6.13. Photo of the 4-module converter with all parts assembled

6.2.4 Converter Control Diagram

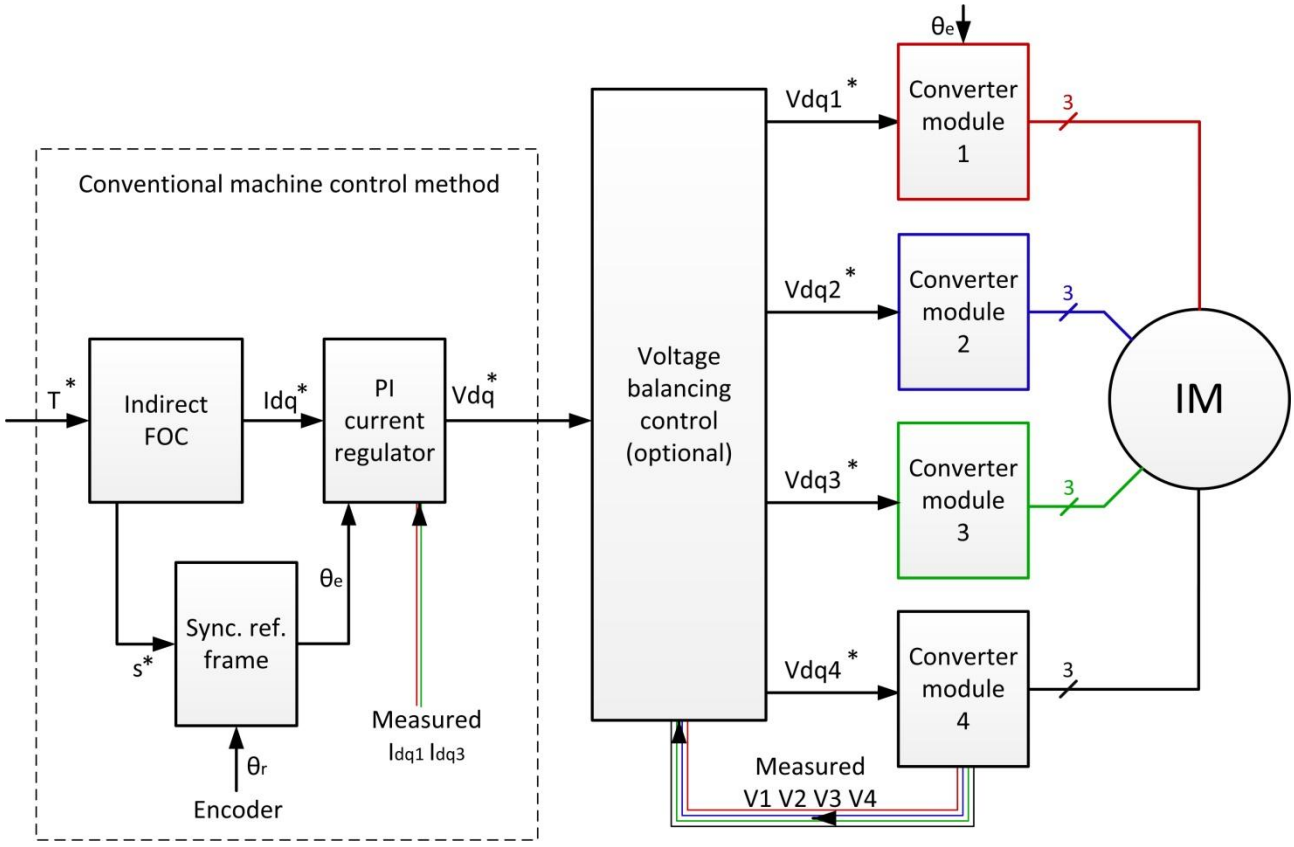


Fig. 6.14. Simplified converter control diagram

The torque of the induction machine is controlled by conventional indirect field oriented control (IFOC). PI current regulators will control the machine current in close-loop. The rotor speed is measured by the encoder. IFOC treats the machine as one piece, just like in a conventional motor drive. Nothing needs to be changed when applying the machine control method to the prototype.

In the experiment, the converter module voltages are controlled by either 'common-duty-ratio' or CVB methods. The voltage balancing control will not affect the machine control (IFOC in the prototype) at all.

6.3 Experiment Results

In the experiment, the prime mover is spinning at an almost constant speed by VFD. The torque of the test machine will be regulated by the prototype converter, which is connected to a 200 V DC-link. During the torque/current transient, module voltages will be monitored and recorded. The expected module voltage is a quarter of 200 V, i.e. 50 V.

At first, the prototype converter is controlling both the flux and torque of the test machine to be zero, i.e., Id = 0 and Iq = 0.

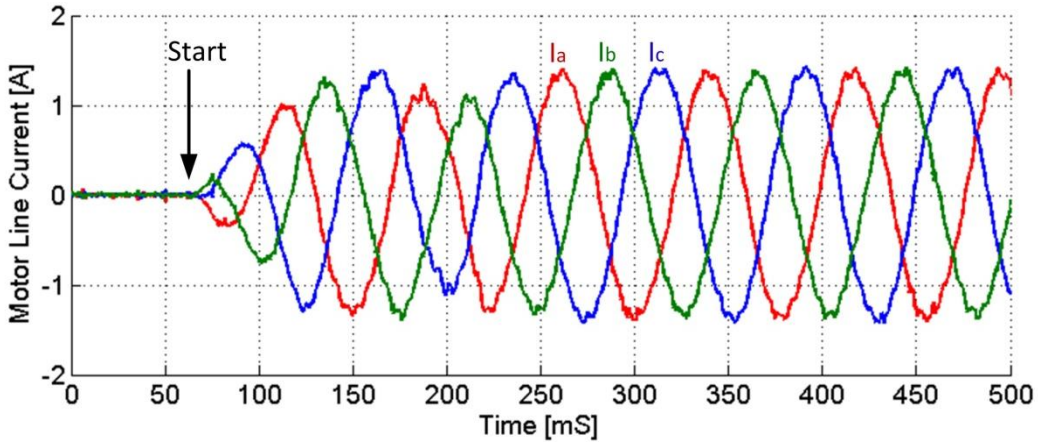
Then, a user command will trigger the prototype converter to control both the flux and torque to be one per unit, i.e., Id = 1.0 p.u. and Iq = 1.0 p.u. The three-phase machine line currents from one module, along with the voltage on four modules are measured and shown in **Fig. 6.15**. The voltage is not controlled in the experiment.

Fig. 6.15(a) shows the sinusoidal three-phase currents and the amplitude is 1.0 p.u. as expected. The currents show the IFOC machine control is working properly. **Fig. 6.15(b)** shows the module voltages are balanced and stay at 50 V during the current transient. This result validates the series-connect converter modules can balance voltage without any control. It proves the concept of this thesis. **Fig. 6.15(c)** illustrates the zoon-in voltage ripples from 4 modules. There exists a 3 V difference between the modules. This is because of the asymmetry of the

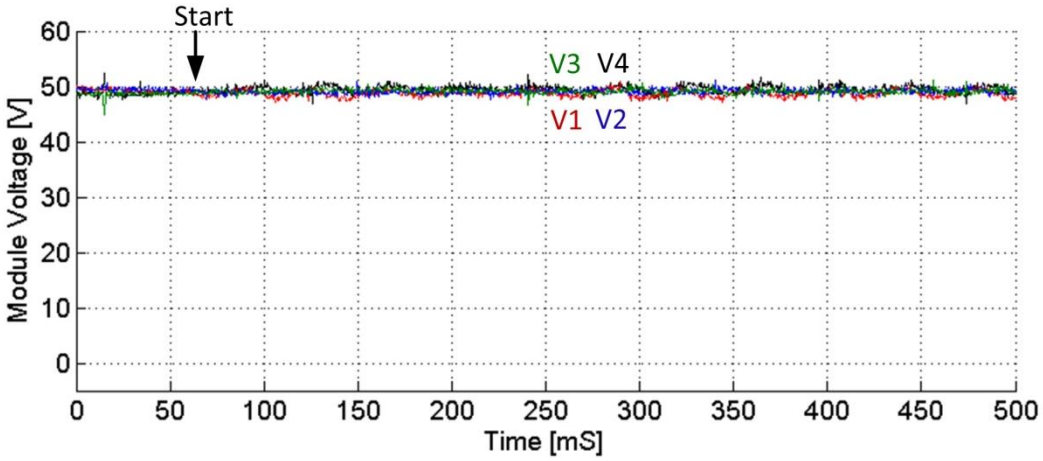
machine and converter modules. Since the machine segments 1 and 2 are coupled, their voltages tend to stay identical. The same rule applies for segments 3 and 4.

Although module voltages are not controlled at all, they have very small differences, meaning the modules can naturally balance their voltages. And of course, the voltage differences can be controlled. As shown in next chapter, the voltage differences can be further suppressed by active control methods.

Fig. 6.16 shows the experiment results for three-phase currents suddenly jumping to zero. The module voltages are naturally balanced at 50 V during this transient. Similarly to previous experiment results, V1 and V2 tend to stay together because they are strongly coupled. There is a voltage difference between V1/V2 and V3/V4. This is due to machine segments asymmetry. When the currents of machine become zero, all converter modules will provide zero power. The machine asymmetry in such condition will no longer affect the module voltages. There will be no module voltage difference when the machine currents are zero. As shown in the **Fig. 6.16**(c), only switching ripples are left.



(a)



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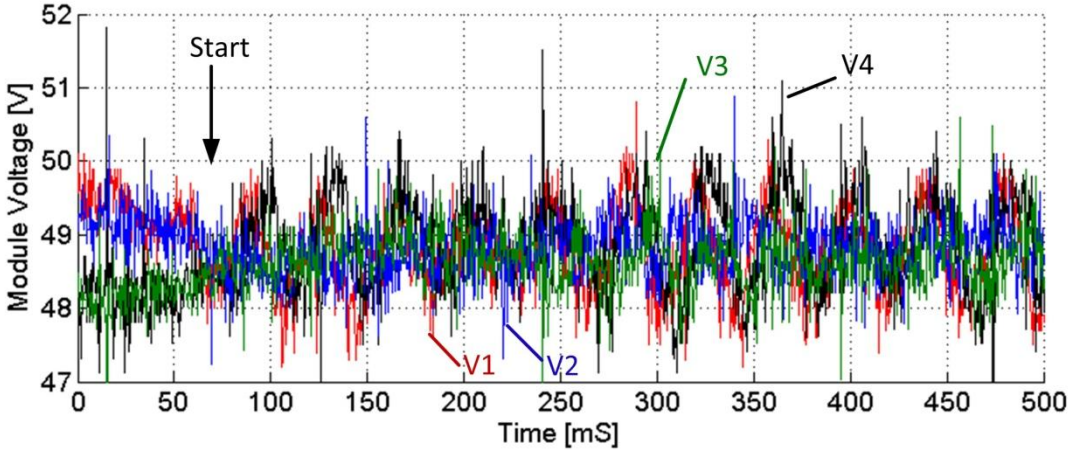
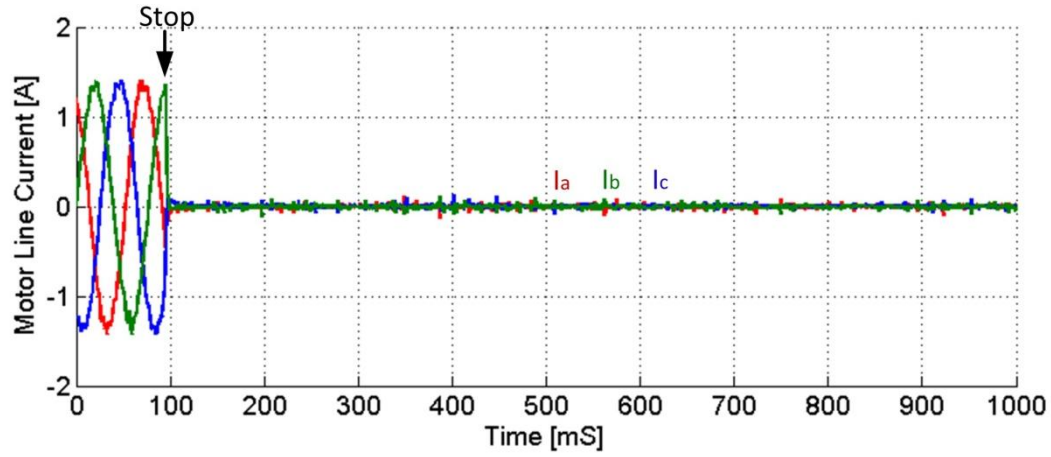
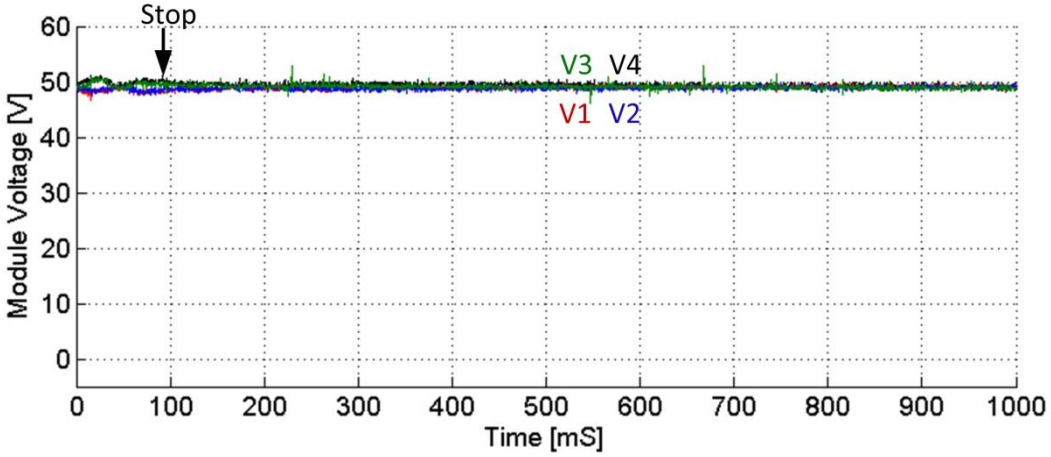


(c)

Fig. 6.15. Experiment results: voltage balancing during 0-100% current transient (a) three-phase currents, (b) module voltages, and (c) zoon-in module voltages



(a)



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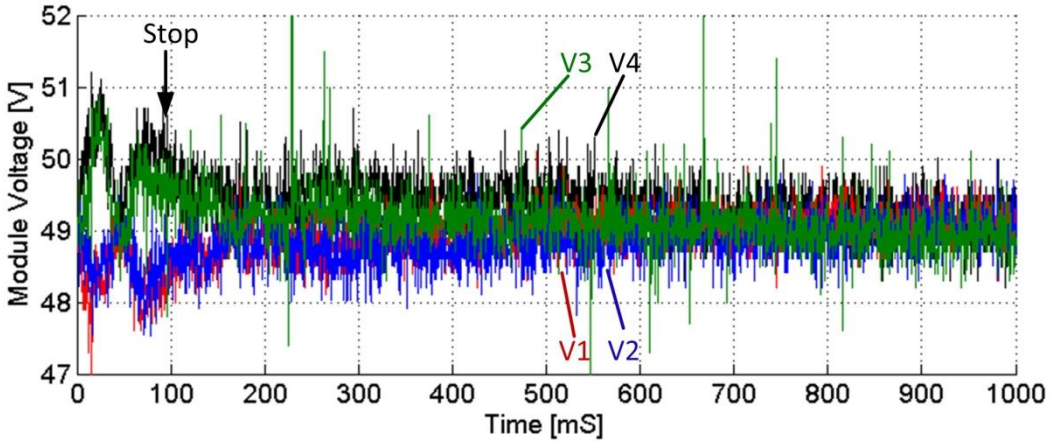


(c)

Fig. 6.16. Experiment results: voltage balancing during 100-0% current transient

(a) three-phase currents, (b) module voltages, and (c) zoon-in module voltages

6.4 Summary

This chapter shows the design and experiment results of a 4-module machine drive system with proposed multilevel structure. The proposed structure enjoys standard modular design and easy to extend number of voltage levels.

The prototype converter validates the multilevel concept proposed in this thesis. The machine can be easily split into 4 segments by removing the original ending windings, without changing the machine design at all. Machine currents can be properly controlled in close-loop via conventional IFOC. Module voltages are naturally balanced with very small ripples due to machine asymmetry. The experiment also demonstrates and proves the concept of two different voltage balancing mechanisms introduced in previous chapters: 1) passive voltage balancing (common-duty-ratio method) for segments in different pole-pairs, and 2) voltage balancing for strongly coupling segments in same slots.

Chapter 7

GaN IMMD Design Considerations

This thesis proposes the input-series multilevel topology to realize an IMMD. The proposed topology can reduce the module voltages and utilize low-voltage GaN devices to improve IMMD efficiency. The heights and sizes of DC-link capacitors are optimized as a function of switching frequency. The heat sinks of IMMD are reduced or eliminated because WBG semiconductors are used. All the concepts and techniques introduced in previous chapters are implemented to build an IMMD. However, there are still many practical challenges in realizing such a compact system. In this chapter, converter design considerations are presented to deal with the challenges.

7.1 The Structure of IMMD

In this research, total 4 generations IMMDs have been built, as shown in **Fig. 7.1**. The first generation IMMD utilizes Si devices that switch at 10 kHz. As a result, the sizes of capacitors are relatively large. But compare to a conventional motor drive, this generation reaches very low profile at 1.2 inches, which is mainly decided by the capacitors. The three phase converter module is realized in a single PCB design. Similar to the first generation, the second generation IMMD also has a three phase module design, but uses GaN devices switch at 50 kHz to reach a higher power density. Moreover, three current sensors are added to the PCB design. As the PCB gets smaller, the routing of PCB traces becomes very difficult to realize a circular shape design and meanwhile maintain low parasitic inductances.

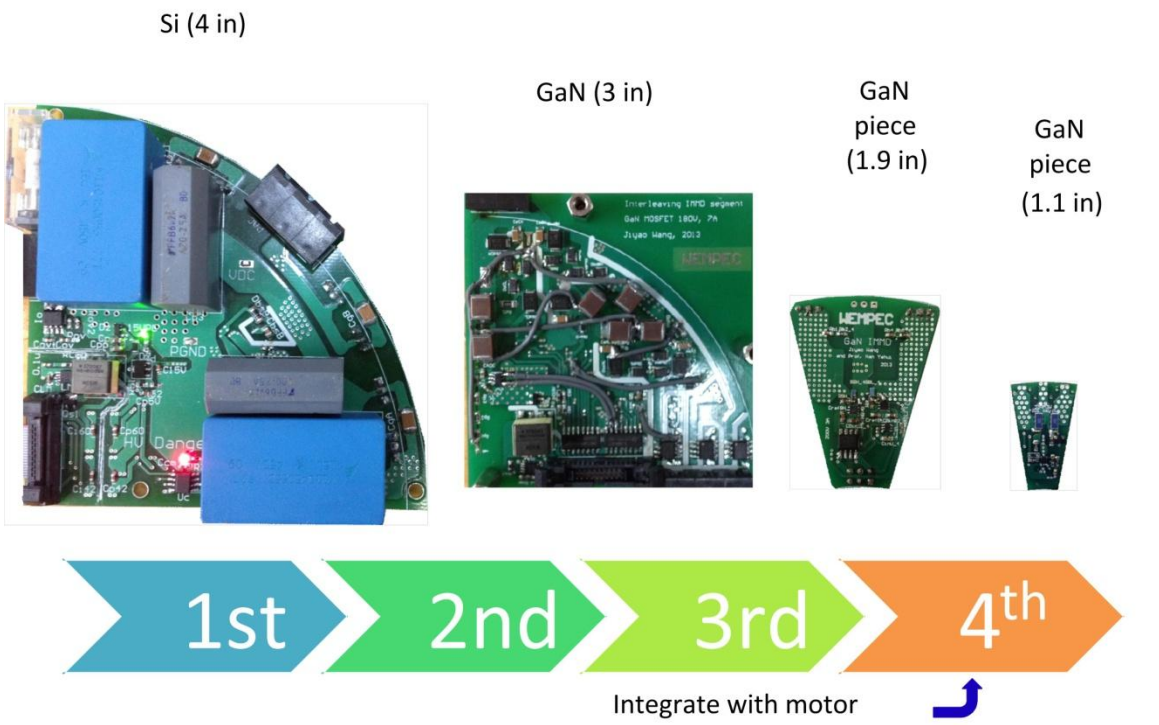


Fig. 7.1. Four generations of IMMD PCB design

The fundamental building block of the first and second generations is three phase converter modules. In the third generation, however, a single phase converter piece becomes the fundamental building block. Three such pieces will combine into a three phase converter. By using the single phase pieces, the converter design will have better consistency in the aspects of parasitic inductance, switching performance and heat dissipation. It is also easier to realize a circular shape in order to integrate with the motor. In the third generation, a large PCB area is simply occupied by copper planes and vias for heat dissipation.

In the fourth generation, parasitic inductance is minimized so the switching performance of GaN devices is good enough to realize a 100 kHz switching frequency with very small switching loss. The GaN devices are more efficient so the area of PCB design is greatly reduced. The

overall height of this single phase piece is 1/4 inch, which is again, mainly decided by the DC-link capacitors.

Based on single phase piece building block, the proposed IMMD structure is shown in the following figure.

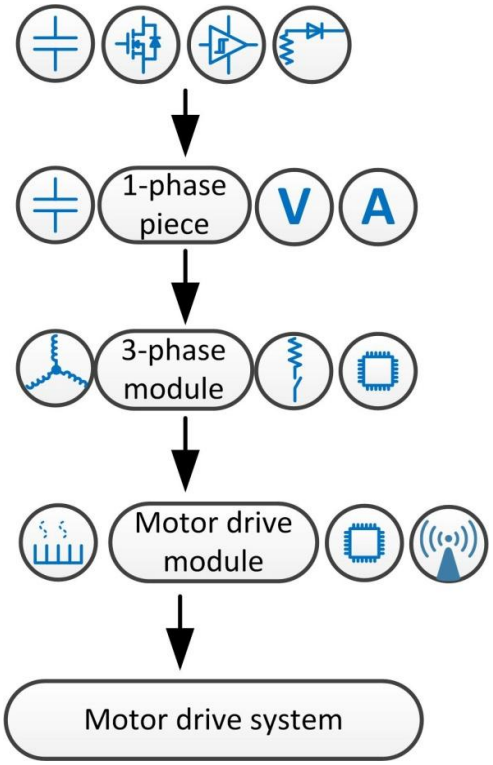


Fig. 7.2. The structure of IMMD

- **Level 1: a single phase converter piece** consists of DC-link capacitors, power switches, gate drives and over-current protections.
- **Level 2: a three phase converter module** consists of 3 single phase pieces, extra DC-link capacitors as well as voltage and current sensors.
- **Level 3: a motor drive module** consists of a three phase converter module, a three phase

motor winding segment, an optional distributed digital controller and optional breaking choppers.

- **Level 4: a motor drive system** consists of several motor drive modules, an optional central digital controller, optional heatsinks and optional communication units (wireless preferred).

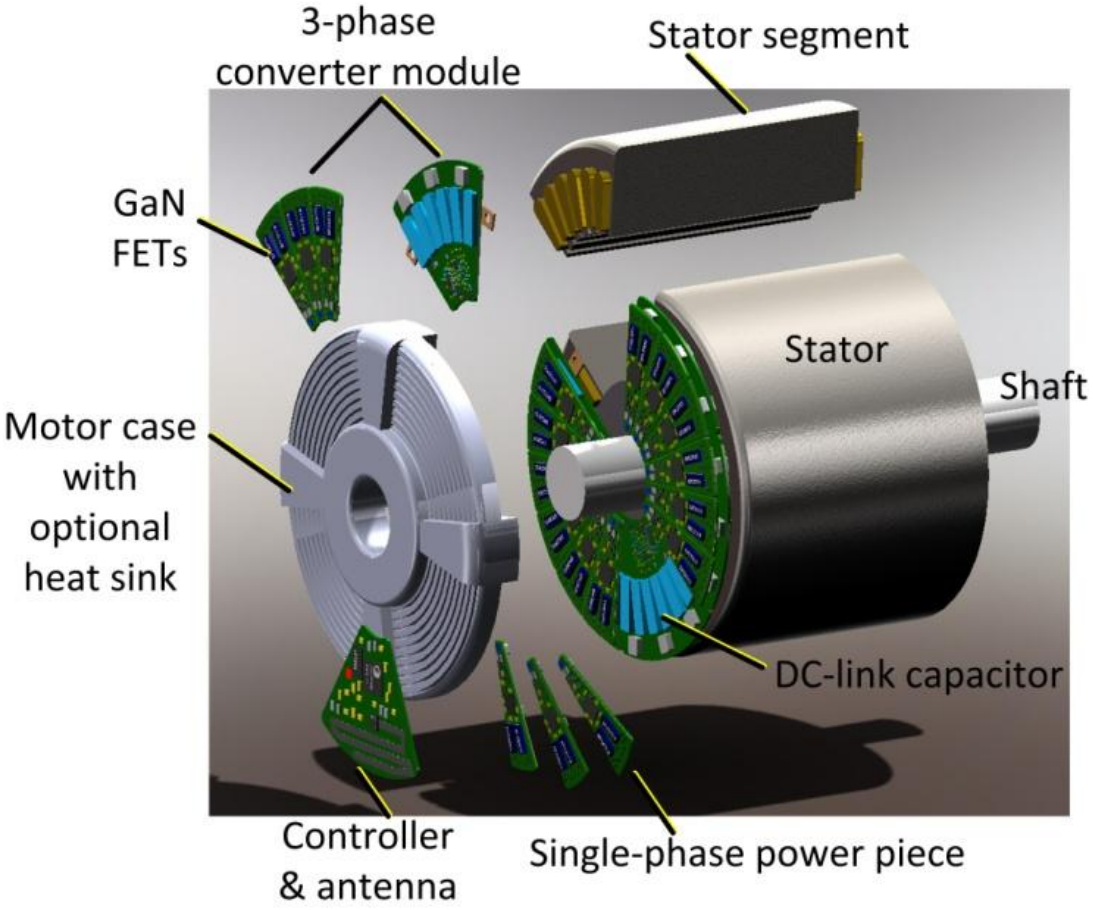


Fig. 7.3. Illustration of IMMD

With this arrangement, the proposed IMMD system is illustrated by **Fig. 7.3**. The single phase power pieces are placed in a circular pattern to match the motor shape. Module voltage can be selected in order to use GaN FETs and capacitors with low profile. The controller and wireless communication units are also integrated inside the IMMD. The motor drive has access to the voltage and current of each machine winding, enabling detection of machine faults quickly and

accurately through the measurements. Optional local digital controllers, though not shown in the figure, can provide better performance. The cost of these extra digital controllers is negligible for high power applications.

The thermal management of IMMD has been addressed in [62]. It is possible to utilize the rotor as a fan to create air flow to cool both the machine and the drive. For relatively low power rating, **Fig. 7.3** shows the GaN FETs facing outside of machine housing and the DC-link capacitors facing inside the machine housing. In this way, the DC-link capacitor can be easily cooled by the rotor air flow, and the GaN FETs can be cooled by motor case. Alternatively, the GaN FETs can be installed facing the machine inside. In this way, the GAN FETs can be cooled by the same heatsinks as the machine. The design for thermal management has never been easy. It will depend on the power rating, efficiency and operating temperature, which may vary case by case.

7.2 Design of GaN Single Phase Pieces

7.2.1 Comparison of Wide Bandgap Semiconductor Devices

As introduced in Chapter 1, Si MOSFETs are typically below 600V and will have very undesired performance at 1200V. Commercialized SiC MOSFETs are mostly 600V, 1200V and 1700V. Commercialized normally-off GaN FETs are below 600V range. To make a fair comparison, the voltage is set at 650V, a voltage level where commercialized Si, SiC and GaN products are all available. The following table shows the comparison of different 650V devices.

	CoolMOS Si	SiC	GaN
Manufacture	Infineon	Rohm	GaN Systems
Manufacture #	IPA60R125	SCT2120	GS66504
Rds(on)@25°C [Ω]	0.125	0.12	0.11
Recommended gate voltage [V]	10	18	7
Input cap. [pF]	2500	1200	130
Output cap. @ 400 V [pF]	90	90	32
Body diode forward voltage [V]	1.2	4.3	2
Body diode reverse recovery time [ns]	430	33	0
Body diode reverse recovery charge [nC]	9000	53	0

Table 7.1. Comparison between 650V Si, SiC and GaN devices

From the table it is clear that SiC and GaN have smaller input capacitance, output capacitance and much better body diode performance than Si products. The body diode forward voltage drops of SiC and GaN products are much higher. It is not desirable to have the body diode conduct for a long time. However, SiC and GaN devices are switching faster and can have shorter deadtime, so the loss of body diode during deadtime can be reduced. Moreover, since the

voltage drop is higher, it is possible to add a parallel schottky diode for the switching device. For Si MOSFETs, however, a parallel schottky diode may not properly work because the body diode has a lower voltage drop than the schottky diode. The body diode will conduct earlier than the schottky diode and null the effect of schottky diode.

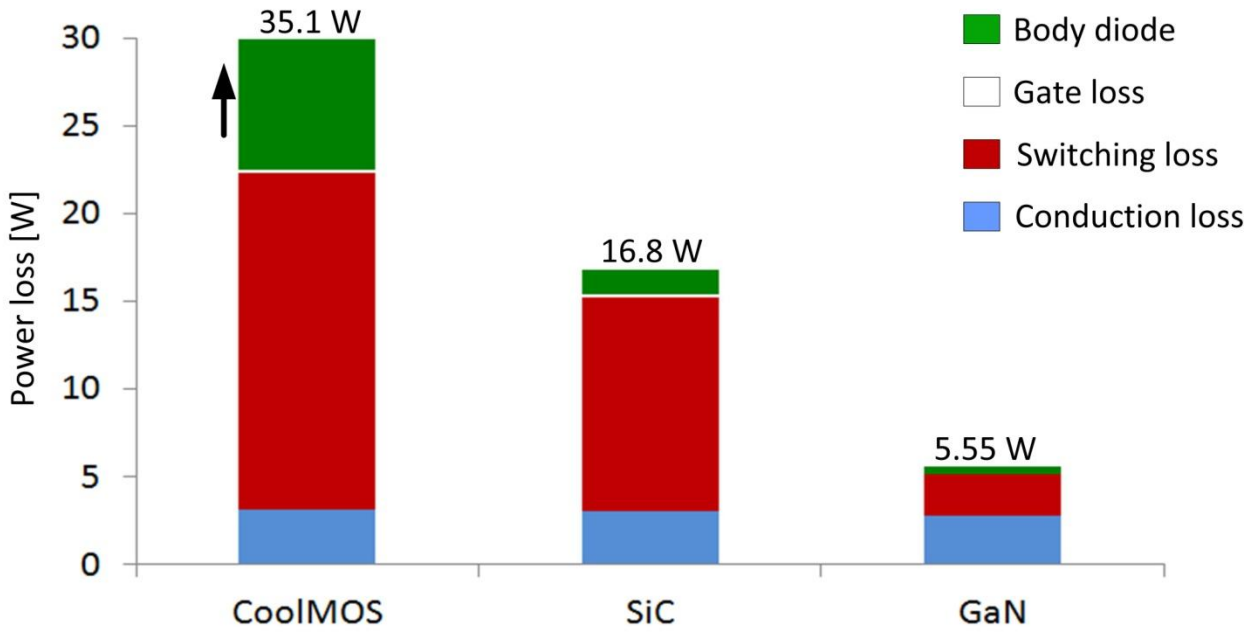


Fig. 7.4. Loss comparison between CoolMOS, SiC and GaN FETs

The losses of these three devices are estimated, as shown in **Fig. 7.4**. The losses are calculated based on a single-phase inverter with 400 V input voltage, 5 A output voltage switching at 100 kHz. Assume the deadtime is 2% and duty ratio is 0.5.

As shown in the figure, the conduction losses of three devices are almost identical, because of their similar $R_{ds\text{-}on}$. The gate losses are in the range of mW and can be neglected for all three devices. For CoolMOS at this voltage level, the body diode reverse-recovery loss

and switching loss are dominant. With the aid of hybrid parallel SiC schottky diode, CoolMOS is possible to get rid of the body diode loss and reaches a 22.5 W total loss. But it is still more than the loss of SiC and GaN. More detailed discussion about loss on different devices can be found in [125][126].

7.2.2 Introduction to Selected Device

Drain-Source voltage [V]	150
Rds(on)@6A [mΩ]	18
Continuous current [A]	12
Gate-source voltage [V]	-5 to 6
Gate-Source threshold voltage [V]	1.4
Total gate charge @ 5 V [nC]	5
Source-Drain forward voltage [V]	1.8
Source-Drain recovery charge [nC]	0

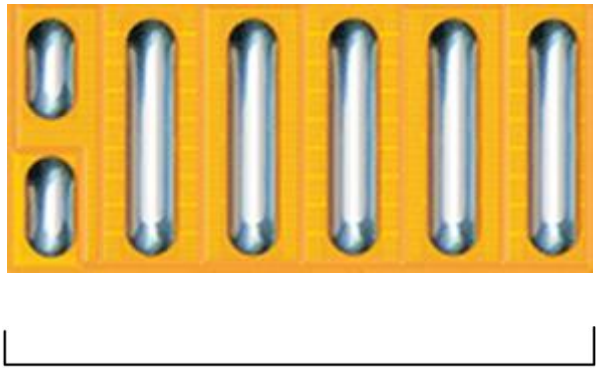
Table 7.2. EPC2018 GaN FET parameters

[127]

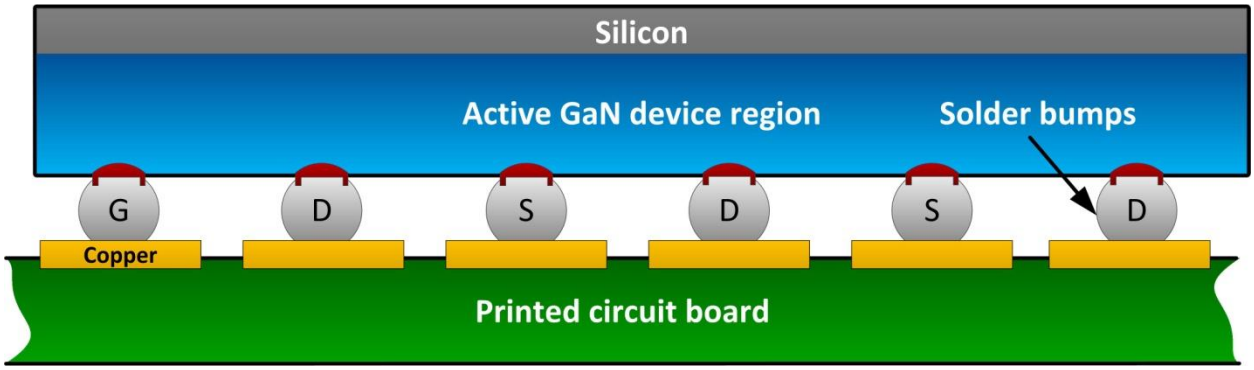
It is possible to build a medium voltage motor drive with 650 V SiC or GaN FETs. In this thesis, due to the limit of available motor and test environment, the target voltage is around 20V-325 V. Hence GaN devices below 200 V are more preferred. The devices are finally decided to be EPC2018.

The selected device EPC2018 has very low on-state resistance 18 mΩ, which will allow very low conduction loss. The total gate charge is only 5nC, so the switch can be turn on or turn off within several nanoseconds. There is no reverse recovery charge, allowing much lower loss during deadtime. The Source-Drain forward voltage is 1.8 V, which is relatively higher than other Si MOSFETs. When switching frequency is low and deadtime can be neglected, the 1.8V voltage does not have influence. However, there are certain applications require high switching frequency, typically > 1 MHz, where the deadtime cannot be neglected so the Source-Drain voltage will greatly affect the converter loss. Method introduced in [128] can solve this problem. But in this thesis, the switching frequency is set below 100 kHz so the effect of Source-Drain voltage is negligible.

The available GaN FETs are supplied in bare die with solder bars, as shown in Fig. 7.5. The bare die has a very small physical dimension. Hence strict soldering temperature profile should be followed to secure the soldering process. Several mils (1 mil = 0.001 inch) mismatch between the bare die and PCB pads may cause breakdown. As reported in [129], if the temperature profile is not properly followed, “solder voiding” can be observed by X-ray imaging.



(a) [127]



(b) [49]

Fig. 7.5. Bare die GaN FET

(a) Bottom view and (b) side view

7.2.3 Parasitic Inductance Minimizing

The advantage of GaN FET with bare die is it has very small package inductance. However, the parasitic inductance of PCB will decide the overall performance of the converter. This kind of bare die devices will add burden to PCB design to minimize the parasitic inductance while maintaining thermal performance and high voltage clearance. As discussed in [129] and [130], the parasitic inductance of PCB copper trace in the power loop and the gate driver loop will affect the switching loss and the voltage overshoot at the switching node. In this section, practical design examples are presented to illustrate the influence of parasitic inductance on circuit performance.

Fig. 7.6 shows the experiment result of one phase output voltage of the 2nd generation PCB design. It clearly shows a set of short circuit events at each rising edge. The high side FET and low side FET are both turning on during the short circuit events. As a result, the output voltage

drops to half of the total DC-link voltage. Saturated current is flowing through both the high side and low side FETs, resulting in large power loss and device break down eventually.

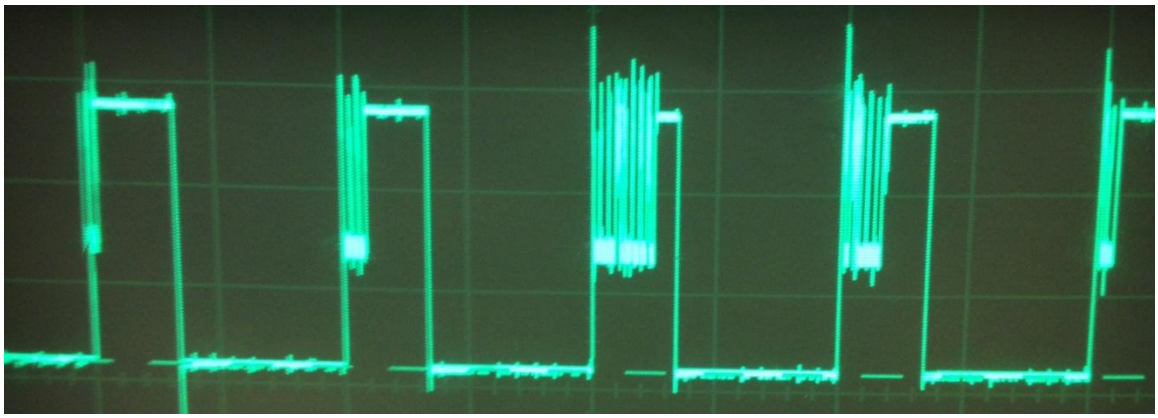


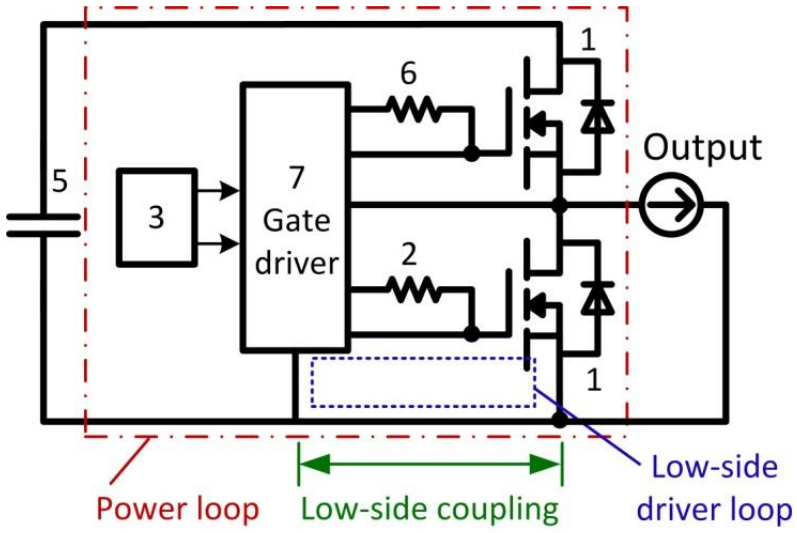
Fig. 7.6. Experiment result: short circuit in the 2nd generation

The reason for this serious problem is the low side FET cannot turn off properly. When the high side FET is turned on, a large dv/dt voltage slope is experienced by the switching node. Since the total gate charge of GaN FET is only 5 nC and the threshold voltage is only 1.6V, it is very easy to be turned on. With a 100 V DC-link, the noise on the ground plane during switching instant may turn on the low side FET. Moreover, since the dv/dt is high, miller effect also has a chance to turn on the low side FET. As long as the short circuit happens, it triggers a huge current flowing in the power loop and generates a very noisy ground plane. This will lead to a set of short circuit events until the ground plane noise drops below the gate threshold voltage. Similarly, the high side FET may also have this problem and must be dealt with.

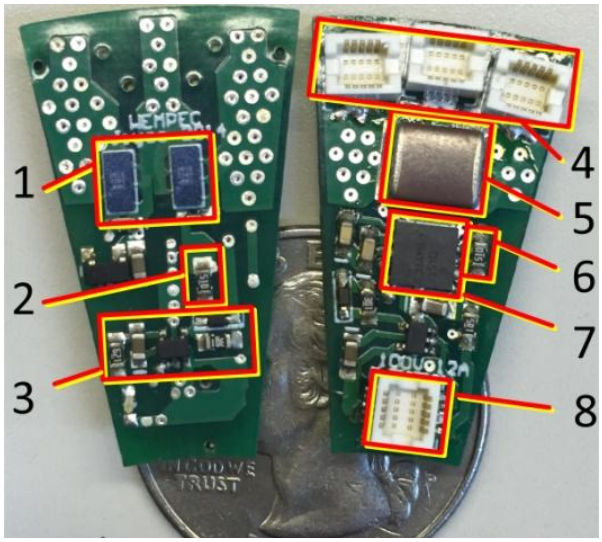
The 2nd generation PCB design is a failure because the parasitic inductance of PCB traces are not properly managed. GaN FETs have very high performance in terms of efficiency and

switching speed. However, they are so sensitive and can be turned on by the PCB noise. **Fig. 7.7** illustrates the basic components of a single phase piece. The loop in blue color is low side driver loop. This loop will fundamentally decide the circuit immunity to noise and miller effect. In design process, this loop must be as short as possible, especially for GaN FETs. The red loop is the power loop. This loop will affect the converter efficiency and voltage overshoot of the switching node. A large voltage overshoot will result in breakdown of the circuit. Consequently, the circuit will not operate safely at rated voltage. The green line in **Fig. 7.7** represents the coupling between the driver loop (the blue loop) and the power loop (the red loop). For a well-designed circuit, the coupling should be as small as possible. Only in this way, the driver loop will not get affected by the power loop during large load transient or switching instant.

[129][131][132] present several PCB layout examples for GaN FET to minimize the parasitic inductance. However for the IMMD application, some of the layout examples do not apply because the DC-link capacitors and GaN FETs must be placed on different sides. Otherwise, the capacitors are taller than the GaN FETs so the heat sinks are not easy to install. IMMD also has higher voltage and requires larger clearance (about 40mil per 100V for exposed vias). Fig. 7.7 (b) shows the design of the 4th generation PCB. The lengths of the power loop and driver loop are minimized in the design.



(a)

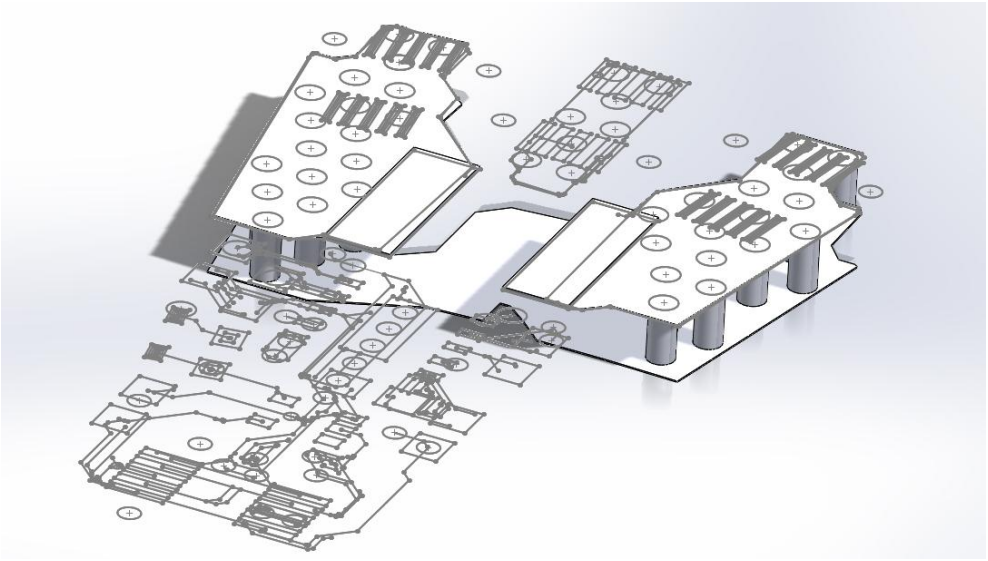


(b)

Fig. 7.7. A single phase power piece

(a) Circuit schematic and (b) 4th generation design example

1. GaN FETs; 2. low-side turn-on resister; 3. dead-time generator;4. power connectors; 5. dc capacitors, 6. high-side turn-on resistor;7. gate driver; 8. signal connector.



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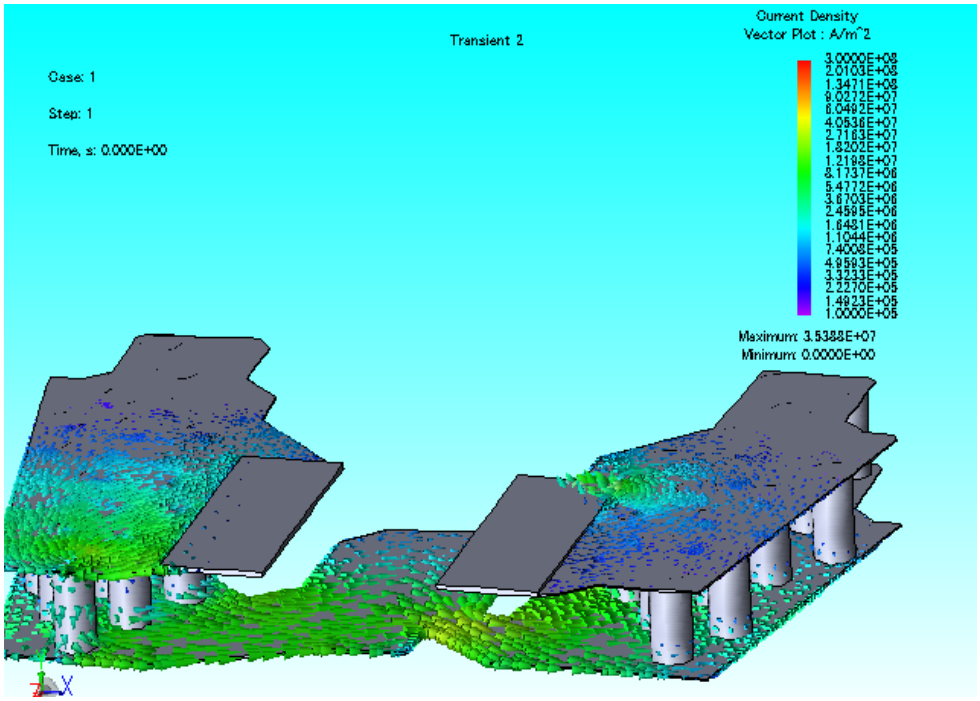
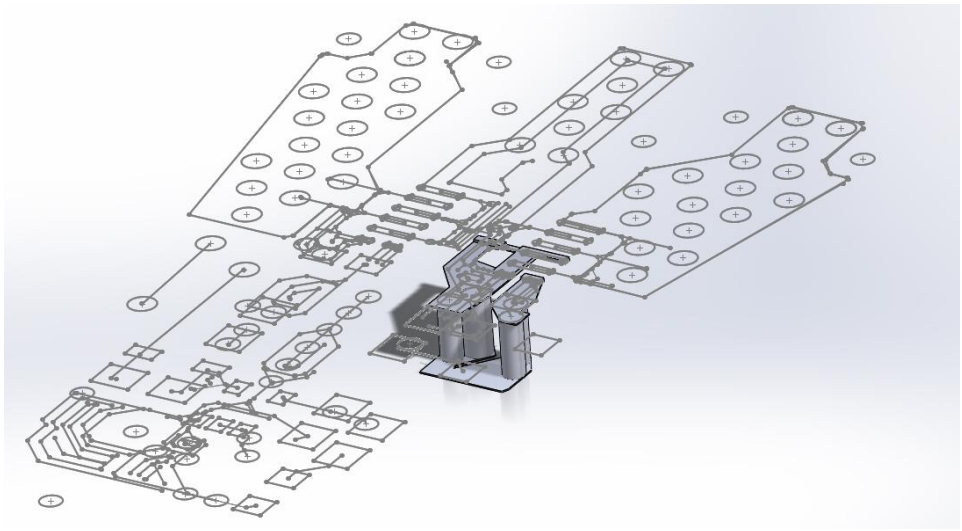


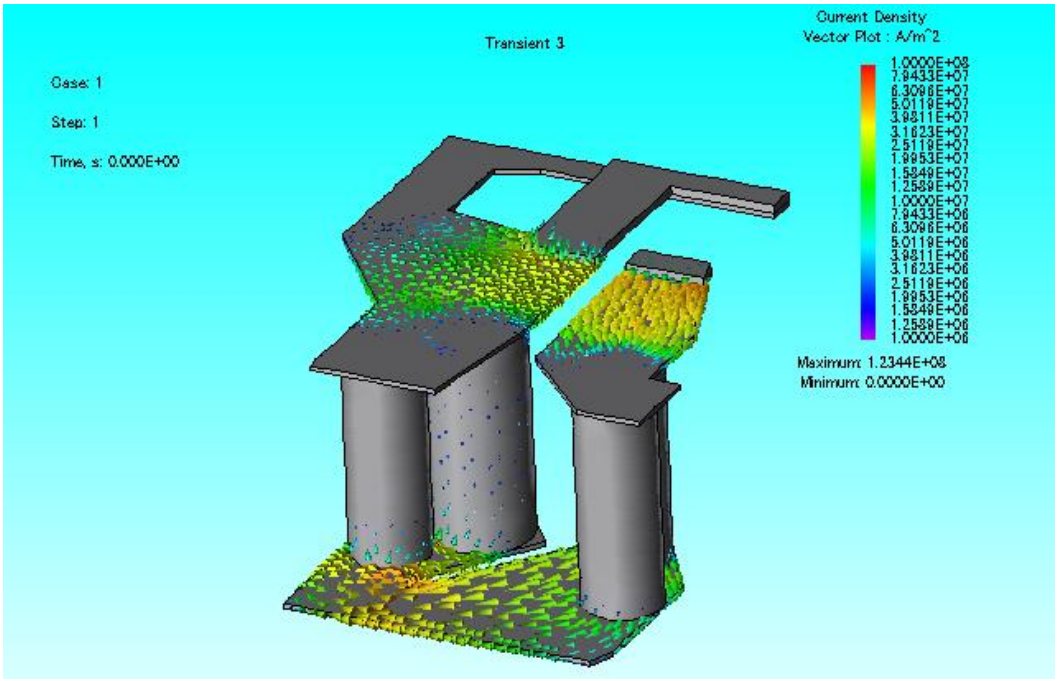
(b)

Fig. 7.8. Power loop parasitic inductance

(a) 3D model and (b) FEA result of current flow



(a)



(b)

Fig. 7.9. Low side gate driver loop

(a) 3D model and (b) FEA result of current flow

Fig. 7.8 and Fig. 7.9 present the 3D models and FEA results of both power loop and gate driver loop. The loop lengths and parasitic inductances are summarized in **Table 7.3**. As a general rule, the power and gate driver loops should have parasitic inductances below 5 nH and the coupling between these two loops should below 1nH.

	Power	Driver	Coupling
Loop total length [in]	0.913	0.350	0.063
Inductance [nH]	3.97	1.73	0.107

Table 7.3. Loop lengths and FEA inductances

7.2.4 Gate resistance for turning on

The extra gate resistance for turning on GaN FET is also a factor that influences the performance of a single phase half bridge. This resistance will not affect the reliability of the circuit because it only affects the turn on process of the FET. The gate driver has a source loop as well as a sink loop, for turning on and turning off the FET respectively. In last section, the focus is purely on the turning off loop to avoid the short circuit. For the turning on loop, a resistor is added to damp the gate signal resonance and to change the turn on performance.

Fig. 7.10 shows the output voltage at the switching node for different turning on gate resistance of the high side GaN FET. The DC-link voltage is 100 V. A smaller resistance will result in a larger gate charge current and a faster turn on slope, so the voltage will rise from 0 V

to 100 V in a shorter time. Typically a faster turn on is more desirable because it leads to smaller switching loss. However, there always exist trade-offs. For faster turn on slope, the dv/dt stress may exceed the limit of the motor winding. In addition, due to the existence of power loop parasitic inductance, a faster turn on slope will cause a larger voltage overshoot. The circuit components must be over-designed to stand the voltage without break down.

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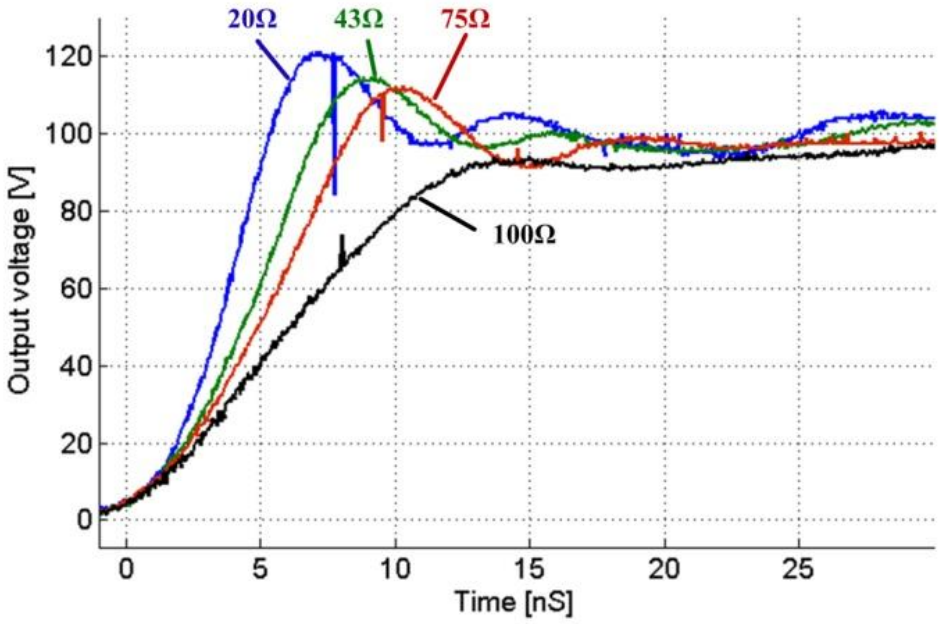


Fig. 7.10. Experiment results: switching performance for different gate resistance

In an IMMD, the gate resistance for turning on should be large enough to avoid voltage overshoot and high dv/dt. It should be small enough so the switching loss is not significant. **Table 7.4** summarizes the experimental switching performance for different resistances. With the test results, a 50 Ω resistance is finally chosen. This will result in an overshot <10% and very acceptable switching loss. It should be noticed that the gate resistance is much larger than a

conventional converter with Si MOSFETs. This is because GaN FETs are more sensitive to the gate voltage. The threshold voltage is only 1.6V and the gate charge is several nC.

Extra gate res. for turn-on [Ω]	20	43	75	100
Rise time [nS]	4.3	5.6	8.9	10.8
Overshoot [%]	21.3	14	6.6	0
Calculated switching loss [W]	0.22	0.28	0.45	0.54

Table 7.4. Switching performance experiment results @ 100 kHz, 5 A load current

The gate resistance also has another important function that damping the gate resonance. The optimal gate-source voltage is 5V for the GaN FETs, but the maximum allowable voltage is 6V. There is only a 1V margin for safe operation. Without gate resistance, the loop inductance and the gate capacitance may resonant and result in overshoot on the gate voltage. With the gate resistance, the gate turn-on loop becomes over-damped and hence there is no overshoot problem on the gate-source voltage.

7.2.5 Efficiency Estimation

The efficiency of the 100 V, 5 A single-phase power piece is estimated to be 98.6%. As can be seen in the figure, the switching loss is dominant. This is because the gate turn-on resistor is as large as 50 Ω. This GaN power piece has the potential to further increase the efficiency by reducing gate turn-on resistor. However in practical, increasing the gate turn-on resistor is not

recommended, for the purpose of avoiding switching resonance and protecting the motor winding.

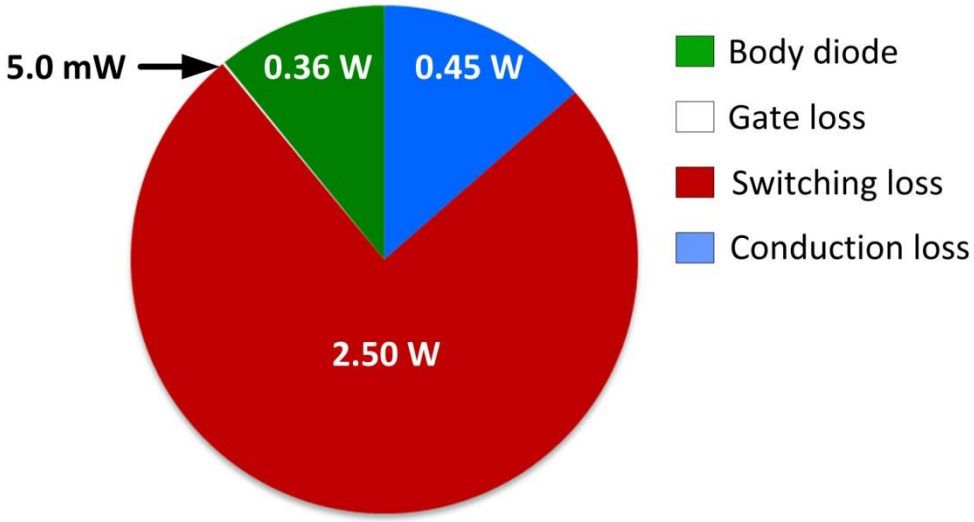


Fig. 7.11. Estimated loss for the single-phase GaN power piece

7.3 IMMD Design Example

In this section, the whole design of 4th generation IMMD is presented. All power converter modules, sensors, controllers and isolators are integrated into the motor housing. The total footprint of the motor and drive system has been reduced to the footprint of the original motor. It is also equipped with a wireless module that communicates with a remote controller. There are two modules connected in series at the DC input. Each module has 3 single-phase GaN pieces connecting to a motor winding segment.

7.3.1 Motor and its split winding

Table 7.5 shows the parameters of the motor for rewinding. Since this motor only has 2 poles, winding configuration #1 is not valid. The winding configuration #2 is applied to this motor and the motor is split into two halves. The original concentric short-pitched windings can be split quite conveniently by its nature without changing any motor property.

Number of poles	2
Motor # slots	36
Motor winding	1 layer, short pitched, concentric
Motor line voltage [Vrms]	190
Motor line current [Arms]	5

Table 7.5. The motor parameters

The motor winding configuration for phase A is shown in **Fig. 7.12**. The original winding has 6 slots per pole per phase. There are two groups of short pitched concentric coils. The two groups of coils are connected together by an end winding. In the rewound winding configuration, this end winding is cut so there are two extra terminals. One of the terminals is the neutral point N1 and another terminal is motor lead A2. The neutral point N1 is soldered with the neutral points from Phase B and C to create a Y-connection. After rewinding, the motor line to line voltage is half of the original value, i.e. 95 Vrms.

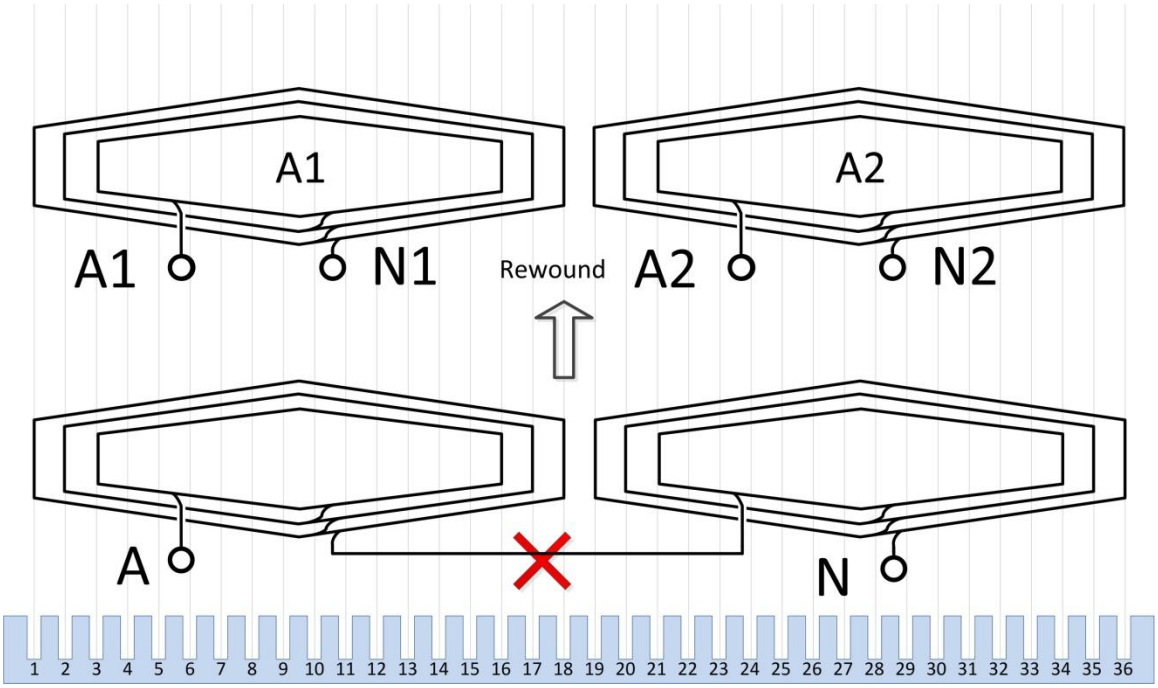


Fig. 7.12. Motor winding configuration of Phase A

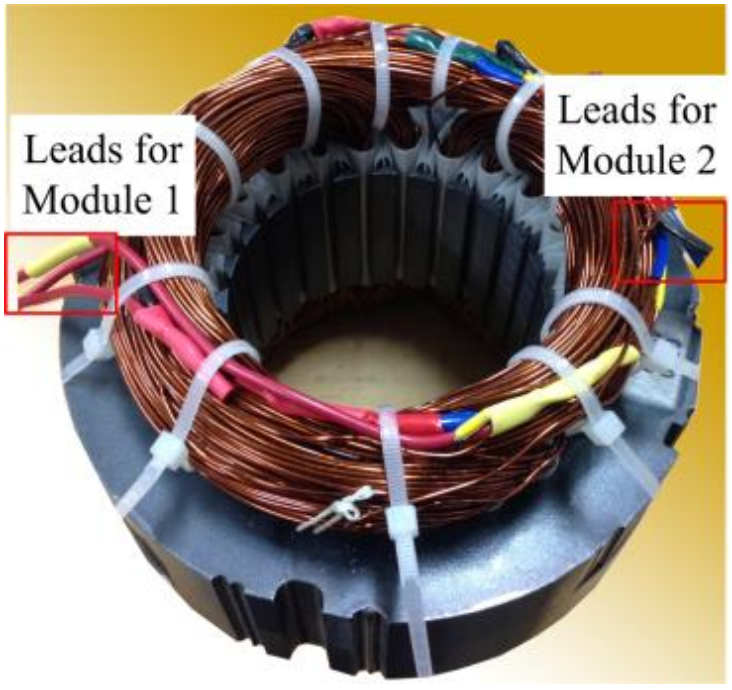
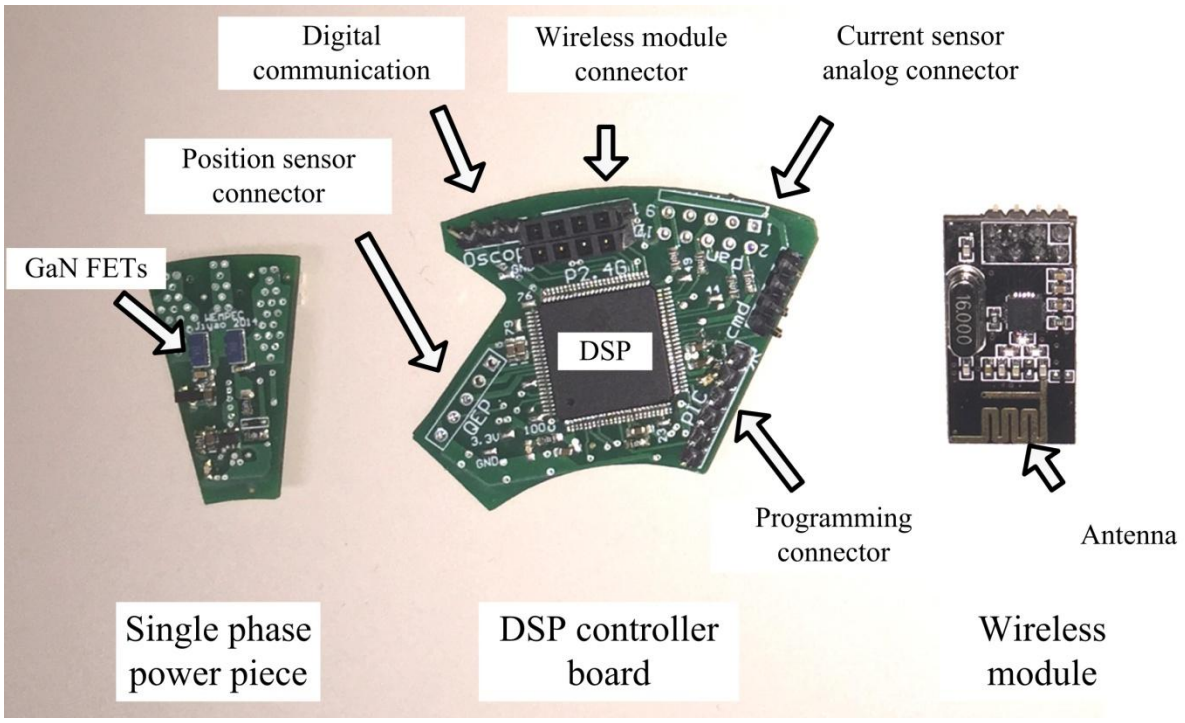


Fig. 7.13. Photo of the rewound motor

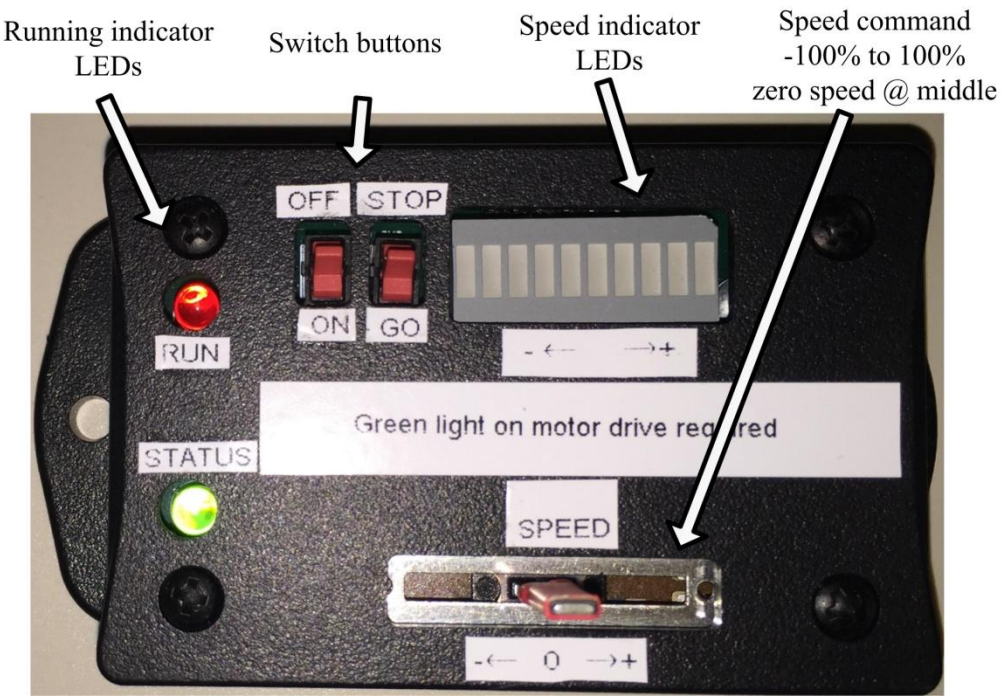
7.3.2 Motor drive

A basement PCB is cut in accordance with the shape of the motor. There are connectors for power input, choppers and other IMMD pieces. Sensors, isolators and extra DC-link capacitors are also in the basement PCB.

6 single-phase GaN power pieces combining into 2 converter modules, a central DSP board and a 2.4 GHz wireless module can be mounted on the basement PCB. These parts are shown in **Fig. 7.14**. There is also another coupled wireless module in the remote controller that can program the IMMD to start, stop, reverse, and accelerate the motor. This wireless communication will be an interface for improving intelligent motor performance and functionality in the future.



(a)



(b)

Fig. 7.14. Photo of IMMD main parts

(a) Single-phase GaN power piece, DSP controller board and 2.4 GHz wireless module,

(b) Wireless remote controller box

Fig. 7.15 shows the IMMD when all parts are mounted on the motor case. The motor winding leads are directly connected to the motor drive without long cable. **Table 7.6** shows the design specifications of the motor drive. The module input capacitance needs to be at least 40 μF to fulfill the 1% voltage ripple requirement according to simulation results. It is finally decided to use 50 μF capacitance in the hardware design. Converter modules with GaN FETs are distributed along the circumference of the motor, resulting in a large area for heat dissipation.

The power rating of this tested motor is relatively small so the motor temperature is within limit even without any heatsinks. If the power rating increases, thermal design has to be taken into consideration. Air holes can be added on PCB or on the side of motor case to boost air venting. Moreover, extra heat sinks can be installed between semiconductor devices and the motor, with vents installed on the side of motor for air cooling [62] or pipes for oil or water cooling [58].

The IMMD uses an open loop V/f control with space vector pulse width modulation (SVPWM). Other conventional close-loop control algorithm can also be applied to IMMD.

Total dc-link voltage [V]	200
Number of modules	2
Module voltage [V]	100
Module capacitance [μF]	50
GaN FETs	EPC2018
FET maximum current [A]	12
Switching frequency [kHz]	100

Table 7.6. Motor drive specifications

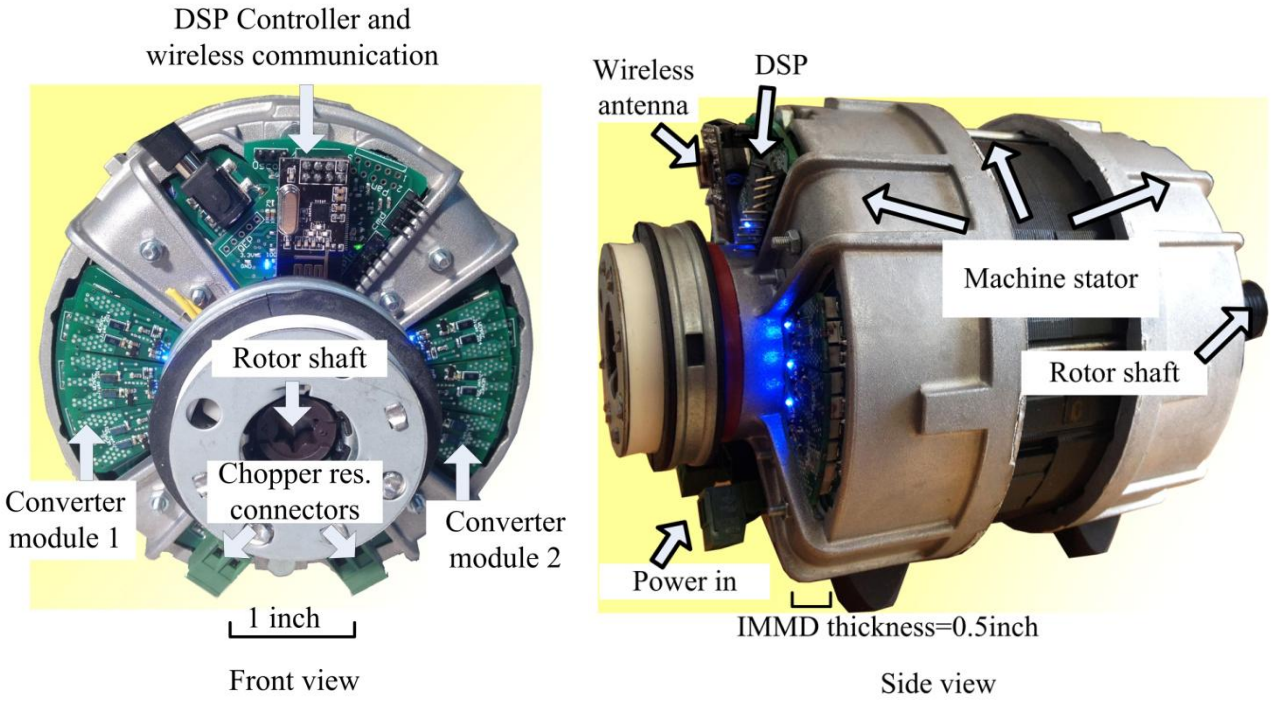


Fig. 7.15. Photo of IMMD with all parts assembled

7.3.3 Experiment results

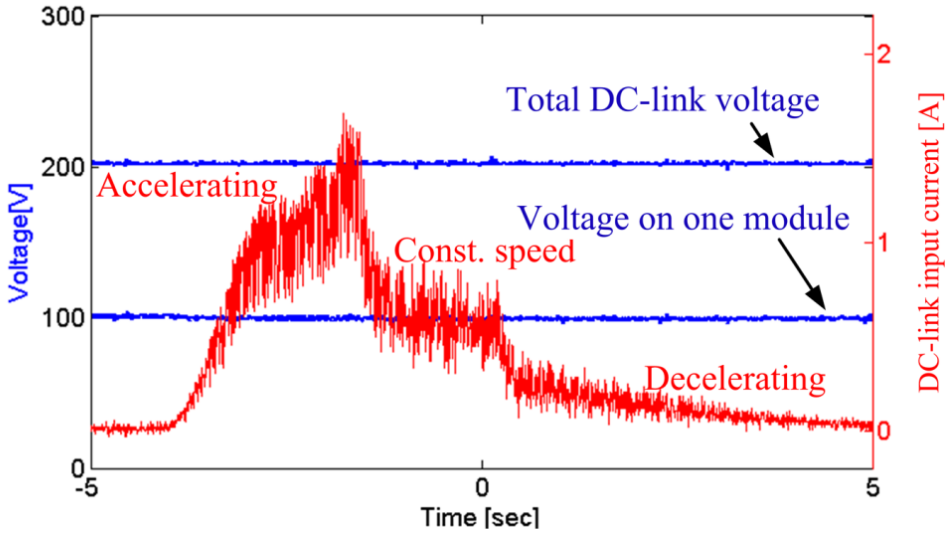


Fig. 7.16. Experiment result for motor start and stop

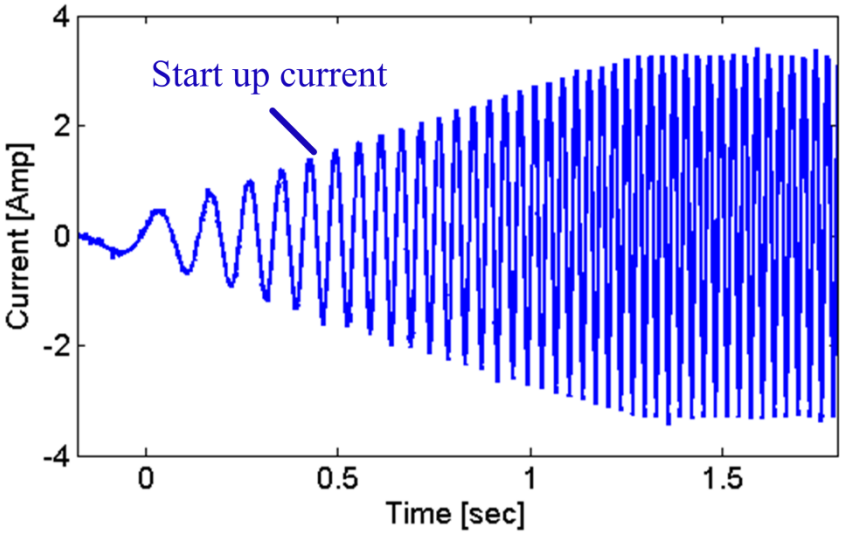
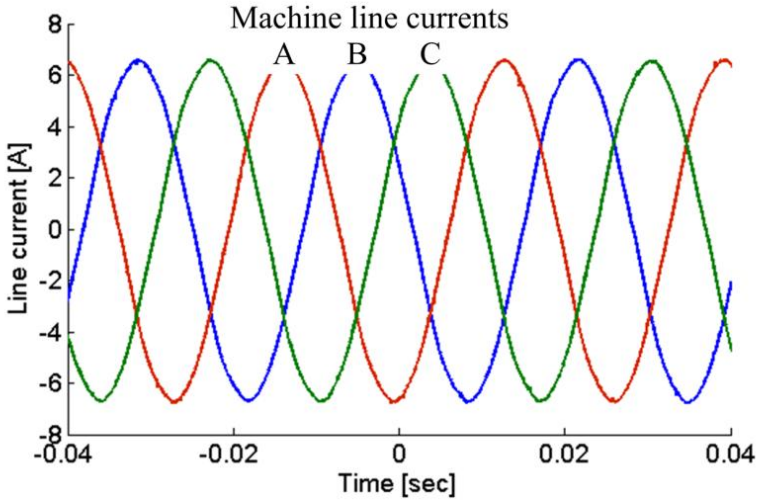
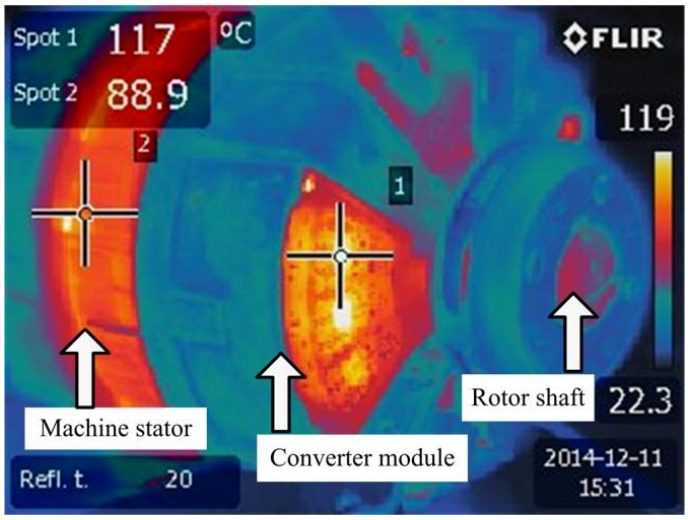


Fig. 7.17. Single phase current for motor start

The experiment result in **Fig. 7.16** illustrates the operation of the IMMD and validates the proposed IMMD can share voltage equally among different modules in a passive balancing approach. In a full operation cycle, the motor is firstly accelerating to the command speed @ 3000 rpm and then keeps a constant speed for about one second, and finally it slows down. The DC-link input current indicates the input power of IMMD. During the whole cycle, there is no voltage balance control and the module voltage remains at 100V, which is half of the total dc-link voltage. **Fig. 7.17** shows the motor line current during start up. These test results show that IMMD can operate with conventional motor control method. An IMMD is almost equivalent to a conventional three phase motor drive.



(a)



(b)

Fig. 7.18. IMMD thermal test

(a) Three phase line currents (b) the thermal measurements

Fig. 7.18(a) shows the three phase currents in steady state from one module during operation. **Fig. 7.18**(b) shows the thermal performance of the IMMD under the load condition. The picture

was taken after the motor ran for 30 minutes and the temperatures of both motor and drive were stable.

Previous chapters have already included many experiment results of this IMMD. These experiment results included in previous chapters are:

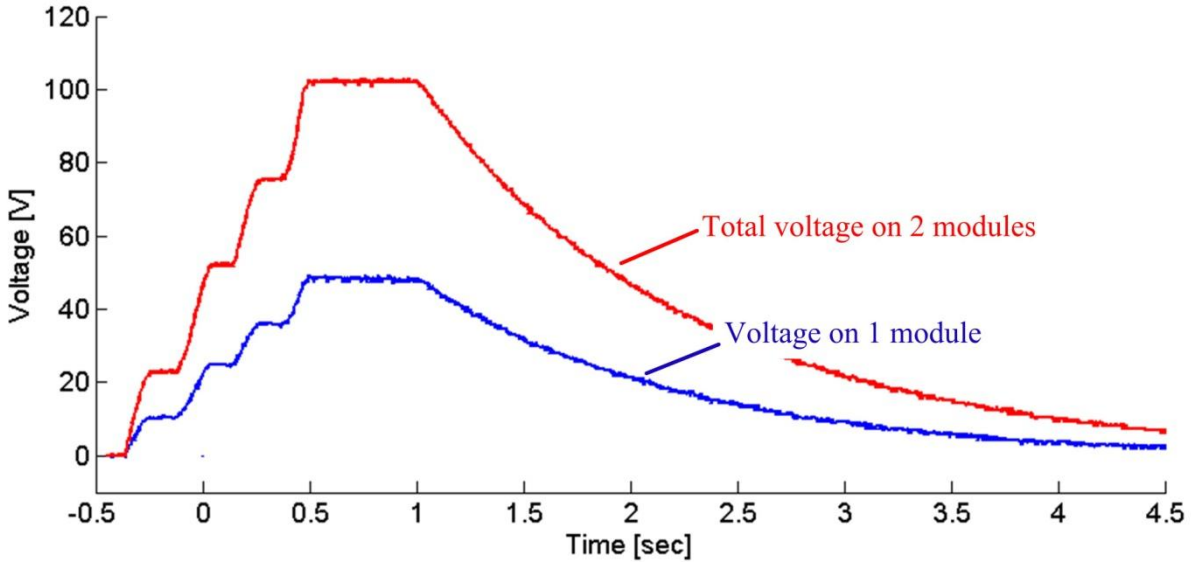


Fig. 3.10. Experiment result for passive voltage balancing

Fig. 3.10 shows the voltage balancing between two IMMD modules when total DC input voltage changing. Voltage on one module is exactly half of the total voltage.

Fig. 3.11 shows the voltage balancing result during normal operation without any voltage control. The module voltages are balanced at about 100 V. There exists a difference between the module voltages, caused by machine asymmetry. This difference is small and will not affect normal operation of IMMD.

Fig. 3.17 shows the voltage balancing result when CVB is applied. With CVB, the difference between module voltages is very small. Only switching ripples can be observed.

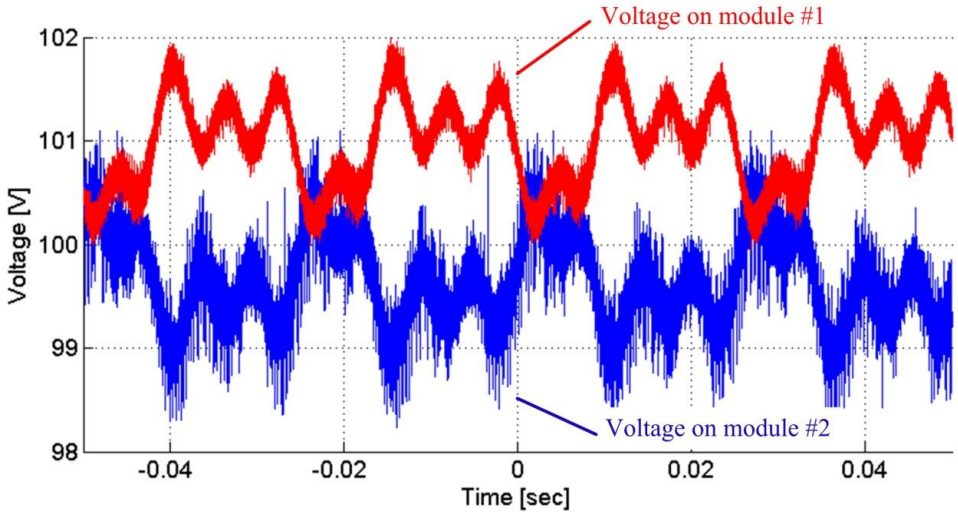


Fig. 3.11. Experiment result of zoomed in voltage ripples under full load

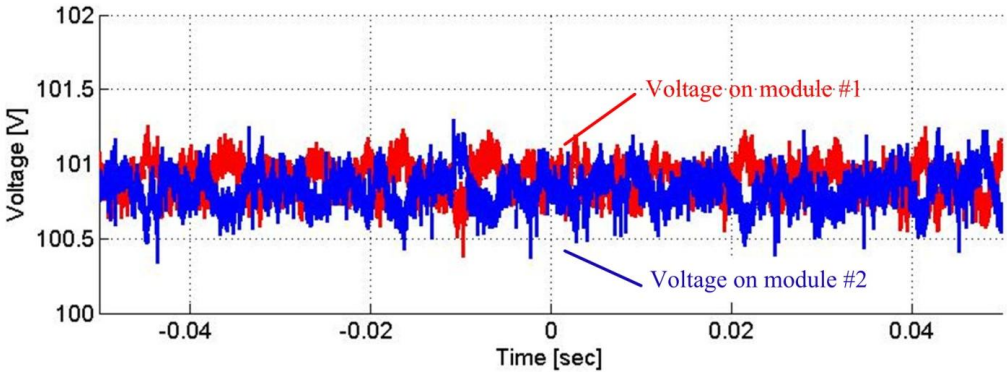


Fig. 3.17. Experiment result of zoomed in voltage ripples with CVB

Fig. 5.5 validates the reduction of input ripples by applying gate signal interleaving technique. **Fig. 5.14** shows the effect of interleaving technique for machine line current ripples.

All these experiment results prove that a compact IMMD can be realized by the proposed multilevel structure and GaN FETs. The proposed multilevel converter can operate as a normal machine drive and the module voltages are always balanced.

Chapter 8

Conclusions, Contributions and Future Work

This thesis presents a multilevel motor drive that utilizes the magnetic properties of machine windings to achieve a better multilevel topology. As a result, the motor drive can have better design flexibility, smaller size and lower cost. Based on this topology, a high power density, fully functional integrated modular motor drive (IMMD) is built for demonstration. Gallium Nitride (GaN) semiconductor devices are used to handle the high operating temperature inside motor housing. In this chapter, conclusions and contributions of this thesis are summarized. Recommended future works are proposed.

8.1 Conclusions

- **Proposed multilevel topology has small size, low cost, high efficiency and great design flexibility.**

The proposed topology utilizes the magnetic properties of motor windings for electric isolation. Hence there is no extra clamping diode, flying capacitor, isolation transformer or filtering inductor as in other multilevel topologies. This allows the proposed topology to have a minimum number of components.

The proposed topology has three-phase converter modules so the DC-link capacitors only handle the switching ripple. By comparison, other multilevel topologies do not have modular

design (NPC and FC) or three-phase structure (CHB, MMC and MHF). The sizes and cost of capacitors are minimized in the proposed topology by using three-phase structure.

The voltage stress on converter modules is reduced in the proposed topology. Hence the size and cost of converter isolation devices can be reduced. The voltage stress on motor winding is also reduced, leading to a longer motor lifespan or less expensive motor winding insulation.

The voltage stress on semiconductor devices is reduced. Much higher efficiency can be achieved by reducing voltage stress on FETs (e.g. reduced by about 20 times if ten 100 V FETs substitute for one 1000 V FET).

With the extended version of the proposed topology, it is possible to utilize commercialized multilevel modules, such as NPCs and FCs. In this way, it is flexible to increase the voltage-level without adding much cost or complexity.

- **Proposed multilevel topology offers an extra degree of control freedom and fault-tolerance.**

The proposed multilevel topology has multiple machine segments driven by individual converter modules. Consequently, extra control freedom is offered by this topology.

The control of an individual converter module can be dynamically adjusted. The power, current, flux and torque of a machine segment can be controlled in a way such that the loss is minimized, the temperature of converter/machine is dynamically distributed, or the common-mode voltages from different modules are canceled.

During fault conditions, the fault machine segment and converter modules can be detected and by-passed. Even when one converter module completely breaks down, other healthy

modules will handle the total DC-link voltage. It is desirable to have more converter modules, because the influence of losing one module will be smaller.

- **Module voltages are balanced without any control. Optional voltage control for the proposed topology is simple and effective.**

Different from other multilevel topologies, the proposed one does not need any voltage balance control algorithm. It can rely on the motor windings to balance the module voltages, because the motor segments are identical or strong coupled. The proposed converter can utilize any conventional motor control algorithm to run the motor. The motor control algorithm has no difference between the proposed multilevel converter and a conventional three-phase motor drive.

Optional voltage balance control can be added to the converter to achieve better noise rejection and fault tolerance. This thesis presents two types of optional voltage balancing control: centralized voltage balancing (CVB) and distributed voltage balancing (DVB), which are both proven to work properly.

- **Split machine segments in different pole-pairs are equivalent to smaller machines tied to the same rotor shaft. Split mmachine segments in same pole-pair are equivalent to the primary and secondary sides of a transformer.**

Split machine winding segments in different pole-pairs are proved to have zero coupling between each other in dq-axis. The individual machine segment also has the same dq-axis model as a conventional machine. This means that the machine segments are equivalent to smaller individual machines tied to the same rotor shaft. The flux, torque and power of one segment can be easily adjusted without affecting other segments.

Machine winding segments in same pole-pair tend to have strong magnetic coupling between each other. Consequently, they are equivalent to the primary and secondary sides of a transformer. The strong coupling will force the converter modules to have identical voltages.

When the machine segments are in the same slots, magnetic coupling is strongest and voltage balancing is strongest. There exist parasitic capacitances between the segments and small LC filters are recommended in this thesis to deal with PWM mismatches between modules.

- **Capacitor size is greatly reduced by properly selecting capacitor type and matching the optimal switching frequency.**

Capacitor selection should meet the requirements of capacitor RMS current, voltage ripple and capacitance value. The optimal switching frequencies for different types of capacitors should also be considered. Beyond the optimal switching frequency, a capacitor cannot further reduce its size because it is limited by its RMS current instead of its capacitance.

- **Gate signal interleaving technique can be applied to further reduce DC-link voltage ripples or DC-link capacitors. Common-mode voltages and currents are also reduced by interleaving.**

Proved by simulation and experiment results, gate signal interleaving technique is effective in reducing total DC-link voltage ripples. In other word, DC-link capacitors can be reduced if the DC-link voltage ripples are maintained.

Common-mode voltage of the machine can be reduced by interleaving. Consequently, the ground wire current and bearing current of the machine are reduced.

- **IMMD can be realized by using the proposed topology, optimizing the selection of capacitors and using GaN devices.**

The proposed topology can effectively reduce the rating voltages of capacitors and field effect transistors (FETs). This allows the capacitors to be thinner and hence easier to integrate. Low voltage FETs have better efficiency and the size of heat sinks can be minimized. In addition, GaN FETs are only commercially available at low voltage, usually below 200 V. The proposed topology makes it possible to use low voltage GaN FETs in motor drive applications. The GaN FETs enjoy the advantages of higher switching frequency, higher operating temperature and higher efficiency. As a result of higher switching frequency, the capacitor size can be reduced to a point that is not achievable by Si devices. With higher operating temperature and efficiency, the separate heatsinks of motor drive can be eliminated. The motor and the motor drive can share the same heatsinks and hence the fully integrated motor drive is achieved.

- **Parasitic inductance of GaN FETs should be minimized and the gate turn-on resistance value should be optimized.**

The 4 generations of hardware IMMD design shows the importance of minimizing parasitic inductance in the gate loops of GaN FETs. The GaN FETs are very sensitive and without proper design, short circuit can be triggered by ground plane noise. Minimizing the parasitic inductance can effectively prevent the short circuit problem.

The gate turn-on resistance should be tuned to an optimal value such that both the voltage overshoot and the switching loss are within reasonable range.

8.2 Contributions

8.2.1 Input-series Multilevel Topology for Integrated Motor Drive

An input-series multilevel topology for integrated motor drive applications is proposed in this work. Key contributions are summarized as follows:

- **Multilevel topology motor drive with input-series three phase modules.**

In this thesis, a multilevel topology is proposed to realize IMMD. It is derived from the single phase cascaded H-bridge (CHB) topology and utilizes motor windings as isolation transformers. Different from other topologies, this multilevel topology considers the motor properties and uses three-phase converter modules to minimize the size and cost of multilevel motor drive.

- **Side by side comparisons between the proposed topology and other existing multilevel topologies.**

A thorough review of existing multilevel topologies is presented in Chapter 1. Based on the review, component quantity and sizing are evaluated and compared to the proposed topology. The voltage stresses on converter modules and motor windings are also compared. These comparisons show that the proposed converter has many advantages for motor drive applications.

- **Development of motor split winding configurations.**

The proposed topology requires a motor with multiple three-phase windings, which is different from a conventional motor with only three leads. The motor winding configurations for different types of motor, e.g. distributed lap, distributed concentric, concentrated and etc., are

developed in this thesis. It has been shown in this work that a motor can be easily modularized into multiple three-phase winding segments without changing any motor property.

- **Extended topologies that greatly improve the design flexibility.**

Based on the proposed fundamental topology, a family of extended topologies is also proposed. This work demonstrates that the proposed topology can utilize existing commercialized multilevel converter modules to further increase number of voltage levels without adding more motor segments.

8.2.2 Evaluation of Capacitor Size in a Three-phase Module

This work demonstrates the procedure of selecting DC-link capacitors to minimize the sizes. Key contributions are summarized as follows.

- **Identification the limits of the capacitor selection.**

It is shown in this work that the capacitors are selected according to both their current limit and capacitance limit. Through theoretical analysis and simulation results, numerical values of these limits are calculated. This work also points out the significant influence of capacitor height on the overall system size. The results in this works can help to select proper DC-link capacitors for a motor drive.

- **Comparative evaluation of different types of capacitors.**

In this thesis, three major types of capacitors, i.e. electrolytic, film and ceramic capacitors are evaluated and compared at different switching frequencies. The differences of these capacitors are identified. Practical experiences and design recommendations are also presented in this thesis.

- **Evaluation of capacitor optimal switching frequency.**

This work points out the existence of optimal switching frequencies for different capacitors. It contributes a practical method to evaluate the size of capacitors and to decide the optimal switching frequency for a motor drive module.

8.2.3 Analytical Model of Split Motor Winding

The split winding machine has several segments and hence the conventional machine modeling method cannot be used. This thesis develops the analytical model for split winding machines. The contributions are summarized as follows.

- **Self and mutual inductances of asymmetry winding coils.**

In this work, the self and mutual inductances of winding coils are developed based on the asymmetry distribution of flux density. It differs from the conventional motor modeling method that assumes winding coils in different pole-pairs are identical and hence generate symmetry flux density. This work contributes the analytical equations to calculate the mutual factor between two coils and it is verified by FEA results.

- **Development of inductance matrix in abc-axis of windings in different motor segments.**

The inductance matrix of one pole-pair and two pole-pairs are developed in this thesis, based on the asymmetry flux density distribution. The results can be extended to any number of pole-pairs. The inductance matrix provides an analytical description of the split winding machine.

- **Development of inductance matrix in dq-axis of windings in one machine segment.**

Based on the abc-axis model, dq-axis model is developed in this thesis, by applying park transform to the abc-axis model. This model proves that the single pole-pair motor segment itself

is identical to a conventional small motor with conventional dq-axis model. This is a significant result that shows the simplicity of the proposed motor with split winding configuration.

- **Finding of time-variant manipulate input decoupling matrix $\mathbf{M_r}$ that decouples the dq-axis model of different machine segments.**

This thesis points out an important fact that zero-axis current/voltage is always zero during normal operation. This allows performing row operation without changing the matrix values. A large portion of effort is spent on finding the proper time variant manipulate input decoupling M_r. It is finally found in this research and can successfully decouple the dq-axis models of machine segments. The significance of this work is to prove that different machine segments have zero coupling between each other, and as a result, the individual segment has an independent, decoupled dq-axis model.

- **Development of equivalent transformer models for machine segments in same pole-pair.**

This thesis develops the equivalent transformer models for machine segments in same pole-pair. The combined equivalent circuit of both machine and drive module is provided. This thesis also points out the existence of parasitic capacitance between two machine segments in same slots. The capacitance may cause current ripples due to PWM mismatches and adding LC filters are recommended in this thesis.

8.2.4 Investigation and verification of Converter Voltage Balancing Methods

- **Investigation of three converter voltage balancing methods: passive, CVB and DVB.**

Three different types of voltage balancing methods are proposed and investigated in this thesis, including passive method, centralized voltage balancing (CVB) method and distributed voltage balancing (DVB) methods. This work demonstrates various possibilities to balance the voltage of converter module. This adds great design flexibility to the proposed converter topology.

- **Experiment and simulation verification of voltage balancing methods.**

This work demonstrates the effectiveness of passive voltage balancing methods for the proposed converter. It is also verified by experiment results. This work identifies the module voltage disturbance caused by motor asymmetry. CVB and DVB control methods are proposed to improve the disturbance rejection ability. Both experiment and simulation results are presented to verify the control methods.

- **Investigation of natural voltage balancing mechanism due to equivalent transformer formed by machine segments in same pole-pair.**

This thesis identifies that the strong coupling between machine segments in same pole-pair will lead to a natural voltage balancing mechanism. It will force the converter modules to have identical voltages, without any active control. This mechanism is verified in this thesis by both simulation and experiment results.

8.2.5 Gate Signal Interleaving for the Proposed Topology

- **Verification of gate signal interleaving technique that can further reduce capacitor size.**

Gate signal interleaving technique is proposed by this work in order to reduce the capacitor size. Experiment results have verified this technique working properly for the proposed input-series topology.

- **Comparative evaluation of gate signal interleaving technique between input-parallel topology and the proposed input-series topology.**

By a group of simulation results, this work demonstrates that gate signal interleaving of input-parallel topology is degrading at high switching frequency. This is because the parasitic inductance between converter modules limits the current ripple cancelling effect. By comparison, gate signal interleaving is effective for the proposed input-series topology at both low and high frequency, because the voltage ripple cancelling is always working properly for input-series topology.

- **Investigation of common-mode voltage/current reduction.**

This work confirms that the common-mode voltage and current of the proposed topology can be reduced by interleaving technique. Both analytical evaluation and simulation results are provided.

8.2.6 Hardware Design of GaN IMMD with the Proposed Topology

The physical integration of IMMD and design of GaN is very challenging and in this work, four generations of hardware designs are presented. Key contributions are summarized as follows.

- **The first motor drive with GaN FETs.**

The work in this thesis presents the first hardware motor drive built with GaN FETs. High efficiency and high switching frequency are achieved by GaN FETs, and hence 1) the heat sinks of motor drive are eliminated, 2) the size of capacitor is reduced and 3) the operation is in ultra-sonic frequency range and there is almost no audible noise. This work demonstrates the concept to build motor drive with GaN FETs and to achieve better performance.

- **Design of IMMD physical structure.**

Through four generations of hardware designs, this thesis comes up with the final version, which is a very practical structure with small physical size. The connectors, component placements and height management are very important aspects in hardware design and they are carefully considered in the proposed structure. This work can serve as hardware design guidance for future IMMD.

- **Design experience of single phase power piece with GaN FETs.**

Experiment results, both good and bad, are presented in this thesis. Since GaN FETs are relatively new devices, this work presents some hardware experience of using GaN FETs. Critical design considerations are addressed in this thesis, such as parasitic inductance and gate turn-on resistance.

- **Prototype design of 4-module GaN machine drive with close-loop IFOC.**

The prototype design of 4-module machine drive with GaN FETs is a solid hardware example of the proposed topology. This design proves that the proposed topology can be easily extended to more modules without difficulty. The success of 4-module machine drive also indicates that this topology is suitable for medium voltage drives, by using 600 V or 1200 V devices. The prototype design also validates the machine drive can be controlled by conventional

method such as IFOC. Meanwhile, the voltage balancing is proved to work effectively even when IFOC generates a large current transient.

8.3 Recommended Future Work

8.3.1 Development of Extended Topologies

Extended topologies introduced in chapter 2 provide great design flexibility to the proposed multilevel converter. This thesis recommends future development of the extended topologies. The control of the extended topology will be more complicated, because the multilevel converter modules (NPCs or FCs) require their own voltage control. The inner module control, the module voltage control and the machine control will be mixed in the extended topologies.

8.3.2 Detailed Investigations of Module Voltage Ripples

It is desirable to further investigate the module voltage ripples of the proposed topology. The module voltages are naturally balanced and the voltage ripples are caused by machine asymmetry. In other word, the voltage ripples are measurements of machine asymmetry. By observing the voltage ripples and monitoring machine asymmetry, it is possible to achieve early detection of mechanical failure or partial demagnetization. By understanding and manipulating the voltage ripples, it is possible to operate the machine more smoothly with smaller torque ripple. New algorithm is recommended to control the voltage ripples in an optimal way.

8.3.3 Multilevel Rectifier for IMMD

This thesis demonstrates a multilevel IMMD which utilizes half of the motor housing space. In the other half, a corresponding multilevel rectifier can be installed. The multilevel rectifier could possibly use new topologies and GaN devices. A fully integrated AC-DC-AC motor drive can be achieved in this way.

8.3.4 Improving Reliability and Fault Tolerance

Due to its modular design, the proposed topology has the potential to achieve better reliability and fault tolerance [62][63]. This thesis recommends implementation of new control techniques to detect and manage fault conditions and improve the reliability for IMMD. When one module breaks down, the control algorithm should identify the fault condition and properly bypass the broken module. The healthy modules should handle the total voltage evenly. Future work should also identify the possibility to continuously operate the machine even under fault conditions. The reliability concerns of current and voltage sensors in multiple modules also require future investigation.

The converter modules can also dynamically control the power consumptions and the load currents. In this way, the total loss of the converter can be distributed to different modules in an optimal way. For example, the module with highest temperature should reduce its loss in order to reduce its temperature. In general, the module with higher voltage tends to have higher output power and loss. By adjusting the module voltage, thermal distribution is controlled and as a result, it helps to improve the converter reliability and lifespan [86]. Other control method is also possible and requires future investigation.

8.3.5 Applying Advanced Machine Control Techniques

With more converter modules, a lot of advance control possibilities can be explored. For example, the modules can have different switching frequency. Majority of the modules can switch at a reduced frequency to reduce the power loss. Minority of the modules can switch at high frequency to improve the control bandwidth, dynamic stiffness and noise rejection of the converter. The switching frequency could even alternate between modules to evenly distribute the power loss. For a second example, special switching pattern can be developed to minimize the common-mode voltage.

The module voltages are controlled by manipulating the power consumption of the module and corresponding machine segment. Advanced machine control techniques, such as deadbeat-direct torque and flux control (DB-DTFC) [106][107], can be applied such that each converter module can have very fast response. Consequently the module voltages can have better dynamic stiffness to reject noise. In addition, the proposed multilevel converter provides extra degree of control freedom. DB-DTFC can adjust the volts-sec of an individual machine segment, and thus control the flux and torque of the machine segment.

The proposed topology has several converter modules. To minimize the data transfer between modules, each module should be smart enough to work independently. It is recommended to implement self-sensing technique [87][88], so the data transfer of position encoder signals can be eliminated. This can greatly reduce complexity and improve the reliability of a converter module.

8.4 Future Possibilities

8.4.1 Active Magnetic Bearing

In the proposed topology, it is possible to manipulate the power and flux of any machine segment. Hence the radial force from an individual segment can be precisely regulated. With proper control, the proposed machine drive could decouple the gravity force of the rotor and realize active magnetic bearing. The advantages of active magnetic bearing include lower audible noise, lower friction loss and longer lifespan of motor drive system.

8.4.2 Current Source Inverter

Current source inverter has been proved to have many desirable features [133]. The machine itself is a large magnetic component. It is a great research opportunity if the machine windings can be utilized as DC-link inductors. In this way, the machine drive system only consists of machine and semiconductor devices, with no DC-link capacitors or inductors.

8.4.3 Online Winding Reconfiguration

The proposed topology has access to all machine segments and it is possible to reconfigure the machine windings in the control algorithm, for example, exchanging phase A and Phase B windings, to extend the operating range of the machine. To realize online winding reconfiguration, it may require special machine design and winding configuration.

8.4.4 Medium Voltage Machine Drive for Hydropower Generator

A hydropower generator usually has low speed, large diameter and many pole-pairs along the circumstance. The proposed topology is very suitable for this type of machine. It is a great research opportunity to combine the proposed topology and a hydropower generator. This machine drive system can directly supply a medium voltage DC-link.

Appendix

A.1. Hardware Design of IMMD

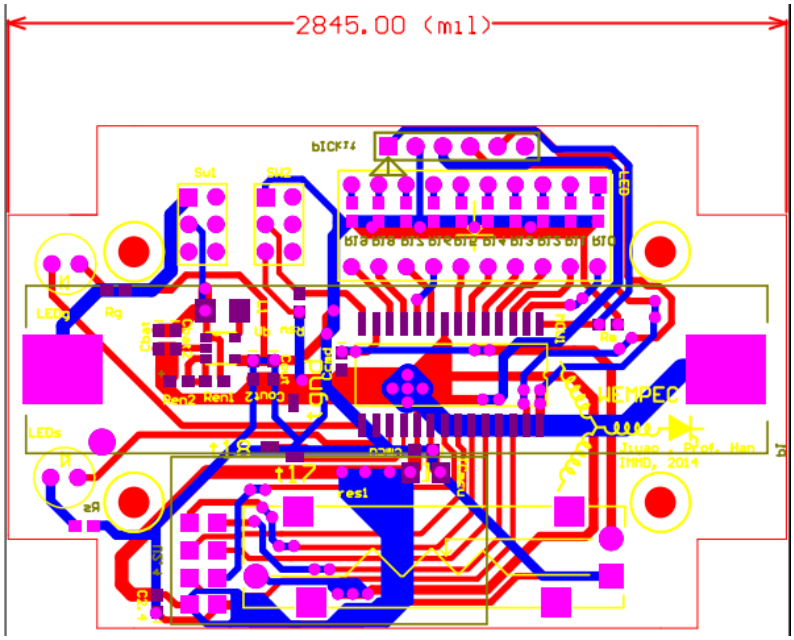


Fig.A.1. Design of IMMD remote controller

including DSP, switch button, battery, wireless module and LED indicators

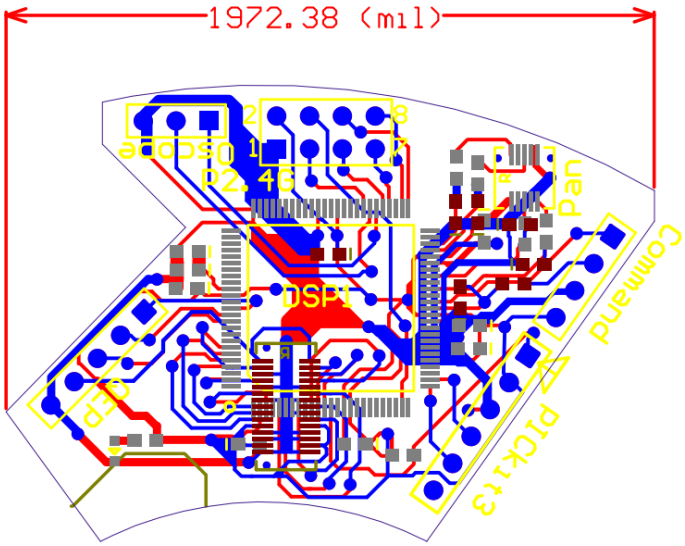


Fig.A.2. Design of DSP controller board

including DSP, connectors for programmer/wireless module/analog signals

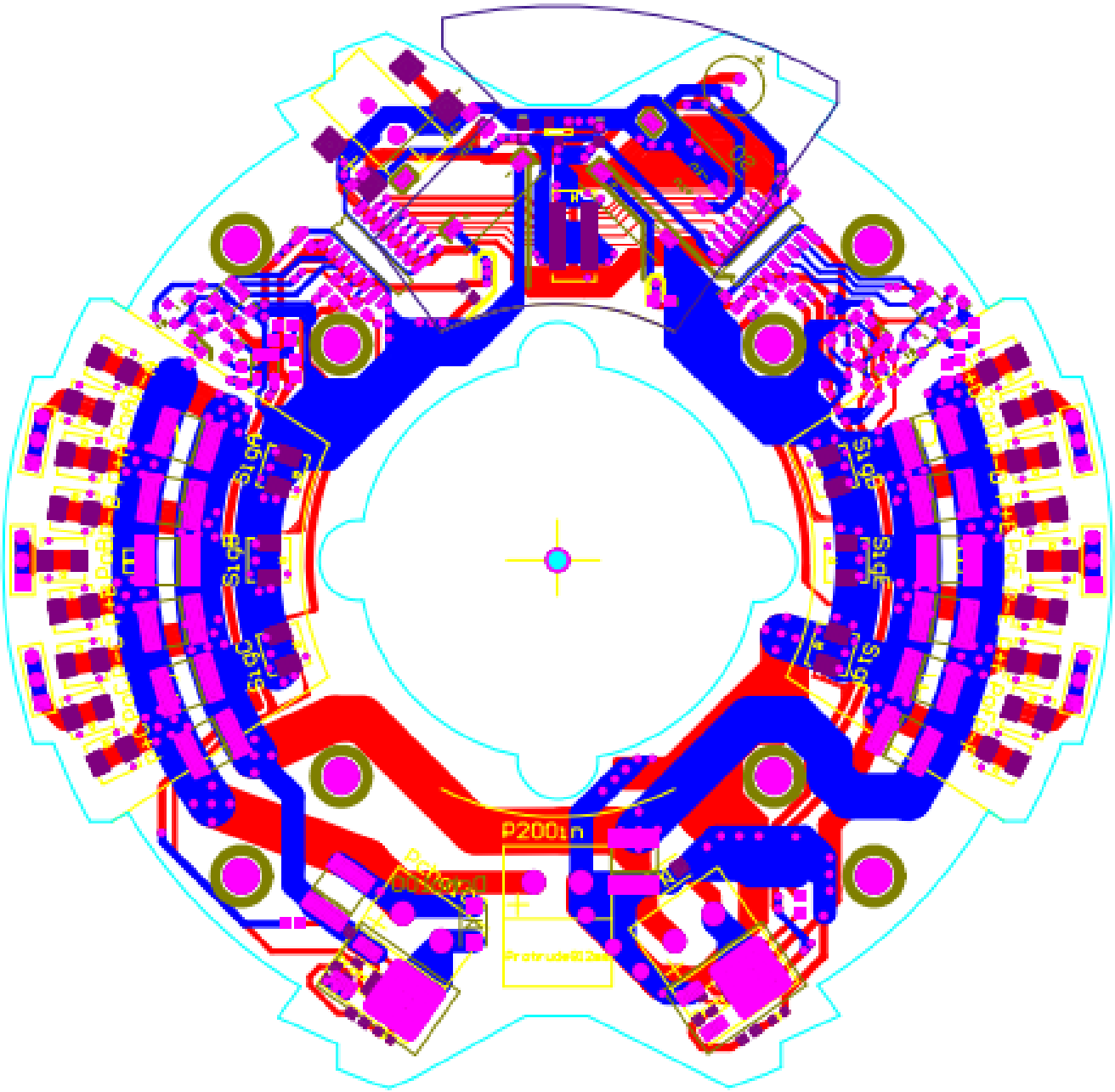


Fig.A.3. Design of IMMD mother board

including extra DC-link capacitors, connectors, isolators, sensors and break choppers

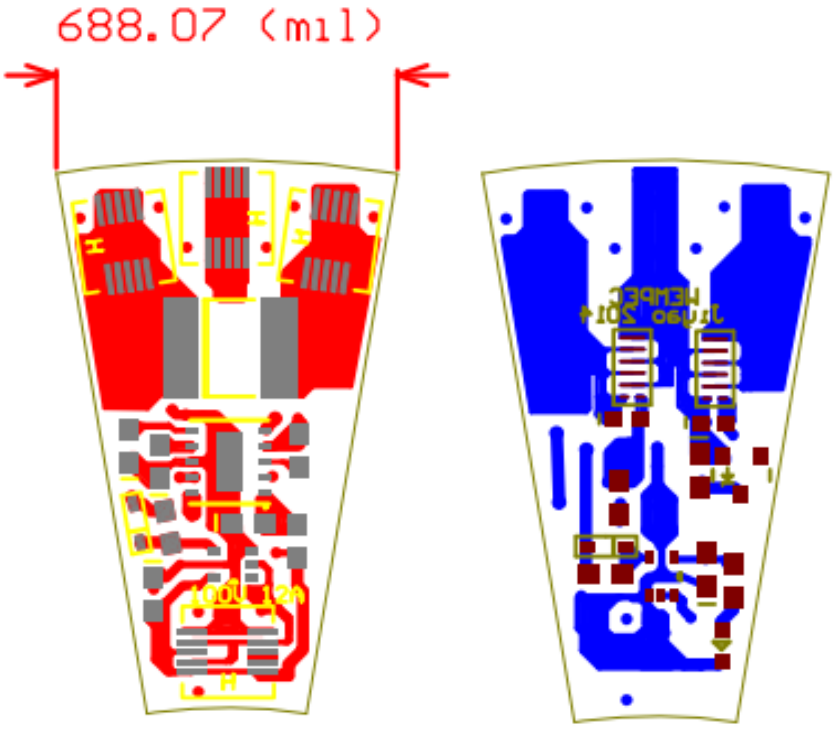


Fig.A.4. Design of single-phase GaN piece

A.2. Hardware Design of 4-Module Multilevel Converter

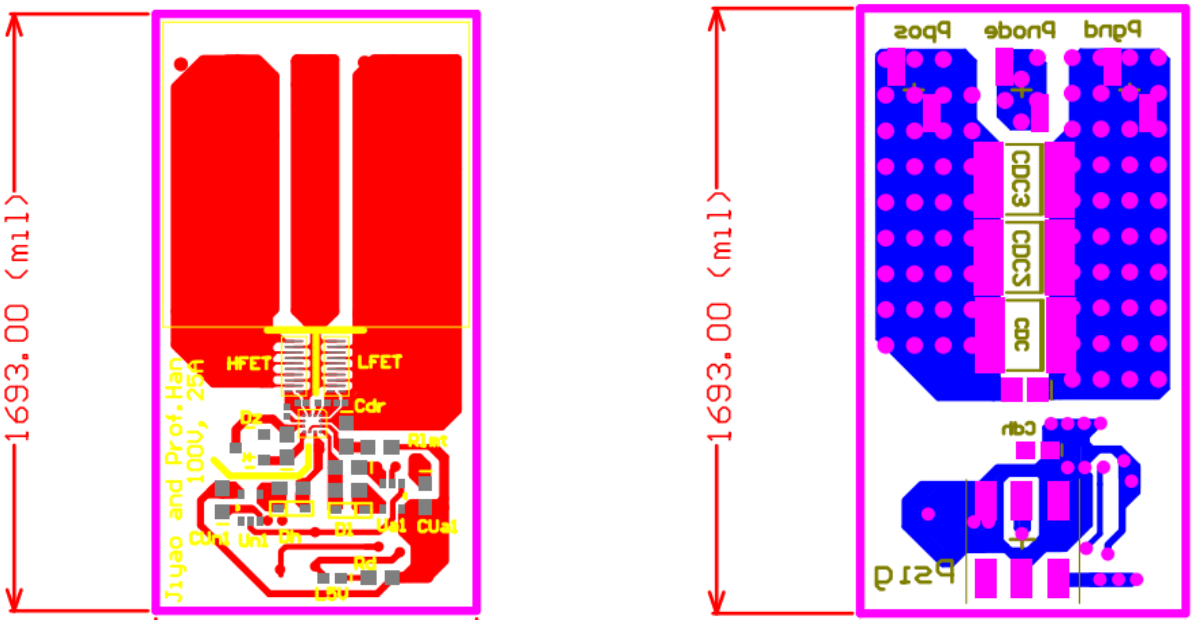


Fig.A.5. Design of single-phase GaN piece

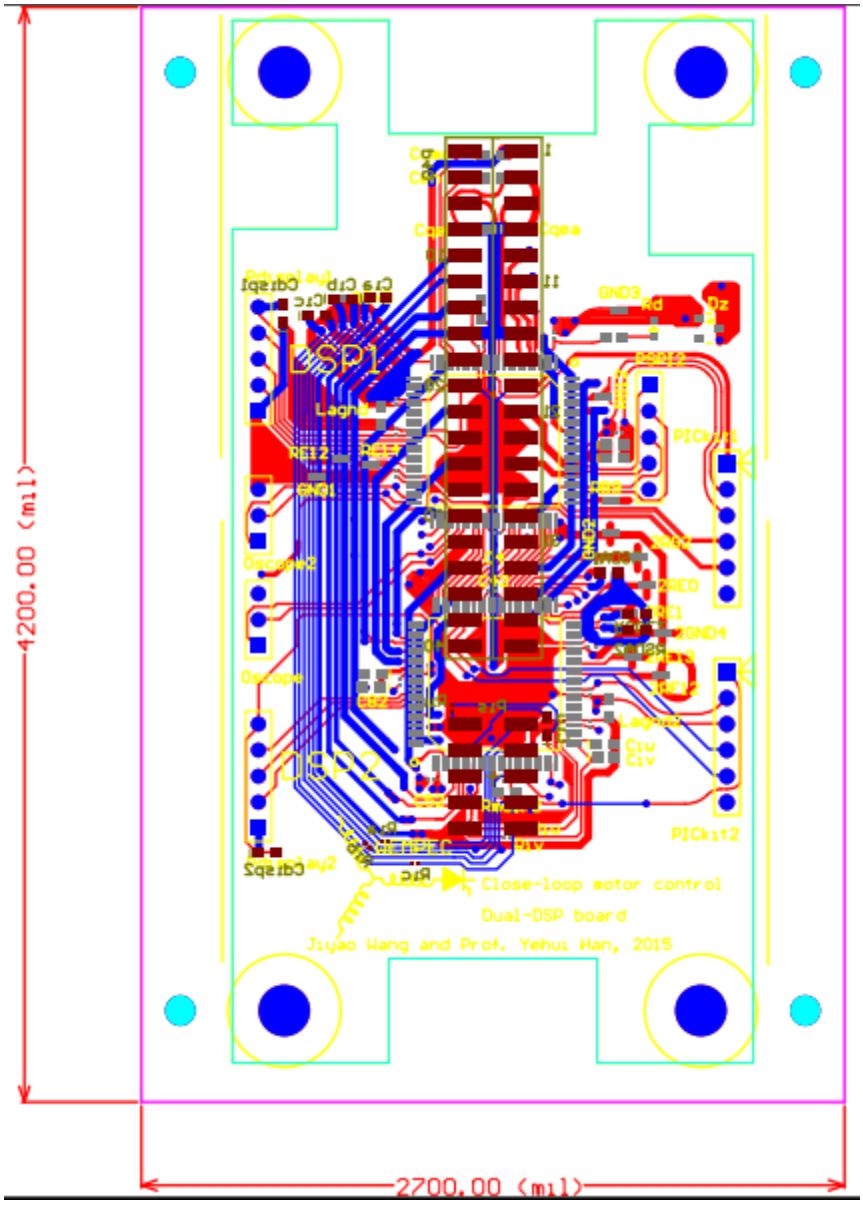


Fig.A.6. Design of dual-DSP controller board excluding middle layers

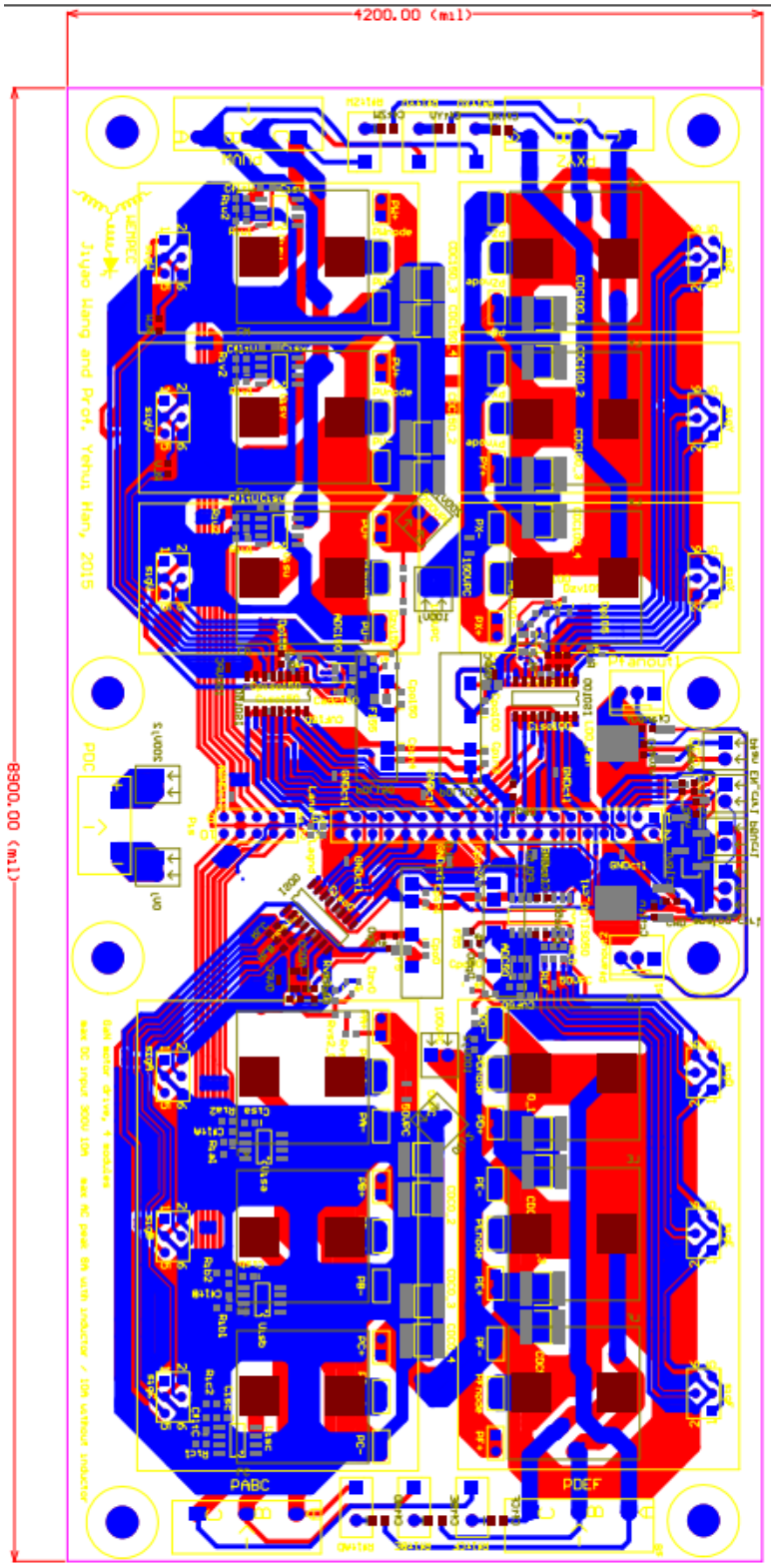


Fig.A.7. Design of multilevel mother board

including connectors, sensors, extra DC-link capacitors, isolators and LC filters

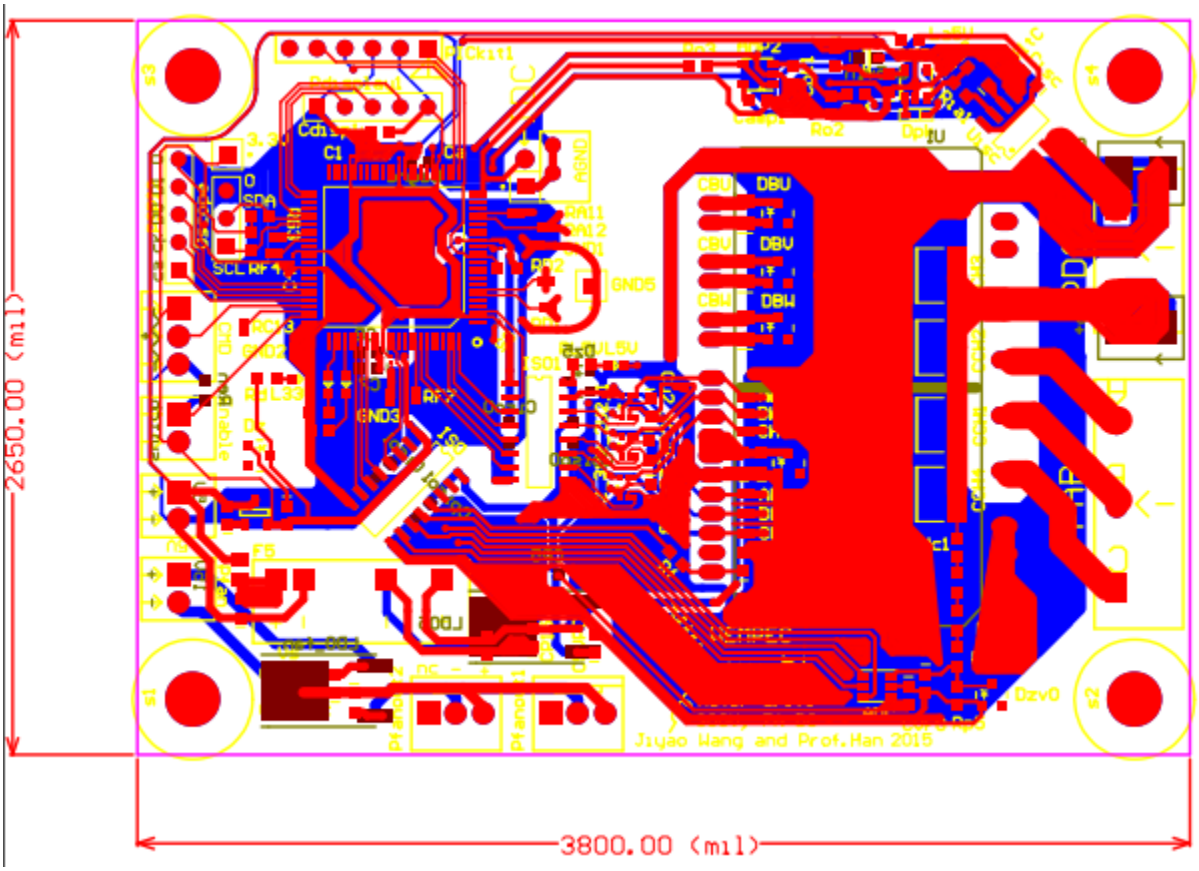


Fig.A.8. Design of prime mover VFD

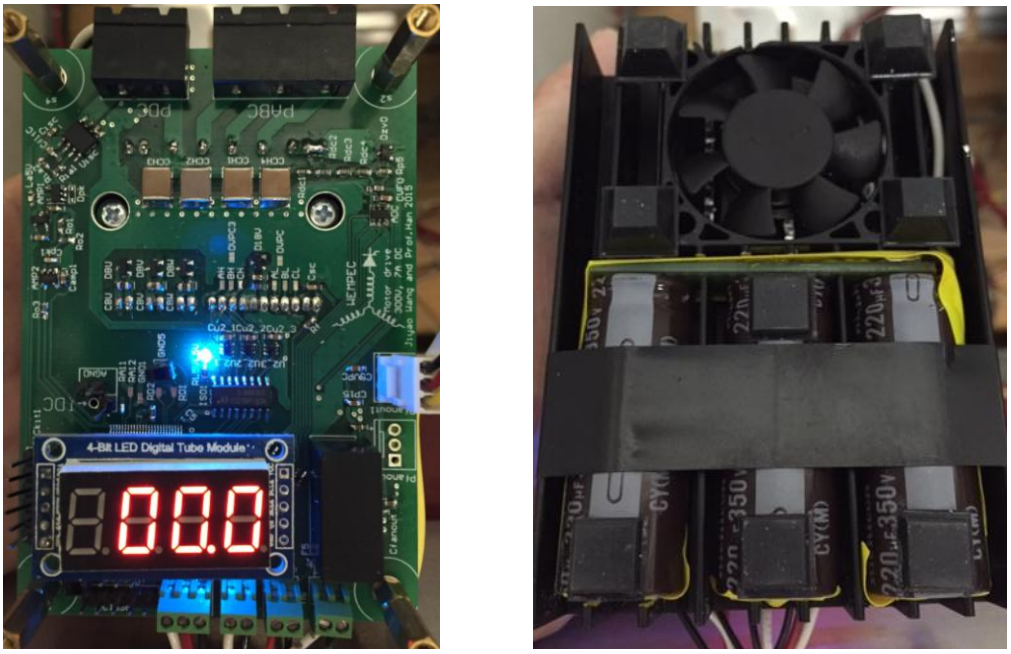


Fig.A.9. Photo of prime mover VFD

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