ULTRAFAST HIGH-VOLTAGE SCHOTTKY VARACTORS FOR NONLINEAR TRANSMISSION LINE TERAHERTZ GENERATION, DETECTION AND SENSING

by

Matthew M Dwyer

A dissertation submitted in partial fulfillment of
the requirements for the degree of

Doctor of Philosophy

(Electrical and Computer Engineering)

at the

UNIVERSITY OF WISCONSIN–MADISON

2017

Date of final oral examination: 06/7/17

The dissertation is approved by the following members of the Final Oral Committee:
Daniel van der Weide, Professor, ECE
Luke Mawst, Professor, ECE
Peter Timbie, Professor, Physics
Scott Sanders, Professor, ME
Felix Lu, Faculty Associate, COE

Acknowledgments

First and foremost, this work would not have been possible without the significant and enduring support of my advisor, Dan van der Weide. Many others have also helped make this work possible. My good friend Kyle for his support and constant encouragement. The WCAM clean room staff for putting up with my mess, questions and odd requests. My fellow clean room users, for empathizing with the unforgiving nature of processing. My labmates, past and present, for always being there to bounce ideas off and vent. Heather and Kyle, without whom I would have never ended up in Madison. My friends, who made my time in grad school so much more enjoyable. And last, but not least, my wife, parents and other family for their steadfast love and encouragement.

Contents

List of Tables

List of Figures

Abstract

Nonlinear transmission lines are monolithic microwave integrated circuits for economically generating ultrafast voltage waveforms with varactor diodes. With applications in high speed sampling and sensing, these circuits are used to convert readily available microwave power into the low-terahertz through the generation of voltage shockwaves. Existing diode designs have focused on cut-off frequency and capacitance modulation without addressing current saturation, a critical limiter of slew rate (voltage/falltime). In this thesis, we introduce optimized high voltage ultrafast double-uniform Schottky diode structures that significantly increase the theoretical slew rate and breakdown voltage. We designed, simulated, and fabricated diode structures and circuits on gallium arsenide, measuring record slew rates. This work highlights a critical design parameter for frequency generating diodes, providing the ground work for large power increases in ultrafast diode-based circuits.

Chapter 1

Terahertz science and technology

The terahertz spectrum, typically defined as 0.3 to 10 terahertz, sits between the two bands traditionally covered by electronics and photonics. Both electronics and photonics provide techniques for generating and detecting terahertz radiation, summarized below.

1.1 Why are we interested in terahertz?

Terahertz technology has slowly gained commercial traction, perhaps most notably in airport body scanners, but has for the most part been confined to science applications. Many spaceborne atoms and molecules have absorption and emission lines in the terahertz band, with 150 discovered by 2011 [1]. Fourier transform terahertz spectroscopy is prevalent in chemistry for studying gases, liquids and solids [1]. Industry leader TeraView has commercialy available terahertz spectrometers and imagers, enabling medical imaging (e.g. skin cancer), explosives detection, noxious gas detection, semiconductor fault analysis, non-destructive imaging, and even art verification. The terahertz technology discussed in this document could be utilized in many of these applications, with significantly reduced footprint.

1.2 Generation and detection methods

Commercial uptake of terahertz technology has been hampered by the lack of appropriate sources, deficient in power and/or compactness. Many sources of terahertz radiation exist and broadly fit into the categories of thermal radiators, vacuum electronic devices, solid state electronics, lasers, and electro-optics.

The first terahertz sources were thermal, including both heated rods and plasma discharge lamps [1]. The globar is the most emissive thermal source, consisting of a silicon carbide cylindrical rod operating at a temperature of 1350 to 1500 K [1]. Lamp sources are most emissive in the lower terahertz band, however also emitting harmful UV radiation.

Vacuum electronic devices encompass backward wave oscillators (BWO), gyrotrons, and klystrons. Very high power levels are achievable, with gyrotrons capable of output power in the hundreds of kilowatts with low duty cycle. BWOs are a popular source of low-terahertz CW radiation with power output on the order of 1 to 10 mW. BWOs have also found use driving solid state multipliers.

Solid state devices range from sub-mm amplifiers and oscillators, to frequency multipliers. Nonlinear transmission lines, the subject of this work, are also classified as solid state devices. Transistors with cut-off frequencies exceeding one terahertz have enabled integrated circuit amplifiers and oscillators covering the low-terahertz region. Multipliers using Schottky or other diodes are typically used in chains to generate CW into the terahertz using microwave sources.

Optically pumped gas lasers have found popular use in terahertz science, producing narrowband CW covering 0.1 to 8 terahertz with power levels up to 100 mW [2]. Quantum cascade lasers (QCL) exploit intersubband transitions in semiconductor heterostructures to generate terahertz radiation at the upper end of the spectrum [2]. Most QCLs require cryogenic cooling, but are capable of relatively high power in both CW and pulsed modes.

Femtosecond optical pulses generated with Ti-sapphire or fiber-loop lasers can be used to excite solid state switches to generate terahertz radiation. A biased photoconductive switch can be used to make a photoconductive antenna, with the

radiated pulses covering a spectrum of 0.1 to 4 terahertz [2]. Many semiconductors can be used, though low-temperature grown GaAs is prevalent. The optical femtopulses can also be driven through a nonlinear crystal, producing terahertz radiation through optical rectification [2].

Terahertz detection is possible with thermal detectors, photodetectors, rectifiers, mixers, and diode samplers [1]. Thermal detectors include the ubiquitous bolometer as well as the Golay cell and pyroelectric detector. Terahertz radiation is converted to heat, which can then be measured. Photodetectors convert photons to electrons, altering the resistance in the semiconductor material. These detectors typically require cryogenic cooling to reduce thermal ionization noise. Rectifiers use diodes to rectify the terahertz signal, producing a proportionate DC component. Mixers down-convert the terahertz signal to a band easily sampled using heterodyne down-conversion. Diode sampling is the technique used in this work and is discussed further in chapter 2.

Nonlinear transmission lines are an economical approach to terahertz generation, and are discussed further in the following chapter.

Chapter 2

Nonlinear transmission line theory

The nonlinear transmission line (NLTL) is a monolithic microwave integrated circuit (MMIC) comprising of a high impedance coplanar waveguide transmission line loaded with shunted Schottky varactor diodes, typically fabricated on gallium arsenide (GaAs). This produces a voltage dependent delay line which compresses the leading negative edge of a waveform to generate a step-like transient shockwave. This shockwave can be differentiated (high pass filtered) to produce a pulse, which can then be used to strobe a sampling bridge. The result is a down converted pulse easily captured by a benchtop oscilloscope.

Much of the initial GaAs NLTL research began with the Bloom group at Stanford in the late 1980s, continuing on at other institutions with former students into the 1990s. The state of the art result by van der Weide [3] produced a 3.5 V (10-90%), 480 fs transient with repetition frequency on the order of 16 GHz, resulting in a spectrum covering the sub-mm/terahertz band. The NLTL sampling head was developed and optimized by Marsland [4], enabling the self-sampling of the 480 fs transient. The Rodwell group also demonstrated strong results, with a 3.7 V (0-100%), 680 fs transient generated using elevated coplanar waveguide transmission lines [5].

Many other groups contributed to the knowledge base of high speed NLTLs [6–13], but no other room-temperature sub-picosecond NLTL transient results were reported to date.

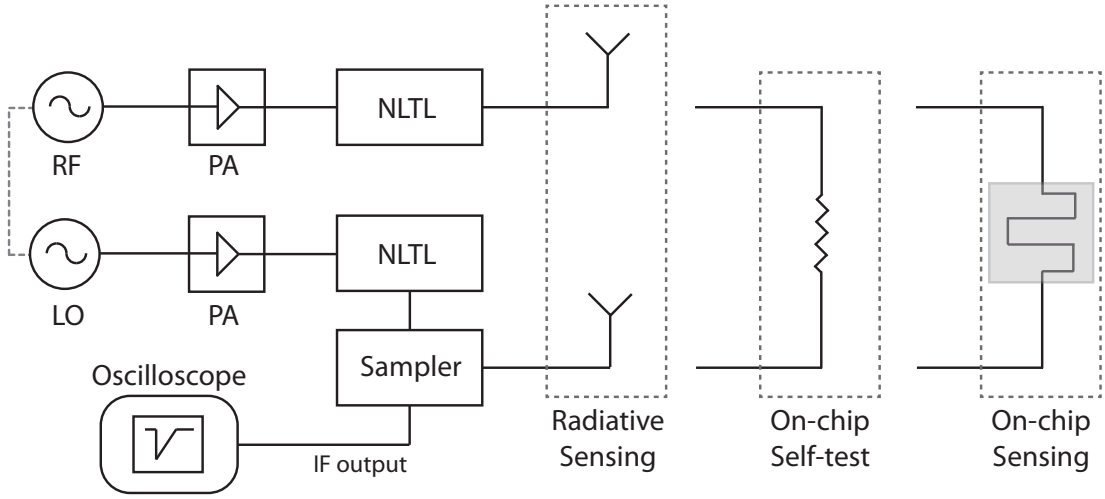

Figure 2.1: NLTL system level diagram.

The NLTL is a passive MMIC, but requires drive electronics to supply the microwave drive signals. Phase-locked synthesizers are typically use to drive transmit and sample NLTLs, offset in frequency to provide a downconverted sampler output. Power amplifiers are required to get the synthesizer output signal up to the 20-35 dBm level needed. The drive signal must stay in the reverse bias range of the NLTL diodes, achieved through either rectification or biasing. The signal generated by the transmit NLTL can be radiated, or driven through an attenuator or sensor, before being sampled, as illustrated in figure 2.1.

2.1 The varactor loaded transmission line

As a periodic struture, an NLTL is made up of cells, with each cell consisting of a high impedance transmission line and a shunt varactor. The circuit diagram and equivalent circuit are given in figure 2.2. Transmission line inductance and capacitance are given by L_l and C_l, respectively. The shunt varactor large signal capacitance and parasitic series resistance are given by C_d and R_s, respectively. The

varactor capacitance is voltage dependent and is the source of nonlinearity. When C_d is written without the voltage dependence, the large signal (average) capacitance is assumed.

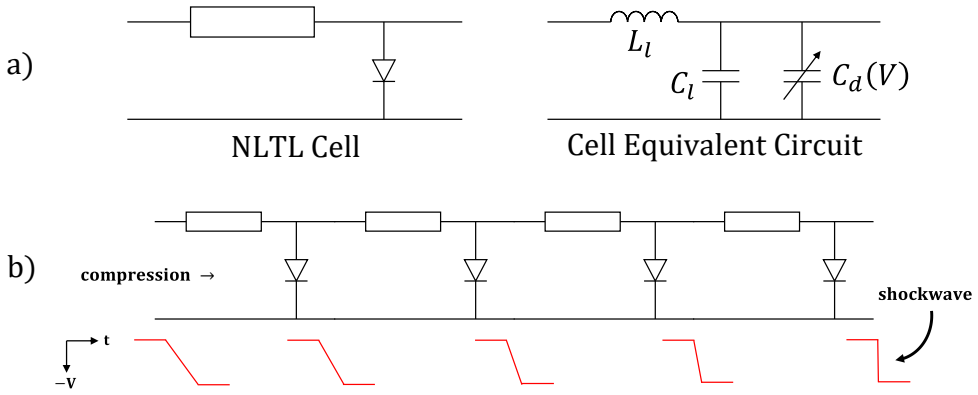

Figure 2.2: (a) NLTL cell circuit diagram and equivalent circuit; (b) Shockwave propagation along circuit.

The ideal cell impedance, Z_{cell}, is given by equation 2.1. In a lossless system, Z_{cell} for every cell could be fixed at 50 Ω. Allen [14] proposed scaling the impedance to counter the line and diode losses, with our implementation discussed in chapter 4.

$$Z_{cell} = \sqrt{\frac{L_l}{C_l + C_d}} \tag{2.1}$$

As C_d is voltage dependent, so too will be the cell impedance. Typically the cell impedance is designed using the average varactor capacitance. The NLTL is fundamentally a voltage dependent delay line. The voltage dependent delay through a cell, T_d, is given by equation 2.2.

$$T_d(V) = \sqrt{L_l \cdot [C_l + C_d(V)]} \tag{2.2}$$

At low negative voltages, C_d is large and thus T_d is large. At high negative voltages, C_d is small and thus T_d is small. As such, high negative voltage travels

through the cell faster than low negative voltage. For a large signal negative waveform, this means the trailing high negative voltage portion will catch up to the leading low negative voltage portion, leading to shockwave formation. The falltime of this shockwave is limited by a number of factors, but the limitation within circuit theory is the cell Bragg frequency f_{Bragg}, given by equation 2.3.

$$f_{Bragg} = \frac{1}{\pi \cdot \sqrt{L_l \cdot (C_l + C_d)}} \tag{2.3}$$

Typically the transmission line length and varactor size are scaled down along the NLTL to increase the f_{Bragg} as falltime decreases. There are limitations, however, as parasitics will dominate for very small cells, limiting any benefit afforded by the higher f_{Bragg}. A faster falltime corresponds to higher harmonic generation, thus an upper limit on harmonic generation also limits the minimum falltime.

2.2 Coplanar waveguide transmission line

GaAs nonlinear transmission lines have almost exclusively used coplanar waveguide (CPW) largely due to easy ground access for the shunted diodes, and also for sampler layout compatibility. Standard 50 Ω lines are simple to fabricate, though higher impedance lines require a narrow center conductor and/or wide signal-ground gaps. High impedance lines can be more easily fabricated by elevating the center conductor using an air bridge process.

The RLGC parameters for standard CPW have been analytically calculated by Heinrich [15], allowing for rapid characterization of any reasonable geometry. The nonideal terms R and G are useful for calculating loss along the NLTL. CPW transmission lines at MMIC geometries suffer from significant radiative losses starting at low-terahertz frequencies [16], but this can be largely suppressed by using narrow ground planes [17].

Elevated CPW (eCPW) transmission lines were successfully used by the Rodwell group, though they found inconsistencies between their measured and simulated LC parameters. No analytical solution exists for eCPW lines, requiring 2D or full-

wave simulation for characterization. The use of eCPW in these NLTLs prompted other groups to characterize this type of transmission line. Schnieder et al [18] found that Sonnet's method of moments solver matched measurements better than their in-house finite difference code. We simulated their test structure and found that CST closely matched their measurements. Hofschen et al [19] also published eCPW measurement results, which we found also matched our CST simulations.

2.3 Schottky diode varactors

NLTLs use Schottky diodes almost exclusively, largely due to their high cut-off frequency (compression) and fast switching speed (sampling). A Schottky contact is formed by a metal-semiconductor junction where the metal work function exceeds the n-type semiconductor work function (opposite for p-type). Schottky diodes for high speed NLTLs use n-type doping due to electron mobility exceeding hole mobility in typically used materials, especially GaAs. High electron mobility provides lower parasitic resistance as discussed below. The Schottky diode is a conductor in forward bias and variable capacitor (varactor) in reverse bias.

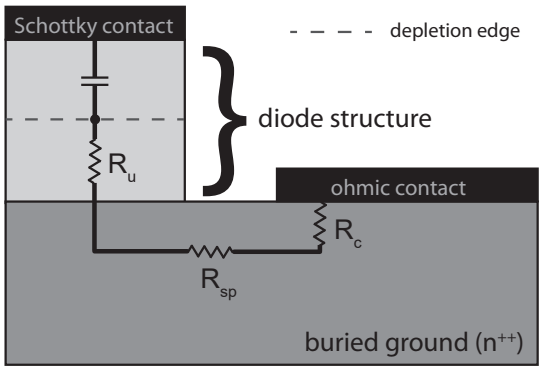

Figure 2.3: Schottky diode structure showing capacitance and parasitic resistance.

The complete planar Schottky diode consists of the metal-semiconductor Schottky contact, the diode structure, the buried ground, and the metal-semiconductor

ohmic contact, shown in figure 2.3. The diode structure largely determines the varactor characteristics and is the main contributor to total parasitic resistance for small geometries.

The Schottky diode is a capacitor in reverse bias as carriers are extracted, or depleted, from the so called depletion region (denoted by the capacitor in figure 2.3), leaving a high-resistivity region that effectively forms a parallel plate capacitor with electrodes at the Schottky junction and at the depleted-undepleted junction. This capacitance is variable due to more carriers being extracted with increasing reverse bias, thereby increasing the thickness of this capacitor dielectric, thus reducing the capacitance. This capacitance-voltage relation is referred to as the CV curve.

An important metric for NLTL Schottky diodes is the cut-off frequency, given by equation 2.4. C_d is the large signal (average) diode capacitance and R_s is the parasitic diode resistance.

$$f_c = \frac{1}{2 \cdot \pi \cdot R_s \cdot C_d} \tag{2.4}$$

A 'fast' Schottky diode implies a high f_c, typically on the order of terahertz. Beyond a few terahertz, plasma frequency effects come into play [20]. However, the harmonic content of even the fastest NLTLs fall below the plasma frequency, so this simple figure of merit remains useful. One can infer from a very high f_c that performance at lower frequencies will be better than for a lower f_c diode.

The CV curve and breakdown voltage are functions of the diode structure thickness and doping. The diode structure thickness is typically designed to be fully depleted at the maximum operating voltage. Avalanche is the typical breakdown mechanism with NLTL Schottky diodes due to the lower diode structure doping, occurring when the electric field in the depletion region exceeds a critical value. This critical electric field (E_c) increases with doping, though the electric field increases more slowly for lower doping as increasing reverse bias is accompanied by more depletion than for higher doping.

Uniform doping is the most simple doping profile with capacitance proportional to $1/\sqrt{V}$. This structure was used in the final stages of both sub-picosecond NLTLs, with varying doping [3, 5]. The hyperabrupt profile grades the doping down from

the Schottky interface towards the buried ground, extending the CV curve to higher voltages. It was popular in NLTL design but didn't produce a sub-picosecond transient, likely due to higher resistance of the progressively lower doped undepleted region and current saturation. Delta doping places a thin highly doped layer near the Schottky interface to limit the zero bias depletion, increasing the capacitance modulation ratio. This delta layer can be etched away to give a low capacitance diode suitable for sampling and the final sections of an NLTL. This structure was used in the fastest NLTL to date, generating a 480 fs, 3.5 V transient [3].

2.4 NLTL sampling

Marsland [4] developed the high performance NLTL sampler that was later used to down-convert van der Weide's 480 fs, 3.5 V transient [3]. The sampler uses the step-like transient generated by an NLTL to strobe a diode sampling bridge. The strobing transient is transformed from a CPW mode to a coplanar stripline (CPS) mode by coupling the center conductor of the CPW to the farside ground of the test signal CPW using an airbridge and capacitor. The capacitor acts as a high pass filter on the strobe signal, turning the step-like function into a pulse. This pulse will strobe the diode bridge every cycle, with the turn-on aperture on the order of the transient falltime. When the sampler NLTL frequency is offset from the test NLTL frequency by some intermediate frequency (IF), the sampler output is then a downconverted replica of the test NLTL transient repeating with frequency IF.

2.5 NLTL-compatible antennas

The wide bandwidth transient and 50 Ω drive impedance of an NLTL limit antenna choices. Slot antennas provide limited bandwidth though have found use in some designs, with bandwidth centered at around 300 GHz [21]. Perhaps the most popular NLTL antenna is the venerable bow-tie with its largely frequency-independent input resistance. By varying the bow angle, the input resistance for a bow-antenna on GaAs can be swept from over 200 Ω to under 50 Ω [22]. These

antennas are typically coupled with a high resistivity silicon lens to collimate the radiation. This is especially useful for the bow-tie antenna as it has a null on bore-sight. Scaled measurements of the bow-tie antenna [21] gave an input impedance closer to 40 Ω, suggesting this would be more appropriate NLTL impedance for radiative applications.

Chapter 3

Double-uniform Schottky diode

Subpicosecond compression NLTLs to date have been limited in voltage to around 3.5 V [3, 5]. Higher voltage NLTLs have been limited in compression due to diode parasitic series resistance and thus low cutoff frequency. To design an optimal varactor diode we first broke down the design parameters and their effect, listed in table 3.1. Diode structures were simulated in Silvaco using the Atlas and DevEdit tools.

Design Parameter	**Effect**
Capacitance density (fF/μm^2)	f_c
Series resistance (Ω-μm^2)	f_c
Capacitance modulation ratio	Efficiency
Capacitance modulation voltage range	Voltage range
Reverse breakdown voltage	Voltage range
Depletion edge velocity saturation	Falltime
Current saturation	Slew rate

Table 3.1: Schottky diode design parameters and effects.

Low capacitance and low series resistance combine to give a high cut off frequency f_c, ensuring most of the transient voltage falls across the capacitance and not the parasitic resistance. High capacitance modulation ratio ensures sufficient nonlinearity to efficiently compress the waveform, but is not as critical for distributed

NLTLs versus, for instance, single varactor multipliers. Capacitance modulation over a large voltage range is critical to fully utilizing the entire usable voltage range, requiring a non-uniform doping profile. High reverse breakdown voltage requires understanding and managing electric fields within the diode structure. Avoiding depletion edge velocity saturation requires restricting the distance of the depletion movement. Current saturation limits the slew rate (voltage/falltime) of the transient and is especially critical as the capacitance-modulating voltage range is increased.

The diodes used in the final section of the fastest NLTL to date [3] were uniform low doped, with 260 nm active region thickness. The low doping caused the diode to be half depleted at zero bias, giving very low capacitance. However, the remaining active region had relatively high resistance and fully depleted at a little over 3 V. This diode was used as the base structure for the optimal NLTL diode. Our goal was to create a diode as fast as [3], but operating over double the voltage range.

3.1 Current and electron velocity saturation

Current saturation occurs when the diffusion current (i_d) induced by the transient through the depleted capacitive region cannot be matched by the conduction current (i_e) through the resistive undepleted region. If the conduction current cannot match the diffusion current, the effective resistance of the conduction region will increase.

The equations for diffusion and maximum conduction current are given by 3.1 and 3.2, respectively [23]. These currents are illustrated in figure 3.1.

$$i_d(t) = C'_d \cdot A_d \cdot \frac{dV_d(t)}{dt} \tag{3.1}$$

$$i_e^{max} = A_d \cdot n_e \cdot v_e(t) \cdot e^- \tag{3.2}$$

C'_d is the diode capacitance per unit area, A_d is the diode area, $\frac{dV_d(t)}{dt}$ is the voltage slew rate, n_e is the donor doping, $v_e(t)$ is electron velocity and e^- is the charge of an electron.

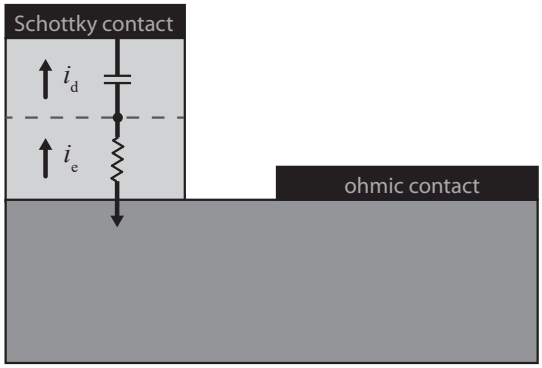

Figure 3.1: Schottky diode structure with diffusion and conduction current.

The electron velocity is a time dependent quantity with peak values on the order of $4 \cdot 10^7$ cm/s for fast transients, but a fraction of that in steady state, though this is highly electric field dependent [24].

Our approach was to assume electron velocity consistent with the state of the art [3], which was also consistent with reported simulated results [25]. We pursued increasing the slew rate by decreasing capacitance and increasing doping through the use of a double uniform doped diode structure. For moderate electric fields, measurements suggested that for doping within our range of interest, electron velocity is fairly comparable [26].

At very high electric fields, velocity slowly but steadily decreases from $8 \cdot 10^6$ cm/s to $6 \cdot 10^6$ cm/s for 50 to 200 kV/cm fields, respectively [27]. However, steady state results do not apply as readily to NLTLs, with short timescales and distances, where transient responses are more relevant.

Silvaco simulations indicate peak electric fields in the undepleted region on the order of 10 to 50 kV/cm. Transient velocities over short distances and timescales were explored with Monte Carlo simulations by [25], finding peak electric fields much greater than steady state. For the 480 fs / 3.5 V transient in [3], solving the i_d/i_e equations gives an electron velocity on the order of $4 \cdot 10^7$ cm/s. This significantly exceeds the steady state GaAs saturated electron velocity of $0.8 \cdot 10^7$

cm/s, but is fully consistent with these Monte Carlo transient simulations.

3.2 Double-uniform diode structure

A double-uniform (DU) structure comprising a 150 nm low-doped zero-bias-depleted region and an equally thick capacitance-modulating moderately-doped region formed the basis of our diode design. A double-uniform doping structure had been proposed before [28], but with markedly different doping and thicknesses which did not address the requirements of an ultrafast NLTL diode. For our diode structure, a low-doped zero-bias-depleted region ensured low capacitance, while the moderately-doped capacitance-modulating region was optimized to meet the other criteria defined above. By increasing the doping in the capacitance-modulating region, the CV curve was extended to higher voltages while also accommodating a higher slew rate. Parasitic series resistance was also reduced in the undepleted region compared with the state of the art [3] due to the higher doping. The capacitance-modulating region was originally doped hyperabrupt (exponential) which would linearize the CV curve at the expense of slew rate. Uniform doping was ultimately chosen due to the simplified epitaxial growth and slew rate improvement.

The double uniform diode structure is illustrated against existing structures in figure 3.2. Breakdown voltage was expected to exceed 10 V, based on past reported measurements of similarly sized and doped diodes.

3.3 Capacitance-voltage curve optimization

With the structure thicknesses set, the doping was then varied to study the effect on capacitance with changing voltage. The low-doped depleted region was doped $4 \cdot 10^{16}$ cm^{-3} to ensure full depletion at zero-bias, but no lower to minimize parasitic resistance in forward operation (sampling).

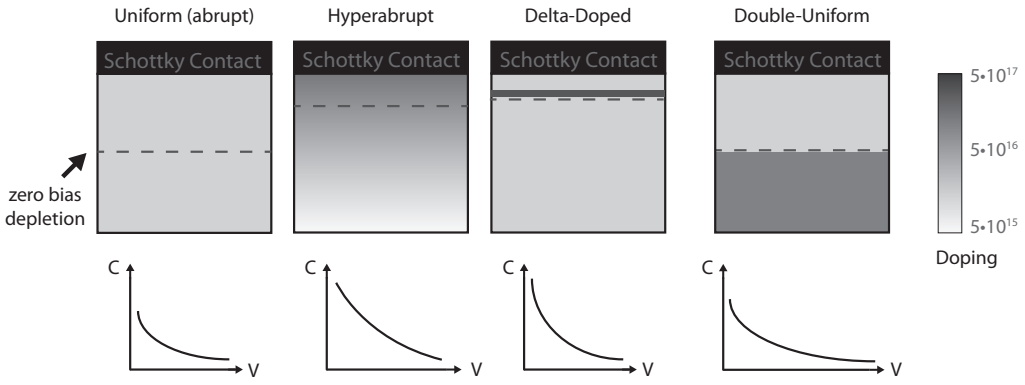

Figure 3.2: Double-uniform compared with existing diode structures.

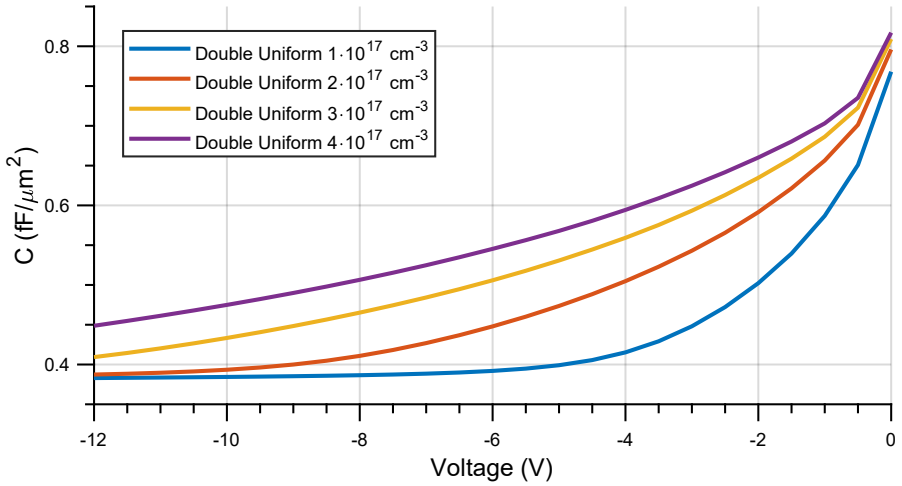

Figure 3.3: Double-uniform diode CV simulation with varying capacitance-modulating region doping.

A doping concentration of $2 \cdot 10^{17}$ cm^{-3} provided capacitance modulation over more than 8 volts, with sufficient buffer before reverse bias breakdown. This was considered the optimal doping for this structure. Higher doping risked operating the diode too close to breakdown voltage. Lower doping could be used for a

sampling NLTL where high peak amplitudes are not critical.

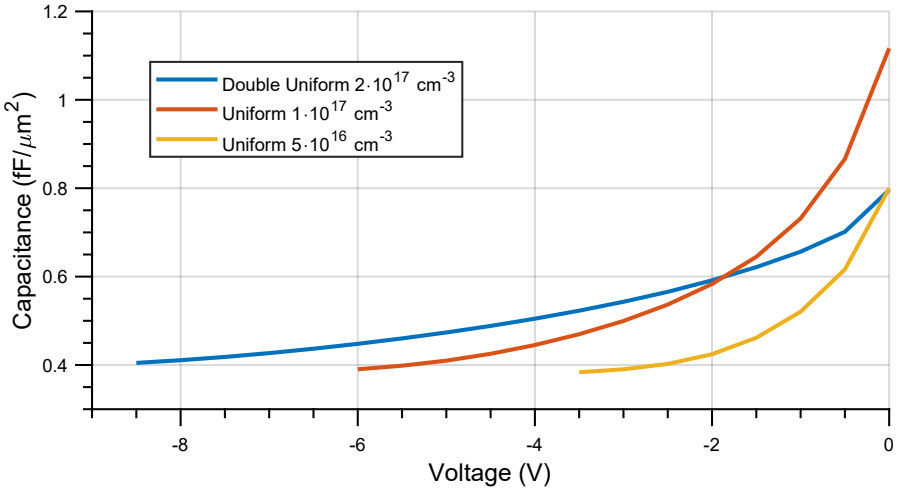

Figure 3.4: Double-uniform versus uniform diode CV simulation.

Figure 3.4 compares the CV curve of this optimal double-uniform diode with uniform diodes used in reported sub-picosecond NLTLs. The double-uniform structure had the same capacitance range as the $5 \cdot 10^{16}$ cm^{-3} uniform diode, just extended from under 3 V to 8 V. The higher doped $1 \cdot 10^{17}$ cm^{-3} uniform diode did however provide a higher capacitance modulation ratio of almost 3 to 1, versus 2 to 1 for the other diodes.

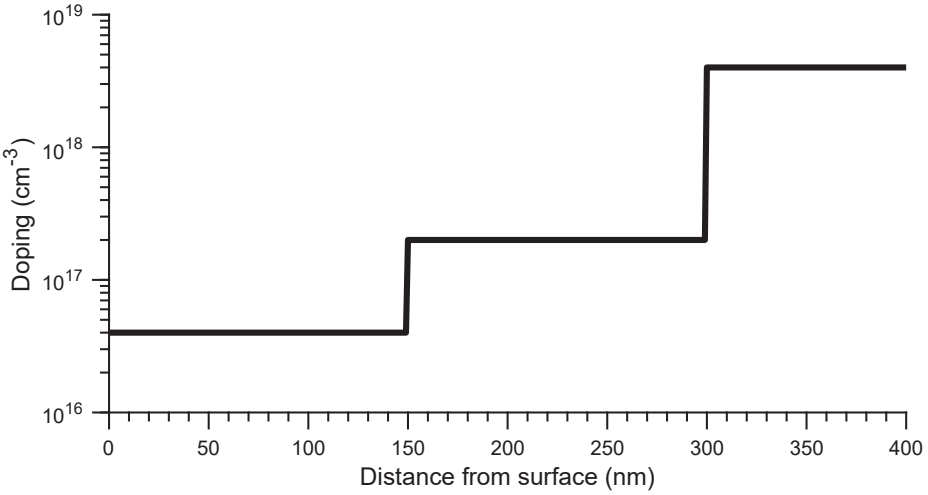

Figure 3.5: Optimized double-uniform structure doping.

The doping and thickness of this optimal diode structure is graphed in figure 3.5. The buried ground would typically extend 1 μm or more to lower spreading resistance.

3.4 Parasitic resistance and cut-off frequency

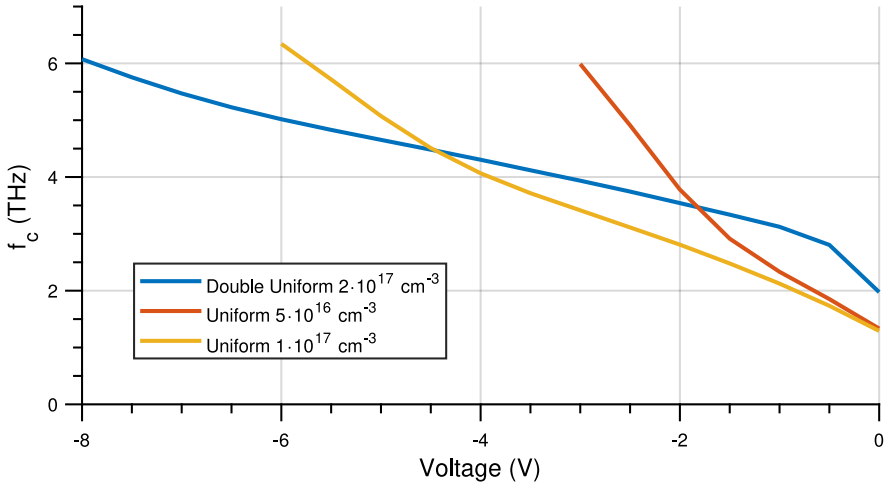

Figure 3.6: Simulated cut-off frequency for 2 μm wide diodes.

The cut-off frequencies of the uniform diodes compared favorably. However, the double-uniform diode showed increased cut-off frequency at lower bias (figure 3.6). This was due to the low zero bias capacitance combined with the higher doping in the undepleted region, and would enable a fast, low-loading sampling diode.

3.5 Epitaxial growth and diode measurements

GaAs epitaxial layers are typically grown with either metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). MBE usually gives tighter doping control, though modern MOCVD systems can produce comparable accuracy. This work used MOCVD grown material supplied by the Mawst group (UW-Madison) and MBE grown material supplied by commercial vendor IntelliEpi. In addition to the diode epitaxial structure, buffer and etch stop layers were grown to aid processing. The buffer layer reduces defects on the wafer surface and the etch stop allowed the controlled removal of device layers for device isolation. Lattice

matched InGaP was used as the etch stop, though AlGaAs could also have been used. Semi-insulating GaAs wafers were used, providing a low loss microwave substrate.

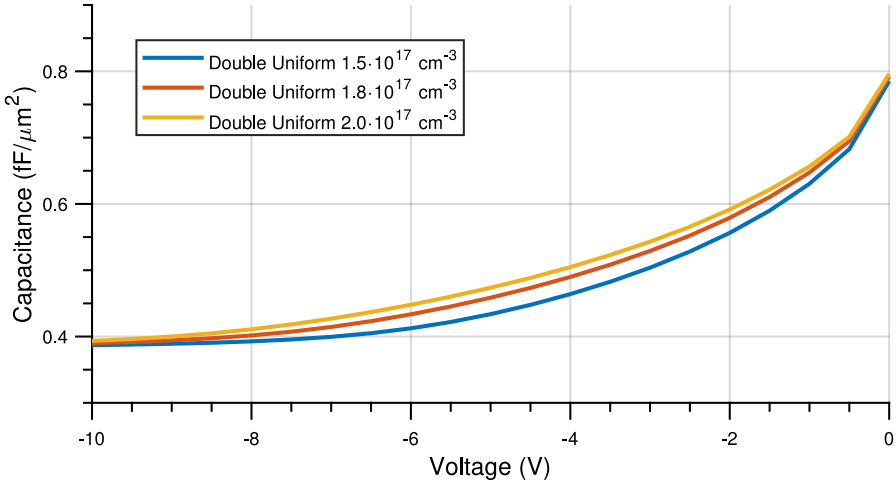

Figure 3.7: Simulated CV curves for the IntelliEpi doping range specification.

After a discussion of doping accuracy capabilities with IntelliEpi, we ordered material with the critical capacitance modulating doping specified as $1.8 \cdot 10^{17}$ cm^{-3}, but within the range of 1.5 to $2 \cdot 10^{17}$ cm^{-3}. Figure 3.7 shows that any doping within this range would still provide a useful CV curve.

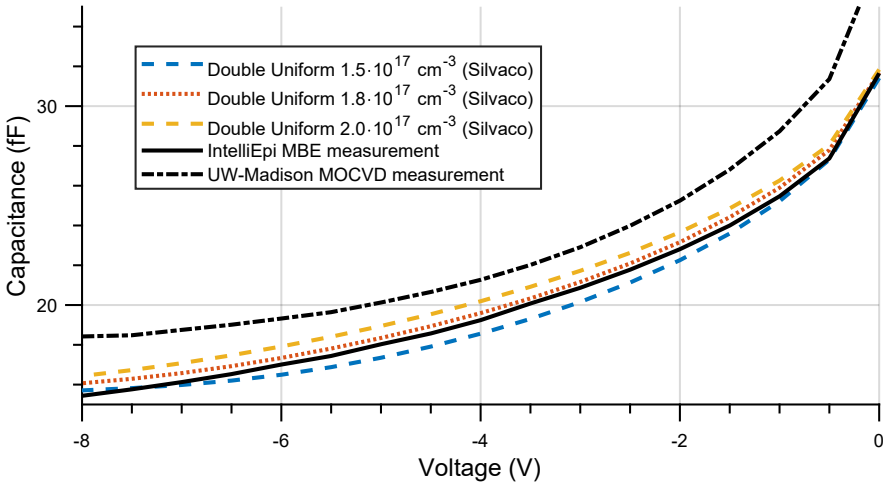

Figure 3.8: Measured vs. simulated capacitance for a 200x200 μm^2 diode.

Large 200 x 200 μm^2 diodes were fabricated on both MBE and MOCVD epitaxial samples following the process in chapter 5, and measured with a Keithley 540 CV Analyzer. These measurements are plotted in figure 3.8 against the specification provided to IntelliEpi. The MBE material closely matched the $1.8 \cdot 10^{17}$ cm^{-3} doping simulation. The MOCVD material region thicknesses were likely 10 to 15% below the specification, resulting in increased capacitance across the voltage range.

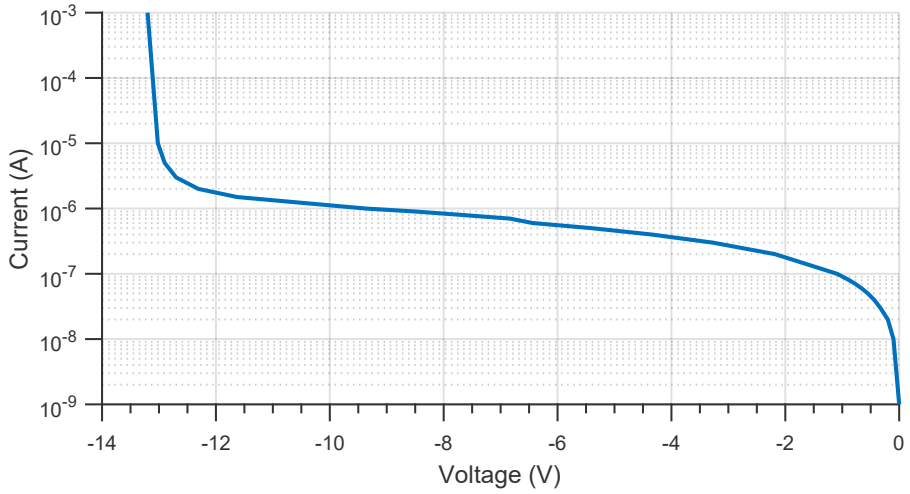

Figure 3.9: Leakage current and breakdown voltage for a 10x10 μm^2 diode.

Leakage current of a 10x10 μm^2 diode on MBE-grown material was characterized with a Keithley 220 current source, stepping through current levels and measuring voltage (figure 3.9). The breakdown voltage of around 13 V was consistent with expectations.

Chapter 4

Nonlinear transmission line design and simulation

The NLTL generation code was implemented in MATLAB, using an excel spreadsheet as the database. The circuit design process was recursive, calculating each subsequent cell's parameters using compression and loss data of the cell before. The wavefront compression of each cell was approximated using the Expand-Compress method detailed by Rodwell [29].

Coplanar waveguide characterization

Elevated CPW (eCPW) enables high impedance transmission lines with reduced parasitics due to the lower signal-ground gap requirement. As discussed in chapter 2, there was some disagreement between simulation and measurements within the literature. In particular, Allen [5] found that their simulated line capacitance was around 20% lower than measurements. Our CST simulations of those test structures also gave similarly conflicting results. However, our CST simulations were consistent with other reported results [19].

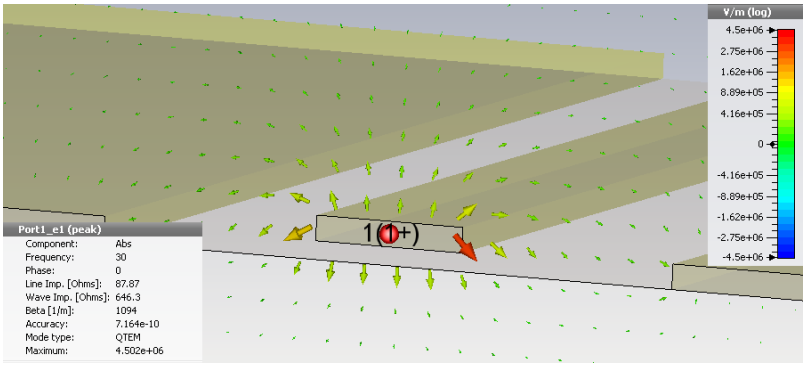

Figure 4.1: Elevated CPW geometry simulated in CST Microwave Studio.

The geometry of the elevated CPW is shown in figure 4.1. The line impedance and β were used to extract the LC line parameters.

Cells	Width (μm)	Gap (μm)	Height (μm)	Z (Ω)	L (H/m)	C (F/m)
1-32	20	26	2.3	88	5.2e-7	7.37e-11
33-63	12	18	2.3	96	5.1e-7	6.05e-11
64-100	6	10	2.3	102	4.6e-7	4.84e-11

Table 4.1: Elevated CPW simulated parameters.

Ultimately we chose three different eCPW geometries, outlined in table 4.1. The geometry was made smaller along the NLTL which reduced both the capacitance and inductance per unit length, increasing the cut-off Bragg frequency. The height of the center conductor was determined by the thickness of photoresist in our air bridge process, discussed in the following chapter.

Scaled test structures were machined from aluminum, fitted with connectors, and mounted on stycast (e_r ~12), but the line impedance measurements were unreliable and ultimately discarded.

Recursive NLTL cell design

The NLTL circuit was designed recursively, with the parameters of each cell calculated using the impedance and compression of the previous cell. The cell impedance was first calculated using the impedance of the previous cell and the loss in the previous cell (equation 4.1).

$$Z_{cell} = Z_{cell-1} \cdot exp(loss_{cell-1}) \tag{4.1}$$

The cell loss is given by sum of the diode loss and transmission line loss, given by equation 4.2 [30].

$$loss_{cell-1} = \frac{1}{2} \cdot (2 \cdot \pi \cdot f \cdot C_d)^2 \cdot R_s \cdot Z_{cell-1} + \frac{R_l}{2 \cdot Z_{cell-1}} \text{ [Np/m]} \tag{4.2}$$

Next, the transmission line length and diode area were calculated by simultaneously solving the equations for Z_{cell} and f_{Bragg}. f_{Bragg} was set as a function of the waveform falltime entering the cell. The waveform falltime was calculated using the Expand-Compress method [29]. The MATLAB *solve* function was used to solve equations 4.3 and 4.4 for diode area and transmission line length.

$$\sqrt{\frac{length \cdot L'_{cell}}{length \cdot C'_{cell} + area \cdot C_d}} = Z_{cell} \tag{4.3}$$

$$\frac{1}{\pi \cdot \sqrt{length \cdot L'_{cell} \cdot (length \cdot C'_{cell} + area \cdot C_d)}} = f_{Bragg} \tag{4.4}$$

This process was repeated for a set number of cells, after which the NLTL circuit parameters and predicted performance could be evaluated.

The free SPICE software LTspice was used to simulate the NLTL circuits and gave falltimes consistent with the analytical design values. The tee attenuator was simulated in Sonnet Suites with a target attenuation of 26 dB.

4.1 Final design values

The final design values for the double-uniform NLTL are listed in table 4.2. These values were chosen through a manual iterative process, optimizing for falltime and ease of fabrication. Keeping the cell impedance low allowed a higher Bragg frequency within the minimum diode size constraint.

Number of cells	100
Input Impedance	20 Ω
Output Impedance	35 Ω
Smallest individual diode	7 μm^2
Output f_{Bragg}	943 GHz
Predicted loss	5.5 dB
Small signal compression	42 ps
Large signal compression	24 ps
Drive frequency	10 GHz
Input falltime	25 ps
Predicted output falltime	770 fs

Table 4.2: Final NLTL design values.

Chapter 5

Fabricated NLTL circuits

This work required the complete development of a monolithic microwave integrated circuit fabrication process specific to the tooling available in the Wisconsin Center for Applied Microelectroncs (WCAM).

5.1 Fabrication overview

The process for fabricating NLTLs was loosely based on recipes used at Stanford for similar devices over twenty years ago. While most processing steps were similar, the specifics of each step required significant optimization or modification for the equipment available in WCAM, and the target dimensions.

Processing started with the growth of the epitaxial diode structure as outlined in chapter 3. Alignment marks were etched into the substrate, along with vernier marks to validate alignment of subsequent layers. Ohmic contacts were deposited after etching the diode structure, and then rapidly annealed. Schottky contacts were deposited, after which the mesas were etch isolated. The interconnect metal was deposited. The sample was then coated with PECVD silicon nitride, with openings then etched. Finally, the air bridge process produced the final metalization to complete the circuits.

Photolithography

NLTL fabrication has traditionally employed contact lithography, with ebeam patterning at times used for sampling diodes [14]. The relatively small feature sizes demanded by NLTLs (on the order of a micron) push the limits of contact lithography, and the number of masks required becomes a significant expense. WCAM's step and repeat tool, a Nikon i-line stepper, was chosen for this MMIC process as it enabled 0.5μm feature size, better than 100 nm alignment accuracy, and required only one 6" reticle for an 8 to 12 layer design. The stepper was more tolerant of varying topography (resulting from etch-isolated mesas) and did not require edge bead removal. However, to achieve the alignment specification, each layer required an offset measured with vernier fiducials to overcome systemic tool misalignment. Wafers were scribed and broken into quarters, and then mounted on a carrier wafer with a small drop of water. After a short bake, the sample was cemented to the carrier and fully compliant with the stepper's wafer handling and alignment systems. The sample was easily removed post-exposure by dousing with water to break the bond.

AZ 5214e was used in image reversal mode for all metal lift-off steps. The same resist was used in positive mode for all other steps except electroplating, where thick AZ 12XT-05 was used.

Alignment marks

Alignment marks were etched into the GaAs substrate using the anisotropic isolation etch discussed later. Evaporated titanium alignment marks were also successfully used, but required more processing effort. Etching allowed very deep alignment marks, beneficial for contrast after subsequent deposition steps, including silicon nitride and electroplating seed metal. Shallow alignment marks, on the order of 50 nm, were found to be unusable after seed metal deposition, though generally 100 nm was sufficient.

Ohmic contacts

Low resistivity ohmic contacts are critical to achieving the best performance from NLTLs. Poor ohmic contacts significantly reduce the diode cut-off frequency through increased parasitic series resistance. The most common metallization is gold germanium nickel (AuGeNi) [31], forming a AuGe eutectic, though poor edge definition results after rapid thermal annealing, and contact resistance spread can be large. Alternatively, solid state (non-eutectic) contacts using palladium germanium (PdGe) metallurgy provide contact resistance comparable to AuGeNi but with lower contact resistance spread and good edge definition. Ivey [32] achieved contact resistance below $5 \cdot 10^{-7}$ Ω-cm^2 using a variety of PdGe metal stacks with Pt/Au caps.

We were not able to replicate the PdGe contact resistances reported, so we ultimately chose the venerable AuGeNi contact. We used a graphite susceptor to evenly distribute the heat when rapid thermal annealing at 400 °C for 60 s. We routinely achieved a contact resistance of $< 0.03\Omega/\mathrm{cm}$, corresponding to a contact resistivity of approximately $1 \cdot 10^{-6}$ Ω-cm^2. The contact resistance was consistent with previously reported results [3].

Ge	110	Å
Au	100	Å
Ge	60	Å
Au	240	Å
Ni	50	Å
Au	160	Å

Table 5.1: AuGeNi ohmic contact metal stack.

The ohmic contact metal stack used in this work is listed in table 5.1, borrowed from an existing NLTL fabrication recipe. Au and Ge were deposited separately as a AuGe alloy crucible was not available. Regardless, depositing separately avoided issues with maintaining correct elemental ratios due to differing vapor pressures.

The diode structure layer was removed using dilute phosphoric acid and hydrogen peroxide, etching approximately 400 nm in 90 s.

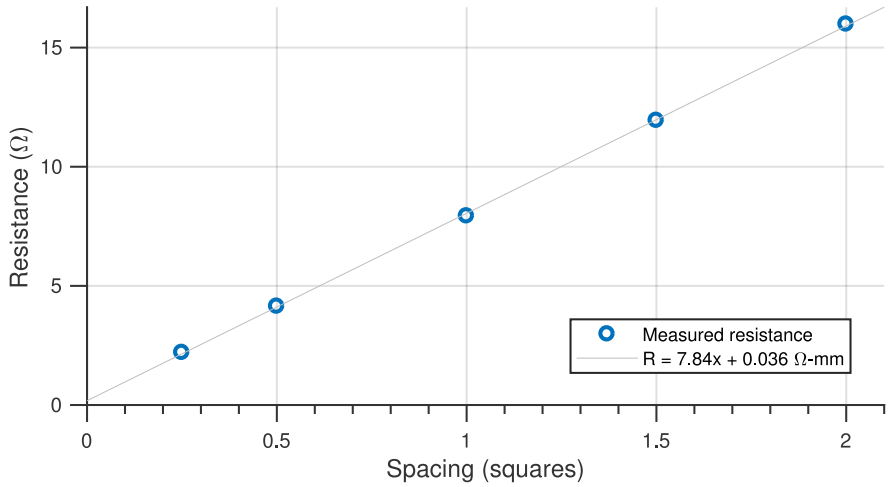

Figure 5.1: TLM contact resistance measurements and resistivity.

Contact resistance was measured with the transmission line method (TLM) using 200 µm wide pads spaced at varying distances, and then extrapolating to zero distance (figure 5.1). Resistance was measured by supplying a known current with one set of probes, and measuring the resultant voltage with another set of probes. This standard four point probe technique removed the effect of probe and probe-contact resistance.

Schottky contacts

The standard Schottky contact metal stack to GaAs is titanium / platinum / gold (Ti/Pt/Au). Ti provides adhesion and Pt prevents Au from diffusing into GaAs at higher temperatures. The amount of Pt needed is minimal, with a Skyworks paper citing 10 nm for practical pinhole-free coverage [33]. Unless the GaAs surface is treated prior to Schottky metal deposition (i.e. with $(NH_4)_2S$ [34]), the fermi level will be pinned. As such the Schottky barrier height will be largely independent of

the contacting metal [31]. In this work we typically deposited 30 nm Ti, 20 nm Pt, and 150 to 300 nm Au.

Resistors and attenuator

Resistors, and attenuators by extension, used the grown epitaxial structure with resistivity of roughly 7 Ω/□. These semiconductor resistors were contacted using ohmic contacts and required no special processing steps.

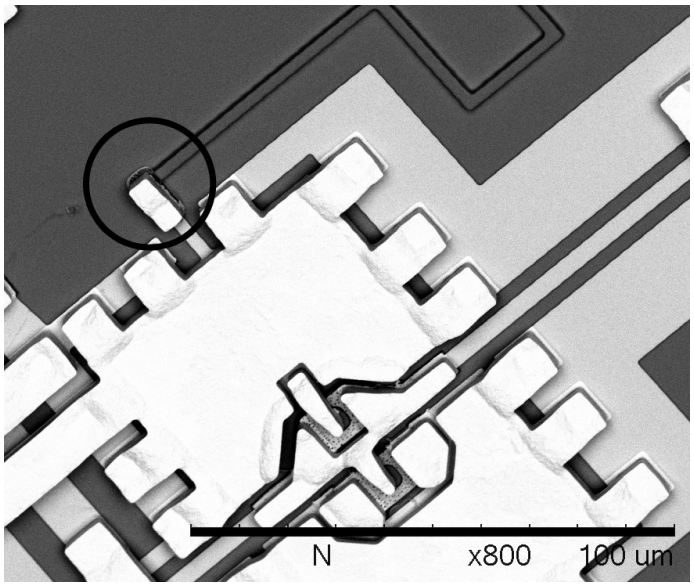

Figure 5.2: Failed GaAs sampler resistor. Note the encircled dark area between the line and the thick plated metal, indicating an open circuit.

An earlier revision left the sampler resistor with a small section without protective nitride, leading to etching and severing of the resistor during the final etch step (figure 5.2). This was corrected by keeping nitride openings to within the ohmic contact so the GaAs material would always be protected.

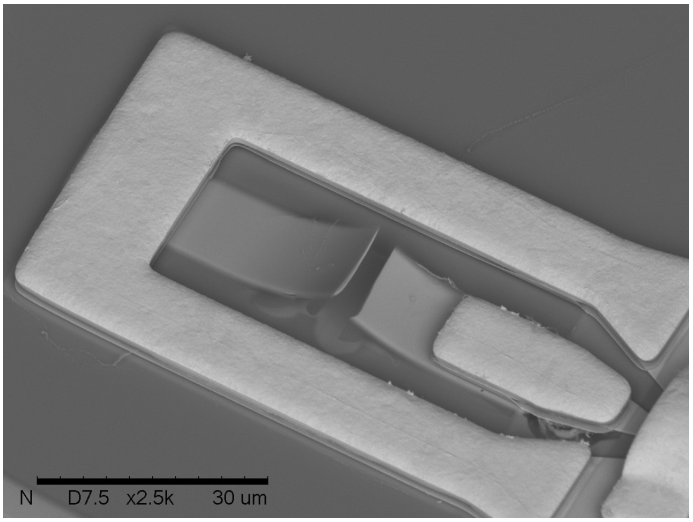

Figure 5.3: Failed TaN resistor.

Significant effort was put into developing a tantalum nitride (TaN) process for improved resistors. A TaN process would allow tailoring of the sheet resistance independent of the GaAs epitaxial structure. TaN was deposited by reactive sputtering, using a pure tantalum target in a controlled mix of argon and nitrogen. The resistors were defined using lift-off with a bilayer photoresist stack. Ultimately all dies using TaN resistors failed either immediately, or within seconds. Figure 5.3 shows one such failed resistor, which could be due to electromigration given failure at the midpoint.

Device/mesa isolation

The epitaxial layers outside of fabricated diodes must be removed or passivated so as to isolate individual diodes in the microwave circuit. Ion implantation is typically used, disrupting the GaAs lattice and leaving the unnecessary epitaxial growth semi-insulating. This work used the mesa approach, where the unnecessary epitaxial growth was etched away with an anisotropic plasma etch.

BCl_3	9	sccm
Cl_2	2	sccm
Ar	18	sccm
Pressure	20	mT
RF	50	W
ICP	200	W

Table 5.2: GaAs anisotropic ICP plasma etch recipe.

This etch, detailed in table 5.2 and adapted from [35], used an inductively coupled plasma etch tool with BCl_3, Cl_2, and Ar gases. The BCl_3 would polymerize and passive GaAs surfaces during etching, which the directional Ar would remove from the horizontal surface, leading to vertical sidewalls.

The selectivity between GaAs and the etch stop InGaP was moderate, and the InGaP thickness minimal, thus requiring operator attention towards the end of the etch. Rings on the sample would appear once the GaAs had been mostly etched, at which point the remaining material could be wet etched using the ohmic contact wet etch recipe. The InGaP etch stop was then wet etched using dilute hydrochloric acid.

After plasma tool servicing and upgrades, an excess of heat during etching led to the photoresist melting. This was remedied by bonding the sample to the actively cooled carrier with Santovac oil, and hard baking the photoresist after a flood exposure to cross-link (image reversal photoresist in positive mode).

The principle motivation for this mesa approach over implant isolation was cost. Implant isolation requires a thick gold mask under a polyimide base, and each implantation session would have cost on the order of $1000. By mesa etching, all processing could be done on campus, with no delays mailing samples to external vendors. Regardless, mesa etching provided excellent isolation as all non-semi-insulating layers were physically removed.

Interconnect metal

The interconnect metal was largely used for the sampler layout and metal under plating (such as capacitors). A similar metal stack to the Schottky contact was used, but with a much thicker Au layer.

Silicon nitride passivation

Silicon nitride (Si_3N_4) deposited by plasma enhanced chemical vapor deposition (PECVD) has been the traditional dielectric approach used in high speed NLTLs, and also other MMIC processes. It provides good passivation of the GaAs surface and excellent protection from scratching and moisture [31]. Our PECVD recipe is listed in table 5.3.

N_2	800	sccm
SiH_4	200	sccm
NH_3	100	sccm
Pressure	900	mT
RF	30	W
Temperature	250	°C

Table 5.3: PT70 PECVD Si_3N_4 deposition recipe.

Standard, low-density PECVD tools suffer from pinholes at low thicknesses and low temperatures. We found good success with a pulsed deposition approach, with RF power applied for 60 s, then off for 15 s. A high density PECVD tool, such as inductively coupled plasma or electron cyclotron resonance, would allow for higher quality films with fewer pinholes.

Air bridge process

The air bridge process was critical to this fabrication approach. By isolating mesas through etching instead of implant isolation, we then needed to connect the Schottky metal while avoiding the mesa edge. When using implant isolation, interconnect

metal can simply overlay the Schottky metal. With our air bridge process, Schottky contacts could be contacted by air bridge fingers with low parasitic capacitance, as shown in figure 5.4. Our air bridge approach represented a significant improvement over other reported implementations [5]. By contacting the diodes with fingers extending from the center conductor, diode mesas could be moved to the ground plane, reducing mesa to center conductor parasitic capacitance.

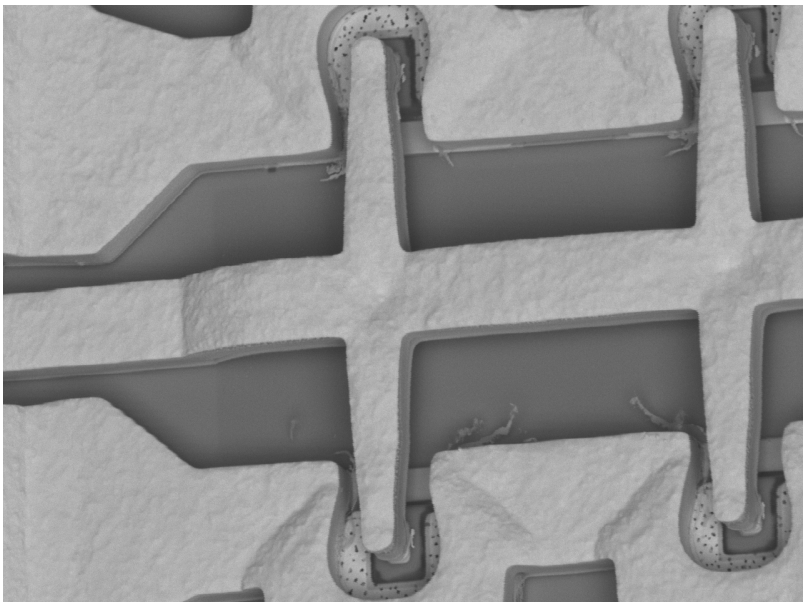

Figure 5.4: Air bridge structure with 6 μm wide center conductor.

Air bridges were fabricated by patterning the post photoresist, sputtering with seed metal, patterning the bridge photoresist, electroplating, and then removing the seed and photoresist. However, three key problems presented significant difficulty in developing the air bridge process.

The seed metal was prone to cracking if not carefully prepared. The post lithography used AZ 5214e photoresist as this could be made thermally stable by exploiting the image-reversal mechanism. After standard positive lithography and hard baking to reflow, the resist was then flood exposed and baked to mimic the image reversal process. This cross-linking image reversal process thermally stabilized

the resist, so as to not cause the seed metal to crack during deposition or other heating steps. When applying the top AZ 12XT photoresist to define areas to be electroplated, the seed was found to crack during the 110°C/120s soft bake. We believed that rapid solvent evaporation was the cause. By ramping this soft bake from 60°C to 100°C over 10 minutes, and holding for 2 minutes, cracking was avoided. We found that Ti/Au/Ti to be the most robust seed metal stack, with thickness optimized for ease of removal. Titanium-tungsten was investigated but was prone to cracking, despite a significant optimization attempt.

Minimizing surface roughness is critical to low loss microwave conductors. We developed a pulse-plating bath to reduce roughness and increase uniformity. Interestingly, the largest predictor of surface roughness was age of plating solution. Initial samples were plated with expired Technics Elevate Gold 7990 with terrible results through no fault of the product itself. For subsequent plating we used Transene TSG-250 sulfite gold plating solution, with excellent results within a few months of solution manufacture. Beyond a few months, the plated interconnects appeared rough, despite the 12 month expiration limit.

The final obstacle to a reliable process was removing the seed metal after plating. Wet etchants were not viable as they etched plated gold several times faster than sputtered gold. They also roughened the plated gold. Many dry etches were investigated until a recipe was decided on. We had good success etching gold with hydrogen, but unfortunately the plasma tool had poor cooling, allowing the sample to destructively overheat. Ultimately a high power, low pressure, chlorine-based recipe was found to be very effective. The highly accelerated chlorine ions were effective at etching the gold despite non-volatility of the etch products. Still, as can be seen in figure 5.4, some (presumably) seed metal cobwebbing remained.

5.2 Layout

The design was drawn using LayoutEditor with much of the layout generated using MATLAB generated macros (see appendix). The MATLAB script pulled design

values from an excel spreadsheet and wrote polygon drawing commands to a macro file that could be executed in LayoutEditor.

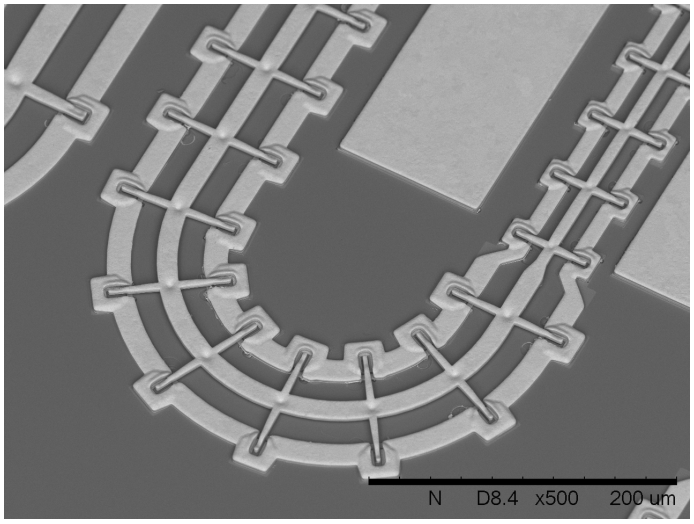

Figure 5.5: Serpentine NLTL with curved layout

The layout was then finished up manually, including curving the transmission line to create a serpentine structure, as shown in figure 5.5.

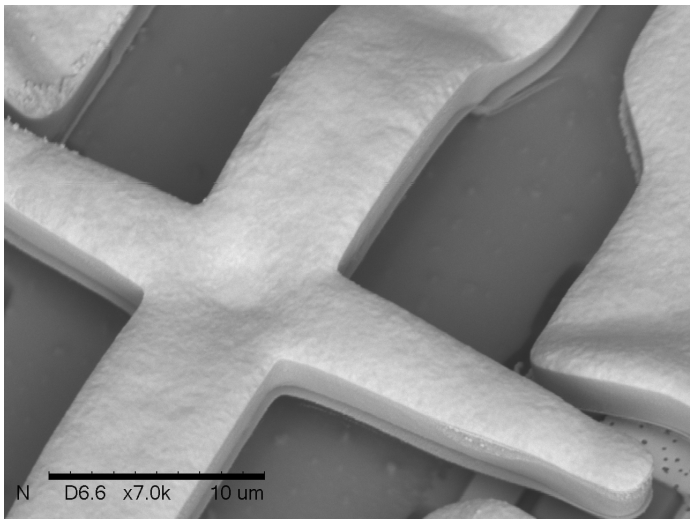

Figure 5.6: Transition from elevated CPW to CPW.

The air bridge center conductor had fingers to contact diodes, seen in figure 5.6 and 5.7.

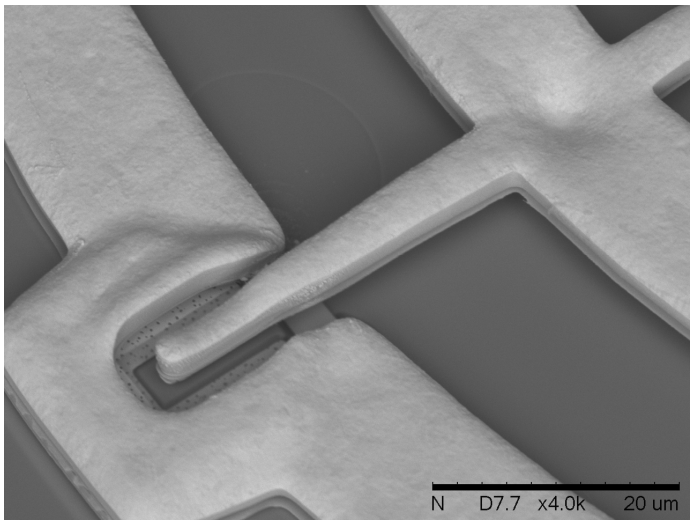

Figure 5.7: Air bridge center conductor with long diode finger.

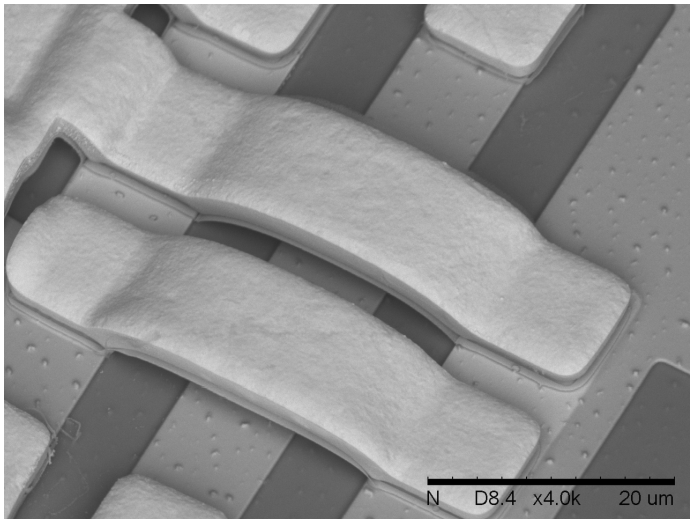

Figure 5.8: Air bridge ground strap.

Air bridge straps were used to connect each ground plane at the inputs to the

sampler (figure 5.8). Note that the rough metalization evident in many of the images was due to the dies being located at the edge of the processed sample, and thus subject to over etching and surface roughening.

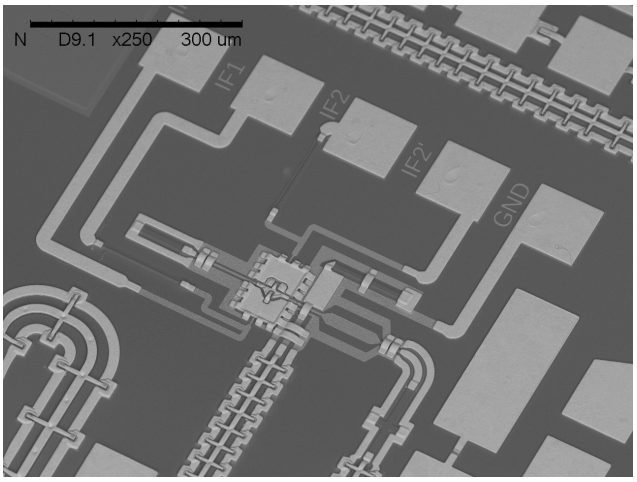

Figure 5.9: Sampler layout with IF pads.

The sampler had equispaced DC/IF pads for extracting the downconverted waveform (figure 5.9).

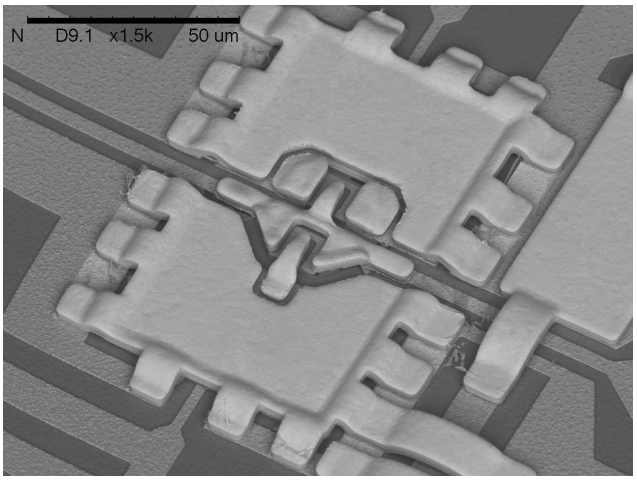

Figure 5.10: Close up of sampling diode bridge with hold capacitors.

The sampling diodes used small air fingers for low capacitance connection (figure 5.10).

5.3 Circuit characterization

NLTL circuits were first characterized with a vector network analyzer (VNA), using the scattering parameters S_{11} to identify shorting and S_{21} on an NLTL with pads at each end to measure delay versus voltage, and insertion loss. Circuits were probed on a Cascade probe station with three probe heads.

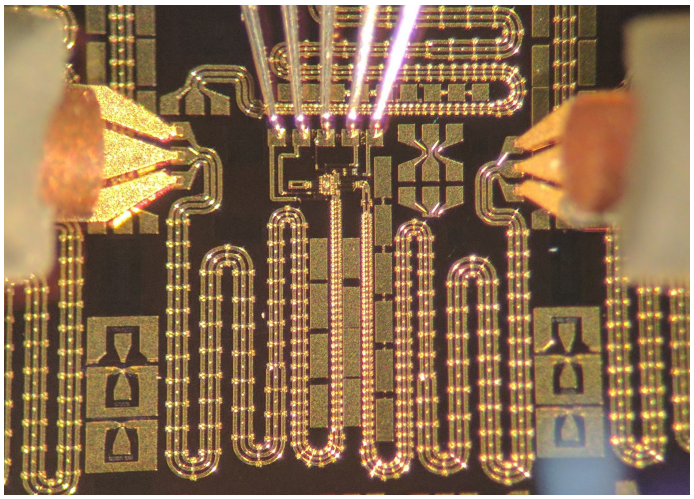

Figure 5.11: Wafer probing with microwave and DC/IF probes.

The two NLTLs that comprised a self-test circuit, sampling and drive, were each probed with Cascade Air Coplanar Probe ACP40 microwave probes with 150 um pad spacing (figure 5.11). The intermediate frequency (IF) sampler outputs were probed with a 5-pin probe, though only two pins were needed to capture the sampler output.

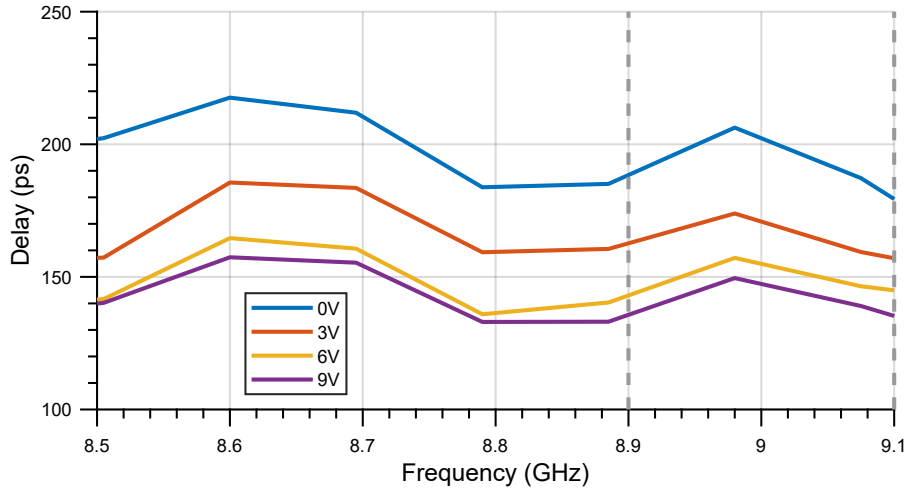

Figure 5.12: NLTL small signal delay with changing bias.

The delta-delay of an NLTL circuit with changing voltage was measured using a VNA with bias tees. The measurement (figure 5.12) was fairly noisy, but still somewhat consistent with the design value of 42 ps.

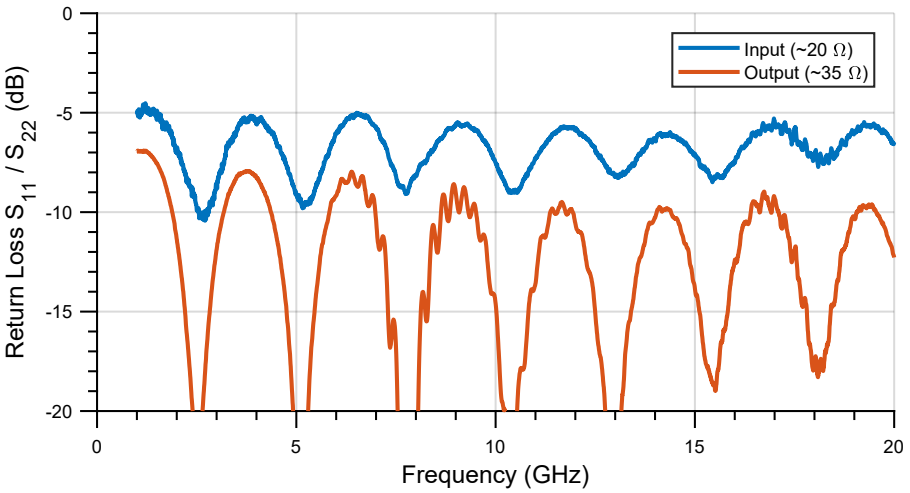

Figure 5.13: NLTL return loss on a test NLTL circuit.

Measured return loss was typically poor (figure 5.13), but not unexpected with such low input impedances. Proposed improvements to return loss are discussed in the final chapter. Note that the low impedance input end of the NLTL gave expectedly poorer return loss than the higher impedance and better matched output.

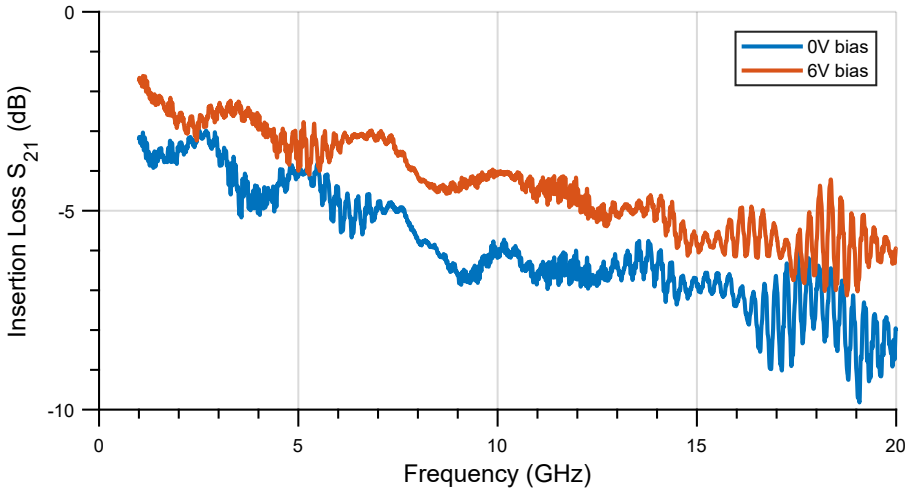

Figure 5.14: NLTL insertion loss on a test NLTL circuit.

Insertion loss was measured over 20 GHz and showed a dependence on bias (figure 5.14). Reverse biasing the diodes reduced parasitic resistance, thus reducing overall loss. The measured insertion loss compares favorably with the design value of 5.5 dB, though it should be noted that performance between dies was quite variable.

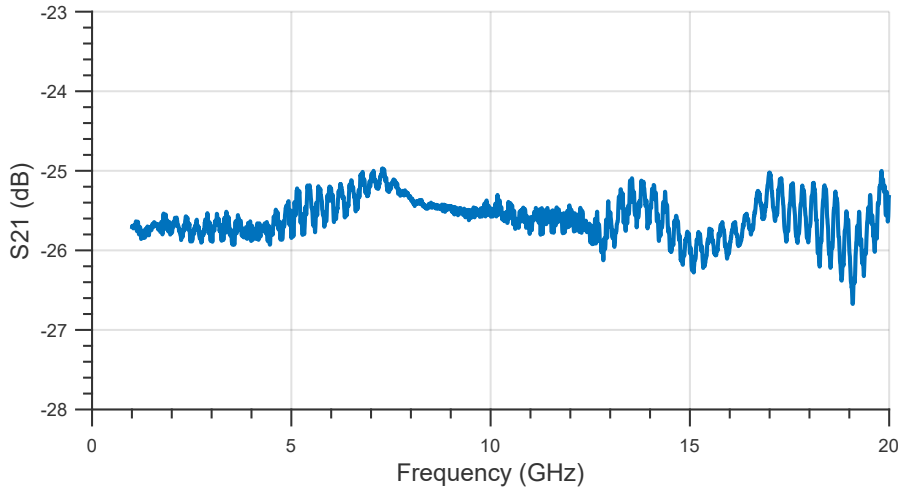

Figure 5.15: Attenuator insertion loss VNA measurement.

The insertion loss of the attenuator was measured over 20 GHz and found to be consistent with the design and simulation values (figure 5.15). This measured attenuation value was used to scale up the down converted waveform.

5.4 Dual-synthesizer measurement setup

Initial large signal measurements were taken using locked dual synthesizers to down-convert the transient waveform (figure 5.16). Hewlett Packard (HP) microwave synthesizers drove Agilent 83020A amplifiers to reach sufficient power levels. Bias tees were used to measure the rectified voltage, providing direct feedback on the amount of power entering the devices. The target bias was around 3.2 V, which was around the limit of the amplifiers. This corresponded to around 7 V peak voltage at the input of the NLTL.

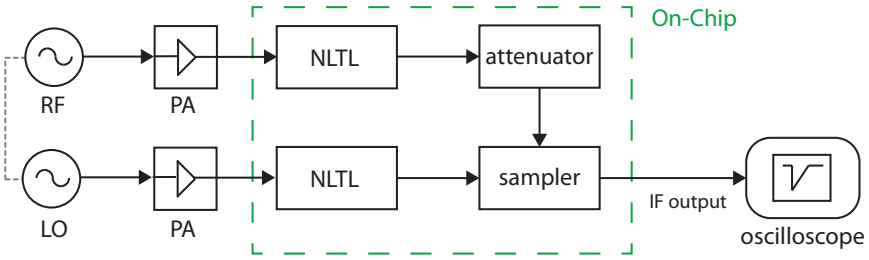

Figure 5.16: Measurement setup with dual locked synthesizers.

Optimum drive frequency was found to be 9 GHz, with a difference frequency of 900 Hz. This drive frequency was close to the target design value of 10 GHz.

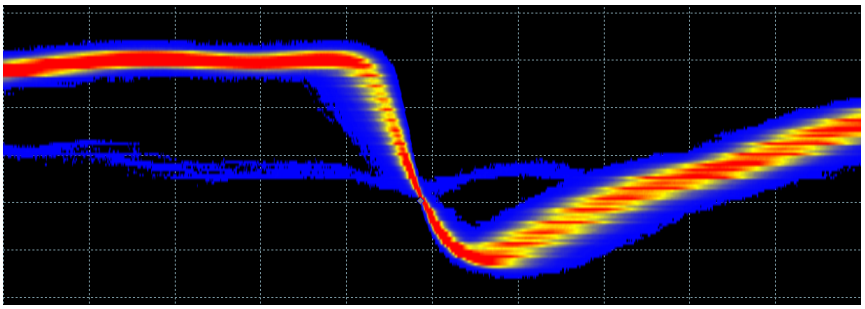

Figure 5.17: Shockwave measurement with persistence capture.

The downconverted waveform falltime was fairly inconsistent, believed due to drifting of the difference frequency. This inconsistency is most evident in the persistence capture of the changing waveform shown in figure 5.17. The unstable difference frequency resulted in an uncertain falltime, as the two are inextricably linked.

5.5 Mechanical phase shifter measurement setup

To gain an accurate measurement of the output falltime, the dual-synthesizer setup was replaced with a single synthesizer and 360 degree waveguide rotary phase

shifter [36].

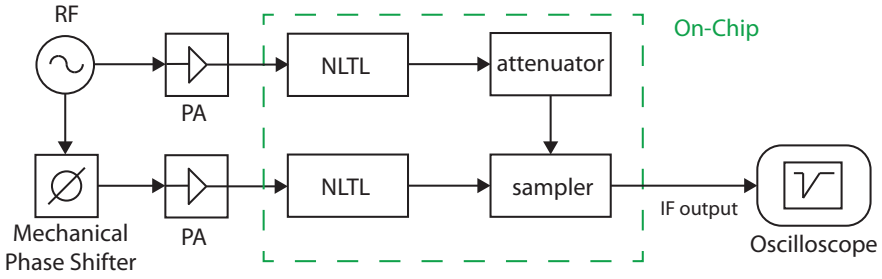

Figure 5.18: Measurement setup with rotating mechanical phase shifter.

The single output of the synthesizer was split, with one output fed through a HP X885A waveguide phase shifter (figure 5.18). Both outputs were then amplified as with the original setup. Attenuators were used at the inputs to the amplifiers to balance the output power levels, indicated by the measured NLTL bias. The phase shifter was jury rigged with a geared DC motor to step through the full 360 degrees at a rate of roughly 3 cycles per minute.

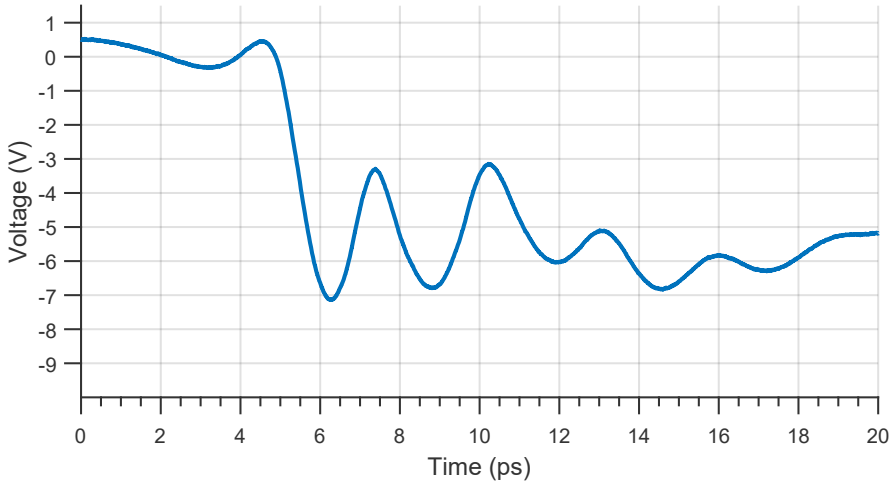

Figure 5.19: Measured waveform for die C4R5.

Downconverted waveforms were consistent and gave repeatable falltime measurements, validating this technique (figure 5.19). The excessive ringing evident is discussed in the following section.

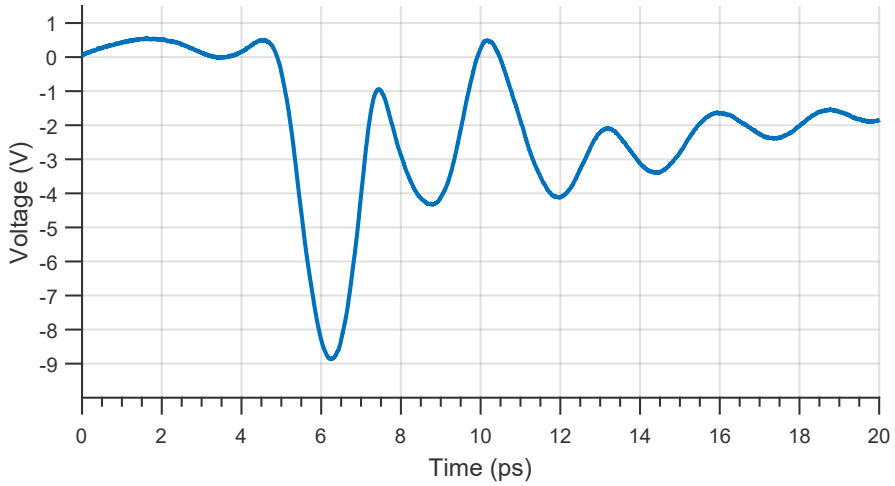

Figure 5.20: Measured waveform for die C4R4.

The fastest waveform measured was on die C4R4 (column/row), with a 10-90% falltime of 930 fs over 7.2 V (figures 5.20, 5.21).

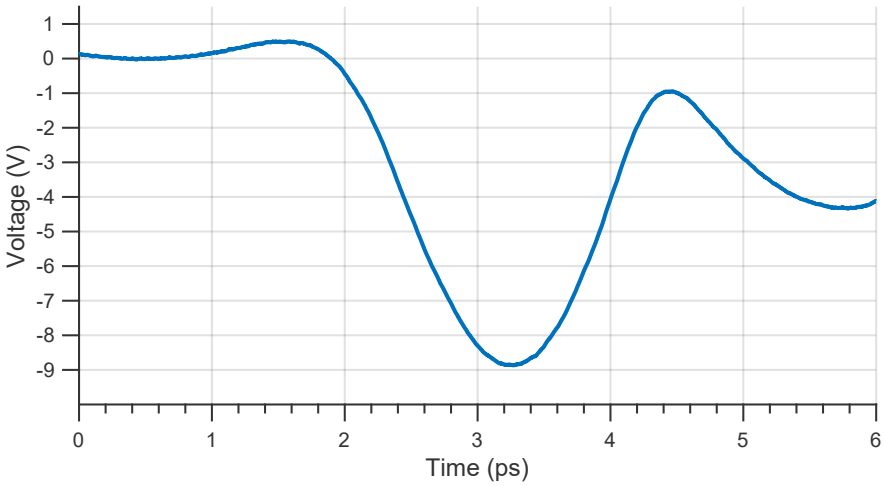

Figure 5.21: Measured waveform for die C4R4.

	Falltime	**Voltage**	**Slewrate**
	fs	V	V/ps
van der Weide [3]	480	3.5	7.29
Allen et al [5]	680	3.0	4.4
This work	930	7.2	7.7

Table 5.4: NLTL falltime reported results.

Comparing the measured waveforms with the state of the art, we can see that the double-uniform NLTL effective slew rate exceeds the other reported results (table 5.4, figure 5.22).

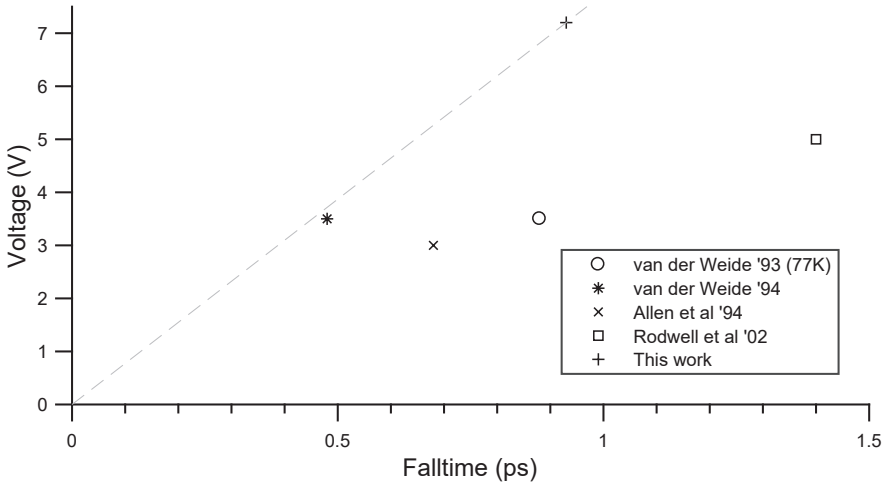

Figure 5.22: Comparison of reported shockwave results, with slew-rate of this work indicated by dashed line.

5.6 Discussion of ringing

The power spectrum of the ringing waveform (figure 5.23) showed that the resonance of the ringing was around 350 GHz. Sonnet simulations of the attenuator structure indicated a resonance at around 350 GHz, prompting further investigation. Also of note, the round trip between the input of the attenuator and shunting resistors was approximately 900 fs. It should be noted that the attenuator was made this large to handle the increased power being sunk over previous NLTL designs. Smaller TaN attenuators were also fabricated, but all failed.

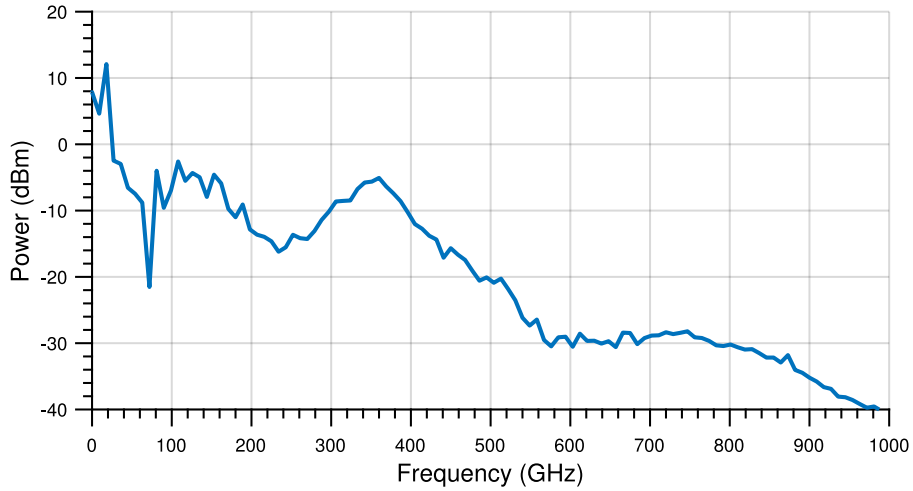

Figure 5.23: Power spectrum of shockwave measurement.

The attenuator was modeled in CST Microwave Studio and excited with step waveforms of varying falltimes (figure 5.24).

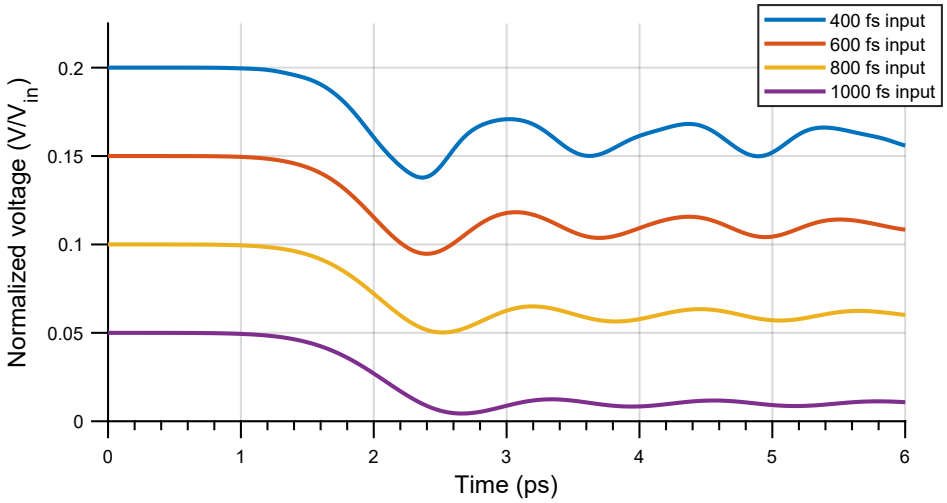

Figure 5.24: CST simulated step waveforms through the attenuator (offset for clarity).

The simulations indicate that the attenuator limits the output falltime to around

900 fs. The ringing of the simulated 400 and 600 fs waveforms were consistent with the ringing evident in the measured waveforms. These faster waveforms were also less attenuated than the slower 1000 fs waveform. Based on this, we believe our generated waveforms are much faster than as measured, but with slightly less amplitude. Combined, the slew rate would be much higher than as measured.

Chapter 6

InGaP/GaAs double-uniform Schottky diode

The breakdown voltage of the double uniform design presented in chapter 3 was fundamentally limited by the critical electric field of GaAs. Breakdown will occur in the low doped zero-bias depleted region as the electric field is a maximum and the critical electric (E_c) field will be lower than in the highly doped capacitance modulating region. By replacing the GaAs low-doped region with a higher critical electric field material, we could increase the breakdown voltage and extend the CV curve. Our approach was to replace the zero-bias depleted GaAs region with a lattice matched, high E_c material with conduction band alignment close to GaAs. As this region would be fully depleted in the operating voltage range, electron mobility was not critical.

The two candidate materials considered for this double uniform heterostructure were indium gallium phosphide (InGaP) and aluminum gallium arsenide (AlGaAs). AlGaAs is slightly lattice mismatched to GaAs, increasing with higher Al concentration. InGaP can be lattice matched to GaAs ($In_{0.49}Ga_{0.51}P$) and provides a significant critical electric field increase for a given doping. InGaP was ultimately chosen for these reasons.

This new diode structure was designed to be a 'drop-in' replacement for the

GaAs double-uniform structure to permit reuse of the NLTL design and layout. As InGaP has a dielectric constant of only 11.8, versus 12.9 for GaAs, the InGaP region thickness was reduced proportionately to 137 nm.

While care was taken to model impact ionization and breakdown of InGaP in Silvaco, we also used reported experimental results to approximate breakdown voltage. Impact ionization coefficients relate to electron-hole pairs generated by carrier collisions per distance accelerated [37]. Excessive collisions will lead to breakdown. The impact ionization rates in [38] show that almost double the electric field is needed for the coefficients of InGaP to reach those of GaAs. Indeed, this is consistent with reports of high-breakdown InGaP Schottky diodes [39].

The GaAs capacitance-modulating region was also susceptible to breakdown, requiring consideration. Critical electric field increases with doping, as dopants scatter and slow down accelerated carriers, reducing electron-hole pair generation. Critical electric field measurements were collated by [40], where they suggest a fourth root relation between doping and critical electric field. The doping of our capacitance modulating region is an order of magnitude higher than the low-doped $4 \cdot 10^{16}$ cm^{-3} region which led to a breakdown voltage of around 13 V for our GaAs double-uniform diode. This model predicts an 80% increase in critical electric field. Further, the electric field at the capacitance-modulating region would be reduced through the low doped region (on the order of 10%), and not subject to increased electric fields due to metal edge effects. With the above considered, we believe our InGaP heterostructure would exceed breakdown in excess of 20 V.

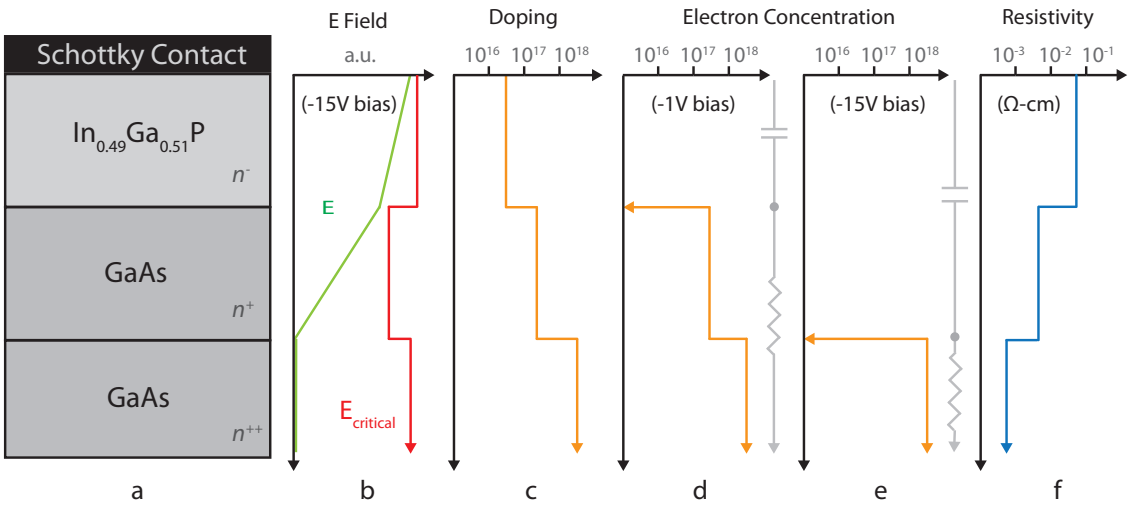

Figure 6.1: a) Diode heterostructure; b) Electric field with high reverse bias; c) Doping profile d) Electron concentration at low reverse bias, with equivalent circuit; e) Electron concentration at high reverse bias; f) Resistivity profile.

The proposed diode structure is illustrated in figure 6.1, along with the electrical characteristics. The electric field graph illustrates the benefit of the heterostructure, showing that low-doped InGaP should have similar E_c to highly-doped GaAs. The electric field will decrease faster through the GaAs n^+ region than the E_c will decrease. The doping is similar to that of the homogeneous double-uniform structure, except that the undepleted n^+ doping could be increased to extend the useful CV modulation to higher voltages. The electron concentrations in reverse bias show that the diode series resistance is unaffected by the higher-resistivity InGaP region as it would be fully depleted, and thus capacitive. The equivalent circuit for each reverse bias extreme is also shown. It should be noted that the inclusion of the lower-mobility InGaP region would result in higher series resistance in forward conduction. As such, this diode would not be ideal for high speed sampling.

6.1 Design procedure

With the InGaP region thickness set at 137 nm, and doped $4 \cdot 10^{16}$ cm^{-3}, the only design variable was the GaAs capacitance-modulating region doping. As with the GaAs double uniform design, this doping determined the extent of capacitance-modulation range. Diode structures were simulated in Silvaco using the Atlas and DevEdit tools.

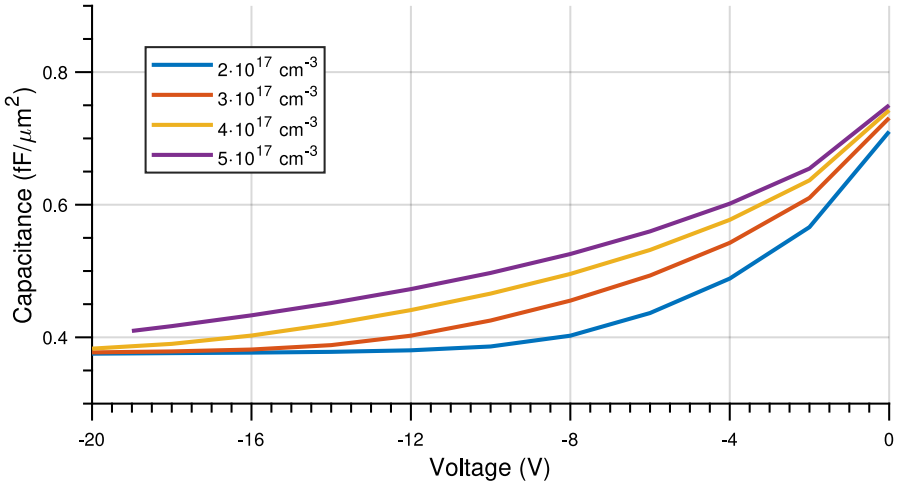

Figure 6.2: InGaP diode structure CV doping sweep

The CV curves with swept doping are shown in figure 6.2. We found the optimal doping to be $3 \cdot 10^{17}$ to $4 \cdot 10^{17}$ cm^{-3}, assuming >20 V breakdown voltage. Doping of $5 \cdot 10^{17}$ cm^{-3} was not fully depleted at 19 V, where Silvaco predicted voltage breakdown.

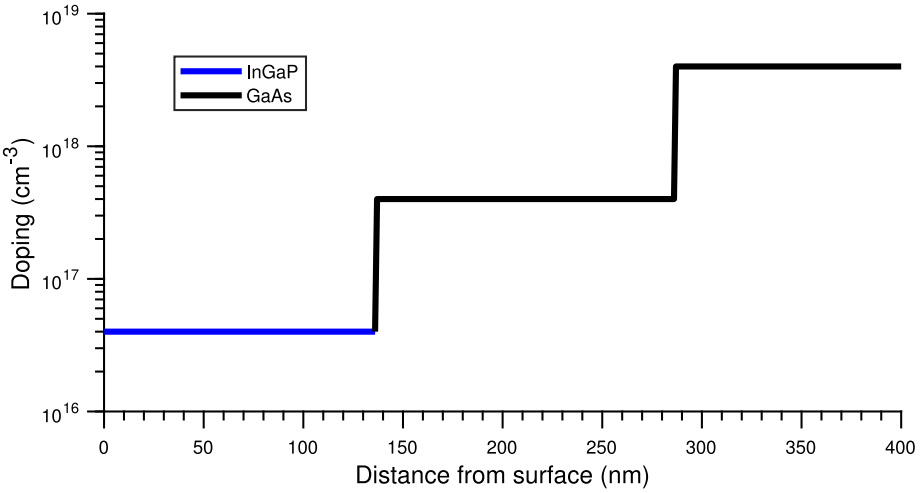

Figure 6.3: InGaP diode structure CV doping sweep.

The final optimized doping of the InGaP/GaAs double-uniform diode is shown in figure 6.3.

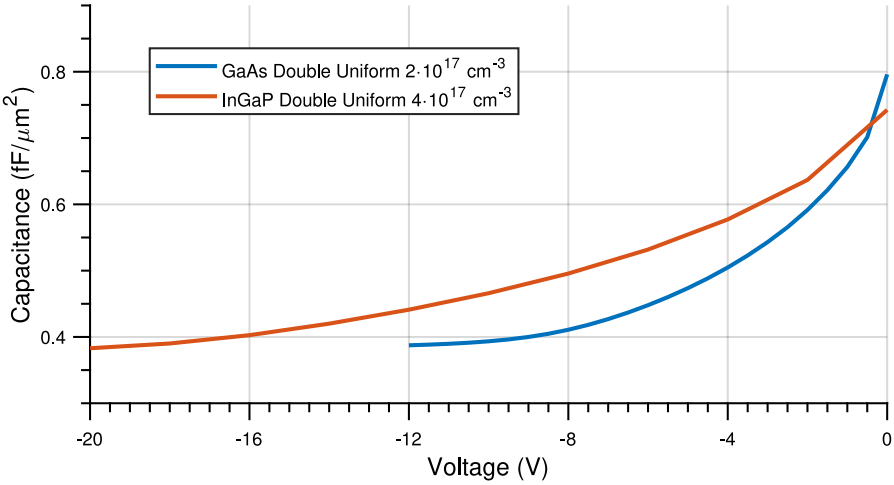

Figure 6.4: InGaP diode structure CV vs. homogeneous double-uniform.

The zero bias capacitance was slightly below that of the homogeneous structure

indicating higher zero bias depletion, but otherwise matched well over the full capacitance range (figure 6.4). By doubling the GaAs doping from the homogeneous case, the maximum slew rate should also double, assuming the transient electron velocities are comparable. This should allow a similar falltime with double the voltage range.

6.2 Diode breakdown voltage simulation

Breakdown voltage was simulated in Silvaco using the Selberrherr model for impact ionization, using the InGaP impact ionization coefficients from [38]. The simulations suggested a breakdown voltage on the order of 20 to 25 V. This was consistent with our earlier rationalization with reported experimental data.

6.3 Conduction band discontinuity

The conduction band offset between InGaP and GaAs (measured at approximately 0.25 eV [39]) resulted in a reduced electron concentration (effectively lower doping) in the undepleted capacitance-modulation region.

This reduced electron concentration resulted in higher resistance in the undepleted region, which can be seen in the cut-off frequency curve (figure 6.5). Schoen et al [39] proposed grading or delta-doping the interface to reduce the degrading effect. We explored grading the InGaP at the GaAs interface with increased gallium. While we found that this removed the discontinuity, Silvaco predicted a significant reduction in breakdown voltage. In reality, the cut-off frequency at very low bias is sufficiently good, and comparable to the uniform diodes discussed in chapter 3.

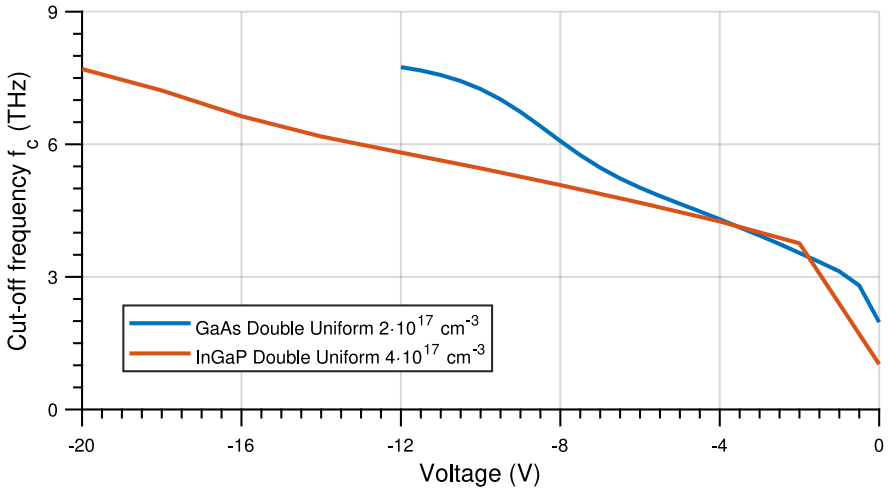

Figure 6.5: InGaP diode structure cut-off frequency vs. homogeneous double-uniform.

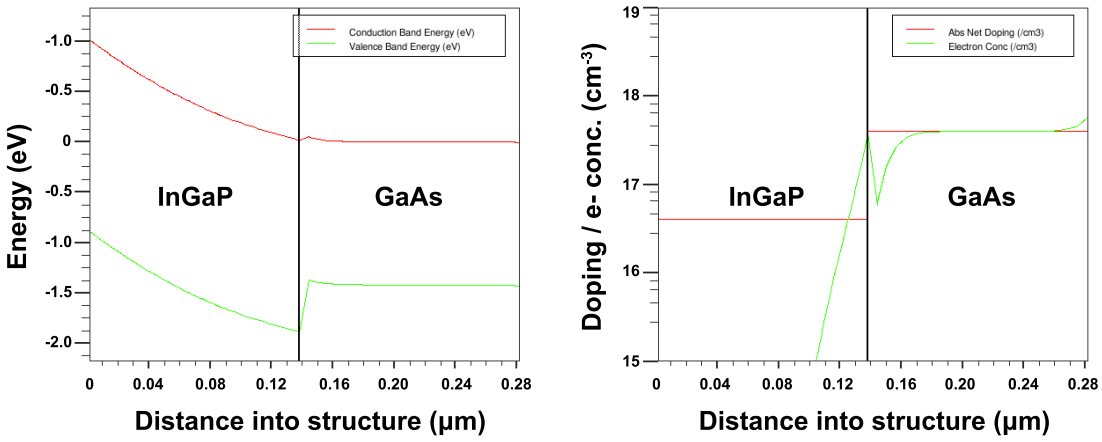

Figure 6.6: InGaP diode band diagram showing the conduction band discontinuity (left) and effect on e^- concentration (right).

The conduction band discontinuity and electron depletion are illustrated in figure 6.6. Silvaco predicted a dip in electron concentration to just below $1 \cdot 10^{17}$ cm^{-3}, which is not especially concerning. It should be noted that this will not

affect current saturation, as this region will be fully depleted under high bias when conducting high current.

Chapter 7

Future work

The double-uniform diode NLTL has delivered strong results with headroom for further improvement. Potential NLTL design and process improvements are discussed in detail below. Further, we explore on-chip terahertz sensing using an NLTL driven sensor.

7.1 Design and process improvements

The first generation of fabricated devices exposed a number of areas for potential improvement. The minimum Schottky diode width of 2 μm was process limited, but could be decreased with new processing techniques. The NLTL impedance scaling could follow an optimal Klopfenstein taper to minimize reflections over linear scaling. Poor input matching due to low input impedance could be addressed with an impedance transformer. Layout parasitics could be minimized through full-wave simulations. These improvements are investigated in more detail below.

Diode size reduction

The minimum diode size of the first generation of devices was process limited. A 2 μm wide diode required a 1.2 μm wide nitride opening centered on the diode, and then the plated air bridge finger again centered over the diode. Lithography

optimization towards the end of first generation processing could have possibly reduced this minimum diode size to 1.5 um or smaller. However, we have devised a self-aligned technique with no minimum size for the second generation (figure 7.1). This technique involved increasing the Schottky metal thickness to approximately 1 μm, and then removing the photoresist near the top of the metal using partial exposure. This would allow us to expose any length Schottky diode for either nitride etching or air bridge plating.

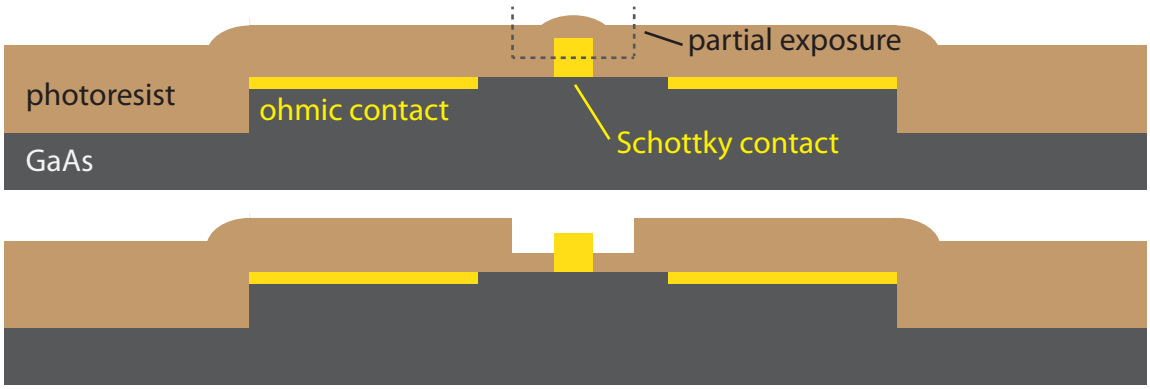

Figure 7.1: Self-aligned partial exposure technique.

NLTL impedance scaling

The cell impedance was scaled in the first generation using a basic loss model, increasing the impedance to maintain voltage despite losses and at the expense of current. This approach gives an essentially linear scaling of impedance, which is a non-optimal taper. The optimal taper, proposed by Klopfenstein [41], was implemented in the MATLAB NLTL generation code (figure 7.2). As the impedance flattens out at the end of the taper, a short linear taper was used for the final sections of the NLTL to account for the increased losses experienced by the near-picosecond transient. The impedance jump in these final sections was low enough that the mismatch reflection would be minimal.

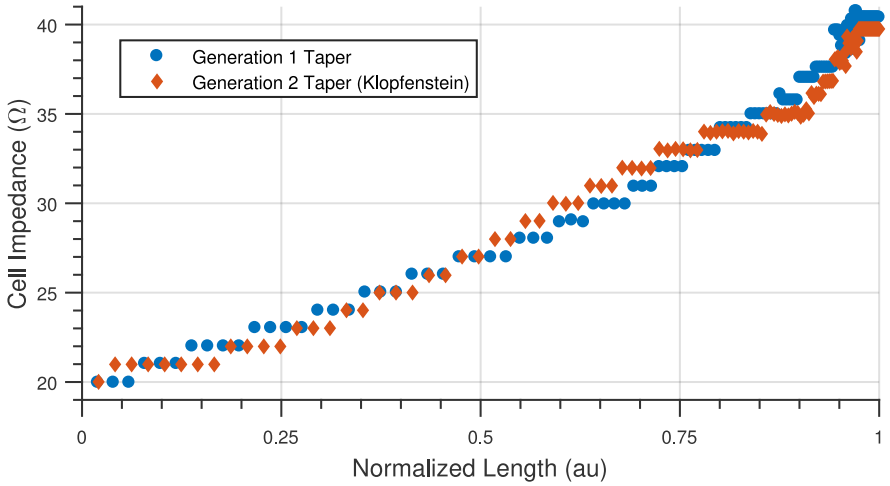

Figure 7.2: NLTL optimial impedance scaling.

Input impedance matching

The return loss of the first generation of devices was undesirably high, on the order of -5 to -10 dB in the band of interest. While such input mismatch could be overcome by increasing the input power, matching this input impedance would increase efficiency and significantly reduce the VSWR. We first investigated a simple tapered coplanar waveguide transmission line to bring the impedance from 50 ohm down to the NLTL's 20 Ω input. As with the NLTL impedance scaling, we chose the optimal Klopfenstein taper. However, coplanar waveguide transmission line on GaAs requires prohibitively impractical dimensions to achieve impedances on the order of 20 Ω. Our proposed solution was to essentially replicate the NLTL structure, using MIM capacitors in place of Schottky diodes. This would allow the creation of cells with impedances down to 20 Ω using 55 Ω coplanar waveguide and air bridge contacted capacitors.

Coplanar waveguide parasitics

In the first generation of devices, parasitics were not taken into account given the use of air bridge fingers over the high-capacitance alternative. We investigated many sources of parasitics using the Sonnet Suites software. The ground plane strap that was included to shorten the current path in the ground plane was found to add more parasitic capacitance than previously approximated, lowering the cell impedance. The post used to periodically support the air bridge center conductor was also found to add unnecessary capacitance and was removed for the final cells where the diode fingers could provide adequate support. Future NLTL layouts would benefit from these changes.

Attenuator bandwidth improvement

The attenuator should be reduced in size to increase bandwidth and minimum falltime. As this will increase the power density, we will explore multiple attenuator sizes to see how small it can be made before component failure.

7.2 On-chip THz time domain spectroscopy (TDS)

Terahertz on-chip sensing has experienced some interest in recent years with both chemical and biological applications [42–50]. Implementations to date have largely utilized photoconductive material to convert optical excitations into electrical pulses. This sensing is effectively time domain transmissometry (TDT), with the pulse traveling along a transmission line loaded with a powder or liquid dielectric and then into a sampler. We propose an all electronic approach to terahertz on-chip sensing, enabling a complete packaged sensor to realistically fit within a one inch cube. The sensor would be a meandering transmission line optimized for minimal loss to increase sensitivity to dielectric loading.

Requirements of an on-chip sensor

CPW on GaAs is not an ideal transmission line as the dielectric constant is so high. The high dielectric constant requires a trade off between radiative loss (narrow conductor/gap) and metal loss (wide conductor). An ideal on-chip sensor would be CPW transmission line on a low loss and low ϵ_r substrate for minimal loss and maximum dielectric loading sensitivity. However, CPW on GaAs significantly simplifies fabrication and could be a viable option if the loss is well characterized. Contributors to loss are:

1. Substrate dielectric loss (tanδ)
2. Metal conductor loss
3. Radiative loss

Substrate dielectric loss (α_d) is proportional to frequency and is given by equation 7.1. This loss is minimal for high quality substrates such as semi-insulating (SI) GaAs and single crystal quartz.

$$\alpha_d = \tan(\delta) \cdot \frac{2 \cdot \pi \cdot f \cdot C' \cdot Z_0}{2} \ [\mathrm{Np/m}] \tag{7.1}$$

C' is the transmission line capacitance per unit length and is a function of substrate permittivity. Dielectric loss isn't a significant contributing factor to the total loss for tanδ $\lesssim 0.002$ (i.e. SI GaAs). For tanδ on the order of 0.01 or higher, loss is significant at higher frequencies (300+ GHz) for our geometries of interest.

Metal conductor loss (α_m) is proportional to the square root of frequency and is given by 7.2.

$$\alpha_m = \frac{R'}{2 \cdot Z_0} \ [\mathrm{Np/m}] \tag{7.2}$$

R' is the transmission line resistance per unit length and is the source of the frequency dependence due to the skin depth effect. With radiation loss suppressed, metal loss is the largest contributor to loss in the low to mid terahertz frequency band.

Radiation is by far the largest contributor to loss in the mid to high terahertz band as it is proportional to the cube of frequency. For large ground planes, loss is given by equation 7.3. Variables in this equation are defined in [51].

$$\alpha_r = \left(\frac{\pi}{2}\right)^5 \cdot 2 \cdot \frac{\left(1 - \frac{\epsilon_{eff}}{\epsilon_r}\right)^2}{\sqrt{\frac{\epsilon_{eff}}{\epsilon_r}}} \cdot \frac{(w + 2s)^2 \cdot \epsilon_r^{1.5}}{c^3 \cdot K'(k) \cdot K(k)} \cdot f^3 \ \ [\mathrm{Np/m}] \tag{7.3}$$

This loss can be significantly reduced by decreasing the size of the CPW ground planes to the size of the center conductor [17]. The increase in overall resistance is around 20%. Reducing the substrate dielectric constant (using e.g. quartz instead of GaAs) affords a similar reduction, but with added fabrication complexity.

CPW on GaAs with 10 µm center conductor width and 10 µm gap affords a good compromise between metal and radiative loss. The losses with this geometry are shown in figure 7.3. Suppressed radiative loss refers to the use of narrow ground planes as described in [17]. Also included is the loss due to dielectric loading of materials with tanδ ranging from 0.01 to 0.05, typical for many plastics. With the radiative loss suppressed, this loading loss is clearly dominant.

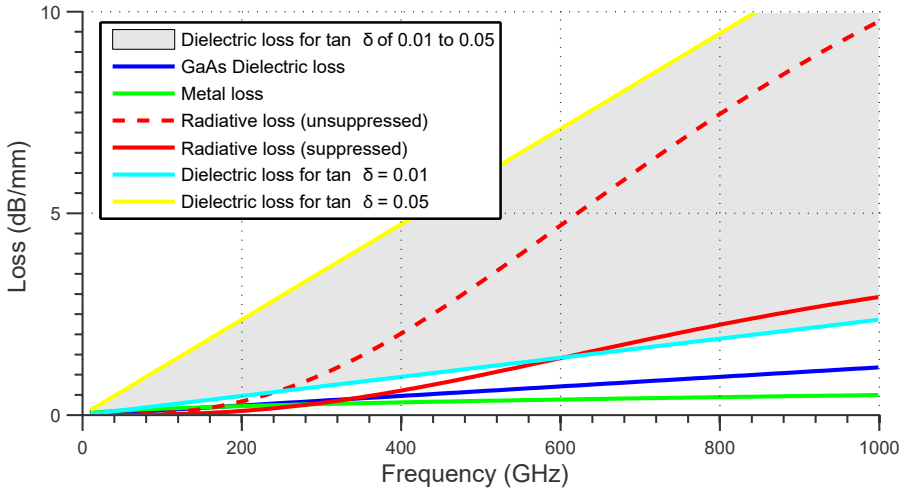

Figure 7.3: Dielectric loss for various tanδ vs. other loss mechanisms.

Appendix A

Silvaco Programs

Programs for simulating Schottky diodes in Silvaco Atlas. Diode structures were modeled in DevEdit.

A.1 GaAs Simulation Code

```
1  # deckbuild command file
2
3  MESH INF=<strucfile>.str width=1
4  # removed cylindrical from above
5  # total area should be 1 um^2
6
7  models srh conmob fldmob auger bgn
8  # ust added for breakdown
9
10 impact selb
11 contact name=anode workf=4.87 surf.rec
12 contact name=cathode con.resist=1e-6
13
14 method newton
15 #climit=1e-4
16
17 solve init
```

```
solve prev
solve vanode=0
output con.band val.band band.param

log outf=<logname>.log
solve vanode=-0.1 vstep=-3 vfinal=-20 name=anode
log off
tonyplot -st <logname>.log

log outf=<logname> s.param inport=anode outport=cathode
solve vanode=0 vfinal=-10 vstep=-0.5 name=anode ac.analysis freq=100e9
log off
tonyplot -st <logname>
```

A.2 InGaP Simulation Code

```
# deckbuild command file

MESH INF=<strucfile>.str width=1

#region InGaP x.comp=0.51
#should be defined in .str file ?? check!

# This should set the cond band offset to 0.1eV (Dong2008)
material GaAs affinity=4

models srh conmob fldmob auger bgn bbt.std
#ust

impact selb e.side jnx.min=1e-12 jny.min=1e-12
impact material=InGaP \
                AN1=3.85e6 AN2=3.85e6 \
                BN1=3.71e6 BN2=3.71e6 \
                EGRAN=0 \
                AP1=1.71e6 AP2=1.71e6 \
```

```
20                    BP1=3.19e6 BP2=3.19e6 \
21                    BETAN=1 BETAP=1
22
23 contact name=anode workfun=5.1 surf.rec vsurfn=3.5e4
24 contact name=cathode con.resist=1e-6
25
26 # vsurfn from ioffe/Pearton94
27 # workfun = affinity + schottky barrier height
28 # InGaP affinity = 4.1; SBH ~=1
29
30 #gummel is slower, but better for poorly defined problems
31 method newton maxtraps=10 carriers=2 climit=1e-4
32 #method gummel
33
34 solve init
35 solve prev
36 solve vanode=0
37 output con.band val.band band.param
38
39 save outf=<strucname>.str
40 tonyplot -st <strucname>.str
41
42 #log outf=<logname>.log
43 #solve vanode=-0.1 vstep=-5 vfinal=-30 name=anode
44 #log off
45 #tonyplot -st <logname>.log
46
47 #log outf=<logname>.log
48 #solve vfinal=-18 vanode=0 vstep=-2 name=anode ac.analysis freq=100e9
49 #log off
50 #tonyplot -st <logname>.log
51
52 log outf=<logname>.log s.param inport=anode outport=cathode
53 solve vanode=0 vfinal=-18 vstep=-0.5 name=anode ac.analysis freq=100e9
54 log off
55 tonyplot -st <logname>.log
56
```

```
save outf=<strucname>.str
tonyplot −st <strucname>.str
```

A.3 Device models

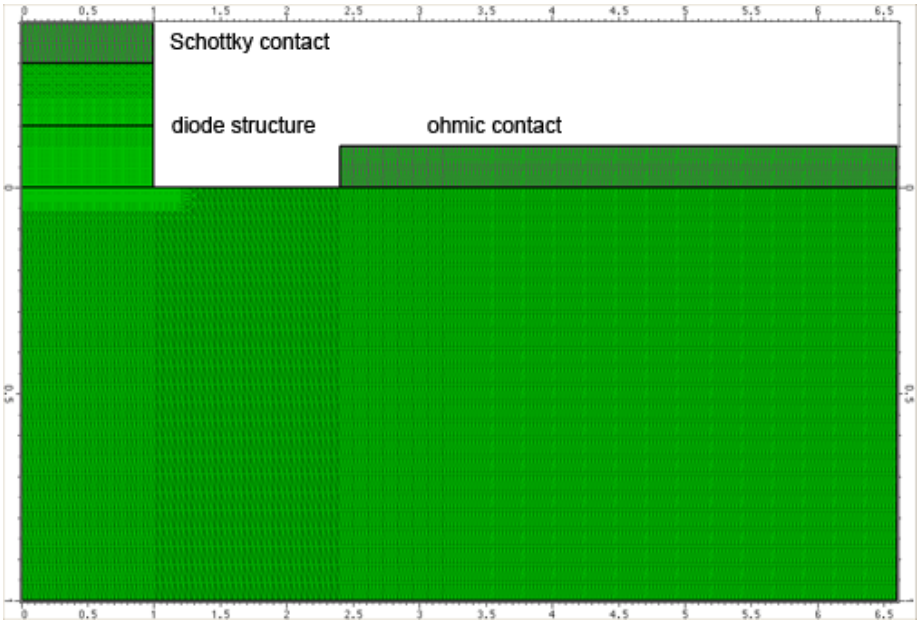

Figure A.1: Silvaco model example in DevEdit.

Appendix B

MATLAB Programs

MATLAB scripts interfaced with an excel spreadsheet to store circuit parameters and computed results.

B.1 Generate NLTL parameters code

Generates the NLTL circuit parameters and results, storing them in the spreadsheet.

```
SheetNumber = 1;
fbragg_ll  = 100;   % bragg freq lower limit
Z_init  = 20;          %  initial   cell  impedance
Cadjust = 1.1;         % adjust line  capacitance to  account for  posts,  etc
geo = xlsread('Quartz NLTL.xlsx', SheetNumber, 'B7:D126');
% geometry(x,y) where x is section,  y=1 is  width, y=2 is  gap,  y=3 is  freq
diode = xlsread('Quartz NLTL.xlsx', SheetNumber, 'K7:P126');
R = zeros(size(geo,1),  1);
L = zeros(size(geo,1),  1);
G = zeros(size(geo,1),  1);
C = zeros(size(geo,1),  1);
Z = zeros(size(geo,1),  1);
f_bragg = zeros(size(geo,1),  1);
ddelay = zeros(size(geo,1),  1);  % delta--delay of cell
falltime_in  = zeros(size(geo,1),  1);
falltime_out  = zeros(size(geo,1),  1);
```

```
17 d = zeros(size(geo,1), 1);
18 A = zeros(size(geo,1), 1);
19 freq_cpw = zeros(size(geo,1), 1);
20 Cd_hi = diode(:,1);
21 Cd_lo = diode(:,3);
22 Cd = diode(:,5);
23 Rd_hi = zeros(size(geo,1), 1);
24 Rd_lo = zeros(size(geo,1), 1);
25 Rd = zeros(size(geo,1), 1);
26 R_undep = zeros(size(geo,1), 1);
27 R_nplus = zeros(size(geo,1), 1);
28 R_ohmic = zeros(size(geo,1), 1);
29 width = zeros(size(geo,1), 1);
30 gap = zeros(size(geo,1), 1);
31 Zavg = zeros(size(geo,1), 1);
32 Zhi = zeros(size(geo,1), 1);
33 Zlo = zeros(size(geo,1), 1);
34 Zcell = zeros(size(geo,1), 1);
35 floss = 20e9;    % drive frequency, for loss
36 atten_V = zeros(size(geo,1), 1); % alpha, voltage attenuation
37 atten_total = 0; % total attenation, dB
38
39 for loop = 1:120
40     % Calculate incoming falltime and the corresponding f_bragg
41     if loop == 1
42         % Set input falltime based on NLTL drive frequency
43         falltime_in(1) = 25;
44         f_bragg(1) = 1e3 / (1 * falltime_in(1)) * 1.5;
45
46         % set initial Zcell
47         Zcell(loop) = Z_init;
48
49         % Set first transmission line geometry
50         width(loop) = 20;
51         gap(loop) = 26;
52         [R(loop), L(loop), G(loop), C(loop), Z(loop)] = RLGC(width(loop)*1e-6,
               gap(loop)*1e-6, 3e-6, 0.001, 12.9, floss, 3e7);
```

```
53          L(loop) = 5.2e-7;
54          C(loop) = 6.7e-11;
55          Z(loop) = sqrt(L(loop)/C(loop));
56
57      else
58          falltime_in(loop) = falltime_out(loop-1);
59          f_bragg(loop) = 1e3 / (1 * falltime_in(loop));
60
61          % calculate Zcell based on previous Zcell and previous atten_V
62          Zcell(loop) = exp(atten_V(loop-1)) * Zcell(loop-1);
63
64          % check if Zcell has changed since last cell
65          if round(Zcell(loop)) == round(Zcell(loop-1)) && f_bragg(loop) < 920
66              f_bragg(loop) = f_bragg(loop-1);
67          end
68
69          % Choose the requisite geometry based on the length of the previous cell
70          if A(loop-1) <= 32
71              % eCPW 6/10/12
72              width(loop) = 6;
73              gap(loop) = 10;
74              [R(loop), L(loop), G(loop), C(loop), Z(loop)] = RLGC(width(loop)*1e-6,
                    gap(loop)*1e-6, 3e-6, 0.001, 12.9, floss, 3e7);
75              L(loop) = 4.6e-7;
76              C(loop) = 4.4e-11;
77              Z(loop) = sqrt(L(loop)/C(loop));
78
79          elseif d(loop-1) <= 140e-6 && A(loop-1) < 125
80              % eCPW 12/18/15
81              width(loop) = 12;
82              gap(loop) = 18;
83              [R(loop), L(loop), G(loop), C(loop), Z(loop)] = RLGC(width(loop)*1e-6,
                    gap(loop)*1e-6, 3e-6, 0.001, 12.9, floss, 3e7);
84              L(loop) = 5.1e-7;
85              C(loop) = 5.5e-11;
86              Z(loop) = sqrt(L(loop)/C(loop));
87
```

```
88          else
89              % eCPW 20/26/20
90              width(loop) = 20;
91              gap(loop) = 26;
92              [R(loop), L(loop), G(loop), C(loop), Z(loop)] = RLGC(width(loop)*1e-6,
                    gap(loop)*1e-6, 3e-6, 0.001, 12.9, floss, 3e7);
93              L(loop) = 5.2e-7;
94              C(loop) = 6.7e-11;
95              Z(loop) = sqrt(L(loop)/C(loop));
96          end
97      end
98
99      freq_cpw(loop) = 1e3 / (2 * falltime_in(loop));
100     w = 2*pi*freq_cpw(loop) * 1e9;
101
102     % Increase line capacitance by 10% to account for parasitics (post/diode)
103     C(loop) = C(loop) * Cadjust;
104
105     % Apply lower limit to fbragg
106     if f_bragg(loop) < fbragg_ll
107         f_bragg(loop) = fbragg_ll;
108     end
109     % ----------------------------
110
111     % ---------- SOLVING FOR DIODE d and A -----
112
113     % Calculate TL length 'd' and diode area 'A' from Z_cell and f_bragg
114     syms dist Area
115     S = solve(sqrt(dist*L(loop) / (dist*C(loop) + Area*Cd(loop))) == round(Zcell(loop)),
            (pi*sqrt(dist*L(loop)*(dist*C(loop)+Area*Cd(loop))))^-1 == f_bragg(loop)*1e9);
116     d(loop) = S.dist(1); % m
117     d(loop) = round(d(loop)*1e6)*1e-6;
118     A(loop) = S.Area(1);
119     %A(loop) = round(A(loop)/2)*2;
120     A(loop) = round(A(loop));
121
122     if A(loop) <= 14 && A(loop-1) ~= 14
```

```
123         %A(loop) = A(loop-1);
124         %d(loop) = d(loop-1);
125         syms dist fbr
126         S = solve(sqrt(dist*L(loop) / (dist*C(loop) + 14*Cd(loop))) ==
                round(Zcell(loop)),(pi*sqrt(dist*L(loop)*(dist*C(loop)+14*Cd(loop))))^-1 ==
                fbr*1e9);
127         d(loop) = double(S.dist(1)); % m
128         d(loop) = round(d(loop)*1e6)*1e-6;
129         f_bragg(loop) = double(S.fbr(1));
130         A(loop) = 14;
131     elseif A(loop) <= 14
132         A(loop) = A(loop-1);
133         d(loop) = d(loop-1);
134         f_bragg(loop) = f_bragg(loop-1);
135     end
136     % ----------------------------------------
137     % ---------- DIODE RESISTANCE CALCULATIONS -
138
139     if A(loop) <= 12
140         r_fact = 0.35;
141     elseif A(loop) <= 16
142         r_fact = 0.45;
143     elseif A(loop) <= 20
144         r_fact = 0.55;
145     elseif A(loop) <= 24
146         r_fact = 0.65;
147     elseif A(loop) <= 28
148         r_fact = 0.75;
149     elseif A(loop) <= 34
150         r_fact = 0.85;
151     elseif A(loop) <= 60
152         r_fact = 0.95;
153     elseif A(loop) <= 80 % 2um
154         r_fact = 1;
155     elseif A(loop) <= 180 % 3um
156         r_fact = 1.5;
157     elseif A(loop) <= 320 % 4um
```

```
158         r_fact  = 2;
159     elseif  A(loop) <= 500 % 5um
160         r_fact  = 2.5;
161     else
162         r_fact  = 2.5;
163     end
164
165     Rd_lo(loop) = 90 * r_fact;     % Simulate with Silvaco...
166     Rd_hi(loop) = 90 * r_fact;
167     Rd(loop) = (Rd_lo(loop) + Rd_hi(loop))./2;
168     % ----------------------------------------------------------
169
170     % ---------- DELAY AND FALLTIME CALCULATIONS -
171     % Calculating delay and falltime
172     gamma = sqrt((1i*w * d(loop)*L(loop)) * (1i*w * d(loop)*C(loop) +
            (1i*w*A(loop)*Cd_hi(loop))/(1+1i*w*Cd_hi(loop)*Rd_hi(loop))));
173     beta = imag(gamma);
174     delay_hi  = 1e12  * beta / w; % 1e12 factor converts from sec to ps
175
176     gamma = sqrt((1i*w * d(loop)*L(loop)) * (1i*w * d(loop)*C(loop) +
            (1i*w*A(loop)*Cd_lo(loop))/(1+1i*w*Cd_lo(loop)*Rd_lo(loop))));
177     beta = imag(gamma);
178     delay_lo  = 1e12  * beta / w; % 1e12 factor converts from sec to ps
179
180     ddelay(loop) = delay_lo - delay_hi;
181
182     T_diode = 2.6 * A(loop)*Cd(loop) * sqrt(Zcell(loop) * Rd(loop)/A(loop));
183     T_per = 0.7 * Zcell(loop) * (d(loop)*C(loop) + A(loop)*Cd(loop));
184
185     T_linear = 1e12 * sqrt(T_diode^2 + T_per^2);
186     falltime_out(loop) = sqrt((falltime_in(loop) - ddelay(loop))^2 + (T_linear)^2);
187     % ----------------------------------------------------------
188
189     % ---------- IMPEDANCE CALCULATIONS ---------
190     % Calculate Zavg
191     Zavg(loop) = sqrt(1i*w*d(loop)*L(loop) / (1i*w*d(loop)*C(loop) +
            ((1i*w*A(loop)*Cd(loop))/(1+1i*w*Cd(loop)*0.5*Rd(loop)))));
```

```
192     % Calculate Zhi
193     Zhi(loop) = sqrt(1i*w*d(loop)*L(loop) / (1i*w*d(loop)*C(loop) +
            ((1i*w*A(loop)*Cd_hi(loop))/(1+1i*w*Cd_hi(loop)*0.5*Rd_hi(loop)))));
194     % Calculate Zlo
195     Zlo(loop) = sqrt(1i*w*d(loop)*L(loop) / (1i*w*d(loop)*C(loop) +
            ((1i*w*A(loop)*Cd_lo(loop))/(1+1i*w*Cd_lo(loop)*0.5*Rd_lo(loop)))));
196     % ----------------------------------------
197
198     % ---------- ATTENUATION CALCULATIONS ------
199
200     atten_V(loop) = R(loop)*d(loop)/(2*Zcell(loop)) + 2 * pi^2 * floss^2 * A(loop) *
            Cd(loop)^2 * Rd(loop) * Zcell(loop);
201     atten_total = atten_total + 8.686*atten_V(loop);
202
203     % ----------------------------------------
204 end
205
206 % ---------- WRITE TO EXCEL FILE ----------------
207 % <removed for brevity>
208 % ---------- / WRITE TO EXCEL FILE --------------
```

B.2 Generate NLTL Layout

Generates LayoutEditor macro to draw structure of NLTL, pulling values from spreadsheet.

```
% Layout Editor macro generator

% This script produces a macro which generates the cell structure and basic
% layout of the NLTL.

numCells = 100;

w = xlsread('Quartz NLTL.xlsx', 1, ['B7:B' num2str(numCells+6)]).*1e3;
g = xlsread('Quartz NLTL.xlsx', 1, ['C7:C' num2str(numCells+6)]).*1e3;
d = xlsread('Quartz NLTL.xlsx', 1, ['Q7:Q' num2str(numCells+6)]).*1e3;
A = xlsread('Quartz NLTL.xlsx', 1, ['R7:R' num2str(numCells+6)]).*1e6;

f = fopen('LayoutMacro.layout', 'w');

fprintf(f, '#!/Program Files (x86)/layout\n');
fprintf(f, '#name=NLTL Cell Generation\n');
fprintf(f, '#help=Generates the CPW cells for an NLTL\n\n');
fprintf(f, 'int main(){\n\n');

dd = zeros(size(d),1);

actualCell = zeros(size(d),1);

for cell = 1:numCells

    if cell == 1
        activeCell = 1; % if cell is repeated, this is first cell
    end


    if cell == 1 || A(cell) ~= A(cell-1)
        % check that current cell is NOT a repeat of previous cell
```

```
33          activeCell = cell;
34
35  % START CELL CONSTRUCTION ----------------------
36
37      % Determine the diode width based off CPW geo & diode area
38      if w(cell) == 20e3
39          if A(cell) < (2 * 4 * 15.6)*1e6
40              diode_width = 4e3;
41          elseif A(cell) < (2 * 6 * 15.6)*1e6
42              diode_width = 6e3;
43          else
44              diode_width = 8e3;
45          end
46
47      elseif w(cell) == 12e3
48          if A(cell) < (2 * 2 * 12)*1e6
49              diode_width = 2e3;
50          elseif A(cell) < (2 * 3 * 12)*1e6
51              diode_width = 3e3;
52          elseif A(cell) < (2 * 4 * 12)*1e6
53              diode_width = 4e3;
54          else
55              diode_width = 5e3;
56          end
57
58      else      % w(cell) == 6
59          diode_width = 2e3;
60      end
61      % END diode_width
62
63      % Extend cell length to account for diode width
64      if w(cell) == 12e3
65          cell_extension = diode_width + 2e3;
66      elseif w(cell) == 6e3
67          cell_extension = diode_width + 2e3;
68      else
69          cell_extension = diode_width + 2e3;
```

```
70      end
71      d(cell) = d(cell) + cell_extension;
72
73      w1 = w(cell);
74      w2 = w(cell);
75      g1 = g(cell);
76      g2 = g(cell);
77
78      fprintf(f, 'string cellname="CPW%d";\n', cell);
79      fprintf(f, ' cellList *cl=layout->drawing->addCell();\n');
80      fprintf(f, 'cl->thisCell->cellName = cellname;\n');
81      fprintf(f, 'layout->drawing->setCell(cellname);\n');
82      fprintf(f, 'layout->drawing->activeLayer=15;\n'); % air bridge
83      % Conductor
84      fprintf(f, 'layout->drawing->point(%d,0);\n', -w1/2);
85      fprintf(f, 'layout->drawing->point(%d,%d);\n', -w2/2,d(cell));
86      fprintf(f, 'layout->drawing->point(%d,%d);\n', w2/2,d(cell));
87      fprintf(f, 'layout->drawing->point(%d,0);\n', w1/2);
88      fprintf(f, 'layout->drawing->polygon();\n');
89
90      % Shorten ground so the diode can just slot in
91      if w(cell) == 20e3
92          ohmic_width = 12.5e3;
93          shorten = 12.5e3 * 2 + diode_width;
94          gnd_w = 20e3;
95      elseif w(cell) == 12e3
96          ohmic_width = 12.5e3;
97          shorten = 12.5e3 * 2 + diode_width; %update diode cell
98          gnd_w = 15e3;
99      else
100         ohmic_width = 12.5e3;
101         shorten = 12.5e3 * 2 + diode_width; %update diode cell
102         gnd_w = 10e3;
103     end
104
105     if d(cell) > 80e3
106         % Extra AirPost to support bridge
```

```
107         post_location = d(cell)/2 + ohmic_width + diode_width/2;
108         post_width = 1.5e3;
109         fprintf(f, 'layout->drawing->activeLayer=14;\n'); % air post
110         fprintf(f, 'layout->drawing->point(%d,%d);\n', -post_width,
                post_location-post_width);
111         fprintf(f, 'layout->drawing->point(%d,%d);\n', post_width,
                post_location+post_width);
112         fprintf(f, 'layout->drawing->box();\n');
113     end
114
115     fprintf(f, 'layout->drawing->activeLayer=15;\n'); % air bridge
116     % Bottom ground
117     fprintf(f, 'layout->drawing->point(%d,%d);\n', -w1/2-g1-gnd_w, shorten);
118     fprintf(f, 'layout->drawing->point(%d,%d);\n', -w2/2-g2-gnd_w,d(cell));
119     fprintf(f, 'layout->drawing->point(%d,%d);\n', -w2/2-g2,d(cell));
120     fprintf(f, 'layout->drawing->point(%d,%d);\n', -w1/2-g1, shorten);
121     fprintf(f, 'layout->drawing->polygon();\n');
122     % Top ground
123     fprintf(f, 'layout->drawing->point(%d,%d);\n', w1/2+g1+gnd_w, shorten);
124     fprintf(f, 'layout->drawing->point(%d,%d);\n', w2/2+g2+gnd_w,d(cell));
125     fprintf(f, 'layout->drawing->point(%d,%d);\n', w2/2+g2,d(cell));
126     fprintf(f, 'layout->drawing->point(%d,%d);\n', w1/2+g1, shorten);
127     fprintf(f, 'layout->drawing->polygon();\n');
128
129     apo = 1e3;   % air post offset from airbridge for interconnects
130
131     fprintf(f, 'layout->drawing->activeLayer=14;\n'); % air post
132     % Bottom ground
133     fprintf(f, 'layout->drawing->point(%d,%d);\n', -w1/2-g1-gnd_w-apo, shorten);
134     fprintf(f, 'layout->drawing->point(%d,%d);\n', -w2/2-g2-gnd_w-apo,d(cell));
135     fprintf(f, 'layout->drawing->point(%d,%d);\n', -w2/2-g2+apo,d(cell));
136     fprintf(f, 'layout->drawing->point(%d,%d);\n', -w1/2-g1+apo, shorten);
137     fprintf(f, 'layout->drawing->polygon();\n');
138     % Top ground
139     fprintf(f, 'layout->drawing->point(%d,%d);\n', w1/2+g1+gnd_w+apo, shorten);
140     fprintf(f, 'layout->drawing->point(%d,%d);\n', w2/2+g2+gnd_w+apo,d(cell));
141     fprintf(f, 'layout->drawing->point(%d,%d);\n', w2/2+g2-apo,d(cell));
```

```
142     fprintf(f, 'layout->drawing->point(%d,%d);\n', w1/2+g1-apo, shorten);
143     fprintf(f, 'layout->drawing->polygon();\n');
144
145     % Schottky contact & inset  dielectric / airpost
146     dpi = 0.4e3;      % dielectric / post inset
147     %cr = 0.6e3;     % corner radius
148     cr = 0;     % corner radius
149
150     corner_area = pi * cr^2;
151     rect_area = 2 * cr * (diode_width-2*cr);
152     end_area = corner_area + rect_area;
153     effective_area = A(cell) - end_area;
154     sel = effective_area / diode_width / 2; % schottky effective length (without edge
            rounding)
155     sel = 1e2 * round(sel*1e-2);
156     sw = diode_width;
157
158     % Draw Schottky polygons
159         fprintf(f, 'layout->drawing->activeLayer=12;\n'); % Schottky layer
160         fprintf(f, 'layout->drawing->point(%d,%d);\n', 0, 0);
161         fprintf(f, 'layout->drawing->point(%d,%d);\n', cr+sel+cr, -sw);
162         fprintf(f, 'layout->drawing->box();\n');
163
164     % Draw airbridge polygons
165         fprintf(f, 'layout->drawing->activeLayer=15;\n'); % airbridge layer
166         fprintf(f, 'layout->drawing->point(%d,%d);\n', 0, 0);
167         fprintf(f, 'layout->drawing->point(%d,%d);\n', cr+sel+cr, -sw);
168         fprintf(f, 'layout->drawing->box();\n');
169
170     % Draw dielectric polygons
171         fprintf(f, 'layout->drawing->activeLayer=16;\n'); % dielectric layer
172         fprintf(f, 'layout->drawing->point(%d,%d);\n', cr + dpi, -cr-dpi);
173         fprintf(f, 'layout->drawing->point(%d,%d);\n', cr+sel+cr - dpi, -sw+cr+dpi);
174         fprintf(f, 'layout->drawing->box();\n');
175
176     % Draw airpost polygons
177         fprintf(f, 'layout->drawing->activeLayer=14;\n'); % airpost layer
```

```
178             fprintf(f, 'layout->drawing->point(%d,%d);\n', cr + dpi, -cr-dpi);
179             fprintf(f, 'layout->drawing->point(%d,%d);\n', cr+sel+cr - dpi, -sw+cr+dpi);
180             fprintf(f, 'layout->drawing->box();\n');
181         end
182
183         actualCell(cell) = activeCell;
184
185     % END CELL CONSTRUCTION ------------------
186     end
187
188         fprintf(f, 'string cellname="NLTL";\n');
189         fprintf(f, ' cellList *cl=layout->drawing->addCell();\n');
190         fprintf(f, 'cl->thisCell->cellName = cellname;\n');
191         fprintf(f, 'layout->drawing->setCell(cellname);\n');
192         yPoint = 0;
193
194         for cell = 1:numCells
195             fprintf(f, 'string cellname="NLTL";\n');
196             fprintf(f, 'layout->drawing->setCell(cellname);\n');
197             fprintf(f, 'point p;\n');
198             fprintf(f, 'p.setY(%d);\n', yPoint);
199             fprintf(f, 'p.setX(0);\n');
200             fprintf(f, 'string cellname="CPW%d";\n', actualCell(cell));
201             fprintf(f, ' cell *cellToInsert=layout->drawing->findCell(cellname);\n');
202             fprintf(f, 'element *e=cl->thisCell->addCellref(cellToInsert,p);\n');
203             yPoint = yPoint + d(actualCell(cell));
204         end
205
206         fprintf(f, '}\n');
207         fclose(f);
208         winopen('LayoutMacro.layout');
```

Appendix C

Fabrication Process

Alignment Marks		
Clean	Degrease	ACE/IPA, 5 min ultrasonic
Litho	Pre Bake	110°C, 60s
	Spin PR	5214e, recipe 6 (4k, 1.4μm)
	Soft Bake	110°C, 60s
	Expose	Stepper 'align' 60ms
	IR Bake	120°C, 60s
	Expose	MA6 flood expose, 60s
	Develop	300MIF, 40s
P Etch	Descum	790ICP/100300O2, 30s
P Etch	Etch	770ICP/GaAsVW1, 60s
Strip	Strip	1165 at 75°C/ultrasonic
P Etch	Descum	790/50250O2 if needed

Ohmic Contact		
Strip	Degrease	ACE/IPA, 5 min ultrasonic
Litho	Pre Bake	110°C, 60s
	Spin PR	5214e, recipe 6 (4k, 1.4μm)
	Soft Bake	110°C, 60s
	Expose	Stepper 'ohmic' 200ms
	Develop	AZ 300MIF, 50s
	Flood	MA flood expose, 10s
	Hard Bake	120°C, 60s (after 10 min delay)
P Etch	Descum	790/100300O2, 30s
Measure	Profilometer	PR thickness
W Etch	Oxide	NH4OH:H2O (1:20), 10s
W Etch	GaAs Etch	(H3PO4 / 4 H2O2 / 45 H2O), 90s, 400nm
Measure	Profilometer	PR + etch thickness
W Etch	Oxide	NH4OH:H2O (1:20), 30s
Deposit	Evap	Ge/Au/Ge/Au/Ni/Ti/Au (110/100/60/240/500/1600 Å)
Strip	Lift off	ACE 2 hrs, lift off, 1165 to descum
P Etch	Descum	790ICP/50250O2 as needed
W Etch	Oxide	NH4OH:H2O (1:20), 30s
RTA	Anneal	400°C, 60s recipe S400_60F (use susceptor)

Schottky Contact		
Strip	Degrease	ACE/IPA, 5 min ultrasonic
Litho	Pre Bake	110°C, 60s
	Spin PR	5214e, recipe 8 (3k, 1.7μm)
	Soft Bake	110°C, 60s
	Expose	Stepper 'schottky' 60ms
	IR Bake	120°C, 60s
	Expose	MA6 flood expose, 60s
	Develop	300MIF, 40s
P Etch	Descum	790ICP/50250O2, 30s
W Etch	Oxide	NH4OH:H2O (1:20), 30s
Deposit	Evap	30nm Ti / 18nm Pt / 300nm Au
Strip	Lift off	ACE 2 hrs, lift off, 1165 to descum

Isolation ICP Etch		
Strip	Degrease	ACE/IPA, 5 min ultrasonic
Litho	HMDS	Prebake 110°C then HMDS
	Pre Bake	110°C, 60s
	Spin PR	5214e, recipe 6 (4k, 1.4µm)
	Soft Bake	110°C,60s
	Expose	Stepper 'iso' 220ms
	Develop	AZ 300MIF, 60s
	Flood	MA flood expose, 10s
	Hard Bake	120°C, 60s (after 10 min delay)
P Etch	Descum	790/100300O2, 30s
P Etch	GaAs	ICP GaAsVW1 recipe, (18 min, 1.6µm)
W Etch	GaAs	(H3PO4 / 4 H2O2 / 45 H2O), 60s, 250nm
W Etch	InGaP	(7 H3PO4 / HCl), (45s, 100nm)
Strip	Strip	1165 at 75°C/ultrasonic
P Etch	Descum	790/50250O2 if needed

Interconnect		
Strip	Degrease	ACE/IPA, 5 min ultrasonic
Litho	HMDS	Prebake 110°C then HMDS
	Pre Bake	110°C, 60s
	Spin PR	5214e, recipe 8 (3k, 1.7µm)
	Soft Bake	110°C, 60s
	Expose	Stepper 'cpw' 60ms
	Rev. Bake	120°C, 60s
	Expose	MA6 flood expose, 60s
	Develop	300MIF, 40s
P Etch	Descum	790/100300O2, 30s
Deposit	Evap	30nm Ti / 18nm Pt / 600nm Au
Strip	Lift off	ACE 2 hrs, lift off, 1165 to descum

Dielectric Passivation		
Strip	Degrease	ACE/IPA, 5 min ultrasonic
P Etch	Descum	790/50250O2, as needed
W Etch	Oxide	(NH4OH / 20 H2O), 30s
Deposit	PECVD	200nm Si3N4 (seed, dep), MultiSIN 10x120s

Dielectric Etch		
Strip	Degrease	ACE/IPA, 5 min ultrasonic
Litho	Pre Bake	110°C, 60s
	Spin PR	5214e, recipe 8 (3k, 1.7µm)
	Soft Bake	110°C, 60s
	Expose	Stepper 'nitride' 220ms, focus -1µm
	Develop	300MIF, 60s (agitate)
	Hard Bake	120°C, 60s
P Etch	Descum	790/100300O2, 30s
P Etch	Etch	790/CF4_40W, 2:15 min
Strip	Lift off	1165@75°C; 1165/ultrasonic
Strip	Strip	1165 at 75°C/ultrasonic
P Etch	Descum	790/100300O2 if needed

Plating (3um)		
Strip	Degrease	ACE/IPA, 5 min ultrasonic
Litho	HMDS	Prebake 110°C then HMDS
	Pre Bake	110°C, 60s
	Spin PR	5214e, recipe 1 (1.5k, 2.3µm)
	Soft Bake	110°C, 60s
	Expose	Stepper 'post' 700ms
	Develop	300MIF, 60s
	Hard Bake	130°C, 3 min
	Expose	MA6, 10s (then delay 10 min)
	Hard Bake	130°C, 3 min
P Etch	Descum	790/100300O2, 20s
Deposit	Sputter	70nm Ti / 35nm Au / <10nm Ti
Litho	Spin PR	AZ 12XP, recipe 1 (850rpm, 7µm)
	Soft Bake	100°C with 4 min ramp from 60°C
	Expose	Stepper 'plating' 300ms
	PE Bake	90°C, 60s
	Develop	300MIF, 60s
P Etch	Descum	790/100W_O2, 30s
P Etch	Ti Etch	790/Z01_TEMP for 1min
Plate	Electroplate	3 µm Au
Strip	Strip	Irrigate with ACE/IPA, rinse quickly
P Etch		770ICP/O2Clean, 10 mins (carrier only)
W Etch	PR Strip	770ICP/PRSTRIP3, 10+10 mins
P Etch	Au/Ti Etch	770ICP/GoldEtch2, 60s
Strip	Strip	AZ 400T @ 80°C for 1+ hr
Dry	CPD	Critical point dry
P Etch	Descum	790/100300O2, as needed

References

[1] Bründermann, Erik, Heinz-Wilhelm Hübers, and Maurice FitzGerald Kimmitt. 2012. *Terahertz Techniques*, vol. 151 of *Springer Series in Optical Sciences*. Berlin, Heidelberg: Springer Berlin Heidelberg.

[2] Shumyatsky, Pavel, and Robert R Alfano. 2011. Terahertz sources. *Journal of biomedical optics* 16(3):033001.

[3] van der Weide, D. W. 1994. Delta-doped Schottky diode nonlinear transmission lines for 480-fs, 3.5-V transients. *Applied Physics Letters* 65(7):881.

[4] Marsland, Robert A. 1990. *Gallium Arsenide Integrated Circuits for Measurement and Generation of Electrical Waveforms to 300 GHz*. Stanford University.

[5] Allen, S.T., U. Bhattacharya, and M.J.W. Rodwell. 1994. 725 GHz sampling circuits integrated with nonlinear transmission lines. In *52nd annual device research conference*, 61–62. IEEE.

[6] Ferrari, P., A. Jrad, J. W. Tao, and J. M. Duchamp. 2002. Design and SPICE simulations of lossy and dispersive nonlinear transmission lines driven by a step-like generator. *Microwave and Optical Technology Letters* 32(1):17–21.

[7] Birk, M., H. Kibbel, C. Warns, A. Trasser, and H. Schumacher. 1998. Picosecond shock wave generation using an all-silicon nonlinear transmission line. In *56th annual device research conference digest (cat. no.98th8373)*, 90–91. IEEE.

[8] Simion, S., G. Bartolucci, R. Marcelli, A. Muller, B. Szentpali, and F. Riesz. 1997. Nonlinear transmission lines on GaAs membranes for picosecond and

large amplitude shockwaves generation. In *1997 international semiconductor conference 20th edition. cas '97 proceedings*, vol. 2, 353–356. IEEE.

[9] Hwu, R.J. 1999. Theoretical analysis and FDTD simulation of GaAs nonlinear transmission lines. *IEEE Transactions on Microwave Theory and Techniques* 47(7): 1083–1091.

[10] Salameh, D., and D. Linton. 1999. Study of the effect of various parameters on nonlinear transmission-line (NLTL) performance. *IEEE Transactions on Microwave Theory and Techniques* 47(3):350–353.

[11] Jrad, A., P. Ferrari, C. Fuchs, A. Dominjon, J.W. Tao, B. Flechet, and G. Angenieux. 1998. A simple and systematic method for the design of tapered nonlinear transmission lines. In *1998 ieee mtt-s international microwave symposium digest (cat. no.98ch36192)*, vol. 3, 1627–1630. IEEE.

[12] Hwu, R.J. 1997. Full-wave analysis of picosecond pulse formation via GaAs nonlinear transmission lines. In *Proceedings of 1997 asia-pacific microwave conference*, 845–848. City Univ. Hong Kong.

[13] Salamh, D., and D. Linton. 1996. Nonlinear transmission line (NLTL) design as a pulse generator. In *Ieee mtt/ed/ap/leo societies joint chapter. united kingdom and republic of ireland section. 1996 2nd high frequency postgraduate student colloquium*, 7–10. IEEE.

[14] Allen, Scott Thomas. 1994. *Schottky Diode Integrated Circuits for Sub-millimeter-wave Applications*. University of California, Santa Barbara.

[15] Heinrich, W. 1993. Quasi-TEM description of MMIC coplanar lines including conductor-loss effects. *IEEE Transactions on Microwave Theory and Techniques* 41(1):45–52.

[16] Whitaker, J.F., T.M. Weller, and L.P.B. Katehi. 1994. Terahertz-bandwidth characteristics of coplanar transmission lines on low permittivity substrates. *IEEE Transactions on Microwave Theory and Techniques* 42(12):2399–2406.

[17] Alexandrou, S., and T.Y. Hsiang. 2005. Attenuation characteristics of coplanar waveguides at subterahertz frequencies. *IEEE Transactions on Microwave Theory and Techniques* 53(11):3281–3287.

[18] Schnieder, F., R. Doerner, and W. Heinrich. 1996. High-impedance coplanar waveguides with low attenuation. *IEEE Microwave and Guided Wave Letters* 6(3): 117–119.

[19] Hofschen, S., and I. Wolff. 1996. Simulation of an elevated coplanar waveguide using 2-D FDTD. *IEEE Microwave and Guided Wave Letters* 6(1):28–30.

[20] Champlin, K.S., and G. Eisenstein. 1978. Cutoff Frequency of Submillimeter Schottky-Barrier Diodes. *IEEE Transactions on Microwave Theory and Techniques* 26(1):31–34.

[21] van der Weide, D. W. 1994. Planar antennas for all-electronic terahertz systems. *Journal of the Optical Society of America B* 11(12):2553.

[22] Button, K.J. 1983. *Infrared and Millimeter Waves V10: Millimeter Components and Techniques, Part 2*. Elsevier Science.

[23] Kolberg, E.L., T.J. Tolmunen, M.A. Frerking, and J.R. East. 1992. Current saturation in submillimeter-wave varactors. *IEEE Transactions on Microwave Theory and Techniques* 40(5):831–838.

[24] Guen-Bouazza, A., C. Sayah, B. Bouazza, and N. E. Chabane-Sari. 2013. Steady-State and Transient Electron Transport within Bulk InAs, InP and GaAs: An Updated Semiclassical Three-Valley Monte Carlo Simulation Analysis. *Journal of Modern Physics* 04(05):616–621.

[25] Maloney, T. J., and Jeffrey Frey. 1977. Transient and steady-state electron transport properties of GaAs and InP. *Journal of Applied Physics* 48(2):781.

[26] Masselink, W T. 1989. Electron velocity in GaAs: bulk and selectively doped heterostructures. *Semiconductor Science and Technology* 4(7):503–512.

[27] Smith, P. M., M. Inoue, and Jeffrey Frey. 1980. Electron velocity in Si and GaAs at very high electric fields. *Applied Physics Letters* 37(9):797.

[28] Wuchenauer, T., and M. Birk. 2000. Doping profiles of Schottky diodes for nonlinear transmission lines. In *Proceedings 2000 ieee/ cornell conference on high performance devices (cat. no.00ch37122)*, 51–60. IEEE.

[29] Rodwell, Mark J. W. 1987. *Picosecond Electrical Wavefront Generation and Picosecond Optoelectronic Instrumentation*. Stanford University.

[30] Nagra, Amit S. 1999. *Varactor Based Technologies for the Tuning and Control of Microwave Circuits and Antennas*. University of California, Santa Barbara.

[31] Baca, Albert G., and Carroll I. H. Ashby. 2005. *Fabrication of GaAs Devices*. IET.

[32] IVEY, D. G, S. EICHER, S. WINGAR, and T. LESTER. 1997. Performance of PdâŁ“Ge based ohmic contacts to n-type GaAs. *Journal of Materials Science: Materials in Electronics* 8(2):63–68.

[33] Tiku, L. Luu-Henderson; L. Rushing, and S. 2006. Reduction of Platinum Metal Usage in GaAs IC Metallization. In *Cs mantech conference*, 137–140. Vancouver, British Columbia, Canada.

[34] Kang, Min-Gu, and Hyung-Ho Park. 2001. Interface-controlled Au/GaAs Schottky contact with surface sulfidation and interfacial hydrogenation. *Journal of Applied Physics* 89(9):5204.

[35] Seethalakshmi, I., Rashmi Joshi, Nandita Das Gupta, and Bijoy Krishna Das. 2014. Inductively Coupled Plasma Etching of GaAs with High Anisotropy for Photonics Applications. 681–683. Springer, Cham.

[36] Barnett, E. F. 1955. A New Precision X-Band Phase-Shifter. *IRE Transactions on Instrumentation* PGI-4(0):150–154.

[37] Sze, Simon M., and Kwok K. Ng. 2006. *Physics of Semiconductor Devices*.

[38] Fu, S.-L., T. P. Chin, M. C. Ho, C. W. Tu, and P. M. Asbeck. 1995. Impact ionization coefficients in (100) GaInP. *Applied Physics Letters* 66(25):3507.

[39] Schoen, K. J., E. S. Harmon, J. M. Woodall, and T. P. Chin. 1997. High voltage GaInP/GaAs dual-material Schottky rectifiers. *Applied Physics Letters* 71(4): 518.

[40] Hudait, M.K, and S.B Krupanidhi. 1999. Breakdown characteristics of MOVPE grown Si-doped GaAs Schottky diodes. *Solid-State Electronics* 43(12):2135–2139.

[41] Grossberg, M.A. 1968. Extremely rapid computation of the Klopfenstein impedance taper. *Proceedings of the IEEE* 56(9):1629–1630.

[42] Kadoya, Y. 2007. THz wave propagation on strip lines: Devices, properties, and applications. In *2007 19th international conference on applied electromagnetics and communications*, 1–4. IEEE.

[43] Ohkubo, T., M. Onuma, J. Kitagawa, and Y. Kadoya. 2006. Micro-strip-line-based sensing chips for characterization of polar liquids in terahertz regime. *Applied Physics Letters* 88(21):212511.

[44] Kasai, Shintaro, Akihiro Tanabashi, Kosuke Kajiki, Takeaki Itsuji, Ryoji Kurosaka, Haruko Yoneyama, Masatsugu Yamashita, Hiromasa Ito, and Toshihiko Ouchi. 2009. Micro Strip Line-Based On-Chip Terahertz Integrated Devices for High Sensitivity Biosensors. *Applied Physics Express* 2(6):062401.

[45] Laurette, S., A. Treizebre, F. Affouard, and B. Bocquet. 2010. Subterahertz characterization of ethanol hydration layers by microfluidic system. *Applied Physics Letters* 97(11):111904.

[46] Kitagawa, J., T. Ohkubo, M. Onuma, and Y. Kadoya. 2006. THz spectroscopic characterization of biomolecule/water systems by compact sensor chips. *Applied Physics Letters* 89(4):041114.

[47] Laurette, S, A Treizebre, and B Bocquet. 2011. Co-integrated microfluidic and THz functions for biochip devices. *Journal of Micromechanics and Microengineering* 21(6):065029.

[48] Onuma, M., T. Ohkubo, J. Kitagawa, and Y. Kadoya. 2006. THz Spectroscopic Performance Comparison between Micro-Strip-Line Based Sensing Methods and Attenuated Total Reflection. In *2006 joint 31st international conference on infrared millimeter waves and 14th international conference on teraherz electronics*, 466–466. IEEE.

[49] Kitagawa, J., S. Yanagi, M. Onuma, and Y. Kadoya. 2007. THz fingerprint spectra detected by sensor chips based on coplanar strip-lines made on low-permittivity plastic substrate.

[50] Tanabashi, A, S. Kasai, R. Kurosaka, H. Yoneyama, M. Yamashita, H. Ito, and T. Ouchi. 2007. High sensitive detection of biomolecules with integrated THz sensor chip.

[51] Frankel, M.Y., S. Gupta, J.A. Valdmanis, and G.A. Mourou. 1991. Terahertz attenuation and dispersion characteristics of coplanar transmission lines. *IEEE Transactions on Microwave Theory and Techniques* 39(6):910–916.